CPE 100 – Digital Logic Design I
Course Syllabus – Spring 2016

Instructor: Dr. Yacouba Moumouni

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Teaching Assistants (Tutors):

- Claire Tsagkari; email address: tsagari@unlv.nevada.edu ; Office TBE-B310; Office Hours Tue&Thurs 1- 4. ---- **Will spend 15hours/week in the tutoring center**-----
- Nima Mohseni; email mohseni@unlv.nevada.edu; Office TBE-B310. ---- **Will spend 15hours/week in the tutoring center**-----

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Prerequisites:

Textbook: Fundamentals of Logic Design, Charles H. Roth, Jr., and Larry L. Kinney, 7th edition

Rules Regarding Homework

- There will be a number of homework assignments.
- Homework assignments are expected to be turned in at the beginning of the class on the due dates.
- Put a box around your final answer.
- Each homework problem should start from a new page.
- Staple all your sheets together.
- Loose papers may not be accepted.
- No late homework will be accepted.
- However, late homework may be accepted for full credit if and only if illness or truly urgent business interferes with the schedule of the course. Please make arrangements in advance.
- Homework turned in without procedures to arrive at final answers may receive no credits.
- Homework solutions will be posted after due date.
- Homework problems will not be discussed in class.
- However, you are welcome to clear doubts during office hours.
- Attendance is required in class.

Quizzes

- There will be 10 to 15 minutes quiz every two weeks. Students are advised to show their work for a full credit.
- **Calculators will not be allowed.**

Exams

- There will be three exams scheduled ahead of time.
- No make-up test/exam will be given under any circumstances. It is your responsibility to check the course website for all activities going on with this course. However, if the student presents convincing evidence for her/his absence on the exam day, s/he will be allowed to take the final with an additional weight equal to that of the mixed exam.

Grading policy

Test 1:	20%	Wednesday Feb. 24th
Test 2:	25%	Wednesday Mar. 16th
Final Exam	30%	Wednesday May 11th
Quizzes	15%	
Homework	10%	
Total	**100%**	

Grades are determined according to the following percentages (+/- sign may be used):
A: 90% - 100%, B: 76% - 89%, C: 60%-75%, D: 50%-59%, and F: <50%.

Cheating and Plagiarism

- Students are encouraged to discuss problems with each other. However, please do not copy homework. It is not going to help you in the long run.
- Any person caught cheating will be given an "F" grade for the course and reported to appropriate university officials.

Topics

Chapters 1-12 except 10

Syllabus Change Disclaimer

Information contained in this syllabus may be subjected to change with advance notice, as deemed appropriate by the instructor.

Yacouba Moumouni
January 19, 2016.

SHORT COURSE DESCRIPTION

CATALOG DATA

- Digital design concepts and fundamentals
- Combinational circuits
- MSI and LSI circuits
- Sequential machine fundamentals sequential circuit analysis and design
- Modern developments

COURSE OBJECTIVES

To gain knowledge on:

- Number systems and binary arithmetic, basics of switching algebra, simplification and minimization methods for Boolean functions
- Basic gates and simple integrated circuits that can be used for combinational network design
- Different types of flip-flops, basics of sequential network design

TOPICS

- Number systems and binary arithmetic
- Basics of switching algebra
- Simplification and minimization methods for Boolean functions
- AND, OR, NOT, NAND, NOR, EXOR gates as construction blocks for switching network design
- Medium scale integrated circuits that can be used for combinational network design
- Different types of flip-flops and their functionality
- Basics of sequential networks design
- Functionality of multiplexers, decoders, ROMs, PLAs, PALs, etc.

COURSE OUTCOMES

Upon completion of this course, students should be able to:

- Convert between number systems and perform binary arithmetic operations
- Simplify Boolean expressions and prove validity of equations
- Analyze and design combinatorial networks using basic gates
- Derive minterm and maxterm expansions for the functions given algebraically or by truth tables
- Design multi- and two-level NOR and NAND networks, including multi-output networks
- Design combinational networks using multiplexers, decoders and ROMs

- Construct timing diagrams for asynchronous and synchronous networks
- Design simple sequential circuits using flip-flops, etc.

Homework Assignments:

Reading Material:
Chapter 1
1.2, 1.3, and 1.4

Quizzes:
1. Wed. January 27th on "Number Systems and Conversion"