A CONTROL INTEGRATED CIRCUIT FOR A HYSTERETIC FLYBACK POWER CONVERTER

By

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Abstract

This Thesis reports the design, simulation, and layout of a switching power supply controller chip for a fly-back switching power supply. The controller chip was designed using ON's Semiconductor C5 process. The resulting switching power supply using the controller chip consists of using various off-chip components such as a power MOSFET, transformer, and capacitors. The main components used in the integrated circuit include a bandgap reference voltage circuit which outputs a reference voltage of 1.25V, a ring oscillator having a nominal frequency of 5MHz, a high-gain comparator, and a buffer that can drive a 5pF capacitor. Under normal simulation conditions the reference voltage was 1.25V, power supply voltage was 5V, a normal operating temperature of 27°C, and a load current of 2.5A which resulted in an output voltage of 12.5V with a 350mV ripple voltage caused by the control loop's hysteresis. The higher value of ripple in the output voltage was shown to be reduced with a larger, thus more expensive, filter capacitor. The output in this nominal case resulted in an average power consumption of the switching power supply of around 16mW while supplying more than 30W to the load. The Thesis reports additional simulation results including temperature being changed between 0°C to 100°C, the power supply voltage being changed away from the standard 5V, and the load current varying between 10mA and 6.25A. During all tests the integrated circuit performed well and under worst-case conditions an efficiency of above 89%.

Acknowledgements

Firstly, I would like to start off acknowledging and thanking Dr. R. Jacob Baker. Without him my experience at UNLV for my undergraduate and graduate studies would have not been the same. His dedication to his students made every class, conversation, and interaction with him worthwhile. Next, I would like to thank the rest of my Thesis Committee which is comprised of: Dr. Yahia Baghzouz, Dr. Biswajit Das, and Professor Xin Li. For their assistance in completing this process of defending my Thesis to earn my Graduate Degree. The Baker Group thank you to each and every one of you, especially Abraham Lopez. Abraham, thanks for the countless hours of studying that we did together and thank you for your friendship on this journey. Lastly, I would like to thank my family, who have always had the belief that I am extraordinary and can do anything that I set my mind to. I love you guys!

Dedication

To my mother, Jacqueline. There are not enough pages I could write or words that I can tell you to properly thank you, but here are some. Thank you for the countless sacrifices that you have made in order to put me in a better position. Thank you for your unwavering support and unconditional love. I hope that you are proud to be my mother. I am the man I am today thanks to you.

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Chapter 1: Introduction

1.1 Motivation

With the ubiquity of portable electronic the efficient supply and use of energy has become an important factor and consideration for consumers when purchasing phones, laptops, tablets, etc. It is quite desirable to have a battery, that is capable of powering electronic devices, that last for as long as possible. This can be achieved by low power design and ensuring that the power management integrated circuit (PMIC) runs efficiently. An efficient power management integrated circuit is one that does not dissipate power, which in this case is a battery that does not get warm. The PMIC is responsible for supplying various voltages to the components of a portable device [1]. This is accomplished using switching power supplies in the PMIC that utilizes various components such as: switches, inductors, transformers capacitors, and a feedback system.

There are two main ways to control a switching power supply one is Pulse Width Modulation and the other is hysteretic control. Pulse Width Modulation in a switching power supply results in a known switching frequency. There can be a significant issue with this approach because of the power involved. There also is radiated electromagnetic energy at the switching frequency along with harmonics. This radiation can electromagnetically interfere with the operation of other electronic devices, especially those that are controlled through a wireless connection. There is another approach when it comes to switching power supplies, which is hysteretic control. Hysteretic control is an approach where the clock frequency varies. This means that the electronic magnetic interference is spread out over a range and not at a particular moment. This means that this reduces the interference

with other electronic devices. There are also more added benefits to using hysteretic voltage controls such as faster response times, lower power dissipation by the control circuitry, and simpler design. As with all things in engineering there are also some drawbacks such that hysteresis causes a ripple voltage on the output and there is a need for hysteresis because if not the noise would dominate the output signal. This means that this can cause excess switching at higher frequencies, which is a major challenge when implementing hysteretic control loops.

1.2 Structure of Thesis

The contents of this Thesis include the theoretically calculated and simulated results relevant to the design and simulation of the proposed Thesis. This Thesis contains the design, simulation, and layout of the controller chip that is used for hysteretic power converters such as a flyback switching power supply. The Thesis will first begin with Chapter 1 which goes over the motivation and structure of the Thesis. Chapter 2 talks about the individual components that are needed for the controller chip that will be needed. In this chapter there are many calculations as to why certain information and values are picked. Later, in Chapter 3 the individual components will be interconnected to see how the final design will take place. Chapter 4 will talk about the data and the analysis. When talking about analysis the data is reviewed and visualized via tables and graphs. After analyzing the data, there might be opportunities to see where future work can improve upon the design. Chapter 5 is where the future work will be talked about in more detail. In this chapter the readers should see how the future work given more time will improve the design in both the individual components and the overall design. Lastly, Chapter 6 is the

conclusion where the proposed controller chip for hysteretic power converters and a conclusion is made. Following the conclusion there is a bibliography and a Curriculum Vitae.

Chapter 2: Components

2.1 Band Gap Reference Voltage

A bandgap voltage refence is a circuit used to generate a fixed voltage that is independent of the power supply voltage VDD, temperature, and process variations. This means that the output of the bandgap circuit needs to be at a fixed voltage. The bandgap circuit is a crucial element for the design of this Thesis because the reference voltage V(ref) needs to be equal to 1.25V. In this circuit the reference voltage needs to be less than that of the power supply voltage. The power supply voltage will be 5V for this Thesis. The bandgap is very important to the overall design because another component talked about later, the comparator needs a base voltage that does not change which comes from the bandgap circuit. This in turn makes so that the comparator circuit can output an appropriate voltage. The diodes found in this circuit exhibit a CTAT (Complementary to Absolute Temperature) behavior, where reference voltage increases with rising temperature. Due to this topology, there will be cascaded NMOS and PMOS devices in the diode branch which tries to keep the refence voltages at a constant value with a change in the voltage of VDD. This makes the design very robust.

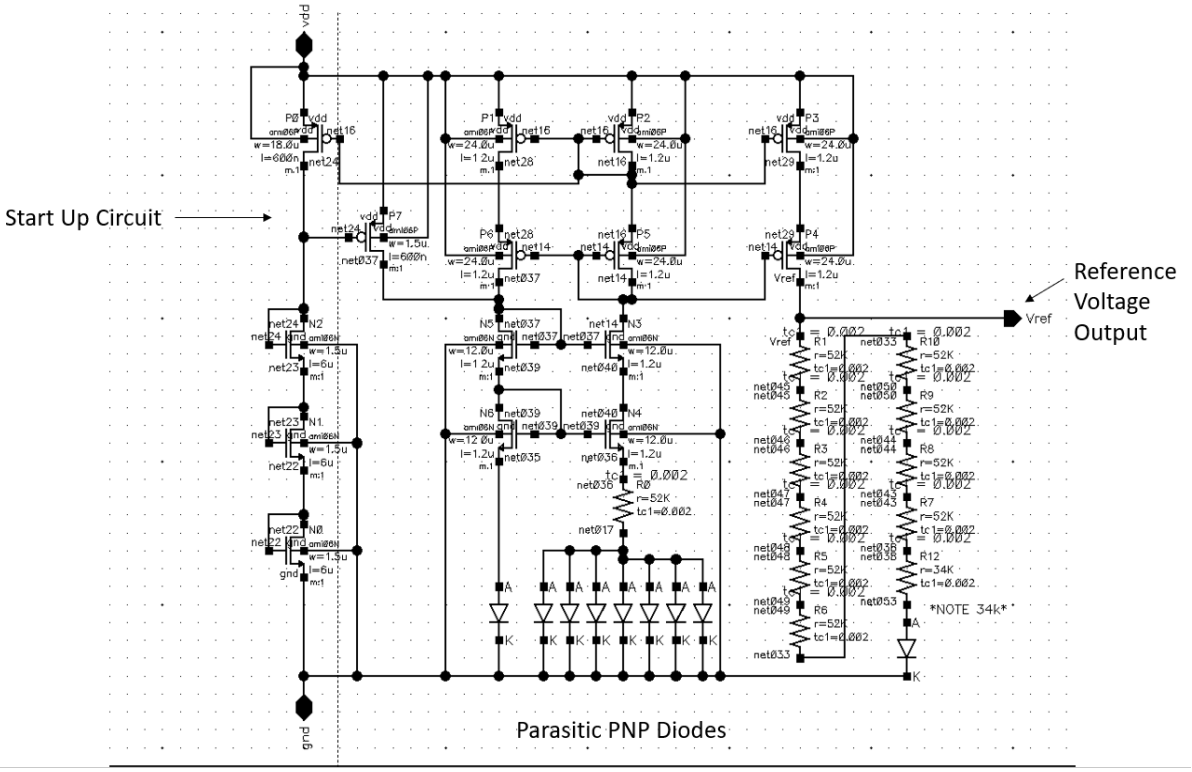

Figure 1 - Bandgap Schematic

As shown in the Figure above the bandgap schematic is made up of transistors, resistors, and parasitic PNP diodes. On the left hand of the dotted line is the startup portion of the circuit. On the lower half of the circuit many parasitic PNP diodes are found. On the right side there are a lot of resistors along with the output Vref, which is the reference voltage.

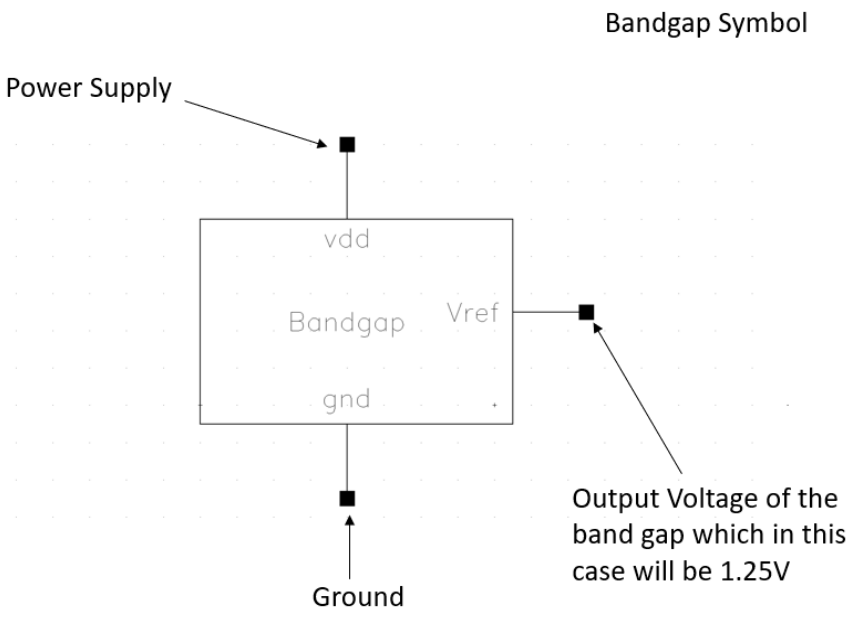

Figure 2 - Bandgap Symbol

The bandgap symbol is a concise view of the bandgap schematic that was previously featured. The bandgap symbol has three pins which are VDD, Vref, and gnd. The output of the bandgap should be constantly equal to 1.25V.

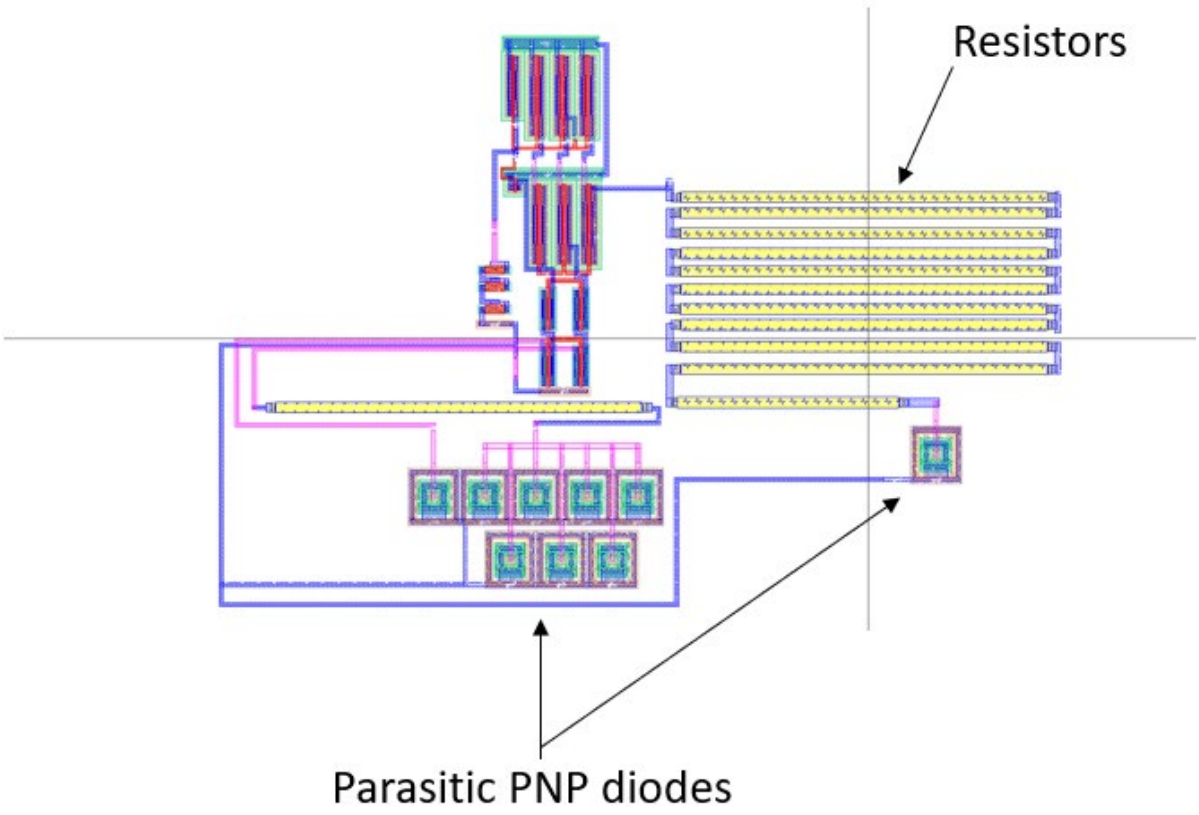

Figure 3 - Bandgap Layout

To make the layout of the bandgap easier, one approach is to break up the schematics and the layouts. After the schematics and layouts have been broken down then the user needs to make sure that the schematics and layouts DRS and LVS. Later, the

broken-down schematics and layouts need to be combined in order to make the final product, which in this case, is the bandgap layout.

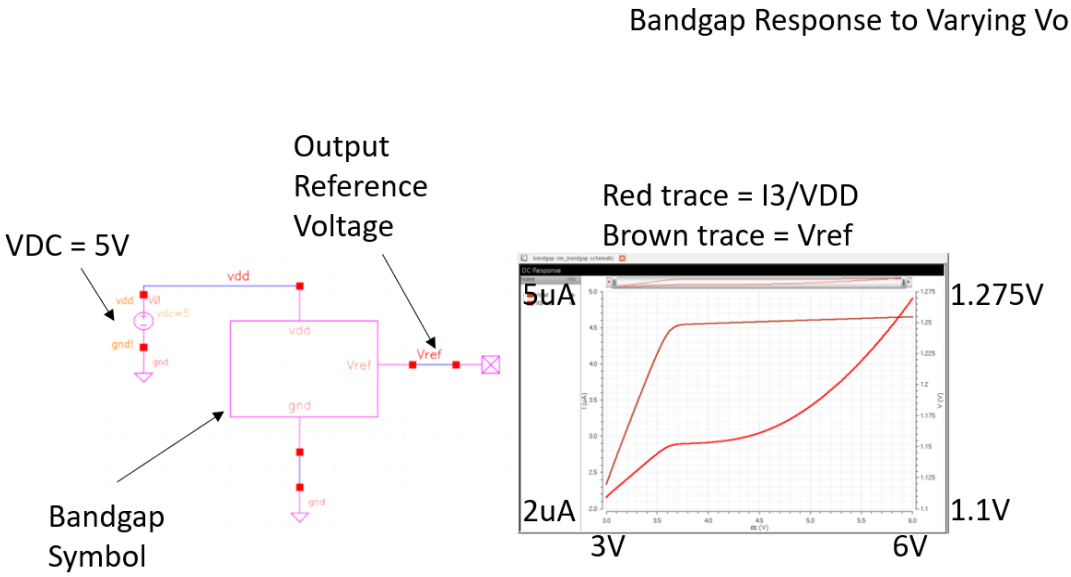

Figure 4 - Bandgap Response to Varying VDD Voltages

From testing the schematic above it is concluded that the power supply voltage can be lowered to around 3.7V before the bandgap output voltage drops. If the VDD voltage is less than 3.7V then the bandgap cannot function properly and stops working. As the bandgap gets swept 3.7V and greater voltages then the reference voltage starts at 1.25V and remains there as the simulation is being swept. The bandgap simulation shows that the

circuit draws between 3uA and 5uA of current, which means that this circuit is working efficiently because it does not draw large currents from the main power.

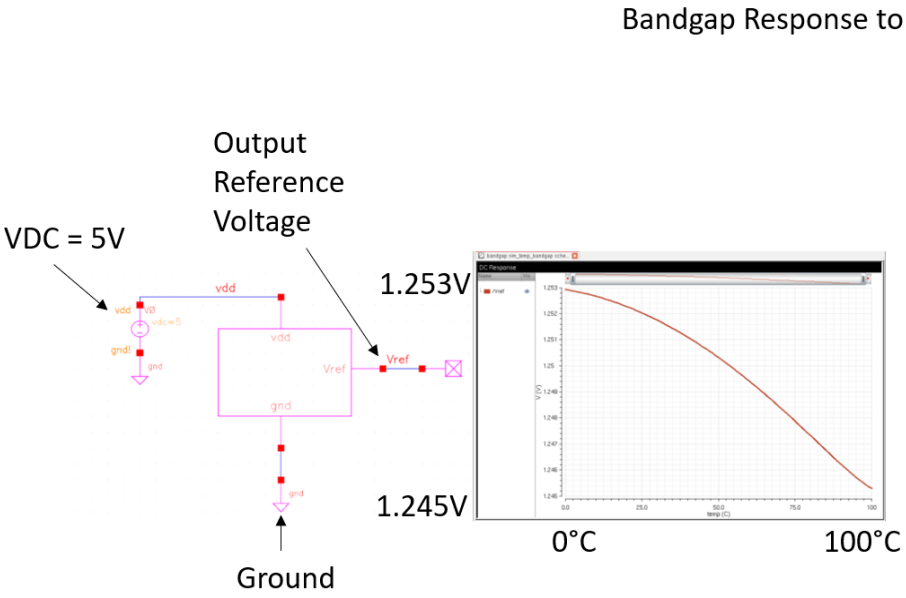

Figure 5 - Bandgap Response to Temperature

The bandgap refence voltage decreases from 1.253V to 1.245V with a temperature increase from 0 to 100 degrees Celsius. This is going to be a difference of 8mV which means that this is around 8 parts per million per degree Celsius. The average PTAT (proportional to absolute temperature) value for an N well resistor is 2000 parts per million per degree

Celsius. By comparing these two values it is concluded that the bandgap voltage refence will not vary much with changes in VDD and temperature. This is exactly the results that are desired because the bandgap circuit needs to maintain the same voltage.

Parasitic PNP diode response to varying diode voltage

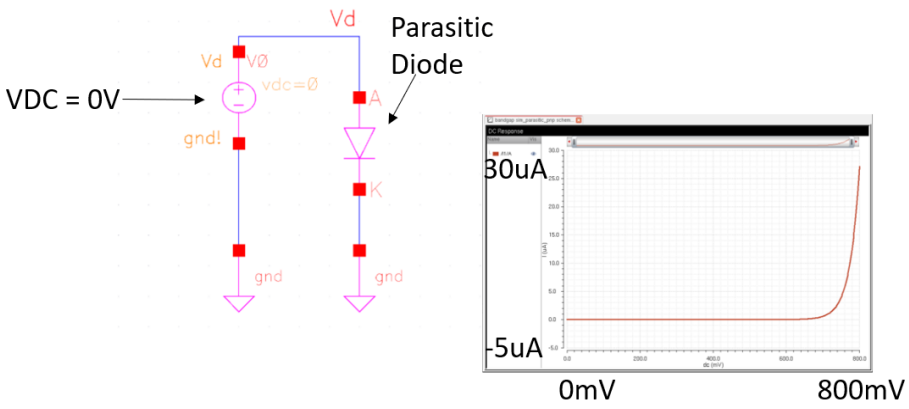

Figure 6 - Parasitic PNP Diode Response to Varying Diode Voltage

The PNP diode at the very least needs 700mV to start generating some current. When it does start generating current then a very low current of micro amps will happen. The threshold voltage of the PNP diode used in this Thesis is 700mV, therefore the voltage drops over the diode are 700mV.

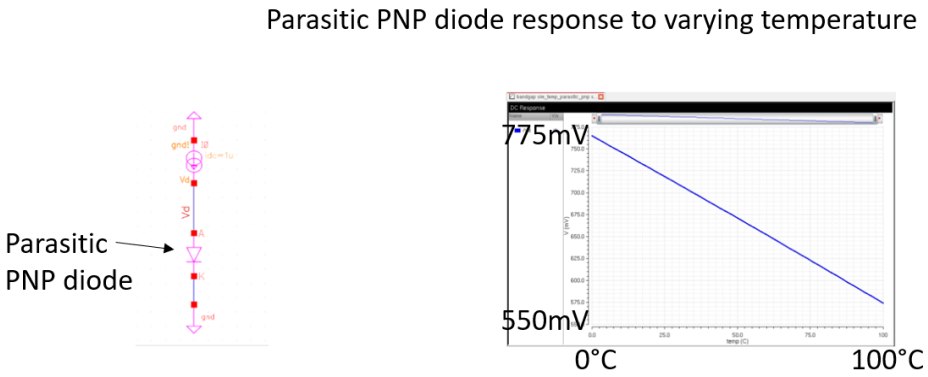

Figure 7 - Parasitic PNP Diode Response to Varying Temperature

Parasitic PNP voltage Vd goes from around 760mV at 0 degrees Celsius to 575 mV at 100 degrees Celsius. It can be deduced that the diode works better at lower temperatures and does not work as well at higher temperatures. Both the bandgap and the diode have negative linearity.

2.2 Comparator

A voltage comparator compares two voltages. After it compares two voltages it will output a Boolean value which will be either a 0 or a 1 depending on the state of the value. The state of the value is 0 if the state of the value is off/ low and the value is 1 if the state of the value is on/high. The comparator has two input terminals, which are the plus and

minus terminal which can be seen labeled in the symbol view as Vinp for Vin plus and Vinm for Vin minus. If the voltage on the Vinp terminal is greater than the Vinm terminal (Vinp>Vinm), then the comparator will output a high (1). If the voltage on the Vinp terminal is less than the Vinm terminal, then the comparator will output a low (0).

For this Thesis two comparator designs were in mind. The first design was a comparator with cascaded PMOS flavor buffer with a NMOS flavor buffer. This design was used first because by using buffers in parallel, the complementary nature results in a buffer that is robust, and works over a wide range of operating voltages. After running several simulations, the output never ended up reaching the desired 12.5V that was hypothesized. This means that the comparator did not have enough gain to reach the desired output voltage. The next design corrected the issue of not getting enough gain. The final design ended up using 3 NMOS flavor buffers cascaded with three inverters attached at the end. The design needs an odd number of inverters if not the Thesis will not work since an even number of inverters will just create a buffer. The use of inverters is needed so that the output has a cleaner result so that it squares the top of the output. The tradeoff for a cleaner result is the increase of power, this is because there are more devices that need to be powered on.

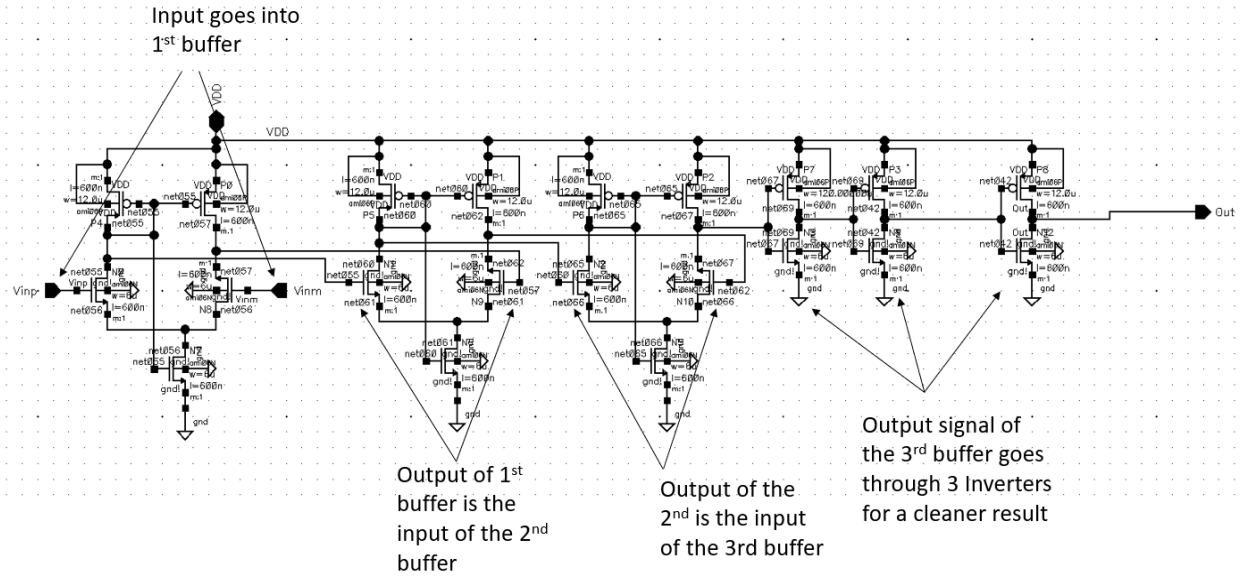

Figure 8 - Comparator Schematic

The comparator used in this Thesis has 3 n flavor buffers along with 3 inverters. The comparator needs to have three n flavor buffers to have a high enough gain to output 12.5V for the output. As seen from the Figure above the input goes into the first buffer then the output of the first buffer is the input to the second buffer, following this the output of the second buffer is the input to the third buffer. After the output of the third buffer the output signal is sent through 3 inverters for a sharper and cleaner output signal.

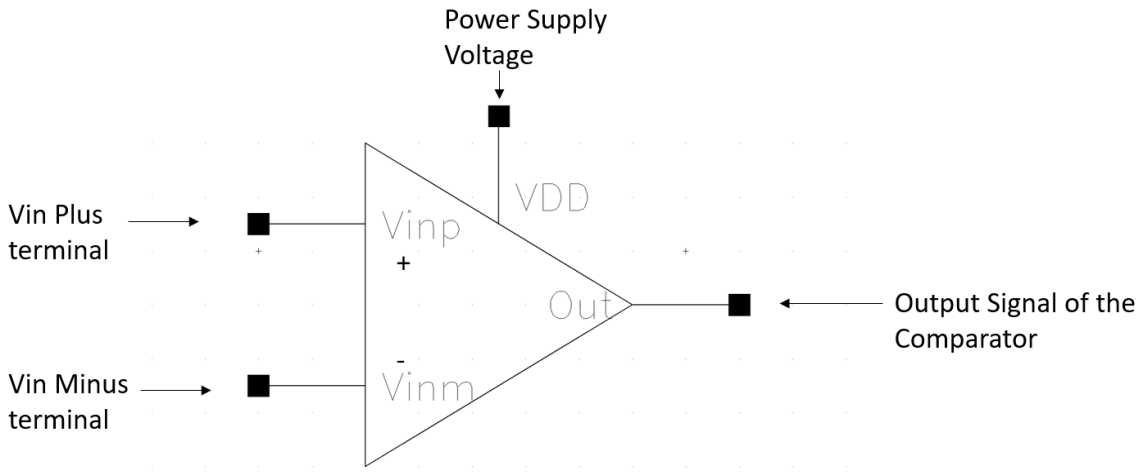

Figure 9 - Comparator Symbol

The comparator symbol simplifies the comparator schematic and only shows the pins that are needed. The comparator symbol has two input signals which are Vinp and Vinm, and one output signal terminal named out. In addition to the pins previously mentioned, the symbol also needs a power supply voltage.

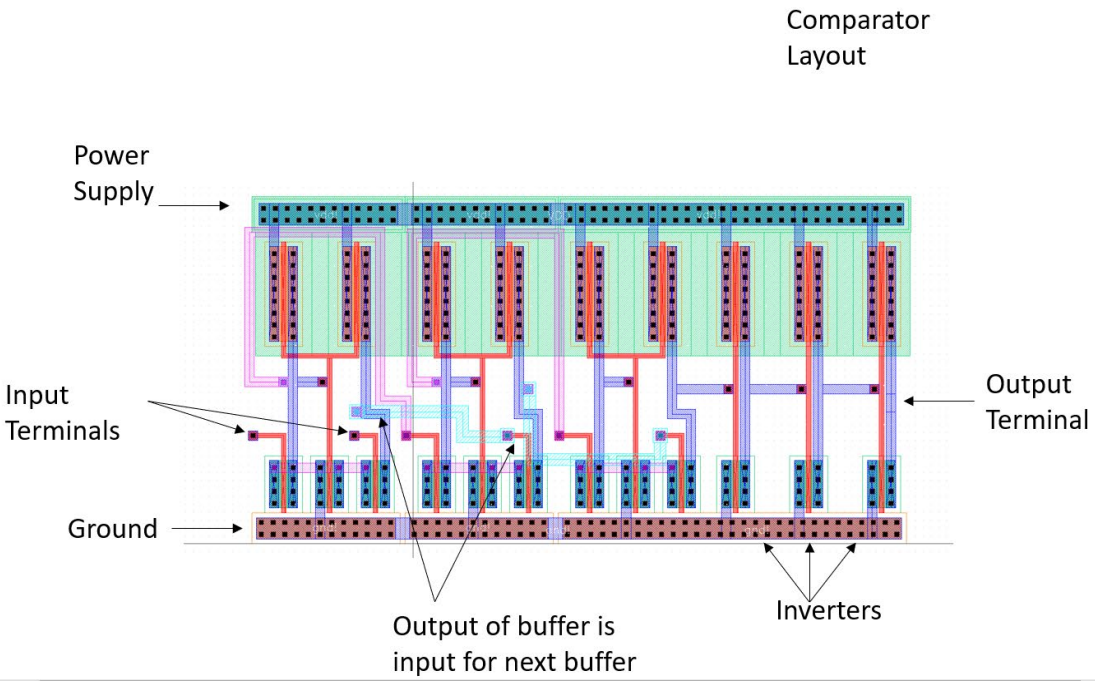

Figure 10 - Comparator Layout

The Figure above shows the layout of the comparator which features 3 n flavor buffers and 3 inverters. As seen from the schematic the output of the first buffer is the input of the second buffer and the output of the second buffer is the input of the third buffer. Later the output of the third buffer is sent through three inverters. The difficulty of this layout was not having the nets cross due to the gate design. To help with this issue there are vias and different metal layers used so that the nets were not crossed, and everything worked properly. Vias are metallic lined holes connected to metal circuitry of a chip between different layers. For example, there is a m1_m2 via to connect that signal from the metal 1 to the metal 2 layer

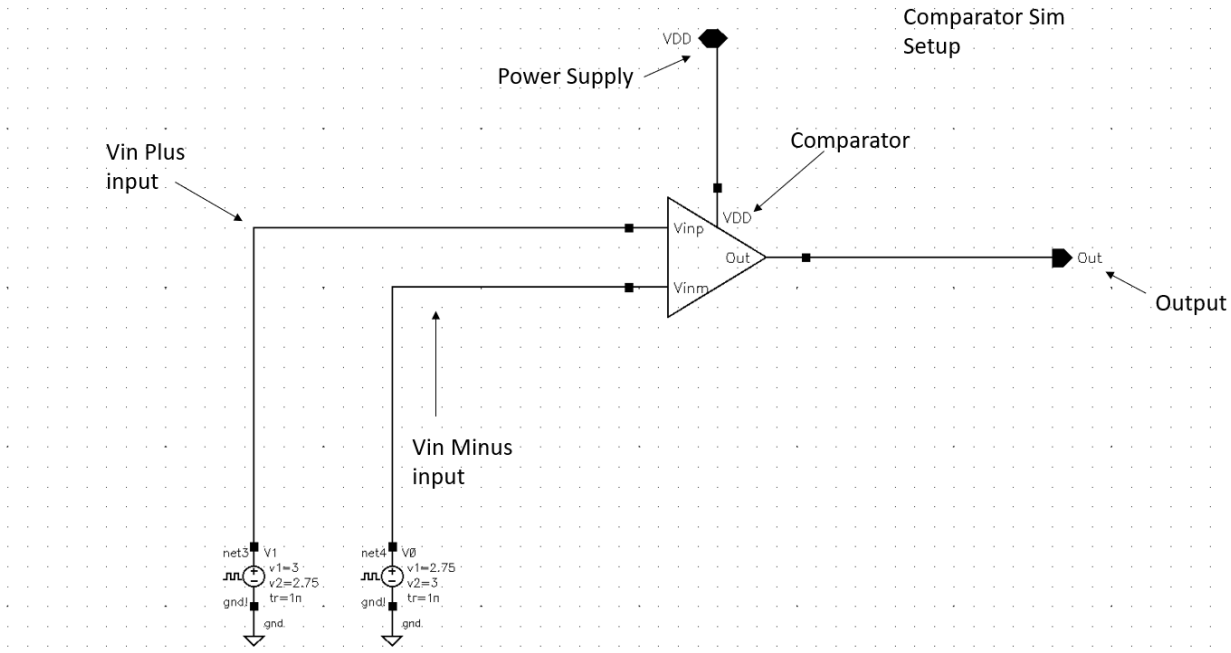

Figure 11 - Comparator Simulation Setup

In the Figure above it is showing the comparator simulation setup where the comparator symbol is laid out and there are two signals going into the input pins. The two input signals are pulse voltage sources that are alternating between being on and off. The top pin is the power supply and the pin on the right is the output signal of the comparator.

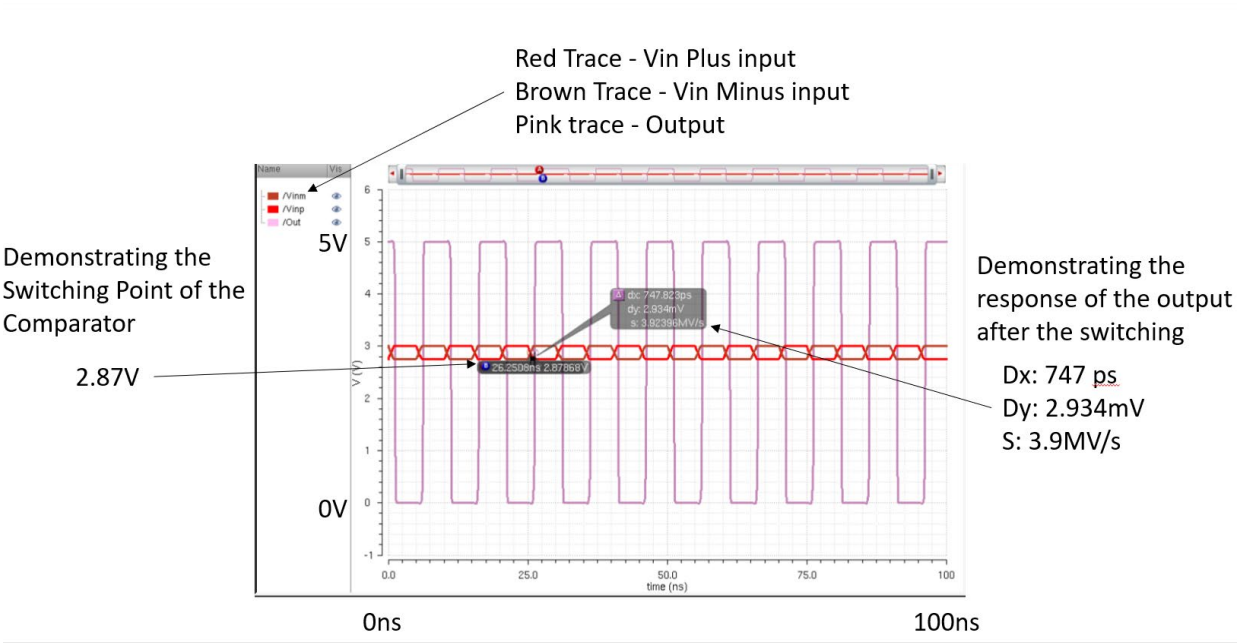

Figure 12 - Comparator Simulation

The Figure above shows a simulation of the comparator used where the switching points and the high/low values can be seen. The voltage switching point is when both input voltages are equal, which in this case is going to be 2.87V. The Red trace is the Vin Plus signal and the brown trace is the Vin Minus Terminal. The pink trace is the output signal. The pink trace shows that due to have cascading n flavor buffers that there is enough gain. Also, in the Figure above, it is showing the response of the output after the switching is being done. It takes 747ps after the switching happens for the output to respond.

2.3 Ring Oscillator

Design Equations

$$Rn = 20k * \left({}^{10.05u}/_{10.05u}\right) = 20k$$

$$Rp = 40k * \left({}^{10.05u}/_{10.05u}\right) = 40k$$

$$C_{ox} = 2.5\frac{fF}{um^2} * 10.05u * 10.05u = 252fF$$

$$252 + 252 + 378 + 378 = 1260fF$$

$$t_{plh}\ (Rp) = 0.7 * 40k * 1260fF = 35.3ns$$

$$t_{phl}\ (Rn) = 0.7 * 20k * 1260fF = 17.64ns$$

$$Total\ Time\ Delay = \ t_{plh} + \ t_{phl} = 35.3ns + 17.64ns = 52.94ns$$

$$f_{osc} = \frac{1}{n(t_{plh} + t_{phl})} = \frac{1}{(5 * 10^{6})(52.94 * 10^{-9})} = 3.7 \ \approx 4\ slow\ inverters$$

Four slow inverters are needed to achieve 5MHz.

According to the calculations the design was supposed to use 4 slow inverters to get the desired frequency of 5MHz, but when the four slow inverter design was simulated, the output was not the desired 5MHz. Therefore, more slow inverters were added to the get the desired frequency. The final design used 13 slow inverters (PMOS=10.05u/10.05u,

NMOS=10.05u/10.05u), one regular inverter 12u/6u, and one NAND gate so that it would be enabled.

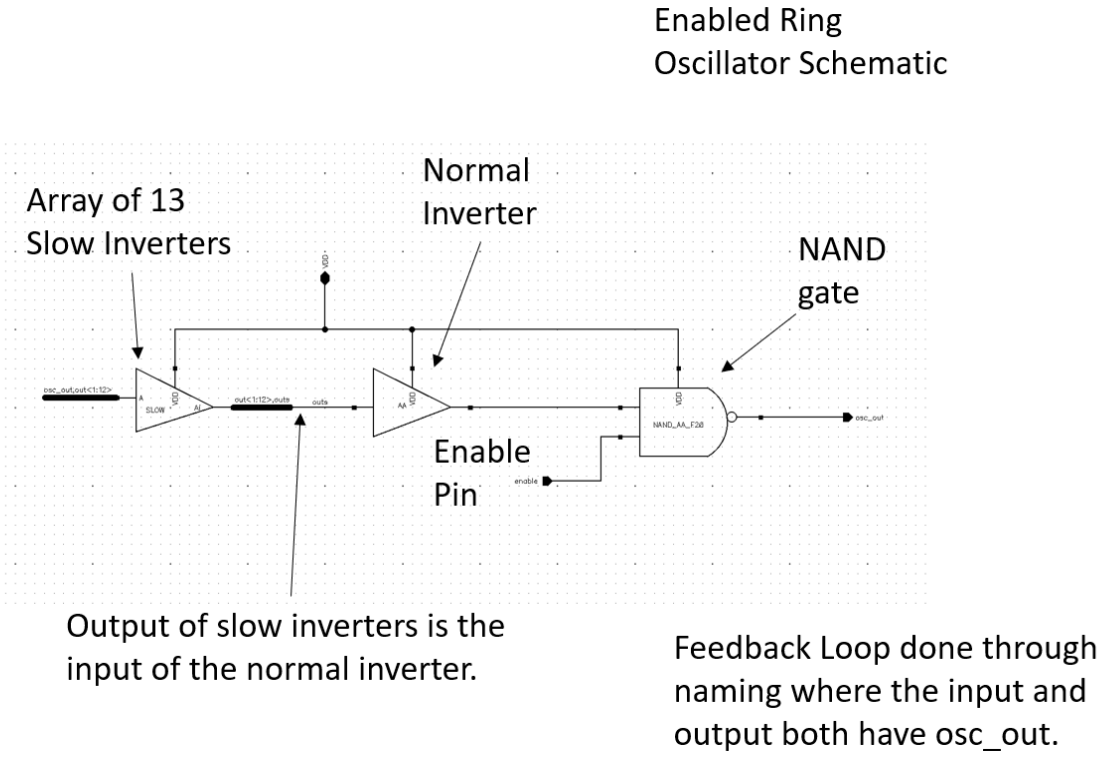

Figure 13 - Ring Oscillator Schematic

The schematic of the ring oscillator has three components which is the array of slow inverters, an inverter, and a NAND gate. The signal goes through the array of the slow inverters then the signal goes through the normal inverter. The array of slow inverter is

used to achieve the desired frequency. The normal inverter was used in order to clean up the signal. There is an even number of inverters because if not the NAND gate will not work with this design. The NAND gate is in the design so that it can shut off the signal when the flyback does hit the intended 12.5V. Also, it is closer to the end of the signal so that if it does shut off there is not a long delay. There is a feedback path through the pins. For the ring oscillator to function properly there needs to be an initial condition of 0V on the output so that it kicks on. There is a feedback loop in this circuit which in the Figure it highlights the fact that it is done by naming the loop with the signal osc_out.

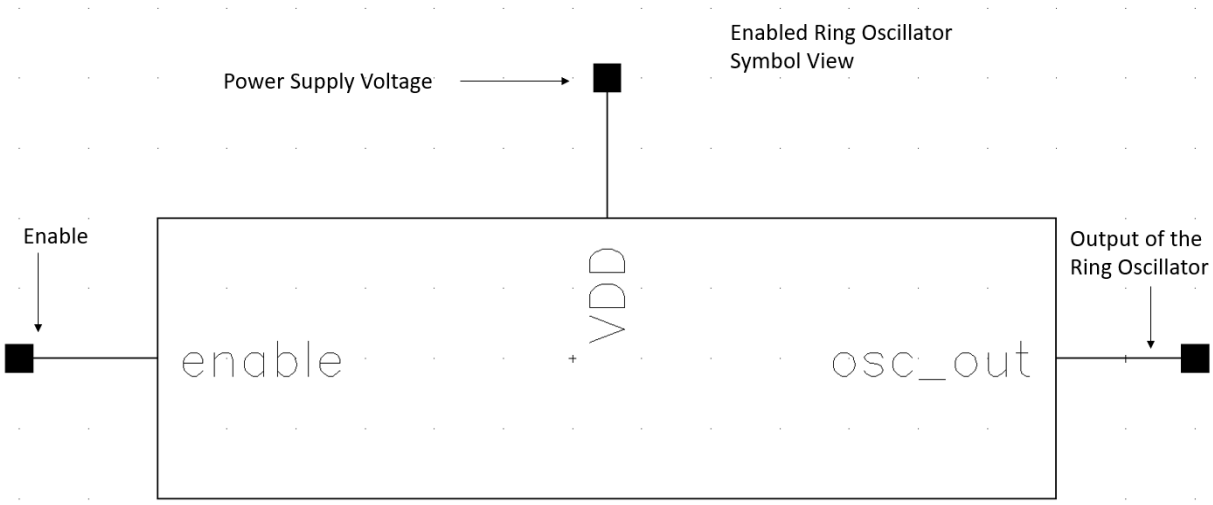

Figure 14 - Ring Oscillator Symbol

The ring oscillator symbol simplifies the ring oscillator schematic by putting the logic behind the symbol and just showing the symbol and the pins. The Figure above shows the ring oscillator symbol which has three pins that are an enable pin for an input, a VDD pin for power, and osc_out for an output.

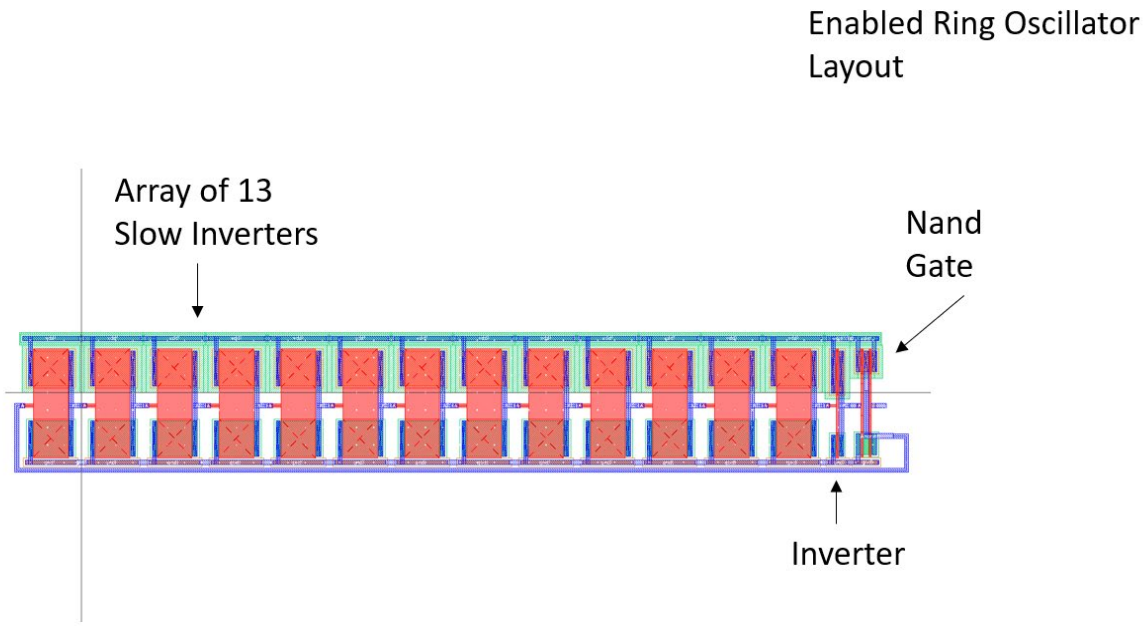

Figure 15 - Ring Oscillator Layout

The layout of the ring oscillator is above. The ring oscillator is rather long, but for further improvement it should be made in a serpentine pattern in order to save space. As it can be seen from the schematic and layout the input signal first goes through the array of

the thirteen slow inverters, later it goes through the inverter, and finally through the NAND gate. What is interesting is that although the NAND gate is at the end of the layout because of the enable it goes through the NAND gate first.

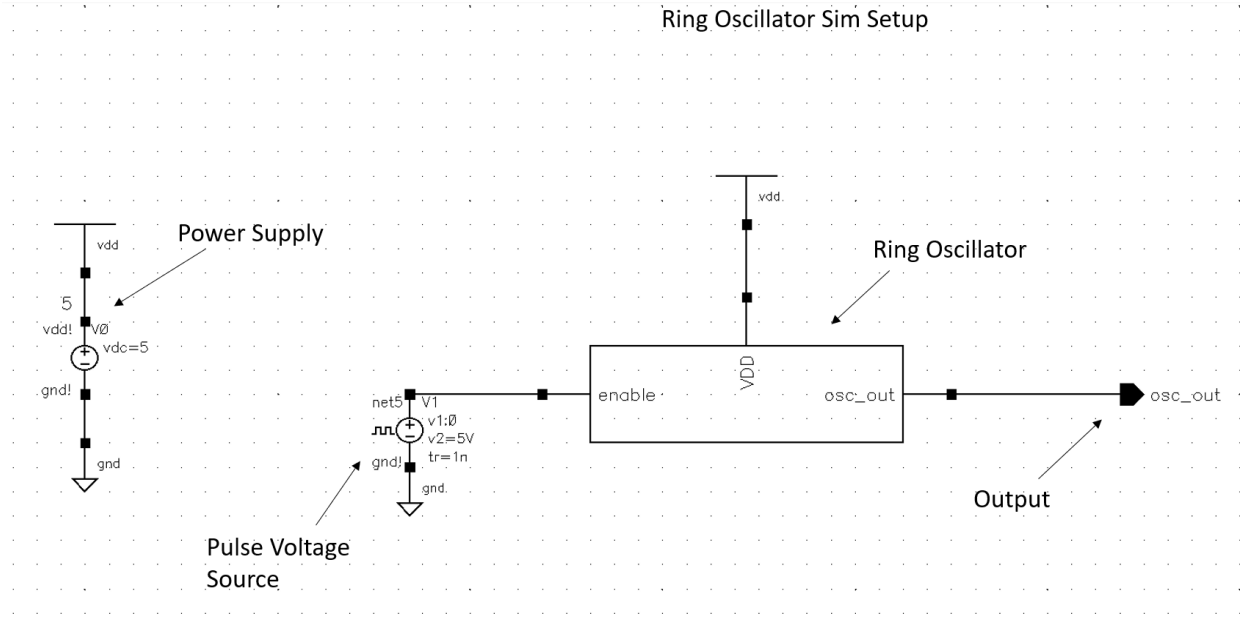

Figure 16 - Enabled Ring Oscillator Simulation Setup

This Figure is showing the simulation setup for the ring oscillator. The ring oscillator symbol is in view and all the pins are connected. The left pin which is the enable pin has a pulse voltage source, the top pin has the power supply voltage connected which is 5V, and the left pin is the osc_out pin.

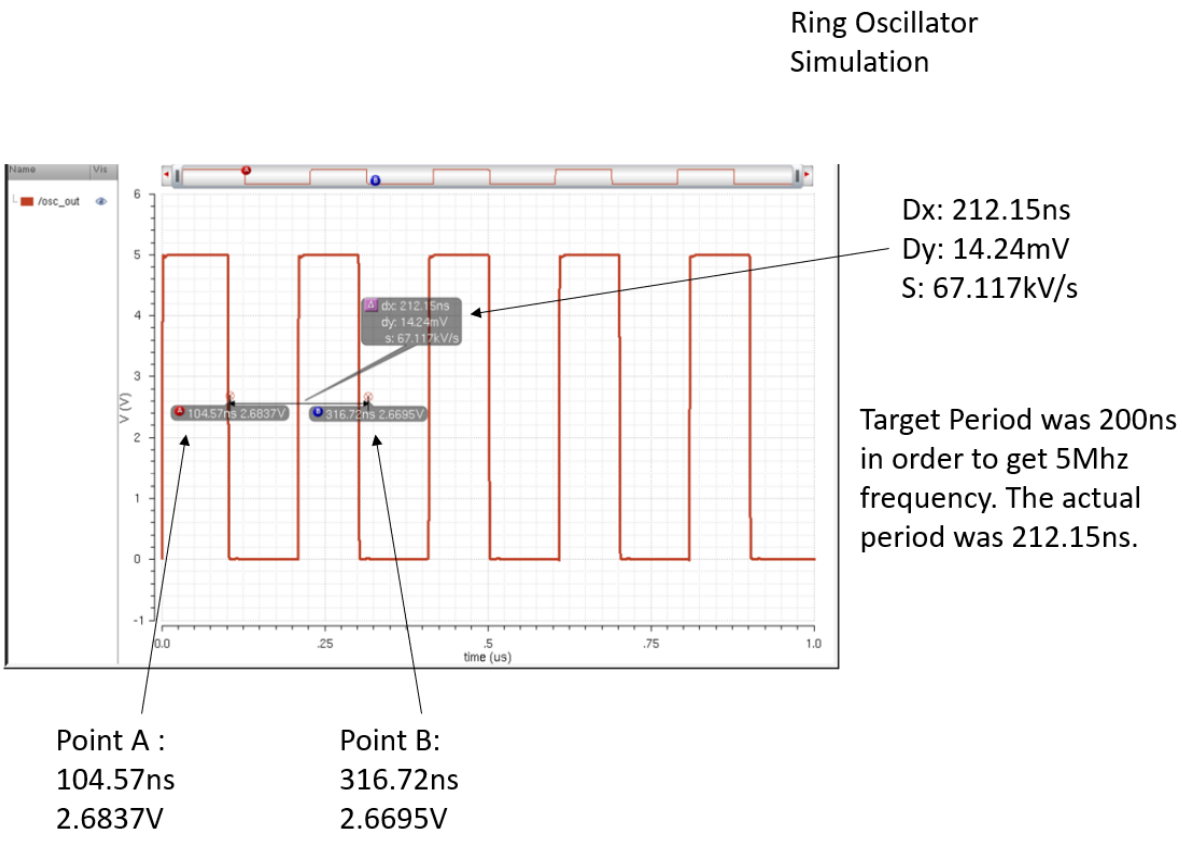

Figure 17 - Ring Oscillator Simulation

The target frequency for this Thesis is 5MHz. In order to achieve 5MHz the period must be 200ns. 1/200ns = 5MHz. The Figure above is showing that the ring oscillator is near the target frequency. In the Figure point A is located at 104.57ns and that point b is located at 316.72ns. This means that the difference between these points are 212ns. The difference of 212ns can be interpreted as the period of this circuit. So instead of the target 1/200ns = 5MHz, the actual value of the circuit based off of the simulations is 1/212ns =

4.7MHz. This is acceptable because of how close it is. What can also be seen through this simulation is that there is not too much delay on the edges of the output.

2.3.1 Slow Inverter

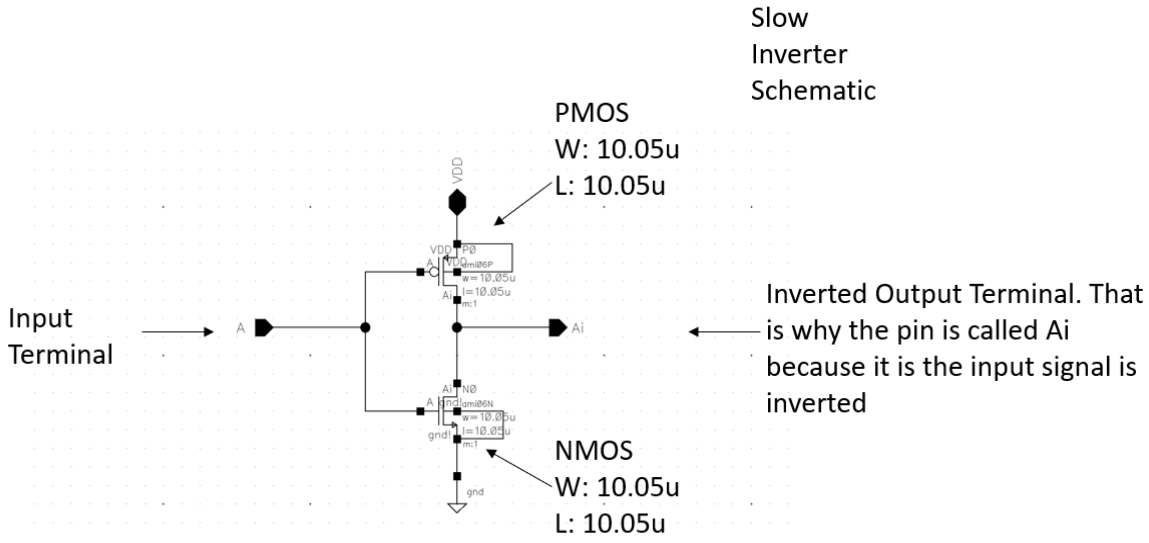

Figure 18 - Slow Inverter Schematic

In order to make an inverter that creates a long delay the length of the devices need to be increased. A regular inverter used in this Thesis is 12u/6u with a length of 600n. As seen in the slow inverter schematic both the PMOS and NMOS are 10.05u/10.05u. The slow inverter is one of the main components to make the ring oscillator, so that the desired frequency of 5MHz can be achieved.

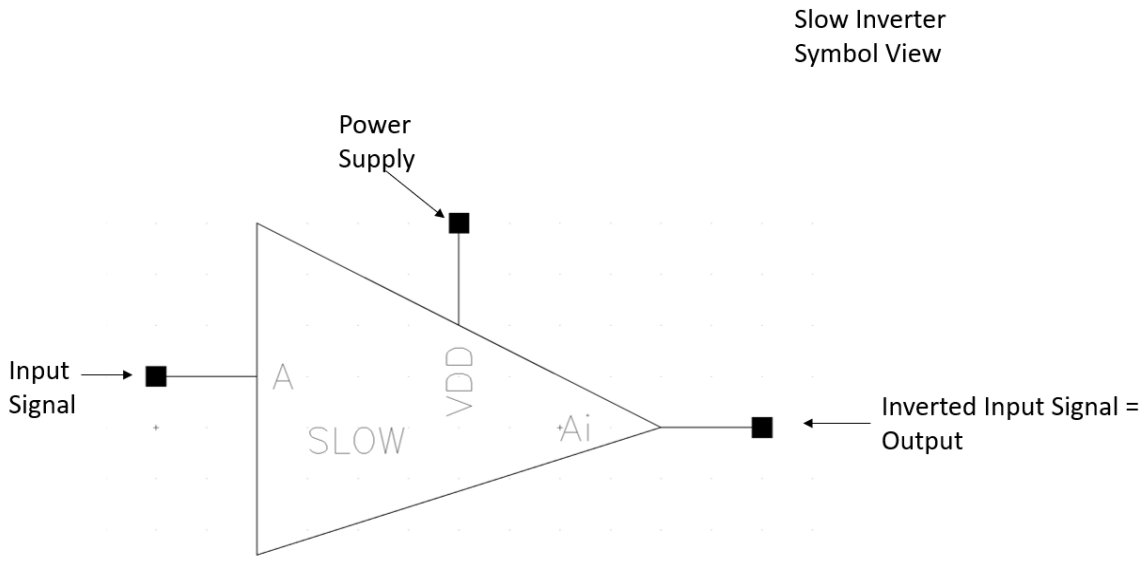

Figure 19 - Slow Inverter Symbol

The slow inverter symbol has 3 pins. The top pin is the VDD pin, while the left pin is the input pin, and Ai is the A pin inverted.

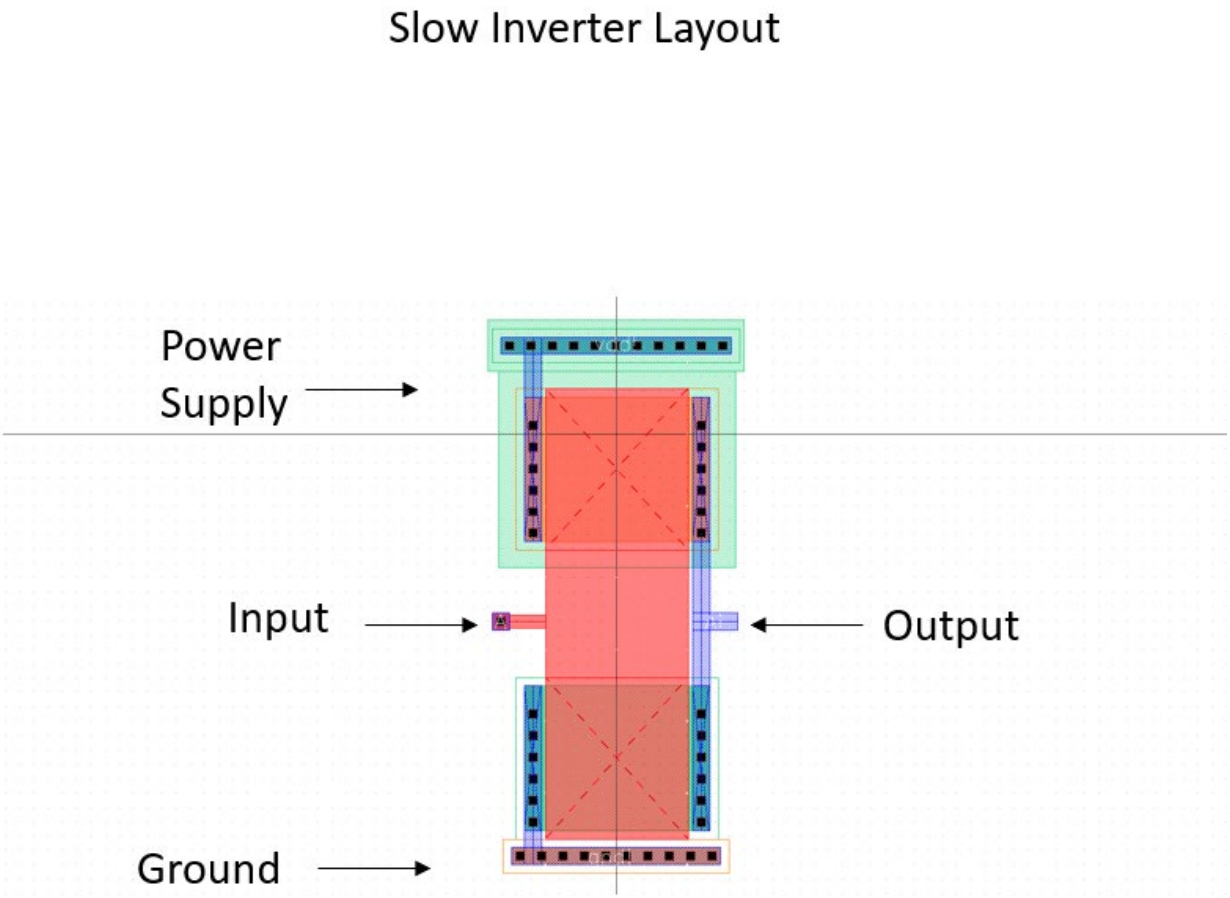

Figure 20 - Slow Inverter Layout

The slow inverter layout differs from most layouts because the gate is much wider than normal inverter layouts.

2.3.2 Inverter

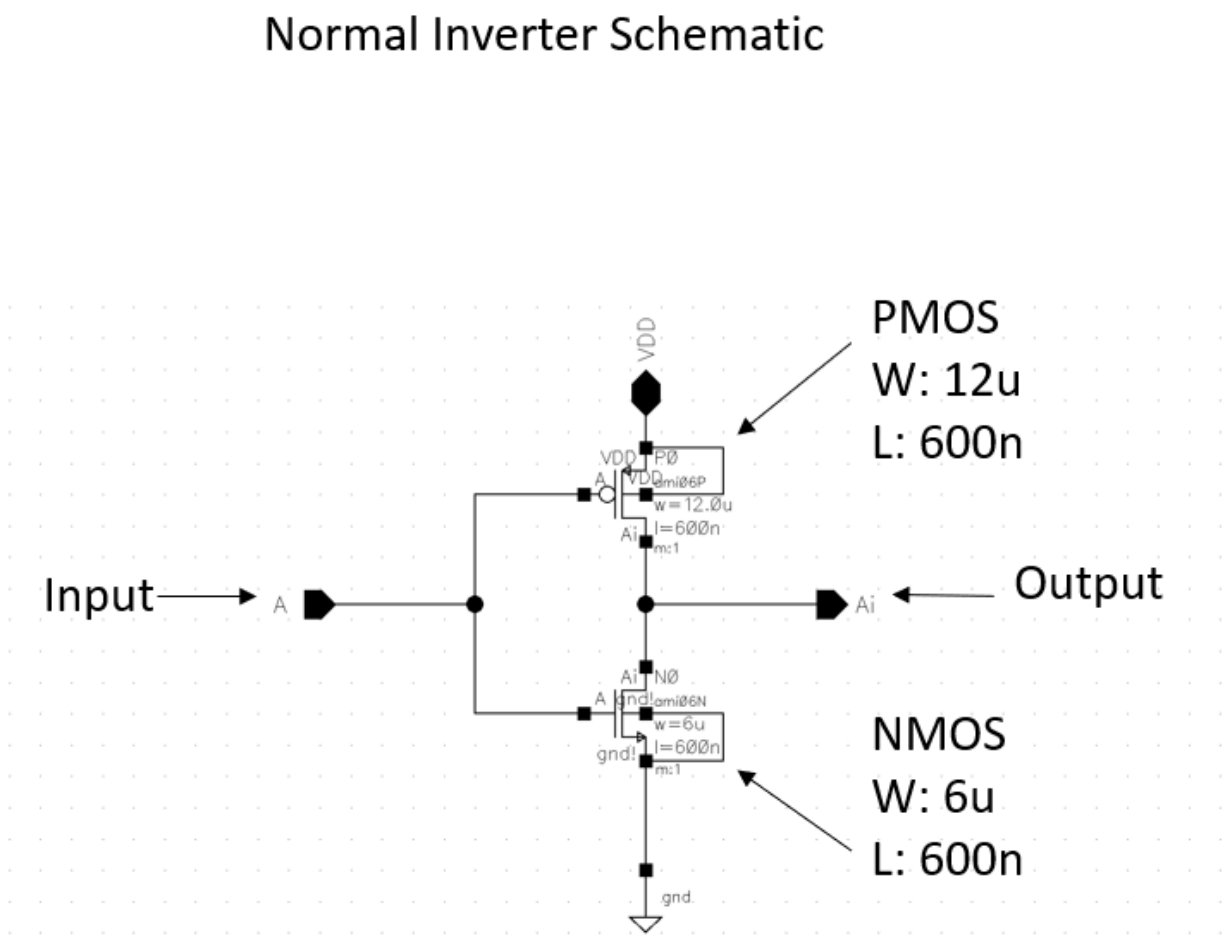

Figure 21 - Inverter Schematic

The inverter schematic used the normal 12u/6u (PMOS/NMOS) that was used throughout the Thesis. The main use of the inverters in this Thesis is to invert signals, or clean up the input/output of signals.

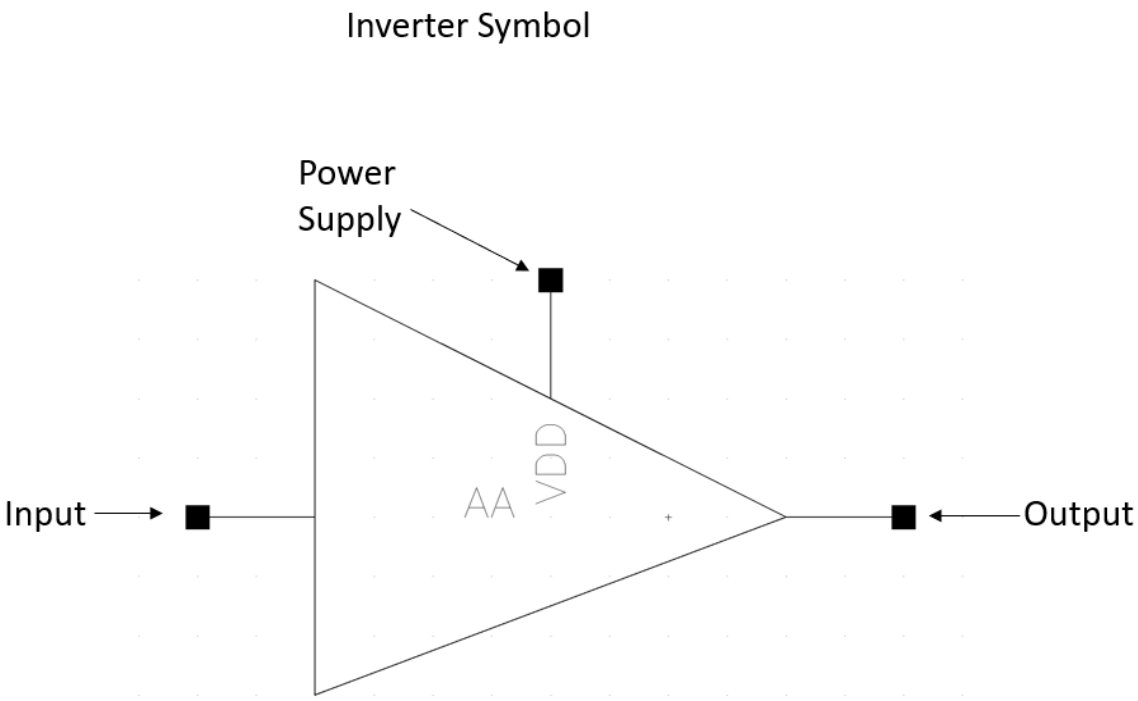

Figure 22 - Inverter Symbol

Again, much like the slow inverter symbol the regular inverter symbol as three pins. One for power, one for the input, and the output signal, which is the input inverted.

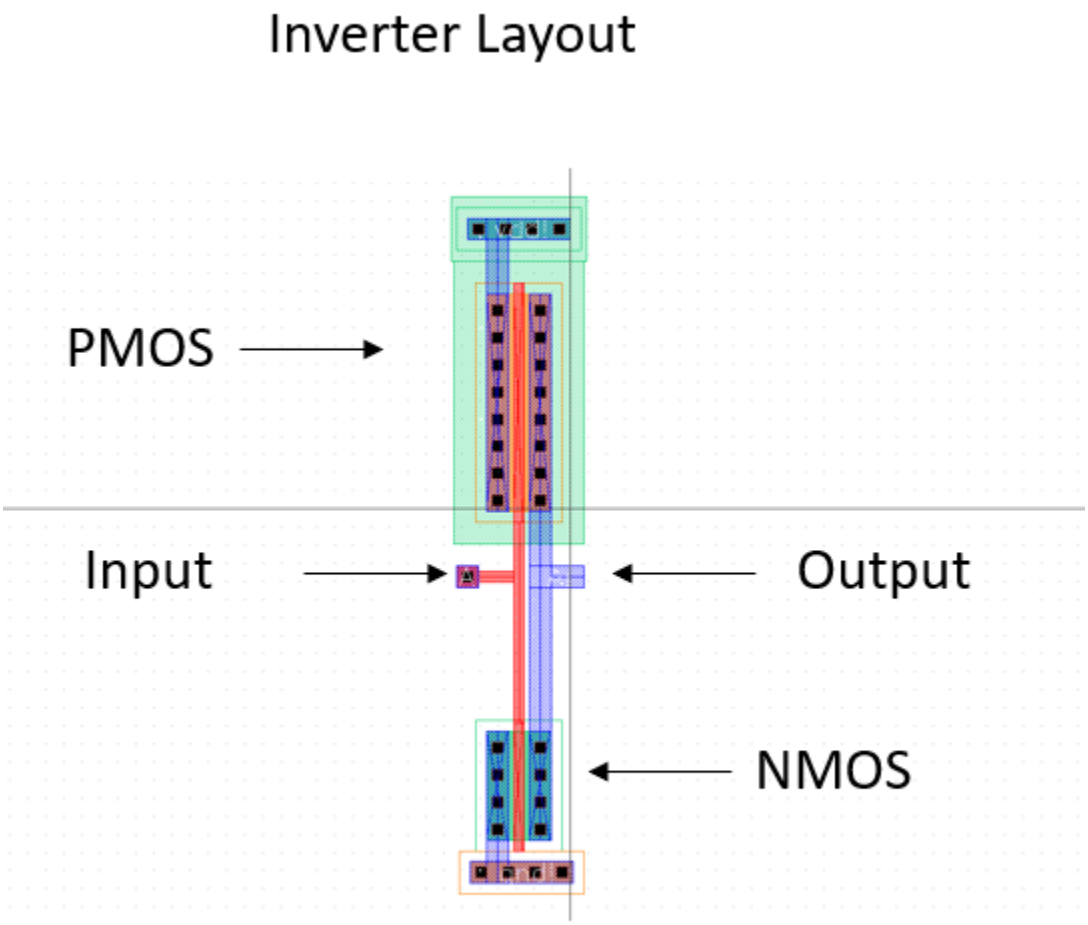

Figure 23 - Inverter Layout

Inverter layout is different to the slow inverter layout, due to the gate width. This layout is relatively smaller than the slow inverter layout.

2.3.3 NAND Gate

The NAND gate is used as an enable in the ring oscillator. The main advantage of the NAND gate is due to its logic it can turn off the ring oscillator quickly, and does not have a long delay. Both the PMOS and NMOS have widths of 6u and lengths of 600n. This is done so that the switching times are more equivalent.

When enable is low, the output of the NAND gate is always high, so in the case that enable is low the NAND gate shuts the oscillator off because the output of the NAND gate does not change regardless of the second input. When enable is high, the output of the NAND gate is the inverse of the second input terminal.

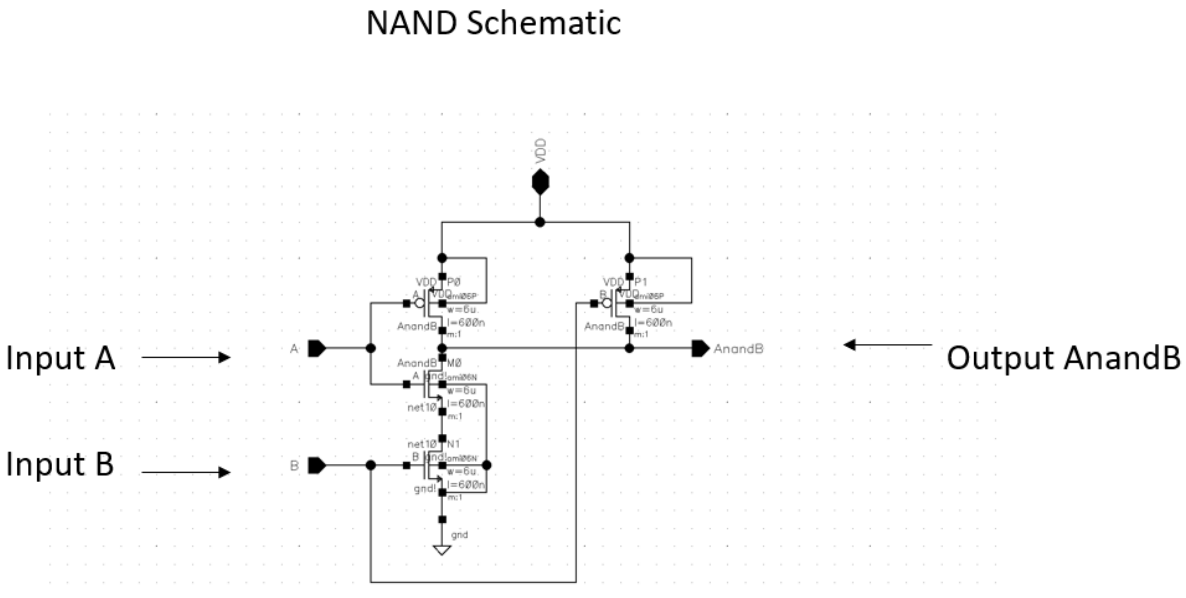

Figure 24 - NAND Schematic

As seen from the schematic above the NAND gate has two PMOS and two NMOS. On the left-hand side, it can be seen that there are two input signals. These signals are Input A and B. On the right-hand side, the output of the NAND gate is seen.

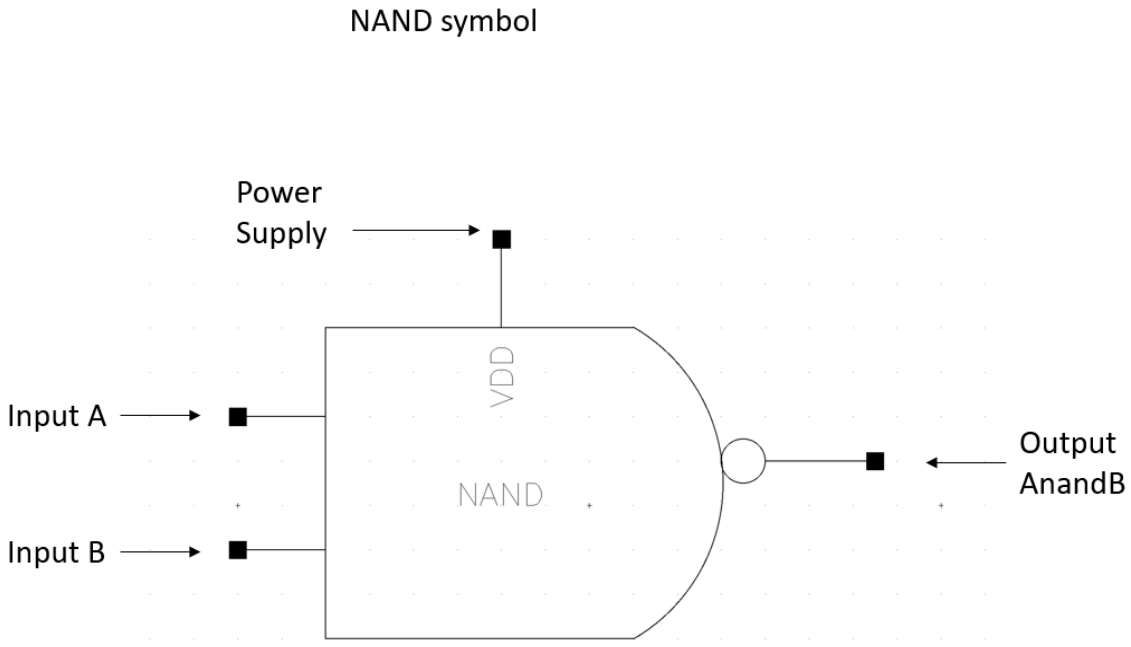

Figure 25 - NAND Symbol

The NAND has two input terminals and one output terminal. One of the input terminals will be the output of the inverter, and the other will be the enabled pin. This symbol hides the logic and devices and shows a clean symbol with the pins.

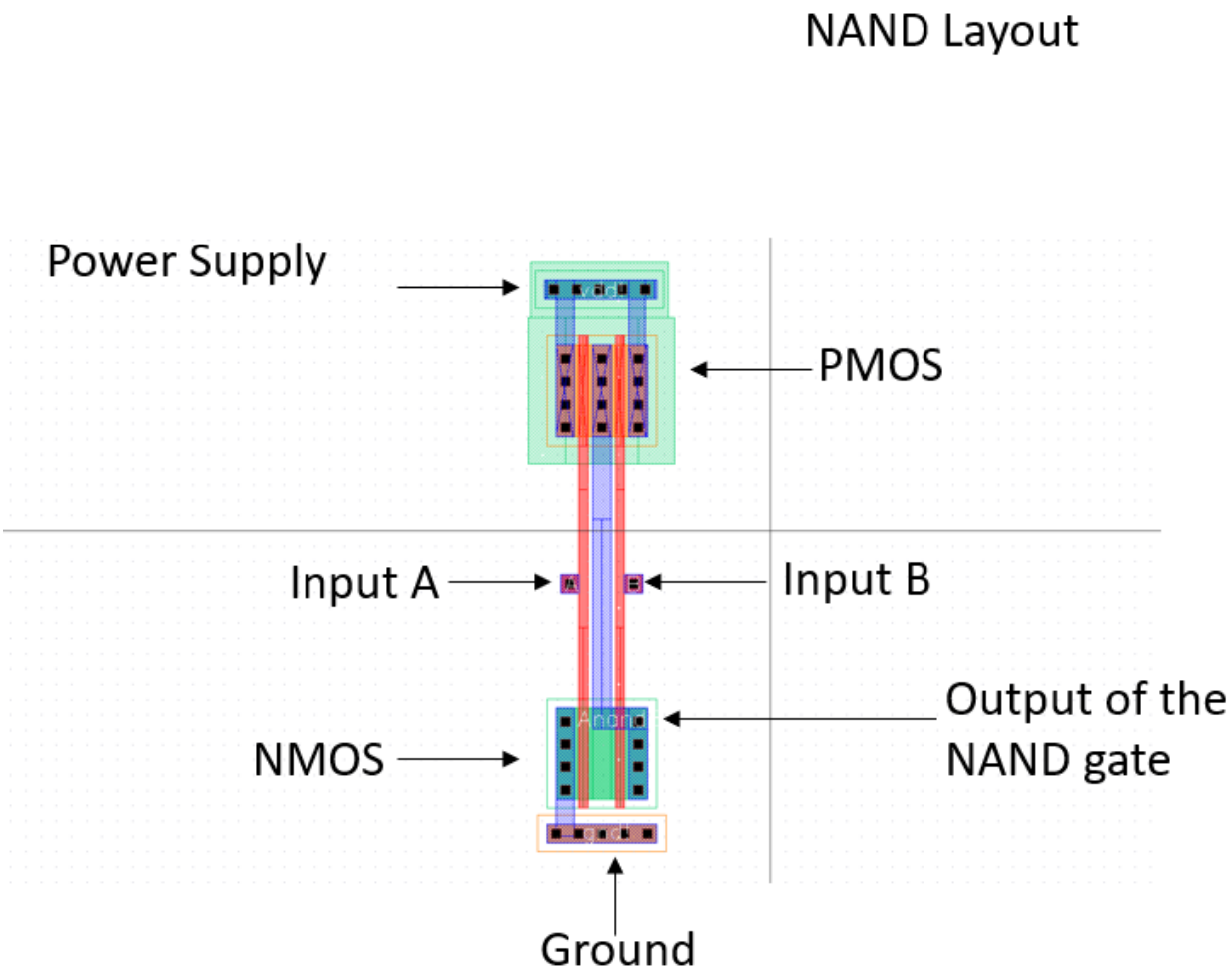

Figure 26 - NAND Layout

For the NAND layout there are two PMOS and two NMOS. For the PMOS section the PMOS have been stacked, while the NMOS has been stacked as well, but the middle body was taken away.

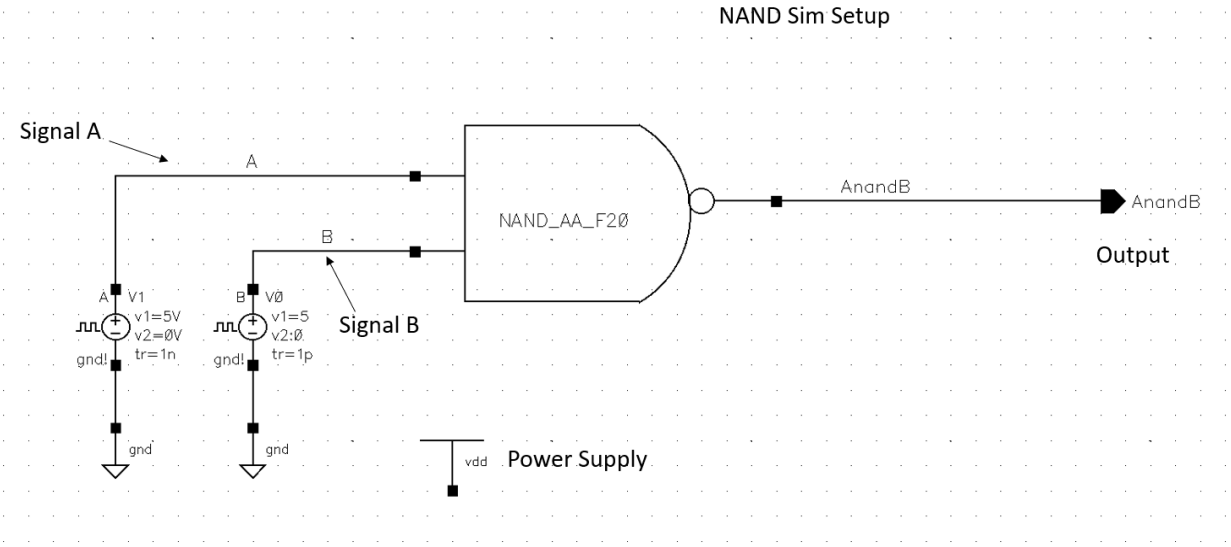

Figure 27 - NAND Simulation Setup

The NAND simulation setup features the NAND gate symbol with two input signals. The input signal are two pulse voltage sources that form the truth table in order to show that the NAND gate works. The A signal is 0,0,1,1 and the B signal is 0,1,0,1. This can be done with the input signals frequency and period.

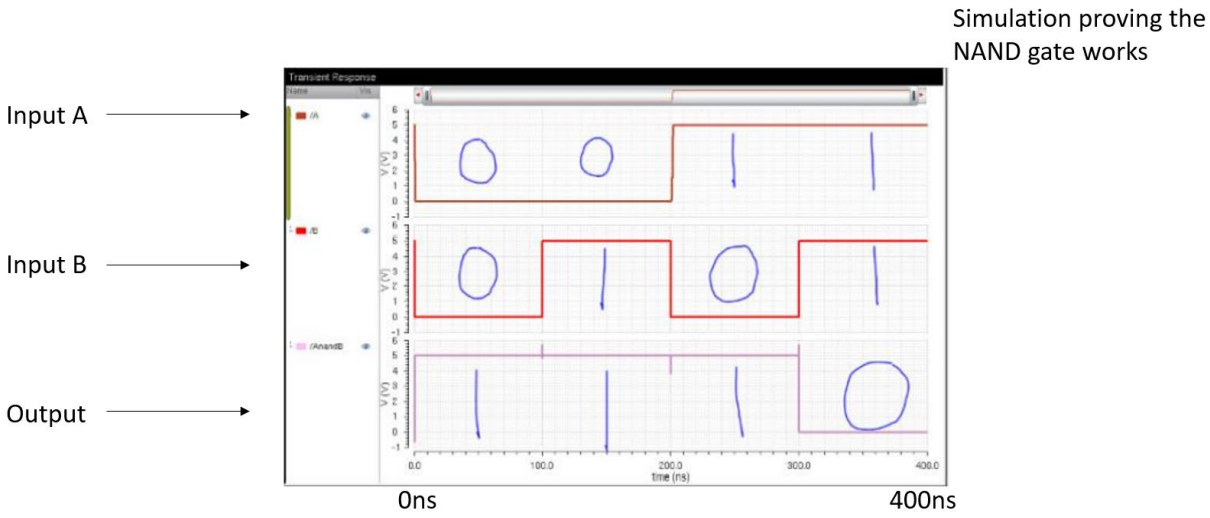

Figure 28 - NAND Simulation

Simulation of the NAND gate proving the truth table that was listed below.

NAND Gate Truth Table

A	B	A (NAND) B
0	0	1
0	1	1
1	0	1
1	1	0

Table 1 - NAND Gate Truth Table

2.4 Buffer

The buffer is a necessity so that it can drive the 5pF capacitor (internal capacitance of the NMOS) that is contained within the flyback switching power supply. The buffer is going to be the most power-hungry component in the controller chip due to its size and number of components. According to the calculations, the design needs a three-stage buffer with the "A" value equal to 8.

Buffer Calculations

$$A_o = \frac{PMOS}{NMOS} = \frac{12u}{6u}$$

$$C'_{ox} = 2.5\frac{fF}{um^2}$$

$$C_{ox}n = 2.5\frac{fF}{um^2} * 6um * 0.6um = 9fF$$

$$C_{ox}p = 2.5\frac{fF}{um^2} * 12um * 0.6um = 18fF$$

Using Miller's Theorem

$$C_{in} = \frac{3}{2}(9fF + 18fF) = 40.5fF$$

Using A = 8

$$N * lnA = ln\frac{C_{Load}}{C_{in}}$$

$$N * ln8 = ln\frac{5pF}{40.5fF}$$

$$N = \frac{4.815}{2.079}$$

$$N = 2.316 \approx 3$$

Although the N value is closer to the value of 2, it was needed to round up to 3 so that the logic of the ring oscillator was kept intact.

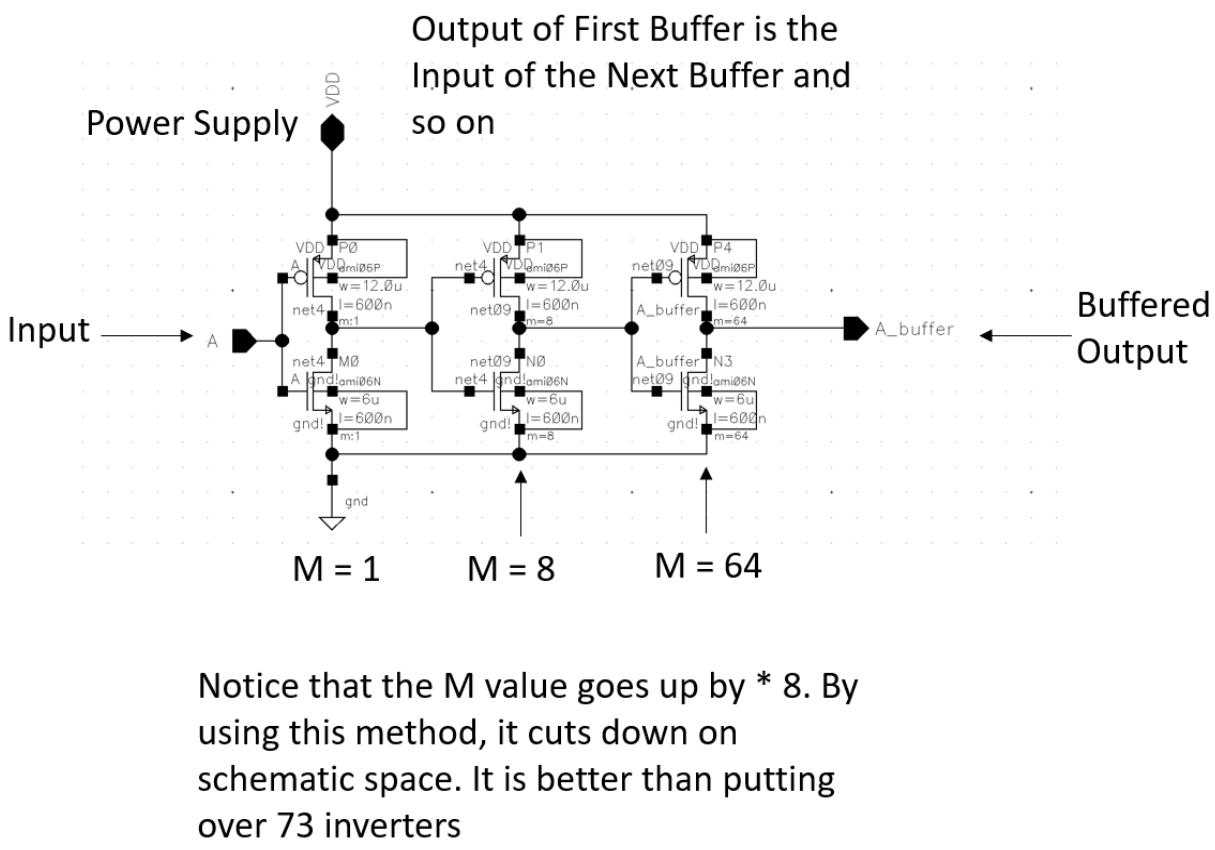

Figure 29 - Buffer Schematic

The buffer schematic is shown above. As shown in the calculations the multiplier was increased by 8. The first inverter m value is one, the second inverter m value is 8, and the third inverter m value is 64.

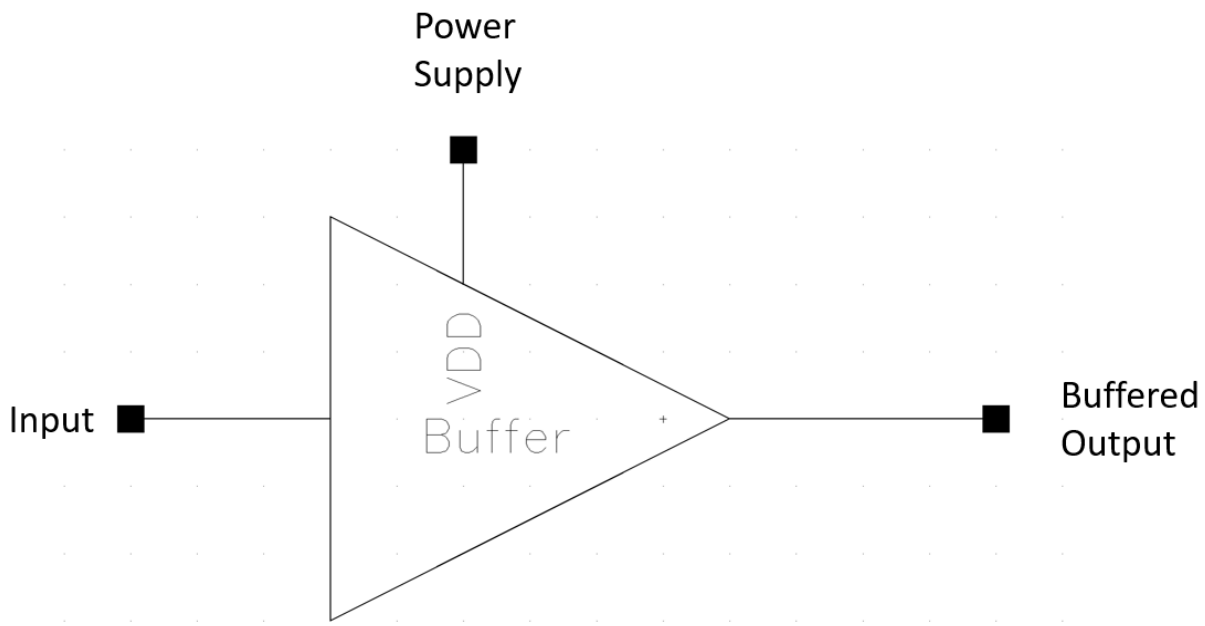

Figure 30 - Buffer Symbol

The buffer symbol has one input terminal and one output terminal, along with a power pin on the top.

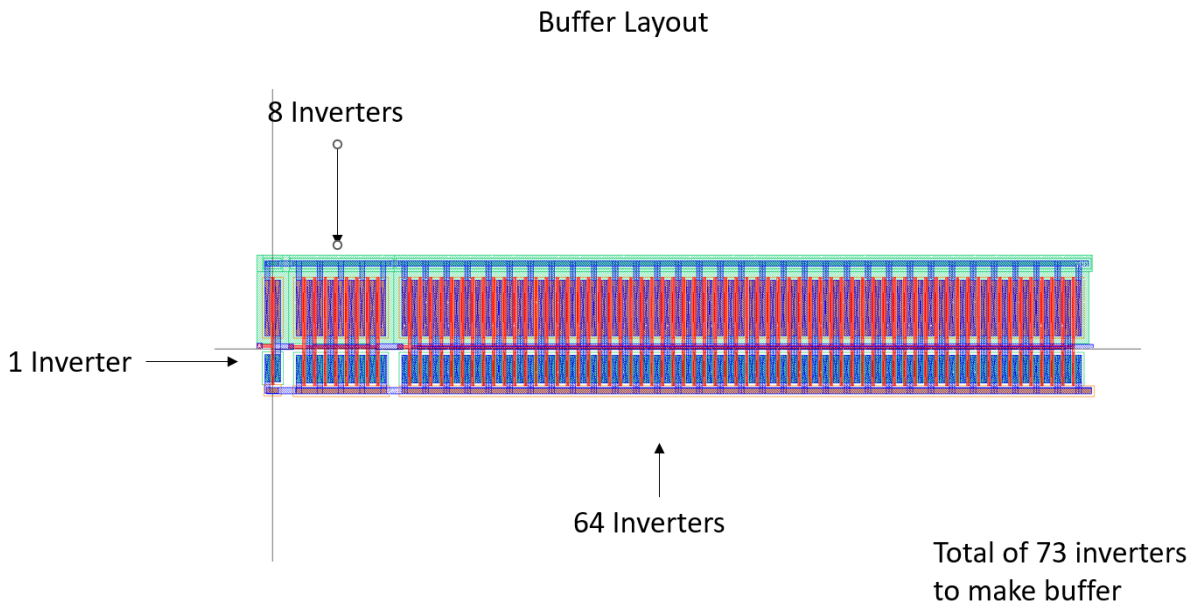

Figure 31 - Buffer Layout

The Figure above shows the layout of the buffer. The layout for the buffer is also very long. For future improvements, the layout can be made shorter by using the serpentine method. It can be seen the input signal goes through the single inverter first, then 8 inverters, and then 64 inverters. This is a total of 73 inverters to make the buffer.

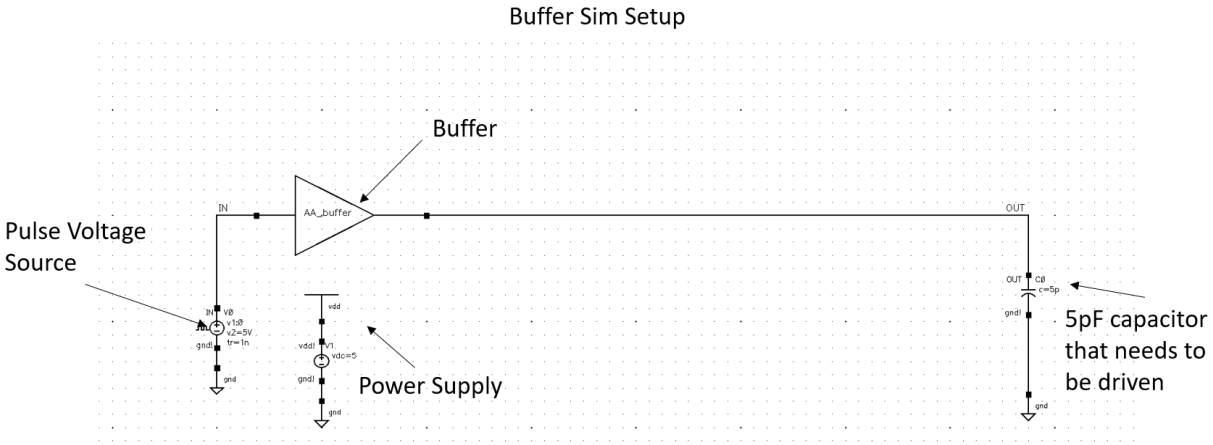

Figure 32 - Buffer Simulation Schematics

The buffer simulation schematic features the buffer symbol. The buffer's input signal is a pulse voltage source. On the buffer's output there is 5 pF capacitor.

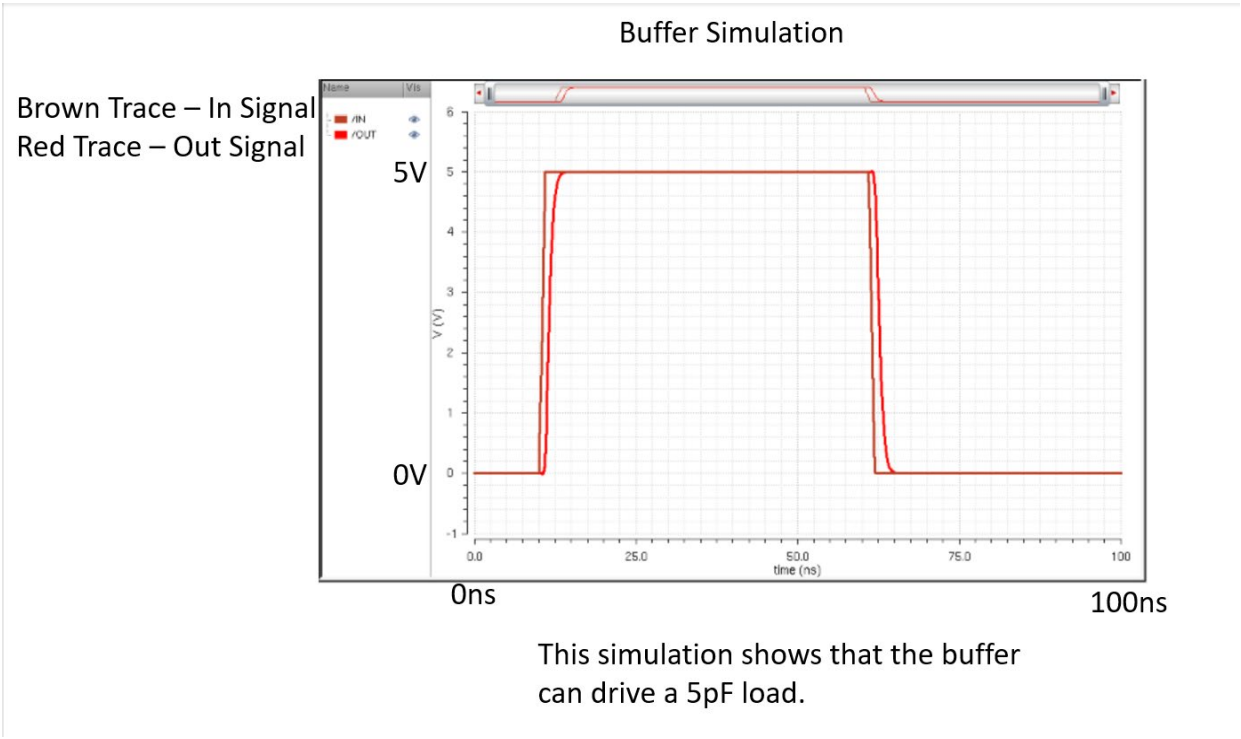

Figure 33 - Buffer Simulation

The simulation above shows that they buffer can drive a 5pF load.

2.5 Passive Components

2.5.1 1K Ohm Resistor: Hi-Res

In the Thesis there needs to be a 1k and 9k resistor in order to make 1/10 voltage divider so that the voltage is small enough that the comparator can turn on. Using On's semiconductor C5 process the Hi-res sheet resistance value is 1000 ohm/ sheet. To make resistors the following formula should be used. Hi-res is a special layer that blocks the implant of the poly layer in the polysilicon.

$$Hi\ Res\ Resistor = Sheet\ Resistance\left(\frac{ohms}{sheet}\right) * \frac{W}{L} = 1000 * \frac{2.4}{2.4} = 1000\ ohms$$

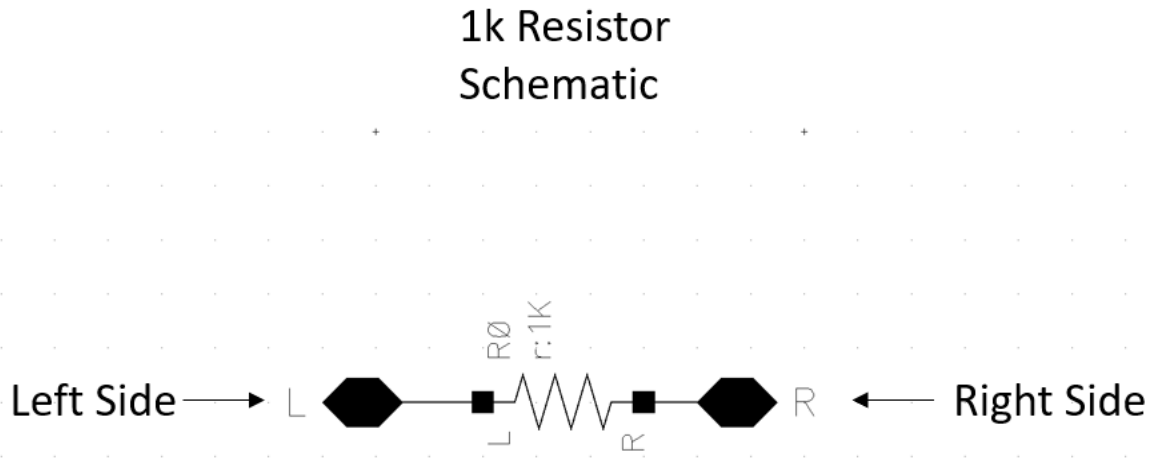

Figure 34 - 1k Hi-Res Resistor Schematic

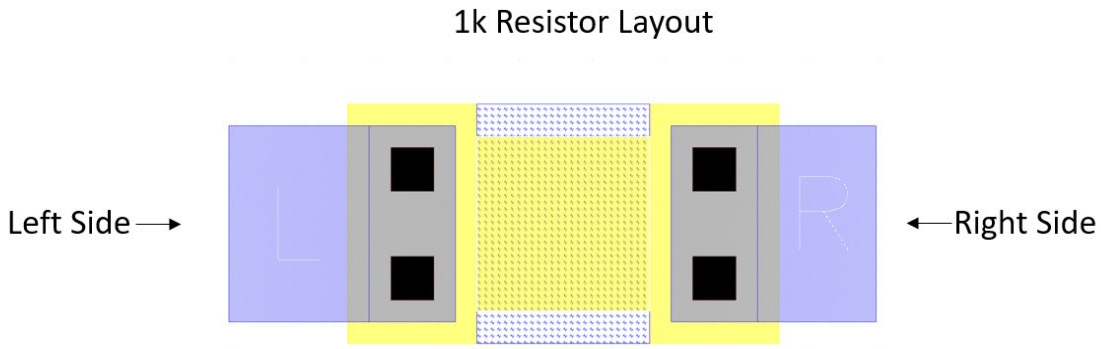

Figure 35 - 1k Hi-Res Resistor Layout

2.5.2 9K Ohm Resistor: Hi-Res

Originally calculated for 9K exactly, but when extracted the resistor value was too high so changes were made to the widths and lengths of the devices. These are the final numbers that were used.

$$Hi\ Res\ Resistor = Sheet\ Resistance\left(\frac{ohms}{sheet}\right) * \frac{W}{L} = 1000 * \frac{20}{2.6} = 7700\ ohms$$

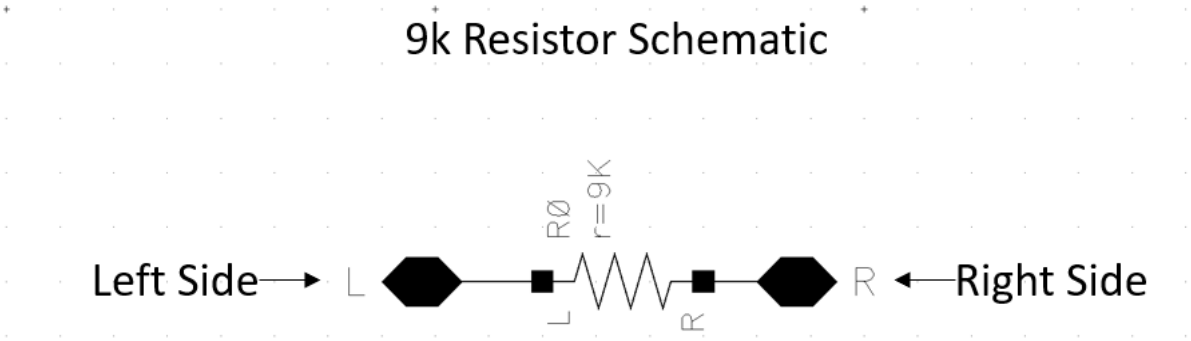

Figure 36 - 9k Hi-Res Resistor Schematic

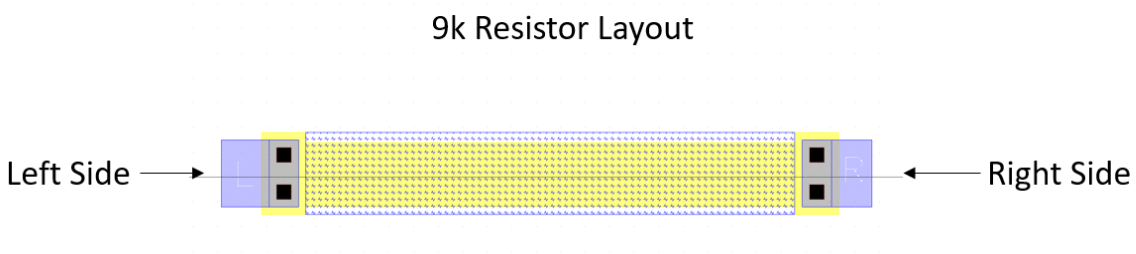

Figure 37 - 9k Hi-Res Resistor Layout

2.5.3 1 pF Poly-Poly Capacitor

Using On's semiconductor C5 process the capacitance between poly 1 and electrode (poly 2) is 900 aF/um^2. To make a poly-poly capacitor the formula below is needed. For example, to make the poly-poly capacitor in this Thesis, first draw a box of poly 1 that is 36um square and next draw an electrode (poly 2) that is 33um on top of the poly 1 square. Poly-Poly capacitors have a very thin oxide between the Poly 1 and Poly 2 layers. It being a

very thin oxide gives a high capacitance due to the formula of C = ϵA/t. Where the term 't' is the distance between the plates of the capacitor. Meaning the smaller the distance between the plates the higher the capacitance because the bottom term t is less in the division.

$$Capacitor\ Value = W * L * 900aF$$

$$Capacitor\ Value = 33um * 33um * 900aF = 1pF$$

The 1pF Poly-Poly Capacitor is used on the output of the bandgap circuit so that the output voltage from the bandgap circuit which is 1.25V has no issues and remains constant with no rippling/ voltage swing.

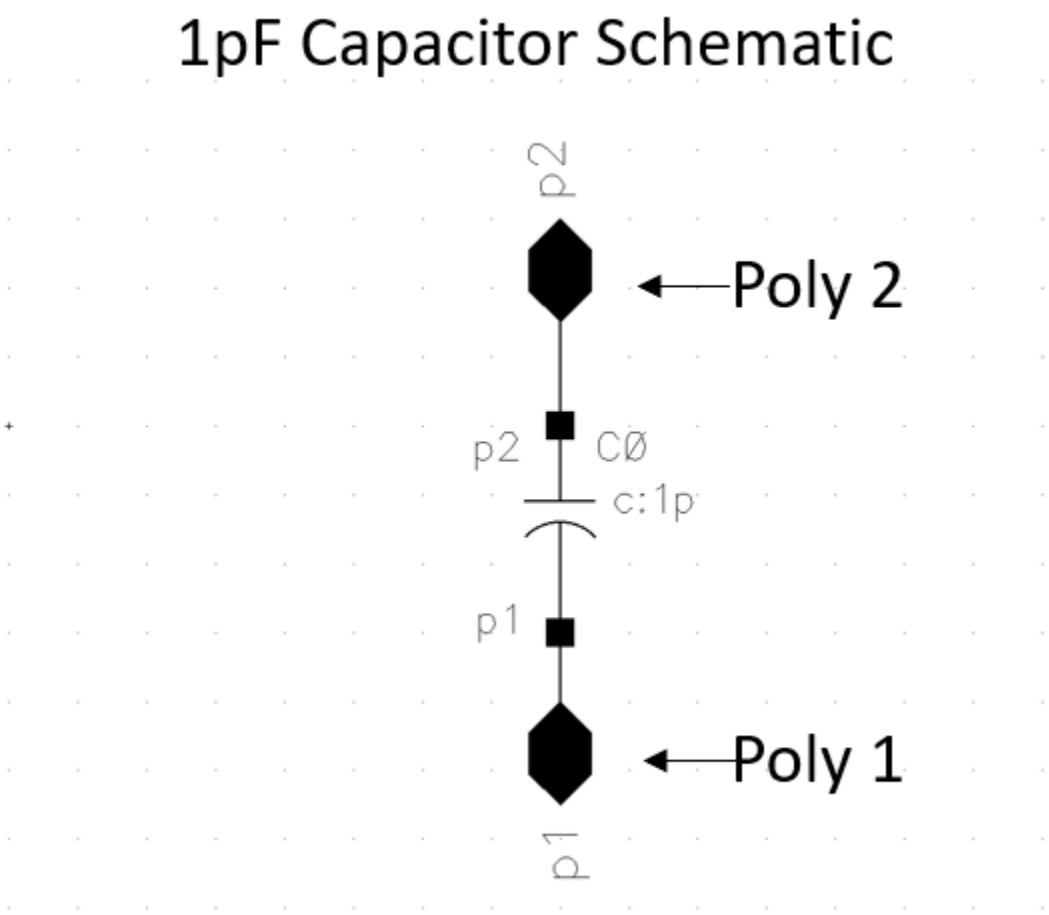

Figure 38 - 1pF Poly-Poly Capacitor Schematic

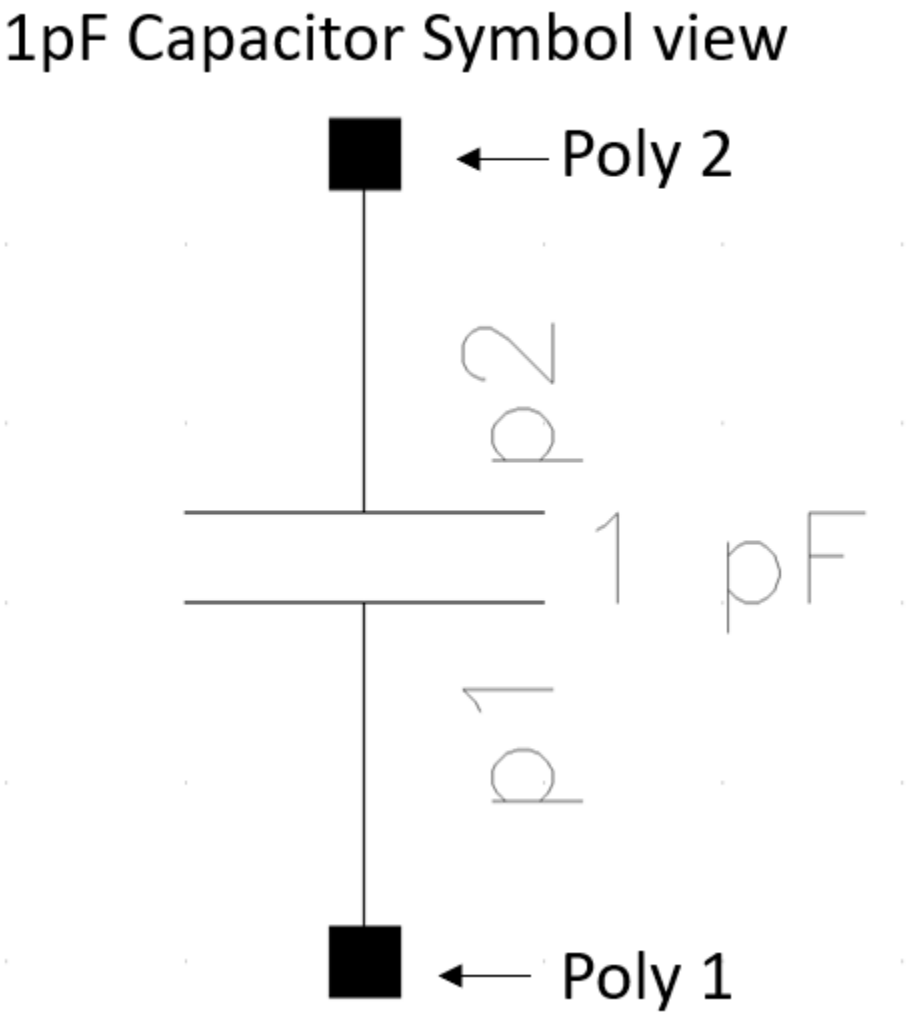

Figure 39 - 1pF Poly-Poly Capacitor Symbol

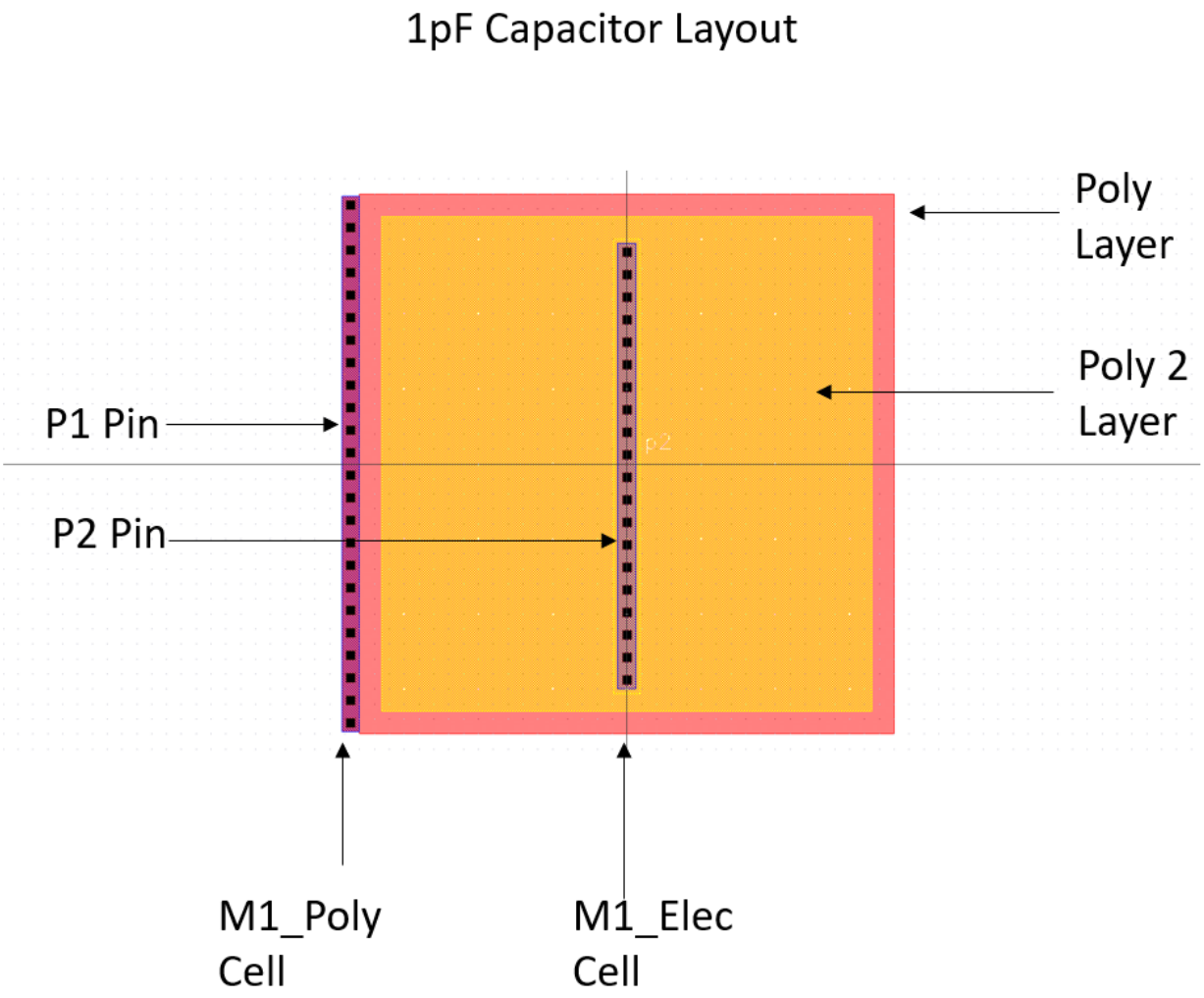

Figure 40 - 1pF Poly-Poly Capacitor Layout

In the 1pF Poly-Poly capacitor layout all the parts to the layout are shown. There are two layers which will be the Poly layer and the Poly 2 Layer. There are also two cells present which are the M1_poly cell which means there is a transition from the Metal 1 layer to the Poly layer. The other cell is the M1_elec cell which means there is a transition from

metal 1 layer to electrode which is also known as poly 2 layer. There are two pins named P1 and P2 which are connected by using a metal 1 layer.

Chapter 3: Top Level

3.1 Controller Final Schematic

An HPS (Hysteretic power supply) feedback system is simple. An example is a thermostat in a home can be set to 22°C. When the temperature drops to 21°C the heater turns on and heats the home to 23°C before the heater shuts off. The temperature in their homes moving around 2°C centered around 22°C, but from the homeowner's point of view the temperature is relatively constant. In this feedback system the input is the temperature the owner set the thermostat to. The feedback in the system is the thermostat sensing the temperature of the home and determining when to turn on or off the heater determining on the ambient temperature. The forward path of the feedback is the heater driving the temperature of the house. An important note is that the output of the system is oscillating. In a hysteretic power system, if the amplitude of the oscillations can be minimized, then it can be a very useful and simple. [1]

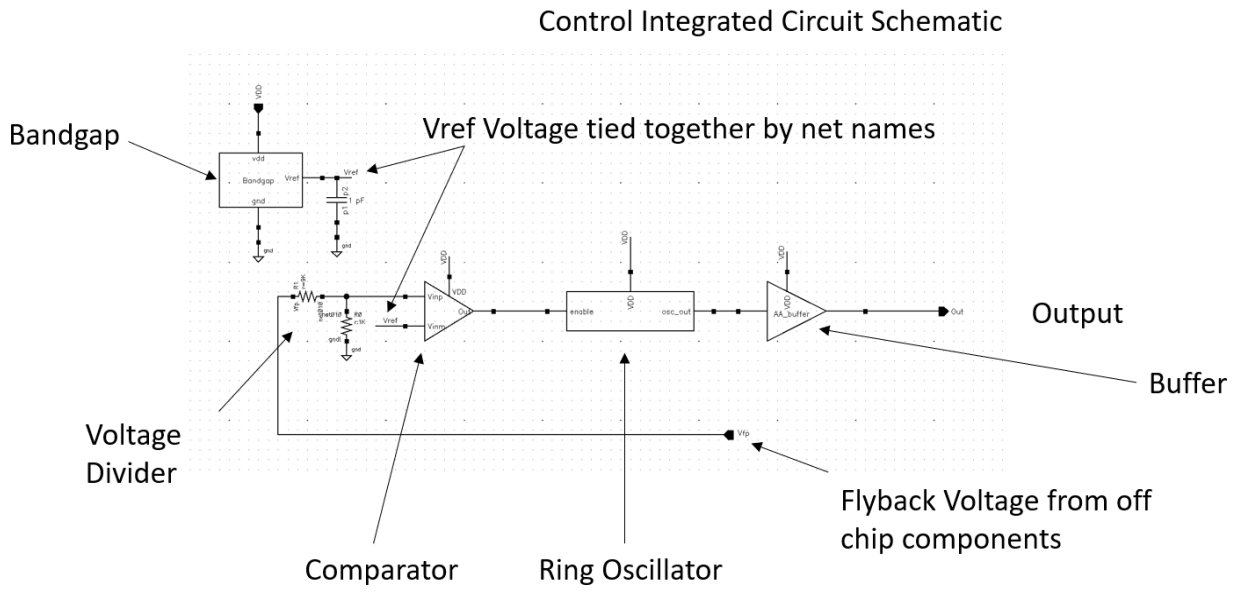

Figure 41 - Top Level Schematic of the Controller Chip

Shown in the Figure above is the final schematic where all the components that were created are connected. V(fp) is connected to a resistive voltage divider where the output of the voltage divider is the plus of the terminal of the comparator while the output of the bandgap is the second of the comparator. The output of the comparator is the input of the ring oscillator. The output of the ring oscillator is the input of the buffer.

3.2 Controller Final Layout

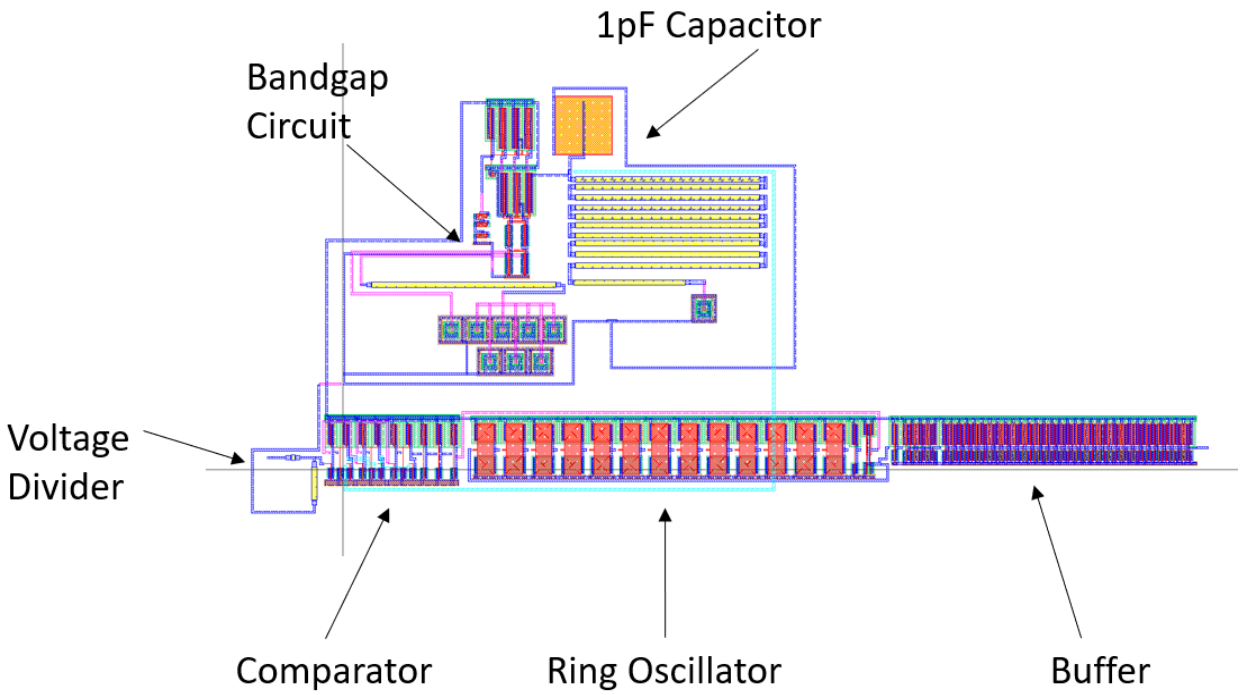

Figure 42 - Top Level Layout of the Controller Chip

The Figure above shows the final layout with all the components talked about in the previous chapter which are now all connected. The top half of the layout is the bandgap circuit. The lower half from left to right is the comparator, the ring oscillator, followed by the buffer.

3.3 Fly-back Switching Power Supply

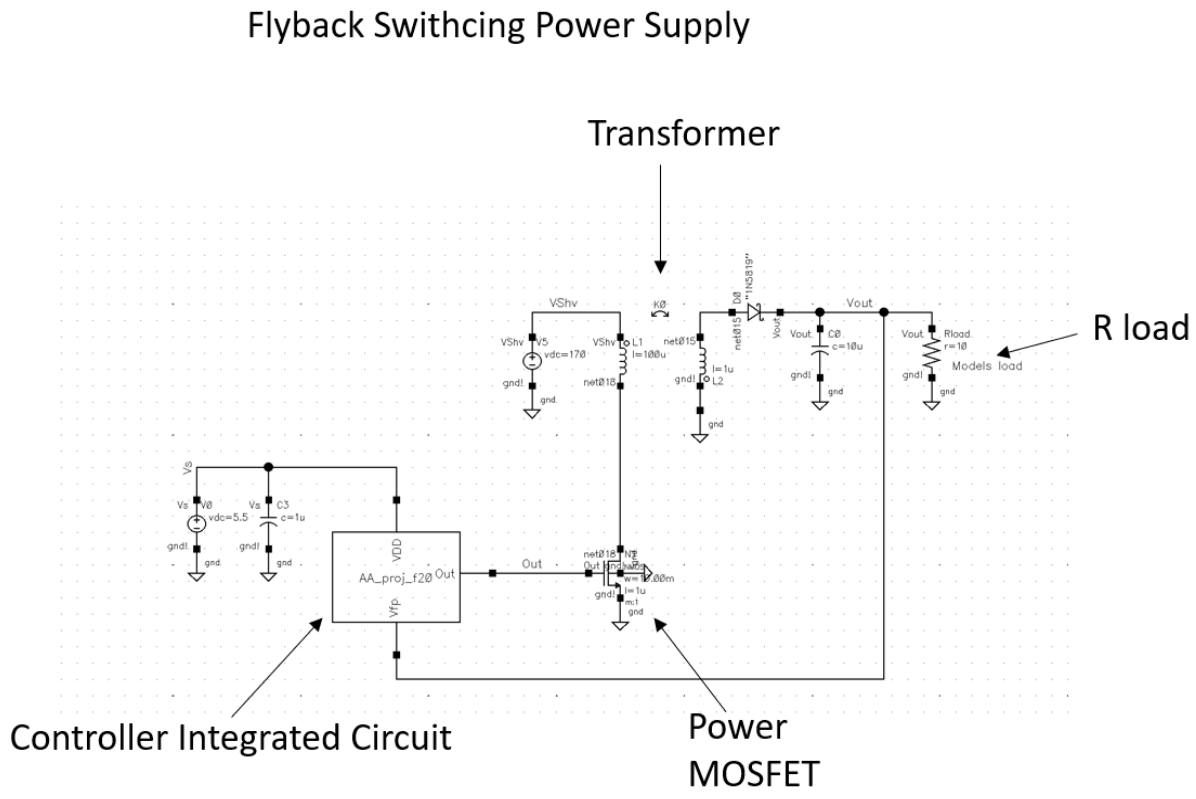

Figure 43 - Controller Chip with Off Chip Components for Flyback SPS

In Figure 43 it shows the Thesis symbol along with some off-chip components that are needed in order to simulate the final design. It is important to note that for the simulation to work, an initial condition is needed on the output of the ring oscillator.

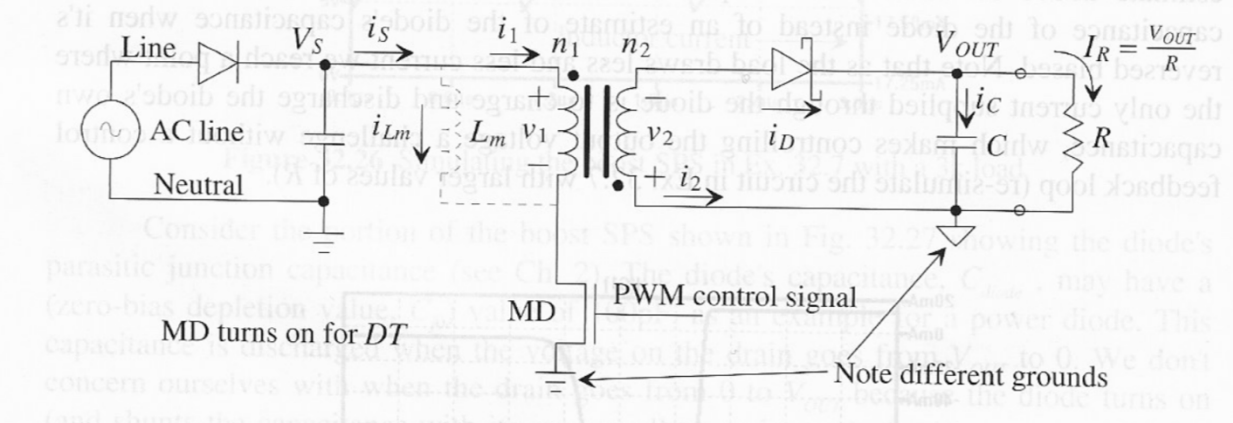

Figure 44 – Flyback SPS [1, Fig 32.29, p. 1200]

The input to the power supply is the AC line (hot and neutral) it is often called an "off-line" supply. This AC voltage is rectified to generate a DC voltage often termed as Vs. This DC voltage is connected to the primary of a transformer and a switch. The switch then provides control to regulate the output voltage. One thing that should be noted is that there are two grounds in this circuit. One of the grounds is associated with the AC line side, and the other is associated with the DC output. One may ask why this a necessity; this is a necessity for safety. A user gets power from this circuit from Vout, if Vout is shorted to ground the amount of current that is supplied is limited due to the transformer. This is not the case on the AC line side where a tremendous amount of current can be supplied. [1]

Next, one might wonder why there is a need for a switch on the primary side of the transformer, and why this is a rectification of the AC, to generate DC, and then connect the DC to the primary of the transformer, and a switch. The first thought would be why not rectify the output of the transformer after the AC line has already been stepped down. The

answer for this is the size of the transformer for an AC input at 50/60 Hz is much larger than the size of a transformer at say for example 100kHZ. Using the switch, can improve the effective frequency of the input to the transformer, and this in turn, reduces the transformer's size. This is very important when ensuring power supplies that are small-sized. [1]

As seen in the Figure 44 above there is a transformer present. As of the Figure the L1 side is the primary side while the L2 is the secondary side. The transformer can be flipped around so that the wire with n2 turns is connected to Vs and the with n1 is connected to the Schottky diode. The relationship with the voltages, currents, inductances, and windings is as follows.

$$\frac{v_1}{v_2} = \frac{i_2}{i_1} = \frac{n_1}{n_2} = \sqrt{\frac{L_1}{L_2}}$$

Notice that there is a Lm in the Figure. This is the magnetizing inductance of the transformer. This is the inductance that one would measure on the primary side of the transformer without anything connected to the secondary (secondary open). Therefore, there is a secondary rectifying Schottky diode. In shorter terms, the inductance of the primary with the secondary open is equal to Lm = L1. So, if the power MOSFET turns on a current iLM flows in the magnetizing inductance Lm. When MD shuts off the magnetizing current wants to continue flowing so it flows backward through the transformer. When this happens, the diode turns on in the secondary of the transformer and the energy is stored in the magnetizing inductance that is supplied to the load which is modeled as R. The Schottky

diode turns on so that it neglects the forward voltage drop -v2 = Vout and then v1 goes to -Vout(n1/n2). [1]

Now that the foundation of the circuit has been laid out, let's move on to the operation of the circuit. When MD is on

$$v_1 = V_S = L_m \frac{di_{LM}}{dt}$$

Assuming that MD is on for DT seconds, whereas D is the duty cycle

$$\Delta i_{Lm,up} = \frac{V_S * DT}{L_M}$$

I1 and i2 are both zero and the secondary rectifying Schottky diode is off when MD Is on. The voltage across the primary Vs, which is large. For this Thesis the AC input is 120V RMS. The peak of the voltage is approximately 170V. Even though there is current flowing in the secondary, there is still a voltage on the secondary as seen in the equation about transformer seen below.

$$\frac{n_1}{n_2} = \sqrt{\frac{L_1}{L_2}} = \sqrt{\frac{100u}{1u}} = 10$$

The primary side has 120V RMS signal on the primary side of the transformer so the secondary voltage v2 is 120/10 or 12V RMS. When no load is connected to the secondary of the transformer the current that flows in the primary side of the transformer has a peak amplitude of $\frac{170}{2\pi * 5Mhz * 100u} = 54mA$. The 10 Ohm load, R, is reflected by this equation [1]

$$\frac{v_1}{i_1} = \frac{v_2}{i_2} * (\frac{n_1}{n_2})^2$$

When a load is connected like the 10-ohm resistor is in the schematic above the peak of i2 is 12V/10ohm or 1.2A. The peak of i1 is i2/10 which is 120mA. Since in this case v2/i2 is 10 ohms (= R) and (n1/n2) ^2 is 100 the 10ohm load is reflected to the primary as a 1k ohm load which is a resistive load in parallel with the 100u magnetizing inductance. The i1 + 1LM current can be calculated [1]

$$i_1 + i_{LM} = \frac{v_1}{R * \left(\frac{n_1}{n_2}\right)^2 || j\omega L_m}$$

$$\frac{170}{1k||j(2\pi 5Mhz)100uH} = \frac{170}{\frac{1000 * j(3140)}{1000 + j(3140)}} = 178mA$$

The net changes in the currents are result in being 0

$$\Delta i_{Lm,up} - \Delta i_{Lm,down} = 0 = \frac{V_s * DT}{L_m} - \frac{V_{out} * (1 - D)T}{L_m} * (\frac{n_1}{n_2})$$

Which means that the DC input which is known as Vs and the DC output Vout can be related to

$$V_{out} = V_s * (\frac{D}{1 - D})(\frac{n_1}{n_2})$$

As the value D approaches to 1 the output voltage can grow without bound even if the power supply is or is not supplying power. This is the very reason that flyback power controllers that generate pulse width modulation control are designed to have maximum duty cycle. For calculating the filter capacitor, the equation below can be used

$$C_{\min} = \frac{D}{R * f * (\frac{\Delta V_{out}}{V_{out}})}$$

In this design a 10uF capacitor is being used. [1]

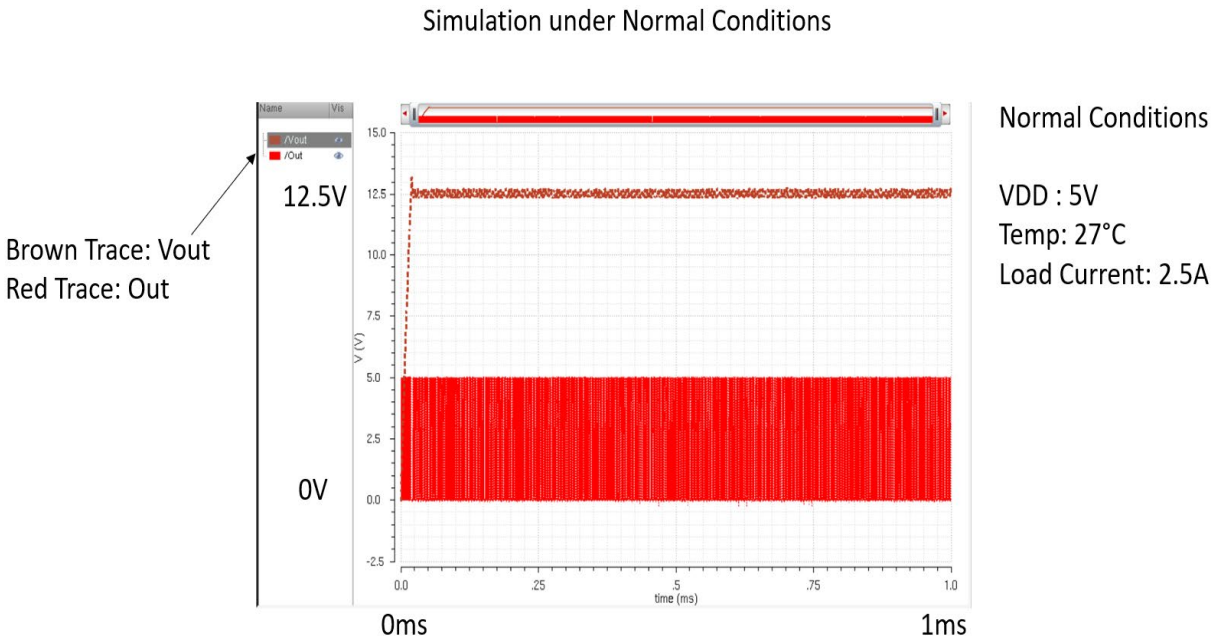

Figure 45 - Simulation Under Normal Conditions

The normal condition for the simulation is that VDD is equal to 5V, and the temperature is 27 degrees Celsius. This simulation is with a load current of 2.5A. The brown trace is Vout and the red trace is out.

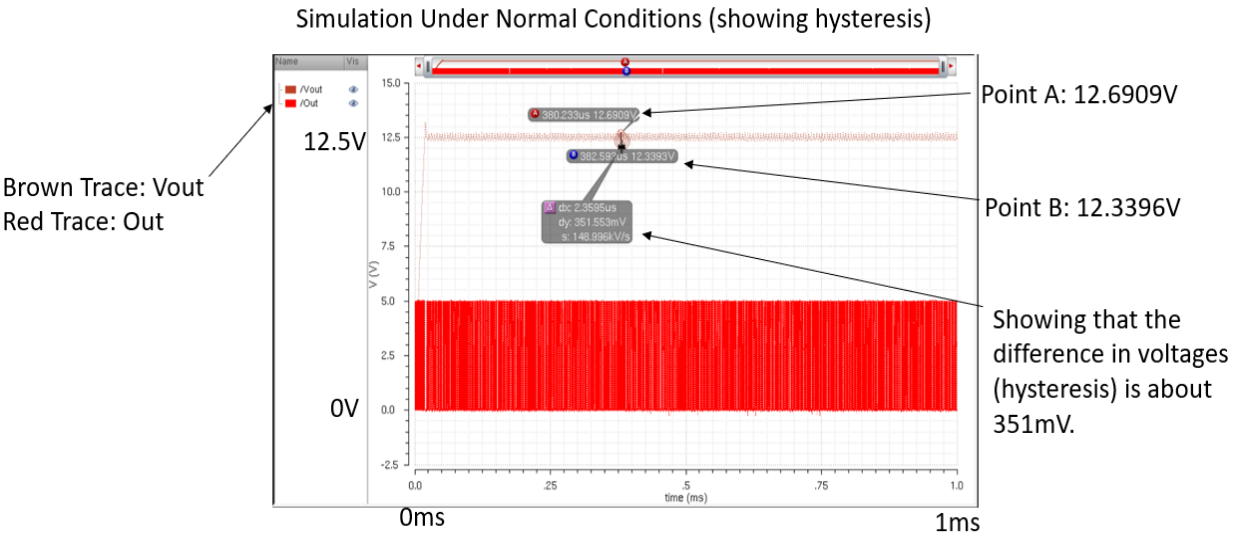

Figure 46 - Simulation Under Normal Conditions Showing Hysteresis

This Figure shows more information about the simulation under Normal Conditions. It also shows the output voltage is 12.5V with a hysteresis of around 350mV. The hysteresis is shown by taking the difference between point A which is 12.6909V and point B 12.3396V which is about 351mV.

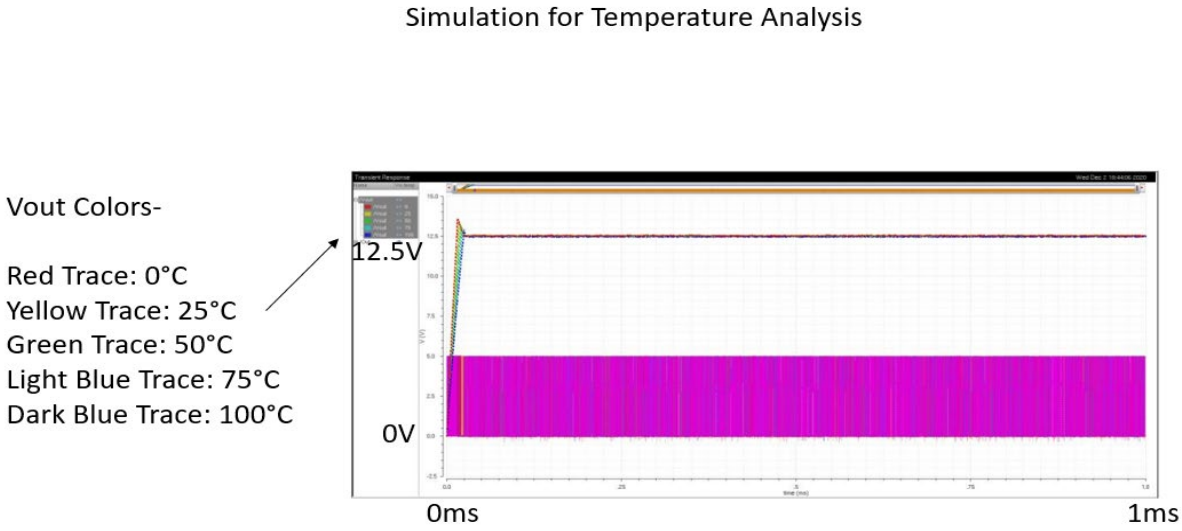

Figure 47 - Simulation Run for Temperature Analysis

The Figure above shows the simulation ran for temperature analysis. The red trace is 0°C, the yellow trace is 25°C, the green trace is 50°C, the light blue is 75°C, and the dark blue trace is 110°C. The data has been summarized and appears in the next chapter, which is the Summary of Performance.

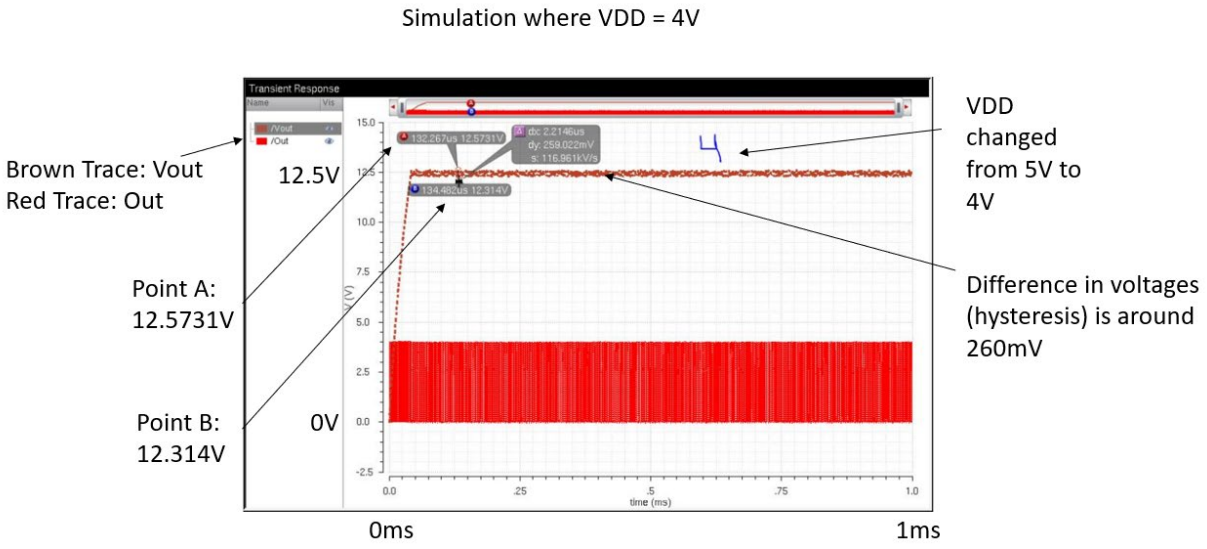

Figure 48 - Simulation where VDD is Lowered From 5V to 4V

In the Figure above, the simulation is run except for the fact that the VDD voltage is lowered from 5V to 4V. When the VDD voltage is changed the hysteresis is shown by taking the difference between point A which is 12.5731 and point B which is 12.314V which is around 260mV.

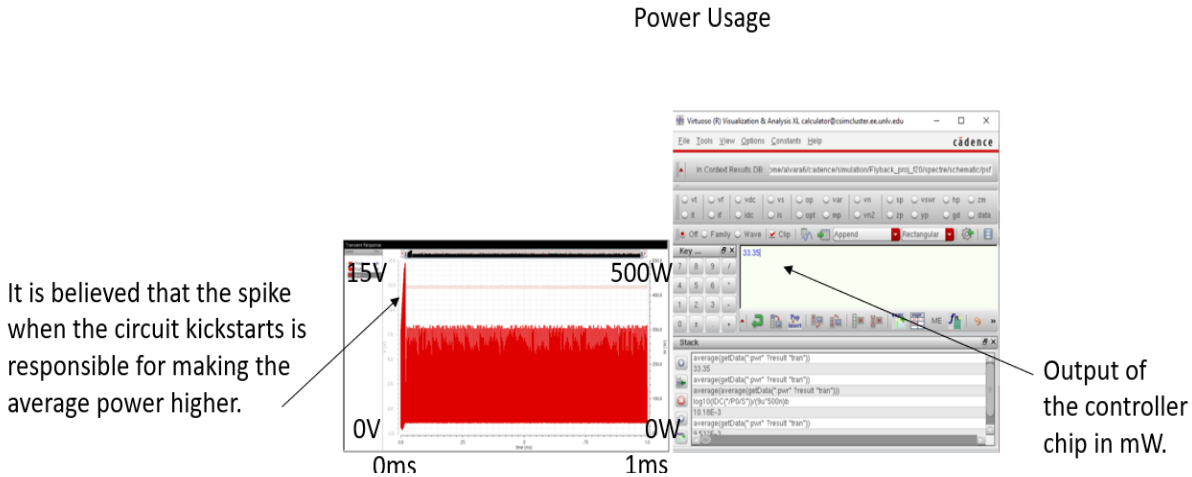

Figure 49 - Power Usage

In the left side of the Figure the graph is showing the power used by the circuit. The right side of the Figure shows the average power of the circuit. It is believed that the average power of the circuit is higher due to the kickstart of the circuit. If the average power of the circuit was calculated in the steady state condition, then this value would be dramatically reduced.

Simulation with different off chip capacitor value

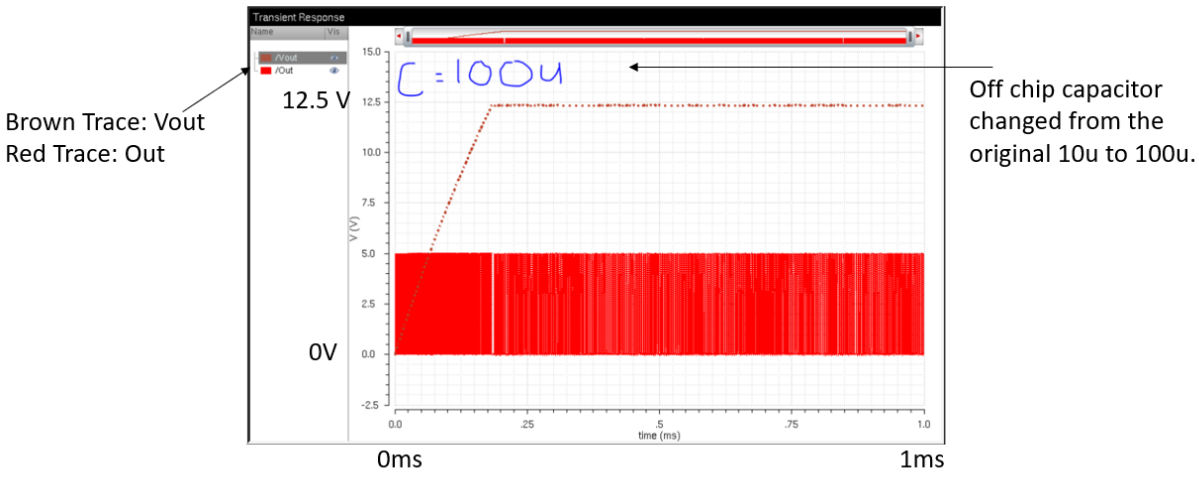

Figure 50 - Simulation with Different Off Chip Capacitor Value

This is what happens when the off-chip capacitor value is switched from 10u to 100u. The difference between the sims between 10u to 100u is that the output is much more filtered.

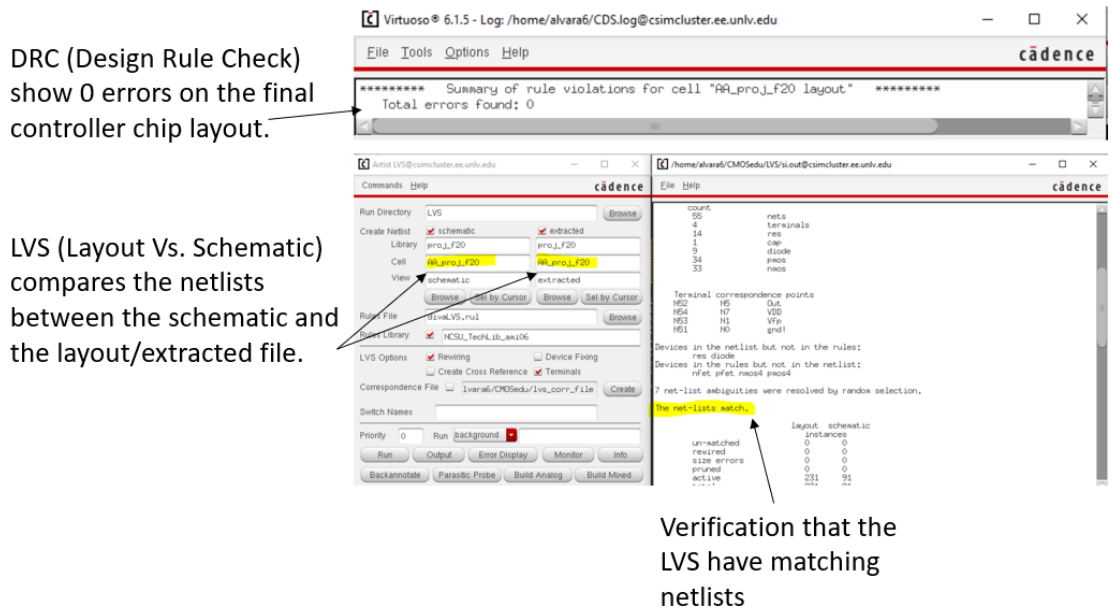

Figure 51 - Verification of DRC and LVS

Design Rule Check shows the final control integrated circuit shows 0 errors on the layout. A design rule check is a set of rules a designer can use to ensure their schematic matches all the dimensional tolerances, and manufacturing considerations. Layout vs. Schematic compares the netlists between the schematic and the layout/extracted file. The Figure verifies that the DRC and LVS have zero errors and that the netlists match. When running the LVS the FET parameters check should be marked.

Chapter 4: Summary of Performance

Useful Formulas

Frequency

$$Frequency = \frac{1}{Period}$$

Ohm's Law

$$Output\ Voltage = Current_{LOAD} * R_{LOAD}$$

Efficiency of a Circuit

$$E = \frac{V_{OUT} * I_{LOAD}}{V_{DD} * (AVG(I(V_{DD})))}$$

4.1 Varying Temperature

Varying Temperature							
Temp (°C)	Output Voltage (V)	Load Current (A)	Ripple Voltage	Period (ns)	Average Power from VDD (mW)	Average Power from 10m NMOS (W)	Efficiency of Circuit (%)
0	12.6	1.26	~ 76mV	187	18.52	16.52	96.1
25	12.57	1.257	~73mV	214	16.9	16.54	95.52
50	12.55	1.255	~68mV	243	15.23	16.42	95.9
75	12.53	1.253	~75mV	276	13.59	16.22	96.79
100	12.49	1.249	~51mV	311	11.99	16.11	96.8

Table 2 - Varying Temperature

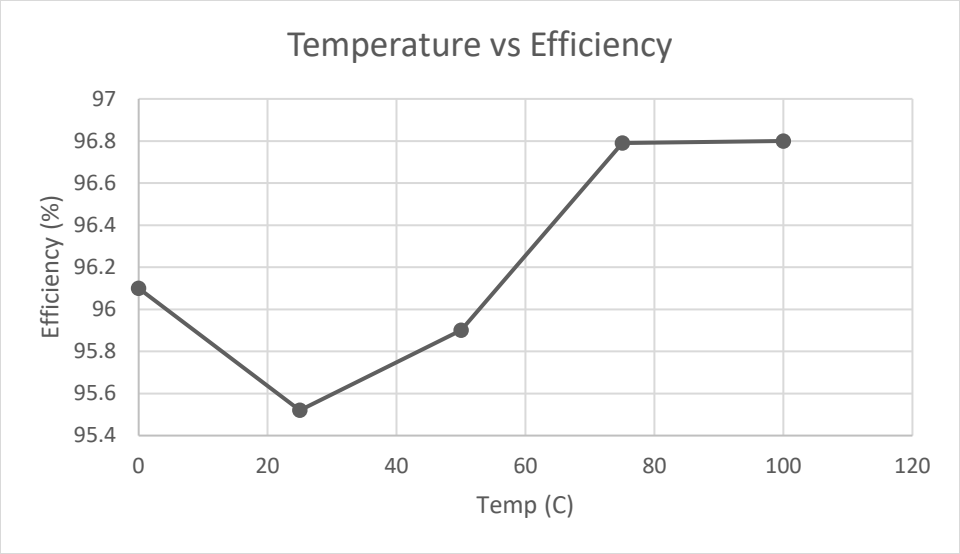

Figure 52 - Temperature Vs. Efficiency

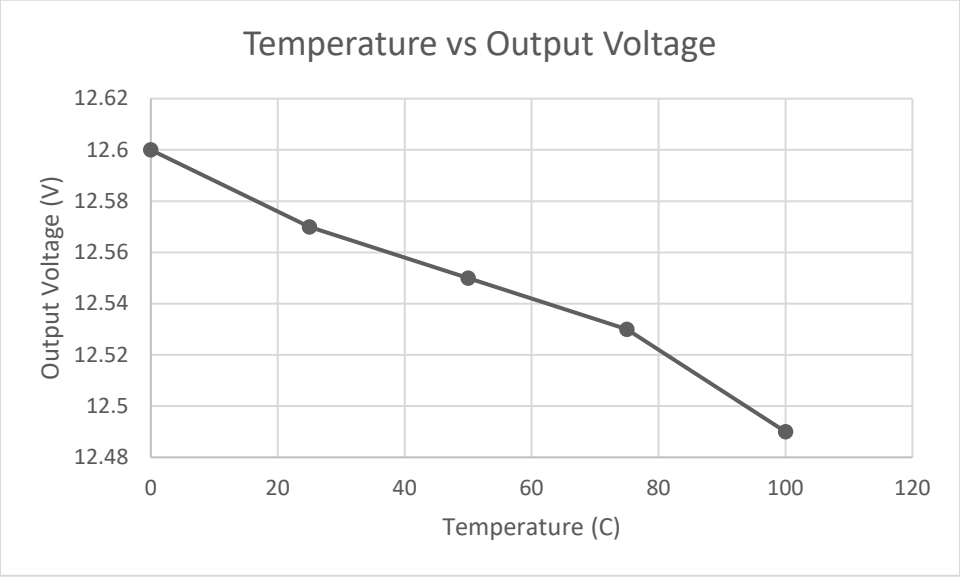

Figure 53 - Temperature Vs. Output Voltage

Summary of the Results: The Thesis topic has been run under several conditions including different temperature conditions ranging from 0° to 100° Celsius. The result from this test is that this Thesis works well in all temperature conditions, because all temperatures tested resulted in above 95% efficiency. An important analyzation to notice is that when temperature is increased, the output voltage decreases.

4.2 Varying VDD Voltage

Varying VDD values = Load Current: 1.25A, Temp: 27 Degrees Celsius							
VDD (V)	Output Voltage(V)	Ripple Voltage (mV)	Frequency and Period (ns)	Average Power from VDD supply (mW)	Average Power from 10m NMOS (W)	Efficiency of Circuit (%)	Run Time
3	11.2	48	393	1.6	31	45	500us
3.5	12.3	63	315	3	28	55	100us
3.75	12.5	78	287	5	24	65	100us
4	12.5	63	270	7	18	86	100us
4.25	12.52	71	248	9	16.39	95	100us
4.5	12.52	60	224	11	16.39	95	100us
4.75	12.53	73	220	13	16.31	96	100us
5	12.52	85	209	16	16.35	96	100us
5.25	12.53	76	200	19	16.43	95	100us
5.5	12.59	75	193	24	16.24	97	100us

Table 3 - Varying VDD Voltage

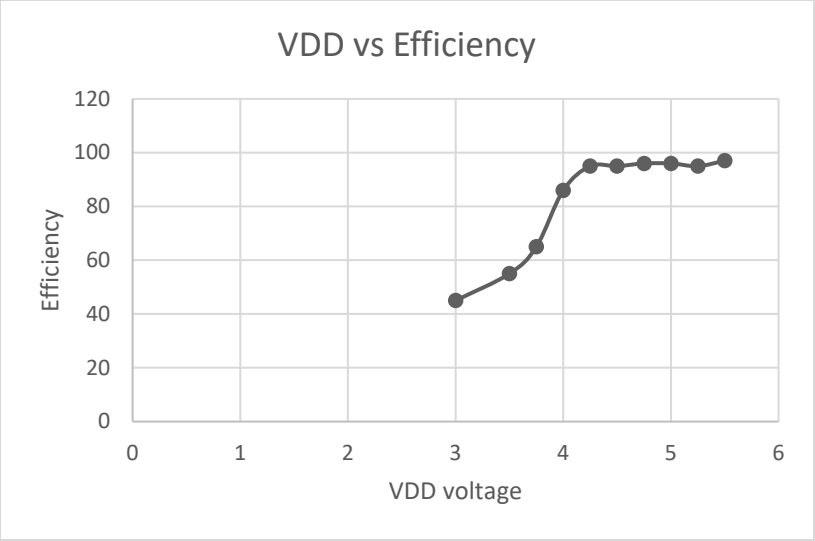

Figure 54 - VDD Vs. Efficiency

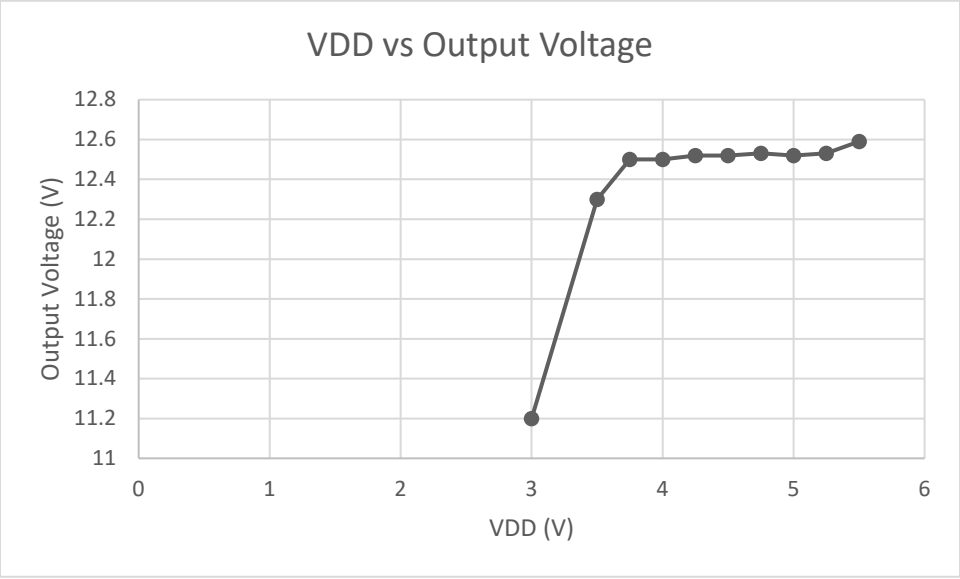

Figure 55 - VDD Vs. Output Voltage

Summary of the Results: The Thesis has been run using several VDD voltages ranging from 3V to 5.5V. What can be deduced from analyzing the results is that as the VDD starts to increase so does the efficiency. This is due to many of the components that are not getting full power to work at their best efficiency at 3V, but as the VDD voltage increases the components start getting full power. Another fact is that as the VDD increases so does the output voltage. Another test that will be run is how output voltage changes with load current.

4.3 Varying R(Load) for Different Load Currents

Varying Load Currents							
Load Current	Output Voltage (V)	Ripple Voltage	Period	Average Power from Vdd (mW)	Average Power from 10m NMOS (W)	Efficiency of Circuit (%)	Run Time
0uA	12.51	14.5mV	14u	10mW	17.37mW	0.007	10ms
10mA	12.86	1.14mV	12.54u	11mW	131mW	89	1ms
100mA	12.55	11mV	1.27us	18mW	2.632W	90	500us
200mA	12.542	4.5mV	697ns	20mW	2.659W	94.6	500us
250mA	12.544	6mV	532ns	14mW	3.2W	98	100us
1.25A	12.56	62.26mV	215ns	12mW	16W	98.16	100us
2A	12.63	222.65mV	216ns	15.62mW	26W	97.15	100us
2.5A	12.65	330mV	217ns	14.25mW	33W	95.8	100us
6.25A	12.86	1.5V	214ns	15mW	90W	89	500us

Table 4 - Varying R(Load) for Different Load Currents

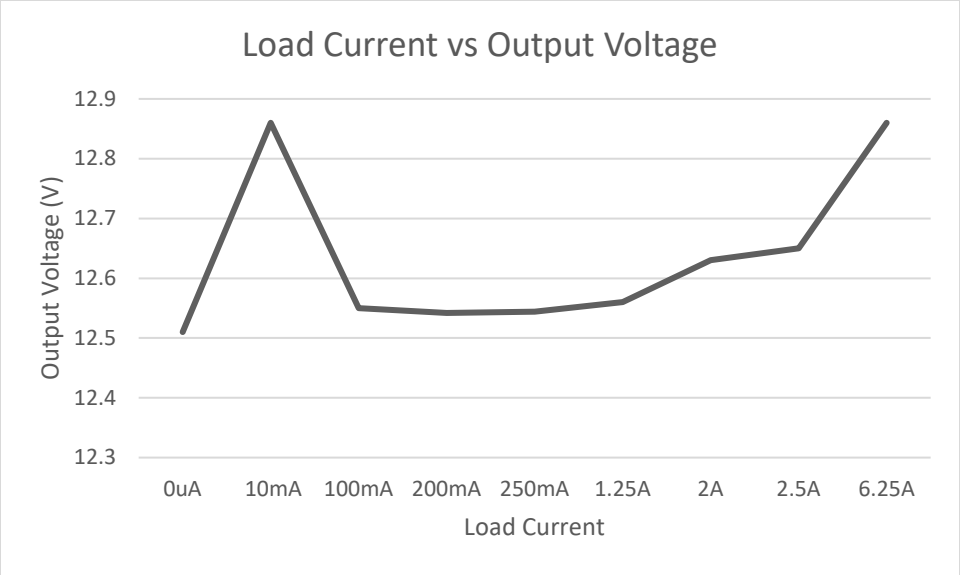

Figure 56 - Load Current Vs. Output Voltage

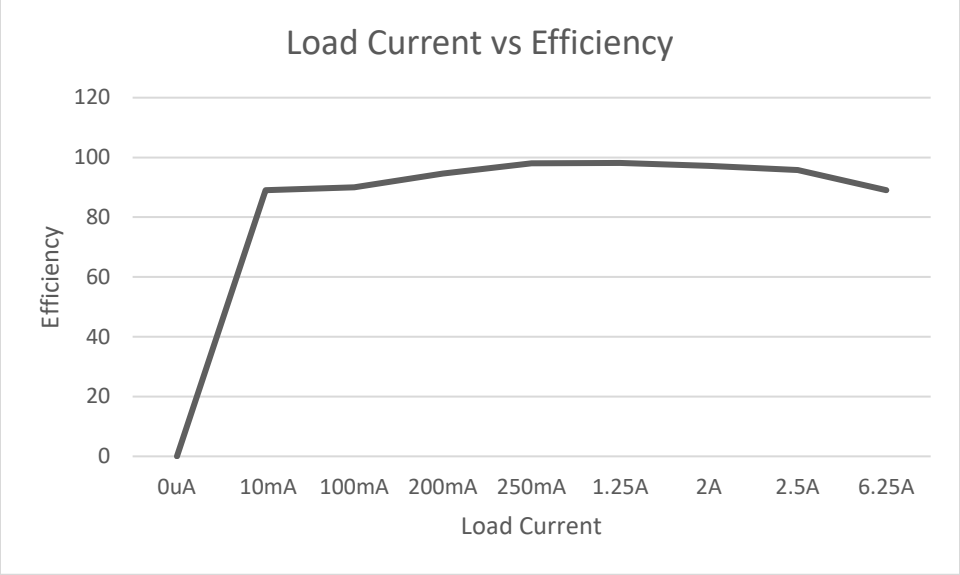

Figure 57 - Load Current Vs. Efficiency

Summary of the Results: The Thesis has been run with several different R-Load resistors to get varying load currents. The circuit runs very poorly when the load current is close to 0. As the results show the circuit works the most efficiently from 10mA to 6.25A. This is good news because this is a large range of current where the circuit works great.

4.4 Trade Offs Table

Design Tradeoffs	
Components	*Description of Tradeoffs*
Comparator Diff Amps	• Transistors sizes of the PMOS and NMOS were chosen to be the normal 12u/600n and 6u/600n, respectively. • Pros – Shorter delays due to the size • Cons – Very large and complicated layout, more power consumption
Ring Oscillator	• Transistors sizes: 12u/6u with the lengths at 600n. • Pros – Easy layout due to copying the same cell, achieved target frequency of 5MHz • Cons – 13 slow inverters, power consumption
Buffer	• Transistors sizes: 12u/6u with the lengths at 600n. I chose a multiplier value of 8. • Pros – drives the 5-pF capacitance that we needed; hand calculations matched to the sim. • Cons – Layout should have been done in serpentine pattern to save space.

Table 5 - Design Tradeoffs

Chapter 5: Future Work

The next step of this Thesis is to connect it to a pad frame. A pad frame is a frame of pads implemented in an integrated circuit. The terminals of the IC are routed to the pads. Wires are then bonded from the chip to the package. The first step is to first make a pad, and later make a frame by adding a total of 40 pads. Later, a schematic is done telling the pad frame where all the connections go. All the pads must be labeled even if they go unused, the connections will be connected to a no connection pin. After the IC chip has been fabricated, the printed circuit board should come next to house the chip. First the IC chip will need to be epoxied on, and then wires should be bonded from the chip to the printed circuit board.

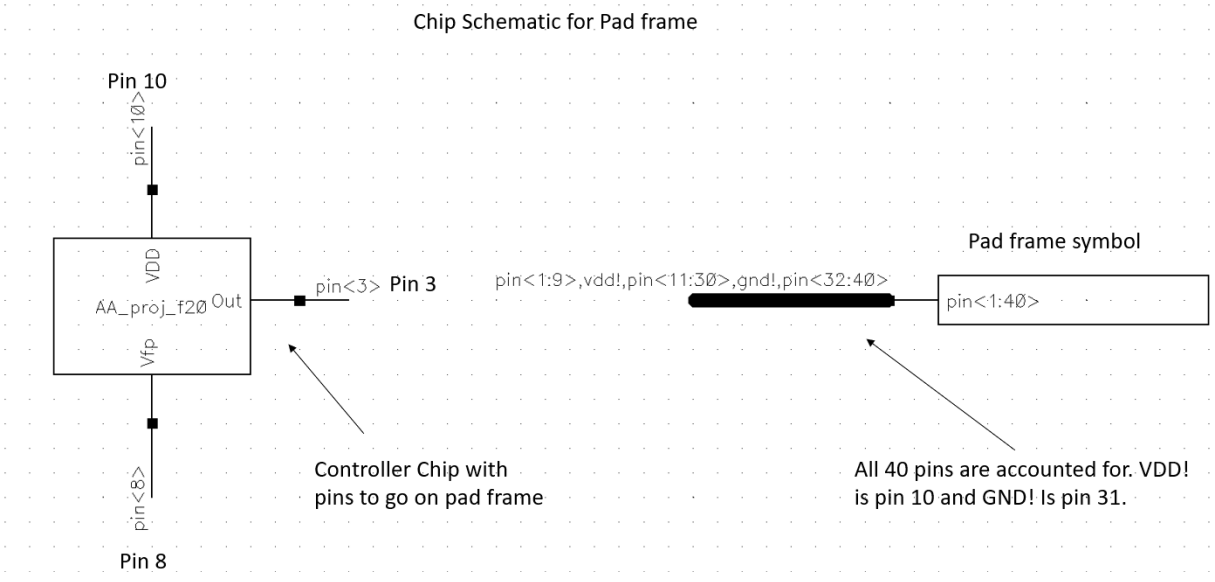

Figure 58 - Chip Schematic for Pad Frame

Here the chip schematic for the pad frame is seen. The Thesis symbol is shown and the VDD is connected to pin10, Vfp is connected to pin 8, and out is connected to pin 3. These pins were chosen due to the layout of the Thesis, the closeness, and ease of the connections that were to be made. The pad frame symbol is also shown. It is important to show that the bus has all the pins shown. Due to the pins that were chosen, this will affect the wire name on the bus that connects to the pad frame symbol.

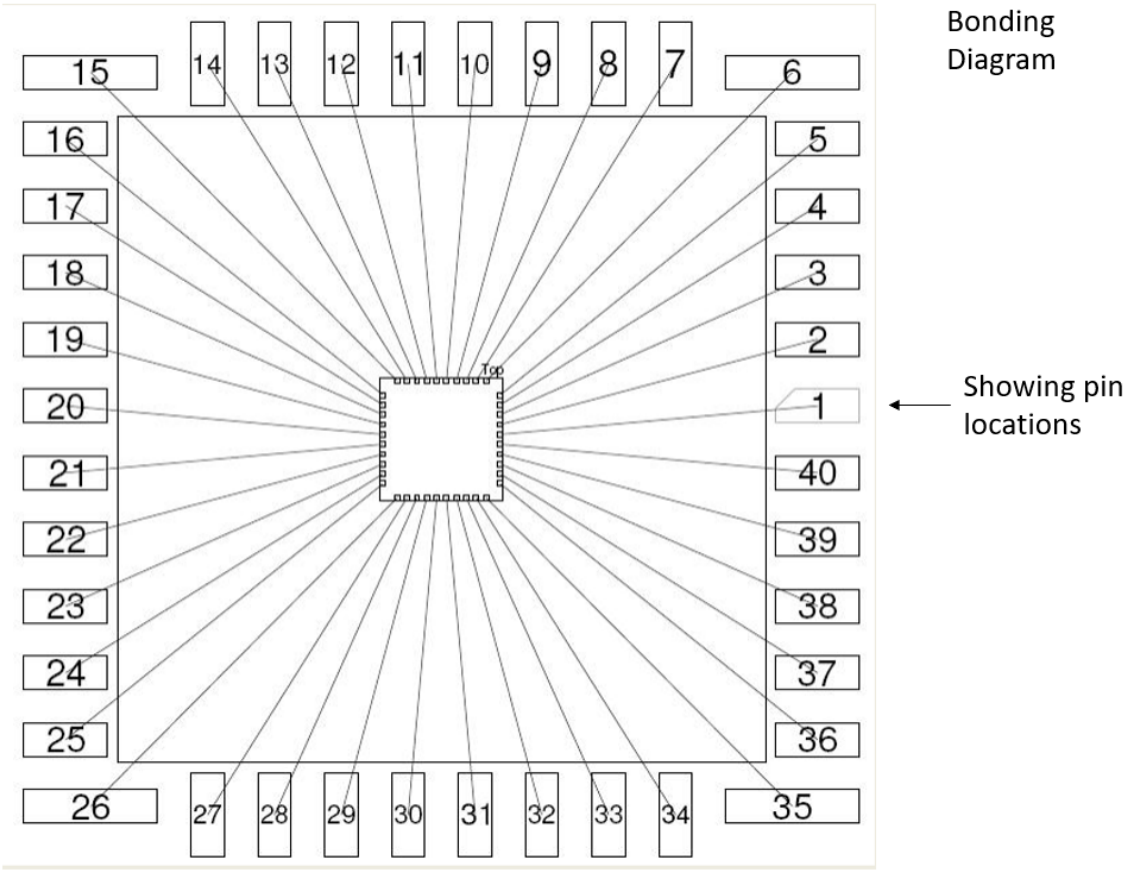

Figure 59 - Bonding Diagram

This diagram shows the typical bonding diagram when it comes to chips. The diagram is showing the pins and their locations. It can be seen that pin 1 is in the middle of the right-hand side, and then the order follows in a counterclockwise direction.

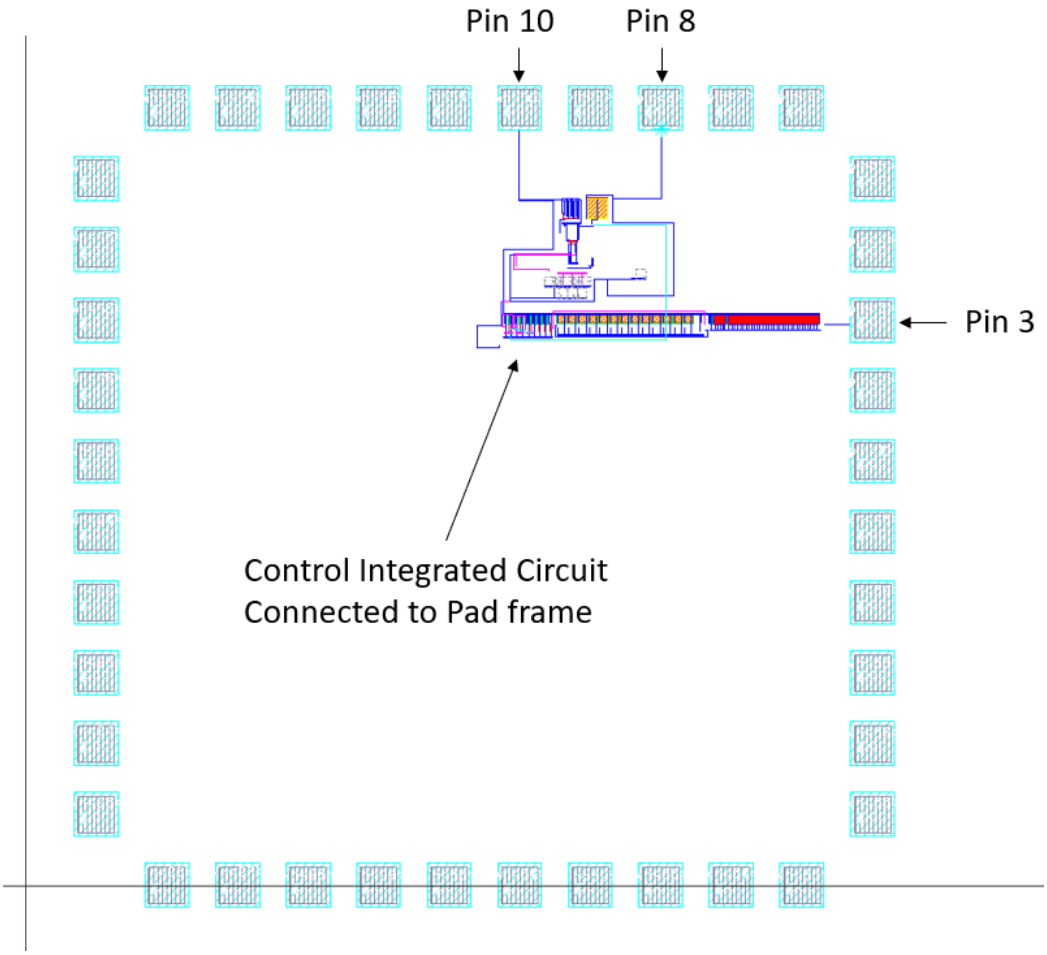

Figure 60 - Control IC Circuit Connected to Pad Frame

Above the control integrated circuit layout is connected to the pad frame. Here it is showing that the pins connected are Pin 3, 8, and 10. The rest of the unused pins will be connected to a nonconnection pin.

After completing this Thesis, there are numerous improvements that could be made for the controller chip to work better. First off, there would be a test for different lengths and widths for the sizes of the comparators. This could have been done in Cadence Virtuoso by making variables called L for length and W for width for when running simulations. Along with testing different lengths and widths, there could possibly be a test to use a different comparator in general. For example, instead of using cascaded n flavor buffers, I would try three cascaded p type buffers, or a combination of both n flavors and p flavors. Another improvement that should be considered is to redesign the ring oscillator. If time permitted there might be a redesign of the ring oscillator where there would be bigger slow inverters, in order to use less of them, in turn hopefully saving power, and potentially space. Although the Thesis did have great efficiency, the hysteresis was still quite too large. 100mV was the target hysteresis for the output voltage, but the lowest that was able to be achieved was 300mV. After laying all the components out, and connecting them, it was realized that the layouts were way too long, especially for the ring oscillator and buffer. Also, the bandgap layout took most of the room for the combined layout. If given the opportunity, the layouts would be redone to save room, making the layouts more functional, and visually appealing.

Another aspect that can be added to this Thesis, is in addition to testing the controller chip with the flyback switching power supply, the controller chip can be tested with the boost switching power supply. It just so happens that there are two topologies that can be used for a controller chip for a switching power supply. One is just a bandgap reference and a comparator that has hysteresis which is used to generate a control signal for the power stage of the switching power supply. The other design which is featured in this Thesis is a comparator which drives an enabled oscillator, then the enabled oscillator drives the output stage of the switching power supply that is needed to regulate and control the Vout. For the first comparator-based topology it works well with the buck switching power supply. The topology with the oscillator works well with the flyback switching power supply, and the boost power supply. The controller chip was tested with the flyback topology, but with future work this controller chip should also be able to work well with the boost topology.

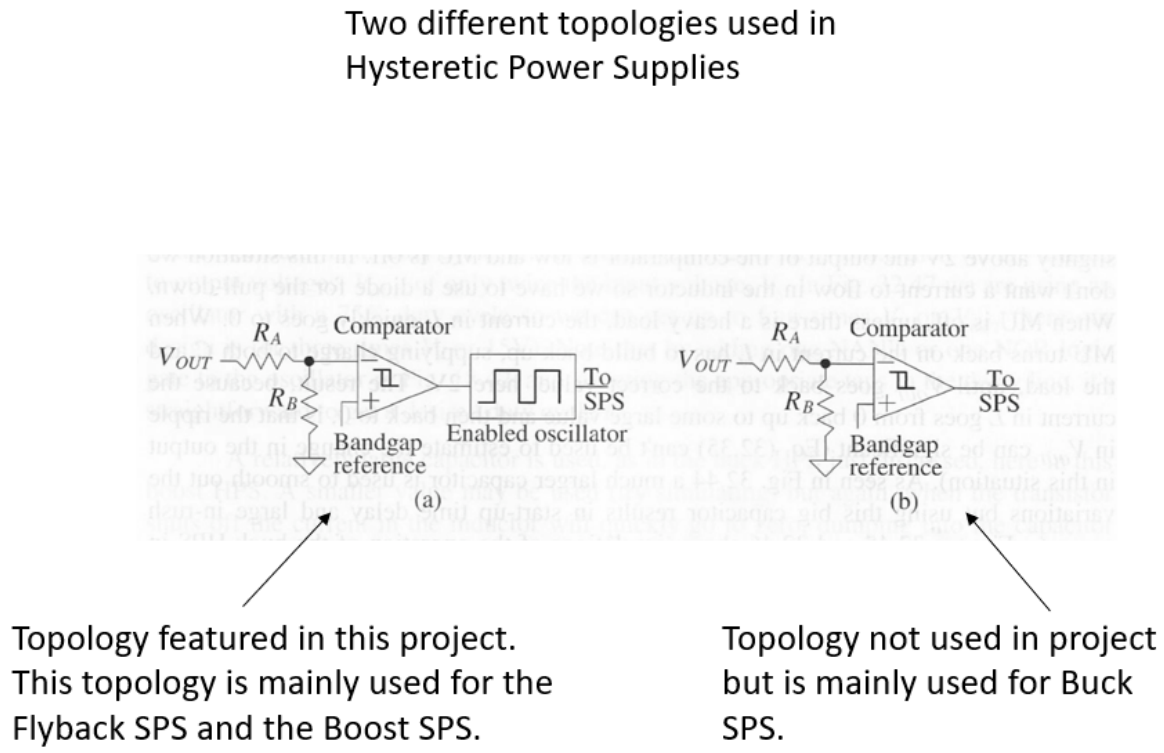

Figure 61 - Showing the Different Topologies Used in HPS [1, Fig. 32.42, p. 1211]

Above are the two different topologies. Again, the left topology is frequently used in flyback and boost switching power supplies applications. The right topology is mainly used in buck switching power supply applications.

Chapter 6: Conclusion

A designer would use a hysteretic power supply because it has a faster response, lower power used in the control circuitry, and has very simply design procedures compared to PWM control. A hysteretic power supply also does not need an op amp which means it will need less energy, consuming less power. There are also disadvantages to using a hysteretic power supply. Some of the drawbacks are that the feedback is more susceptible to noise, and that there is a ripple in the output voltage because of the discontinuous current operation. This Thesis involved doing hand calculations, finding delays, selecting the number of stages for the buffer, and drafting schematics and layouts. Future work would include making a printed circuit board, fabricating, and testing the chip.

Bibliography

[1] Baker, Russel Jacob. *CMOS: Circuit Design, Layout, and Simulation*. IEEE Press, 2019.

Curriculum Vitae

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Education

Master of Science: Electrical Engineering, UNLV **December 2022**

Focus: Electronics, Signal Processing, Power Engineering

GPA: 3.75

Bachelor of Science: Electrical Engineering, UNLV **May 2021**

GPA: 3.62

Experience

Senior Power Electrical Engineer **June 2022 – Present**

State of Nevada

- **Relaying**—develops system, facility and equipment protection schemes and programs; inputs and adjusts relay settings; maintains and operates relaying equipment; and analyzes fault data to determine cause and remedies.
- **SCADA and Metering**—operates and maintains SCADA system; develops SCADA human/machine interface screens for new and renovated facilities using the newest software platform that is compatible with the local utility; prepares and analyzes alarm reports and histories; prepares designs and material procurement specifications for metering equipment; and operates and maintains power metering system.
- **Studies and Reports**—prepares load flow analysis, fault duty studies, load forecasts and fault analysis reports; performs studies on equipment coordination, maintenance practices and programs, including life- cycle analysis; assists in preparation of Standard Operating Procedures (SOPs) for systems, facilities, and equipment; and assists in development of maintenance programs and instructions.
- **Operations**—prepares switching programs, maintains certified switchman status and conducts switching as necessary.
- **Capital Projects**—prepare system, facility and equipment construction cost estimates; prepare procurement specifications for substation equipment, including transformers, power circuit breakers, lightning arresters, capacitor coupled voltage transformers, bus and fitting systems, cabling and conductor systems; review vendor submittals; prepare designs and bill of materials, schematic diagrams and wiring diagrams for relay panels—AC and DC panels; and, prepare designs including one-line, three-line and general arrangement drawings.

Research Assistant **January 2021 – Present**

UNLV

- Design, Produce, and Verify Printed Circuit Boards that were requested with an accelerated timeline of completion
- Solder through-hole and surface mount components on to printed circuit boards, in order to test to see if the board was working effectively

Electrical Design Intern **January 2022 – May 2022**

TJK Consulting Engineers, Inc.

- Corrected power and lighting project elements in Revit/AutoCAD in order for the professional engineer to stamp and sign drawings for projects that are sent out to clients and architects
- Designed electrical distribution and lighting plans for multiple homes, hotels, and schools with AutoCAD, Revit, and Visual Lighting, enabling the learning of design practices that are accepted within the NEC

Engineering Student Intern **May 2019 – May 2020**

NV Energy

- Analyzed large sets of distribution feeder data from 2018 and 2019 for use in upcoming studies that was presented in front of public utility commission, that proved to be vital
- Assisted a team of licensed professional engineers by collecting and analyzing large sets of substation data for northern and southern Nevada that proved to be useful for NWA analyses and hosting capacity studies that were shared to shareholders
- Created sequencing plans based on expected power demand for master plan development projects, that prevented damage and extended the life of power equipment
- Developed phase balancing solutions to power circuits that possess loads near 100% capacity, which made distribution system safer and run more efficiently
- Developed Visual Basic Macros to study large data sets produced by power line telemetry where data was linked from excel into access databases

Projects

- **A Control Integrated Circuit for a Hysteretic Flyback Power Converter** - Design and simulation of a switching power supply controller chip for a fly-back switching power supply that rivals commercial designs due to the performance of varying temperature, voltages, loads
- **Custom Arduino Uno Shield** - Designed a custom prototyping shield for an Arduino Uno by using the Ki CAD software

- **High Speed Digital Receiver** - Design, layout, and simulation of a digital receiver circuit that accepts a high-speed digital input signal
- **Room Monitoring System (IoT Device) for Senior Design** - The Room Monitoring System (RMS) is a system of fully integrated IoT devices that collect, store, process, and display information about a room. The purpose of the RMS is to increase the efficiency of hotel staff by providing data at the glance of an eye

Technical Skills

- Auto CAD, C++, Cadence Virtuoso, Dip Trace, Ki Cad, LT Spice, MATLAB, Microsoft Office, Power World, Quartus, REVIT, Soldering, Synergi Electric, Visual Lighting