Overview of Packaging DRAMs and Use of an RDL

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ECG 721, Fall 2021, Dr. Baker

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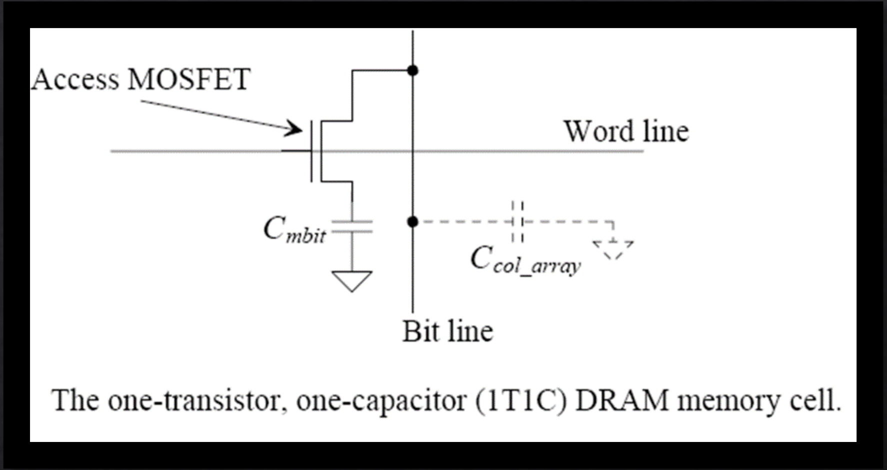
What is DRAM?

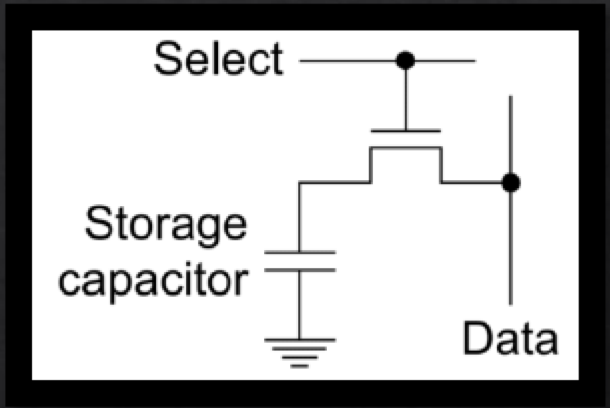
- DRAM – Dynamic Random-Access Memory
  - Usually utilizes a memory cell consisting of <u>one transistor and one capacitor (1T1C)</u>
  - A bit is represented as a “1” or a “0” depending on the state of charge of the capacitor
  - Refresh process is integral to proper operation (“dynamic”)
  - Data is quickly lost when power is removed (volatile)



1T1C DRAM Memory Cell [7]

DRAM Uses

- Pros: simple design, relatively low cost, relatively fast
- Cons: volatile memory, relatively high power consumption, complex manufacturing, refresh is integral to proper operation
- Usually found on integrated circuit chips
  - Tens to billions of memory cells depending on the application
- Commonly used in low-cost, high-capacity computer memory electronics
  - Ideal in systems where speed is a main priority
  - Used in PC’s, video game consoles, and many portable devices [1]



1T1C DRAM Memory Cell

DRAM Types

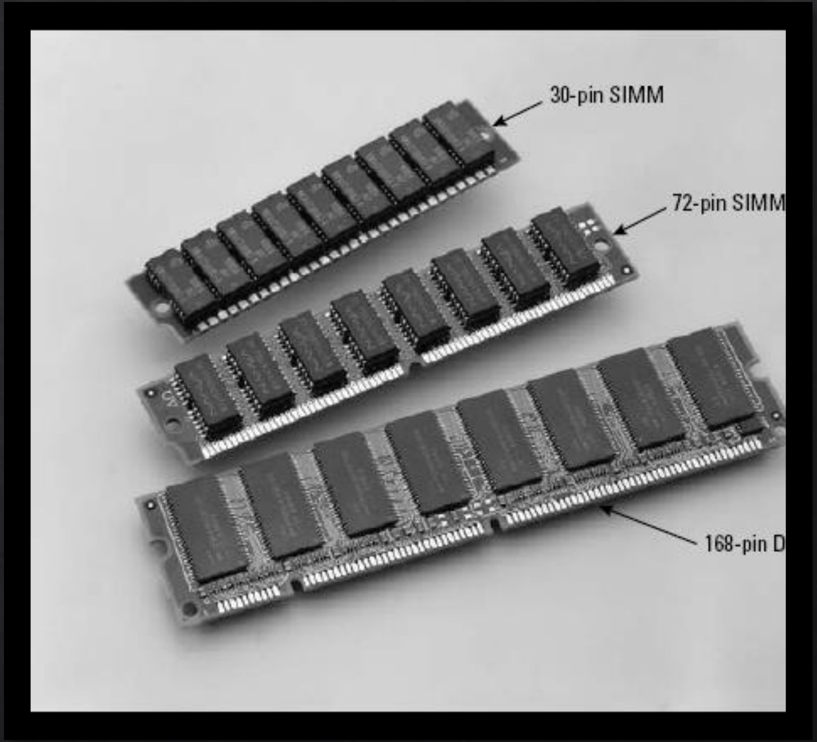
- Synchronous DRAM (SDRAM) – syncs memory speeds with clock speeds
- Double Data Rate SDRAM (DDR SDRAM) – double pinning is used to almost double the bandwidth in data rate; data is transferred on both rising and falling edges of the clock [8]
  - DDR1, DDR2, DDR3, DDR4, DDR5 – upgraded standards (shown on table)
- Fast Page Mode DRAM (FPM DRAM) – focuses on fast page access, allowing for higher performance
- Extended data out DRAM (EDO DRAM) – improves time to read from memory [1]
- Major manufacturers: Samsung, PNY Technologies, SK Hynix, Micron [8]

Table showing sample specs for upgrading standards of DRAM

DDR SDRAM Standard	Internal rate (MHz)	Bus clock (MHz)	Prefetch	Data rate (MT/s)	Transfer rate (GB/s)	Voltage (V)
SDRAM	100-166	100-166	1n	100-166	0.8-1.3	3.3
DDR	133-200	133-200	2n	266-400	2.1-3.2	2.5/2.6
DDR2	133-200	266-400	4n	533-800	4.2-6.4	1.8
DDR3	133-200	533-800	8n	1066-1600	8.5-14.9	1.35/1.5
DDR4	133-200	1066-1600	8n	2133-3200	17-21.3	1.2

DRAM Modules

- There are two main ways of packaging DRAM:
  - Single Inline Memory Module (SIMM) – used in 1980s and 1990s [2]
    - Typically had 32-bit transfer rates
  - Dual Inline Memory Modules (DIMM) – commonly used now [2]
    - Typically have 64-bit data transfer rates
    - Has pins on both sides of the chip, and usually support 168+ pin connecters
- The main difference between SIMM and DIMM is the amount of pins each module has; DIMMs have twice as many pins because there are different connectors on either side [8]
  - This allowed DIMMs to become a replacement technology for SIMMs

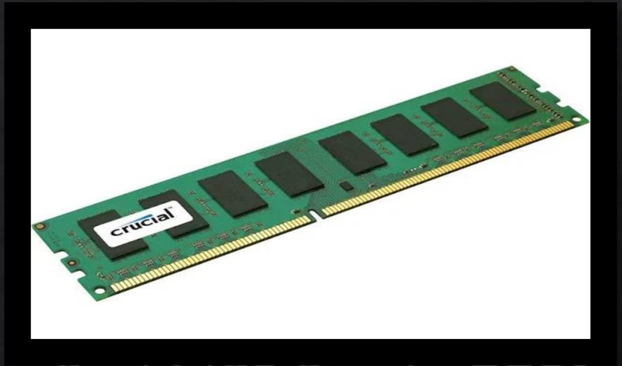


SIMM vs DIMM – notice that the 72-pin DIMM is around the same size as the 30-pin SIMM (but with double the pins) [4]

DRAM Modules: DIMM

- Different IC architectures are set as package types for DIMM [1]
  - Unbuffered DIMMs (UDIMMs) - commonly used in laptops/desktops
    - Pros: faster speed, lower price
    - Cons: decreased stability
  - Registered DIMMs (RDIMMs) – commonly used with servers requiring stability and robustness
    - Pros: increased stability
    - Cons: slower speed (also known as “buffered” memory) [2]

Micron 4GB DDR3 1600MHz 240 Pin Unbuffered DIMM
US $15.00



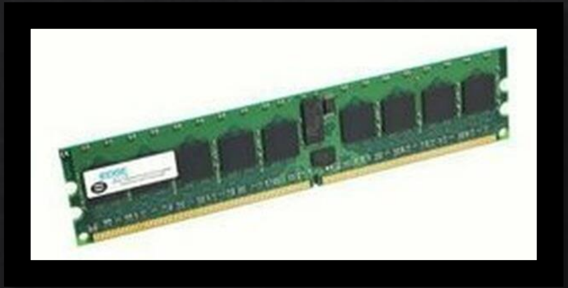
Crucial 4GB Capacity, DDR3 PC3-14900, 240-Pin DIMM
$75.76

DRAM Modules: DIMM (Cont.)

- Fully Buffered DIMMs (FB-DIMMs) – commonly used in larger memory systems
  - Pros: increased reliability, improved error detection, bigger capacity
  - Cons: slower speed

Edge Memory PC25300 ECC 240 Pin Fully Buffered (PE20746502)
US $49.60

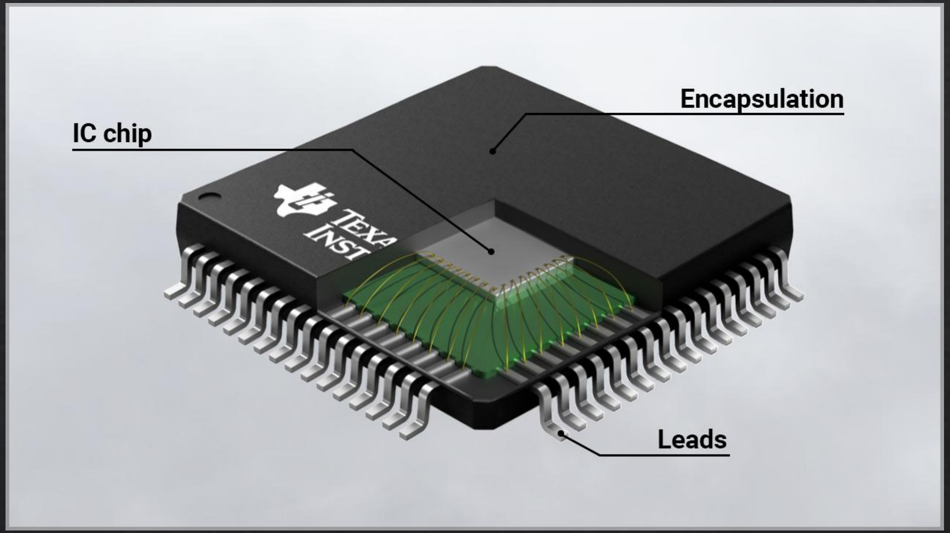
- Load Reduced DIMMs (LR-DIMMs) – used in largest possible memory footprints; use Isolation Memory Buffer technology to reduce load by buffering data and address lanes
  - Pros: largest capacity
  - Cons: slower speed



Edge Memory PE243869 DDR3 - 64 GB - LRDIMM 240-Pin
$839.27

What is Chip Packaging?

- Packaging is used as a means of encasement that usually occurs during the final stage of fabrication of a device
  - Necessary to maintain cleanliness, prevent corrosion, and avert damage [1]
- The package creates a means of connection from inputs/outputs to an outside circuit



Cross section of an IC showing the chip, leads, and encapsulation (package)

Evolution of DRAM Packaging

- In the early 2000s, a switch from TSOP packaging to FBGA was made [3]
  - Allowed for higher density
  - New generations of DDR (DDR2 and newer) used FBGA technology

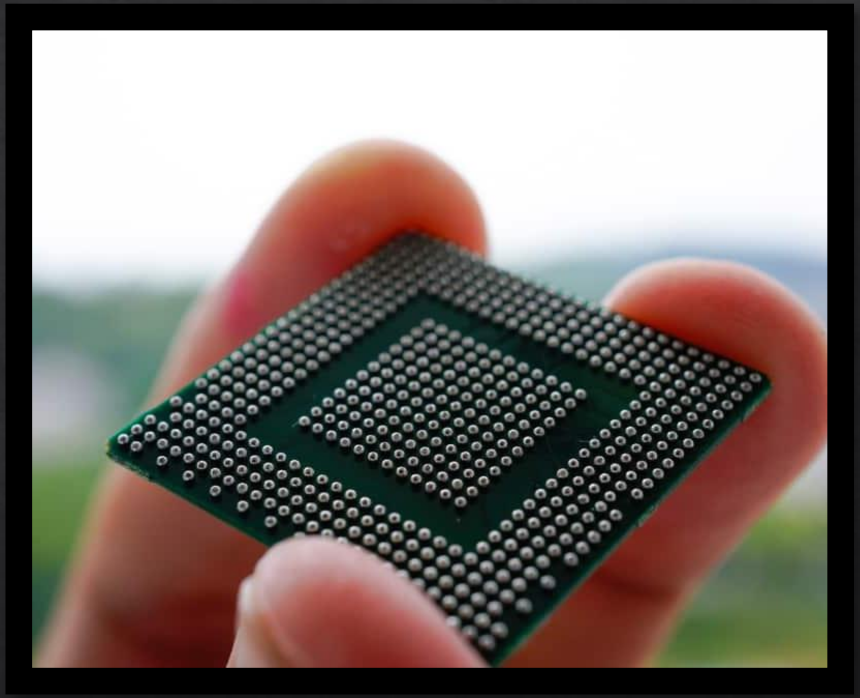
Thin Small-Outline Packaging (TSOP)

- Thin Small-Outline Packaging is a surface mount IC package that was used
  - This packaging is basically obsolete with new DRAM generations standard
    - Standard with DDR1; later standards used FBGAs (next slide)
  - Small density because each pin protruded from encasement
  - Two types
    - Type I: 28,32,40,48, or 56 pin options
    - Type II: 6, 20, 24, 28, 32, 40, 44, 50, 54, or 60 pin options
      - 54 pin shown in image

SDRAM 128Mbit 3.3V 54-Pin TSOP-II
(Part is now obsolete)

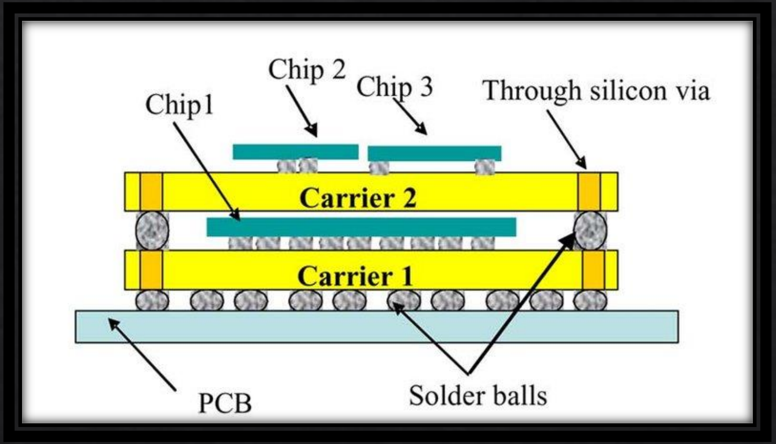
FBGA Packaging

- Fine Pitch Ball Gate Array (FBGA) is a method of packaging that uses an array of solder balls as pin connections
  - Surface mount package
  - Most commonly used with DDR2, DDR3, DDR4 and DDR5 (new standard)
  - Near chip-scale (differs from BGA)
  - Pros: High density, better heat dissipation, increased performance, lower inductance [anysil]
  - Cons: Inability to inspect the package after soldering, proper soldering technique must be used
    - Solder balls can encompass entire face of package



Stacking

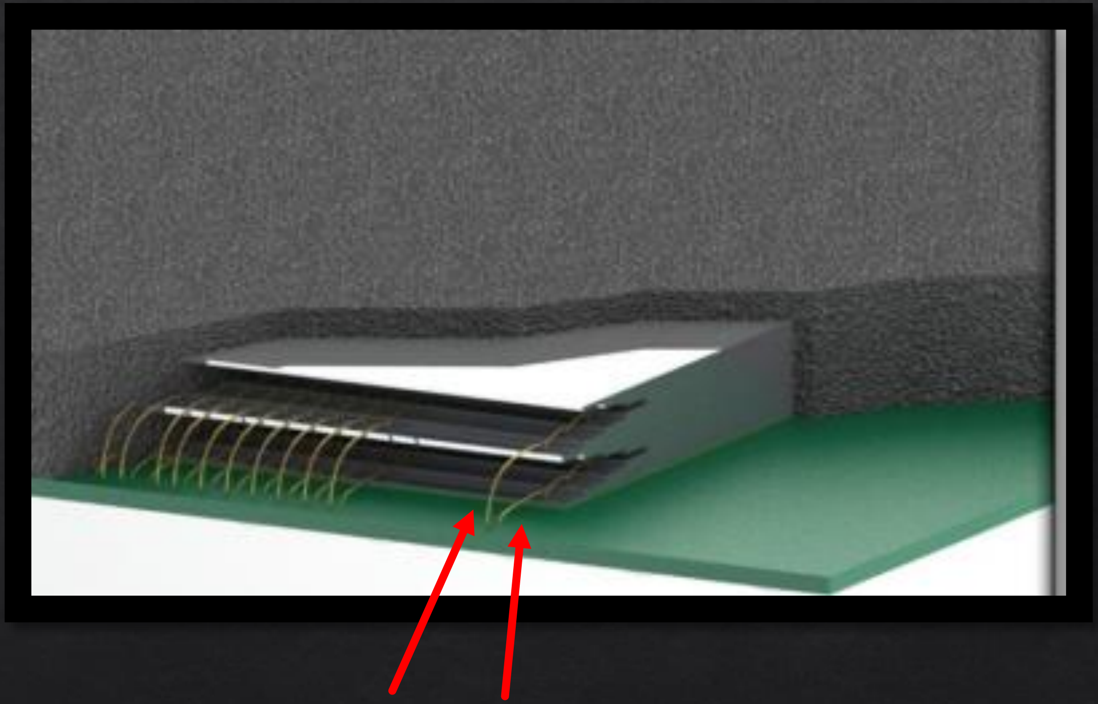
- The number of dies in a package correspond to the number of memory chips
  - These dies can be stacked to allow for double, triple, ect. of the memory density
    - Stacking allows for a significant decrease in the amount of real estate that these die would individually take up
    - Can also result in better electrical performance of the device, as there is a shorter routing of interconnections between circuits (ie. a smaller propagation delay)
- In DRAM, the name for the number of identical die stacked in a package:
  - Single Die Package (SDP) – 1 die
  - Double Die Package (DDP) – 2 die
  - Three Die Package (3DP) – 3 die
  - Quad Die Package (QDP) – 4 die



Cross sectional view of stacked die (3DP)

DRAM Packaging Tradeoffs

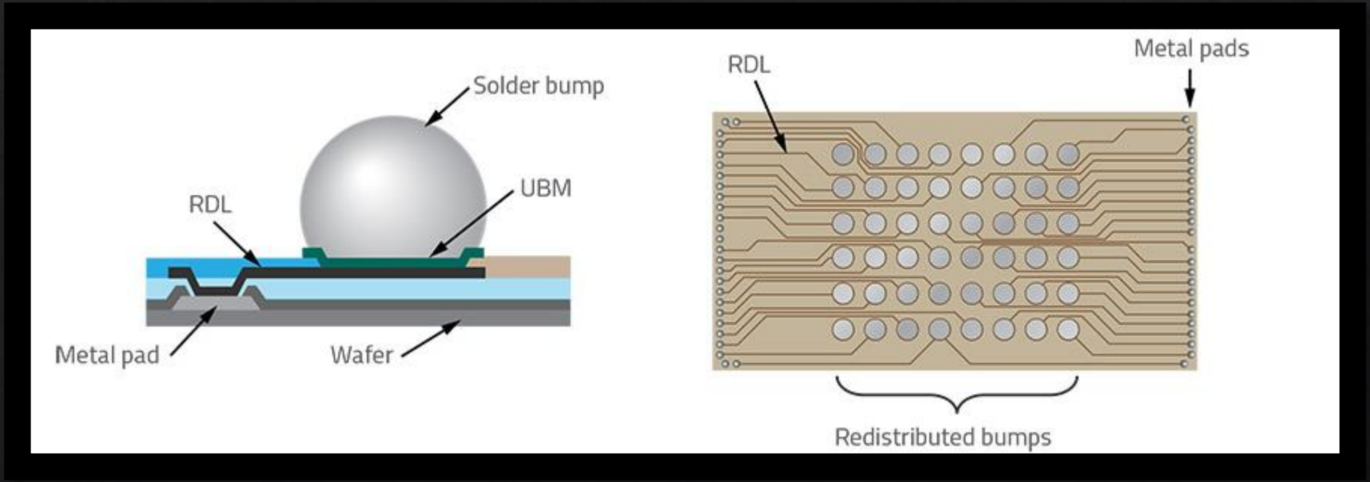
- When deciding how to package a DRAM, there is a tradeoff between <u>speed, cost, bandwidth and density</u>
- As the density increases (dies are stacked, cost goes up), the distance between the connections from the chip to the package will increase, meaning that the speed will decrease
  - This is usually still a better alternative than non-stacked methods
  - <u>As density increases, cost increases, speed decreases</u>



Notice that the top wire bond is longer than the bottom one; the speed will be decreased

Packaging Methodologies: Redistribution Layer

- The Redistribution Layer (RDL) is defined as the metal wiring and dielectric layer that can be used to route the position of an input/output pad to a new location on the package (usually on the edge of the chip)
  - Redistribute pins to different parts of the chip to make them easier to access
  - Added on top of the die
- Example: Bump array in the center of a chip can be rerouted to the edge of the chip so that it can be bonded to/from



RDL Process Steps

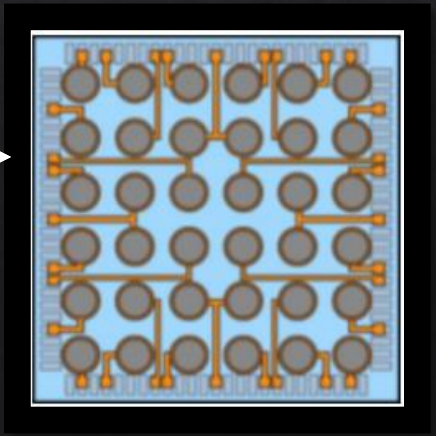
- The steps in adding the redistribution layer revolve around adding a metal later that connects to the current bonding pads and routes to a new location. [5]
- This is especially useful for pins that need to be accessed that are located in the center of the chip
- Single layer and two later routing (using the substrate)

Dielectric film is deposited (for electrical isolation) → Original bonding pads are exposed → Metal lines are deposited to reroute the pads to their new locations → Under-bump metallization layers are created to support solder bumps

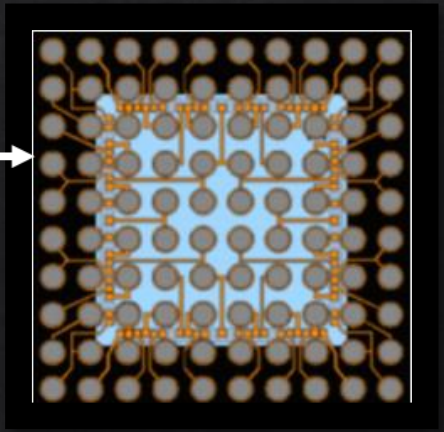
Advanced RDL Technology

- Fan-out packaging was developed in the early 2000s to combat the issue that arose when larger numbers of I/Os were required
  - Results in a package around the same size as the die itself
  - Allows for redistribution of I/Os beyond the surface of the die
  - Creates suitable structure for wire bonding
  - Good electrical connectivity
- Fan-in packaging routes all traces toward the center of the die

Fan-in packaging – notice the traces being routed toward the center of the die

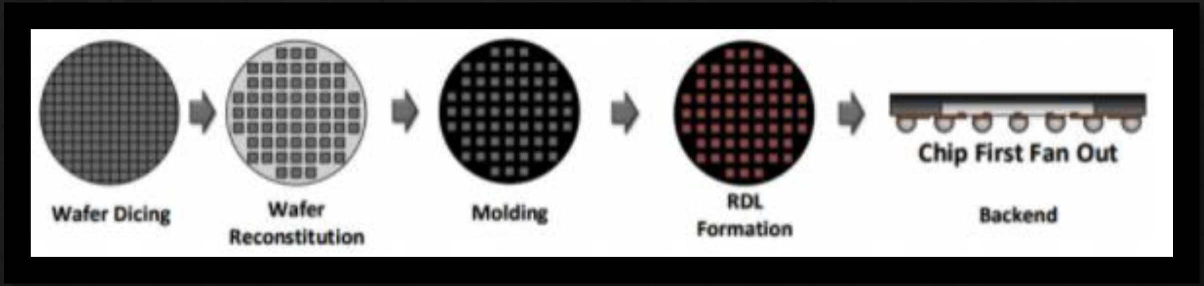


Fan-out packaging – notice the traces being routed toward the edges of the die

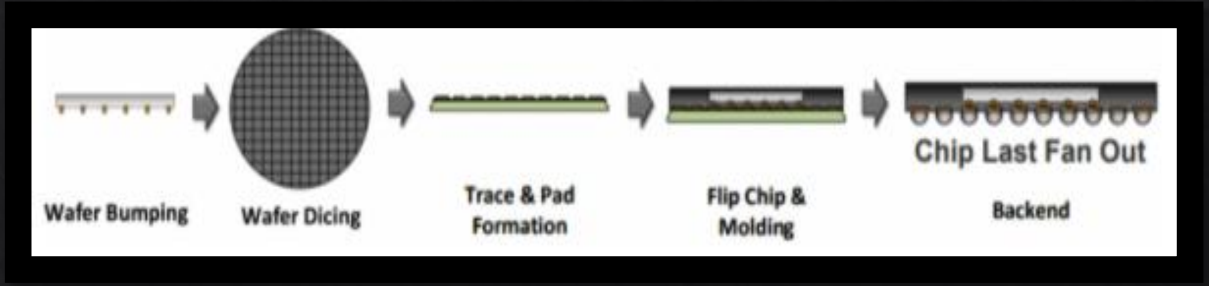


Advanced RDL Technology (Cont.)

- Two primary fan-out structures:
  - Chip-First: chips are embedded, followed by the RDL
    - Lower cost
    - Limited use in multi-chip packaging because of die shift/protrusion
  - Chip-Last (RDL first): RDL is pre-formed on wafer, then chip is integrated into the packaging
    - Increased reliability
    - Allows for fine pitch scales (2um)



Chip first fan-out process



Chip last fan-out process

Packaging Methodologies: Wire Bonding

- Wire bonding is a method of connection through means of metal wire – in this case, between the package and the chip
  - Dominant technology for chip-to-package connections
  - Usually uses wire made of gold and pads made of nickel-palladium or aluminum [5]

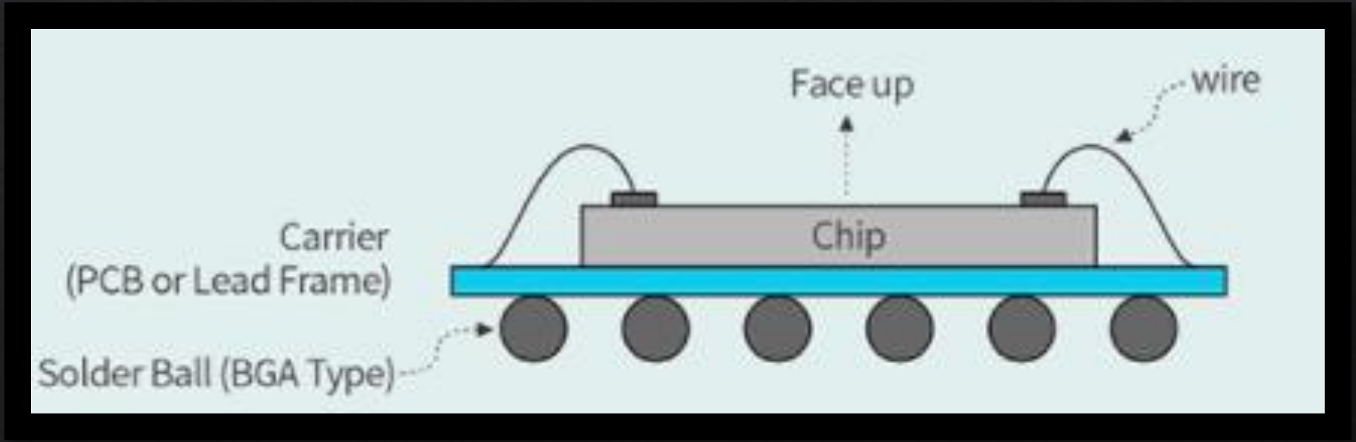
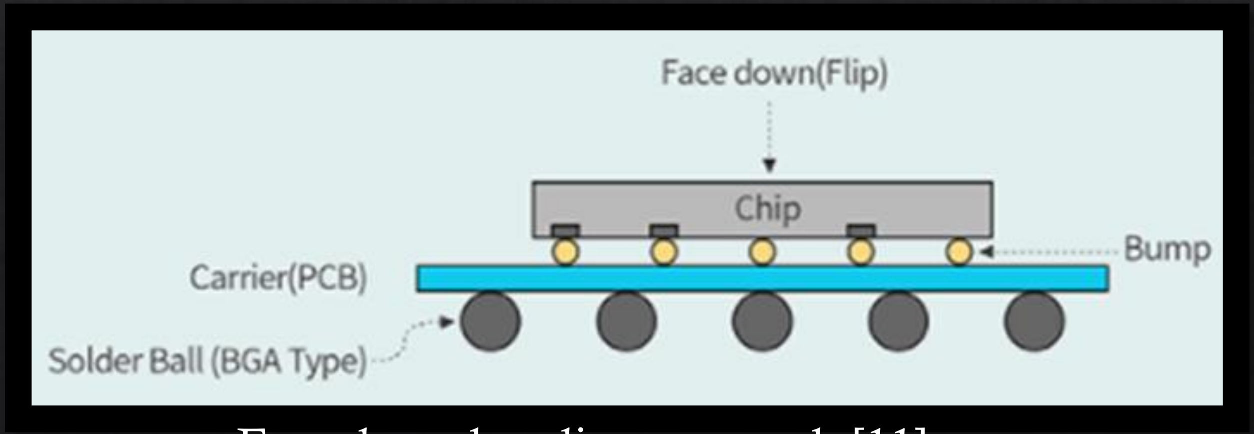


Image showing chip to package wire bonds – notice the bonding occurs on the edge of the chip [11]

Packaging Methodologies: Flip-chip Bonding

- Flip-chip (FC) is traced back to the 1960s [9]
  - Makes up for just under ten percent of memory packaging market
  - Increased integration into PC/server applications because of high bandwidth requirement [11]
    - DDR5 is expected to move heavily toward FC
- Method uses a "face down" chip, where top of chip is facing the bumps



Face down bonding approach [11]

Packaging Methodologies: TSV

- Through Silicon Via (TSV) is a method of electrical connection that allows for a vertical connection that goes through a die
- Creates shorter electrical paths (clear in the figure) → leads to faster device
- Useful in die stacking techniques
- Very small sector of current market, but usage is expected to grow because of its high bandwidth ability

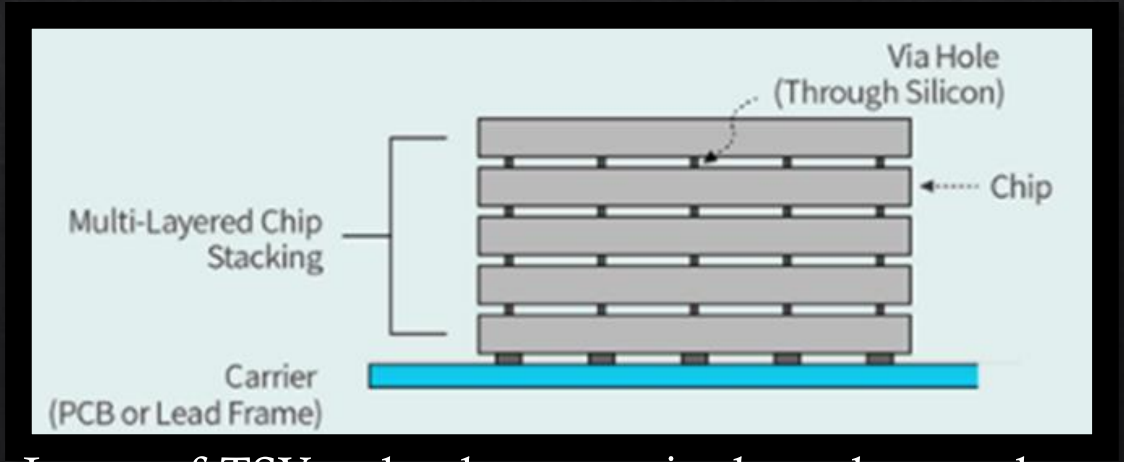
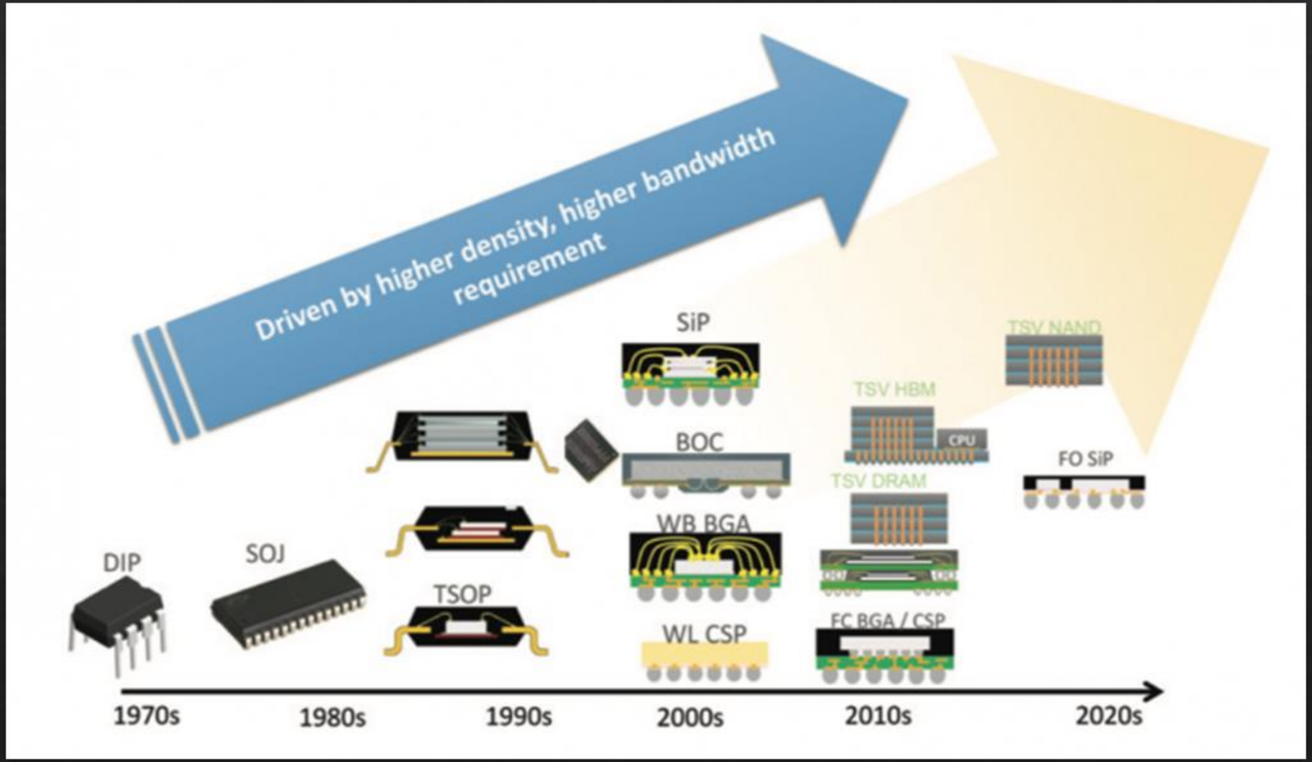


Image of TSV technology – notice how short each electrical path is; also notice the use of the stacked die [11]

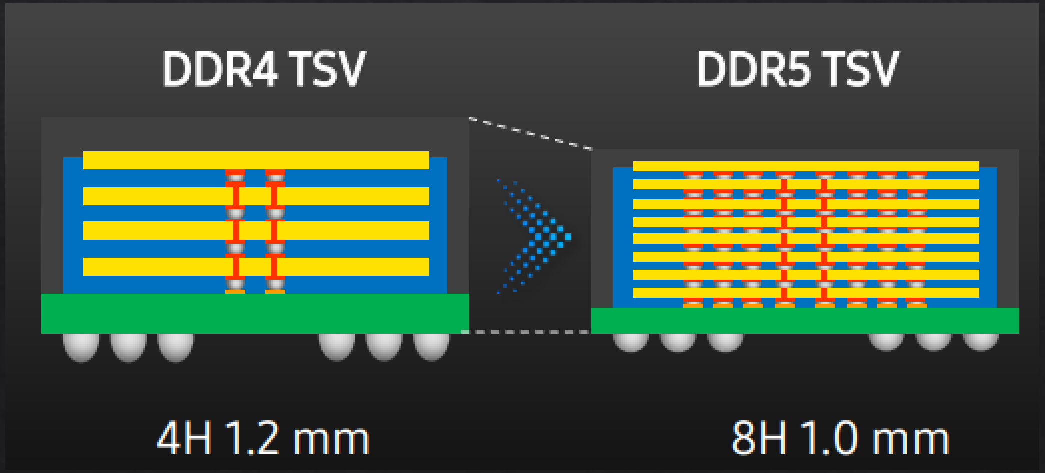
What's Next?

- The future in memory packaging surrounds finding ways to make speed, density, and bandwidth lower [10].
- Strong demand coming from mobile and computing markets (to be expected)
- Trends are leaning toward BGA devices staying the most popular, but FC technology is expected to grow to almost 15% of the memory market by 2022 [9].



What's Next? (Cont.)

- DDR5 was released in July of 2020 but is expected to become the new standard for SDRAM by 2023 [9].
- Reduces power consumption and doubles the bandwidth in comparison to the DDR4 standard



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