A High-Speed Transimpedance Amplifier

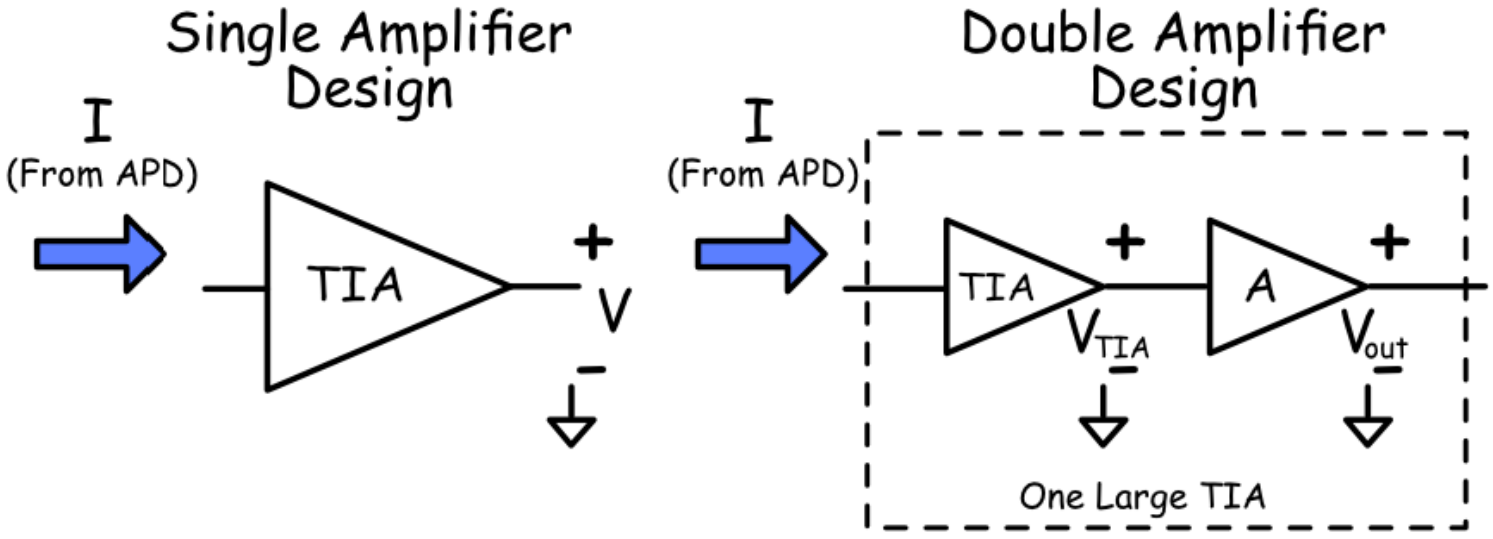
By David Santiago
ECG 720 – Advanced Analog IC Design
Spring 2021

Abstract

The purpose of this project is to demonstrate the fundamentals of a transimpedance amplifier (TIA), how to change certain parameters, and to use to detect current impulses from an avalanche photodiode (APD).

Two designs will be considered: A design in which we have one amplifier that expects a current input and outputs a voltage, and a design in which a second amplifier is in series to the first amplifier and takes in a voltage input and converts it into a voltage output.

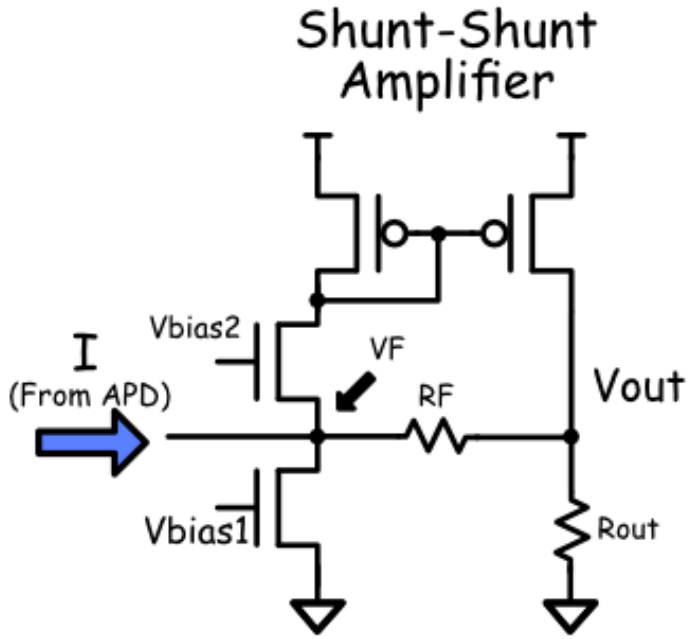
In picture form:



Note that in the above figure, a current will always be at the input stage of the amplifier, and the output stage will always be a voltage.

From the first design, the transimpedance amplifier is also known as a Shunt-Shunt (Current In, Voltage Out) amplifier, in which the input is shunted to the feedback node, and the output is also shunted to the feedback node. In the double amplifier design, the added second amplifier is a voltage gain amplifier, which can be used to ease the loading on the first stage TIA and extend the bandwidth.

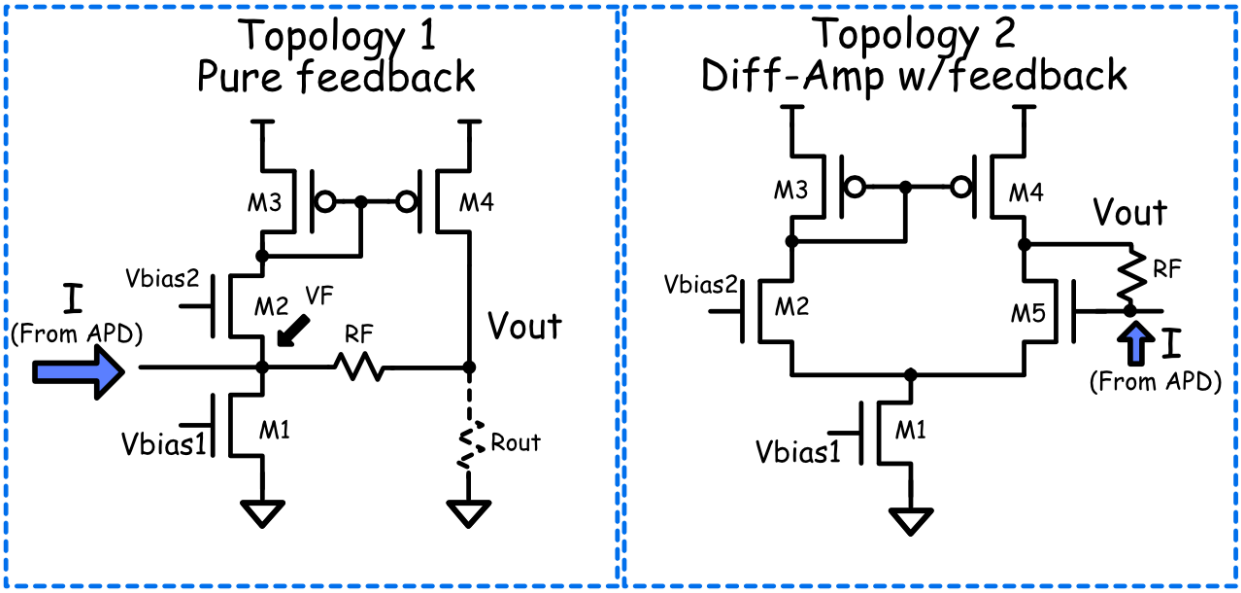
In picture form (as an example):



From above, the input current flows towards the feedback node and mixes with the feedback current, and the output is shunted towards the feedback node.

Stage 1: The Transimpedance Amplifier

Two designs will be explored: A topology that relies on a pure resistive feedback, and one that relies on a differential amplifier with feedback.



Topology 1:

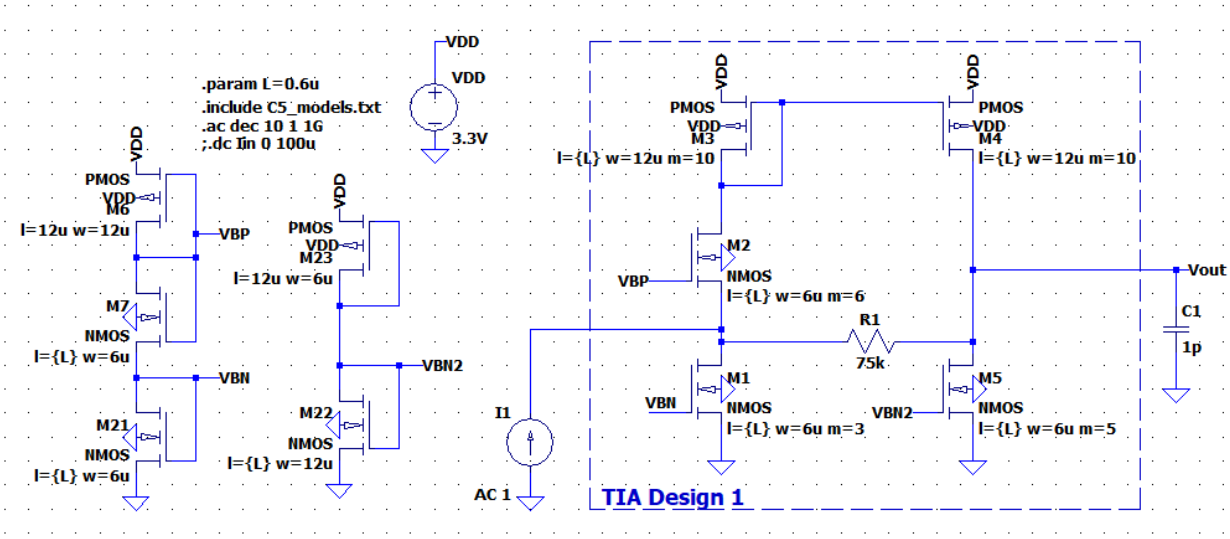
With the first topology, we note that the Open-loop gain, A_{OL}, can be estimated by (using parameters defined in the block diagram above):

$$\left|\frac{V_{out}}{I_{in}}\right| = \frac{R_{M3}}{\frac{1}{g_{M2}} + R_{M1}} \cdot \frac{R_{out}}{\frac{1}{g_{M4}}}$$

From the above equation, to increase the gain, it would be obvious to make the resistance at the output node (Vout) a large value and also make the resistance at M3 large.

We can use an NMOS current mirror there so that we can have a higher output impedance at that node.

The following simulation was created:



Things that were considered for this design:

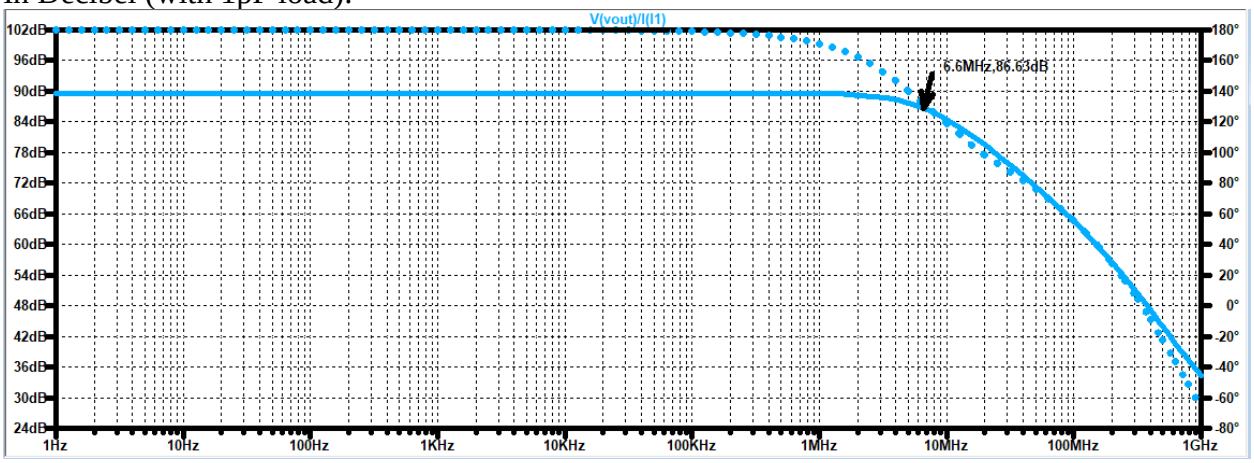
- Three separate bias voltages were created, each controlling a different NMOS device. This is used to vary the resistances of each one freely.
- The resistance of M5 should be large, therefore the bias voltage at the gate of M5 should be small.
- Ideally, M1 should be small however, practically if the resistance at M1 is small, it will literally be shorting to GND and therefore make this amplifier impractical.
- The PMOS M4 can be sized up to increase the transconductance, however at the cost of current.

The negatives for this design can be described by:

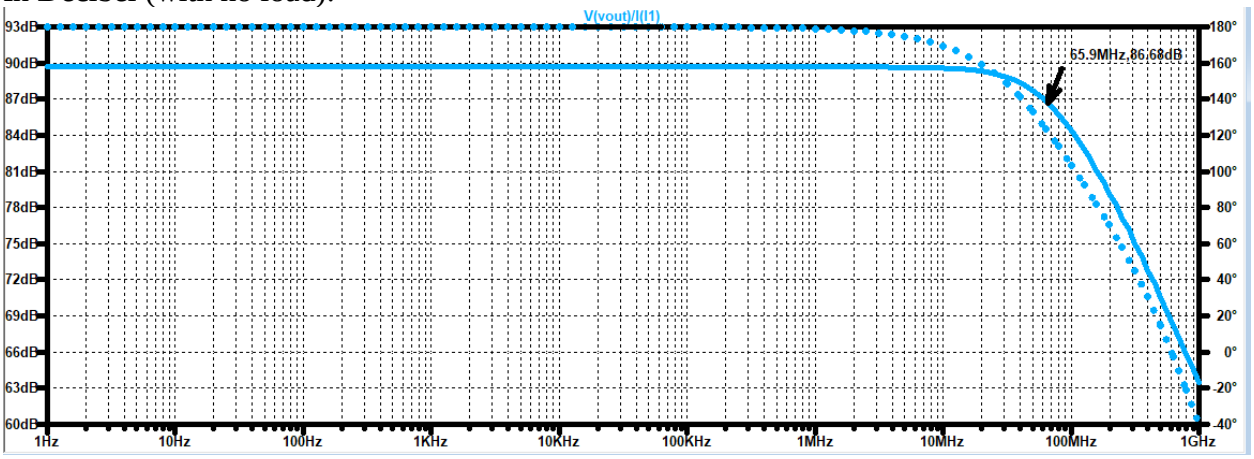
- In a later simulation, the MOSFET bias voltage generator will be a function of VDD, and therefore affect the transimpedance amplifier.

- The feedback resistance is large to achieve a large gain, however, depending on the materials of the resistor, a propagation delay may be present that the simulation does not account for and the circuit may not properly work after fabrication.
- The circuit contains many current mirrors that will all fight against each other (PMOS vs NMOS) and will be hard to bias correctly.

Quick Simulation:
In Decibel (with 1pF load):



In Decibel (with no load):

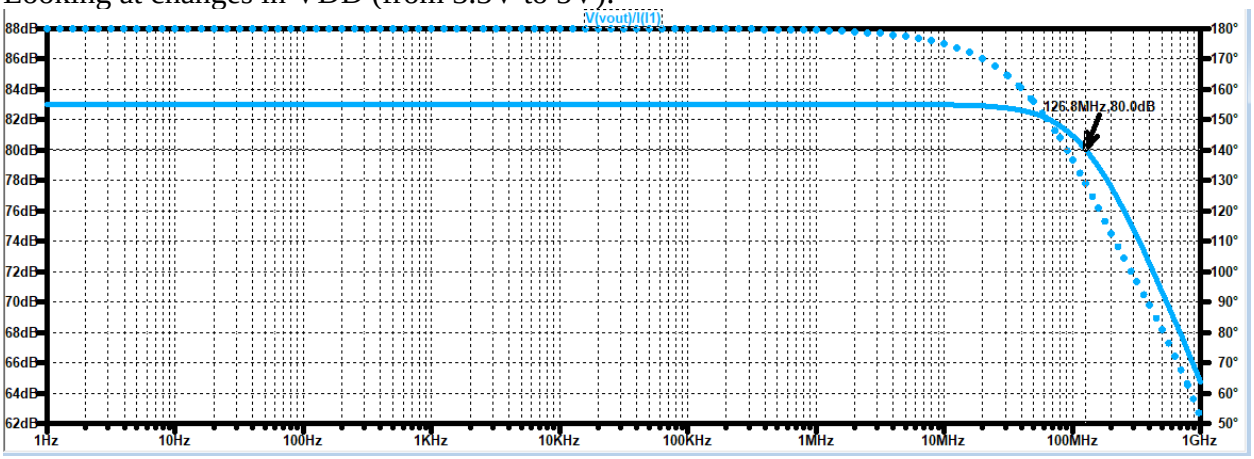


From the above, we see that the gain is high, however the circuit is only able to get up to 7MHz and this is due to the natural RC circuit that is achieved between the large resistance at M4 and 1pF capacitor. By estimation,

$$R \approx \frac{1}{2\pi fC} = \frac{1}{2\pi 7MEG \cdot 1p} = 22k\Omega$$

From this calculation itself, this is foreshadowing why a second stage amplifier is needed to reduce this output resistance so that the knee frequency (bandwidth) can be extended.

Looking at changes in VDD (from 3.3V to 5V):



Or in terms of Linear, we get a gain of 14kΩ, which does not meet the gain requirement. We could tinker with the bias voltages; however, this is considered bad design if parameters should be changed to meet certain specifications.

If one were to design for a Low-Power, High Gain Transimpedance amplifier, this design will work phenomenal as the current in each branch is relatively low at 3.3 volts.

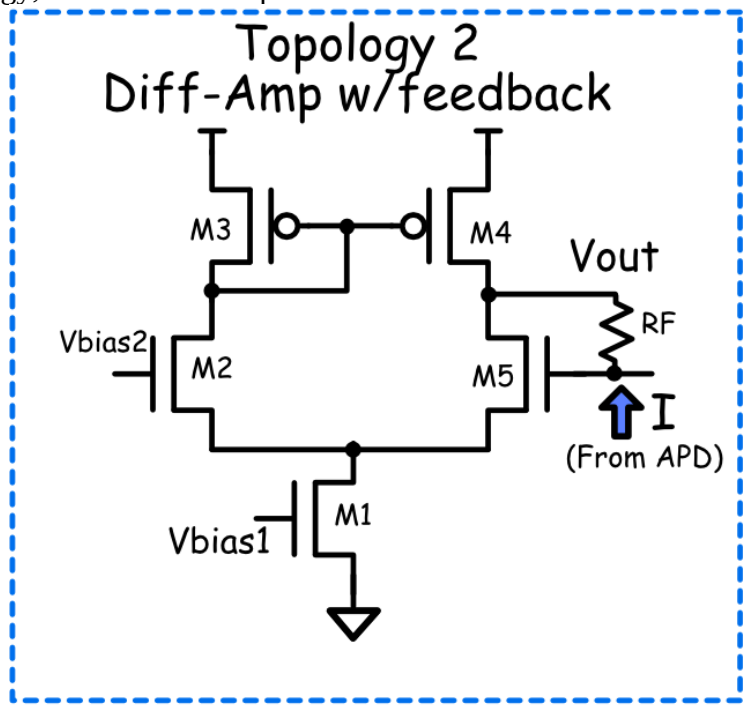
Summary of the 1st Shunt-Shunt TIA design:

VDD		3.3V	5V
Gain		30.4kΩ	14.2kΩ
Bandwidth (No Load)		65.9MHz	126.8MHz
Bandwidth (w/ 1pF Load)		6.6MHz	11.4MHz
Estimated Output Resistance (using Loaded Bandwidth)		22kΩ	14kΩ
Current consumed		60µA	371µA

From the above table, we can see that if we use more current (which increases the transconductance), our output resistance lowers which then extends our bandwidth.

Topology 2:

For the next topology, a differential amplifier will be used.



Calculating the gain:

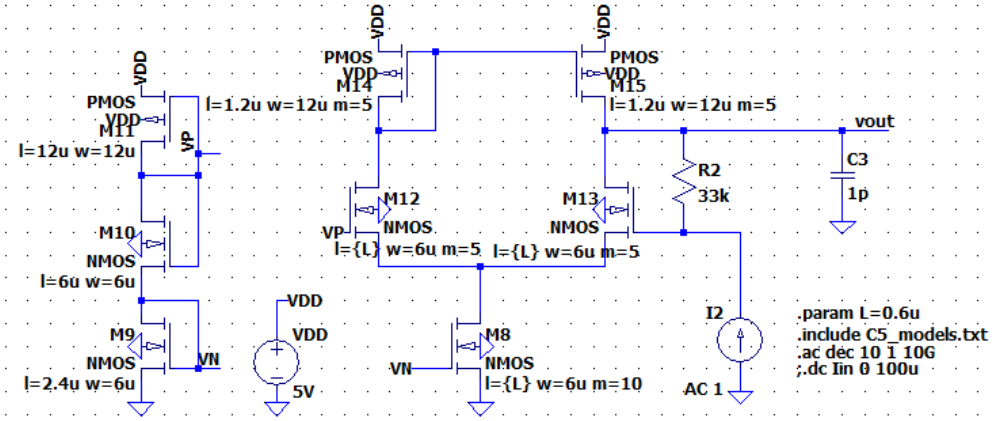
$$\left|\frac{V_{out}}{I_{in}}\right| = g_{m,M5} \cdot R_F \cdot \left(R_{o,M5} || R_{o,M4} || R_F\right)$$

From this, we can increase the gain by increasing the transconductance parameter, or by increasing the feedback resistance.

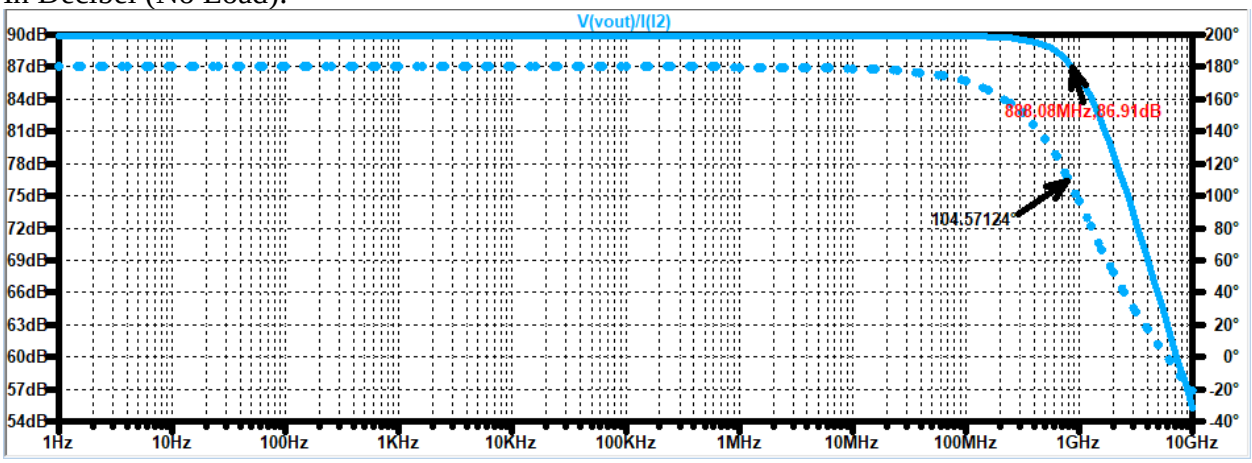
Considerations for this design:

- There are only two bias voltages to generate, and are simple to create.
    - A lot of current in the bias generator can also be saved in this circuit by adjusting the length of a PMOS device to be longer and keep the voltages relatively on due to being gate-drain connected diodes.
- The widths of the diff-amp can be increased to push out the bandwidth, however, there is a certain point where Q-Peaking can be observed and can make the TIA oscillate and go unstable.
- The open-loop gain can also be increased by lowering the widths of the PMOS current mirrors, or increase the lengths, at the cost of bandwidth. Another positive of increasing the lengths is that the input-referred noise contribution of the PMOS devices will shrink.

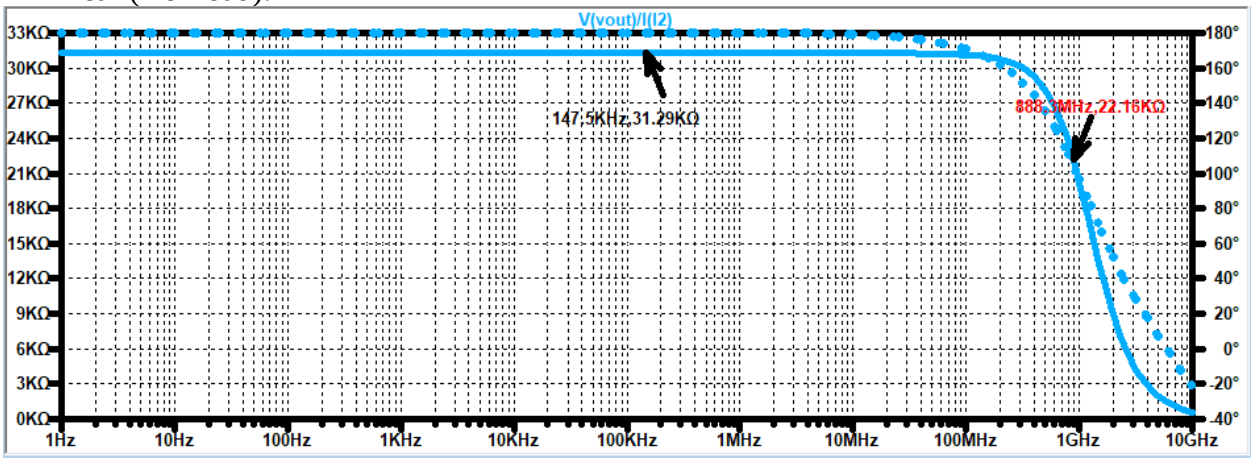
Quick Simulation of the Diff-Amp TIA:



In Decibel (No Load):

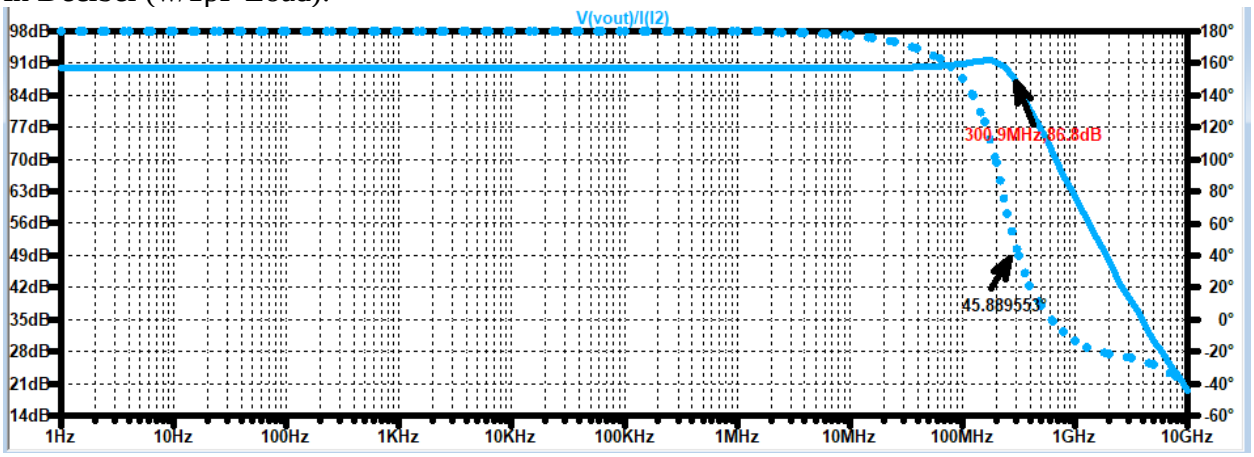


In Linear (No Load):



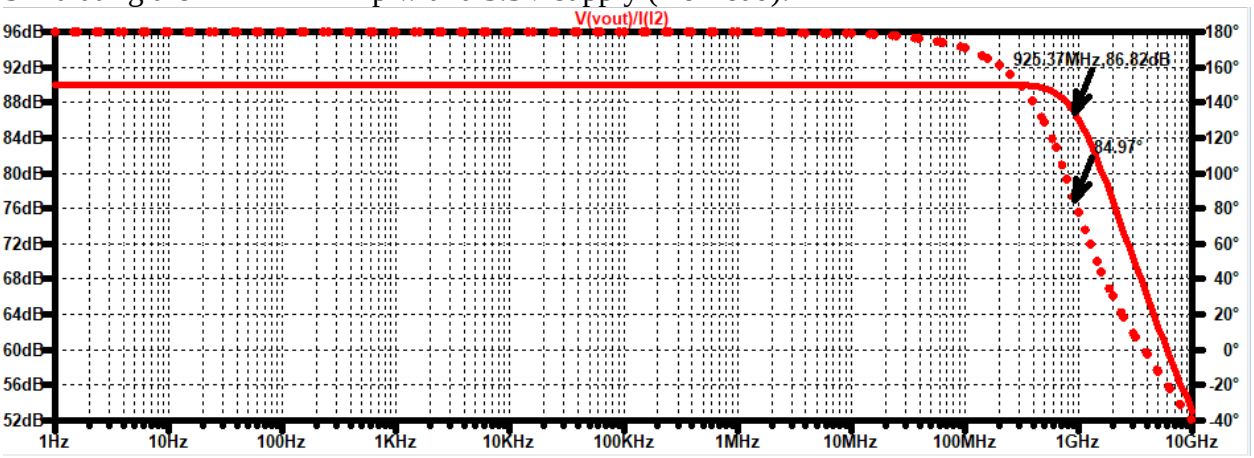
From the above, we see that the diff-amp TIA meets both the gain and bandwidth specification! However, what will indecisively dictate the TIA bandwidth is the load it needs to drive, seen in the next simulation.

In Decibel (w/1pF Load):



Looking at the above simulations, the bandwidth is choked down to 300MHz due to the 1pF capacitor load. The other thing to take into consideration is the phase of the output relative to the input signal, where the difference is well over 135°. Note that there is slight Q-peaking happening near the bandwidth cutoff, which means our TIA is approaching instability and oscillation.

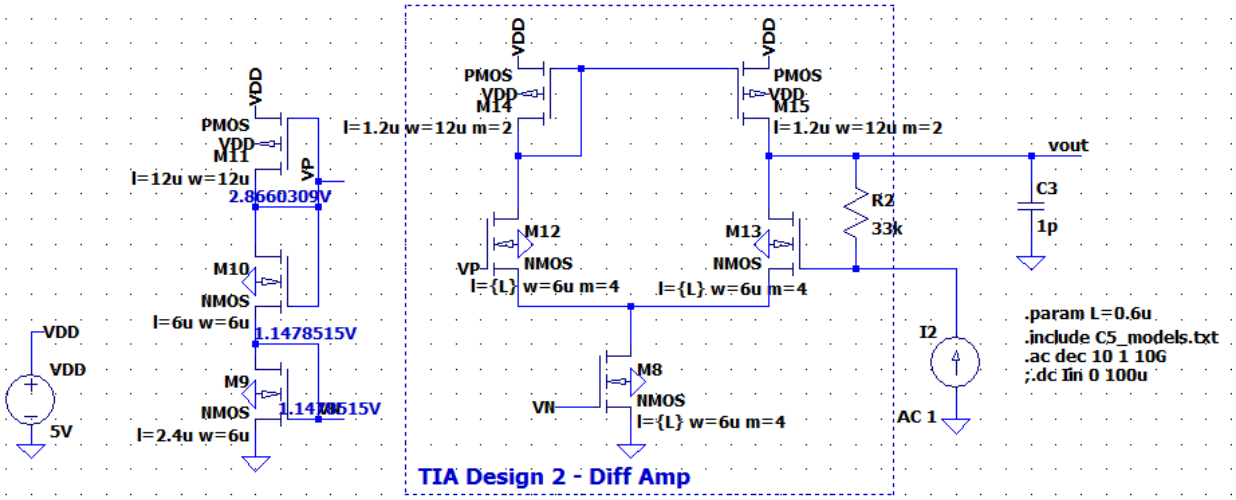
Simulating the TIA Diff-Amp with a 3.3V supply (No Load):



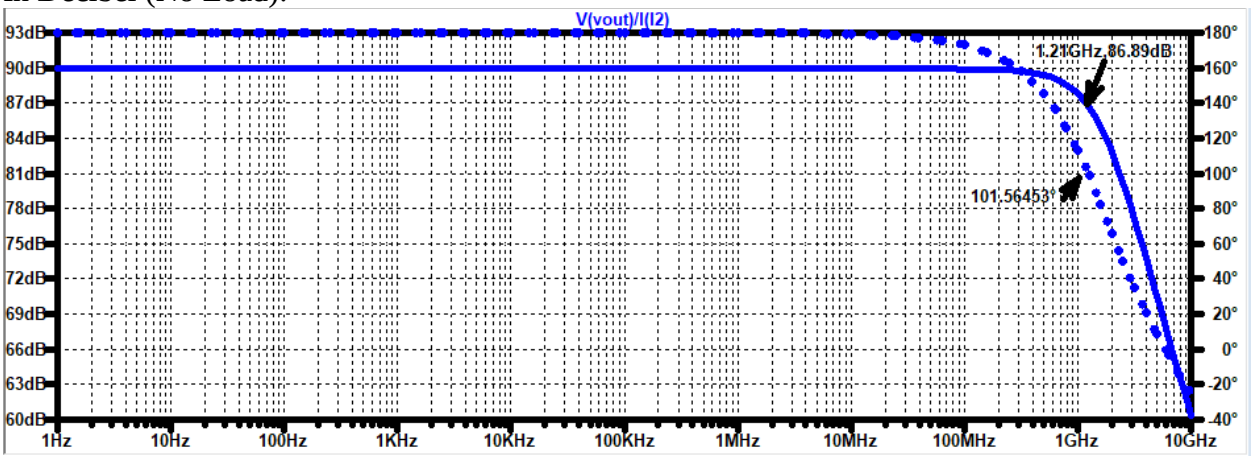
The greatest strength of the Differential-Amplifier is the ease of biasing the MOSFETs and how the amplifier is not necessarily affected to changes in VDD. If needed, the topology above can be used at lower VDDs (and therefore low power) at the consumer's convenience.

The maximum current that was simulated at 5 volts was well above 1mA. The sizes of all MOSFETs can be decreased by a common factor, and therefore lower current usage.

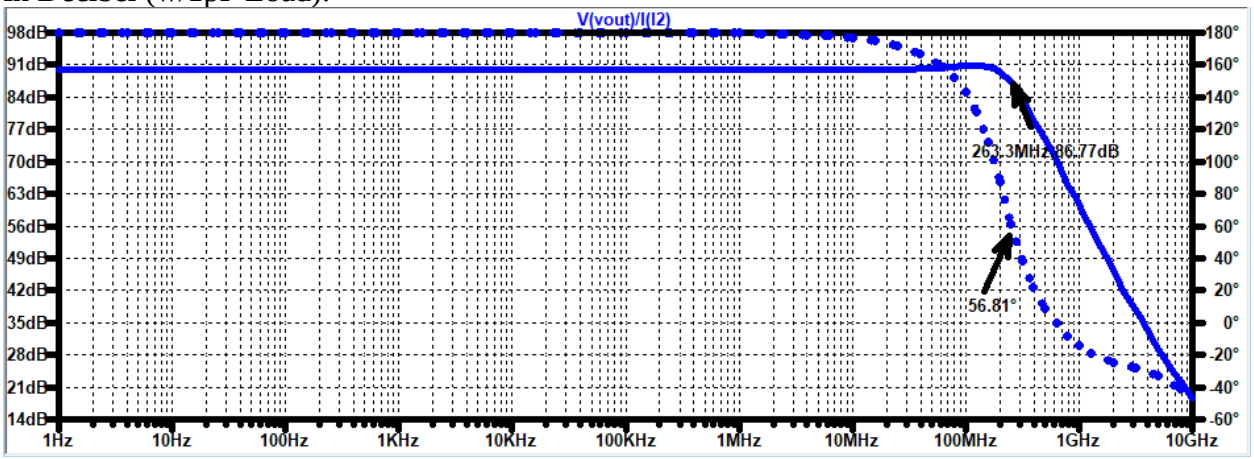
Final TIA Diff-Amp Design:



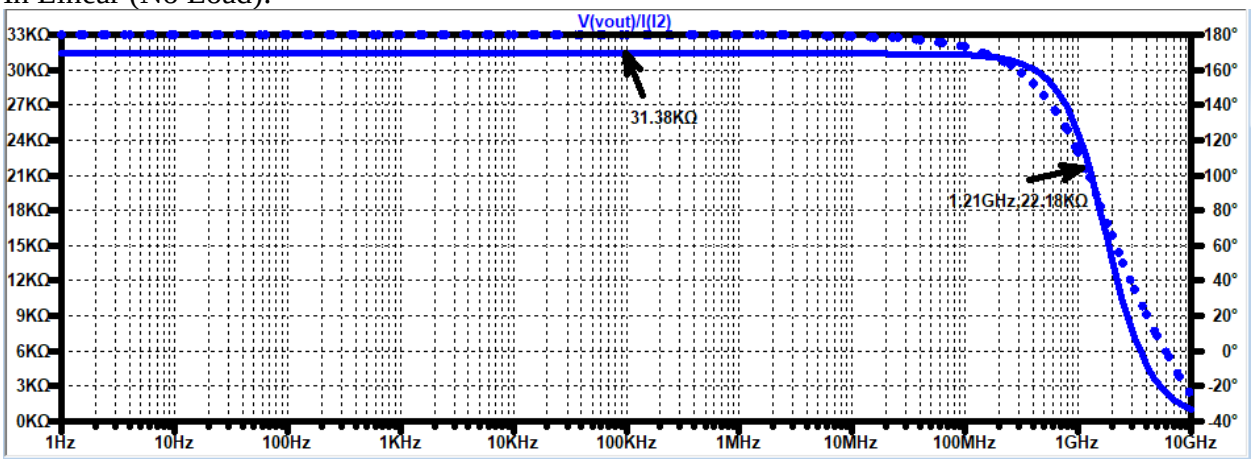
In Decibel (No Load):



In Decibel (w/1pF Load):



In Linear (No Load):



Summary of 2nd Design TIA:

VDD		3.3V	5V	5V (Smaller Size)
Gain		31.48kΩ	31.29kΩ	31.3kΩ
Bandwidth (No Load) + ϕ°		925MHz (84°)	888MHz (104°)	1.21GHz
Bandwidth (w/ 1pF Load) + ϕ°		227MHz (45°)	301MHz (45°)	263MHz
Estimated Output Resistance (using Loaded Bandwidth)		701Ω	528Ω	605Ω
Current consumed		247µA	1.31mA	542µA

Summary of TIA Diff-Amp Design:

- The differential-amplifier can be used as a shunt-shunt amplifier simply by connecting the input gate of one of the diff pairs to its corresponding drain with a feedback resistance.
- Biasing can easily be controlled using only three transistors with long length devices (for less current consumption). The output voltage can be controlled by the bias voltage located at the opposite side of the diff-amp (since the diff-amp tries to make the voltages at the gate of the diff pair the same).
- The noise generated from the PMOS current mirrors can be decreased by increasing the lengths (which decreases current usage)
- The diff-amp can withstand changes in VDD, and is able to function at both 3.3V and 5V power supplies.

Trade off Considerations:

- A lot of current can be burned through the wide transistors; however, the output is able to drive large loads and have a fairly wide bandwidth.
- A choice between extending the bandwidth can be made, however, there is a chance that Q-Peaking will occur if the diff-pair widths are made too large. Q-Peaking causes the TIA to oscillate and although the bandwidth can be extended, it is better to make the diff-pair small (and cutoff the bandwidth) and make sure the TIA is able to have a relatively good phase difference between the input and output.

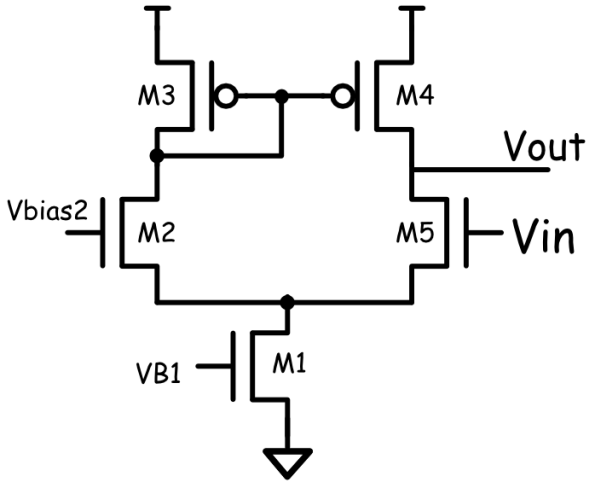
Discussion for a 2nd Stage Amplifier

From the above, the final design TIA is able to meet both the bandwidth and gain specifications, however, while carrying a load, the phase between the input and output become too large, and there will be a chance the TIA will become unstable.

It would be desirable to make the TIA work at a larger bandwidth so that the phase between the input and output of the TIA will be ideally close to 180° (inverted).

A voltage amplifier can be used so that the TIA will not need to carry a large capacitive load, and the output stage of the amplifier can utilize a larger current output to drive heavy loads.

The following topology will be used:



From the Diff-Amp TIA, a bias voltage was created for the diff-pair so that the input/output voltage can shift relative to the voltage at the other side of the gate.

Since the voltage at the output stage of the TIA is relatively near the gate bias voltage of the diff-pair, we can easily bias up the 2nd stage amplifier and also reuse a bias voltage!

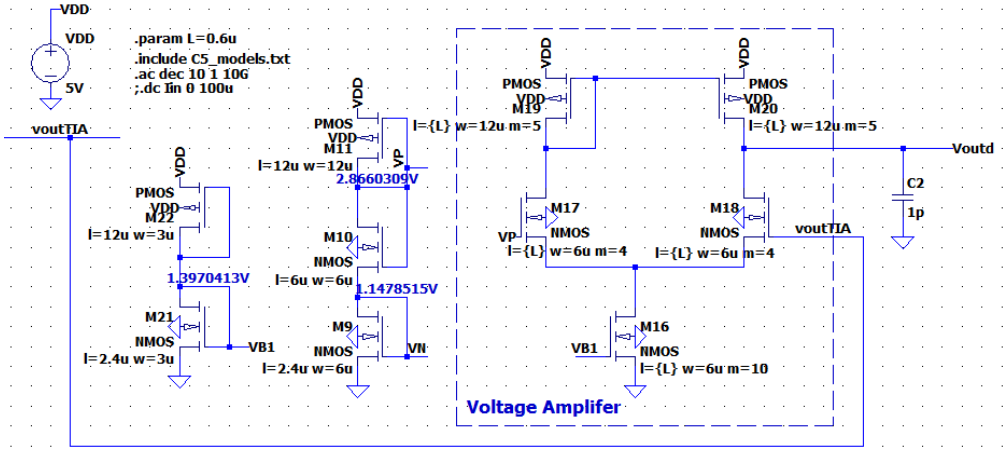
The gain for the above topology can be summarized by:

$$\left|\frac{V_{Out}}{V_{in}}\right| = g_{m,N5} \cdot (R_{M4} || R_{M5})$$

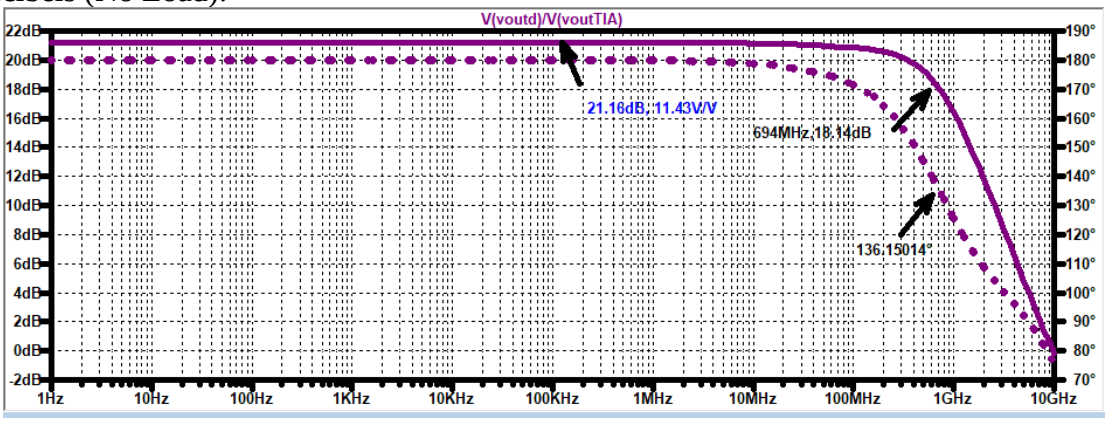
From above, the gain can be controlled simply by changing the transconductance in the diff-pair by increasing the current sink (at the cost of using more power), or by increasing the widths of the diff-pair.

We will be connecting the output of the diff-amp TIA to the input of the voltage amplifier to better mimic the DC bias voltage at the gate of the diff-pair.

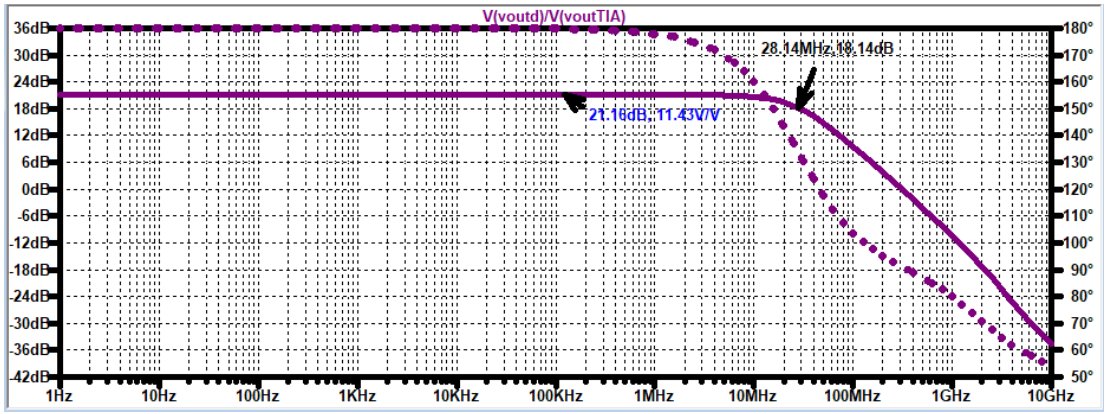
Simulation:



In Decibels (No Load):



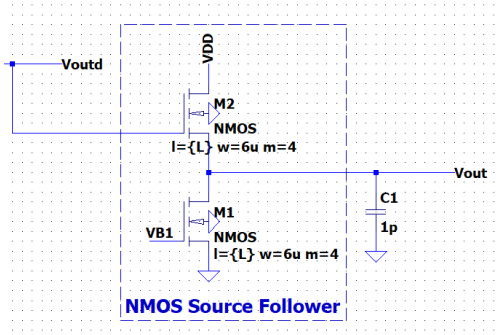
W/1pF Load:



The voltage amplifier's maximum bandwidth is around 694MHz, however, adding the 1pF load bring the bandwidth down to nearly 30MHz!
One method that can be done is increase the widths of the PMOS current mirrors and lower the output resistance, however, too much current will be wasted in this stage.

A source follower (current buffer) can be used to drive the heavy load.

Using an NMOS source follower:

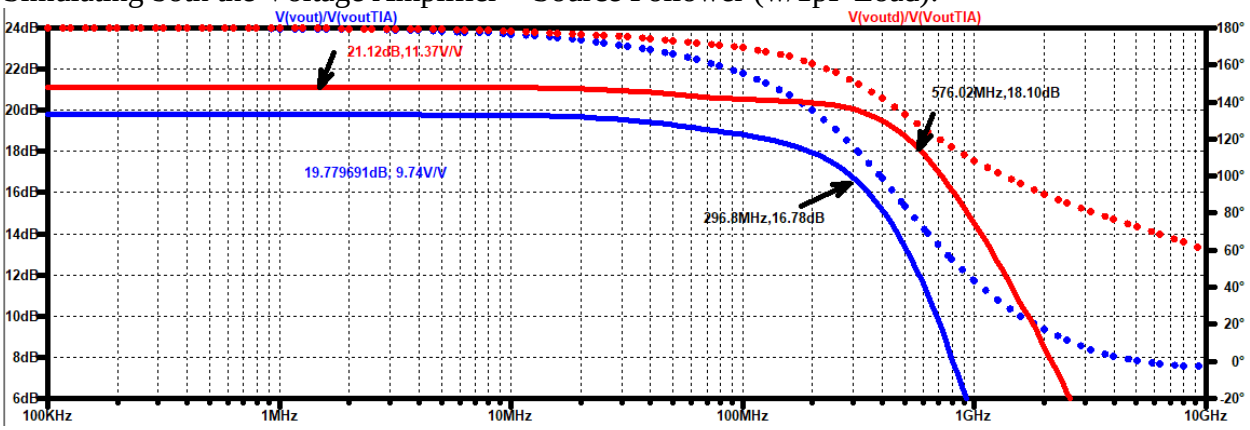


Where the gain is:

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{\frac{1}{g_{M1}}}{\frac{1}{g_{M1}} + \frac{1}{g_{M2}}}$$

The gain can be increased by making sure the gate voltage at the bottom NMOS M1 is low to reduce the transconductance parameter, and therefore keep the gain near (but still less than) one.

Simulating both the Voltage Amplifier + Source Follower (w/1pF Load):



Although the overall voltage gain decreased from 11.37V/V to 9.74V/V, the source follower is able to carry the 1pF capacitive load!

Lowering the power supply voltage to 3.3 Volts:

Final two-stage Transimpedance Amplifier: