Final Project – ECG 720

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Final Project Introduction

As a part of the course, the student was assigned a final project to apply the knowledge gained throughout the semester. The final project was to design a transimpedance amplifier (TIA) to convert current from an avalanche photo diode (APD) into an output voltage. The TIA was required to be designed using On Semiconductor's 500nm process.

TIA requirements:

Characteristic	Value/Range
First Stage Gain	30kΩ
Second Stage Gain	10-20 times V/V
TIA Minimum Bandwidth	250 MHz
Input Referred Noise	Less than 5 $pA/\sqrt{Hz}$
Output Swing	1.5 – 2 V
VDD Voltage	3.3 V or 5 V
Current Consumption	Less than 5 mA
Max Load	1pF
Slew-rate with Max Load	Greater than 100 V/µs = 100 mV/ns
Layout Process	C5 (500nm) process

Table 1) Design Requirements

Initial Design Process (Device Sizing)

The project is required to be created using the C5 process. The minimum length in the C5 process is 600nm. One of the first parameters the student had to choose was the length of the devices to be used. The student initially decided to go with a length of 2 times the minimum

(1.2µm). The student had issues with speed so ended up using the minimum length of 600nm to get more speed.

L = 600 nm

The next parameter that needed to be determined was the width size of the devices. The width influences the amount of current that is sourced/sunk by the MOSFETs. This is important because the amount of current influences a number of things. First, it affects current consumption, which is required to be below a certain limit for this project. It also affects the gain and speed. Gain and speed are inversely proportional, so reaching a mid-point to meet all requirements can be challenging. The student initially chose a NMOS width of 18µm and a PMOS width of 36µm. After going through numerous simulations, the student realized the sizing was consuming too much current. The student tried multiple widths and came up with the following final width sizes:

NMOS width of 7µm and a **PMOS width of 14µm**

First Stage Design

The first stage of the design needs to take the current from an APD and sample out a voltage. Based on this, the student knew that a shunt-shunt feedback topology was needed. The next question needed to be answered was which type of amplifier to use. The student simulated a few types to get an idea on which one to use. The one selected was the self-biased differential amplifier. The main reasons for selecting a self-biasing differential amplifier are:

1) Differential amplifiers in general tend to have high bandwidths, which is useful in meeting the 250Mhz bandwidth.
2) Only one bias voltage is needed for the self-biased differential amplifier.

The following is the LTspice schematic diagram that shows the first stage design.

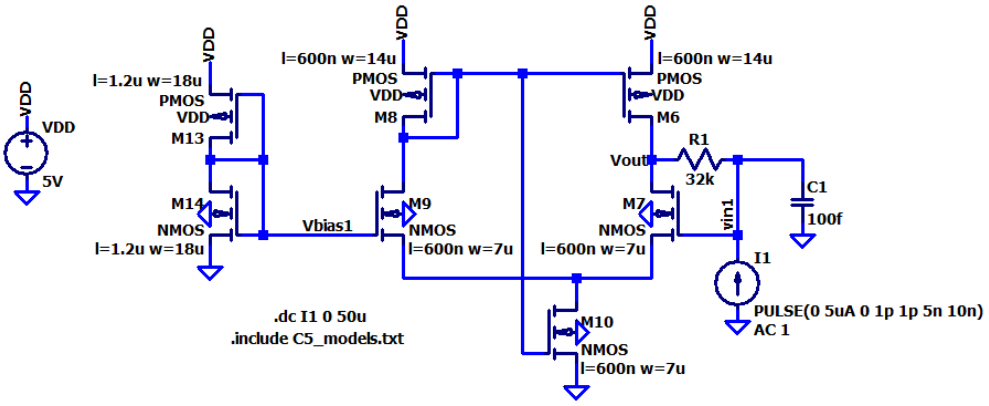

Figure 1) Schematic of the First Stage of TIA

The design seen in Figure 1 is a self-biasing differential amplifier with a shunt-shunt feedback topology. This means that the amplifier takes in current as input (current mixing) and outputs a voltage (voltage sampling). The current source pulse seen feeding into the gate of M7 simulates the current outputted by an APD. The capacitance in parallel with the current source helps more accurately simulate the APD because APDs have a parasitic capacitance (student chose 100fF for simulations).

The student ran a dc sweep simulation of the current source to get the gain of first stage. Figure 2 shows the results. As can be noted, the gain is close to 30kΩ until the current source goes above 25µA, where the gain starts to decrease more drastically.

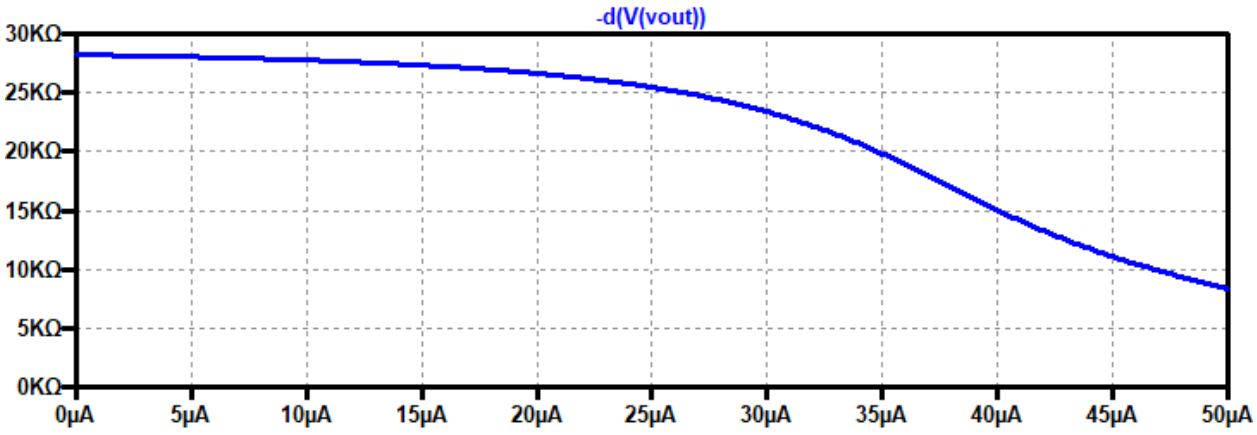

Figure 2) Gain of the First Stage of the TIA

Discussion for the Need of a Second Stage

A single stage TIA is not ideal to use for a few reasons. First, the gain of just a single stage is not enough to create a wide enough voltage swing. This becomes a big issue when trying to measure/record the output of the single stage TIA. Second, the single stage is not able to drive the load of 1pF, specified in the project description, well enough. When the load is connected, it kills the bandwidth and along with it the gain. The student created an LTSpice schematic (Figure 3) and simulations that confirm the previous statements.

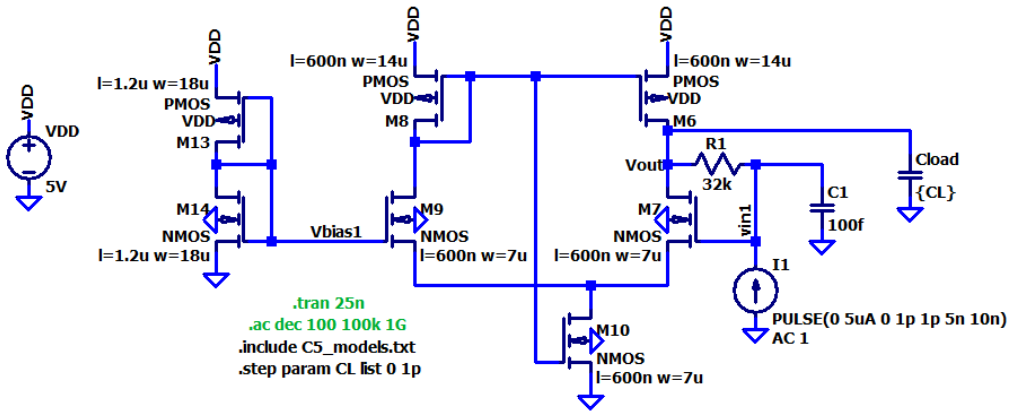

Figure 3) Single Stage TIA with and without Load

Figure 4 shows the result of the transient simulation of the single stage TIA with a step parameter that changes the value of the load capacitor from 0F to 1pF. The green trace is when there is no load and the blue trace is when there is a load. Notice that the pulse becomes distorted into a sine wave, which is undesirable. In addition, the voltage swing is only about 150mV which is very far off from the minimum required voltage swing of 1.5V.

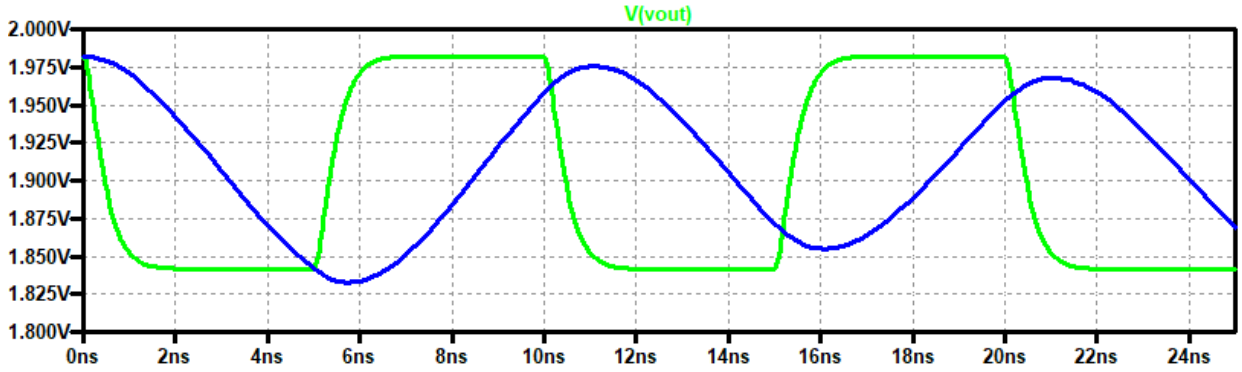

Figure 4) Voltage Swing of Single Stage TIA with and without Load

Figure 5 shows the result of the ac analysis of the single stage TIA with a step parameter that changes the value of the load capacitor from 0F to 1pF. Again, the green trace is when there is no load and the blue trace is when there is a load. It is easy see that the bandwidth is reduced by about 4.6 times, from 434Mhz to 94Mhz, which does not meet the requirement.

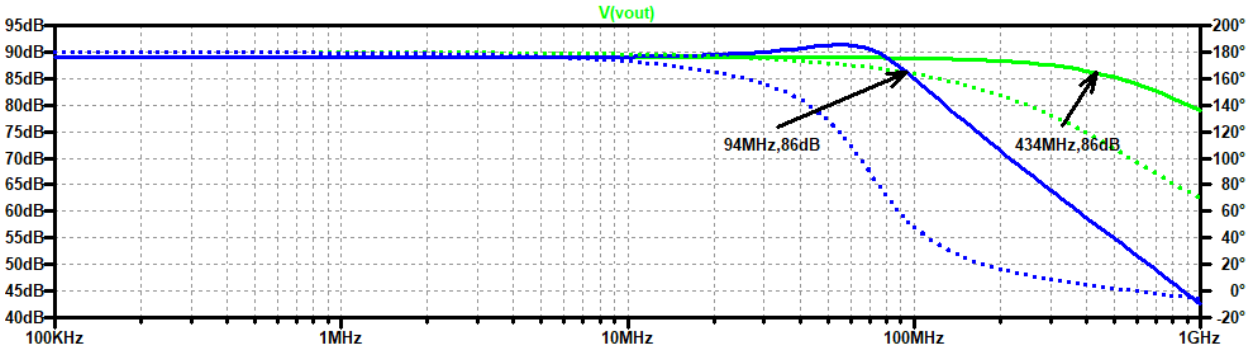

Figure 5) Bandwidth and Gain of Single Stage TIA with and without Load

Based on these observations, it can be said with confidence that there is a need for the inclusion of a second stage to the TIA.

Second Stage Design

The second stage of the design is required to have an output that is ten to twenty times larger than the input to it. The main purpose of the second stage is to increase the gain of the signal, which also increases the output voltage swing. There are several considerations that must be made when choosing an appropriate second stage amplifier topology including bandwidth, gain, current consumption, and others. After simulating a few different types of topologies, the student concluded to also use a self-biasing differential amplifier for the second stage. The reasons for choosing it are:

1) The good bandwidth from the first stage would be preserved relatively well.
2) The gain of the differential amplifier would be enough to get the desired 10-20x gain.
3) The student could use the same bias voltage circuit from the first stage in the second stage.

The following is the LTspice schematic diagram that shows the second stage design.

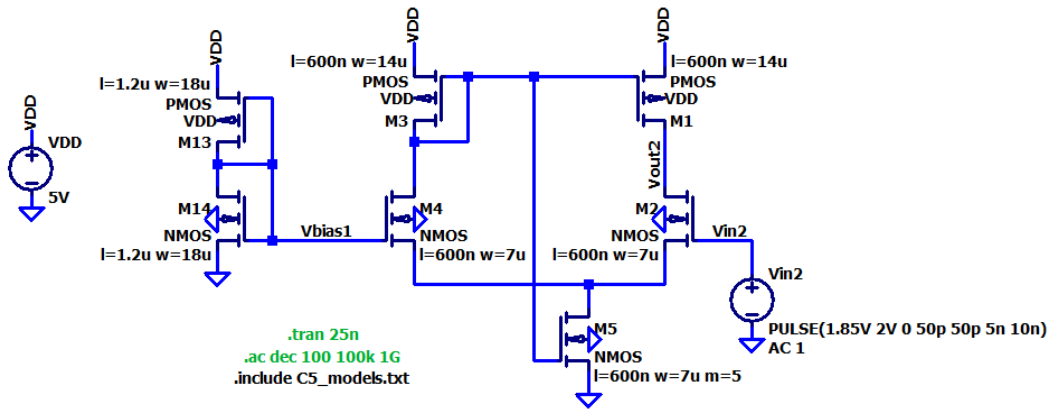

Figure 6) Schematic of Second Stage of TIA

The design seen in Figure 6 is a self-biasing differential amplifier used to amplify the voltage output from the first stage of the TIA. The student looked at the output signal from the first stage seen in Figure 4 to create an appropriate input for the second stage and test it. A transient simulation was ran to show what the voltage swing of the output looks like. As can be noted in Figure 7, the voltage swing of the output is 1.62V. This is great because it meets the voltage swing requirement.

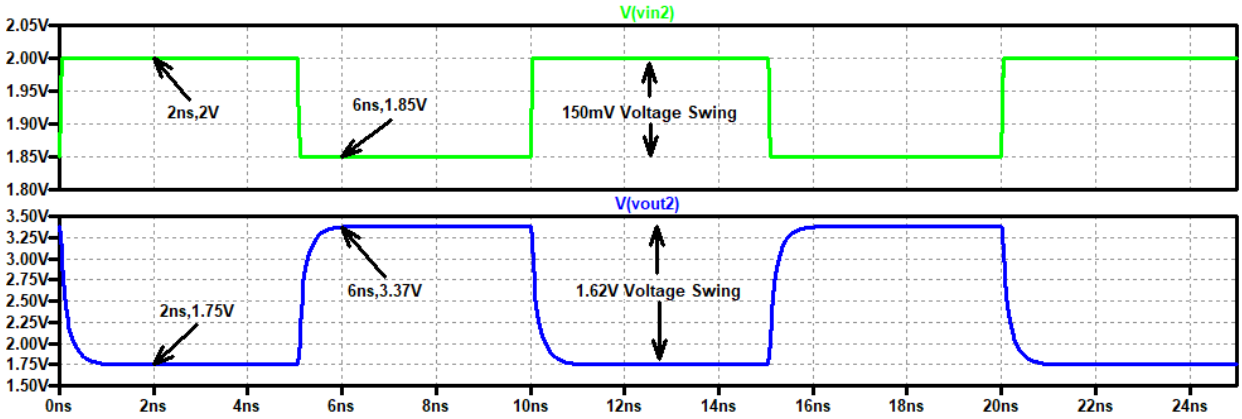

Figure 7) Voltage Swing of Output of Second Stage

Next, the student ran a ac analysis to demonstrate what the bandwidth and gain look like. Figure 8 shoes the simulation results of the AC analysis. The gain of the second stage is 19.1dB and the bandwidth is 1.23GHz, which is way past the 250MHz requirement. This design looks promising based in these initial results.

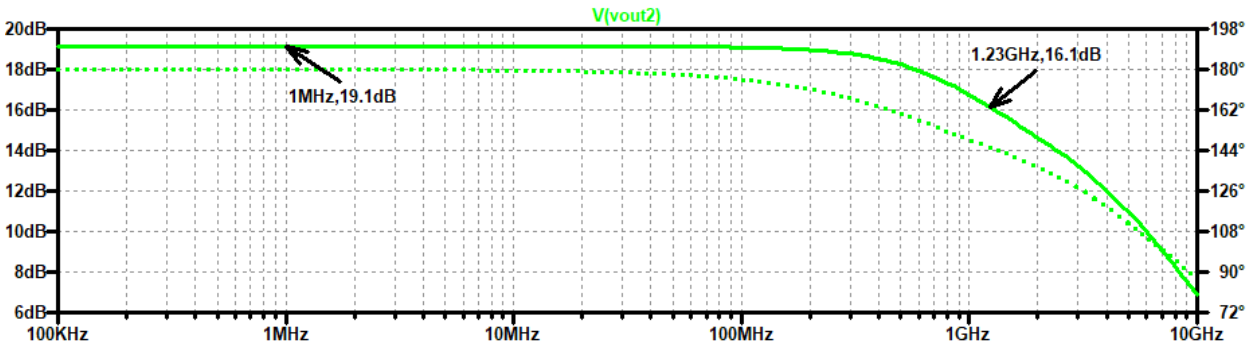

Figure 8) Bandwidth and Gain of Second Stage

The next thing the student needed to check is how the bandwidth and gain hold up having the max load of 1pF connected. Figure 9 shows the ac analysis simulation of the second stage with the load connected to the output. Unfortunately, the self-biased differential amplifier alone does not have the capability to drive the 1pF load while meeting the bandwidth requirement (goes down to 12.2MHz when 250MHz is required).

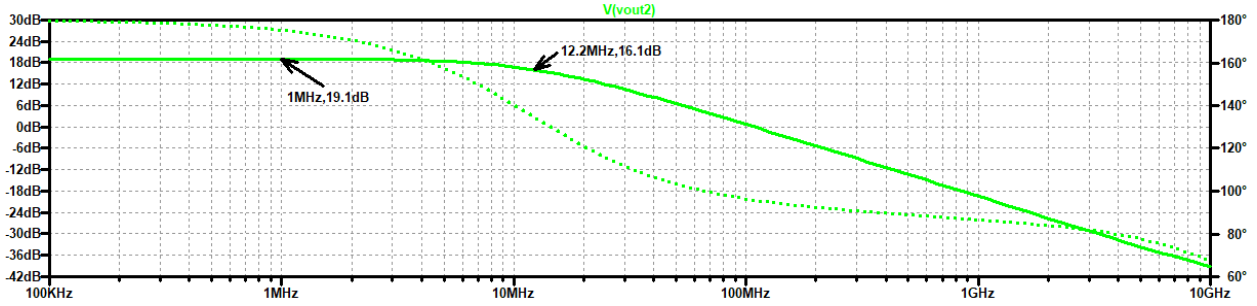

Figure 9) Bandwidth and Gain of Second Stage with Load

The student decided to add an additional part to the second stage to improve the drivability. After going through a few simulations, the student found that a common source amplifier would help solve the problem because they can typically drive larger loads. Figure 10 shows the schematic of the second stage with the addition of the common source amplifier. The bottom NMOS was biased using the same bias voltage the differential amplifier uses. This is useful because no additional bias circuit is needed.

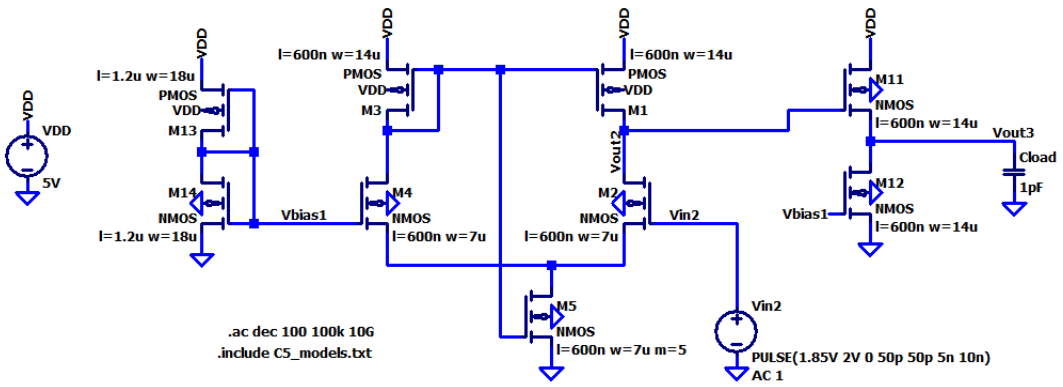

Figure 10) Second Stage of TIA with addition of Common Source

To demonstrate that the common source amplifier was able to drive the load while meeting bandwidth, the student ran an ac analysis. Figure 11 shows the simulation results of the ac analysis. As can be seen, the bandwidth of the improved second stage is now 282MHz while driving the load.

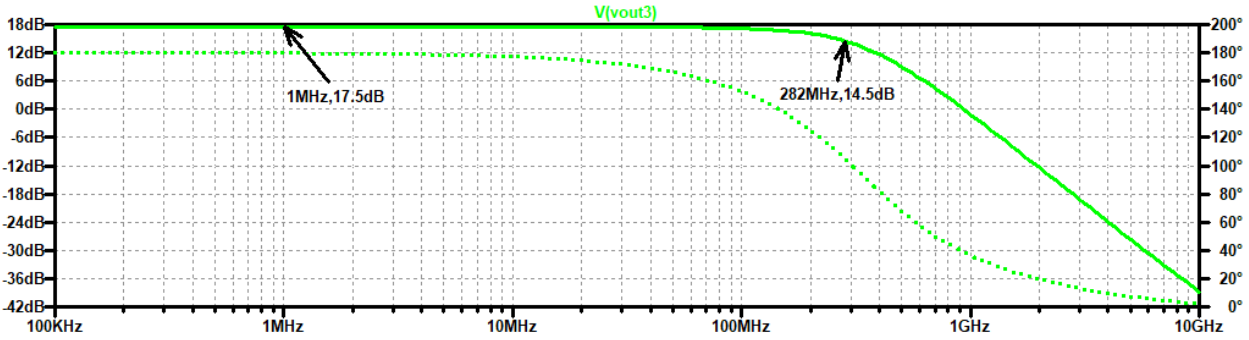

Figure 11) Gain and Bandwidth of Final Second Stage Design with Load

From this point, the next thing that was done was to connect everything together and check if all the requirements are met.

Complete TIA Design

The following figure is the complete schematic of TIA which includes the bias voltage circuit, first stage, second stage part one, and second stage part two.

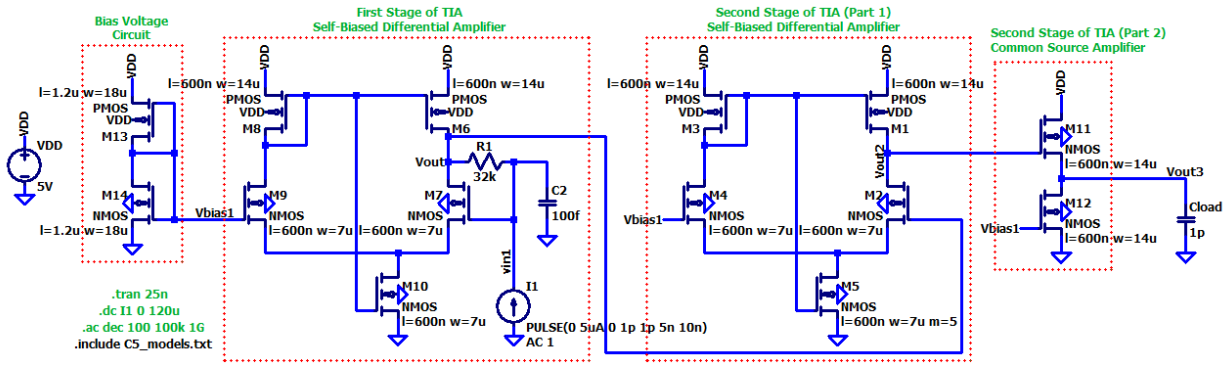

Figure 12) Complete TIA Schematic Diagram

Bandwidth

The minimum bandwidth requirement of the TIA is 250 MHz. There are several factors that the student took into consideration to reach this requirement. First, the student selected the minimum length devices for the fastest speeds. Second, the student chose the differential amplifier topology for the first and second stage because they have wide bandwidths. Figure 13 shows the ac analysis that demonstrates that the complete TIA meets the requirement. As shown in the figure, the 3dB frequency is 254 MHz confirming the requirement was met.

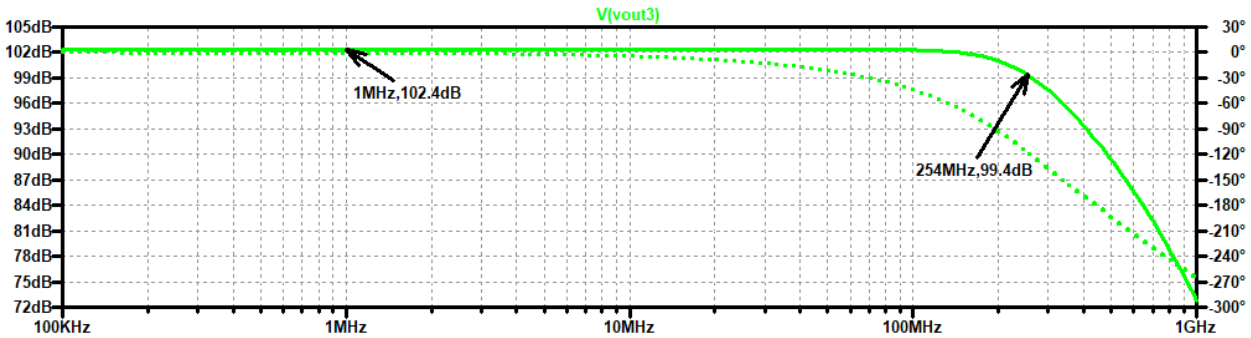

Figure 13) Bandwidth of Complete TIA

Output Swing

The output voltage swing performance of the complete TIA was required to be from 1.5V to 2V. In the beginning of the design process, the student reduced the sizes of the devices to design for speed. In the process of the chase for speed, the final output voltage swing was overlooked. The output voltage swing of the 1st part of the second stage meets the voltage swing requirement as seen in Figure 7. Unfortunately, when the 2nd part of the second stage was

added (the common source amplifier) to improve load performance, the output voltage swing suffered. Figure 14 shows the final output voltage swing. The final voltage swing is 1.05V, indicating the student did not meet the requirement by 0.45V. The drawback of adding a common source amplifier was that the gain is less than the desired Av = 1. The student decided to keep the common source regardless, because without it, the TIA would not be able to drive the required load. This was a challenging decision to make, but the student believes that load drivability has priority over voltage swing.

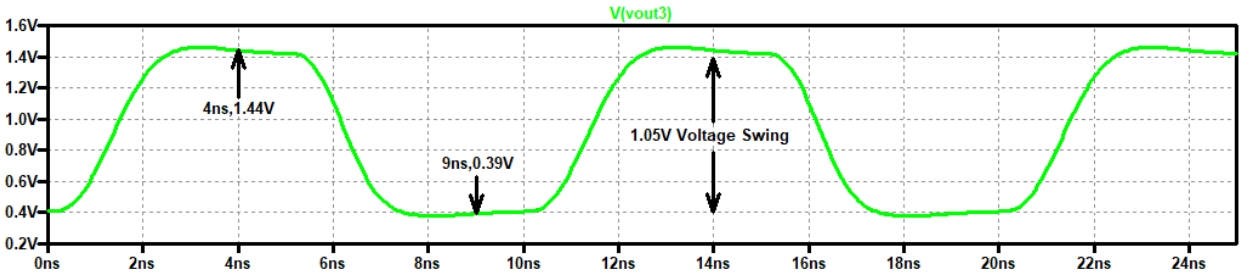

Figure 14) Voltage Swing of Final Output

Current Consumption

The power supply voltage that was chosen from the two options was 5V. Regardless of which voltage value was selected, the TIA had to consume less than 5mV as a requirement. To demonstrate the current consumption of the complete TIA, the student ran a transient simulation. Figure 15 shows that the current drawn from the power source is being monitored. The green trace shows the current consumption with no load, while the blue trace shows the current consumption with the 1pF load. The complete TIA design meets the current consumption requirement given that the maximum current draw is 4.5mA.

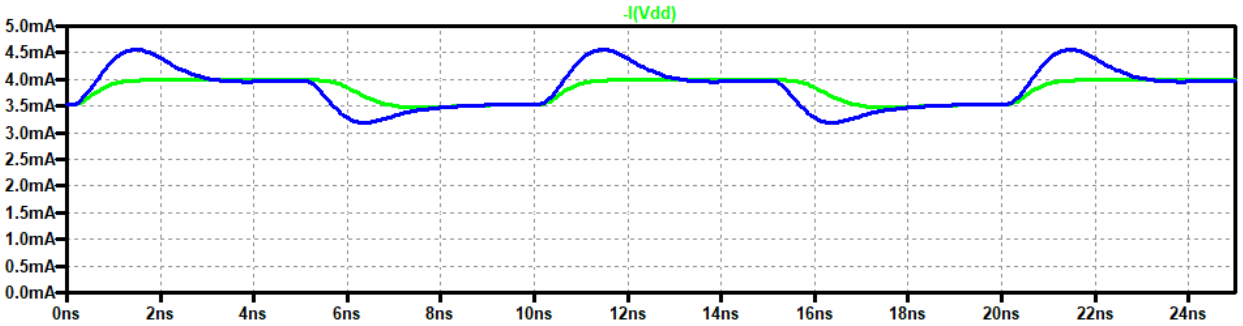

Figure 15) Current Consumption of TIA

Slew-rate with Maximum Load

The slew-rate under maximum load is required to be greater than 100 V/µ = 100 mV/ns. The slew rate can also be demonstrated using a transient simulation. As seen in figure 16, the slope is highlighted in blue. This is the change in volts per second, but the student represented the value in terms of Volts/microseconds as seen below.

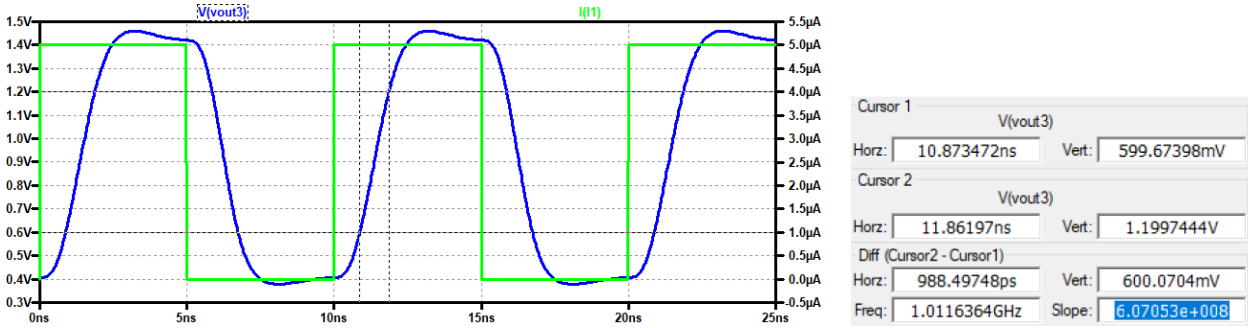

Figure 16) Slew-rate of Complete TIA

As seen by the calculation below, the student has a 6 times greater slew rate than required indicating a fast TIA.

$$slew\ rate = 607M\frac{V}{s} = 607M\frac{V}{s} * \left(\frac{10^{-6}}{\mu}\right) = 607\frac{V}{\mu s}$$

Settling Time and Slewing with Max Load and No Load

The following simulation demonstrates the settling time with max load connected to the final output. As can be see in Figure 17, the settling time for both the rising and falling edge are 2.8ns. Another simulation was ran , and as can be noted in figure 18, the settling time decreased when there was no load (blue trace is with load, green trace is no load).

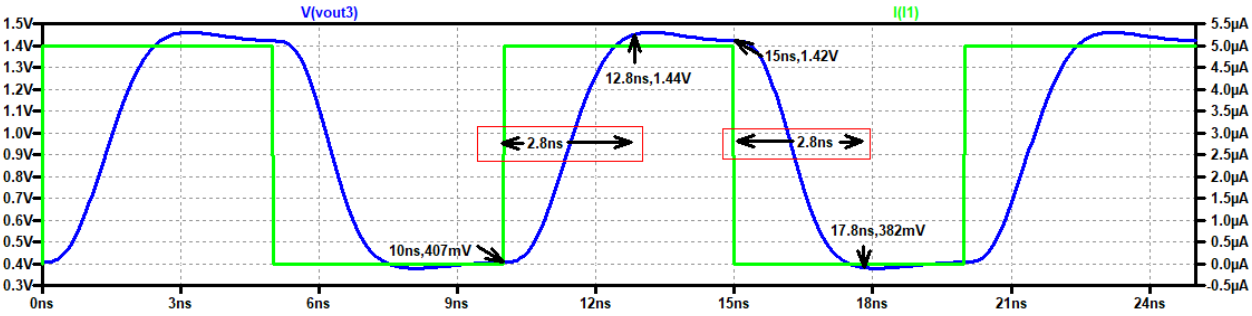

Figure 17) Settling Time with Max Load

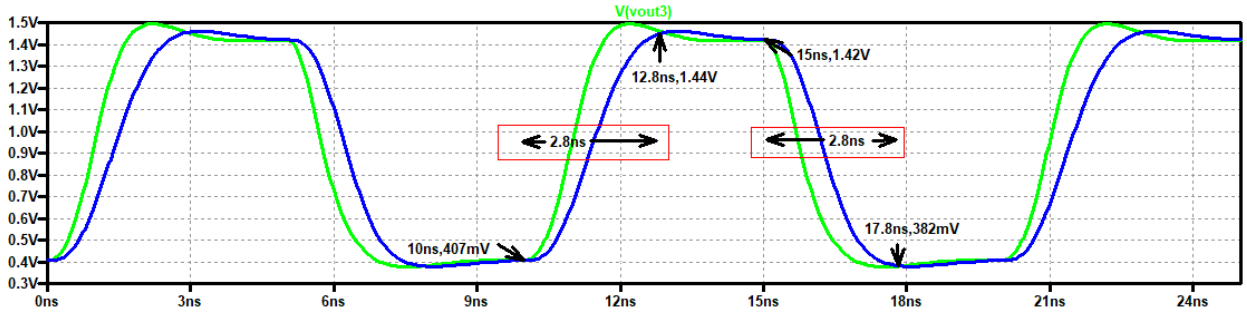

Figure 18) Settling Time Load/No-Load Comparison

Noise Performance

The student had to meet an input refereed noise of less than 5 $pA/\sqrt{Hz}$. The student was also required to show the significance of capacitance on the input of the front-end. The student ran a noise simulation with varying capacitance to demonstrate how it affects the input referred noise. As seen in Figure 19, when the capacitance is relatively large (200fF) the noise increases to a max of 3.5 $pA/\sqrt{Hz}$. Even with a capacitance of 200fF, the noise stays well within range to meet the noise requirement.

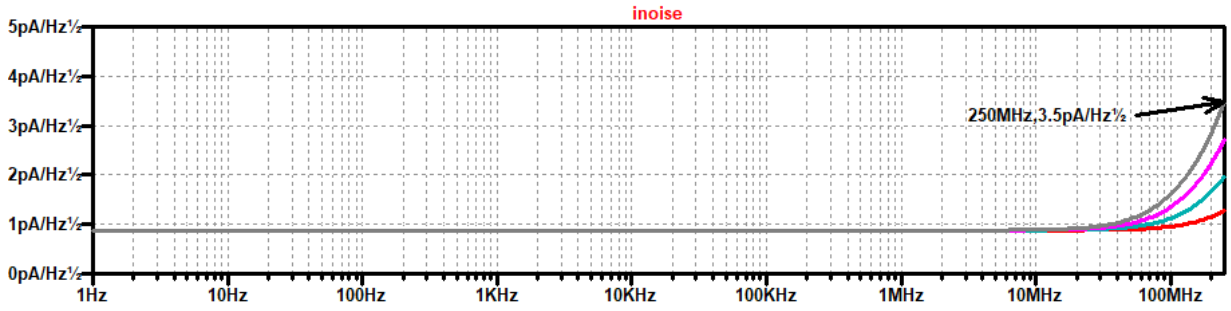

Figure 19) Noise Performance of TIA

Result Summarization

Complete TIA Specifications:

Characteristic	Value
First Stage Gain	30kΩ
Second Stage Gain	10-20 times V/V
TIA Bandwidth	254 MHz
Input Referred Noise (Max)	3.5 $pA/\sqrt{Hz}$
Output Swing	1.05 V
VDD Voltage	5 V
Current Consumption (Max)	4.5 mA
Max Load	1pF
Slew-rate with Max Load	607 V/µs = 607 mV/ns
Layout Process	C5 (500nm) process

Table 2) TIA Specifications

Concluding Thoughts

The student met all the final project requirements, except for one. The requirement that was not met was the output voltage swing. In the pursuit of high speed and large bandwidth, the voltage swing fell below the requirement. Other than that, the rest of the TIA work well within requirements. If more time were allowable, the student would focus on adjusting parameters to find a middle ground between a good voltage swing and good bandwidth.