Quantum Transistors

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EE 453 - 1001

Background of Quantum transistors

To understand the quantum field-effect transistor (QFET) we must first look at when the first field-effect transistor (FET) was made. The FET is a type of transistor which uses an electric field to control the flow of current. FETs are devices with three terminals: source, gate, and drain. FETs control the flow of current by the application of a voltage to the gate. The concept for the FET was first patented by physicist Julius Edgar Lilienfeld in 1925 and by Oskar Heil in 1934, but they were unable to build a working practical semiconducting device based on the concept. Figure 1 below shows pictures of them when they were coming up with the patent.

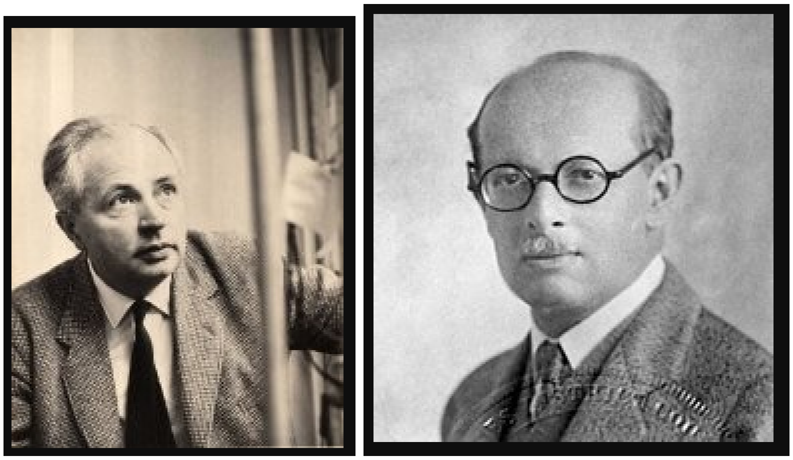

Figure 1 - Picture portraits of Oskar Heil (left) and Julius Edgar Lilienfeld (right)

Later on, the transistor effect was explained by John Bardeen and Walter Houser Brattain while working under William Shockley at Bell Labs in 1947. Shockley initially attempted to build a working FET, by trying to modulate the conductivity of a semiconductor, but was unsuccessful.When trying to find an explanation on why they couldn't build a FET, their research made Bardeen and Brattain instead build a point-contact transistor in 1947, which was followed by Shockley's bipolar junction transistor in 1948. There were multiple FET devices made using different processes and able to function differently on their properties, hence their different names. The first FET device to be successfully built was the junction field-effect transistor (JFET), which was first patented by Heinrich Welker in 1945. There was also the static induction transistor (SIT), which was invented by Japanese engineers Jun-ichi Nishizawa and Y. Watanabe in 1950. In the early 1950s ,the insulated-gate field-effect transistor (IGFET) was theorized as a potential alternative to junction transistors, but researchers were unable to build working IGFETs, so by the mid-1950s, researchers had largely given up on the FET concept, and instead focused on bipolar junction transistor (BJT) technology. In 1948, Bardeen, with the theory he made, patented the progenitor of MOSFET, an insulated-gate FET (IGFET) with an inversion layer. The inversion layer confines the flow of minority carriers, increases modulation and conductivity. Bardeen's patent as well as the concept of inversion layer forms the basis of complementary metal oxide semiconductor (CMOS) technology today. In 1955, Ian Munro Ross filed a patent for a FeFET or MFSFET. Its structure was like that of a modern inversion channel MOSFET, but ferroelectric material was used as a dielectric/insulator instead of oxide. In February 1957, John Wallmark filed a patent for what he described as a double gate FET. Now we can move on to the QFET where the idea for it came up in 2002 when Ken Scott Fisher and Kevin Cotton Baxter filed a patent for a quantum tunneling transistor. Now a QFET or quantum-well field-effect transistor (QWFET) is a type of MOSFET (metal–oxide–semiconductor field-effect transistor) that takes advantage of quantum tunneling to greatly increase the speed of transistor operation by eliminating the traditional transistor's area of electron, a schematic diagram of a quantum dot transistor, a type of QFET, can be seen in Figure 2.

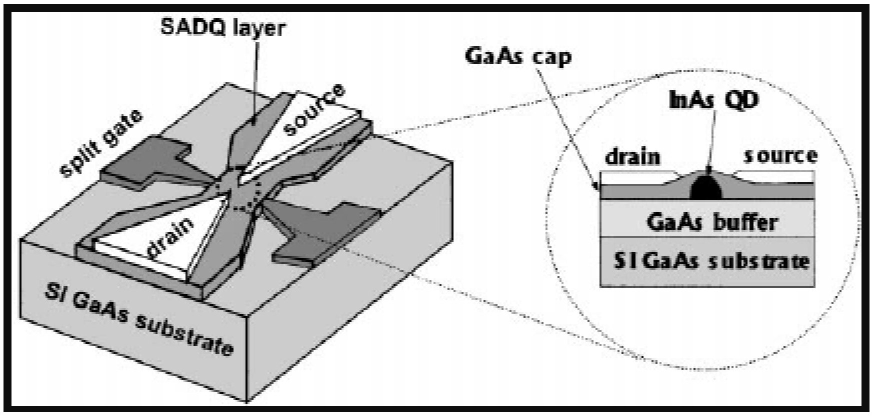

Figure 2 - schematic diagram of a quantum dot transistor

The result is an increase in logic speed with a simultaneous reduction in component power requirement and size. It achieves these things through a manufacturing process known as rapid thermal processing (RTP) that uses ultrafine layers of construction materials. Modern examples of quantum field-effect transistors integrate structures traditional to conventional MOSFETs and utilize many of the same materials. QFET, similar to MOSFETs, have source and drain terminals connected to doped regions insulated by the body region. These are either p or n type regions, with both terminals being of the same type and opposite to that of the body type. FET structures are typically constructed gradually, layer by layer, using a variety of techniques such as molecular-beam epitaxy, liquid-phase epitaxy, and vapor-phase epitaxy, an example being chemical vapor deposition. Typical MOSFETs are constructed on the micron scale. In order to construct QFETs ,ultrathin semiconductor layers are used in the production of QFETs, whose band gaps are smaller than those of the surrounding materials. In the case of a one-dimensional quantum well QFET, a nanoscale semiconductor layer is grown between two insulating layers. The semiconductor layer has some amount of thickness, and the electron charge carriers are trapped in a potential well. The charge carriers can be activated (or deactivated) by applying a potential to the gate terminal that matches a corresponding energy level. These energy levels depend on the thickness of the semiconductor layer and the material properties. A promising semiconductor candidate for QFET implementation, InGaAs, has a de Broglie wavelength of around 50 nanometers. Larger gaps between energy levels can be achieved by lowering the thickness of the layer. In the case of InGaAs, layer lengths of around 20 nanometers have been achieved. In practice, three dimensional quantum wells are produced, with the dimensions of the plane of the layer being much larger in relative size. QFETs orchestrated with quantum wires similarly confine electron charge carriers in a potential well, yet the nature of their narrow geometric shape enables a manufacturer to trap the electrons in two dimensions. Quantum wires are able to provide a tighter carrier confinement and a predictable current flow, in Figure 3 we can see several photos of quantum wires made of different materials.

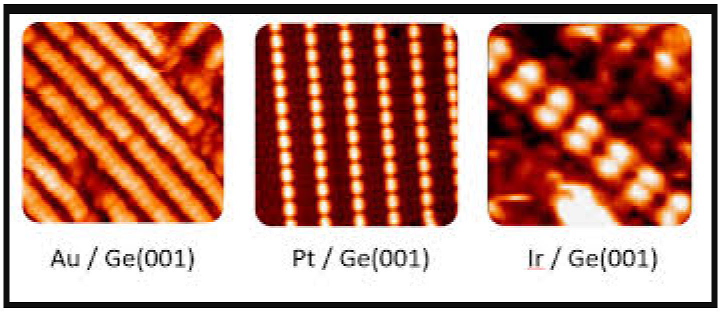
Au / Ge(001)
Pt / Ge(001)
Ir / Ge(001)

Figure 3 - Quantum wires made of Au/Ge (001), Pt/Ge (001), Ir/Ge (001)

All semiconductors have a unique conduction and valence band structure. In direct band gap semiconductors, the conduction band minimum and valence band maximum energies occur at the same wavenumber, corresponding to the same momentum. QFETs with quantum-well structures have conduction bands that are split into numerous subbands, which correspond to their appropriate quantum numbers and offer a higher density of states at their lowest allowed conduction-band and highest allowed valence-band energy levels than MOSFETs. This gives QFETs interesting properties, particularly in their optical characteristics and applications. QFETs are often used for quantum-well devices such as laser diodes, where the photons interact with electrons and holes via transitions between the valence and conduction bands. Transitions from photon interactions in quantum-well semiconductors are governed by the energy gaps between subbands.

Current Progress

There are many types of quantum devices under development. One type is the double electron layer tunneling transistor (DELTT) built by researchers at Sandia National Laboratories, in Albuquerque, N.M. Also another type of quantum device used to boost the performance of conventional transistors is resonant tunnel diodes, which are similar to DELTT. Another sort of quantum device that shows great promise for nonvolatile memory is the single electron transistor or the quantum dot transistor. A single-electron memory cell of silicon, operating at room temperature, should prove to have faster read and write times than conventional nonvolatile memories. A photo of the DELTT can be seen in Figure 4 below.

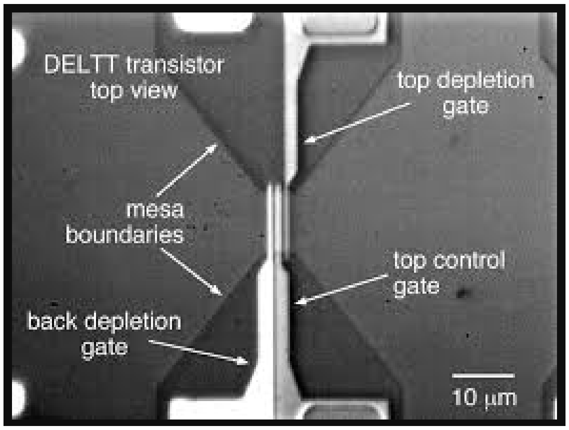

Figure 4 - Photo of the top view of DELTT transistor

Now let us delve deeper into DELTTs with the mechanism being used to develop them which is tunneling. Tunneling means that a particle plunges through a barrier that would be impenetrable in the classical world. DELTTs are also set to volume manufacturing, because they are built with a planar process which uses conventional semiconductor deposition. As deposition can be controlled to within a few tenths of a nanometer, it is more than adequate for all DELTT operations. For the structure of the DELTT, it positions an insulating barrier between two two-dimensional wells. The DELTT operates when electrons quantum mechanically tunnel from one well to the other through the barrier. The device speed benefits from the tunneling process, which is much faster than the drift of electrons across a channel. The well is formed by surrounding one region holding a large number of free electron energy states with another region having a little to none of them. The well is deemed two-dimensional when it is so narrow in one dimension that electron motion is restricted to the plane of the well, these dimensions of the well and the height of the barrier determine the discrete energy states allowed to the electrons in the well. An electron can tunnel through the barrier only if its energy and its momentum in the plane of the well are both conserved. So, an electron can tunnel only if the energy state of the quantum well on the other side of the barrier is equal in energy and momentum to the state the electron originally occupied. In most cases when no voltage is applied to the device, there are no matching states in the two wells, and the device is off. But when the energy level of the electrons in one well is shifted, the energy states line up opposite each other and tunneling occurs, which is also known as resonance. Applying voltage to a control gate or biasing one of the wells relative to the other will shift the energies and both have voltages applied when operating the DELTT. The DELTT's operation is like the switching of a transistor, where at a certain source to drain bias voltage, the device can be switched on or off by applying a voltage to the gate, but there is one important difference. Raising the gate or drain voltage on a conventional transistor will increase the current, but in a DELTT, raising the voltage beyond the point of resonance shuts off the current. Another way to look at it is the differential resistance, which is the change in voltage with respect to a change in current, can become negative. This allows complementary circuits to be built with only one type of transistor, rather than the n-type and p-type transistors required for CMOS circuits.

Figure 5 - Staff at Sandia Laboratories testing the temperature of the DELTT

It's a unipolar device, which means the only carriers are electrons, but the transconductance can take either sign, depending on the control gate voltage, it is possible to make complementary circuits that are multifunctional, which means that it is possible to make the same circuit functions with fewer devices. For example, the Sandia researchers built a static RAM cell using two DELTTs in series.A conventional CMOS static RAM cell requires n-type and p-type transistors. However, there are multiple drawbacks to the DELTT, one is the milli-volt levels at which it operates not only are hard to integrate ,but also mean susceptibility to noise. Also, the speed is limited by the DELTT's RC time constant. It is easy to shrink the resistance by using a very thin barrier, but then the two wells are so close that the capacitance is large. To help deal with this, the development team behind the DELTT added a third well to the device. In the new configuration, electrons tunnel from the first to the second well, then continue through a second tunnel barrier to the third, very wide well. The large voltage drops across the wide third well allows the electrons to pick up speed. The team has also demonstrated the structure working at voltages on the order of a volt, compatible with existing electronics. Also, the source-drain capacitance is much smaller because the starting and ending layers of electrons are very far apart compared to the two wells. They also managed to raise the operating temperature. While early devices required temperatures below 4.2 K, the boiling point of liquid helium, more recent DELTTs operate at very low temperatures. A photo of some staff testing the temperature can be seen above in Figure 5.

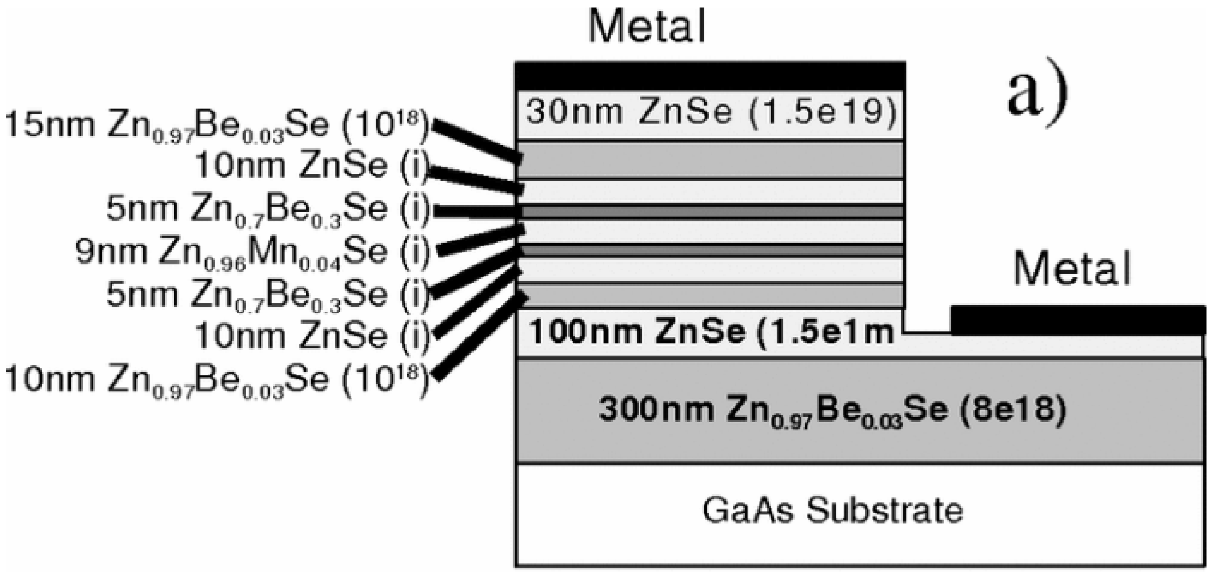

Figure 6 - Structure of a resonant tunneling diode (RTD)

The goal, though, is room temperature operation. Now to delve into the resonant tunneling diodes (RTDs), which routinely operate at room temperature. Although they are not exactly transistors because they do not have a third terminal, RTDs still have a role by being combined with ordinary transistors to improve performance of conventional circuits. The structure of an RTD can be seen in Figure 6 above. In RTDs, electrons tunnel through two barriers separated by a well as they pass from an input source to output drain. Since, the RTD well is narrow, then energy levels allowed to electrons are quantized and widely spaced. Usually, only one quantized state in the well has any bearing on device operation. When a voltage is applied between the source and drain, current starts to flow and reaches a maximum at resonance, when the applied voltage raises the energy of the electrons in the source to line up with the well's quantized state and once this point is passed the current drops. Similar to the Deltts, the RTDs display a negative differential resistance. This means that they can put them back to back and latch. That makes it possible to make a static RAM cell with two back-to-back RTDs and one transistor. Which makes it a lot smaller and reduces power consumption within the device.

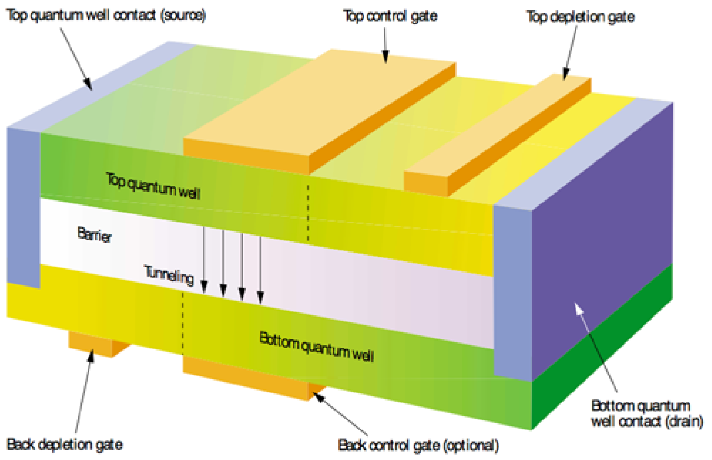

Figure 7 - Diagram of a quantum dot transistor

Now we'll talk about the single electron transistor and the basic building block of the single electron transistor is a small island of conducting material, sometimes called a quantum dot. When the island is small enough, the energy needed to land an electron on it or take one from it depends on how large it is and how many electrons are already on it. For room temperature operation, an island as small as 1 to 3 nm is needed and a simple way to get electrons on and off the island is to add an electron source separated from the island by a thin oxide through which electrons can tunnel.

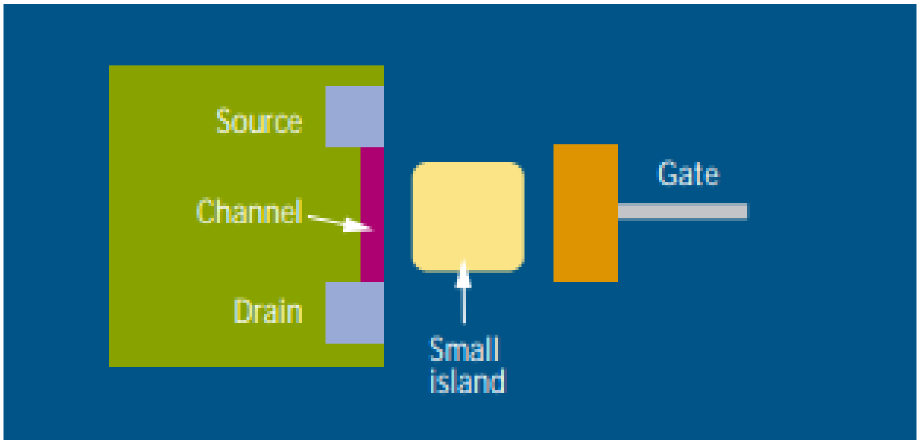

Figure 8 - Formation of a nonvolatile memory cell using a quantum transistor

A gate over the island changes its energy state, determining the conditions under which electrons tunnel where the result is a structure called a single-electron box. Applying a gate voltage polarizes the island, then as the voltage is increased from zero, an electron in the source lacks enough energy to charge the island. This Coulomb blockade is the basis of all single-electron transistors, but the greater the voltage, the greater the polarization charge becomes, until it equals one electronic charge, where the energy conditions favor the tunneling of one electron to the island from the source electrode. A possibility is to replace the channel of an FET by an island and separate it from the source and drain by tunneling barriers. As the source to drain voltage is raised, no current flows until a threshold voltage is reached. Usually, the devices work below the threshold voltage. In this region, the gate voltage controls the source to drain current. The gate applies a potential to the island and the polarity of the potential makes it advantageous for electrons to enter the island as it changes the Coulomb blockade threshold. As the gate voltage is increased, the blockade threshold voltage drops, and the source-drain current grows until the blockade threshold voltage equals zero. But when the gate voltage is increased beyond this point, the blockade voltage rises again and the current drops. Which means that the single-electron transistor oscillates between regions of positive and negative transconductance. The advantage is only one type of device is needed to make a complementary logic gate. Bias one transistor so that its transconductance is positive and the other so that it is negative. There are some disadvantages to this system, because of the small transconductance it takes a long time to charge up long interconnects making background charge also a problem. The sensitive transistor is also affected by single charged impurity, which occurs often in the making of dielectric materials. The island can also be used between the gate and the channel of a field-effect transistor, divided from each by an insulator. The channel becomes the island's electron source, and the transistor gate acts as the gate electrode for the island. The combination of the charge stored on the island with the source to drain and gate voltages determines the current through the channel. These devices are like electrically erasable programmable ROM cells or flash cells which can be used for nonvolatile memory. The formation of this cell can be seen in Figure 8 above.

Future applications

There are several types of research going on currently for using quantum transistors for ultra fast signals and/or saving power. One research is using Indium antimonide (InSb) which holds promise for ultra-fast, very low power digital logic applications as it has the highest electron mobility and saturation velocity of any known semiconductor. The possible performance potential was demonstrated before in a 200 nm gate length depletion mode InSb quantum well transistor (QWFET) and subsequently a 100 nm LG depletion mode device.

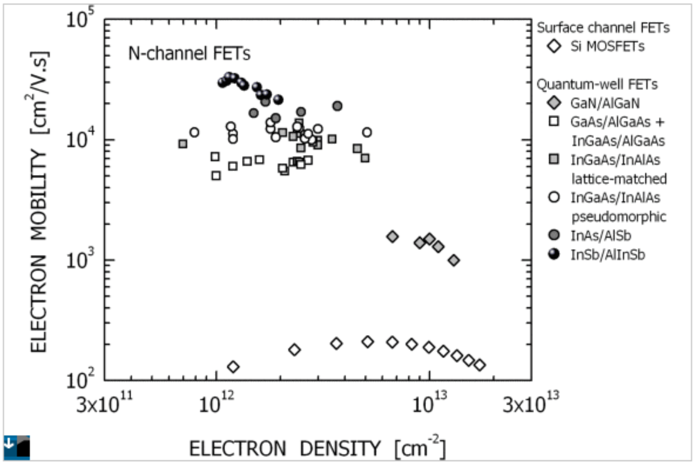

Figure 9 - Electron mobility and density graph for channel materials of FETs

The quantum well transistor architecture employs barrier layers with higher bandgap materials to mitigate the effect of the narrow bandgap InSb on device leakage and breakdown. For high speed direct coupled FET logic applications. The FETs showed in the demonstration that high performance depletion and enhancement mode InSb QWFETs makes the technology a promising candidate for future high speed, low power logic applications. Another type of future application is using QFETs as a type of FET that operates purely on the flow of spin current in the absence of charge current. A spin field effect transistor or SFET is constructed without magnetic material, but with the help of a spin flip mechanism provided by a rotating external magnetic field. The SFET generates a constant instantaneous spin current that is sensitively controllable by a gate voltage as well as by the frequency and strength of the rotating field. There also has been much interest and progress made in the study of non silicon electronic materials, such as semiconductor nanowires and III-V materials, for future high-speed and low-power computation applications on QFET devices. These materials have significantly higher intrinsic mobility than silicon, and they can potentially be used to replace silicon as the channel of the transistor for very high speed applications, which can be seen in Figure 9. Semiconductor nanowires are formed using bottom up chemical synthesis, and they currently suffer from no practical and reliable way to precisely align and position them. On the other hand, III-V materials can be patterned into desirable device structures using conventional top down lithography and etch techniques. In this regard, III-Vs are considered far more practical than nanowires for future high-speed device applications. In fact, III-V materials have been used in communication and optoelectronic products for quite some time. The resulting III-V quantum-well field-effect transistors (QWFETs) are showing some very attractive and tangible merits over scaled silicon MOSFETs. However, there still remain challenges to overcome before these devices can replace silicon MOSFETs for future high-speed, low-power CMOS logic applications. But if we can solve these problems, III-V materials can play a major role in future high-speed and low-power computational devices.

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