

# High Speed Op-amp Design: Compensation and Topologies for Two and Three Stage Designs

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## **Abstract :**

As CMOS technology continues to evolve, the supply voltages are decreasing while at the same time the transistor threshold voltages are remaining relatively constant. Making matters worse, the inherent gain available from the nano-CMOS transistors is dropping. Traditional techniques for achieving high gain by vertically stacking (i.e. cascoding) transistors becomes less useful in sub-100nm processes. Horizontal cascading (multi-stage) must be used in order to realize op-amps in low supply voltage processes. This seminar discusses new design techniques for the realization of multi-stage op-amps. Both single- and fully-differential op-amps are presented where low power, small VDD, and high speed are important. The proposed, and experimentally verified, op-amps exhibit significant improvements in speed over the traditional op-amp designs while at the same time having smaller layout area.

# Outline

- Introduction
- Two-stage Op-amp Compensation
- Multi-stage Op-amp Design
- Multi-stage Fully-Differential Op-amps
- Conclusion

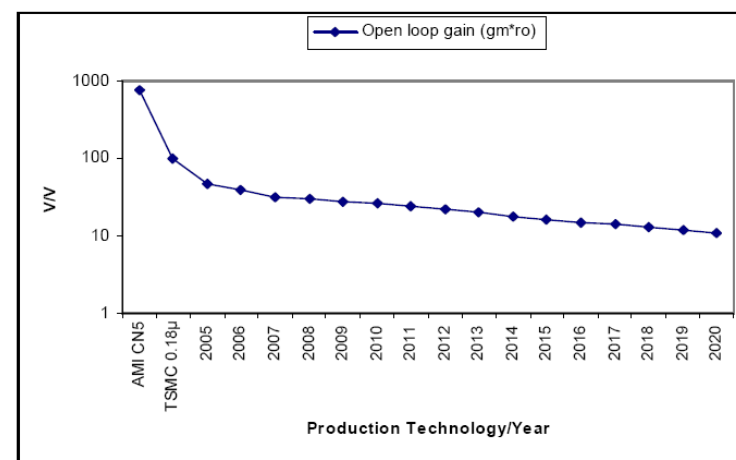
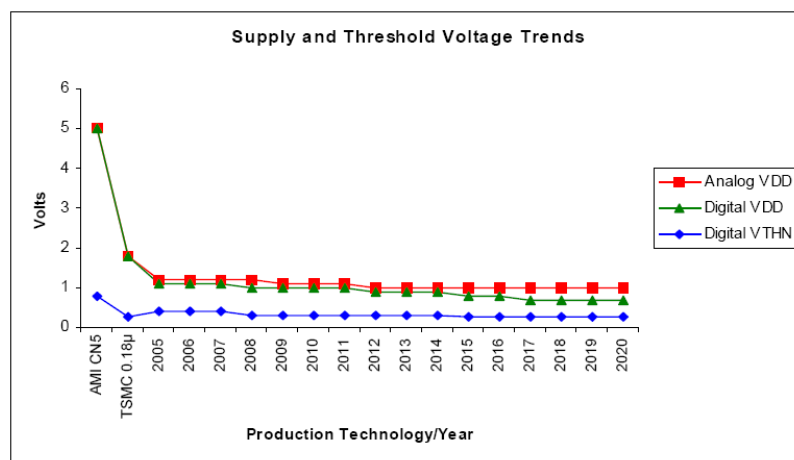
## Op-amps and CMOS Scaling

- ❑ The Operational Amplifier (op-amp) is a fundamental building block in Mixed Signal design.
  - ✓ Employed profusely in data converters, filters, sensors, drivers etc.
- ❑ Continued scaling in CMOS technology has been challenging the established paradigms for op-amp design.
- ❑ With downscaling in channel length (L)
  - ✓ Transition frequency increases (more speed).
  - ✓ Open-loop gain reduces (lower gains).
  - ✓ Supply voltage is scaled down (lower headroom) [1].

$$f_T \propto \frac{V_{ov}}{L}$$

$$g_m r_o \propto \frac{L}{V_{ov}}$$

# CMOS Scaling Trends



- ❑ VDD is scaling down but  $V_{THN}$  is almost constant.
  - ✓ Design headroom is shrinking faster.
- ❑ Transistor open-loop gain is dropping (~10's in nano-CMOS)
  - ✓ Results in lower op-amp open-loop gain. But we need gain!
- ❑ Random offsets due to device mismatches.  $\sigma_{\Delta V_{TH}} \propto \frac{1}{L \cdot W}$

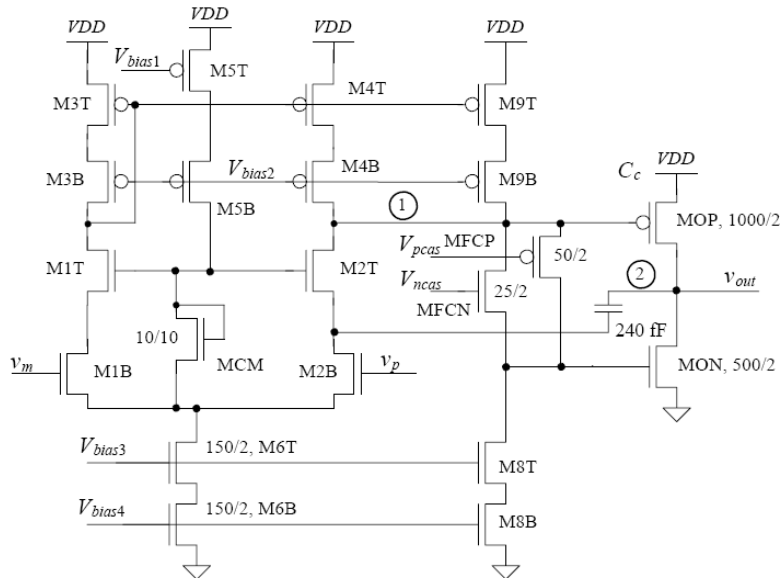
[3], [4].

## Integration of Analog into Nano-CMOS?

- Design low-VDD op-amps.
  - ✓ Replace vertical stacking (cas coding) by horizontal cascading of gain stages (see the next slide).
- Explore more effective op-amp compensation techniques.
- Offset tolerant designs.
- Also minimize power and layout area to keep up with the digital trend.
- Better power supply noise rejection (PSRR).

# Cascoding vs Cascading in Op-amps

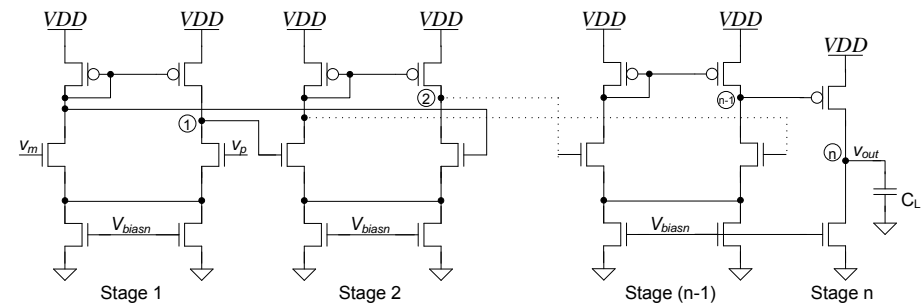
## A Telescopic Two-stage Op-amp



$$VDD_{\min} > 4V_{ovn} + V_{ovp} + V_{THP} \text{ with wide-swing biasing. [1]}$$

## A Cascade of low-VDD Amplifier Blocks.

(Compensation not shown here)



$$VDD_{\min} = 2V_{ovn} + V_{ovp} + V_{THP}.$$

- Even if we employ wide-swing biasing for low-voltage designs, three- or higher stage op-amps will be indispensable in realizing large open-loop DC gain.

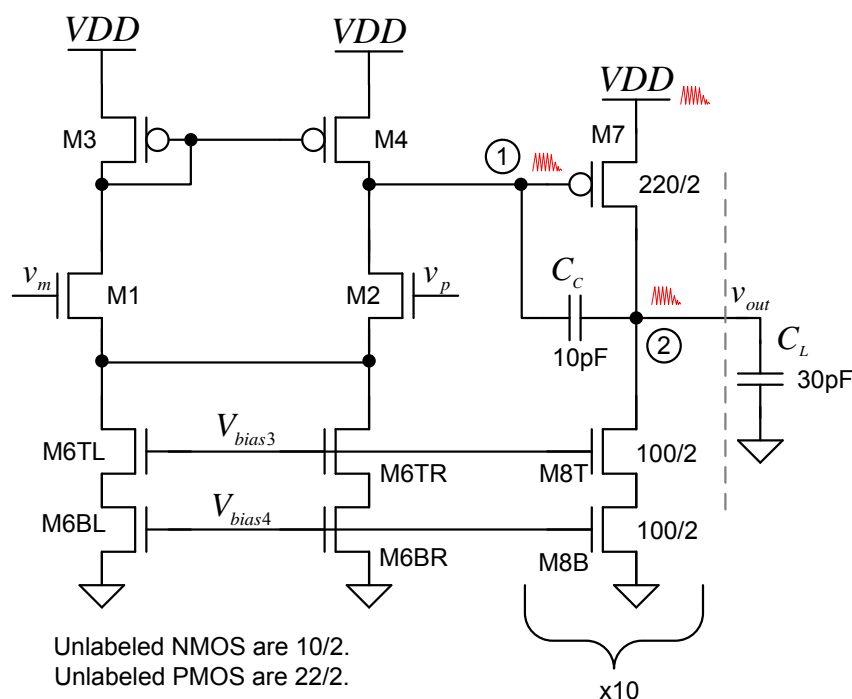


# TWO-STAGE OP-AMP COMPENSATION



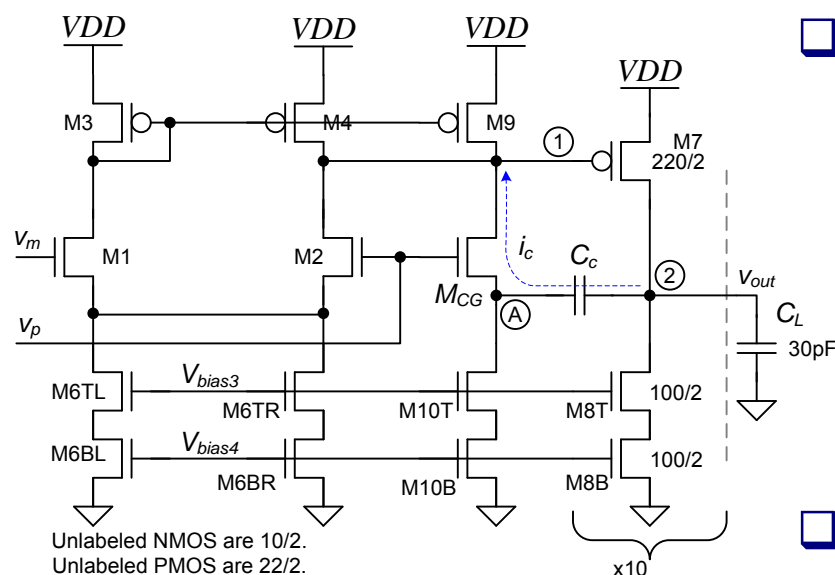


# Drawbacks of Direct (Miller) Compensation



- ❑ The RHP zero decreases phase margin
  - ✓ Requires large  $C_C$  for compensation (10pF here for a 30pF load!).
- ❑ Slow-speed for a given load,  $C_L$ .
- ❑ Poor PSRR
  - ✓ Supply noise feeds to the output through  $C_C$ .
- ❑ Large layout size.

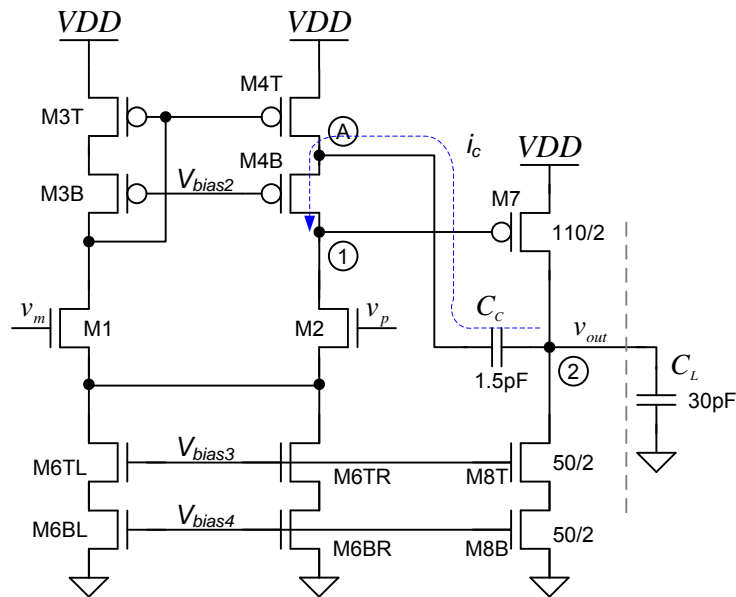
# Indirect Compensation



An indirect-compensated op-amp  
 using a common-gate stage.

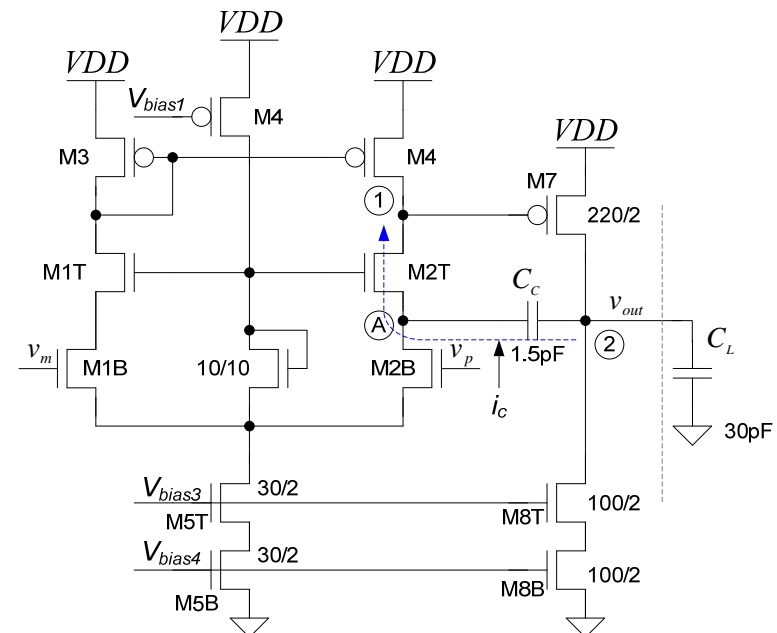
- ❑ The RHP zero can be eliminated by blocking the feed-forward compensation current component by using
  - ✓ A common gate stage,
  - ✓ A voltage buffer,
  - ✓ Common gate “embedded” in the cascode diff-amp, or
  - ✓ A current mirror buffer.
- ❑ Now, the compensation current is fed-back from the output to node-1 indirectly through a low- $Z$  node-A.
- ❑ Since node-1 is not loaded by  $C_C$ , this results in higher unity-gain frequency ( $f_{un}$ ).

# Indirect Compensation in a Cascoded Op-amp



Unlabeled NMOS are 10/2.  
Unlabeled PMOS are 44/2.

Indirect-compensation using cascoded current mirror load.

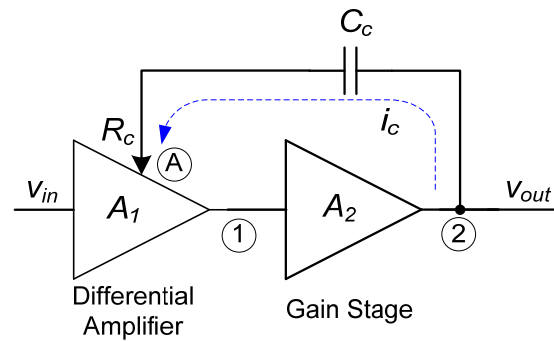


Unlabeled NMOS are 10/2.  
Unlabeled PMOS are 22/2.

Indirect-compensation using cascoded diff-pair.

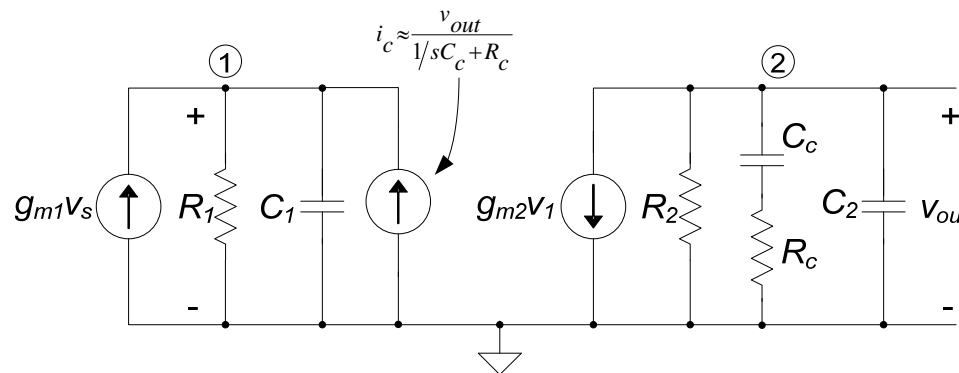
- Employing the common gate device “embedded” in the cascode structure for indirect compensation avoids a separate buffer stage.
  - ✓ Lower power consumption.
  - ✓ Also voltage buffer reduces the swing which is avoided here.

# Analytical Modeling of Indirect Compensation



The compensation current ( $i_c$ ) is indirectly fed-back to node-1.

Block Diagram

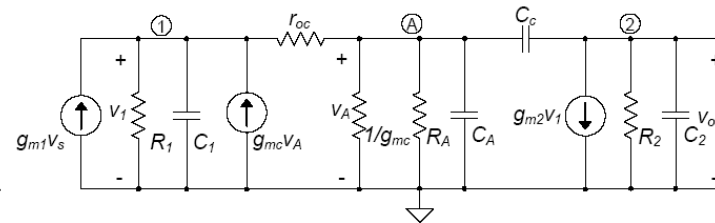


$R_C$  is the resistance attached to node-A.

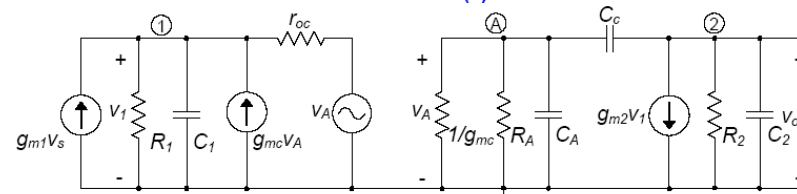
Small signal analytical model

# Derivation of the Small-Signal Model

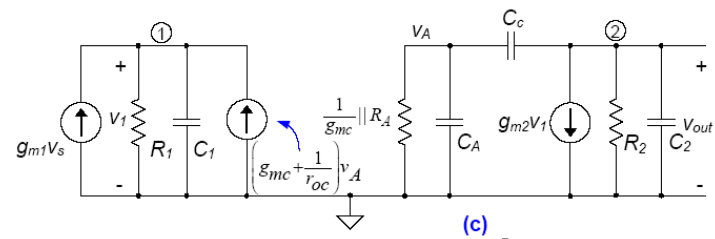
Resistance  $r_{oc}$  is assumed to be large.



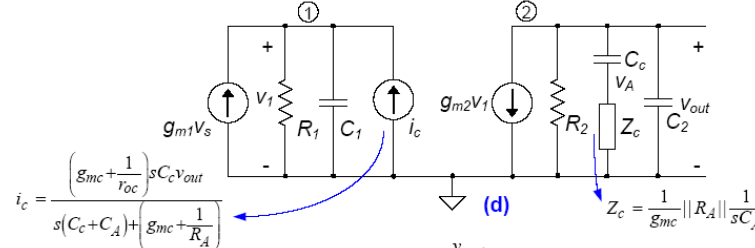
(a)



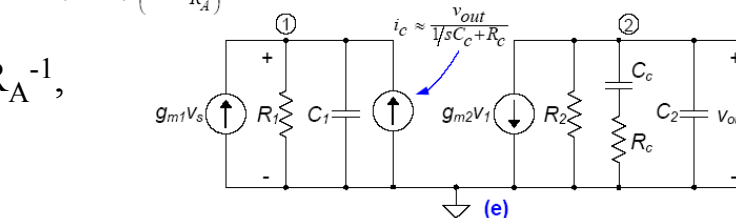
(b)



(c)



(d)

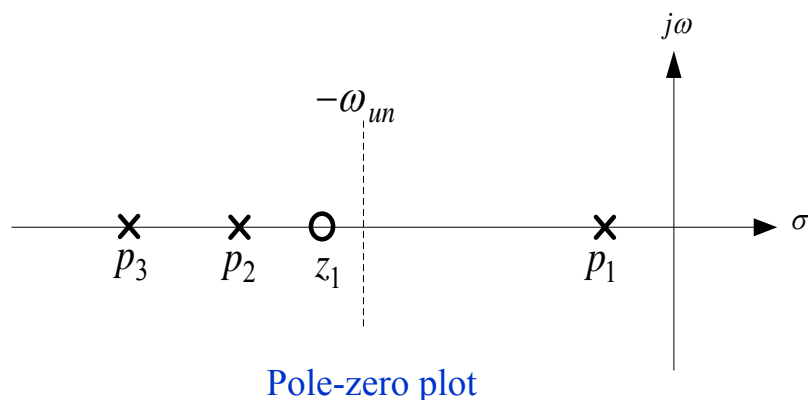


(e)

The small-signal model for a common gate indirect compensated op-amp topology is approximated to the simplified model seen in the last slide.

$$g_{mc} \gg r_{oc}^{-1}, R_A^{-1}, C_C \gg C_A$$

# Analytical Results for Indirect Compensation



- ❑ Pole  $p_2$  is much farther away from  $f_{un}$ .
  - ✓ Can use smaller  $g_{m2} \Rightarrow$  less power!
- ❑ LHP zero improves phase margin.
- ❑ Much faster op-amp with lower power and smaller  $C_C$ .
- ❑ Better slew rate as  $C_C$  is smaller.

$$\frac{v_{out}}{v_s} = -A_v \left( \frac{1 + b_1 s}{1 + a_1 s + a_2 s^2 + a_3 s^3} \right)$$

$$z_1 \approx -\frac{1}{R_c C_c} \quad \text{LHP zero}$$

$$p_1 \approx -\frac{1}{a_1} = -\frac{1}{g_{m2} R_2 R_1 C_c}$$

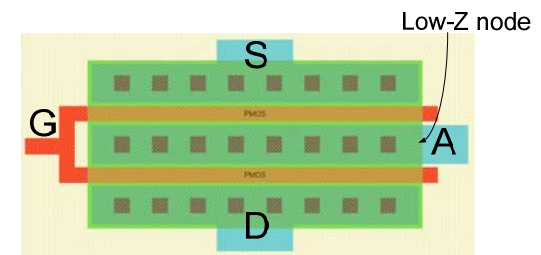
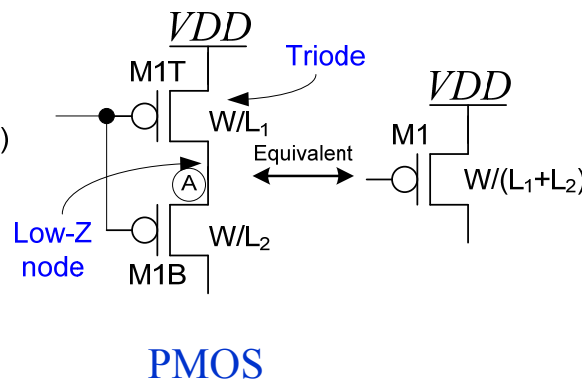
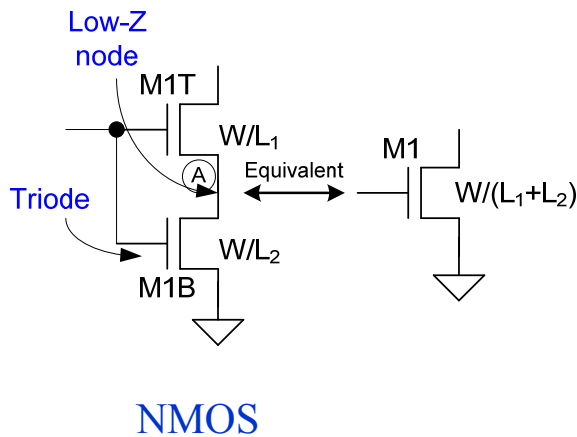
$$p_2 \approx -\frac{a_1}{a_2} = -\frac{g_{m2} R_1 C_c}{C_2 (R_c C_c + R_1 C_1)} \approx -\frac{g_{m2} C_c}{C_L C_1}$$

$$p_3 \approx -\frac{a_2}{a_3} = -\left[ \frac{1}{R_c C_c} + \frac{1}{R_1 C_1} \right]$$

$$f_{un} = \frac{|p_1| A_v}{2\pi} \approx \frac{g_{m1}}{2\pi C_c}$$

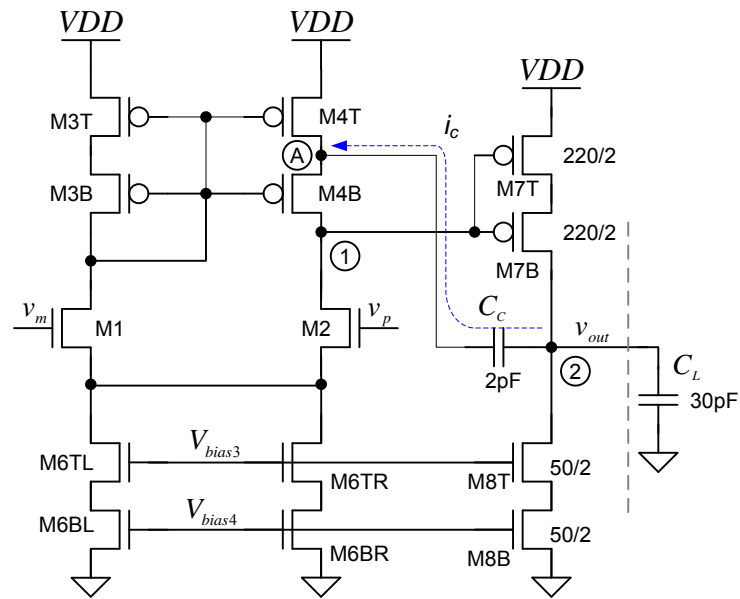
# Indirect Compensation Using Split-Length Devices

- ❑ As VDD scales down, cascoding is becoming tough. Then how to realize indirect compensation as we have no low-Z node available?
- ❑ Solution: Employ split-length devices to create a low-Z node.
  - ✓ Creates a pseudo-cascode stack but its really a single device.
- ❑ In the NMOS case, the lower device is always in triode hence node-A is a low-Z node. Similarly for the PMOS, node-A is low-Z.



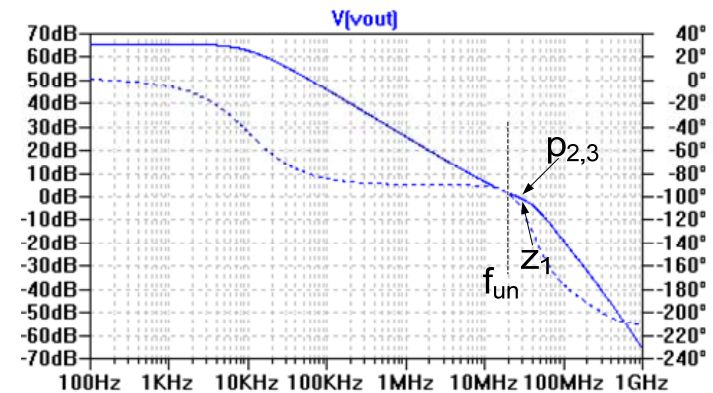
Split-length  $44/4(=22/2)$   
PMOS layout

# Split-Length Current Mirror Load (SLCL) Op-amp

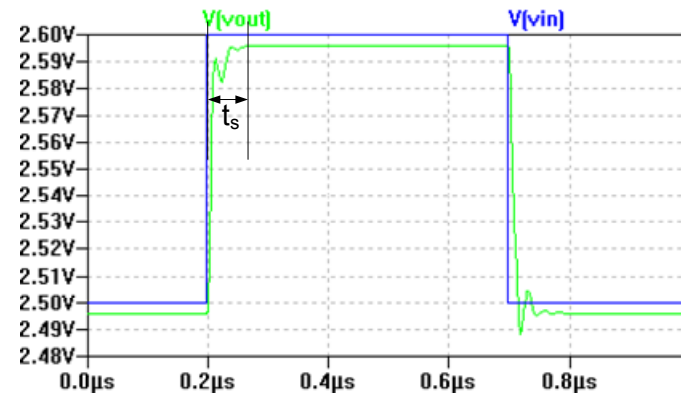


Unlabeled NMOS are 10/2.  
Unlabeled PMOS are 22/2.

- The current mirror load devices are split-length to create low-Z node-A.
- Here,  $f_{un} = 20\text{MHz}$ ,  $PM = 75^\circ$  and  $t_s = 60\text{ns}$ .



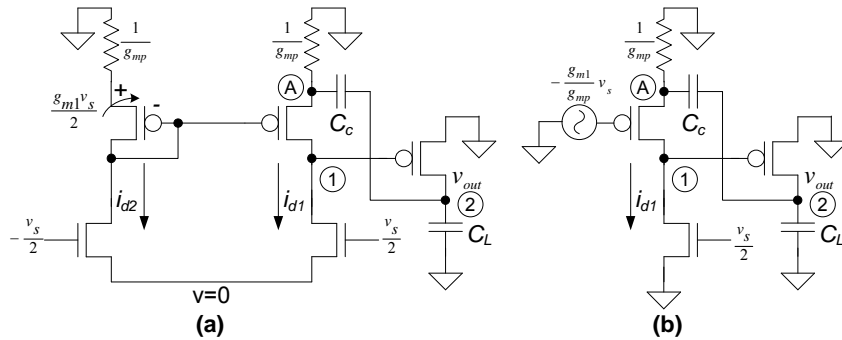
Frequency Response



Small step-input settling in follower configuration



# SLCL Op-amp Analysis

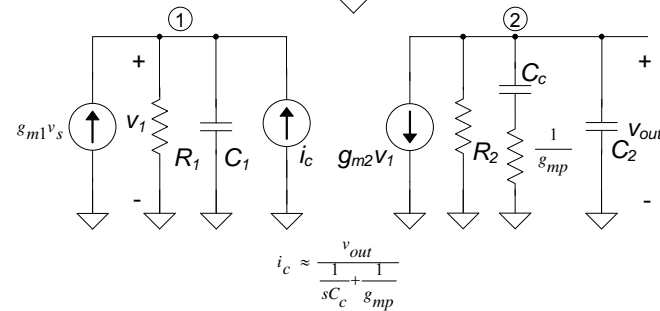
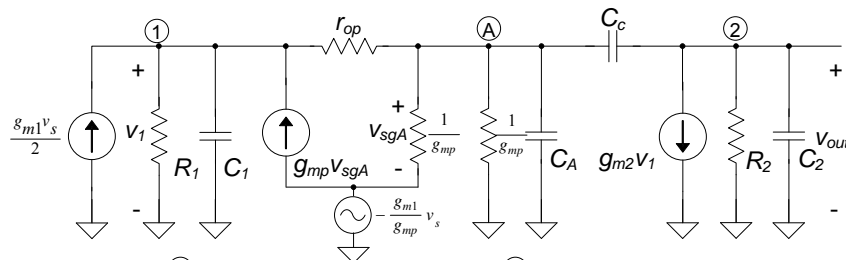


$$f_{un} = \frac{g_{m1}}{2\pi(2C_c)}$$

$$p_1 \approx -\frac{1}{2g_{m2}R_2R_1C_c}$$

$$|Re(p_{2,3})| = \frac{g_{m2}}{C_L} \sqrt{\frac{g_{mp}C_L}{g_{m2}C_1}}$$

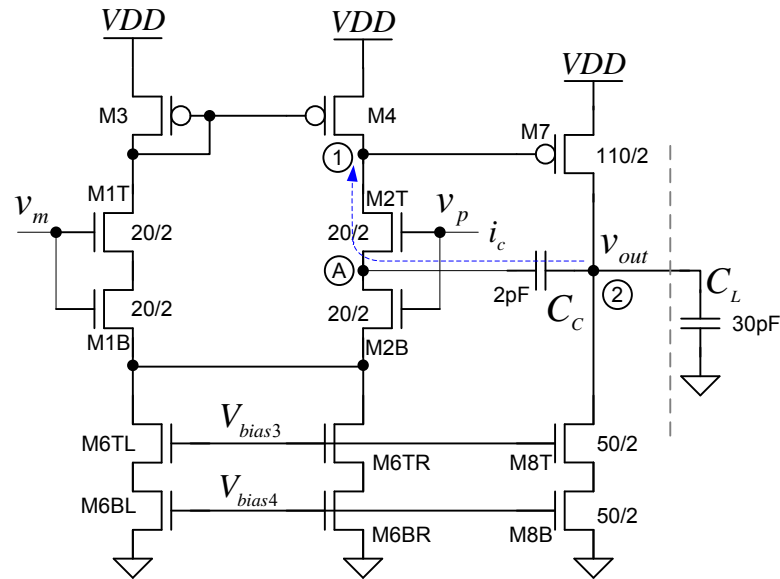
$$z_1 \approx -\frac{4g_{mp}}{3(C_c + C_A)} = -\frac{4\sqrt{2}g_{m1}}{3(C_c + C_A)} \approx \frac{8\sqrt{2}}{3}\omega_{un}$$



$$i_c \approx \frac{v_{out}}{\frac{1}{sC_c} + \frac{1}{g_{mp}}}$$

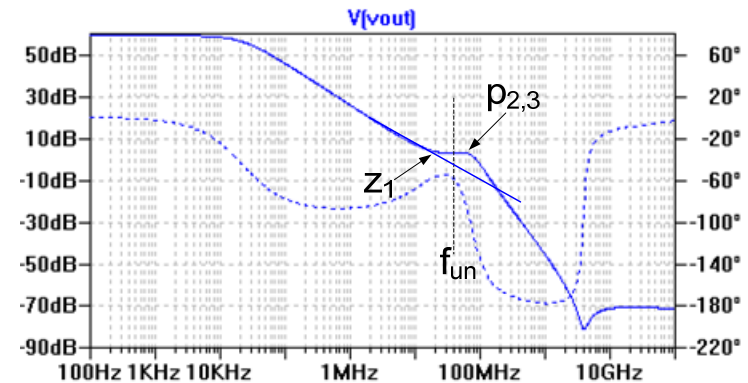
- Here  $f_{z1} = 3.77f_{un}$ 
  - ✓ LHP zero appears at a higher frequency than  $f_{un}$ .

# Split-Length Diff-Pair (SLDP) Op-amp

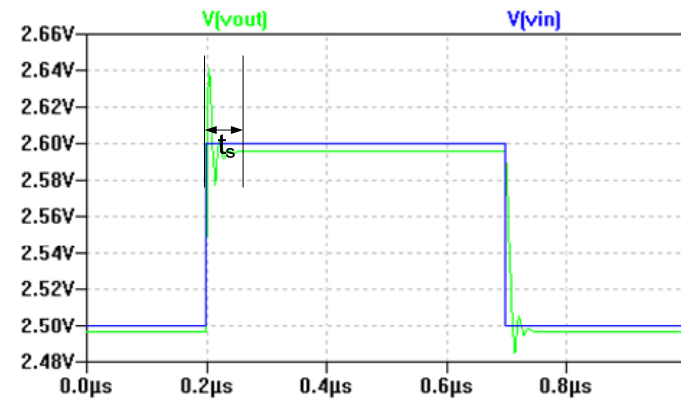


Unlabeled NMOS are 10/2.  
Unlabeled PMOS are 22/2.

- ❑ The diff-pair devices are split-length to create low-Z node-A.
- ❑ Here,  $f_{un}=35\text{MHz}$ ,  $PM=62^\circ$ ,  $t_s=75\text{ns}$ .
- ❑ Better PSRR due to isolation of node-A from the supply rails.

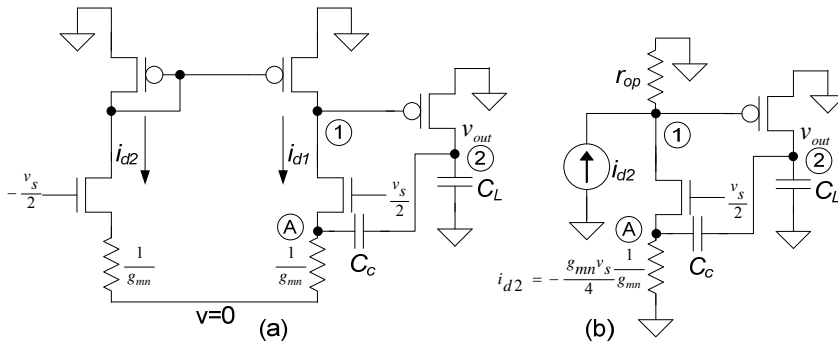


Frequency Response



Small step-input settling in follower configuration

# SLDP Op-amp Analysis

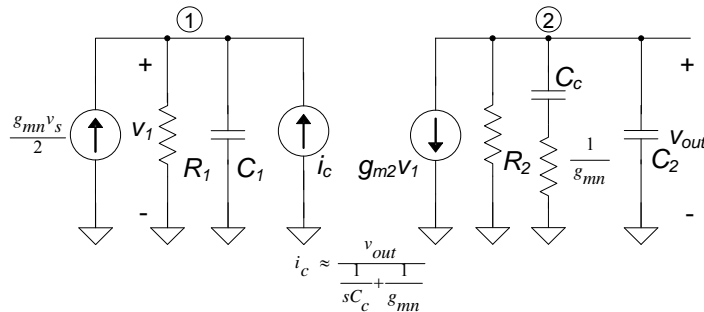
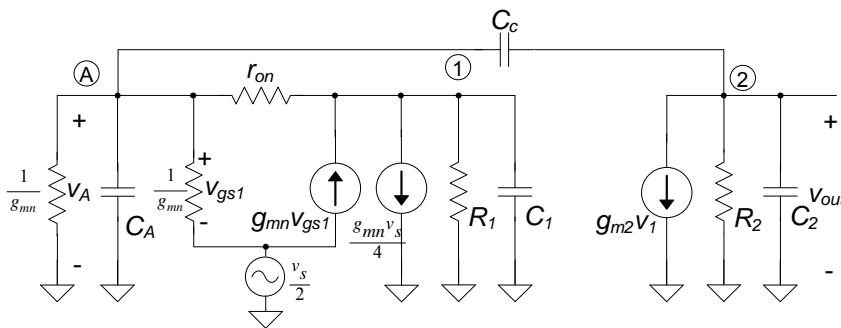


$$f_{un} = \frac{2g_{m1}}{2\pi C_c}$$

$$p_1 \approx -\frac{2}{g_{m2}R_2R_1C_c}$$

$$|Re(p_{2,3})| = \frac{g_{m2}}{C_L} \sqrt{\frac{g_{mp}C_L}{g_{m2}C_1}}$$

$$z_1 \approx -\frac{4g_{mn}}{3(C_c + C_A)} = -\frac{4\sqrt{2}g_{m1}}{3(C_c + C_A)} \approx \frac{2\sqrt{2}}{3}\omega_{un}$$



$$i_c \approx \frac{v_{out}}{\frac{1}{sC_c} + \frac{1}{g_{mn}}}$$

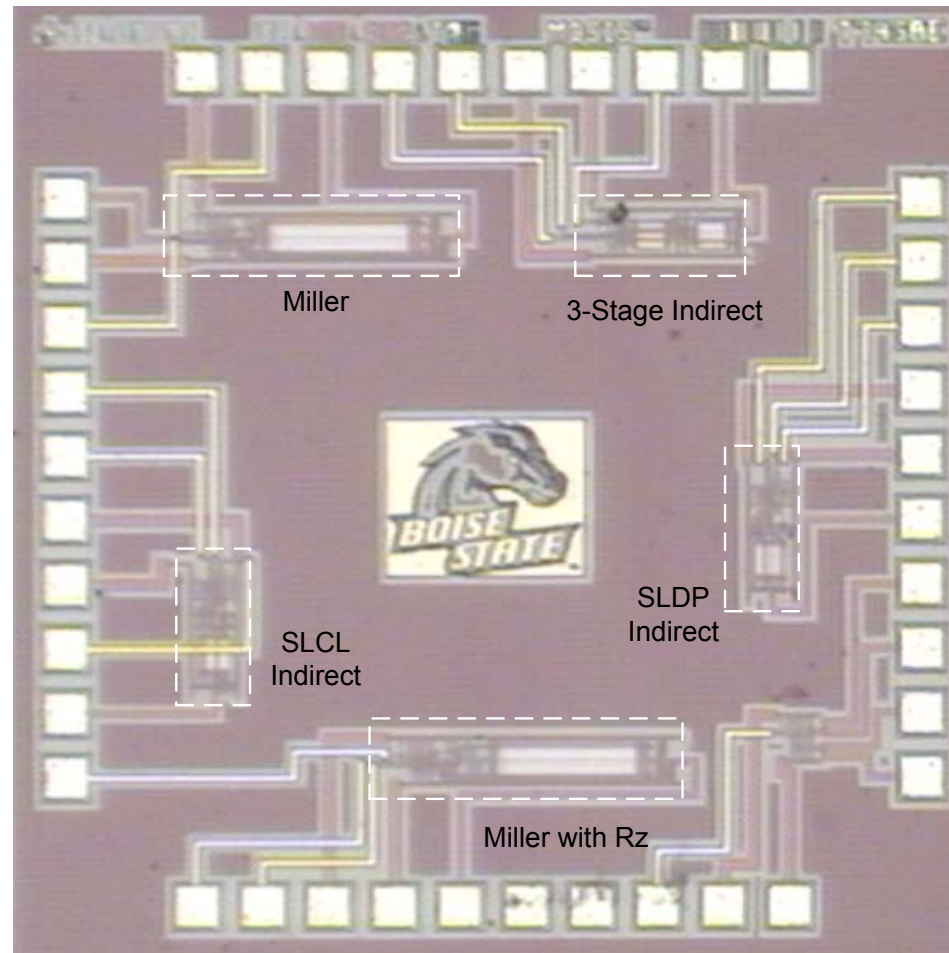
Here  $f_{z1} = 0.94f_{un}$ ,

✓ LHP zero appears slightly before  $f_{un}$  and flattens the magnitude response.

✓ This may degrade the phase margin.

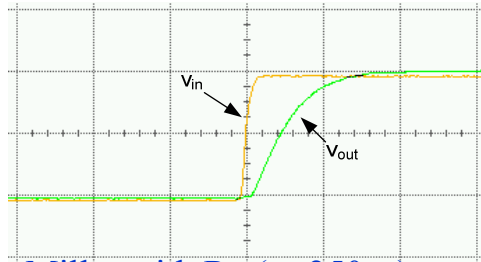
Not as good as SLCL, but is of great utility in multi-stage op-amp design due to higher PSRR.

# Test Chip 1: Two-stage Op-amps

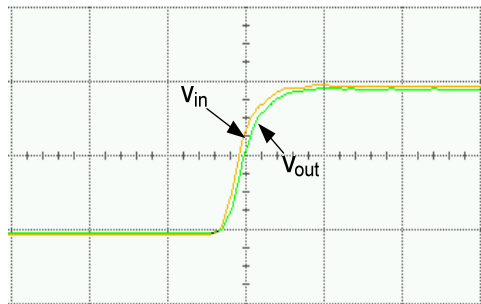


- ❑ AMI C5N 0.5 $\mu$ m CMOS, 1.5mmX1.5mm die size.

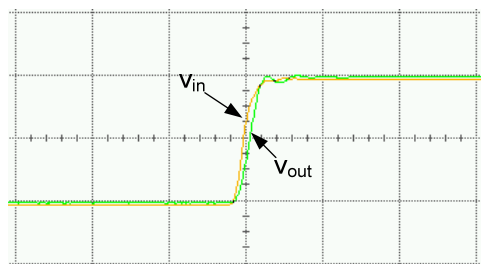
# Test Results and Performance Comparison



Miller with  $R_z$  ( $t_s=250\text{ns}$ )



SLCL Indirect ( $t_s=60\text{ns}$ )



SLDP Indirect ( $t_s=75\text{ns}$ )

Performance comparison of the op-amps for  $C_L=30\text{pF}$ .

Op-amp Topology	$A_{DC}$ (dB)	$f_{un}$ (MHz)	$C_C$ (pF)	PM	$t_s$ (ns)	Power (mW)	Layout area ( $\text{mm}^2$ )
Miller	57	2.5	10	$74^\circ$	270	1.2	0.031
Miller with $R_z$	57	2.7	10	$85^\circ$	250	1.2	0.034
SLCL (this work)	66	20	2	$75^\circ$	60	0.7	0.015
SLDP (this work)	60	35	2	$62^\circ$	75	0.7	0.015

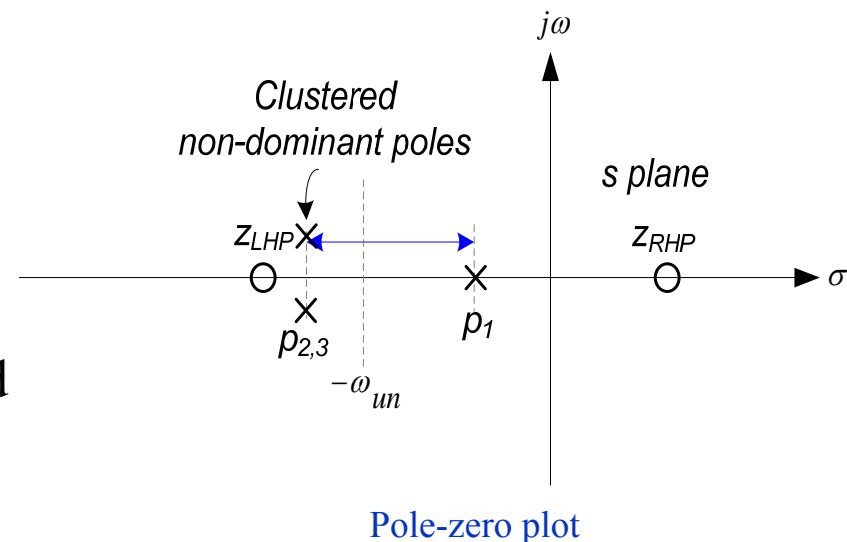
- 10X gain bandwidth ( $f_{un}$ ).
- 4X faster settling time.
- 55% smaller layout area.
- 40% less power consumption.



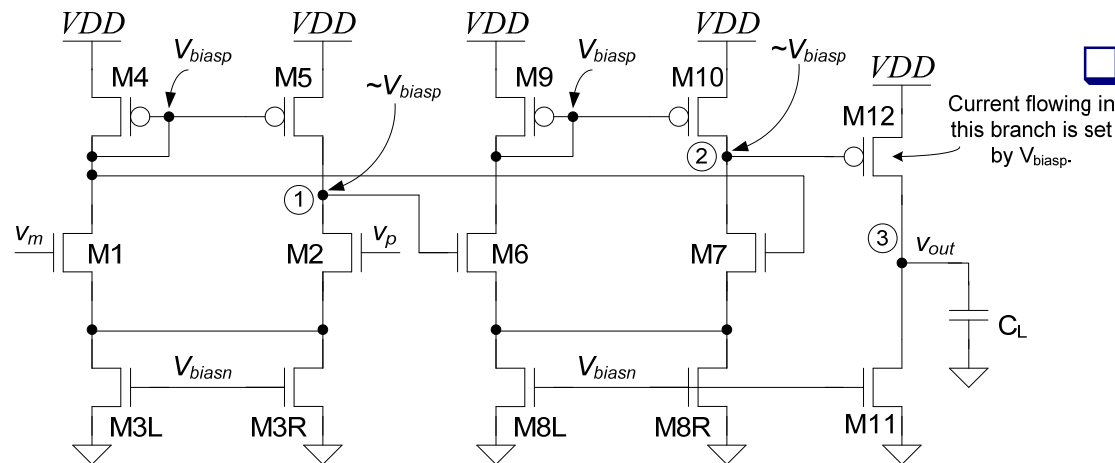
# MULTI-STAGE OP-AMP DESIGN

## Three-Stage Op-amps

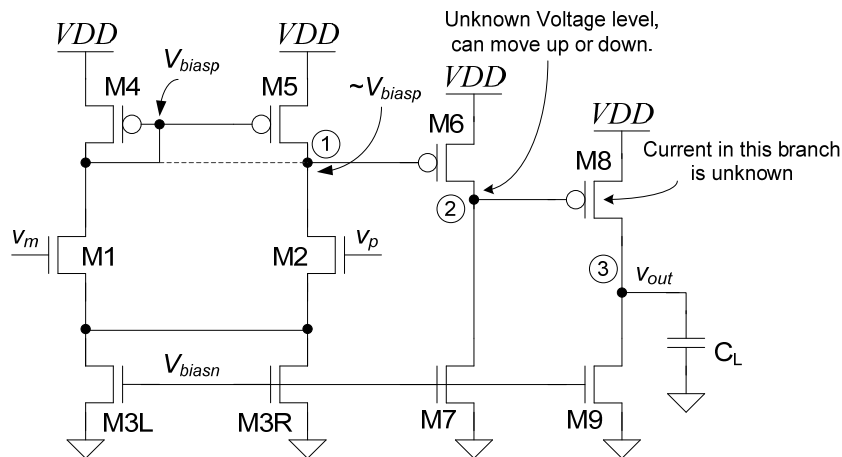
- ❑ Higher gain can be achieved by cascading three gain stages.
  - ✓ ~100dB in 0.5 $\mu$ m CMOS
- ❑ Results in at least a third order system
  - ✓ 3 poles and two zeros.
  - ✓ RHP zero(s) degrade the phase margin.
- ❑ Hard to compensate and stabilize.
- ❑ Large power consumption compared to the two-stage op-amps.



# Biassing of Multi-Stage Op-amps



Robust Biasing



Fallible Biasing

Diff-amps should be employed in inner gain stages to properly bias second and third gain stages

- ✓ Current in third stage is precisely set.
- ✓ Robust against large offsets.
- ✓ Boosts the CMRR of the op-amp (needed).

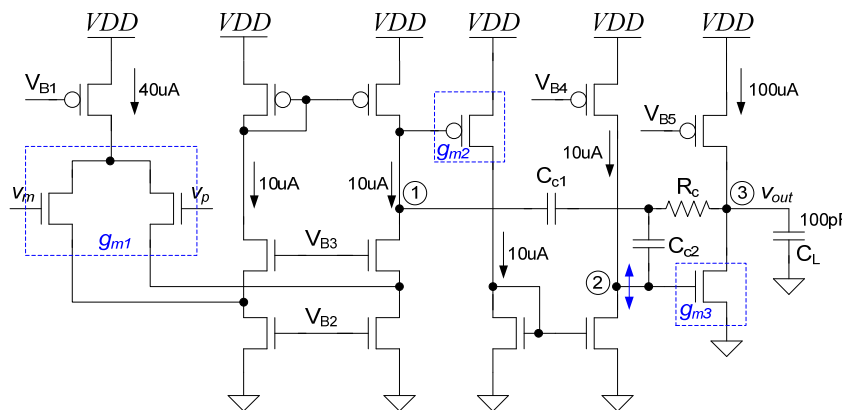
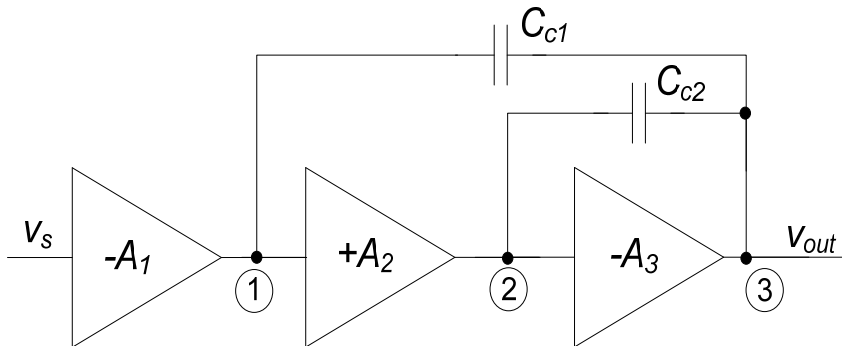
Common source second stage should be avoided.

- ✓ Will work in feedback configuration but will have offsets in nano-CMOS processes.



# Conventional Three-Stage Topologies

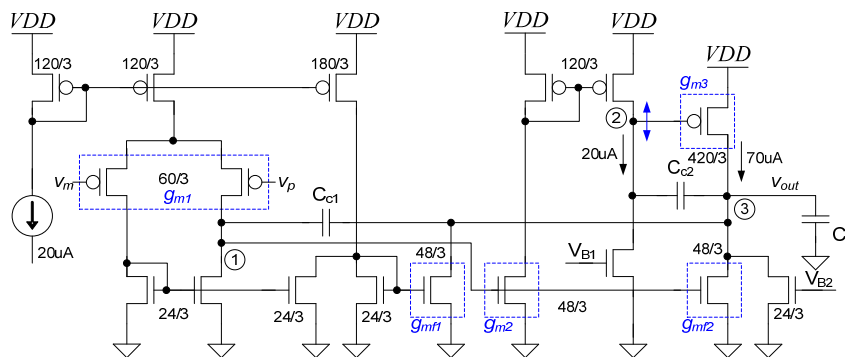
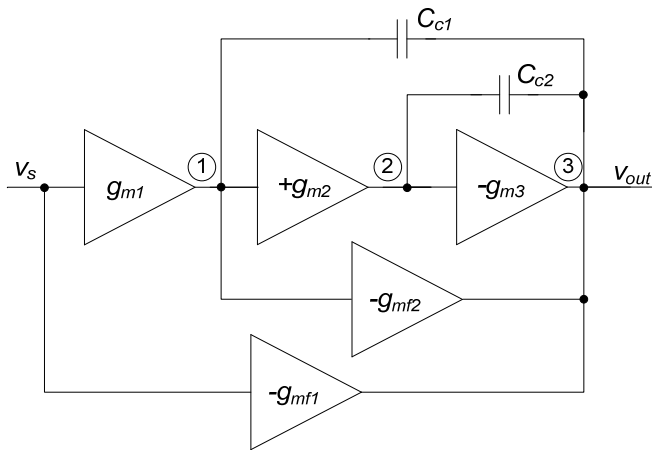
## Nested Miller Compensation (NMC) [6]



- ❑ Requires  $p_3=2p_2=4\omega_{un}$  for stability (Butterworth response)
  - ✓ Huge power consumption
- ❑ RHP zero appears before the LHP zero and degrades the phase margin.
- ❑ Second stage is non-inverting
  - ✓ Implemented using a current mirror.
  - ✓ Excess forward path delay (not modeled or discussed in the literature).

# Conventional Three-Stage Topologies contd.

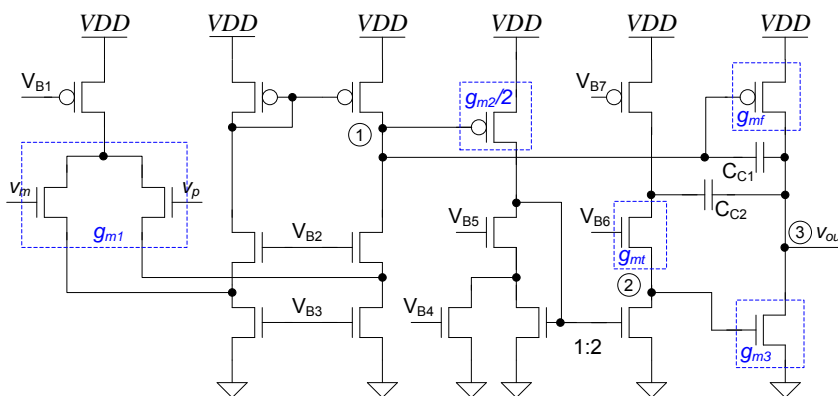
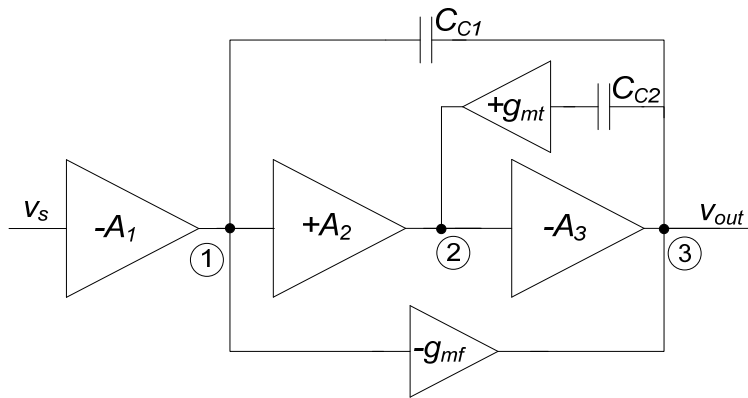
## Nested Gm-C Compensation (NGCC) [7]



- ❑ Employs feed-forward  $g_m$ 's to eliminate zeros.
  - ✓  $g_{mf1} = g_{m1}$  and  $g_{mf2} = g_{m2}$
- ❑ Class AB output stage.
- ❑ Hard to implement  $g_{mf1}$  which tracks  $g_{m1}$  for large signal swings.
  - ✓ Also wasteful of power.
- ❑  $g_{mf2}$  is a power device and will not always be equal to  $g_{m2}$ .
  - ✓ Compensation breaks down.
- ❑ Still consumes large power.

# Conventional Three-Stage Topologies contd.

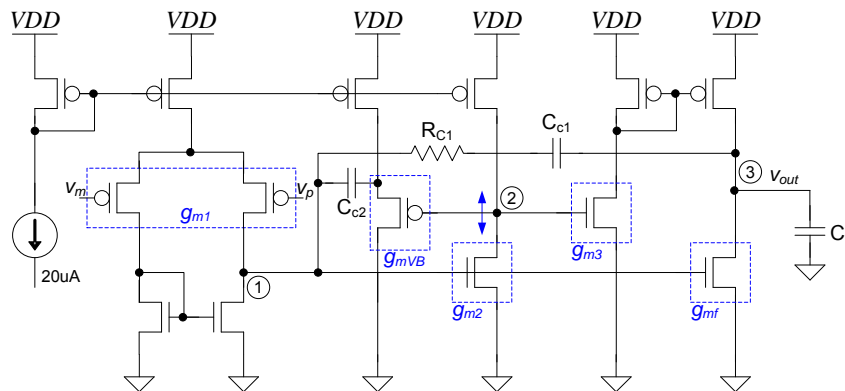
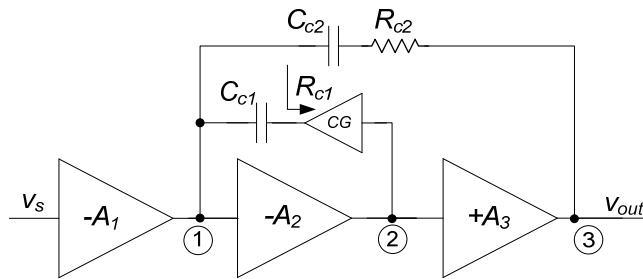
## Transconductance with Capacitive Feedback Compensation (TCFC) [14]



- Four poles and double LHP zeros
  - ✓ One LHP zero  $z_1$  cancels the pole  $p_3$ .
  - ✓ Other LHP zero  $z_2$  enhances phase margin.
- Set  $p_2 = 2\omega_{un}$  for  $PM = 60^\circ$ .
- Relatively low power.
- Still design criterions are complex.
- Complicated bias circuit.
  - ✓ More power.
- Excess forward path delay.

# Three-Stage Topologies: Latest in the literature

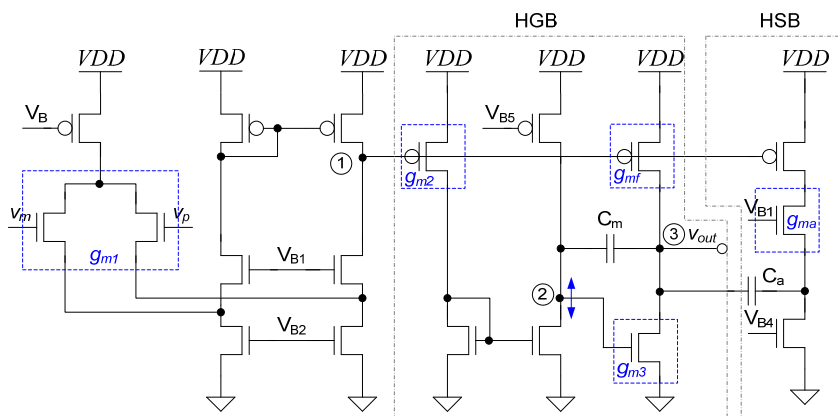
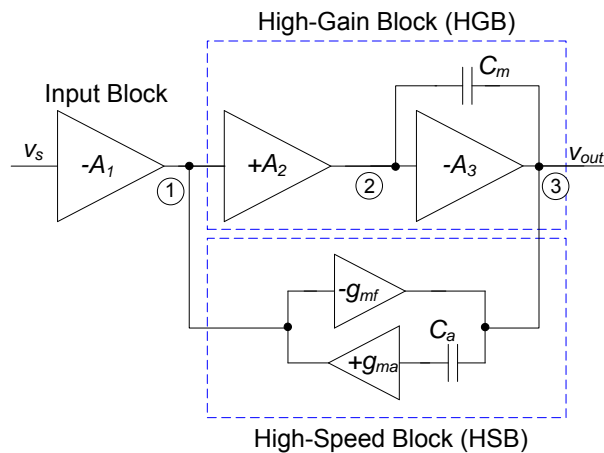
## Reverse Nested Miller with Voltage Buffer and Resistance (RNMC-VBR) [8]



- ❑ Employs reverse nesting of compensation capacitors
  - ✓ Since output is only loaded by only  $C_{C2}$ , results in potentially higher  $f_{un}$ .
  - ✓ Third stage is always non-inverting.
- ❑ Uses pole-zero cancellation to realize higher phase margins.
- ❑ Excess forward path delay.
- ❑ Biasing not robust against process variations. How do you control the current in the output buffer?

# Three-Stage Topologies: Latest in the literature contd.

## Active Feedback Frequency Compensation (AFFC) [9]



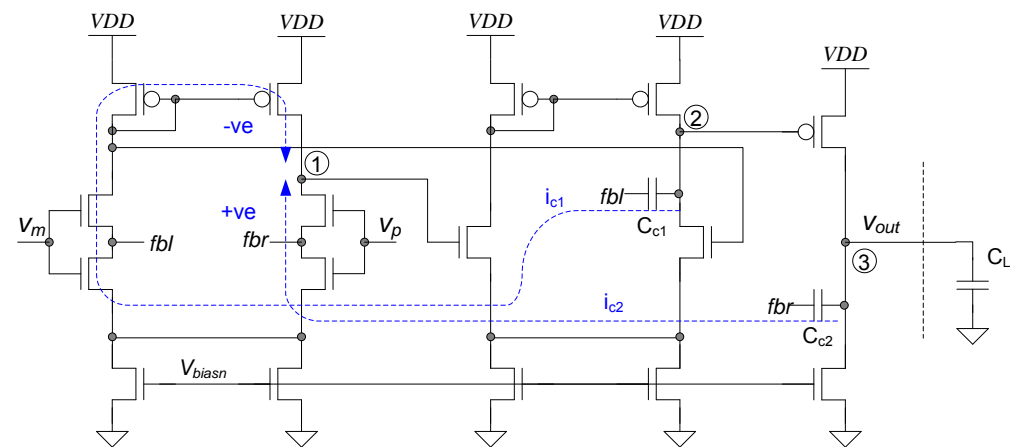
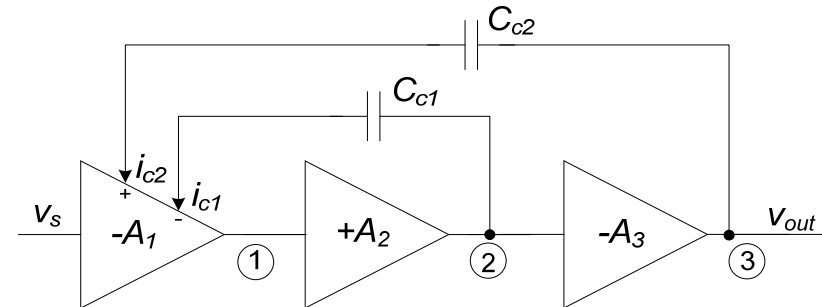
- ❑ Reversed nested with elimination of RHP zero.
  - ✓ High gain block (HGB) realizes gain by cascading stages.
  - ✓ High speed block (HSB) implements compensation at high frequencies.
- ❑ Complex design criterions.
- ❑ Excess forward path delay. Again, uses a non-inverting gain stage.
- ❑ Employs a complicated bias circuit.
  - ✓ More power consumption.

## Three-Stage Topologies: Latest in the literature contd.

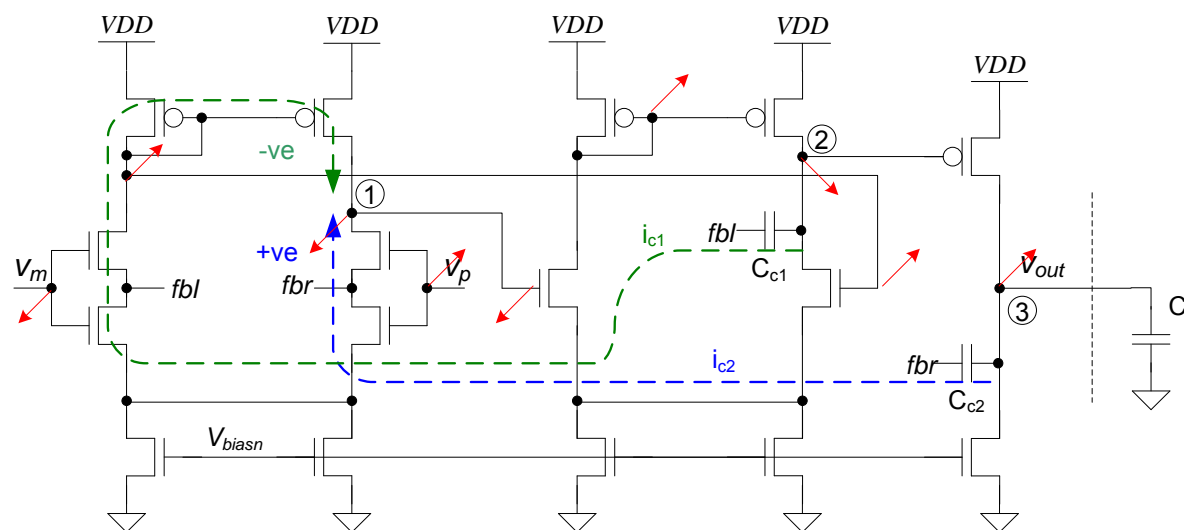
- ❑ Various topologies have been recently reported by combining the earlier techniques.
  - ✓ RNMC feed-forward with nulling resistor (RNMCFNR) [17].
  - ✓ Reverse active feedback frequency compensation (RAFFC) [17].
- ❑ Further improvements are required in
  - ✓ Eliminating excess forward path delay arising due to the compulsory non-inverting stages.
  - ✓ Robust biasing against random offsets in nano-CMOS.
  - ✓ Further reduction in power and circuit complexity.
  - ✓ Better PSRR.

# Indirect Compensation in Three-Stage Op-amps

- ❑ Indirectly feedback the compensation currents  $i_{c1}$  and  $i_{c2}$ .
  - ✓ Reversed Nested
    - ❑ Thus named RNIC.
- ❑ Employ diff-amp stages for robust biasing and higher CMRR.
- ❑ Use SLDP for higher PSRR.
- ❑ Minimum forward path delay.
- ❑ No compulsion on the polarity of gain stages.
  - ✓ Can realize any permutation of stage polarities by just changing the sign of the fed-back compensation current using 'fbr' and 'fbl' nodes.
- ❑ Low-voltage design.
- ❑ Note Class A (we'll modify after theory is discussed).



## Indirect Compensation in Three-Stage Op-amps contd.

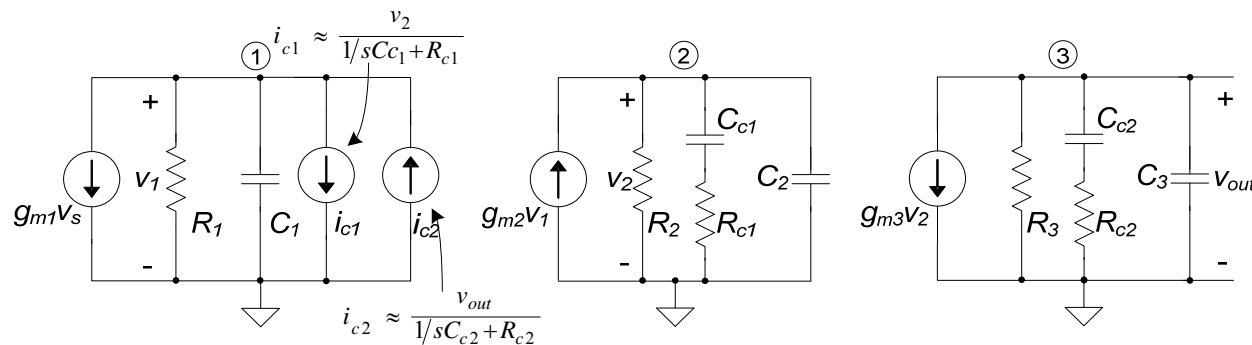


- ❑ Note the red arrows showing the node movements and the signs of the compensation currents.
  - ✓ fbr and fbl are the low-Z nodes used for indirect compensation (have resistances  $R_{c1}$  and  $R_{c2}$  attached to them).
- ❑ The  $C_C$ 's are connected across two-nodes which move in opposite direction for overall negative feedback the compensation loops.
- ❑ Note feedback and forward delays!



# Analysis of the Indirect Compensated 3-Stage Op-amp

- Plug in the indirect compensation model developed for the two-stage op-amps.



$$\frac{v_{out}}{v_s} = A_v \left( \frac{b_0 + b_1 s + b_2 s^2}{a_0 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4 + a_5 s^5} \right)$$

$$z_1 = -\frac{1}{R_{c1} C_{c1}}$$

$$z_2 = -\frac{1}{R_{c2} C_{c2}}$$

Two LHP zeros

$$p_1 \approx -\frac{a_0}{a_1} = -\frac{1}{g_{m3} R_3 g_{m2} R_2 R_1 C_{c2}}$$

$$f_{un} = \frac{|p_1| A_v}{2\pi} \approx \frac{g_{m1}}{2\pi C_{c2}}$$

Four non-dominant poles.

# Pole-zero Cancellation

- ❑ Poles  $p_{4,5}$  are parasitic conjugated poles located far away in frequency.
  - ✓ Appear due to the loading of the nodes fbr and fbl.
- ❑ The small signal transfer function can be written as

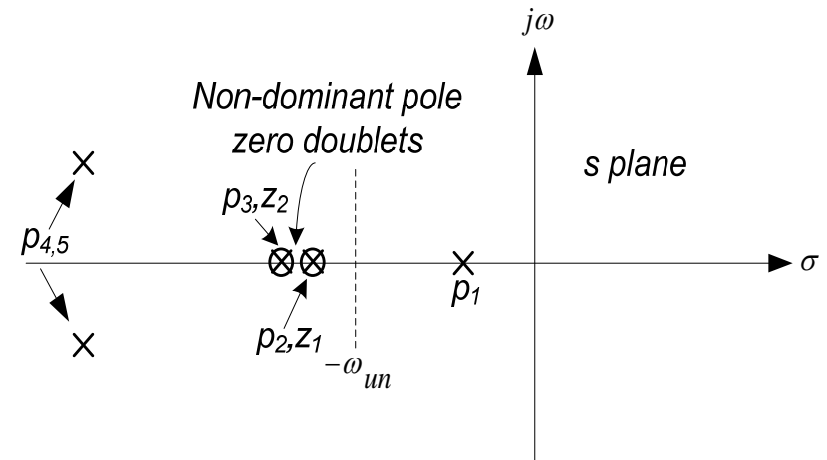
$$A(s) = \frac{\cancel{(b_0 + b_1 s + b_2 s^2)}}{(1 + s/p_1) \cancel{\left(1 + \frac{a_2}{a_1} s + \frac{a_3}{a_1} s^2\right)} \left(1 + \frac{a_4}{a_3} s + \frac{a_5}{a_3} s^2\right)}$$

- ❑ The quadratic expression in the denominator describing the poles  $p_2$  and  $p_3$  can be canceled by the numerator which describes the LHP zeros.
  - ✓ Results in LHP zeros  $z_1$  and  $z_2$  canceling the poles  $p_2$  and  $p_3$  resp.
- ❑ The resulting expression looks like a single pole system for low frequencies. →Phase margin close to  $90^\circ$ .

$$\frac{v_{out}}{v_s} \approx \frac{-A_v}{\left(1 - \frac{s}{p_1}\right) \left(1 + \frac{a_4}{a_3} s + \frac{a_5}{a_3} s^2\right)} \approx \frac{-A_v}{\left(1 - \frac{s}{p_1}\right)} \text{ for } f \ll f_T$$

## Pole-zero Cancellation contd.

- ❑ Place pole-zero doublets ( $p_2-z_1$  and  $p_3-z_2$ ) out of  $f_{un}$  for clean transients.
  - ✓ i.e.  $f_{p2}, f_{p3} > f_{un}$ .
- ❑ Best possible pole-zero arrangement for low power design.
- ❑ Results into design equations independent of parasitics ( $C_3 \approx C_L$  here).
- ❑  $R_{c1}$  and  $R_{c2}$  are realized by adding poly R's in series with  $C_{c1}$  and  $C_{c2}$ .
  - ✓ Also  $R_{c1}, R_{c2} \geq R_{c0}$ , the impedance attached to the low-Z nodes fbr/fbl.
- ❑ Robust against even 50% process variations in R's and C's as long as the pole-zero doublets stay out of  $f_{un}$ .

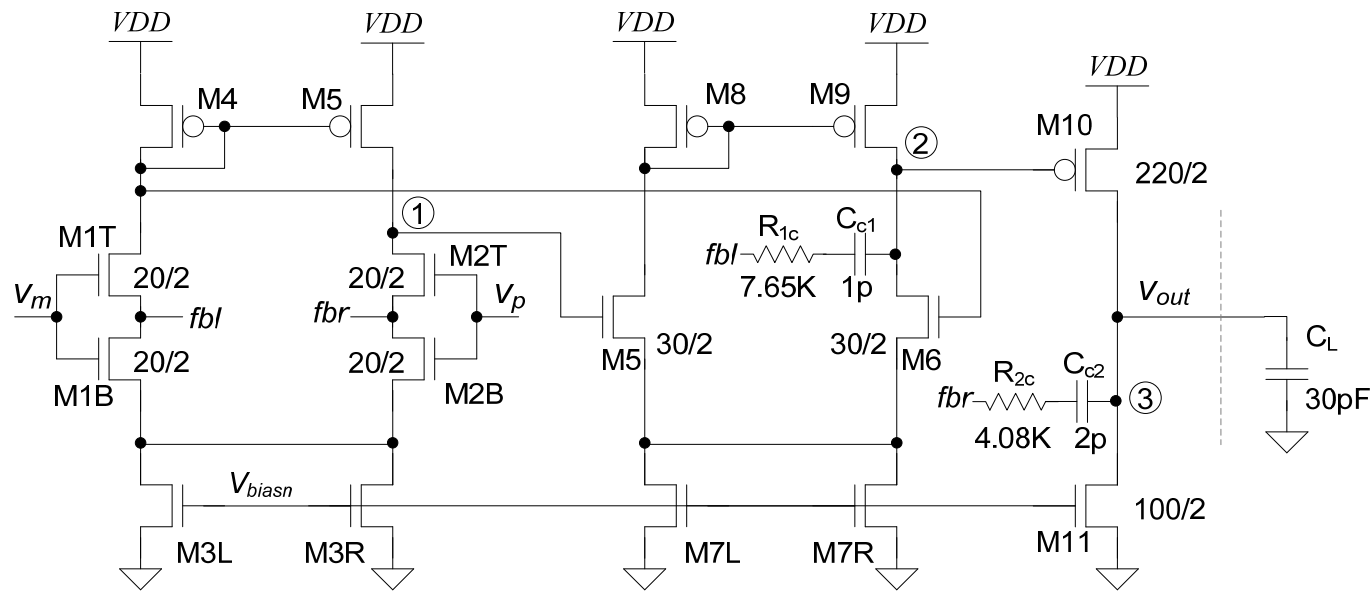


### Design Equations

$$R_{c1} \approx \frac{C_3}{g_{m3} C_{c2}}$$

$$R_{c2} \approx \frac{C_{c1}}{C_{c2}^2 g_{m3}} (C_3 + C_{c2})$$

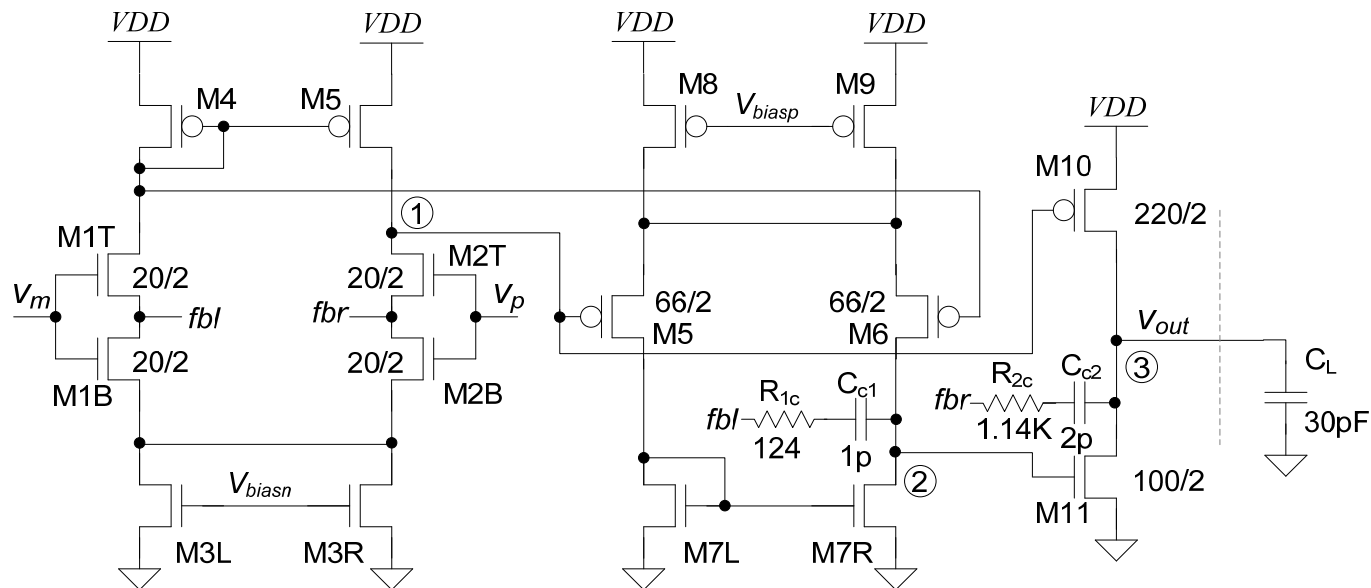
# Pole-zero cancelled Class-A Op-amp



Unlabeled NMOS are 10/2.  
Unlabeled PMOS are 22/2.

- ❑ A Here, the poly resistors are estimated as  $R_{kc} = R_{ck} - \frac{1}{\sqrt{2}g_{m1}}$ ,  $k=1,2$
- ❑ Low power, simple, robust and manufacturable topology\*.
- ❖ The presented three-stage op-amps have been designed with transient and SR performances to be comparable to their two-stage counterparts.

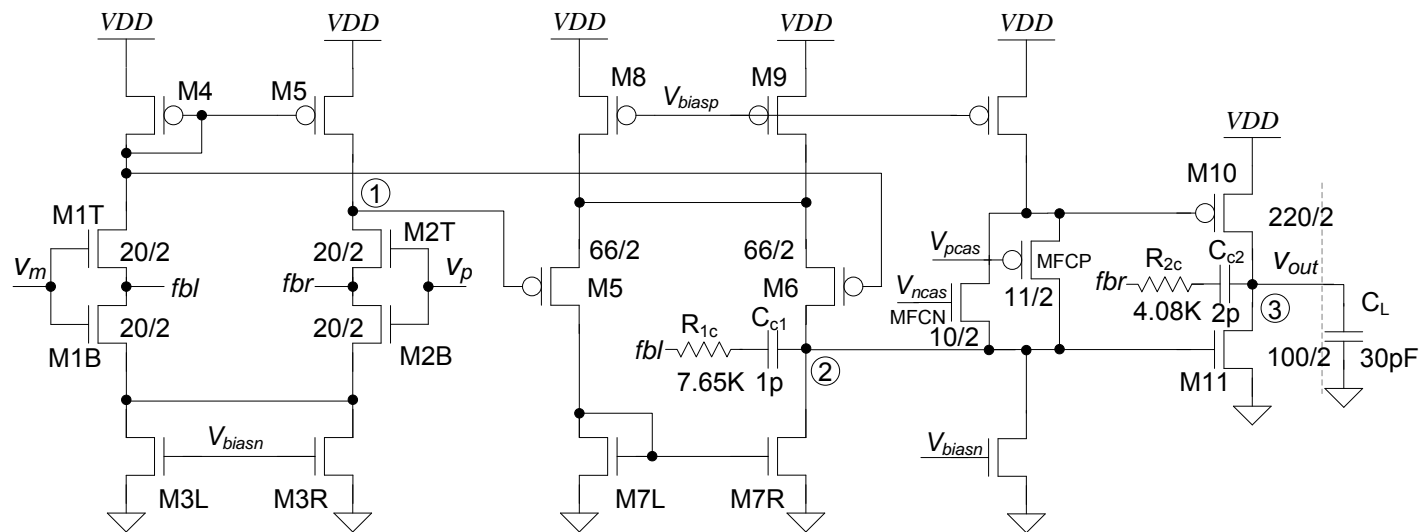
# Pole-zero cancelled Class-AB Op-amp 1



Unlabeled NMOS are 10/2.  
Unlabeled PMOS are 22/2.

- A dual-gain path, low-power Class-AB op-amp topology (RNIC-1).
- The design equation for  $R_{c1}$  is modified as 
$$R_{c1} \approx \frac{C_3}{g_{m3} C_{c2}} - \frac{1}{g_{m2}}$$

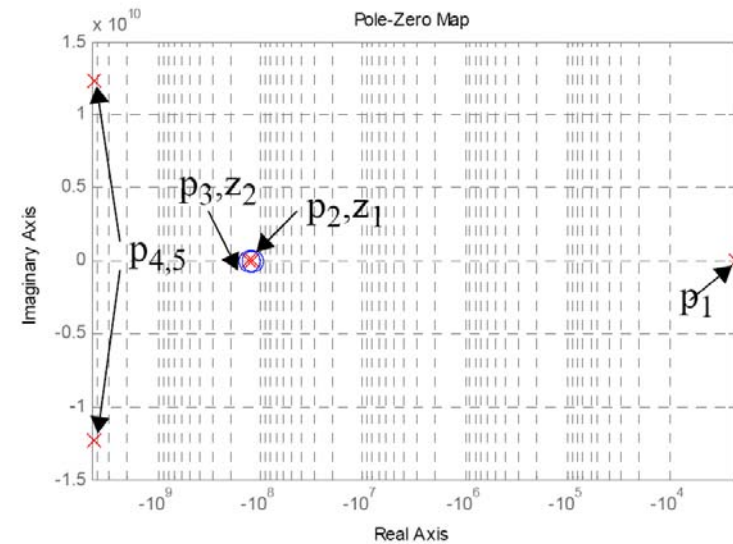
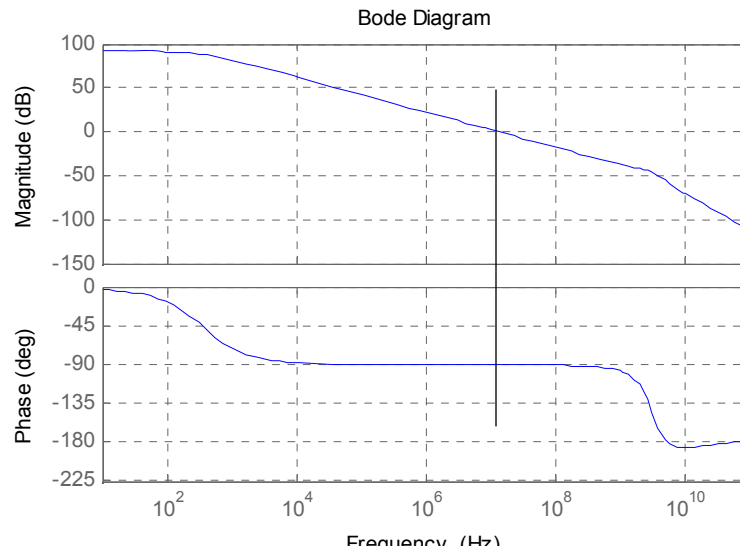
# Pole-zero cancelled Class-AB Op-amp 2



Unlabeled NMOS are 10/2.  
Unlabeled PMOS are 22/2.

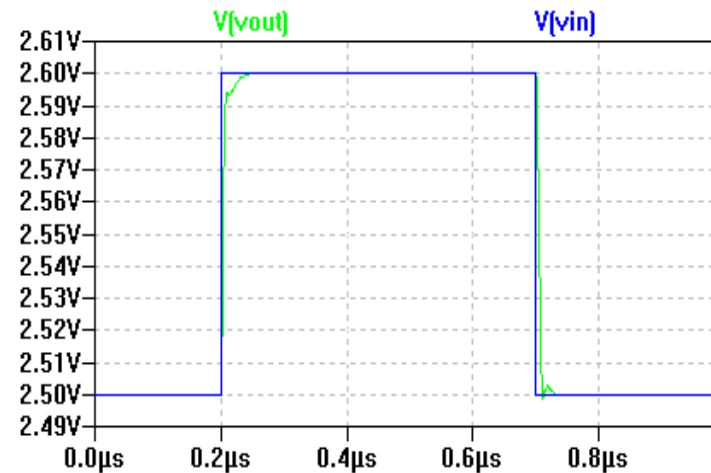
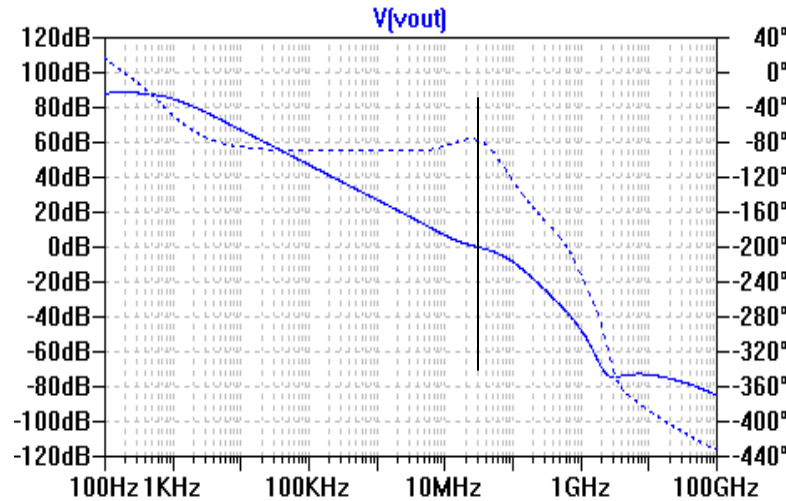
- A single-gain path, Class-AB op-amp topology for good THD performance.
  - ✓ Floating current source for biasing the output buffer.
  - ✓ Here,  $V_{ncas} = 2V_{GS}$  and  $V_{pcas} = VDD - 2V_{SG}$ .
  - ✓ Note the lack of gratuitous forward delay.

# Simulation of Three-stage Op-amps



- ❑ Analytical model of the Class-AB (RNIC-1) topology is simulated in MATLAB.
- ❑ The pole-zero plot illustrates the double pole-zero cancellation (collocation).
  - ✓  $p_4$  and  $p_5$  are parasitic poles located at frequencies close to that of the  $f_T$  limited (or mirror) poles.
- ❑ Here,  $f_{un} \approx 30\text{MHz}$  and  $PM = 90^\circ$  for  $C_L = 30\text{pF}$ .

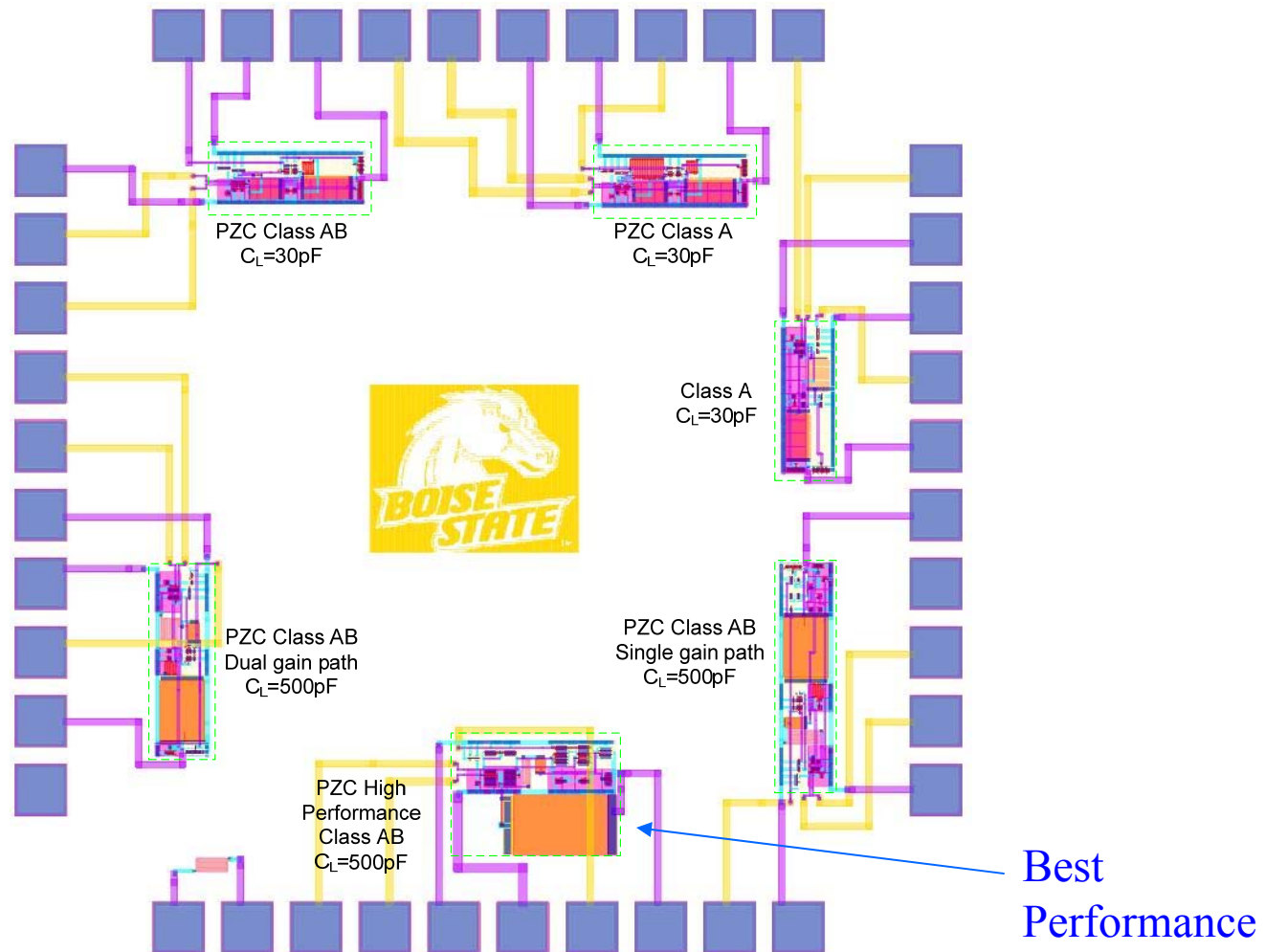
# Simulation of Three-stage Op-amps contd.



- ❑ SPICE simulation of the same Class AB op-amp.
- ❑  $C_L=30\text{pF}$ :  $f_{un}=30\text{MHz}$ ,  $PM\approx 88^\circ$ ,  $t_s=70\text{ns}$ ,  $0.84\text{mW}$ ,  $SR=20\text{V}/\mu\text{s}$ .
- ❑ As fast as a two-stage op-amp with only 20% more power, at 50%  $V_{DD}$  and with the same layout area (simpler bias circuit).
- ❑ Operates at  $V_{DD}$  as low as 1.25V in a 5V process (25% of  $V_{DD}$ ).
- ❑ SPICE simulation match with the MATLAB simulation
  - ✓ Our theory for three-stage indirect compensation is validated.



# Chip 2: Low-VDD 3-Stage Op-amps



□ AMI C5N 0.5 $\mu\text{m}$  CMOS, 1.5mmX1.5mm die size.

# Performance Comparison

Topology	$C_L$ (pF)	$V_{DD}$ (V)	$I_{DD}$ (mA)	Power (mW)	$f_{un}$ (MHz)	Avg. SR (V/ $\mu$ s)	$C_{c1}, C_{c2}$ (pF)	FoM <sub>S</sub> (MHz.pF/mW)	FoM <sub>L</sub> (V/ $\mu$ s.pF/mW)	IFoM <sub>S</sub> (MHz.pF/mA)	IFoM <sub>L</sub> (V/ $\mu$ s.pF/mA)
MNMC [10]	100	8	9.5	76	100	35	--	132	46	1053	368
NGCC [10]	20	2	0.34	0.68	0.61	2.5	--	18	74	36	147
NMCFNR [11]	100	2	0.2	0.4	1.8	0.79	30, 5.3	450	198	900	395
DFCFC [12]	1000	2	0.2	0.4	1	0.36	55, 3	2500	900	5000	1800
AFFC [9]	100	1.5	0.17	0.255	5.5	0.36	5.4, 4	2157	141	3235	212
ACBCF [13]	500	2	0.162	0.324	1.9	1	10, 3	2932	1543	5864	3086
TCFC [14]	150	1.5	0.03	0.045	2.85	1.035	1.1, 0.92	9500	3450	14250	5175
DPZCF [15]	500	1.5	0.15	0.225	1.4	2	30, 20	3111	4444	4667	6667
RNMCVBNR [16]	15	3	0.48	1.44	19.46	13.8	3, 0.7	203	144	608	431
SMFFC [17]	120	2	0.21	0.42	9	3.4	4	2571	971	5143	1943
RNMCFBNR [18]	500	3	0.085	0.255	2.4	1.8	11.5, 0.35	4706	3529	14118	10588
RAFFC [18]	500	3	0.105	0.315	2.4	1.95	11.5, 0.35	3810	3095	11429	9286
RAFFC Low-Power [18]	500	3	0.035	0.105	1.1	1.29	11.5, 0.35	5238	6143	15714	18429
RNIC-1 (This work)	30	3	0.28	0.84	30	20	1, 2	1071	714	3214	2143
RNIC-2 (This work)	500	3	0.18	0.54	12	8	5, 0.2	11111	7407	33333	22222
RNIC-3 (This work)	500	3	0.5	1.5	35	20	10, 0.2	11667	6667	35000	20000
RNIC-1A (This work)	30	2	0.28	0.56	15	20	1, 2	804	1071	1607	2143
RNIC-2A (This work)	500	2	0.18	0.36	6	20	5, 0.2	8333	27778	16667	55556
RNIC-3A (This work)	500	2	0.5	1	17	20	10, 0.2	8500	10000	17000	20000

## Figures of Merit

- ✓  $FoM_S = f_{un} C_L / \text{Power}$
- ✓  $FoM_L = SR \cdot C_L / \text{Power}$
- ✓  $IFoM_S = f_{un} C_L / I_{DD}$
- ✓  $IFoM_L = SR \cdot C_L / I_{DD}$

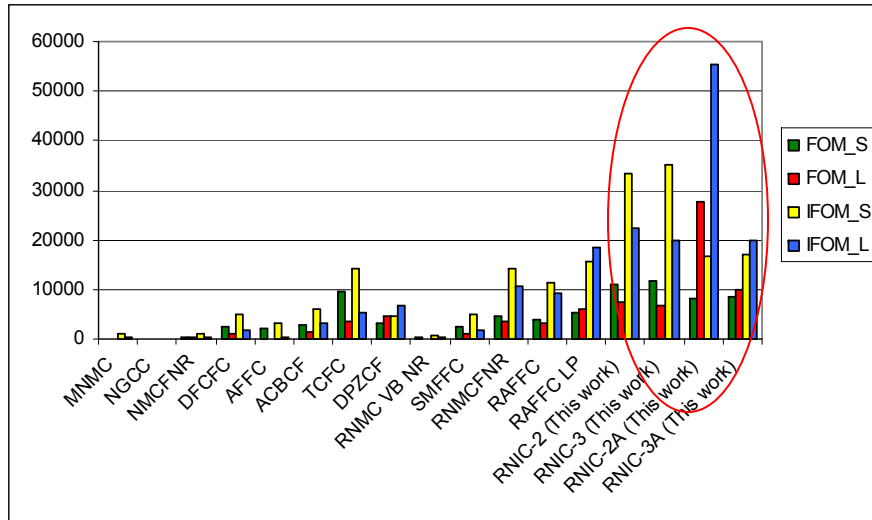
RNIC op-amp designed for 500pF load for a fair comparison.

FoMs > 2X than state-of-the-art at  $V_{DD} = 3V$ .

Comparable performance even at lower  $V_{DD} = 2V$ .

Practical, stable and production worthy.

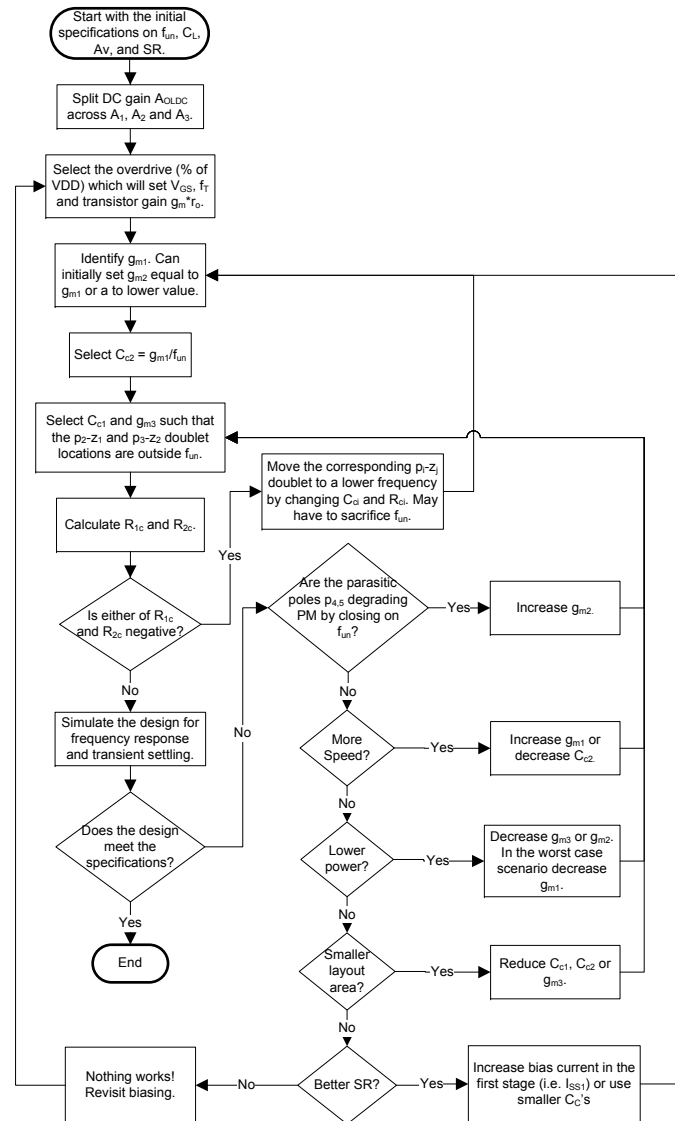
# Performance Comparison contd.



- Higher performance figures than state-of-the-art.
- 10X faster settling.
- Better phase margins.
- Layout area same or smaller.

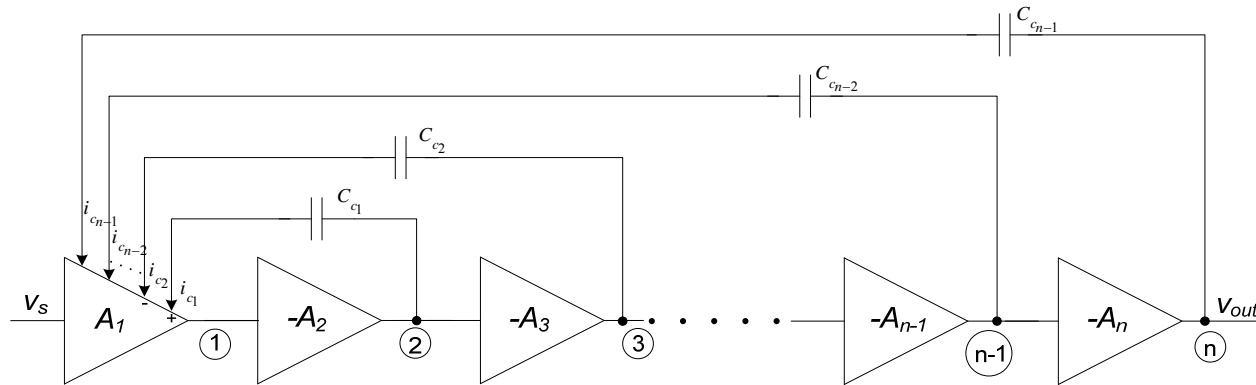
Op-amp Topology	VDD (V)	C <sub>L</sub> (pF)	Power (mW)	f <sub>un</sub> (MHz)	Avg. SR (V/μs)	PM	t <sub>s</sub> (ns)	Area (mm <sup>2</sup> )
RNMCFBNR [18]	3	500	0.255	2.4	1.8	58°	810	0.025
RAFFC [18]	3	500	0.315	2.4	1.95	58°	560	0.025
RAFFC Low-Power [18]	3	500	0.105	1.1	1.29	56°	1000	0.024
<b>RNIC-1 (This work)</b>	<b>3</b>	<b>30</b>	<b>0.84</b>	<b>30</b>	<b>20</b>	<b>89°</b>	<b>70</b>	<b>0.018</b>
<b>RNIC-2 (This work)</b>	<b>3</b>	<b>500</b>	<b>0.54</b>	<b>12</b>	<b>8</b>	<b>88°</b>	<b>250</b>	<b>0.022</b>
<b>RNIC-3 (This work)</b>	<b>3</b>	<b>500</b>	<b>1.5</b>	<b>35</b>	<b>20</b>	<b>72°</b>	<b>100</b>	<b>0.031</b>
<b>RNIC-1A (This work)</b>	<b>2</b>	<b>30</b>	<b>0.56</b>	<b>15</b>	<b>20</b>	<b>89°</b>	<b>90</b>	<b>0.018</b>
<b>RNIC-2A (This work)</b>	<b>2</b>	<b>500</b>	<b>0.36</b>	<b>6</b>	<b>20</b>	<b>88°</b>	<b>350</b>	<b>0.022</b>
<b>RNIC-3A (This work)</b>	<b>2</b>	<b>500</b>	<b>1</b>	<b>17</b>	<b>20</b>	<b>72°</b>	<b>150</b>	<b>0.031</b>

# Flowchart for RNIC Op-amp Design



# N-Stage Indirect Compensation Theory

- The three-stage indirect compensation theory has been extended to N-stages and the closed form small signal transfer function is obtained.

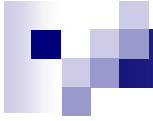


$$\begin{bmatrix} \frac{1}{Z_1} & -\frac{1}{Z_{c_1}} & \frac{1}{Z_{c_2}} & \dots & \dots & \frac{(-1)^{k-1}}{Z_{c_{k-1}}} & \dots & \frac{(-1)^{n-2}}{Z_{c_{n-2}}} & \frac{(-1)^{n-1}}{Z_{c_{n-1}}} \\ g_{m2} & \frac{1}{Z_2} & 0 & \dots & 0 & 0 & \dots & 0 & 0 \\ 0 & g_{m3} & \frac{1}{Z_3} & \dots & 0 & 0 & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & 0 & \dots \\ 0 & 0 & 0 & \dots & g_{m(k-1)} & \frac{1}{Z_k} & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & 0 & \dots \\ 0 & 0 & 0 & \dots & \dots & \dots & \dots & \frac{1}{Z_{n-1}} & 0 \\ 0 & 0 & 0 & \dots & \dots & \dots & \dots & g_{mn} & \frac{1}{Z_n} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ \dots \\ v_k \\ \dots \\ v_{n-1} \\ v_n \end{bmatrix} = \begin{bmatrix} g_{m1} V_s \\ 0 \\ 0 \\ \dots \\ 0 \\ \dots \\ 0 \\ 0 \end{bmatrix}$$

$$\frac{v_{out}}{V_s} = \frac{\left( \prod_{k=1}^n g_{mk} R_k \right) \prod_{j=1}^{n-1} (1 + s\tau_{c_{j-1}})}{\prod_{i=1}^n (1 + s\tau_i) \prod_{j=1}^{n-1} (1 + s\tau_{c_{j-1}}) + \left( \prod_{k=1}^n R_k \right) \sum_{r=2}^n \left( \frac{s C_{c_{r-1}}}{g_{m1}} \prod_{p=1}^r g_{mp} R_p \prod_{q=r+1}^n (1 + s\tau_q) \prod_{j=1}^{n-1} (1 + s\tau_{c_{j-1}}) \right)}$$

$$z_k = -\frac{1}{\tau_{c_k}} = -\frac{1}{R_{c_k} C_{c_k}}, \quad k=1, \dots, n-1$$

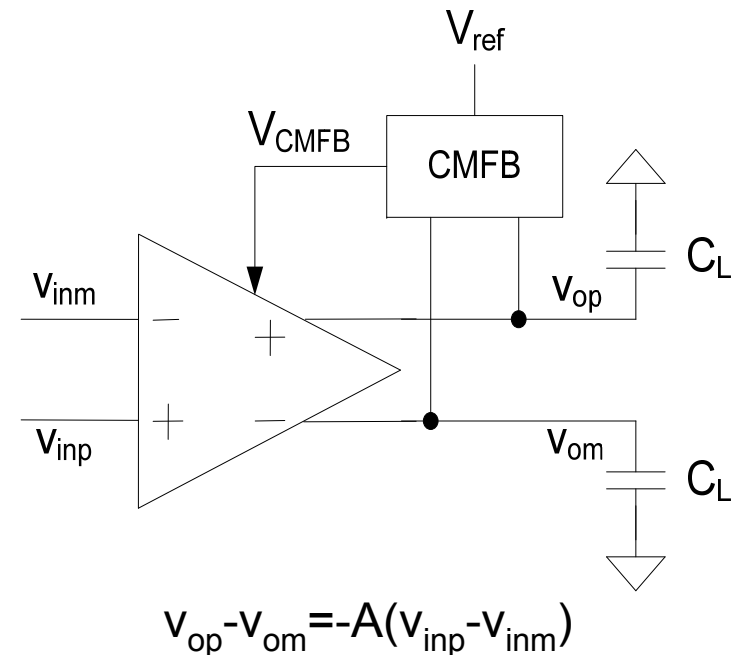
$$p_1 \approx -\frac{1}{\left( \prod_{k=2}^n g_{mk} R_k \right) R_1 C_{c_{n-1}}} \quad f_{un} \approx \left| \frac{A_v p_1}{2\pi} \right| = \frac{g_{m1}}{2\pi C_{c_{n-1}}}$$



# MULTI-STAGE FULLY-DIFFERENTIAL OP-AMPS

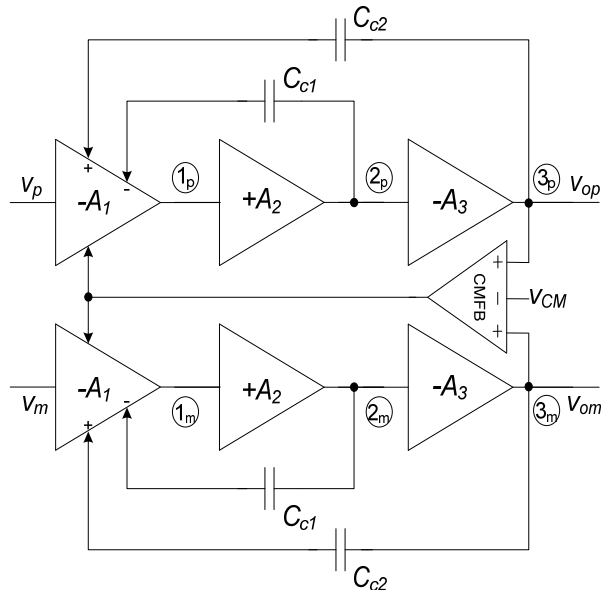
# Fully Differential Op-amps

- ❑ Analog signal processing uses ‘only’ fully differential (FD) circuits.
  - ✓ Cancels switch non-linearities and even order harmonics.
  - ✓ Double the dynamic range.
- ❑ Needs additional circuitry to maintain the output common-mode level.
  - ✓ Common-mode feedback circuit (CMFB) is employed.

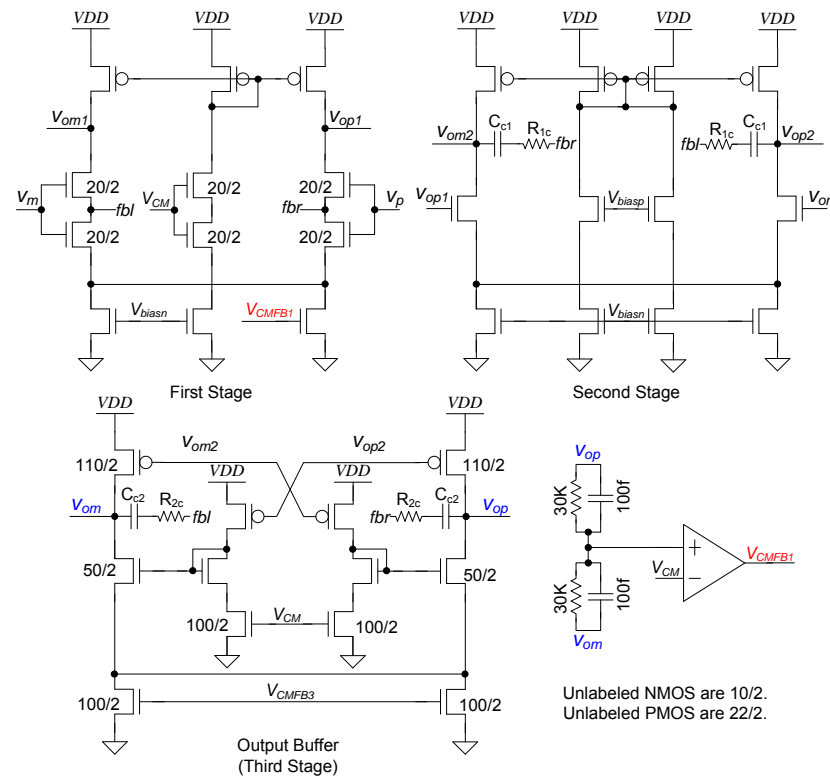


# Three-Stage FD Op-amp Design: Problems

Block Diagram



Circuit Implementation



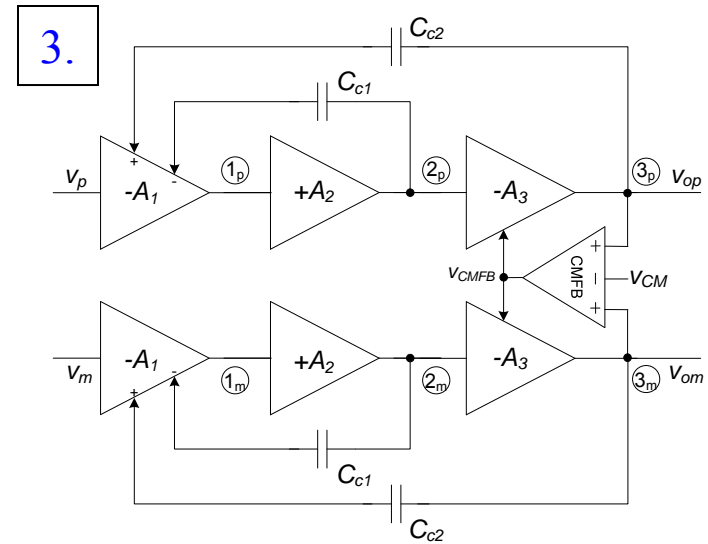
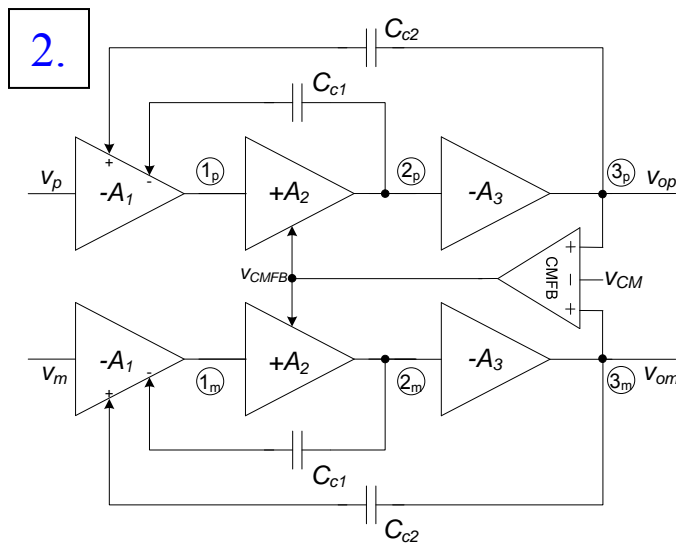
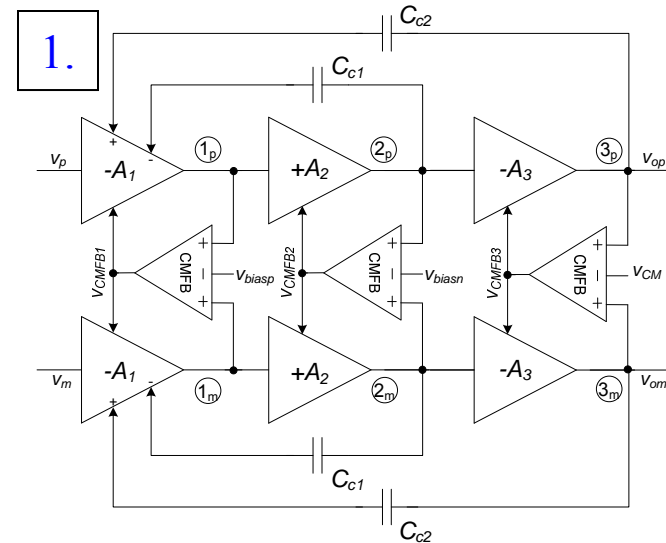
- ❑ The CMFB loop disturbs the DC biasing of the intermediate gain stages.
  - ✓ Degrades the gain, performance and may cause instability.



# Three-Stage FD Op-amp Design: Solutions

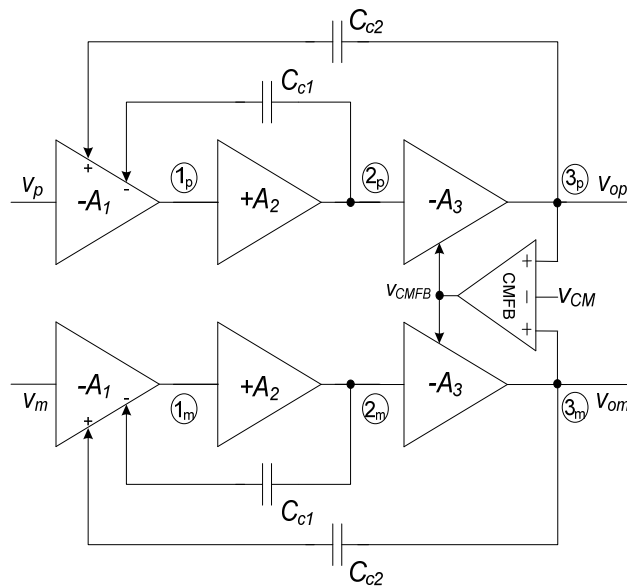
□ Employ CMFB

1. Individually across all the stages.
2. Only across the last two stages as the biasing of the output buffer need not be precise.
3. Only in the third stage (output buffer).

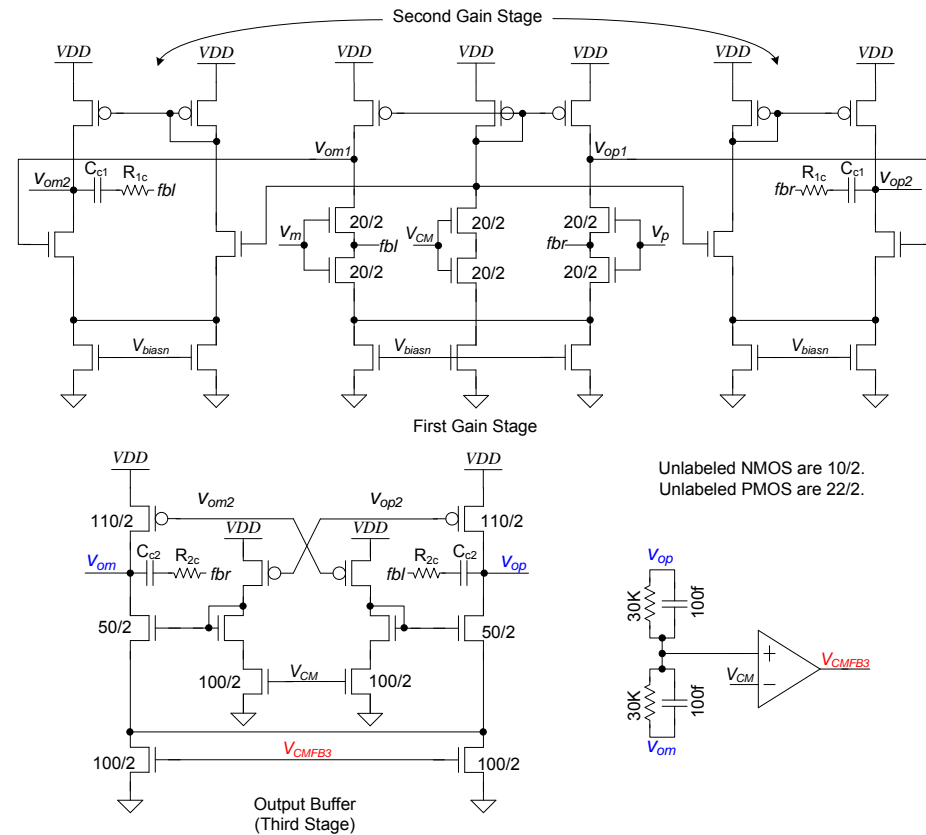


# Three-Stage FD Op-amp Design

Block Diagram

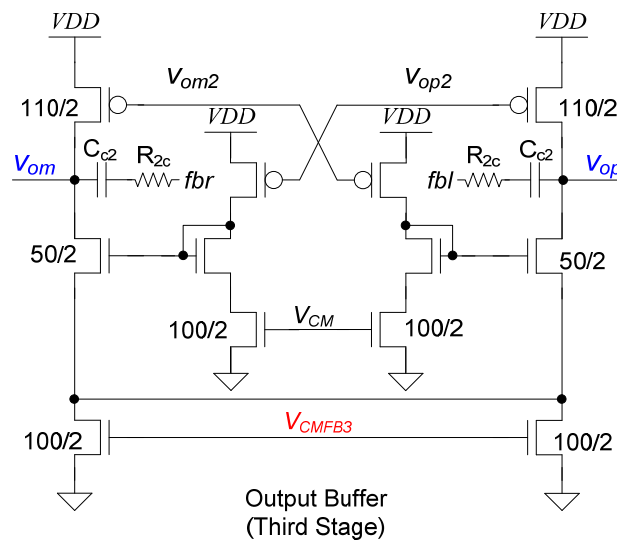
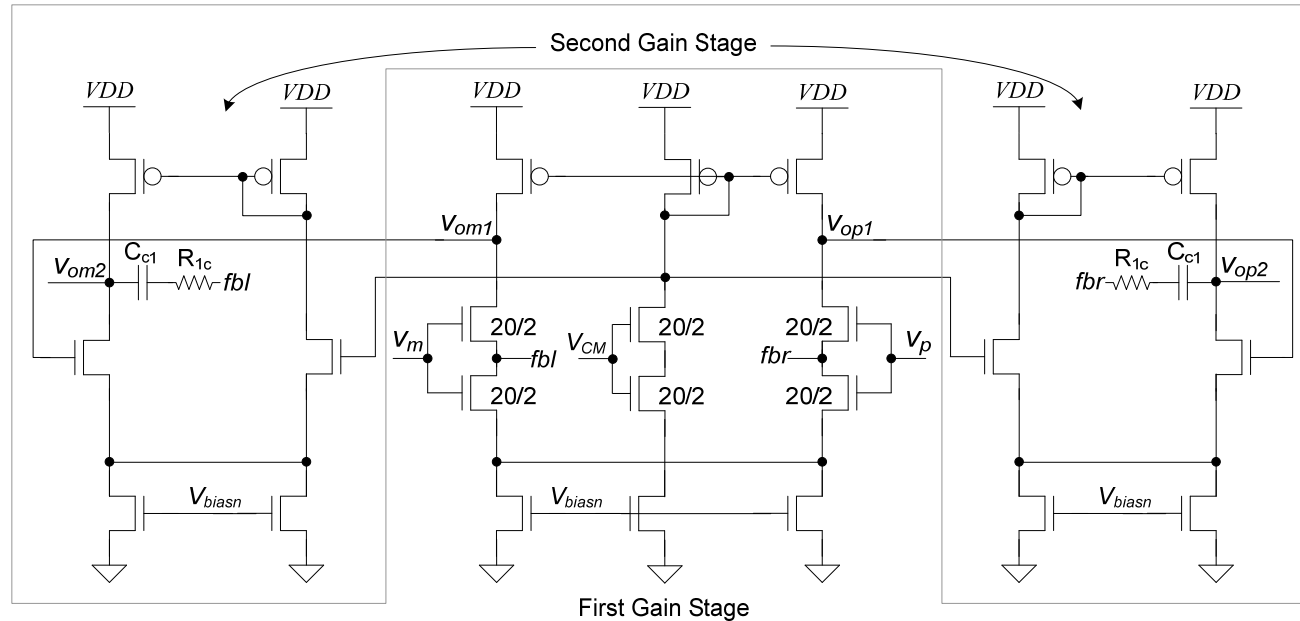


Circuit Implementation

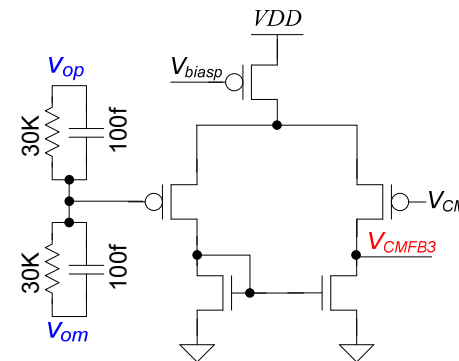


- Use CMFB only in the output (third) stage. → Manufacturable design.
  - ✓ Leaves the biasing of second and third stage alone without disturbing them.
- Employ diff-amp pairs in the second stage for robust biasing.

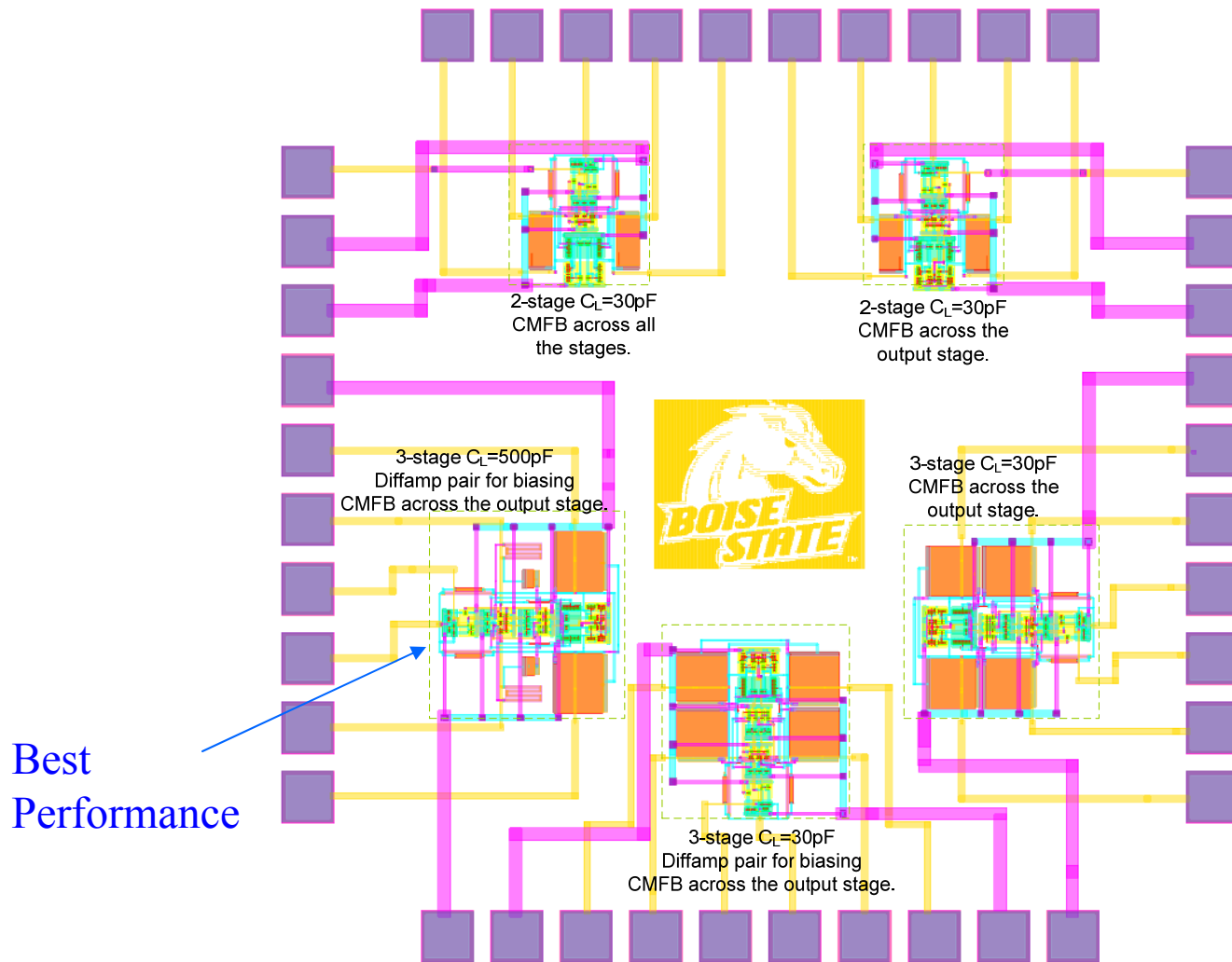
# Three-Stage FD Op-amp: Enlarged



Unlabeled NMOS are 10/2.  
Unlabeled PMOS are 22/2.



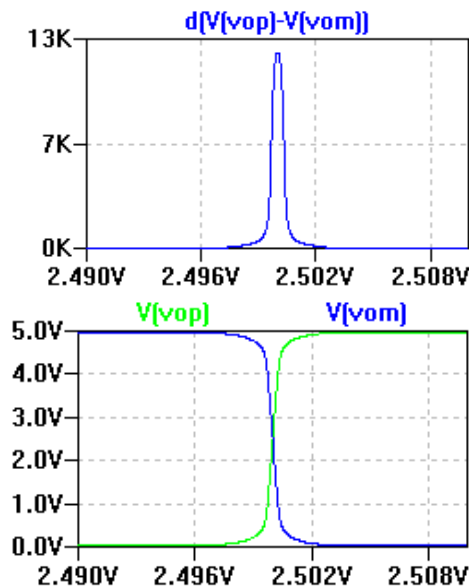
# Chip 3: Low-VDD FD Op-amps



□ AMI C5N 0.5 $\mu m$  CMOS, 1.5mmX1.5mm die size.

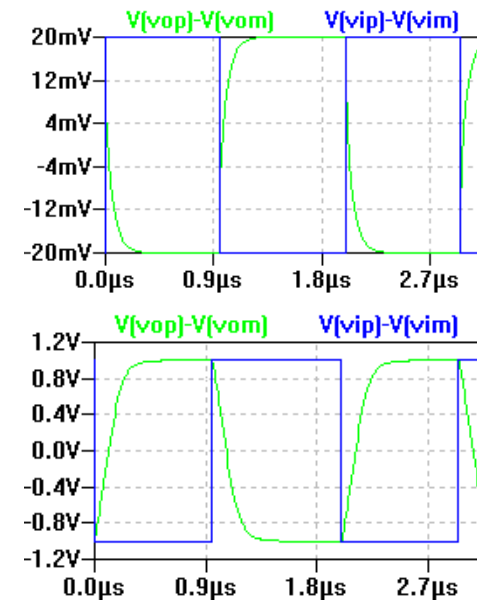
# Simulation and Performance Comparison

DC behavior



82dB gain

Transient response

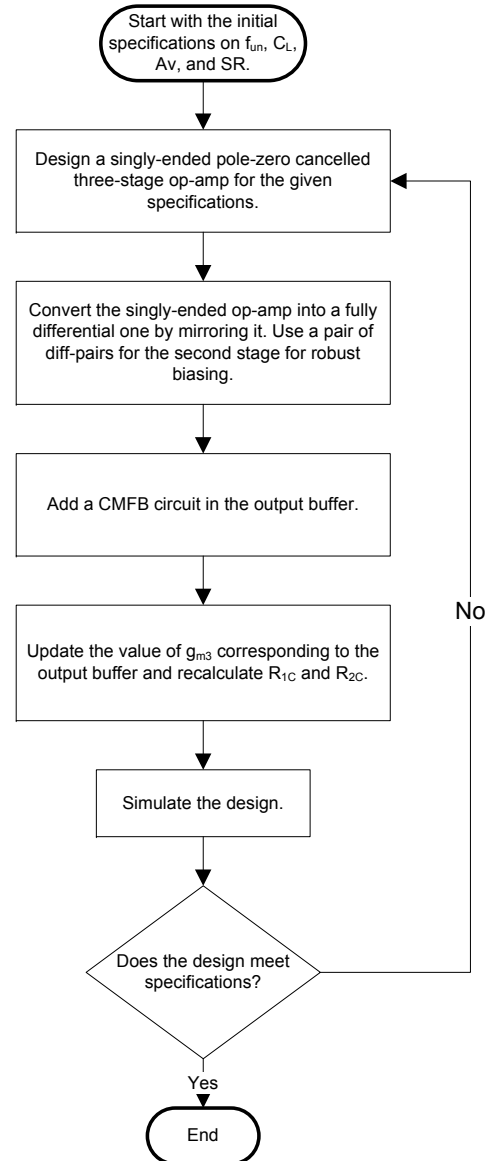


$t_s=275ns$

Topology	$C_L$ (pF)	$V_{DD}$ (V)	$I_{DD}$ (mA)	Power (mW)	$f_{un}$ (MHz)	Avg. SR (V/μs)	$C_{c1}, C_{c2}$ (pF)	$t_s$ (ns)	FoM <sub>S</sub> (MHz.pF/mW)	FoM <sub>L</sub> (V/μs.pF/mW)
Buffered RNMC [19]	100	1.2	0.285	0.342	8.9	5.5	2, 0.65	2400	2602	1608
RNIC-1-FD (This work)	30	3	0.4	1.2	12	10	4, 4	275	300	250
RNIC-2-FD (This work)	500	3	0.4	1.2	20	8	5, 0.2	370	8333	3333

☐  $>2.5X$  figure of merit (FoM).

# Flowchart for Three-Stage FD Op-amp Design



## Conclusions

- ❑ Indirect compensation leads to significantly faster, lower power op-amps with smaller layout area.
- ❑ Indirect compensation using split-length devices facilitates low-VDD op-amp design.
- ❑ Novel pole-zero canceled three-stage RNIC op-amps exhibit substantial improvement over the state-of-the-art.
- ❑ A theory for multi-stage op-amps is presented.
- ❑ New methodologies for designing multi-stage FD op-amps proposed which improve the state-of-the-art.
- ❑ All proposed op-amps are low voltage
  - ✓ Open new avenues for low-VDD mixed signal system design.

## Future Scope

- ❑ Mathematical optimization of PZC op-amps.
- ❑ Design of low-VDD systems in nano-CMOS process
  - ✓ Pipelined and Delta-Sigma data converters,
  - ✓ Analog filters,
  - ✓ Audio drivers, etc.
- ❑ Further investigation into indirect-compensated op-amps for  $n \geq 4$  stages.



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