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# Incorporation of Chopping in Continuous Time K-Delta-1-Sigma Modulator

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***Abstract*—A chopping technique in a continuous time K-delta-1-sigma modulator (KD1S) is reported in this paper. It is shown that the presence of the inherent path filter in the proposed technique can significantly improve the performance of the modulator by minimizing the aliased quantization noise. Also reported are how the selection of chopping frequency and its relation to sampling frequency and the trade-offs. To support the theory, a first order K-delta-1-sigma topology was designed in a 180nm CMOS process. Simulations are used to illustrate the validity of the results. The modulator works at a sampling frequency of 1 MHz with an oversampling ratio of 256. It consumes an average current of 61.18 µA from 1.8 V supply. The simulation result shows that there is more than 25dB improvement in the Signal-to-Noise Ratio (SNR) of the KD1S, when chopped at the right frequency.**

***Keywords — delta-sigma modulator, chopping, SNR, flicker noise, aliasing, oversampling, chopping effects, integrator, FIR DAC***

## I. INTRODUCTION

Continuous time delta sigma modulators (CTDSM) are popular in various low frequency applications mainly due to their inherent anti-aliasing effects and notable energy efficiency. However, the performance of these modulators can get degraded by the presence of flicker noise (1/f noise). Such problems can be easily mitigated in a discrete time version by using the auto zeroing techniques. In the continuous time delta sigma modulators, however, efficient techniques should be employed to decrease the low frequency flicker noise. One of the traditional methods that has been employed was to increase the size of the transistors used in the first stages of the design. The problem with this technique is the resulting increase in layout area. Moreover, increasing the device sizes can also increase the parasitic capacitance and thereby creating additional poles in the system.

Chopper stabilization (chopping) is a popular technique that has been widely used to reduce flicker noise [1-5]. This is achieved by modulating the 1/f noise to higher frequencies and thus out of the signal band. This technique has been successfully implemented in various low frequency-based amplifiers [1,2]. A continuous time delta sigma modulator can also make use of chopping by placing the chopper circuit on the first stage of the op-amp used in the integrator. However, the effects of chopping on a CTDSM are undesirable [4]. Figure 1 illustrates the block diagram of a CTDSM with a sampling frequency of $f_s$ and chopping frequency of $f_{ch}$. It can be observed that the integrator in the CTDSM will process the shaped quantization noise that is fed back from the output. However, because of chopping, the quantization noise from the multiples of $2 * f_{ch}$ will also get aliased (folded-back) into the signal band. This will result in the significant degradation of Signal-to-Noise Ratio (SNR) in the CTDSM as the out of band components are several orders of magnitude larger than those in the signal band. A conventional method that has been employed to mitigate this problem is to chop at the sampling frequency, $f_s$ [3]. The disadvantage with this approach is that chopping at higher frequencies will create parasitic switched capacitor resistance at the chopper circuit. This will result in both reduced DC gain of the op-amp and non-linearities.

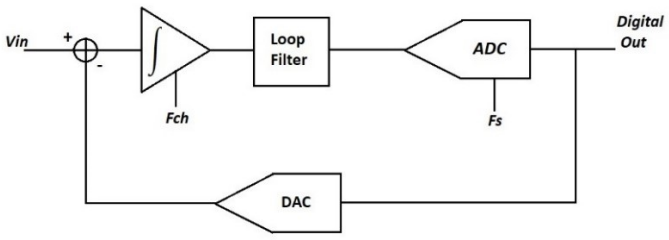


Figure 1: Block diagram of a Delta-Sigma modulator

Several techniques have been introduced in the literature to mitigate the discussed issue [3-5]. The design in [4] makes use of a finite impulse response (FIR) feedback-based DAC to reduce the effect of aliased quantization noise. This is an effective method to tackle the chopping artifacts. Similarly, for the design in [5], the aliased quantization noise is reduced by making use of return-to-zero RZ-DACs and switched capacitor based DACs. This paper discusses the incorporation of chopping in K-delta-1-sigma modulators. The paper is organized as follows. Section II introduces the K-delta-1-sigma modulator (KD1S). Section III discusses chopping in a KD1S modulator. The simulation results are illustrated in section IV and the paper is concluded in section V.

## II. KD1S MODULATOR TOPOLOGY

In order to achieve higher sampling rate in the delta-sigma modulator, several techniques have been implemented. The time interleaving technique is one of the most straightforward methods, where each delta-sigma path is clocked at different

phase of a slower frequency. Thus, an effective sampling rate of $K * f_s$ can be achieved (K is the number of paths). One of the main drawbacks with this technique is that it cannot achieve true noise shaping, where the noise transfer function can be moved all the way to $(K/2) * f_s$. This is because all the paths are mutually exclusive and the feedback signal arrives at the input after a delay of $T_s(1/f_s)$. Moreover, this time interleaving technique will also contribute to higher power consumption and larger layout area. One way to achieve true noise shaping is by feeding back the output after a delay of $T_s$/K. This is achieved by using the K-delta-1-sigma modulator [6]. Figure 2 shows the basic block diagram of the KD1S topology. The topology consists of K paths and one shared integrator. The output of the integrator is shared with comparators that are clocked by K phases of a clock with a sampling rate of $f_s$. In this way, an effective sampling rate of $K * f_s$ can be achieved and the quantization noise can also be pushed to a much higher frequency of $(K/2) * f_s$. The noise transfer function of such topology will be:

$$NTF(f) = 2\sin(\frac{2\pi f}{K*f_s}) \quad (1)$$

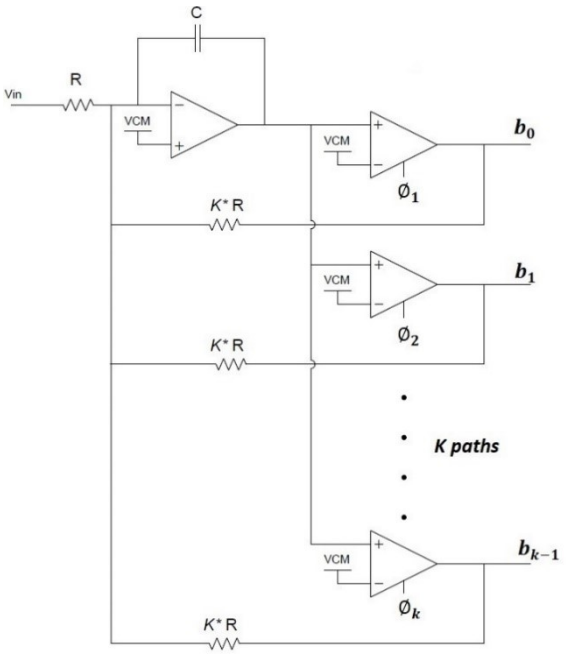


Figure 2: Block diagram of KD1S modulator

One of the main advantages of the KD1S topology is that there is a relaxed bandwidth requirement and lower power consumption. Moreover, the mismatches in each path can be averaged out using the K feedback paths. The offset of the comparators is also less significant because of the integrator gain.

However, there are drawbacks associated with this topology. Since every path is feeding back the signal based on the previous information, it must be ensured that the comparator has minimal delay. Otherwise, there will be distortion contributed to the modulator, ruining the overall performance. There are also stringent requirements on the comparator's clock jitter.

A special feature of this topology is that the combined output of each path will behave as a Sinc filter with a transfer function of [7,8]:

$$H(z) = \frac{1-z^{-K}}{1-z^{-1}} \quad (2)$$

where K is the number of paths. From the above equation, it can be inferred that spectral nulls are present at the integral multiples of $f_{s,eff}/K$. This can be seen on Figure 3. This is an interesting feature that can be utilized while incorporating chopping in KD1S modulators.

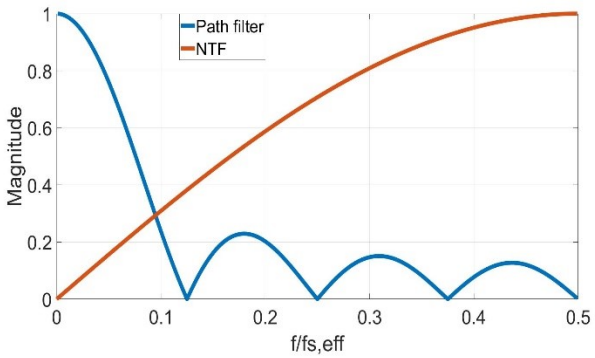


Figure 3: Path filter response of KD1S modulator

## III. Chopping in KD1S Modulator

One of the popular techniques to mitigate the chopping artifacts is to add an FIR DAC in the feedback path of the CTDSM [4]. The FIR filter can be designed appropriately so that the quantization noise at the multiples of $2* f_{ch}$ will fall under the spectral nulls of the filter. For example, an N-tap FIR filter has spectral nulls at the multiples of $f_s/N$. Therefore, if the chopping frequency is set to $f_s/2N$, the aliased quantization noise will be negligible. In this way, one can use a low chopping frequency with minimal effect of aliased quantization noise. Even though this is an effective method, there are a few limitations in this technique. Firstly, the inclusion of the FIR filter can result in the delay of the feedback loop and thus instability. This is fixed in higher order system by adding an extra feedback loop in the system. Second, the layout area of the modulator increases with the increase in the number of taps in the FIR filter.

A KD1S modulator can be used to address these limitations. The presence of an inherent path filter (illustrated in Figure 3) will ensure that no additional FIR feedback is required for this topology. The chopping frequency can be selected appropriately so that the quantization noise can be reduced considerably. For instance, for a K-path KD1S modulator with an effective sampling frequency of $f_{s,eff}$, if the chopping frequency is set to $f_{s,eff}/K$, then the multiples of $2*f_{ch}$ will be at the spectral nulls of the path filter. Therefore, the aliased quantization noise is reduced considerably. Thus, in a chopped

KD1S modulator, a low chopping frequency can be used and a higher effective sampling rate can also be achieved.

Similar to Figure 2, a first order fully differential KD1S modulator has been designed. As previously discussed, there are multiple comparators forming K-paths and one shared integrator. A conventional clocked comparator design is used in each path [8]. It should also be noted that each comparator should be clocked at different phases of the same frequency and thereby achieving the high sampling rate. The clock signals in this topology were generated using a 4-stage non overlapping clock generator [6]. The schematic of the same is portrayed in Figure 4. The values of resistances and capacitances for the integrator are carefully chosen so that the fed back signals can be integrated accurately.

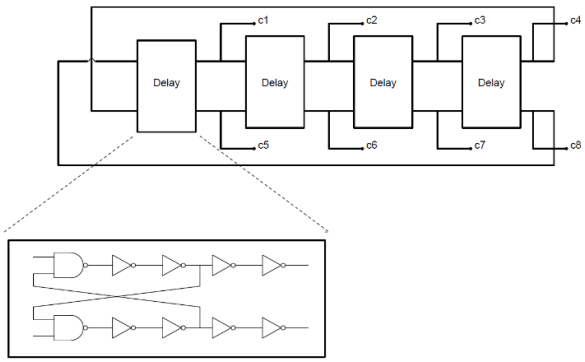


Figure 4: Non-overlapping clock generator

The op-amp for the integrator comprises two stage self-biased differential pair with a DC gain of almost 57 dB. This is illustrated in Figure 5. The chopper circuits were placed at the input and output of the first stage amplifier. The operation of chopping is straightforward where the 1/f noise is up modulated to higher frequencies (out of the signal band).

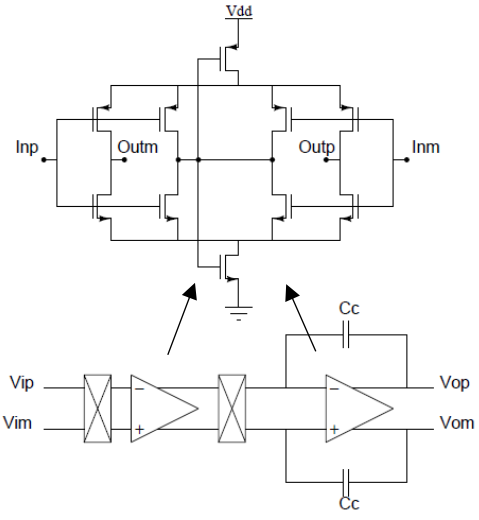


Figure 5: Operational amplifier used in the integrator with the chopper circuits

## IV. Simulated Results

A first order 8-path KD1S modulator was designed in a 180 nm CMOS process. The sampling frequency ($f_s$) in each path is 125 kHz and thus an effective sampling frequency ($f_{s,eff}$) of 1 MHz is achieved. An input signal of 1.7 V peak-to-peak and a frequency of 500 Hz was applied to the modulator.

The SNR of the topology is estimated in a signal bandwidth of 1.9 kHz (oversampling ratio is 256). The output PSD of the KD1S modulator, processed in MATLAB, is illustrated in Figure 6 (1 x $10^5$ points Hanning widow). If chopping is not enabled, the signal-to-noise ratio (SNR) that is achieved for this topology is 34.12 dB (orange trace). However, if the modulator is chopped at the wrong frequency (e.g. $f_{ch}$=50 kHz, $f_{s,eff}$ /20), the modulator will not provide a major improvement. This is also illustrated in Figure 6 (red trace). The SNR value achieved in this case was 35.48 dB. When the chopping frequency is 125 kHz ($f_{s,eff}$/8; realized by $\emptyset_1$ signal), it can be seen that the noise floor is decreased significantly (blue trace). In this way, 64.36 dB SNR is achieved. The SNDR in this case is lower which can be improved in higher order architectures. Nevertheless, this technique validates the idea of chopping at a lower frequency of 125 kHz ($f_{s,eff}$/8).

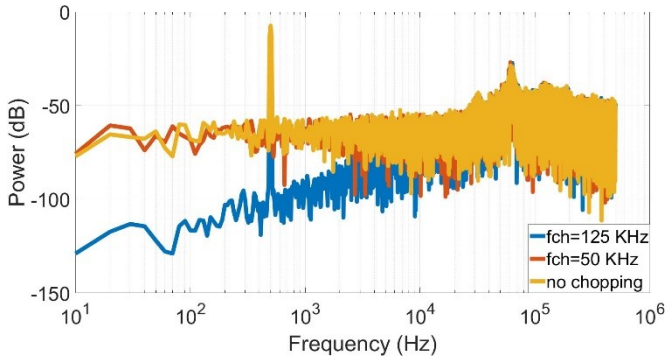


Figure 6: PSD of the KD1S modulator at different chopping frequencies

Figure 7 portrays the dynamic range performance of the KD1S modulator. It should be noted that the signal has an input frequency of 500 Hz and the modulator is chopped at 125 kHz ($f_{s,eff}$/K). The first order 8-path chopped KD1S modulator has a dynamic range of approximately 62.2 dB.

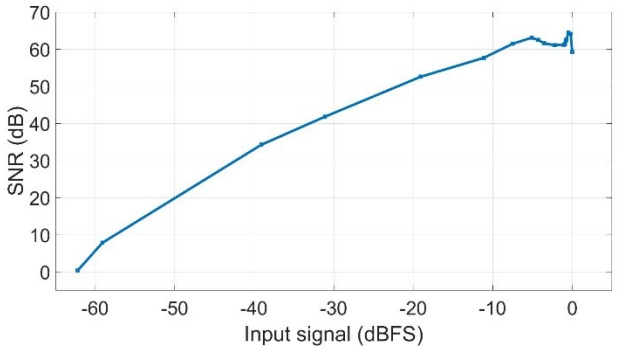


Figure 7: Dynamic range performance of the KD1S modulator

The performance of the KD1S modulator has been further validated by adding offset to the first stage amplifier of the op-amp. Figure 8 shows the SNR of the modulator for different input offset voltages. It can be confirmed that the KD1S modulator's performance is not considerably affected by the offset.

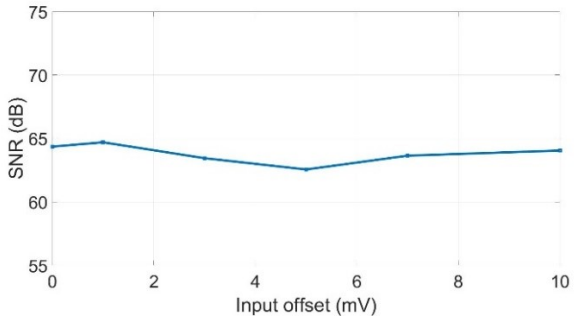


Figure 8: Effect of input offset on the KD1S modulator

From the above discussions, one can infer that the number of paths can be increased significantly for higher performance. However, this can also bring some penalties. As the paths are increased, there will be possible delays in the feedback paths and thus gradually deteriorating the SNR. This is shown in Figure 9. Moreover, increasing paths can also add to the power consumption and layout area. The 8-path KD1S has maximum SNR in this design.

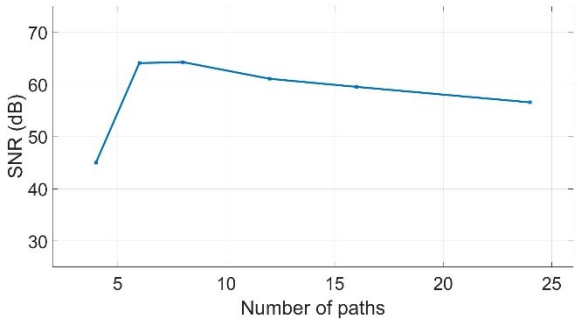


Figure 9: SNR performance for different K paths

## V. Conclusion

This paper discusses the chopping techniques in continuous time delta-sigma modulators. Even though chopping is an effective technique for reducing low frequency noise, its incorporation in delta sigma modulators can result in undesirable effects. Several techniques have been introduced in the literature to rectify this problem. The use of KD1S architecture can provide a feasible solution, where a very low chopping frequency can be used while sampling at a high frequency. It has been inferred that, for a KD1S modulator, if the chopping frequency is set to $f_{s,eff}/K$, the SNR will be improved significantly. The illustrated simulation results validate the theory. The simulated parameters are also summarized in Table I. The proposed technique can be easily expanded to higher order architectures for superior performance.

Table I. Summary of results

| **Parameter** | **Value** | | |
|---|---|---|---|
| Process Technology | 180 nm CMOS | | |
| Supply voltage | 1.8 V | | |
| Number of paths | 8 | | |
| Sampling frequency | 1 MHz | | |
| Bandwidth | 1.98 kHz (OSR=256) | | |
| Power (w/o clock gen) | 110.14 µW | | |
| Dynamic range (DR) | 62.2 dB | | |
| Chopping frequency | **125kHz** | 50kHz | - |
| SNR | **64.36dB** | 35.48dB | 34.12dB |
| SNDR | **47.56dB** | 34.6dB | 33.8dB |
| Walden FOM ($\frac{Power}{DR*f_s}$) | 1.77 pJ/bit | | |
| Schreier FOM ($10\log(\frac{DR^2 f_s}{Power})$) | 135.46 dB | | |

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