Current Comparator with SiGe BiCMOS Input Stage for Photon-Counting LiDAR Applications

Gonzalo Arteaga [1, 3], Sachin P. Namboodiri [1], Angsuman Roy [1, 2], and R. Jacob Baker [1]
[1] Department of Electrical and Computer Engineering, University of Nevada Las Vegas, Las Vegas, NV, USA
[2] Freedom Photonics, LLC, 41 Aero Camino, Santa Barbara, CA, 93117
[3] arteag1@unlv.nevada.edu (corresponding author)

***Abstract*—A current-mode photon-counting circuit is proposed for long-range LiDAR applications to interface with a microchannel plate (MCP) photomultiplier tube (PMT). Based on the idea of a current-mode comparator, the proposed topology combines a BiCMOS regulated cascode current buffer together with a CMOS current comparator. The circuit accepts two input current signals, the photodetector current and a user-adjustable threshold current, and outputs a 1.8-V digital signal depending on the polarity of the difference current. Designed and characterized in a 180-nm SiGe BiCMOS process, the proposed design provides a 50-Ω input impedance up to 2-GHz and can detect 8-uA current pulses with widths of 300-ps FWHM at a count rate of 1-GHz. The solution also offers a low static power consumption of 4.07-mW/channel dissipated from a 2.5-V and 1.8-V dual supply.**

Keywords—readout integrated circuit (ROIC), silicon photomultiplier (SiPM), photon-counting system, photomultiplier tube (PMT), microchannel plate (MCP)

I. Introduction

Photon-counting techniques, made possible by the invention of single-photon-sensitive photodetectors, have greatly expanded the capabilities of low-light imaging technology. This has led to the adoption of photon-counting optical receivers in various fields involving high-energy physics, medical imaging, and LiDAR. In satellite-based LiDAR applications, for example, the ability to detect individual photons allows for the detection of faint laser pulses which travel large distances and are subject to much attenuation as they pass through various aerosols in the atmosphere. Just as important, is the count rate of the detector which impacts the spatial resolution of the resulting distance measurements. Both parameters demonstrate how critical the features of the photodetector are to the overall LiDAR performance. Typical candidates for the photodetector include photomultiplier tubes (PMT) or silicon photomultipliers (SiPM). While the latter provides a compact solution with lower supply voltage requirements, PMTs may be adopted for their lower dark counts and resistance to radiation which is beneficial in satellite-based applications. In either case, the detector should be paired with a readout circuit which best preserves the features of the detector signal to optimize performance.

With the trend towards smaller process technologies, attempts to implement voltage-mode readout circuits have been met with some difficulty. An example described in [1] shows how the use of a charge-sensitive amplifier to read a signal from a SiPM in a deep submicron technology can become impractical due to the tradeoff between a high dynamic range and a high bandwidth. The author's proposed current-mode front-end design, however, did not suffer from the same constraint. Similarly, [2] implements a SiPM readout using a current conveyor as a scalable current buffer to fit the input signal to the dynamic range of its subsequent RC filter as well as achieve a lower input impedance. This highlights some of the potential design benefits to current-mode topologies as an alternative to those which typically feature the use of feedback amplifiers.

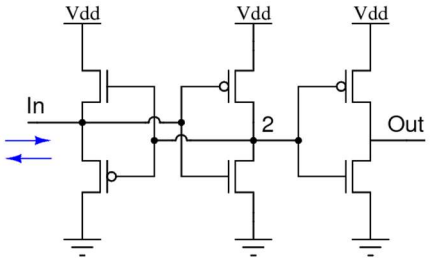

Figure 1: Schematic view of current comparator from [3].

The proposed readout design is based on the use of a current comparator circuit, an example of which is shown in Figure 1 and is reported in [3]. As the name implies, this circuit is a current analogue of the standard voltage comparator. The circuit discriminates between currents of different polarities by outputting a different logic state depending on whether the input current flows into or away from the input terminal. From left to right, the circuit consists of a class-B source follower (SF), a feedback inverter, and an additional output inverter for producing a rail-to-rail digital output. Building on this design, the proposed circuits of [4-5] introduce a class-AB SF to improve the high-frequency performance for small-magnitude input currents by minimizing the dead zone present in the comparator of [3]. While these circuits show promise as high-speed comparators within a readout circuit, a prior buffer stage is required to provide a constant and low input impedance to interface with the photodetector of interest.

In this work, a photon-counting readout circuit for long-range LiDAR applications is proposed. The design consists of a BiCMOS current buffer stage which interfaces with the off-chip

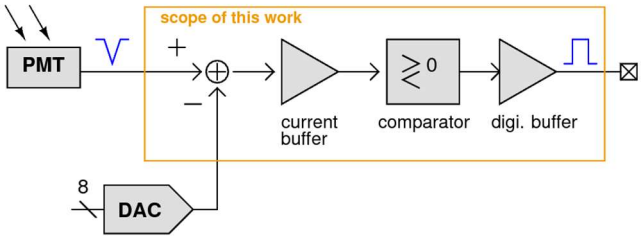

Figure 2: Block diagram of the proposed design.

photodetector, a CMOS current comparator, and a digital output buffer. The design is intended to interface with a microchannel plate PMT (MCP-PMT) which can produce signals with a minimum height of 8-µA with subnanosecond pulse widths. The circuit was designed using a standard, 180-nm SiGe BiCMOS process. Descriptions of the major circuit sections are provided in Section II. The simulated characteristics of the design are presented in Section III. Finally, concluding remarks are presented in Section IV followed by brief acknowledgments in Section V.

II. Circuit Description

A block diagram showing the proposed circuit is provided in Figure 2. The photodetector shares an input terminal with a current DAC which provides an adjustable threshold current for comparison. The two current signals are subtracted from one another, and the resulting difference current is delivered through the current buffer to the current comparator. Subsequent buffers are used to square the pulses and to provide better drive strength.

A. Current Buffer Stage

The current buffer used in the proposed circuit consists of a regulated cascode (RGC) current buffer and is shown in Figure 3 with annotations explicitly showing the currents running through each branch ignoring base currents. This variant of the current buffer makes use of local feedback, provided by a common-emitter amplifier (Q1, M1-M2), to boost the transconductance of the amplifying device (Q2). This also yields a proportional decrease in the input impedance of the circuit as demonstrated by the following

$$Z_{in} \cong \frac{1}{g_{m,Q2}\,(1 + g_{m,Q1}R_o)} \qquad (1.1)$$

where g_m is the transconductance and Ro is the impedance seen at the collector of Q1.

The decrease in the input impedance not only helps minimize the input time constant to preserve the fast characteristics of the input signal, but it also helps with impedance matching, as will be described shortly. Given the fast, rising edges from the photodetector and its connection to the chip, one must consider transmission line effects. To minimize signal reflections, the input impedance of the circuit is matched with that of the interconnecting line, 50-ohms. Another benefit of the low input impedance is the ability for the input node to operate as a current summing junction with minimal disturbance to the biasing of the greater circuit. At this node, the

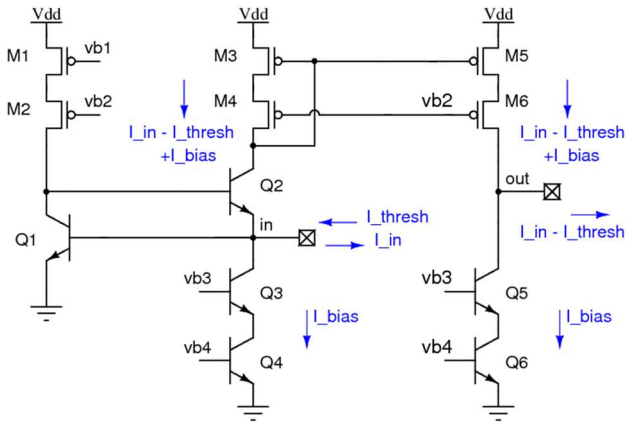

Figure 3: Current buffer stage with annotated currents. A bias of 250-µA was used to bias each of the circuit branches.

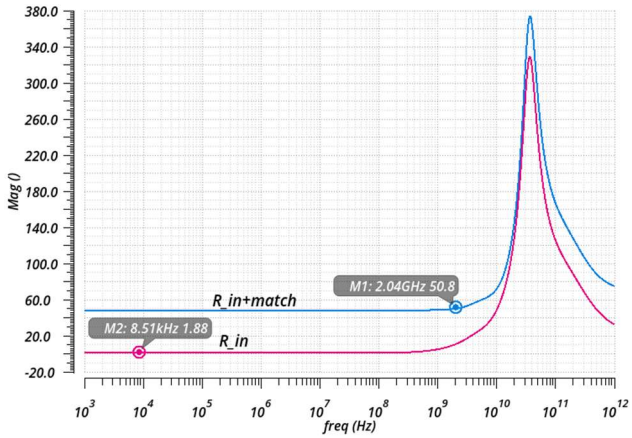

Figure 4: Simulation plot of input impedance.

difference current is formed by having both input currents flow in opposite directions. Since the photodetector steals charge from the input upon detection of a photon, the threshold current is oriented such that it flows into the input terminal.

A plot of the simulated input impedance is shown in Figure 4. The red trace displays the input impedance of the standalone current buffer while the blue trace shows the impedance seen with a 47-ohm matching resistor placed in series with the current buffer. This latter trace shows how the target 50-ohm input impedance is achieved for frequencies up to about 2-Ghz.

The above plot demonstrates a benefit of using a BiCMOS design incorporating SiGe heterojunction bipolar transistors (HBT). Had NMOS transistors been used in their place, the inductive peaking around 40-GHz that occurs because of the local feedback would occur at much earlier frequencies because of their larger capacitances. Additionally, the HBT devices come with the benefit of promoting a radiation-resistant design.

The drawbacks to the BiCMOS design include a larger layout area and the larger voltage overhead requirement that is a result of the substantial base-emitter voltage combined with the RGC buffer topology. The latter of which led to the adoption of a 2.5-V supply voltage for this stage. The base currents of the devices can also produce an error current that manifests at the

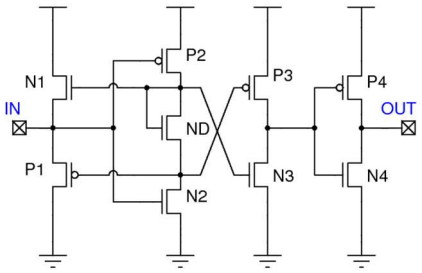

Figure 5: Schematic view of the current comparator.

output of this stage. Because the collector currents of Q1 and Q2 in Figure 3 are similarly biased, the base current of Q2 is re-used for the base current for Q1 in which case there is a negligible error. As the collector currents of the devices differ, however, a small error current will appear.

The load of the current buffer simply consists of a PMOS current mirror which mirrors the difference current over to a high impedance output. By itself, this stage operates as a current mirror comparator like that of [6] with large delays as a result of the large time constant at the output node. Instead, the circuit's output is tied to the low-impedance input of the subsequent current comparator for improved high frequency performance.

B. Current Comparator Stage

The current comparator adopted for this application was introduced in [5] and is shown in Figure 5. The circuit consists of a class-AB SF variant of the comparator from [3]. In this case, the diode-connected device (ND) is used to facilitate the class-AB operation without any additional increase in current draw. As a result of this alteration, both SF devices (N1 and P1) conduct current while idle and the corresponding input impedance of the circuit is described by

$$Zin = \frac{1}{g_{m,N1} + g_{m,P1}} \qquad (1.2)$$

where g_m is the transconductance of the SF devices. The added device minimizes the dead zone in the SF stage which would otherwise be a source of significant delay for the low-level currents one would anticipate in photon-counting applications.

The two outputs of the modified feedback inverter (drains of P2 and N2) are then applied to another inverter which is driven harder to allow for faster charging and discharging of the gate of the final inverter (P4 and N4). For the displayed circuit, currents

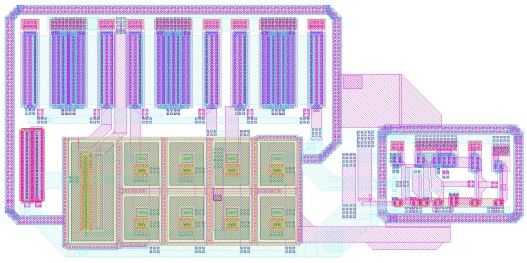

Figure 6: Layout of the proposed circuit not including the output buffer.

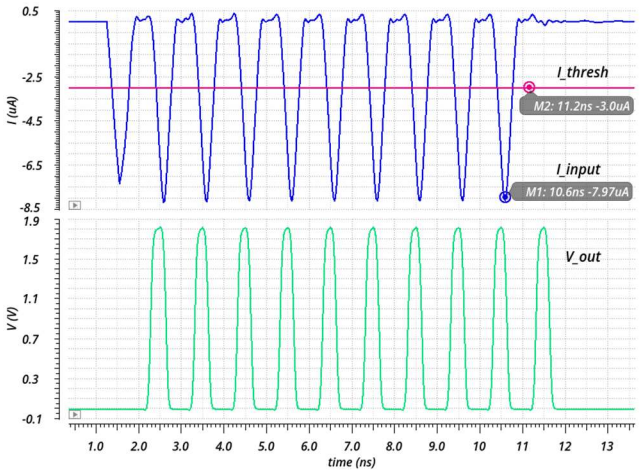

Figure 7: Response to train of 8-uA pulses at 1-GHz.

flowing into the input terminal yield a LOW output voltage, whereas currents flowing away from the input yield a HIGH output voltage. In effect, the circuit operates as a transimpedance stage by operating on the difference current and outputting a corresponding voltage signal.

III. Simulated Performance

The current mode photon-counting circuit was designed and simulated using a 180-nm SiGe BiCMOS process. The layout of a single channel of the design, excluding the digital output buffer, is shown in Figure 6. Most of the layout area consists of the current buffer and its biasing circuit while the small right-most section is comprised of the current comparator. The displayed layout takes up an area of 76-µm x 37-µm.

The circuit was simulated using a proprietary model of the MCP-PMT and its associated interconnect consisting of an ideal current source, a 50-ohm transmission line, and various parasitics specific to the detector. A typical signal anticipated from the detector is shown in Figure 7 where a train of 8-µA, 300-ps FWHM pulses occur at a rate of 1-GHz. With the threshold current set to a value of 3.0-µA the circuit generates distinct, 1.8-V digital output pulses as shown by the bottom output trace. While the threshold current is adjustable via a DAC, the tuneability of the threshold current is limited by the ability to resolve the narrow input pulse. This means placing the threshold current value at roughly half the height of the input pulse. For slower or wider signals this requirement is relaxed.

An important metric for the proposed design is its ability to detect small amplitude pulses immediately following a large input pulse. In practice this can manifest when a highly reflective surface returns a large proportion of the initial laser pulse back to the photodetector. Depending on the strength of the returned pulse this may temporarily "blind" the readout circuit, decreasing the circuit's count rate, and reduce the spatial resolution of the system. In Figure 8, the circuit is subject to a train of alternating 10-µA and 105-µA current pulses at a frequency of 1-GHz. Each current pulse again has a width of 300-ps FWHM. With the threshold current set to 3.5-µA, the circuit is still able to support the max count rate.

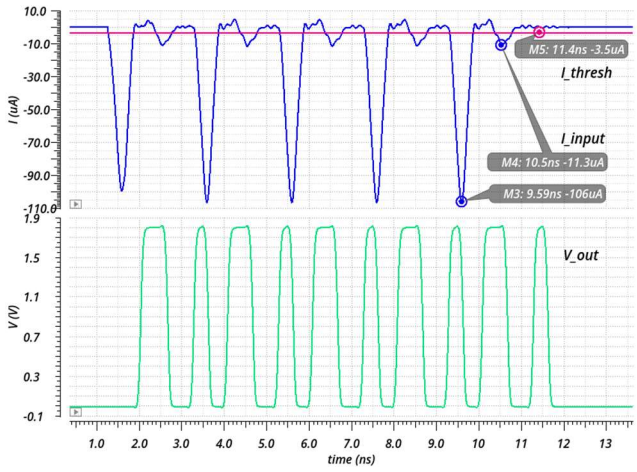

Figure 8: Response to alternating train of 10-uA and 105-uA pulses at 1-GHz.

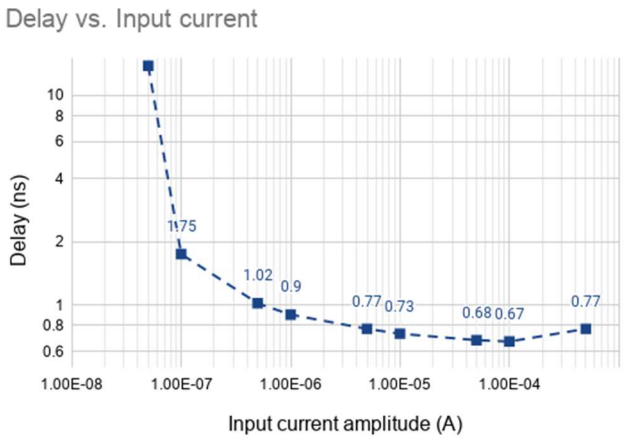

Figure 9: Plot of delay time as a function of input current amplitude.

The delay versus current amplitude plot of the proposed circuit is shown in Figure 9. To determine the relationship between the two parameters, a square current pulse centered about the switching point of the circuit was applied and the time difference between the input and output traces was measured at 50% of their final value. The values displayed in the plot include the delay through a four-stage output buffer which was designed to drive loads up to 10-pF. As seen in the plot, the delay is expected to be no more than about 900-ps for any anticipated pulse height from the photodetector assuming proper selection of a threshold current value.

A summary of the characteristics of the proposed design is presented in Table I. Shown in the table, and not yet addressed, is the power consumption of the circuit which has a value of 4.07-mW/channel during static conditions. Most of the power consumption comes from the current buffer stage and its biasing circuit. In dynamic conditions, the power demands from the output buffer will start becoming more significant with increases in the count rate. Future iterations of the proposed design will not require such a large output buffer and will instead route to a low voltage differential signaling (LVDS) driver for off-board processing.

IV. Conclusion

A current-mode photon-counting circuit was designed and characterized in a standard 180-nm, SiGe BiCMOS process. The circuit features a BiCMOS current buffer, incorporating SiGe HBTs devices, that complements a CMOS current comparator to provide a low input impedance suitable for interfacing with an off-chip photodetector and preserving the fast edges of the input signal. The simulation results, summarized in Table I, demonstrate the circuit's ability to detect single-photon-level pulses (8-µA amplitude, 300-ps FWHM) from the MCP-PMT detector at a 1-GHz count rate. Future developments will include testing the fabricated circuit to experimentally validate the performance of the proposed design.

TABLE I. Summary of Results

Parameter	Value	Units
Process	180-nm SiGe BiCMOS	—
Input Impedance (w/ Rmatch)	50 (up to 2-GHz)	Ω
Supply Voltages	2.5 (current buffer)	V
	1.8 (all else)	V
Input Current Offset	0.2	µA
Static Power Consumption	4.07	mW/ch
Max. Count Rate	1.0	GHz
Prop. Delay (@ 1-µA amplitude)	0.9	ns
Layout area	76 x 37 (w/out buffer)	µm2
	103 x 43 (o/p buffer only)	µm2

Acknowledgments

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