

**UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION**

Vervain, LLC,

Plaintiff,

v.

SK hynix Inc., SK hynix America, Inc.,
SK hynix NAND Product Solutions Corp. (d/b/a
Solidigm), and Solidigm Inc.

Defendants.

Civil Action No. 1:26-cv-259

JURY TRIAL DEMANDED

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Vervain, LLC (“Vervain”) asserts the following claims for patent infringement against Defendants SK hynix, Inc., SK hynix America, Inc., SK hynix NAND Product Solutions Corp. (d/b/a Solidigm), and Solidigm Inc. (collectively “Defendants” or “SK”), and alleges as follows.

NATURE OF THE ACTION

1. This is a civil action for infringement under the patent laws of the United States of America, 35 U.S.C. § 1 *et seq.*

2. Vervain is the owner of all rights, title, and interest in U.S. Patent Nos. 8,891,298; 9,196,385; 9,997,240; 10,950,300; 11,830,546; 12,119,054; and 12,224,005 (collectively, the “Asserted Patents”).

3. Defendants have infringed and continue to infringe one or more claims of Vervain’s Asserted Patents by making, using, offering to sell, and/or selling within the United States, and/or importing into the United States, including in this District, certain flash memory products. Vervain seeks injunctive relief and monetary damages.

THE PARTIES

4. Plaintiff Vervain is a Texas limited liability company with its principal place of business located at 1317 Shetland Road, Plano, Texas 75093.

5. On information and belief, Defendant SK hynix Inc. is a corporation organized and existing under the laws of the Republic of Korea, having a principal place of business at 2091, Gyeongchung-daero, Bubal-eup, Icheon-si, Gyeonggi-do, 17336, Korea. On information and belief, SK hynix Inc. is the worldwide parent corporation for Defendant SK hynix America Inc., and is responsible, either directly or indirectly through its subsidiaries, for its infringing activities.

6. On information and belief, Defendant SK hynix America Inc. is a corporation organized and existing under the laws of California, with its principal place of business at 3101 North First Street, San Jose, California 95134. Defendant SK hynix America Inc. can be served at the address for its agent for service, The Prentice-Hall Corporation System, 211 E. 7th Street, Suite 620, Austin, Texas 78701.

7. On information and belief, Defendant SK hynix NAND Product Solutions Corp., doing business as Solidigm, is a corporation organized under the laws of Delaware, with its principal place of business at 10951 White Rock Road, Rancho Cordova, California 95670. Defendant Solidigm can be served at the address for its agent for service, CT Corporation System, 1999 Bryan St., Ste. 900, Dallas, Texas 75201-3136.

8. On information and belief, Defendant Solidigm Inc. is a corporation organized under the laws of Delaware, with its principal place of business at 10951 White Rock Road, Rancho Cordova, California 95670. Defendant Solidigm Inc. can be served at the address for its agent for service, CT Corporation System, 1999 Bryan St., Ste. 900, Dallas, Texas 75201-3136. On information and belief, the recently established Solidigm Inc is an SK subsidiary to which all

of SK hynix NAND Product Solutions Corp.’s existing business operations will be transferred.¹ Accordingly, Defendants SK hynix NAND Product Solutions Corp. and Solidigm Inc. will be referred to collectively as “Solidigm.”

9. SK is “the world’s top tier semiconductor supplier offering Dynamic Random Access Memory chips (‘DRAM’) and flash memory chips (‘NAND flash’) for a wide range of distinguished customers globally.”² SK is “the second-largest DRAM and NAND supplier globally with a 33% and 21% market share, respectively, as of 2024.”³ It has been ranked as the second largest company in Korea by market capital.⁴

10. SK sells a variety of flash memory products, including solid state drives (SSDs)⁵ and embedded flash products like eMMC and UFS.⁶ SK touts its SSDs’ speed, efficiency, and reliability.⁷ To achieve this performance, SK uses a variety of flash memory controllers, including its own proprietary controller designs, and controllers sourced from third parties, including Silicon Motion Technology Corporation (“Silicon Motion”) and PHISON Electronics Corporation (“Phison”). These flash memory controllers manage the storage of data on SK’s devices in a reliable, efficient way.

11. One of the key ways that SK’s flash memory controllers manage the storage of data is through the use of SLC and MLC flash. SK touts the benefits of its hybrid MLC and SLC systems, noting that “enabl[ing] some of the cells—the storage areas of NAND—to operate as

¹ Ex. RRR, <https://news.skhynix.com/sk-hynix-launches-ai-company-focusing-on-ai-solutions/>.

² Ex. H, <https://news.skhynix.com/sk-hynix-presents-next-generation-nand-storage-product-strategy-at-ocp-2025/>.

³ Ex. I, <https://www.alpha-sense.com/earnings/000660.kr>.

⁴ Ex. J, <https://news.skhynix.com/corporate/fact-sheet/>.

⁵ Ex. K, <https://product.skhynix.com/products/ssd/ssd.go>; Ex. L, <https://www.solidigm.com/products/data-center.html>.

⁶ Ex. M, <https://product.skhynix.com/products/nand/nand.go>.

⁷ Ex. N, <https://product.skhynix.com/products/ssd/essd.go>.

SLCs with fast processing speeds ... allows selected data to be quickly read and written, speeding up the operation of AI services and general PC operations.”⁸

12. SK has over \$45 billion in annual revenue, and over 46,000 employees worldwide.⁹

13. SK sells its storage products not only to end users and customers throughout the U.S., but also to major computer and electronics manufacturers—including Apple, Dell, and Lenovo—to provide the storage that manufacturers need for their products.¹⁰

14. SK operates and owns the product.skhynix.com, ssd.skhynix.com, and solidigm.com websites, and markets, offers, distributes, and provides technical support for its flash memory products throughout the United States, including in this District.

15. SK develops, designs, manufactures, distributes, markets, offers to sell, or sells infringing products or services within the United States, including in this District, and otherwise purposefully directs infringing activities to this District in connection with its Austin, Texas sales staff, its skhynix.com website, and its other places of business in Texas and the rest of the United States.

16. SK has employees in the state of Texas and this District—for example, Karthikeyan Rajendran, a Senior Technical Account Manager based in Austin, Texas. Mr. Rajendran represents that his “mission is to enable SK hynix to gain market share by aligning its products to Dell Technologies’ needs technically and strategically.”¹¹ On information and belief, SK directs Mr.

⁸ Ex. O, <https://news.skhynix.com/sk-hynix-unveils-highest-performing-ssd-for-ai-pcs-at-nvidia-gtc-2024/>.

⁹ Ex. J, <https://news.skhynix.com/corporate/fact-sheet/>.

¹⁰ Ex. P, <https://wccftch.com/apple-iphone-17-dram-and-nand-supply-chain-increased-to-four-companies/>; Ex. Q, <https://lenovopartsstore.com/products/5ss0v26439>; Ex. R, https://i.dell.com/sites/csdocuments/Corporate_corp-Comm_Documents/en/dell-suppliers.pdf.

¹¹ Ex. S, <https://www.linkedin.com/in/msrkarthikeyan>.

Rajendran to work in the Western District of Texas in order to serve SK's local customers in the Austin area, particularly Dell Technologies.

17. SK has maintained an office at 4201 West Parmer Lane Bldg. B, Suite 245, Austin, in the Western District of Texas,¹² and filed tax returns for its property in Texas.¹³ In prior litigation, SK has represented that its Austin employees are “involved in sales of memory products.”¹⁴

18. SK subsidiary Solidigm also has employees in the state of Texas and this District—for example Michael Hanson, Solidigm's Chief Information Security Officer based in Austin Texas.¹⁵ On information and belief, SK directs Mr. Hanson to work in the Western District of Texas in order to serve SK's local customers in the Austin area.

19. Defendants have been and are acting in concert, and are otherwise liable jointly, severally, or otherwise for relief related to or arising out of the same transaction, occurrence, or series of transactions or occurrences related to the making, using, selling, offering for sale, or otherwise distributing flash memory products in this District.

20. In addition, this action involves questions of law and fact that are common to all Defendants. For example, Defendants are making, using, offering for sale, selling, or otherwise distributing at least some of the same flash memory products in this District.

¹² SK's website also lists an Austin sales office address at 10801-1, 3rd Fl., Suite 300, N. MoPac Expressway, Austin, Texas 78759. Ex. T, www.skynix.com/company/UI-FR-CP06.

¹³ Ex. U, *Netlist, Inc. v. SK hynix Inc. and SK hynix America Inc.*, case No. 6:20-cv-00525-ADA, Docket No. 17; Exs. V and W, *Netlist, Inc. v. SK hynix Inc. and SK hynix America Inc.*, case No. 6:20-cv-00194-ADA, Docket Nos. 26-2, and 87.

¹⁴ Ex. V, *Netlist, Inc. v. SK hynix Inc. and SK hynix America Inc.*, case No. 6:20-cv-00194-ADA, Docket No. 26-2.

¹⁵ Ex. X, <https://www.linkedin.com/in/michael-hanson-85332623/>.

JURISDICTION AND VENUE

21. This is a civil action for patent infringement arising under the patent laws of the United States, 35 U.S.C. § 1 *et seq.* This Court has subject matter jurisdiction over the matters asserted in this Complaint under 28 U.S.C. §§ 1331 and 1338(a) and 35 U.S.C. §§ 271 *et seq.*

22. This Court has personal jurisdiction over SK in accordance with the Due Process Clause of the United States Constitution and the Texas Long Arm Statute (*see* Tex. Civ. Prac. & Rem. Code §§17.041 *et seq.*) because, among other things, (i) SK has done and continues to do business in Texas, (ii) SK “recruits Texas residents, directly or through an intermediary located in this state, for employment inside or outside this state,” Tex. Civ. Prac. & Rem. Code § 17.042(3), and (iii) SK has committed and continues to commit, directly or through intermediaries (including subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others), acts of patent infringement in this State and this District. Such acts of infringement include making, using, offering to sell, selling, and/or importing Accused Products in this State and this District. SK places its Accused Products into the stream of commerce through established distribution channels with the expectation and intent that such products will be sold to and purchased by consumers in the United States, this State, and this District; and with the knowledge and expectation that such products (whether in standalone form or as integrated in downstream products) will be imported into the United States, this State, and this District.

23. SK, directly and through agents, regularly conducts, solicits, and transacts business in this District and elsewhere in Texas, including through its skhynix.com and solidigm.com websites. For example, Defendants employ sales and marketing employees that regularly offer to sell, sell, or otherwise distribute flash memory products in this District and elsewhere in Texas.

24. In particular, SK has committed and continues to commit acts of infringement in violation of 35 U.S.C. § 271, and has made, used, marketed, distributed, offered for sale, and sold

infringing products in Texas, including in this District, and engaged in infringing conduct within and directed at or from this District. The infringing flash memory products have been and continue to be distributed to and used in this District. SK's acts cause injury to Vervain, including injury suffered within this District.

25. Venue is proper in this District under 28 U.S.C. §§ 1391 and 1400(b) because a substantial part of the events or omissions giving rise to the claims occurred in this District, and because Defendants have committed acts of infringement in this District and have a regular and established place of business in this District.

26. In particular, Defendants have regular and established places of business in this District located at the workplaces of Karthikeyan Rajendran¹⁶ and Michael Hanson,¹⁷ and at their offices located at 4201 West Parmer Lane Bldg. B, Suite 245, Austin, Texas and/or 10801-1, 3rd Fl., Suite 300, N. MoPac Expressway, Austin, Texas. Furthermore, Defendants are registered to do business in Texas. Upon information and belief, Defendants instruct Mr. Rajendran, Mr. Hanson and others to work in the Western District of Texas—including at their offices located at 4201 West Parmer Lane Bldg. B, Suite 245, Austin, Texas and/or 10801-1, 3rd Fl., Suite 300, N. MoPac Expressway, Austin, Texas—so that they can easily meet with customers such as Dell Technologies to provide sales, support information, and SK products.

27. Upon information and belief, SK hynix America Inc. and Solidigm are wholly-owned subsidiaries of SK hynix, Inc.

¹⁶ As discussed above, Mr. Rajendran represents SK in the Austin area to interface with Dell Technologies.

¹⁷ As discussed above, Mr. Hanson is Solidigm's Chief Information Security Officer and is based in Austin.

RELATED CASES

28. This case is related to two cases within this District presently before Judge Alan D. Albright—*Vervain, LLC v. Phison Electronics Corporation*, 1:24-cv-00259-ADA, and *Vervain, LLC v. Kingston Technology Company, Inc., et al.*, 1:24-cv-000254-ADA—as well as two closed cases that were previously before Judge Albright—*Vervain, LLC v. Micron Technology, Inc., et al.*, 6:21-cv-00487-ADA, and *Vervain, LLC v. Western Digital Corp.*, 6:21-cv-00488. Many of the patents asserted in this complaint are presently asserted in both the *Phison* and *Kingston* matters and were previously asserted in the *Micron* and *Western Digital* matters. Additional patents asserted in this complaint are recently issued members of the same patent family, which concern the same field of flash memory devices, and which are terminally disclaimed relative to the other asserted patents.

VERVAIN'S ASSERTED PATENTS

29. U.S. Patent No. 8,891,298 (“the ’298 patent”) is entitled “Lifetime Mixed Level Non-Volatile Memory System” and issued on November 18, 2014. A true and correct copy of the ’298 patent is attached as Exhibit A to this Complaint. Vervain is the owner of all rights, title, and interest in and to the ’298 patent, with the full and exclusive right to bring suit to enforce the ’298 patent, including the right to recover for past infringement. The ’298 patent is valid and enforceable under United States patent laws.

30. U.S. Patent No. 9,196,385 (“the ’385 patent”) is entitled “Lifetime Mixed Level Non-Volatile Memory System” and issued on November 24, 2015. A true and correct copy of the ’385 patent is attached as Exhibit B to this Complaint. Vervain is the owner of all rights, title, and interest in and to the ’385 patent, with the full and exclusive right to bring suit to enforce the ’385 patent, including the right to recover for past infringement. The ’385 patent is valid and enforceable under United States patent laws.

31. U.S. Patent No. 9,997,240 (“the ’240 patent”) is entitled “Lifetime Mixed Level Non-Volatile Memory System” and issued on June 12, 2018. A true and correct copy of the ’240 patent is attached as Exhibit C to this Complaint. Vervain is the owner of all rights, title, and interest in and to the ’240 patent, with the full and exclusive right to bring suit to enforce the ’240 patent, including the right to recover for past infringement. The ’240 patent is valid and enforceable under United States patent laws.

32. U.S. Patent No. 10,950,300 (“the ’300 patent”) is entitled “Lifetime Mixed Level Non-Volatile Memory System” and issued on March 16, 2021. A true and correct copy of the ’300 patent is attached as Exhibit D to this Complaint. Vervain is the owner of all rights, title, and interest in and to the ’300 patent, with the full and exclusive right to bring suit to enforce the ’300 patent, including the right to recover for past infringement. The ’300 patent is valid and enforceable under United States patent laws.

33. U.S. Patent No. 11,830,546 (“the ’546 patent”) is entitled “Lifetime Mixed Level Non-Volatile Memory System” and issued on November 28, 2023. A true and correct copy of the ’546 patent is attached as Exhibit E to this Complaint. Vervain is the owner of all rights, title, and interest in and to the ’546 patent, with the full and exclusive right to bring suit to enforce the ’546 patent, including the right to recover for past infringement. The ’546 patent is valid and enforceable under United States patent laws.

34. U.S. Patent No. 12,119,054 (“the ’054 patent”) is entitled “Lifetime Mixed Level Non-Volatile Memory System” and issued on October 15, 2024. A true and correct copy of the ’054 patent is attached as Exhibit F to this Complaint. Vervain is the owner of all rights, title, and interest in and to the ’054 patent, with the full and exclusive right to bring suit to enforce the ’054

patent, including the right to recover for past infringement. The '054 patent is valid and enforceable under United States patent laws.

35. U.S. Patent No. 12,224,005 (“the '005 patent”) is entitled “Lifetime Mixed Level Non-Volatile Memory System” and issued on February 11, 2025. A true and correct copy of the '005 patent is attached as Exhibit G to this Complaint. Vervain is the owner of all rights, title, and interest in and to the '005 patent, with the full and exclusive right to bring suit to enforce the '005 patent, including the right to recover for past infringement. The '005 patent is valid and enforceable under United States patent laws.

36. G.R. Mohan Rao is the sole inventor of the Asserted Patents.

37. Dr. Rao is the named inventor listed on approximately 113 U.S. patents and the author of at least 15 technical publications spanning several decades.

38. Dr. Rao has been an innovator in the semiconductor industry since the 1960s. After receiving his first Ph.D. in physics with a specialization in electronics in September 1968 from Andhra University in Waltair, India, near the village where he grew up, Dr. Rao traveled to the United States to attend a graduate program in physics at the University of Cincinnati, fulfilling his lifelong dream to study in the United States.

39. Shortly after beginning his studies at the University of Cincinnati, Dr. Rao found a bulletin indicating that Prof. William Carr of Southern Methodist University (SMU) was looking for a graduate assistant for his work on MOS transistors. Dr. Rao called Prof. Carr about the opportunity, and by December 1968, after completing the fall semester at the University of Cincinnati, Dr. Rao had received the assistantship with Prof. Carr and moved to Dallas, Texas. Following the transfer to SMU, Dr. Rao earned a Ph.D. in Electrical Engineering.

40. At the laboratory at SMU, Dr. Rao was able to build MOS devices from scratch. In the 1969-1970 timespan, while attending SMU, Dr. Rao also worked in the SMU laboratory with Jack Kilby of Texas Instruments, a pioneering electrical engineer who would later receive a Nobel Prize for his work. In early 1972, Mr. Kilby set up an interview for Dr. Rao at Texas Instruments' Houston facility, then the home of Texas Instruments' MOS-related work.

41. Dr. Rao began working for Texas Instruments in June 1972. He would go on to work for the company for 22 years, until 1994. Dr. Rao rose through the ranks at Texas Instruments, starting in an Engineer position and ascending to the position of Senior Fellow—one of 12 Senior Fellows out of approximately 20,000 engineers at the company at the time. He then moved into a management position, starting as a Vice President in 1983 and becoming a Senior Vice President in 1985.

42. Dr. Rao received his first patent while working in a process and product engineering capacity to solve a production problem with Texas Instruments' 4-kilobit RAM product. From the late 1970s through the mid-1980s, he worked on and/or managed the following products at Texas Instruments: (1) 64 kilobit (kb) RAM, in a project management capacity as a Senior Member of Technical Staff; (2) 256 kb RAM, in a project management capacity as a Fellow; (3) 1 megabit (Mb) RAM, in a management capacity as a Senior Fellow, overseeing several projects; and (4) 4 Mb RAM, in a management capacity as a Senior Fellow, overseeing several projects. At Texas Instruments, Dr. Rao also worked on projects involving EEPROM, SRAM, and microcontrollers. In total, Dr. Rao received approximately 35 U.S. patents during his time at Texas Instruments.

43. Some of Dr. Rao's work for Texas Instruments is featured in the Smithsonian Institution, in the Texas Instruments Collection. For example, the Smithsonian Institution has a

display of Texas Instruments' experimental 1 Mb CMOS DRAM with one-micron feature size, produced in April 1985 under Dr. Rao's leadership.¹⁸

44. After his time at Texas Instruments, Dr. Rao joined Cirrus Logic in 1994. Although Cirrus Logic was a California company, Dr. Rao coordinated a team in the Dallas area. His work focused on a major project involving integration of a graphics controller and memory. During his time at Cirrus Logic, Dr. Rao received approximately 22 U.S. patents relating to his work on integrated graphics controllers and memory. Dr. Rao left Cirrus Logic in the summer of 1996.

45. Later in 1996, Dr. Rao started a company called Silicon Aquarius. Through a relationship between Silicon Aquarius and Matsushita, Dr. Rao led a design team in working on a 256 Mb DRAM chip.

46. After Silicon Aquarius ceased operations, Dr. Rao did consulting work for a number of different companies and devoted much of his free time to thinking about various challenges and problems with which the semiconductor industry had struggled for years. For example, Dr. Rao worked to improve non-volatile memories that are used for long term storage of data after the power is turned off, and how to reduce the power consumption of those devices.

47. In non-volatile memories, there are two types of storage cells: single-level cells (SLCs) that store one bit of information, and multi-level cells (MLCs) that store multiple bits of information. SLCs are faster, more reliable, and have a longer life. MLCs are less expensive and can store more data in less space with less power consumption. While working to improve these non-volatile memories, Dr. Rao developed inventions that combine the long life and high-performance of SLCs with the more cost-effective MLCs. The result is the best of both types of cells – longer life and better performance at less cost. By using the MLCs as the default storage,

¹⁸ Ex. Y, https://americanhistory.si.edu/collections/object/nmah_689635.

the cheaper, more reliable MLCs are used for the bulk of the data storage. Meanwhile, the SLCs are used for the data that needs it the most.

48. The claims of the Asserted Patents are directed to patent-eligible, non-abstract ideas. They address, among other things, specific improvements for controlling non-volatile memory modules. The claims are particularly useful for flash memory products or other memory devices that use a combination of SLCs and MLCs. If, for example, a range of addresses in a MLC memory module fails a data integrity test, the range of addresses may be mapped to a new range of addresses in a SLC memory module. Also, if a block in the MLC module is used frequently, the block may be transferred to the SLC module. By doing so, the reliability and life of the flash memory is increased.

49. Vervain's Asserted Patents claim, among other things, a specific implementation of a solution to a problem in the design and fabrication of flash memories. For example, the patents identify numerous specific advantages that Vervain's claimed techniques provide compared to traditional forms of flash memories. *See, e.g.*, Ex. A, '298 patent at 1:25-32; Ex. B, '385 patent at 1:28-35; Ex. C, '240 patent at 1:40-47; Ex. D, '300 patent at 1:44-51; Ex. E, '546 patent at 1:35-42; Ex. F, '054 patent at 1:51-58; Ex. G, '005 patent at 1:58-65. Further, the claimed technologies cannot be performed as mental steps by a human, nor do they represent the application of a generic computer to any well-known method of organizing human behavior.

50. The Asserted Patents claim inventive concepts that are significantly more than any patent-ineligible, abstract idea. In particular, the claimed technologies, including individual limitations as well as ordered combinations of limitations, were not well-understood, routine, or conventional, and cover multiple advantages, and combinations of advantages, that were not well-understood, routine, or conventional. *See, e.g.*, Ex. A, '298 patent at 5:24-40, 6:24-35; Ex. B, '385

patent at 5:28-44, 6:28-39; Ex. C, '240 patent at 5:43-59, 6:46-58; Ex. D, '300 patent at 5:51-67, 6:53-65; Ex. E, '546 patent at 5:41-57, 6:44-56; Ex. F, '054 patent at 5:51-67, 6:53-65; Ex. G, '005 patent at 5:51-67, 6:53-65.

SK'S INFRINGING PRODUCTS AND ACTIVITIES

51. SK is a global manufacturer and supplier of memory products, including non-volatile memory products. SK's flash memory products, such as solid state drives (SSDs)¹⁹ and embedded flash products like eMMC and UFS,²⁰ are managed by a controller chip. Certain ones of SK's controllers are made by third-party companies including Phison and Silicon Motion. Most SK products utilize proprietary controllers designed by SK itself. For example, the exemplary products listed below have the controllers listed below:

<u>Drive</u>	<u>Controller²¹</u>
SK hynix Silver S32	Silicon Motion SM2259XT
SK hynix BC901	Silicon Motion SM2269XT
SK hynix Gold P42	Phison E21T
Solidigm P42 Plus	Silicon Motion SM2268XT

¹⁹ Ex. N, <https://product.skhynix.com/products/ssd/essd.go>; Ex. Z, <https://ssd.skhynix.com>.

²⁰ Ex. M, <https://product.skhynix.com/products/nand/nand.go>.

²¹ Based on Ex. AA, https://www.techpowerup.com/ssd-specs/?f=mfgr_SK%20Hynix, or Ex. BB, https://www.techpowerup.com/ssd-specs/?f=mfgr_Solidigm, unless otherwise indicated.

Solidigm P41 Plus	Silicon Motion SM2269XT ²²
Solidigm 670p	Silicon Motion SM2265
SK hynix SC3010	SH87810AA
SK hynix PVC10	Aries Lite
SK hynix Platinum P51	Alistar
SK hynix Platinum P41	Aries
SK hynix PE8130	Aquarius
SK hynix PE8110	Aquarius
SK hynix PE6011	SH58800GG
SK hynix PCB01	Alistar
SK hynix PC801	Aries
SK hynix PC601	Cepheus Plus
SK hynix Gold S31	SK Hynix Quartz
SK hynix Gold P31	Cepheus
SK hynix Canvas SC300	SH87810AA
SK hynix Beetle X31	Cepheus 2
Solidigm P44 Pro	Aries
Solidigm D7-PS1030	Atomos Prime
Solidigm D7-PS1010	Atomos Prime
Solidigm D7-P5510	SLNBX Sentinel Rock

²² Ex. CC, <https://www.kitguru.net/components/ssd-drives/simon-crisp/solidigm-p41-plus-2tb-ssd-review/>.

Solidigm D5-P5430 ²³	Unknown
Solidigm D5-P5336	SLNQG Sentinel Rock Plus

52. SK designs, makes, uses, offers to sell, sells, imports, supplies, and/or otherwise distributes, and provides support for, flash memory products, including the exemplary products listed above, as well as other SSDs, embedded flash products, or other flash products that have the same or similar structures, features, or functionalities as the aforementioned products (“Accused Products”).

53. The Accused Products are integrated into devices made, used, offered for sale, sold, imported, supplied, or otherwise distributed in the United States by, among others, SK, SK’s customers, original equipment manufacturers (“OEMs”), original design manufacturers (“ODMs”), foundry suppliers, distributors, retailers, and other third parties. SK’s Accused Products are essential, non-trivial components of the products into which they are integrated.

54. SK also conducts research, development, and testing of Accused Products in the United States.

55. SK maintains a website that advertised and continues to advertise the Accused Products, including identifying the applications for which they can be used and specifications for the Accused Products.

56. SK’s development, sales, marketing, and manufacturing activities in the United States, including within this District, directly contributed to SK’s net revenue in the United States.

²³ Ex. DD, <https://www.solidigm.com/products/data-center/d5/p5430.html>.

COUNT I: INFRINGEMENT OF U.S. PATENT NO. 8,891,298

57. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

58. SK has directly infringed and continues to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '298 patent by making, using, offering for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). SK has also induced infringement of at least claim 1 of the '298 patent in violation of 35 U.S.C. § 271(b). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

59. The Accused Products meet all the limitations of at least claim 1 of the '298 patent. Specifically, claim 1 of the '298 patent recites:

A system for storing data comprising:

at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and

a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to:

- a) maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;

- b) determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;
- c) determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed; and
- d) allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module.

Ex. A, '298 patent at 7:7-8:9.

60. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, SK's SSDs and other flash storage products are all systems for storing data.



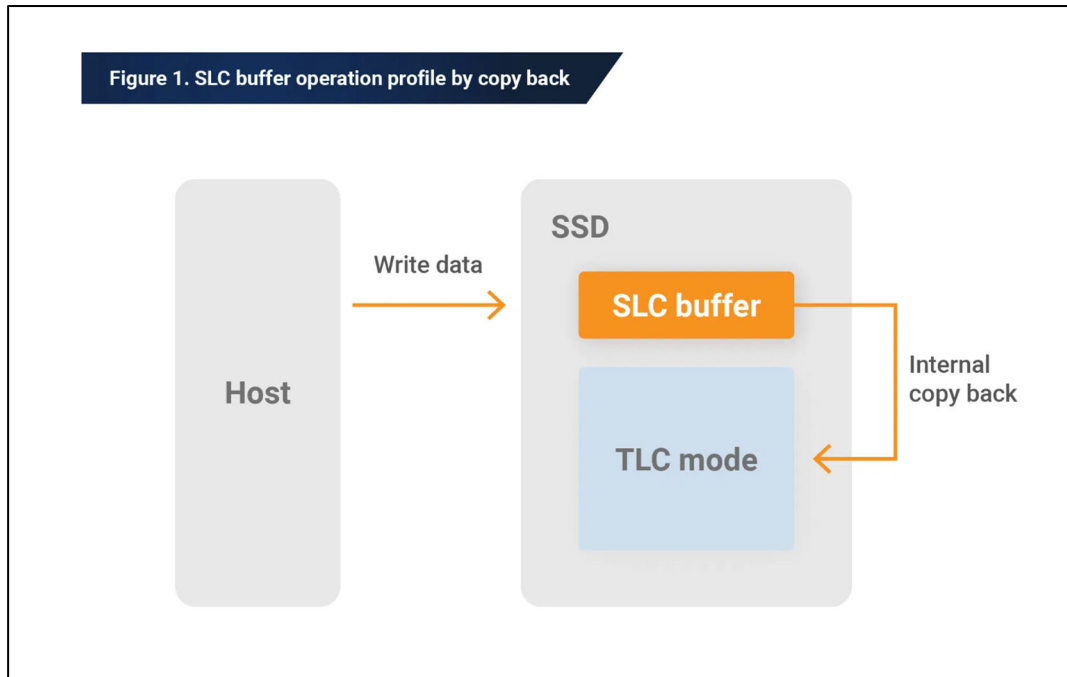
Ex. K, <https://product.skhynix.com/products/ssd/ssd.go>.

Made for Modern Data Demands

The broadest enterprise-grade storage portfolio available is also the most capable of solving for real-world deployments. Our purpose-built solutions address the unique demands of today's biggest storage challenges.

Ex. L, <https://www.solidigm.com/products/data-center.html>.

61. The Accused Products include at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks. For example, SK's Phison-based products use MLC (e.g. "TLC mode") memory as part of an SLC buffering system, and SK's Silicon Motion-based products use "Direct-to-TLC" and "SLC Caching" systems that include MLC memory.



Ex. EE, <https://phisonblog.com/the-benefits-of-using-slc-buffers-with-ssds-2/>.

Leveraging Silicon Motion's proprietary NANDXtend™ error-correcting code (ECC) technology, the SM2259 and SM2259XT enhance the endurance and retention of 3D NAND. Besides, SM2259 and SM2259XT include such enterprise features such as end-to-end data path protection and SRAM ECC capabilities to ensure the data integrity and reliability. SM2259 and SM2259XT also features advanced Direct-to-TLC and SLC Caching algorithms for optimal sustained performance with TLC and QLC NAND.

Ex. FF, https://www.siliconmotion.com/download/q/a/SM2259_XT_PB_EN_201910.pdf.

62. Likewise, the Accused Products that use proprietary controllers include at least one MLC non-volatile memory module:

Model & Capacity		Type
	SK Hynix Silver S32 500 GB 1 TB 2 TB	TLC SK Hynix 176-layer
	SK Hynix SC3010 960 GB	MLC SK Hynix Planar
	SK Hynix PVC10 1 TB	TLC SK Hynix 238-layer
	SK Hynix Platinum P51 500 GB 1 TB 2 TB	TLC SK Hynix 238-layer
	SK Hynix Platinum P41 500 GB 1 TB 2 TB	TLC SK Hynix 176-layer
	SK Hynix PE8130 800 GB 1.6 TB 3 TB 6 TB	TLC SK Hynix 128-layer
	SK Hynix PE8110 960 GB 1.9 TB 3.8 TB 7.5 TB	TLC SK Hynix 128-layer

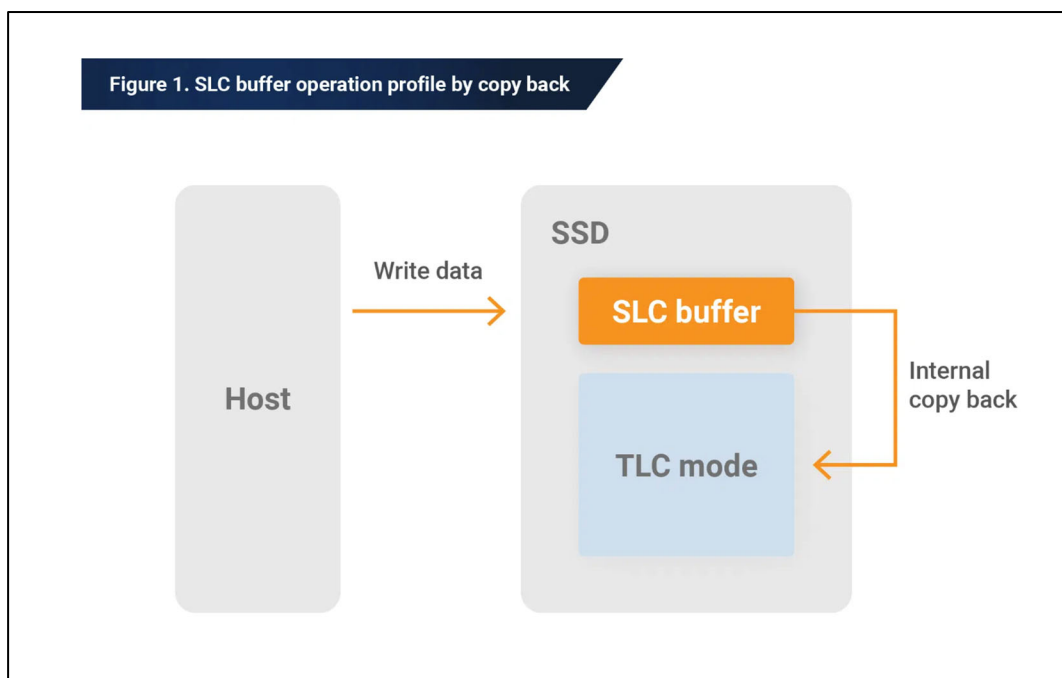
Ex. AA, https://www.techpowerup.com/ssd-specs/?f=mfg_SK%20Hynix.

63. The flash memory uses individually erasable blocks. For example, Phison explains that individual blocks are erased, and that this is an “intrinsic characteristic of NAND device physics”:

A flash memory cell is composed of pages, and pages form a block. Due to the intrinsic characteristic of NAND device physics, the flash cell allows data to be programmed on a page level but only erased on a block level. This inconsistency between program and erase tasks is the major impact on SSD endurance.

Ex. GG, <https://phisonblog.com/ssd-garbage-collection/>.

64. The Accused Products include at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks. The SLC caching systems, for example, used by the Accused Products use individually erasable SLC blocks.



Ex. EE, <https://phisonblog.com/the-benefits-of-using-slc-buffers-with-ssds-2/>.

Leveraging Silicon Motion's proprietary NANDXtend™ error-correcting code (ECC) technology, the SM2259 and SM2259XT enhance the endurance and retention of 3D NAND. Besides, SM2259 and SM2259XT include such enterprise features such as end-to-end data path protection and SRAM ECC capabilities to ensure the data integrity and reliability. SM2259 and SM2259XT also features advanced Direct-to-TLC and SLC Caching algorithms for optimal sustained performance with TLC and QLC NAND.

Ex. FF, https://www.siliconmotion.com/download/q/a/SM2259_XT_PB_EN_201910.pdf.

The SK Hynix Platinum P51 is a solid-state drive in the M.2 2280 form factor, launched on March 19th, 2024. It is available in capacities ranging from 500 GB to 2 TB. This page reports specifications for the 1 TB variant. With the rest of the system, the SK Hynix Platinum P51 interfaces using a PCI-Express 5.0 x4 connection. The SSD controller is the Alistar (ACNT093) from SK Hynix, a DRAM cache chip is available. SK Hynix has installed 238-layer TLC NAND flash on the Platinum P51, the flash chips are made by SK Hynix. To improve write speeds, a pseudo-SLC cache is used, so bursts of incoming writes are processed more quickly. Thanks to support for the fast PCI-Express 5.0 interface, performance is excellent. The Platinum P51 is rated for sequential read speeds of up to 13,500 MB/s and 11,500 MB/s write.

Ex. HH, <https://www.techpowerup.com/ssd-specs/sk-hynix-platinum-p51-1-tb.d1967> (noting that the SK hynix Platinum P51 implements “a pseudo-SLC cache”).

The SK hynix Gold P31 NVMe SSD contains their own proprietary NVMe 4-channel SSD controller, code named the Cepheus Controller, two pieces of the world's first 4D 128-layer TLC NAND flash memory with SLC caching and the SK hynix DRAM cache memory. It is a single sided SSD.

Ex. II, <https://www.thesdreview.com/our-reviews/nvme/sk-hynix-gold-p31-1tb-nvme-ssd-review-worlds-1st-128-layer-ssd-performs-at-an-amazing-price/>.

The Solidigm D7-PS1010 is a solid-state drive in the U.2 form factor, launched on August 6th, 2024. It is available in capacities ranging from 1.9 TB to 15 TB. This page reports specifications for the 1.9 TB variant. With the rest of the system, the Solidigm D7-PS1010 interfaces using a PCI-Express 5.0 x4 connection. The SSD controller is the Atomos Prime (ACNT08M) from SK Hynix, a DRAM cache chip is available. Solidigm has installed 176-layer TLC NAND flash on the D7-PS1010, the flash chips are made by SK Hynix. To improve write speeds, a pseudo-SLC cache is used, so bursts of incoming writes are absorbed more quickly. Thanks to support for the fast PCI-Express 5.0 interface, performance is excellent. The D7-PS1010 is rated for sequential read speeds of up to 14,500 MB/s and 4,100 MB/s write; random IO reaches 2350K IOPS for read and 150K for writes.

Ex. JJ, <https://www.techpowerup.com/ssd-specs/solidigm-d7-ps1010-1-9-tb.d2148> (noting that the Solidigm D7-PS1010 implements “a pseudo-SLC cache”).

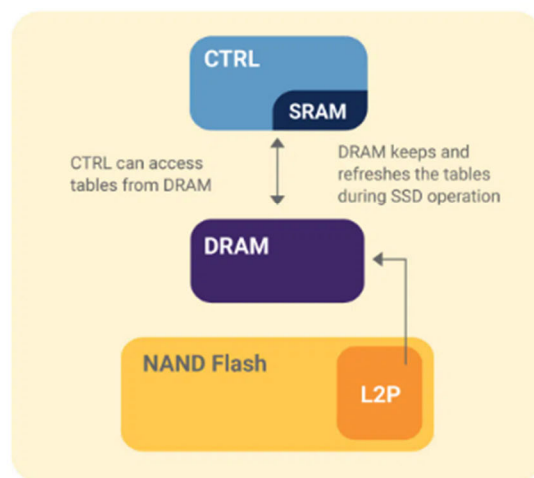
65. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module. For example, the exemplary products listed in the table in paragraph 51 above include the listed controllers.

66. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module. For example, Phison and Silicon Motion controllers in the Accused Products use a mapping table such as an L2P (logical-to-physical) table to keep track of the relationship between the logical blocks and the physical addresses of the flash memory.

67. Phison controllers use an L2P table:

The most important information that gets cached to or retrieved from a DRAM is the mapping information that turns logical addresses into the physical locations of stored data within the NAND flash array. This information is stored in mapping tables called L2P (logical-to-physical) tables and is updated frequently as SSDs move data in and out of flash storage. During shutdowns, the L2P table is stored in flash memory, since DRAM quickly becomes inoperable without a continuous power supply.

Figure 2. Cache operating mechanism of SSD with DRAM

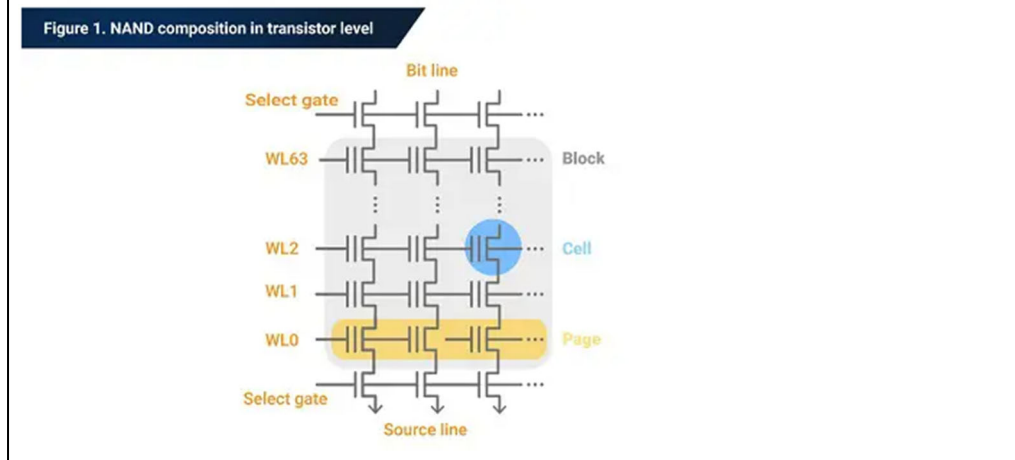


Ex. KK, <https://phisonblog.com/host-memory-buffer-2/>.

68. In Phison controllers, a minimum quanta of addresses—such as a page—is used:

NAND Flash is a non-volatile memory composed of millions of floating-gate transistors that capture electrons within the gate. These floating-gate transistors can be thought of as memory cells. When millions of memory cells are connected, they form an array. Each array consists of blocks and each block contains numbers of pages.

Fig.1 gives a brief illustration of a NAND array f schematic.



Ex. LL, <https://phisonblog.com/ensuring-data-correctness-with-phisons-guaranteedflush-2/>.

69. Silicon Motion controllers provide logical-to-physical translation:

DRAM cache with data redundancy:

no data loss during data transfers

Silicon Motion's new PCIe FerriSSD features an embedded DRAM which has a self-error detection and correction code (ECC) capability. This DRAM provides for secure, frequent read/write cache requests, and stores logical-to-physical address mapping information.

Ex. MM, https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf, at 2.

70. Silicon Motion's address map may take the form of a table:

Block translation in Markers table

In the last step of each case, it's necessary to arrange logical blocks in the Markers table, and in the case of these controllers, this step is quite simple and looks similar for every model of these controllers.

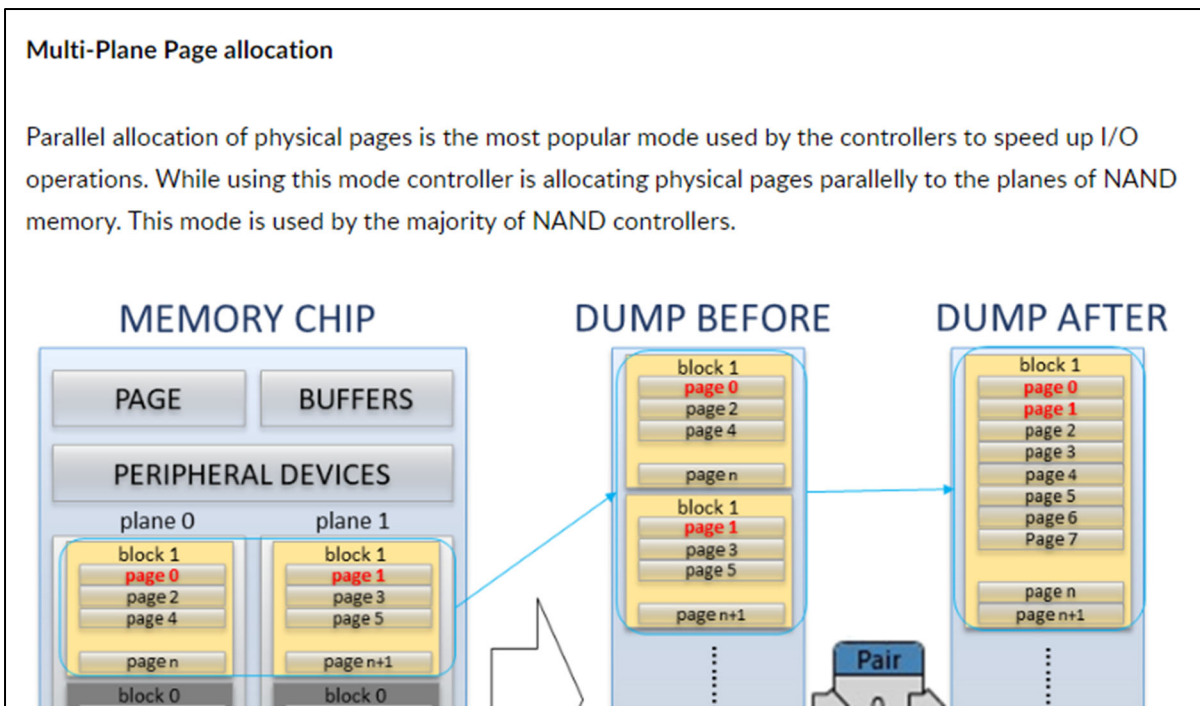
Structures of Service area

SiliconMotion controllers have exactly the same structure of the Service area.



Ex. NN, <https://support.rusolut.com/portal/en/kb/articles/silicon-motion-data-recovery>.

71. In Silicon Motion's address map, a minimum quanta of addresses—such as a page—is mapped to physical locations:



Ex. NN, <https://support.rusolut.com/portal/en/kb/articles/silicon-motion-data-recovery>.

72. Likewise, SK's proprietary controllers, coupled to the SLC and MLC non-volatile memory modules, are adapted to maintain address maps. While public documentation is limited, SK patent applications demonstrate how its controllers map logical addresses to physical addresses in MLC and SLC memory. For example, U.S. Patent No. 12,038,848 (the "'848 patent"), entitled "Compression of Logical-to-Physical Address Indirection Table on Solid-State Drives," issued July 16, 2024, and listing Solidigm as both Applicant and Assignee, states:

solid-state drives (SSDs). An SSD typically has an address indirection table that maps logical addresses associated with a host device to physical addresses of NAND flash memory in the SSD. Each memory unit of the SSD needs to be addressable in the address indirection table. Memory units can be grouped into larger block sizes and addressed with fewer addresses. However, as a capacity of the SSD increases, its memory units are addressed with more physical addresses, and more bits are inevitably needed to represent each physical address of the SSD. Long physical

Ex. OO, '848 patent at 1:26-35.

FIG. 5A is a diagram of a sequence of physical addresses corresponding to a sequence of logical addresses, in accordance with some embodiments.

FIG. 5B-5D are diagrams of three example data structures of an L2P address indirection table, in accordance with some embodiments.

FIG. 6A is a diagram illustrating a process of extracting a physical address from an L2P address indirection table, in accordance with some embodiments.

FIG. 6B is a diagram illustrating a process of updating a physical address **302** that is stored in an L2P address indirection table, in accordance with some embodiments.

FIG. 7 is a diagram of an example data structure of an L2P address indirection table including integrity data, in accordance with some embodiments.

FIG. 8 is a flow diagram of a method for compressing addresses stored in an L2P address indirection table, in accordance with some embodiments.

Ex. OO, '848 patent at 3:21-38.

73. U.S. Patent No. 11,709,623 (the “’623 patent”), entitled “NAND-based Storage Device with Partitioned Nonvolatile Write Buffer,” issued July 25, 2023, and listing Solidigm as both Applicant and Assignee, states:

access requests. In one example, the system comprises part of a solid state drive (SSD). In one example, the system further includes: a logic block address (LBA) map to indicate LBAs stored in the partitioned nonvolatile storage media and a location in the partitioned nonvolatile storage media of the LBAs. In one example, the partitioned nonvolatile storage media comprises a non-NAND storage media. In one example, the partitioned nonvolatile storage media comprises a single level cell (SLC) NAND media and the NAND storage media comprises a quad level cell (QLC) NAND media. In one example, the system includes one or

Ex. PP, ’623 patent at 24:40-50.

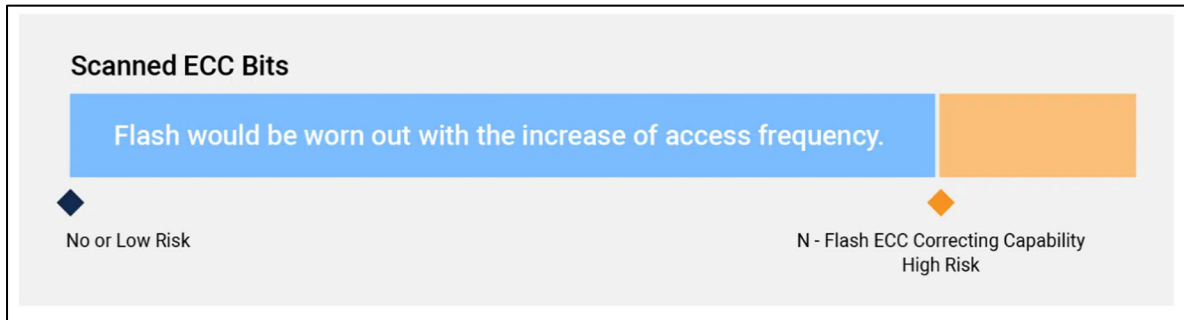
74. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module. For example, SK’s products include Phison and Silicon Motion controllers that incorporate defect and error management technology, and use a variety of tests to determine that there is a data integrity problem.

75. Phison controllers use a variety of data integrity tests to determine when there is a data integrity problem:

Phison's SmartRefresh™ technology

To protect the data stored in an SSD, Phison developed a proprietary technology called SmartRefresh™ that uses two primary methodologies:

1. Dynamic Error Bit Monitoring (DEBM)
2. Read Retry



Ex. QQ, <https://phisonblog.com/phisons-smartrefresh-2/>.

Data Reliability	• Phison 4th generation LDPC ECC • End-To-End Data Path Protection • Smart ECC 2.0 (RAID ECC)
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Ex. RR, https://www.phison.com/phocadownload/Brochure/Consumer_PS5021-E21T.pdf.

76. Upon a data integrity failure, Phison controllers remap degraded data to the next available location:

Phison's embedded firmware runs in the background to check the error bit of each block. Once there is a block fail within the criteria set by our firmware (i.e., the number of error bits is over the threshold decided in advance), the firmware performs specific actions on this failed block to guarantee the integrity of user data.

Ex. QQ, <https://phisonblog.com/phisons-smartrefresh-2/>.

NAND Flash Translation Layer

Phison has well over a decade of accumulated hardware and firmware expertise that enabled our proprietary FTL design with advanced mechanisms

SmartRefresh™

Scans NAND flash for errors when idle



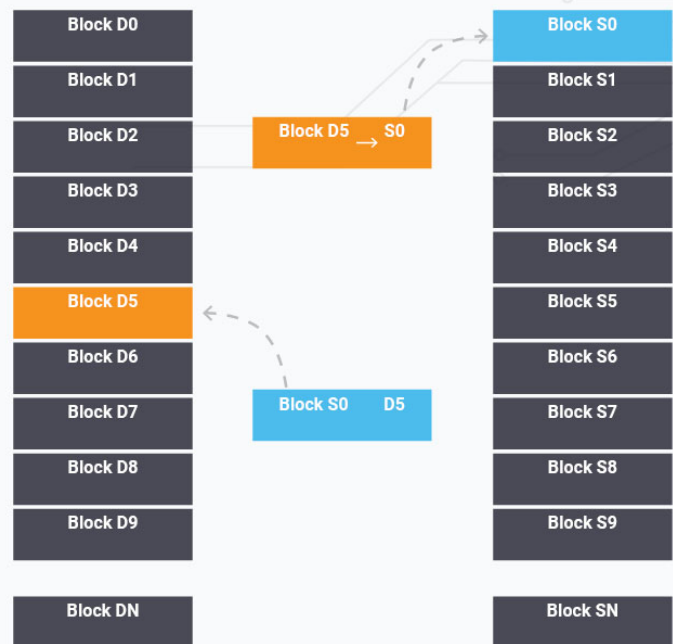
SmartFlush™

Works to prevent data loss by flushing the DRAM cache when idle is detected



Adaptive Wear Leveling

Efficient algorithms prolong the life of the NAND by monitoring not only the health of cells, but also the rate of cell degradation



Ex. SS, <https://www.phison.com/en/technology>, FTL tab.

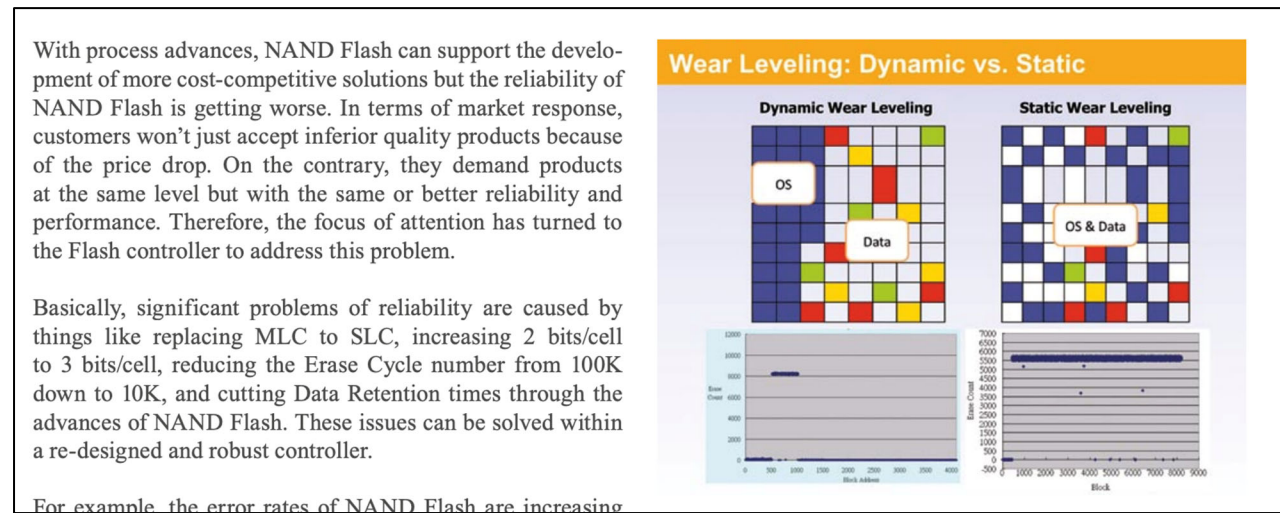
77. In particular, Phison controllers move data from MLC to SLC as part of the relocation above as part of Phison's SLC caching technology, where writes are made to SLC before being moved to MLC:

Consumer workloads also write over a limited LBA range. Writing the data to SLC first ensures that only the final valid copy of the data is written to the QLC. This limits the writes to QLC, enabling QLC NAND to be used for consumer drive, despite its lower endurance.

SLC cache is used in the consumer TLC drive today. It takes advantage of customer workloads to address the similar limitation of lower speed and limited endurance on TLC NAND. QLC based drives provide 33% higher capacity as compared to TLC NAND. This lowers the cost of the drive.

Ex. TT, <https://phisonblog.com/qlc-nand-for-consumer-ssds-2/>.

78. For example, Phison's articles describing its controllers discuss "replacing MLC to SLC":



Ex. UU, [https://www2.advantech.com/embcore/promotions/whitepaper/PHISON%20Electronics-The Stability and Reliability of Storage Devices.pdf](https://www2.advantech.com/embcore/promotions/whitepaper/PHISON%20Electronics-The%20Stability%20and%20Reliability%20of%20Storage%20Devices.pdf).

79. Silicon Motion controllers use a variety of data integrity tests to determine when there is a data integrity problem:

**Full end-to-end data path protection:
no bit errors sent to host**

Conventional SSDs may employ error detection and correction circuitry at the far ends of the data path: at the front-end host interface and at the back-end

NAND interface. This omits an important gap at the internal SRAM and/or DRAM transfer buffers, and other circuit paths. Data errors that occur between the NAND interface and the host, such as soft error bits, are often extremely difficult to identify and duplicate.

While conventional SSDs may have some internal error detection circuitry, the new PCIe FerriSSD storage solutions incorporate full data recovery engines to provide enhanced data integrity throughout the entire Host-to-NAND-to-Host data path.

The PCIe FerriSSD data recovery algorithm can effectively detect any error in the SSD data path, including hardware errors, firmware errors and memory errors arising in SRAM, DRAM or NAND. The PCIe FerriSSD implements an additional redundant back-up in NAND – the SMI Ferri Group Page Raid – which reinforces the protection against the risk of uncorrectable error in the NAND storage medium.

Ex. MM,

https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf, at 2.

**IntelligentScan & DataRefresh:
proactive data loss prevention measures**

The features described above protect against the risk of data loss or error in data-transfer operations. The PCIe FerriSSD also incorporates sophisticated functions which ensure the integrity of data in storage.

The IntelligentScan & DataRefresh function achieves this by identifying at-risk memory cells and refreshing the data stored in them. The risk of loss of stored data increases as:

- **the aggregate number of Program / Erase (P/E) cycles increases**
- **the ambient temperature rises**

In either condition, the operation of the IntelligentScan & DataRefresh function becomes increasingly important.

Read disturbance

Performing an excessive number of read cycles from a cell, can cause unintended over-charging of adjacent cells, leading to unrecoverable bit errors, a phenomenon known as Read disturbance. FerriSSD products avoid potential Read disturbance errors by performing periodic IntelligentScan & DataRefresh operations on NAND blocks that undergo repetitive Read cycles. The PCIe FerriSSD firmware – an advanced 4th generation algorithm (IntelligentScan) – automatically manages DataRefresh cycles and processing time to minimize data loss due to the impact of intensive Read operations on the NAND Flash storage medium.

Ex. MM,

https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf, at 2-3.

The IntelligentScan function is responsible for checking whether the stored charge has declined below its threshold value. If it has, it reads out the data bit and rewrites it via the ECC engine, and DataRefresh recharges the cell to restore the NAND cell's voltage to the correct level.

Ex. VV, https://www.siliconmotion.com/download/3g1/a/FerriSSD_Gaming_WP_EN.pdf at 5.

With Intelligent Scan, FerriSSD's firmware will respond to changing usage conditions to intelligently determine where, when and how frequently to scan the SSD. The scan will be triggered during idle time, based on preset thresholds and self-adopting algorithms, to determine which cells should be scanned according to severity priority (such as temperature readings, read counts, and other factors).

When IntelligentScan identifies overstressed cells, SMI's proprietary DataRefresh function will be activated automatically to recharge, repair or retire the cell block accordingly. As a result of the combination of Intelligent Scan and Data Refresh, FerriSSD can prolong its usage life much beyond typical NAND specifications.

Ex. WW, https://www.siliconmotion.com/download/3TY/a/FerriSSD_BGASSD_WP_EN.pdf, at 5.

NANDXtend™ Technology

The SM2259 and SM2259XT employs the company's proprietary NANDXtend™ ECC technology consisting of LDPC hard and soft decoding as well as RAID protection that together enhance the P/E cycles of 3D NAND - extending the SSD lifespan and ensuring data integrity. The new generation NANDXtend™ includes 2KB LDPC engine with advanced firmware algorithm delivers higher power efficiency, decoding efficiency and correction capability to maintain consistent data throughout and provide a better user experience, even as error bits increase throughout the product lifecycle of NAND Flash.

PE CYCLE

RAID Data Recover
Soft Decode
Hard Decode

POWER EFFICIENCY

New NANDXtend™ +20%

DECODING EFFICIENCY

+40%

SOFT-DECODING CORRECTION CAPABILITY

New NANDXtend™ +25%

HARD-DECODING CORRECTION CAPABILITY

New NANDXtend™ X2

Ex. FF, https://www.siliconmotion.com/download/q/a/SM2259_XT_PB_EN_201910.pdf, at 2.

Silicon Motion's SM689 and SM681 FerriSSDs supports enhanced reliability and data integrity features for use in demanding automotive, commercial, enterprise and industrial applications. Its set of features includes:

- End-to-end data path protection, which applies error correction code (ECC) to the SSD's SRAM and DRAM buffers as well as to the primary NAND Flash memory array
- DRAM data cache to ensure data programming and enable data redundancy, without delaying host processor operations
- Hybrid Zone which enables a single disk to be partitioned into single-level cell (SLC) and multi-level cell/three-level cell (MLC/TLC) zones, enabling faster access speeds and data retention
- Intelligent Scan/DataRefresh protects against the higher data loss from operating at high temperatures
- NANDXtend™ technology incorporating Silicon Motion's proprietary 4th generation high-performance LDPC ECC engine with RAID, ensuring better data integrity even in extreme physical environments

Ex. XX, <https://www.prnewswire.com/news-releases/silicon-motion-announces-worlds-first-pcie-nvme-single-chip-ssds-with-enterprise-grade-data-protection-features-300604092.html>.

End to End Data Path Protection

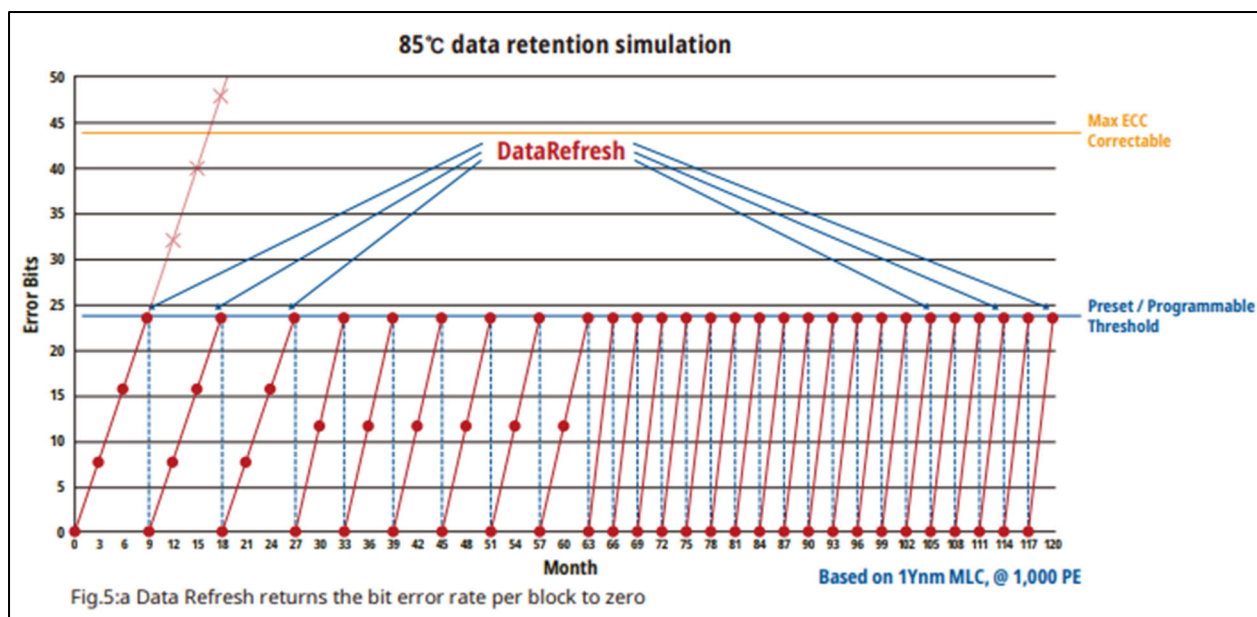
Silicon Motion's SSD controller solutions incorporate full data error detection with recovery engines to provide enhanced data integrity throughout the entire Host-to-NAND-to-Host data path. The data recovery algorithm can effectively detect any error in the SSD data path, including hardware (i.e. ASIC) errors, firmware errors, and memory errors arising in SRAM, DRAM, or NAND.

Ex. YY, <https://www.siliconmotion.com/products/client/detail>.

80. Upon a data integrity failure, Silicon Motion controllers remap (or “refresh”) the data to the next available location:

The IntelligentScan & DataRefresh function achieves this by identifying at-risk memory cells and refreshing the data stored in them. The risk of loss of stored data increases as:

Ex. MM, https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf, at 2.



Ex. ZZ,

https://www.siliconmotion.com/download/3TZ/a/Ferri_Family_Optimizes_Embedded_WP_EN.pdf, at 5 (showing that when data integrity test shows error bits exceed a threshold, the data is rewritten to new blocks and that the error rate returns to zero).

81. In particular, Silicon Motion controllers may move data from MLC to SLC as part of the relocation above as part of Silicon Motion's SLC caching technology. Further, Silicon Motion's system also moves data to SLC for emergency shutdown operations, which may be considered a response to a failure of a data integrity test (such as power loss that jeopardizes data):

Without foregoing the density benefits of MLC/TLC, single NAND die SSDs can still maintain fast Write

SLC memory, which is ideal for emergency power shutdown operations. Without a portion of memory implemented as SLC, both the cost and the size of battery storage needed for MLC/TLC power shutdown would increase. The implementation of

Ex. MM,

https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf, at 4.

82. SK's proprietary controllers likewise perform a variety of data integrity tests and remap data to SLC memory in response to data integrity test failures. While public documentation is limited, SK patent applications demonstrate how its controllers operate. For example, U.S. Patent Application Pub. No. US 2024/0289040, entitled "Controlling Memory Overhead for Storing Integrity Data in Solid State Drives," published August 29, 2024, and listing Solidigm as the Applicant, depicts data integrity testing and remapping to SLC:

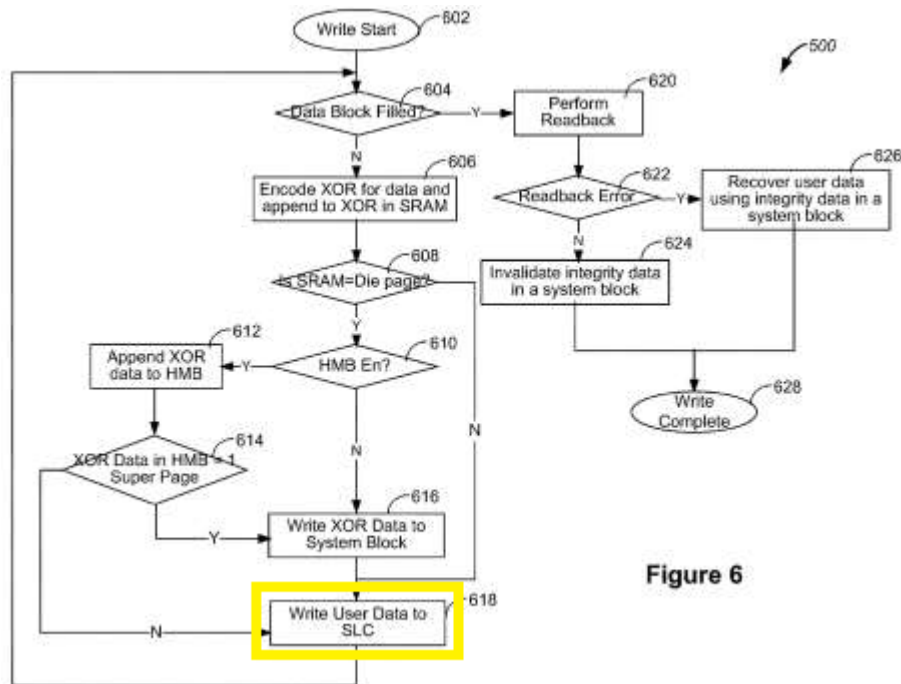
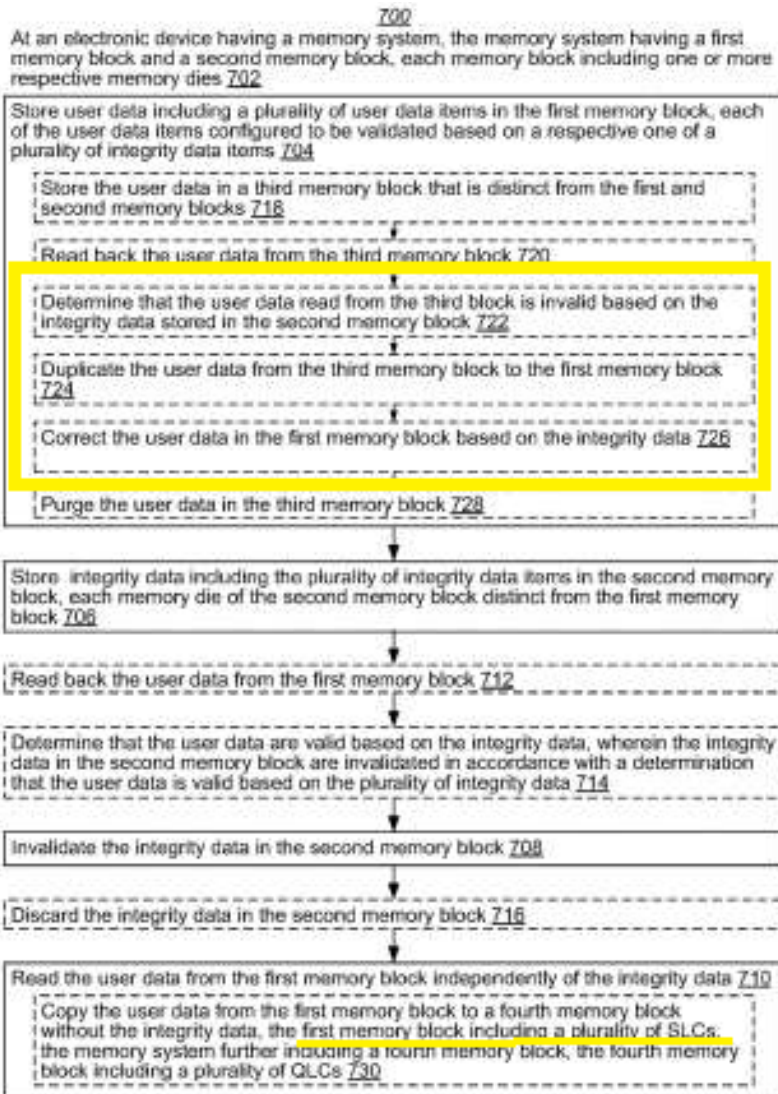


Figure 6

Ex. AAA, U.S. Pat. App. Pub. No. US 2024/0289040, Fig. 6 (highlight added).

**Figure 7**

Ex. AAA, U.S. Pat. App. Pub. No. US 2024/0289040, Fig. 7 (highlights added).

[0048] After the integrity data **304** in the second memory block **306** is invalidated, the user data **302** is read from the first memory block **306A**, independently of the integrity data **304**. In some embodiments, the first memory block **306A** includes a plurality of first cells of a first cell type (e.g., SLC). The memory system **200** further includes a fourth memory block **306D** having a plurality of second cells of a second cell type (e.g., QLC). In an internal copy back **310**, the user data **302** is copied from the first memory block **306A** to the fourth memory block **306D** without the integrity data **304**. Each of the first and second cell types is a

respective one of an SLC, MLC, TLC, QLC, PLC, and six- or higher-level cell, while the first cell type is distinct and different from the second cell type.

Ex. AAA, U.S. Pat. App. Pub. No. US 2024/0289040, [0048].

83. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed. For example, SK's products use controllers, such as Phison or Silicon Motion controllers, that employ various types of block counting.

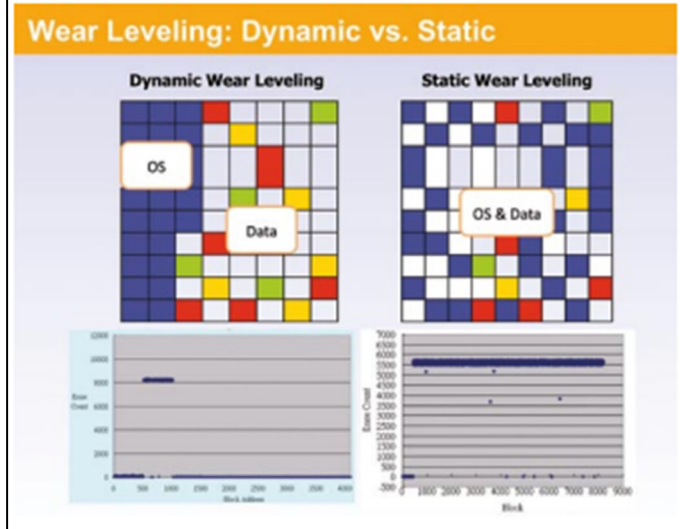
84. For example, Phison controllers use count data, such as program/erase counts and valid page counts, to maintain a count of the number of times each one of the blocks is accessed:

Dynamic SLC buffer (D3)

A dynamic SLC buffer used with TLC flash, meaning that the SLC buffer in zone D3 zone can dynamically use the TLC flash by erasing the count balance scheme. The SSD firmware configures to select the block with the lowest erase count every time the dynamic SLC buffer is processed. The dynamic SLC buffer can be automatically disabled using FW calculations based on flash endurance for different flash types.

Ex. EE, <https://phisonblog.com/the-benefits-of-using-slc-buffers-with-ssds-2/>.

In addition, decreasing the Erase Count has brought about a shorter life expectancy of NAND Flash. The wear leveling mechanism of the controller can resolve this problem. NAND Flash consists of many blocks and each block has its certain life span. The number of erasable cycles represented the block life-expectancy and was called the Erase Count. In order to extend the lifetime of NAND Flash, we have to balance the Erase Count of all blocks. With a wear leveling mechanism implemented, the controller can achieve this goal to average the Erase Count of each block.



Ex. UU,

[https://www2.advantech.com/embc/core/promotions/whitepaper/PHISON%20Electronics-The Stability and Reliability of Storage Devices.pdf](https://www2.advantech.com/embc/core/promotions/whitepaper/PHISON%20Electronics-The%20Stability%20and%20Reliability%20of%20Storage%20Devices.pdf).

“A memory management method, and a memory control circuit unit and a memory storage apparatus using the same are provided. The method includes associating physical erasing units with a data area or a spare area, configuring a plurality of logical addresses for mapping to the physical erasing units, and obtaining a garbage collection threshold based on a plurality of valid logical addresses among the logical addresses, and the physical erasing units mapping to the valid logical addresses are associated with the data area. The method further includes performing a garbage collection operation on the data area if the number of the physical erasing units associated with the data area is no less than the garbage collection threshold.”

Ex. BBB, U.S. Pat. App. Pub. No. 2019/0073298, Abstract (Phison).

85. For example, Silicon Motion controllers use count data, such as program/erase (P/E) counts and valid page counts, to maintain a count of the number of times each one of the blocks is accessed:

Effect of temperature on data retention

One of the most significant inhibitors to data retention is elevated NAND temperature – the higher the ambient working temperature, the shorter the retention capability of the NAND itself. The PCIe FerriSSD incorporates a Silicon Motion patent-pending monitoring algorithm which logs cumulative junction temperature readings, the number of P/E cycles, SSD power on-time, and other essential reference points to dynamically select and prioritize which NAND cells to DataRefresh, and when.

Ex. MM,

https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf, at 3.

Armed with Silicon Motion's proprietary IntelligentScan & DataRefresh, FerriSSD will intelligently activate a self-scanning feature to prevent potential data lost before it occurs; the self-scan frequency will be intelligently adjusted by ambient temperature, erase count, read count, and associated factors. FerriSSD's

Ex. WW, https://www.siliconmotion.com/download/3TY/a/FerriSSD_BGASSD_WP_EN.pdf, at 3.

Silicon Motion patents and patent applications also discuss this functionality:

“In the control method, by establishing a valid page count table, a detailed valid page count table and/or a zone valid page count table according to deallocate command from the host device, the flash memory controller can efficiently and quickly determine if any one of the zones does not have any valid data, so that the flash memory controller can recommend the host device to send a reset command to reset the zone. In addition, after receiving the reset command from the host device, the flash memory controller can use a garbage collection operation or directly put the blocks corresponding to the erased zone into a spare block pool, for the further use.”

Ex. CCC, U.S. Patent 11,809,328, Abstract; *see also* Ex. DDD, U.S. Patent App. Pub. No. 2023/0350799, Abstract (describing valid page count table).

86. Likewise, SK's proprietary controllers use count data—such as program/erase counts and valid page counts—to maintain a count of the number of times each one of the blocks is accessed. While public documentation is limited, SK patent applications demonstrate its

controllers' use of such counts. For example, U.S. Patent No. 10,008,250 (the "'250 patent"), entitled "Single Level Cell Write Buffering for Multiple Level Cell Non-Volatile Memory," issued June 26, 2018, and presently assigned to Solidigm, describes tracking erase counts:

In one embodiment, every time a new host block is opened for writing, it is opened in SLC mode. As soon as a write idle threshold is met, the content from SLC blocks are processed/moved (e.g., garbage collected) to TLC blocks. The SLC blocks are simply accounted as if they were TLC block in terms of endurance (i.e., one SLC erase operation is counted as if it is a TLC erase operation). Moreover, TLC

Ex. EEE, '250 patent at 6:59-65.

87. The '623 patent describes classifying data based on write frequency, and how that function may be implemented in a controller:

In contrast to traditional systems that process writes as they are received and therefore mixes data with different lifetimes in the same blocks, in one example, classification engine **130** enables system **100** to separate data based on the lifetime of the data associated with the write requests. In one example, classification engine **130** is a software engine executed on host platform **110**, such as a module of filesystem **126**. In one example, classification engine **130** is a driver of interface **128** that receives data from filesystem **126**, and separates the data into different classes within write buffer **140**. In one example, classification engine is implemented in firmware either in interface hardware. In one example, classification engine **130** is implemented in controller **152** when write buffer **140** is part of nonvolatile storage device **150**.

Ex. PP, '623 patent at 5:8-22.

88. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the

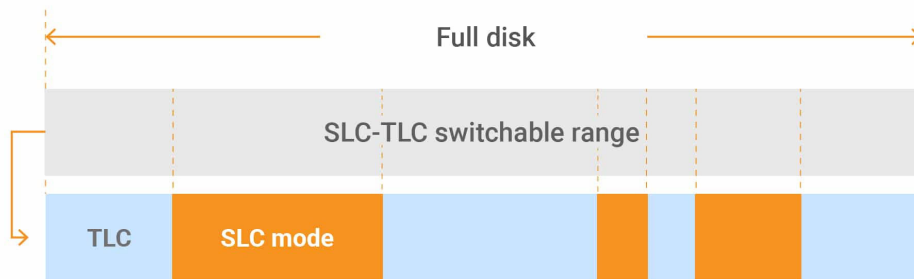
controller is adapted to allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module.

89. Phison controllers move frequently accessed data to SLC NAND. A “count balance scheme” is used to transfer frequently written blocks to SLC, and blocks are switchable between SLC and TLC:

Dynamic SLC buffer (D3)

A dynamic SLC buffer used with TLC flash, meaning that the SLC buffer in zone D3 zone can dynamically use the TLC flash by erasing the count balance scheme. The SSD firmware configures to select the block with the lowest erase count every time the dynamic SLC buffer is processed. The dynamic SLC buffer can be automatically disabled using FW calculations based on flash endurance for different flash types.

Figure 3. Dynamic SLC buffer profile



Ex. EE, <https://phisonblog.com/the-benefits-of-using-slc-buffers-with-ssds-2/>.

90. In addition, garbage collection can relocate frequently accessed data based on a page count:

For random writes, the main issue is invalid pages. Whenever garbage collection engages, the controller needs to write valid pages to other unused blocks. With the background read/write and Host read/write requests, the overall drive performance degrades.

Ex. FFF, <https://phisonblog.com/using-overprovisioning-with-ssds-2/>.

91. Phison also uses a “double rotation” scheme to move data to SLC blocks:

Therefore, controllers are using many sophisticated functions to protect stored data. We can observe these results during our daily work, many steps have to be applied before data will be recovered and almost every operation, we reverse, is applied to protect user data as well as possible.

In this article, we would like to bring closer SLC blocks topic and present to you the solution for Phison controllers which are using double rotation mode.

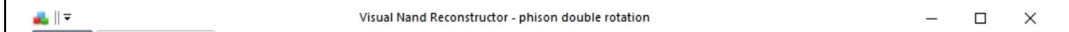
How to recognize that controller uses double rotation?

How to reverse this type of rotation?

How to pull out data from the SLC block?

All this information you will find in this article.

In the example below we have a dump from a micro SD card equipped with a Phison controller. We’ve used static rotation, but despite, that the rotation element is attached, we could not access the file system.



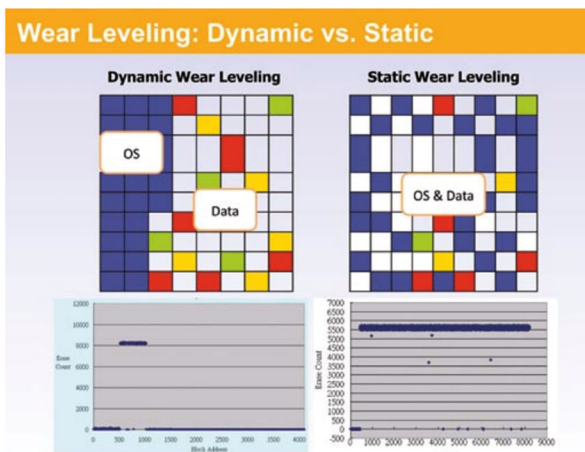
Ex. GGG, <https://support.rusolut.com/portal/en/kb/articles/no-pic-no>.

92. Phison’s articles discuss “replacing MLC to SLC”:

With process advances, NAND Flash can support the development of more cost-competitive solutions but the reliability of NAND Flash is getting worse. In terms of market response, customers won’t just accept inferior quality products because of the price drop. On the contrary, they demand products at the same level but with the same or better reliability and performance. Therefore, the focus of attention has turned to the Flash controller to address this problem.

Basically, significant problems of reliability are caused by things like replacing MLC to SLC, increasing 2 bits/cell to 3 bits/cell, reducing the Erase Cycle number from 100K down to 10K, and cutting Data Retention times through the advances of NAND Flash. These issues can be solved within a re-designed and robust controller.

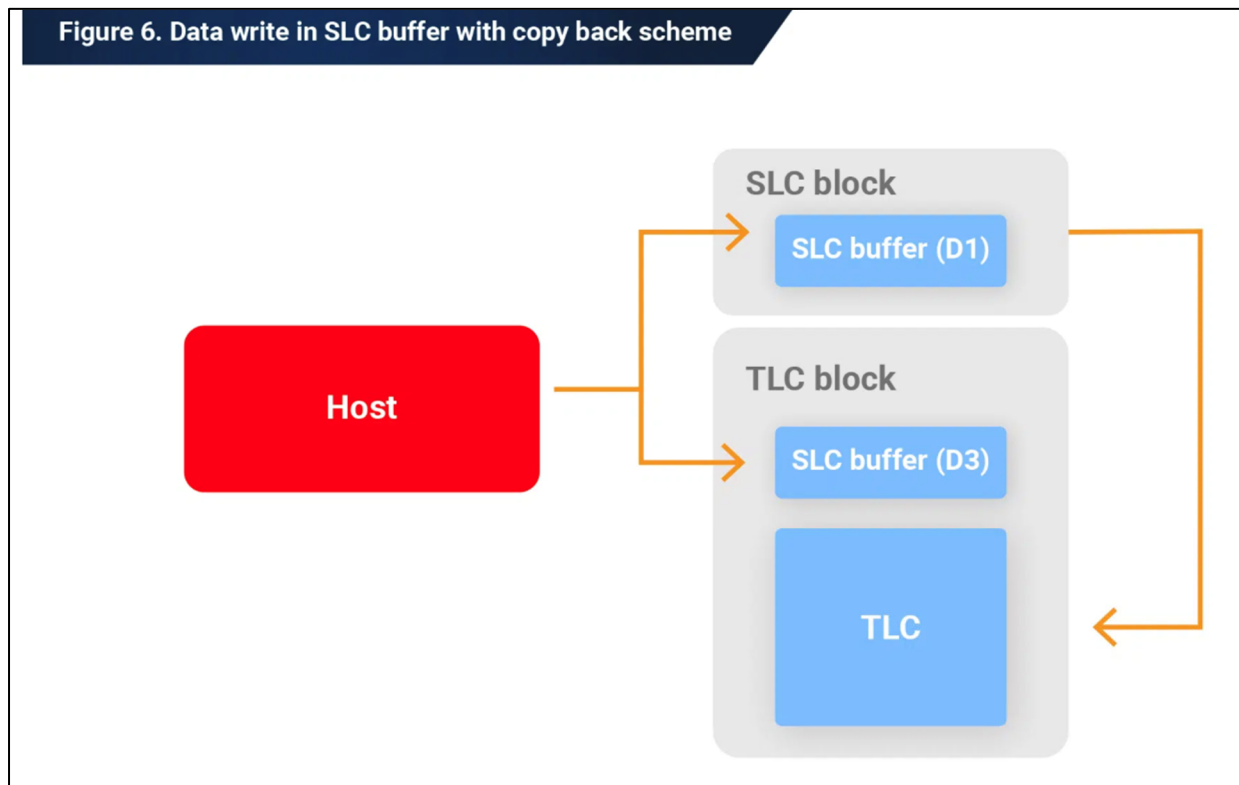
For example, the error rates of NAND Flash are increasing



Ex. UU,

[https://www2.advantech.com/embcore/promotions/whitepaper/PHISON%20Electronics-The Stability and Reliability of Storage Devices.pdf](https://www2.advantech.com/embcore/promotions/whitepaper/PHISON%20Electronics-The%20Stability%20and%20Reliability%20of%20Storage%20Devices.pdf).

93. Phison's controllers have a copyback scheme where data is moved between SLC and TLC blocks; with this scheme, data being rewritten as part of garbage collection may be moved from TLC to SLC. For example, Phison's blog explains that "When an SSD uses copy back, host data moves into zone D1," where D1 represents SLC.



Ex. EE, <https://phisonblog.com/the-benefits-of-using-slc-buffers-with-ssds-2/>.

94. Silicon Motion controllers move frequently accessed data to SLC NAND.

Hybrid Zone, a unique feature of the PCIe FerriSSD, offers a way to take advantage both of the low latency of SLC cells and the high memory density of TLC cells.

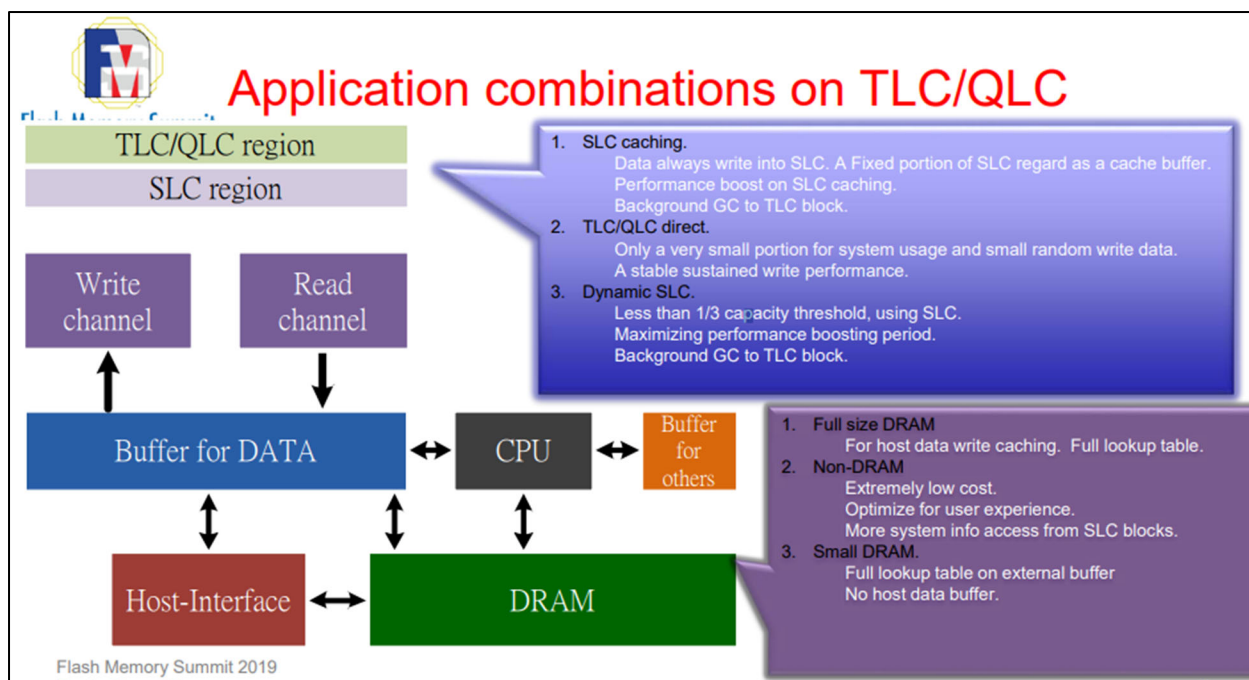
The Hybrid Zone feature partitions a single NAND die into separate SLC and MLC/TLC zones. Partitioning a single drive is particularly useful in low- to medium- density SSDs.

Without foregoing the density benefits of MLC/TLC, single NAND die SSDs can still maintain fast Write

SLC memory, which is ideal for emergency power shutdown operations. Without a portion of memory implemented as SLC, both the cost and the size of battery storage needed for MLC/TLC power shutdown would increase. The implementation of SLC memory is also ideal for high reliability and fast access— assigning SLC to boot code for instance – while also preserving a portion of the NAND medium for higher density MLC/TLC uses.

Ex. MM,

https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf, at 4.



Ex. HHH, https://www.flashmemorysummit.com/Proceedings2019/08-05-Monday/20190805_PreConfG_Yang.pdf, at 5.

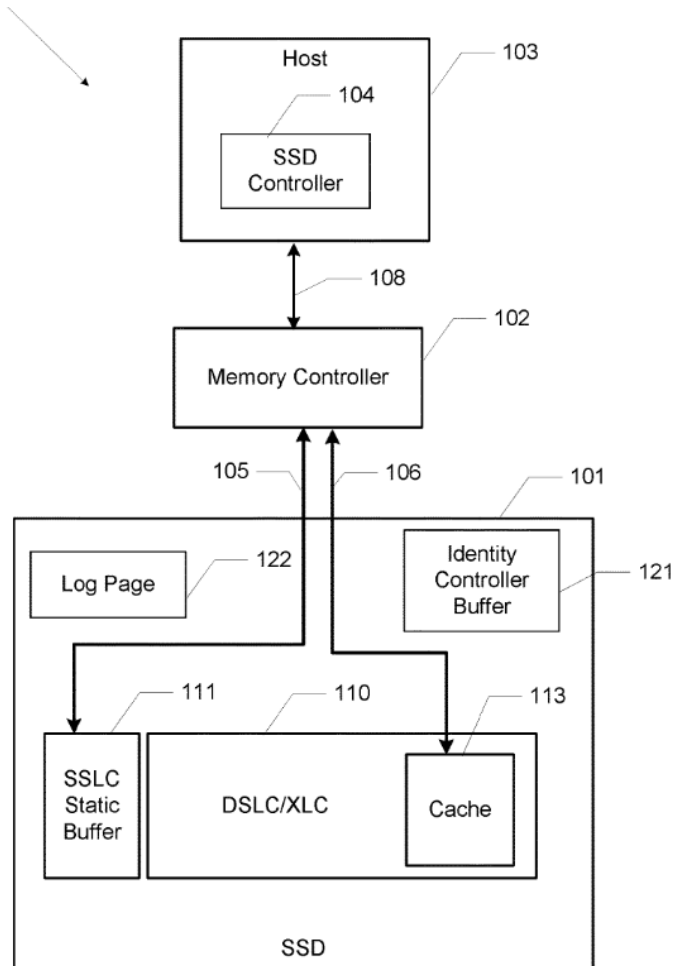
95. Likewise, SK's proprietary controllers transfer the contents of frequently written blocks to SLC. While public documentation is limited, SK patent applications demonstrate the transfer and caching of these blocks in SLC. For example, US Patent No. 10,379,782 (the "'782 patent"), entitled "Host Managed Solid State Drivecaching Using Dynamic Write Acceleration," issued August 13, 2019, and presently assigned to Solidigm, states:

An SSD may include a static SLC NAND buffer to improve burst write performance for writing data to the SSD followed by writing the data to MLC (for example, TLC or QLC) NAND via direct writes to MLC NAND along with eviction of the data from the static SLC NAND buffer. Another approach for providing faster data access is called dynamic SLC wherein a portion of MLC NAND is used in SLC mode and then dynamically converted to MLC mode when additional user-capacity is needed. Neither of these techniques account for caching of most frequently accessed data (hot data) in fast media (for example, SLC NAND).

Ex. III, '782 patent at 1:59-2:2.

Turning now to FIG. 1A, a host managed SSD caching solution **100** provides an ability to read/write data **104** into/out of a fast media, for example, a SLC (DSL²C) buffer region **113** in a SSD **101**. In an embodiment the host **103** has

Ex. III, '782 patent at 2:15-18.



Ex. III, '782 patent at Fig. 1A.

Q.

What is wear leveling?

A.

The NAND flash memory component of a SSD stores data.

Wear leveling is a technique that prolongs the lifespan of the NAND flash memory by avoiding writing (i.e. storing data) in the same blocks repetitively and instead storing data in less heavily used locations.

This technique allows the NAND flash memory to evenly use all data blocks, thereby increasing the lifespan of a SSD.

Ex. JJJ, https://skhynix.freshdesk.com/support/solutions/folders/48000658601#faq_title, Product Specification tab.

96. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

97. Defendants indirectly infringe the '298 patent, as provided in 35 U.S.C. § 271(b), including by inducing infringement by third parties such as computer manufacturers—*e.g.*, Dell, Apple, or Lenovo. The third parties who make, have made, use, have used, import, have imported, export, have exported, offer to sell, have offered to sell, sell, and/or have sold products that incorporate SK Accused Products have directly infringed and continue to directly infringe each of the claims as specified above. On information and belief, and based on the websites and marketing information cited herein, SK induces this direct infringement through its affirmative acts of manufacturing, selling, distributing, and/or otherwise making available the Accused Products to third parties, and providing direction, instruction, documentation, and other information to third parties suggesting they use the Accused Products in an infringing manner. SK performs these affirmative acts with knowledge or willful blindness of the '298 patent and with the intent, or willful blindness, that the induced third parties directly infringe the '298 patent.

98. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

99. Upon information and belief, SK was aware of Vervain's patents as early as July 8, 2020, when Vervain and SK executed a standstill agreement specifically identifying the '298, '385, and '240 patents, as well as the then-pending application that resulted in issuance of the '300

patent. Despite having knowledge of the '298 patent and knowledge that it is directly and/or indirectly infringing one or more of its claims, SK has continued its infringing conduct and disregarded an objectively high likelihood of infringement. SK's infringing activities have been, and continue to be, willful, wanton, and deliberate, such that Vervain is entitled to enhanced damages under 35 U.S.C. § 284.

100. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of Defendants' infringement of the '298 patent.

101. Vervain is entitled to all rights to recover for present, past, and future infringement for each of the patents-in-suit. Vervain is entitled to recover to the full extent allowable under 35 U.S.C. §§ 284-287, including for up to six years prior to the filing of the complaint. There is no marking issue under 35 U.S.C. § 287 or otherwise which would limit damages, and Vervain has complied with all relevant statutes for maximum recovery under the law.

COUNT II: INFRINGEMENT OF U.S. PATENT NO. 9,196,385

102. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

103. SK has directly infringed and continues to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '385 patent by making, using, offering for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). SK has also induced infringement of at least claim 1 of the '385 patent in violation of 35 U.S.C. § 271(b). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

104. The Accused Products meet all the limitations of at least claim 1 of the '385 patent.

Specifically, claim 1 of the '385 patent recites:

A system for storing data comprising:

at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and

a flash translation layer (FTL); wherein the FTL is adapted to:

- a) maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;
- b) determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;
- c) determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed; and
- d) allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module.

Ex. B, '385 patent at 7:12-8:4.

105. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

106. The Accused Products include at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks. As explained in Count I above, the Accused

Products store certain data in MLC memory with individually erasable blocks, for example as part of an SLC caching or direct-to-TLC system.

107. The Accused Products include at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks. As explained in Count I above, the Accused Products store certain data in SLC memory with individually erasable blocks, for example as part of an SLC caching system.

108. The Accused Products include a flash translation layer (FTL). For example, as explained in Count I above, the Accused Products provide mapping between logical and physical addresses using a data structure such as a L2P table. This is known as a flash translation layer:

NAND Flash Translation Layer

Phison has well over a decade of accumulated hardware and firmware expertise that enabled our proprietary FTL design with advanced mechanisms

Ex. SS, <https://www.phison.com/en/technology>, FTL tab.

109. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module. For example, as explained in Count I above, the Accused Products provide mapping between logical and physical addresses using a data structure such as a L2P table, and these mappings have a minimum quanta such as a page.

110. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of

physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module. For example, as explained in Count I above, the controllers in the Accused Products perform a variety of data integrity functions, and remap data to SLC memory upon the failure of a data integrity test.

111. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed. For example, as explained in Count I above, a variety of block counting mechanisms are present in the Accused Products.

112. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module. For example, as explained in Count I above, frequently written blocks are allocated and their contents transferred to SLC.

113. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

114. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

115. Defendants indirectly infringe the '385 patent, as provided in 35 U.S.C. § 271(b), including by inducing infringement by third parties such as computer manufacturers—*e.g.*, Dell, Apple, or Lenovo. The third parties who make, have made, use, have used, import, have imported, export, have exported, offer to sell, have offered to sell, sell, and/or have sold products that incorporate SK Accused Products have directly infringed and continue to directly infringe each of the claims as specified above. On information and belief, and based on the websites and marketing information cited herein, SK induces this direct infringement through its affirmative acts of manufacturing, selling, distributing, and/or otherwise making available the Accused Products to third parties, and providing direction, instruction, documentation, and other information to third parties suggesting they use the Accused Products in an infringing manner. SK performs these affirmative acts with knowledge or willful blindness of the '385 patent and with the intent, or willful blindness, that the induced third parties directly infringe the '385 patent.

116. Defendants' infringement is willful. As described under Count I above, Defendants were aware of Vervain's patents and of their infringement. Defendants have continued their infringing conduct and disregarded an objectively high likelihood of infringement. Defendants' infringing activities have been, and continue to be, willful, wanton, and deliberate, such that Vervain is entitled to enhanced damages under 35 U.S.C. § 284.

117. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '385 patent by Defendants.

118. Vervain is entitled to all rights to recover for present, past, and future infringement for each of the patents-in-suit. Vervain is entitled to recover to the full extent allowable under 35 U.S.C. §§ 284-287, including for up to six years prior to the filing of the complaint. There is no

marking issue under 35 U.S.C. § 287 or otherwise which would limit damages, and Vervain has complied with all relevant statutes for maximum recovery under the law.

COUNT III: INFRINGEMENT OF U.S. PATENT NO. 9,997,240

119. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

120. SK has directly infringed and continues to infringe, either literally or under the doctrine of equivalents, at least claim 6 of the '240 patent by making, using, offering for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). SK has also induced infringement of at least claim 6 of the '240 patent in violation of 35 U.S.C. § 271(b). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

121. The Accused Products meet all the limitations of at least claim 6 of the '240 patent. Specifically, claim 6 of the '240 patent recites:

6. A system for storing data comprising:

at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and

a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;

wherein the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks; and

wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;

wherein the controller is further adapted to maintain a count value of those blocks that are accessed most frequently and, on a periodic basis when the count value is a predetermined count value, transfer the contents of those counted blocks into the SLC non-volatile memory module, wherein the counted blocks transferred to after reaching the predetermined count value are determined in accordance with the next equivalent range of physical addresses determined by the controller.

Ex. C, '240 patent at 8:20-59.

122. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

123. The Accused Products include at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks. As explained in Count I above, the Accused Products store certain data in MLC memory with individually erasable blocks, for example as part of an SLC caching or direct-to-TLC system.

124. The Accused Products include at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks. As explained in Count I above, the Accused Products store certain data in SLC memory with individually erasable blocks, for example as part of an SLC caching system.

125. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller

maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module. For example, as explained in Count I above, the Accused Products provide mapping between logical and physical addresses using a data structure such as a L2P table, and these mappings have a minimum quanta such as a page.

126. In the Accused Products, the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks. For example, as explained in Count I above, frequently written blocks are allocated and their contents transferred to SLC, and infrequently written data is moved to MLC through copyback/garbage collection and other procedures.

127. In the Accused Products, the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module. For example, as explained in Count I above, the controllers in the Accused Products perform a variety of data integrity functions, and remap data to SLC memory upon the failure of a data integrity test.

128. In the Accused Products, the controller is adapted to maintain a count value of those blocks that are accessed most frequently and, on a periodic basis when the count value is a

predetermined count value, transfer the contents of those counted blocks into the SLC non-volatile memory module, wherein the counted blocks transferred to after reaching the predetermined count value are determined in accordance with the next equivalent range of physical addresses determined by the controller. For example, as explained in Count I above, the Accused Products employ various types of block counting, and transfer the contents of frequently written blocks to the next available locations in SLC based on the count value.

129. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

130. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

131. Defendants indirectly infringe the '240 patent, as provided in 35 U.S.C. § 271(b), including by inducing infringement by third parties such as computer manufacturers—*e.g.*, Dell, Apple, or Lenovo. The third parties who make, have made, use, have used, import, have imported, export, have exported, offer to sell, have offered to sell, sell, and/or have sold products that incorporate SK Accused Products have directly infringed and continue to directly infringe each of the claims as specified above. On information and belief, and based on the websites and marketing information cited herein, SK induces this direct infringement through its affirmative acts of manufacturing, selling, distributing, and/or otherwise making available the Accused Products to third parties, and providing direction, instruction, documentation, and other information to third parties suggesting they use the Accused Products in an infringing manner. SK performs these

affirmative acts with knowledge or willful blindness of the '240 patent and with the intent, or willful blindness, that the induced third parties directly infringe the '240 patent.

132. Defendants' infringement is willful. As described under Count I above, Defendants were aware of Vervain's patents and of their infringement. Defendants have continued their infringing conduct and disregarded an objectively high likelihood of infringement. Defendants' infringing activities have been, and continue to be, willful, wanton, and deliberate, such that Vervain is entitled to enhanced damages under 35 U.S.C. § 284.

133. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '240 patent by Defendants.

134. Vervain is entitled to all rights to recover for present, past, and future infringement for each of the patents-in-suit. Vervain is entitled to recover to the full extent allowable under 35 U.S.C. §§ 284-287, including for up to six years prior to the filing of the complaint. There is no marking issue under 35 U.S.C. § 287 or otherwise which would limit damages, and Vervain has complied with all relevant statutes for maximum recovery under the law.

COUNT IV: INFRINGEMENT OF U.S. PATENT NO. 10,950,300

135. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

136. SK has directly infringed and continues to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '300 patent by making, using, offering for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). SK has also induced infringement of at least claim 1 of the '300 patent in violation of 35 U.S.C. § 271(b). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing

activities, products, and services, including, for example, on the basis of information obtained during discovery.

137. The Accused Products meet all the limitations of at least claim 1 of the '300 patent.

Specifically, claim 1 of the '300 patent recites:

A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space;

at least one controller to operate memory elements and associated memory space;

at least one MLC nonvolatile memory element that can be mapped into the MLC memory space;

at least one SLC nonvolatile memory element that can be mapped into the SLC memory space;

at least one random access volatile memory;

an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory;

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory;

the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation is performed thereon by comparing the stored data to the retained data in the random access volatile memory;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical

addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

Ex. D, '300 patent at 7:36-8:12.

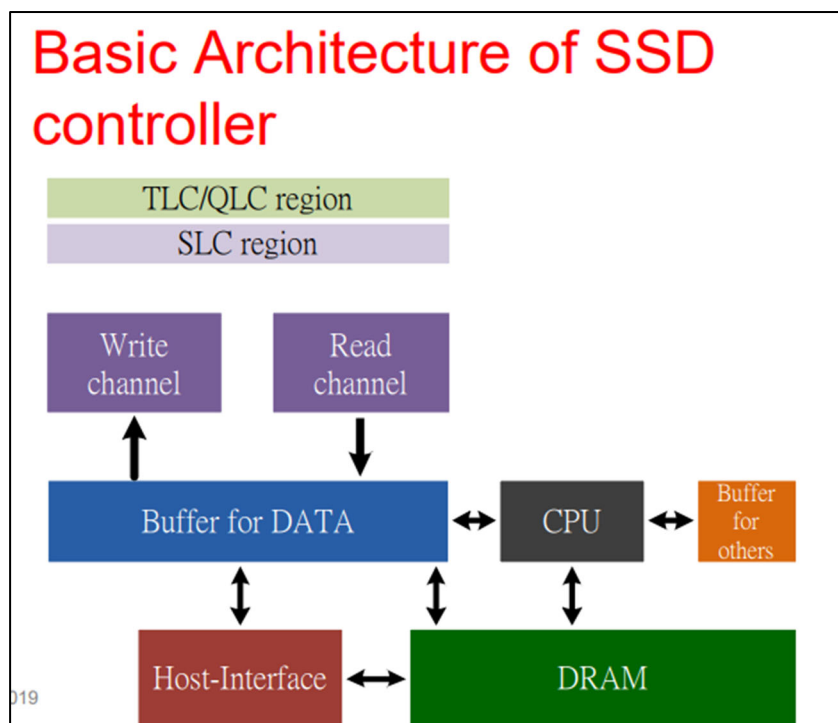
138. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

139. The Accused Products include memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space. For example, as explained in Count I above, the Accused Products include MLC and SLC memory. These locations are mapped to memory space:

How GC processes data

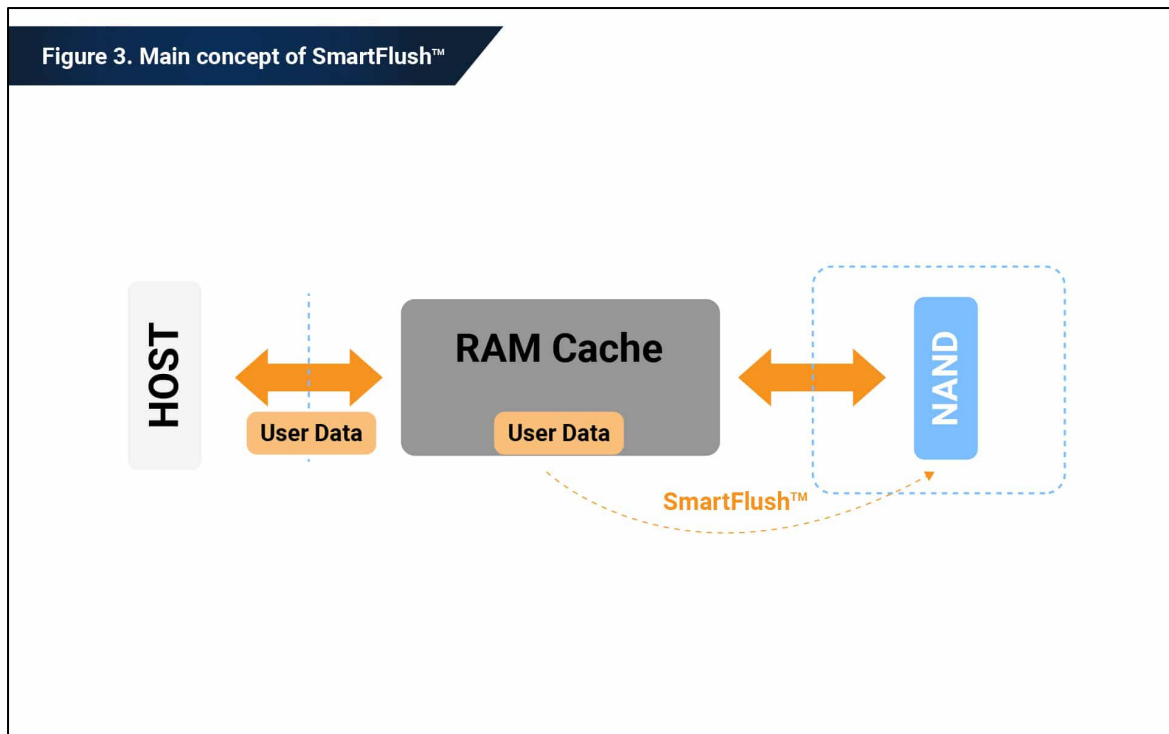
Since SSDs cannot overwrite existing data in NAND memory cells, they must first erase old data before programming new data to the same location. GC is the process of relocating existing data to new locations within free memory space and allowing the surrounding invalid data to be erased thoroughly.

Ex. GG, <https://phisonblog.com/ssd-garbage-collection/>.



Ex. HHH, https://www.flashmemorysummit.com/Proceedings2019/08-05-Monday/20190805_PreConfG_Yang.pdf, at 3.

In addition, both Phison and Silicon Motion controllers use RAM caching to store user data and metadata in RAM (volatile) memory:



Ex. KKK, <https://phisonblog.com/smartflush/>.

**DRAM cache with data redundancy:
no data loss during data transfers**

Silicon Motion's new PCIe FerriSSD features an embedded DRAM which has a self-error detection and correction code (ECC) capability. This DRAM provides for secure, frequent read/write cache requests, and stores logical-to-physical address mapping information.

When the PCIe FerriSSD communicates with the host system and data is written to or read from the NAND Flash memory array, the DRAM temporarily stores the internal Flash mapping tables, as well as the user data that is being written or read.

This provides insurance in case a sudden defect occurs in the NAND Flash storage medium during the data programming process: the PCIe FerriSSD can use the redundant data in the DRAM to complete the data programming process to the NAND Flash array without delay to the host, eliminating the risk of data loss during any transfer of data between NAND Flash and host.

Ex. MM,

https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf, at 2.

140. The Accused Products include at least one controller to operate memory elements and associated memory space. The Accused Products include controllers, for example the controllers identified in paragraph 51 above.

141. The Accused Products include at least one MLC nonvolatile memory element that can be mapped into the MLC memory space. For example, as explained in Count I above, the MLC memory in the Accused Products is mapped into a memory space.

142. The Accused Products include at least one SLC nonvolatile memory element that can be mapped into the SLC memory space. For example, as explained in Count I above, the SLC memory in the Accused Products is mapped into a memory space.

143. The Accused Products include at least one random access volatile memory. For example, the Accused Products include RAM. Certain of the Accused Products, including at least the Platinum P41, PE6011, PC801, PC601, Gold S31, Gold P31, P44 Pro, D7-P5510, and D7-P5430, include a type of RAM called DRAM.²⁴

A Closer Look at Solidigm P44 Pro



(Image credit: Tom's Hardware)

The Solidigm P44 Pro looks almost identical to the Platinum P41. It's a single-sided drive with a controller, DRAM, and two NAND packages.

Ex. LLL, <https://www.tomshardware.com/reviews/solidigm-p44-pro-ssd-review>.

The SK hynix Gold P31 NVMe SSD contains their own proprietary NVMe 4-channel SSD controller, code named the Cepheus Controller, two pieces of the world's first 4D 128-layer TLC NAND flash memory with SLC caching and the SK hynix DRAM cache memory. It is a single-sided SSD.

²⁴ Ex. AA, <https://www.techpowerup.com/ssd-specs/?f=mfg SK%20Hynix>; Ex. BB, <https://www.techpowerup.com/ssd-specs/?f=mfg Solidigm>.

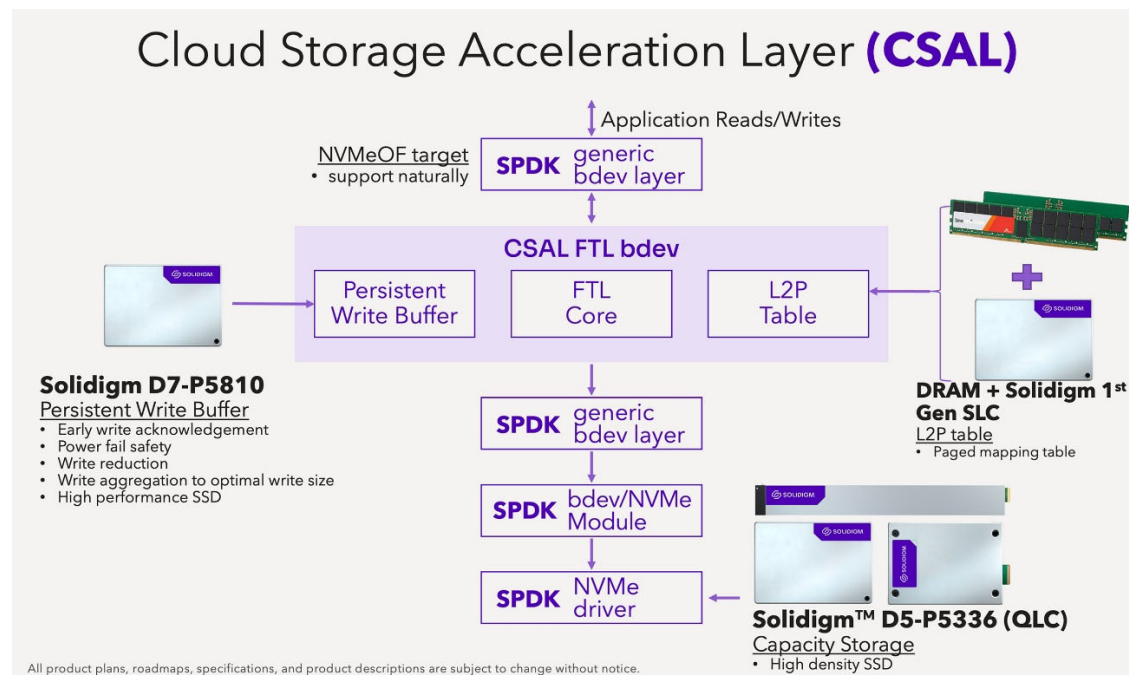
Ex. II, <https://www.thessdreview.com/our-reviews/nvme/sk-hynix-gold-p31-1tb-nvme-ssd-review-worlds-1st-128-layer-ssd-performs-at-an-amazing-price/>.



Inside their aluminum chassis, which is smooth all around and doesn't feature integrated heatsink fins like the D7-series (from both Intel and Solidigm), these drives feature some DRAM (16GB in the case of the 15.36GB model), in addition to the controller and NAND, and capacitors that enable full

Ex. MMM, <https://hothardware.com/reviews/solidigm-ssd-d5-p5430-data-center-ssd-review>.

Finally, SK instructs users to combine many of the Accused Products with a host system that has available random access memory and a flash translation layer:



Ex. NNN, <https://www.solidigm.com/products/technology/cloud-storage-acceleration-layer-write-shaping-csal.html>.

144. The Accused Products' controllers also include other types of random access volatile memory, such as static RAM ("SRAM").

145. The Accused Products that utilize Phison and Silicon Motion controllers use RAM for a variety of purposes, including to store user data and metadata in RAM (volatile) memory and as a backup for data.

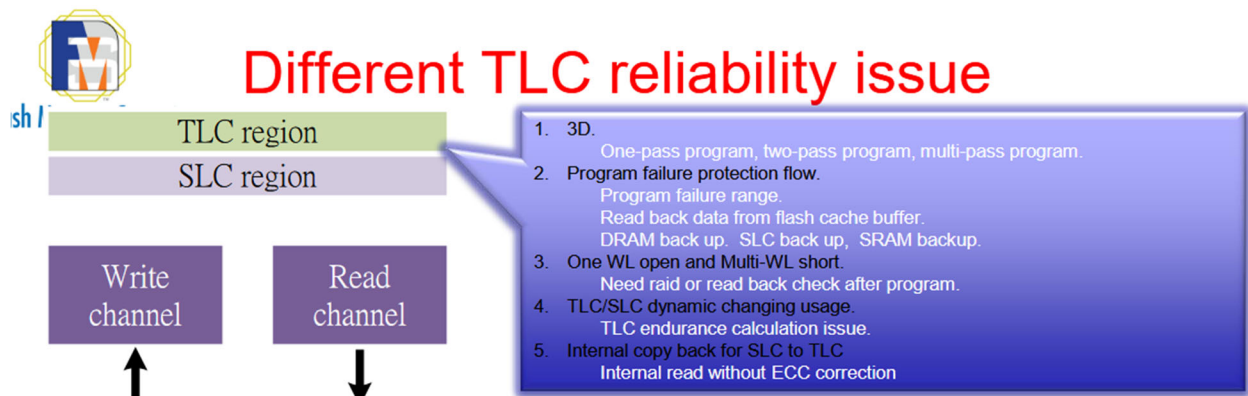
**DRAM cache with data redundancy:
no data loss during data transfers**

Silicon Motion's new PCIe FerriSSD features an embedded DRAM which has a self-error detection and correction code (ECC) capability. This DRAM provides for secure, frequent read/write cache requests, and stores logical-to-physical address mapping information.

When the PCIe FerriSSD communicates with the host system and data is written to or read from the NAND Flash memory array, the DRAM temporarily stores the internal Flash mapping tables, as well as the user data that is being written or read.

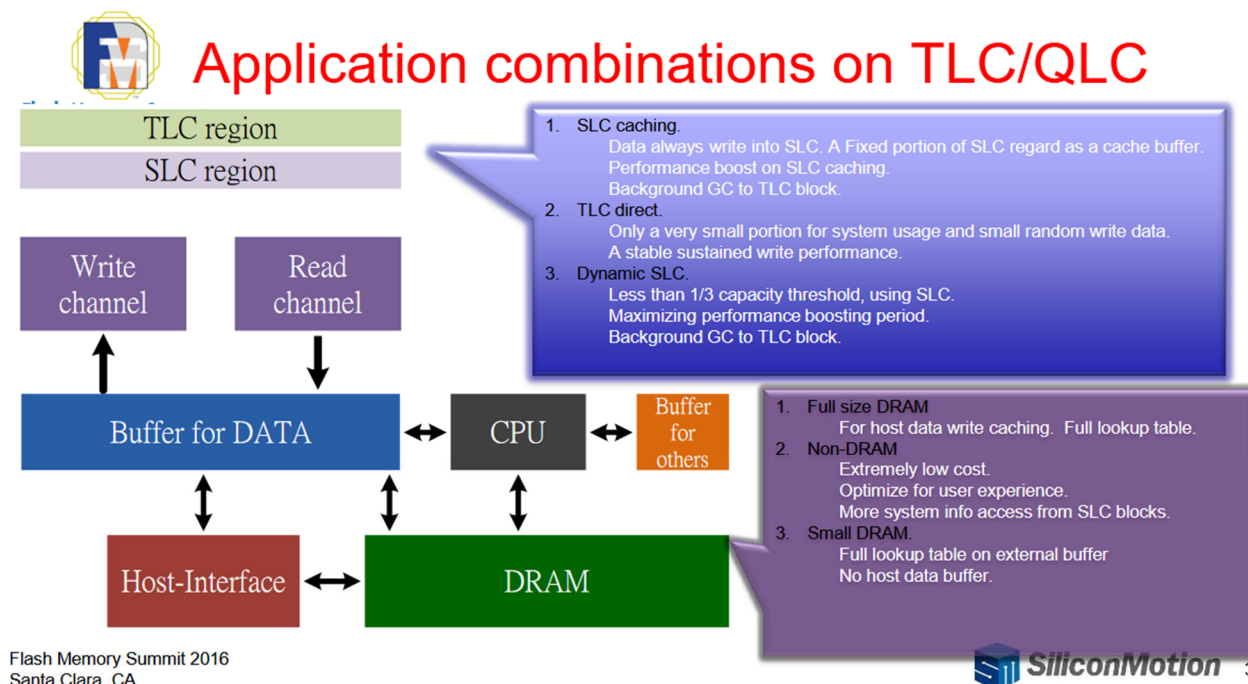
This provides insurance in case a sudden defect occurs in the NAND Flash storage medium during the data programming process: the PCIe FerriSSD can use the redundant data in the DRAM to complete the data programming process to the NAND Flash array without delay to the host, eliminating the risk of data loss during any transfer of data between NAND Flash and host.

Ex. MM, https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf, at 2.



Ex. OOO,

https://files.futurememorystorage.com/proceedings/2017/20170807_PreConfH_Yang.pdf, at 4.



Ex. OOO,

https://files.futurememorystorage.com/proceedings/2017/20170807_PreConfH_Yang.pdf, at 3.

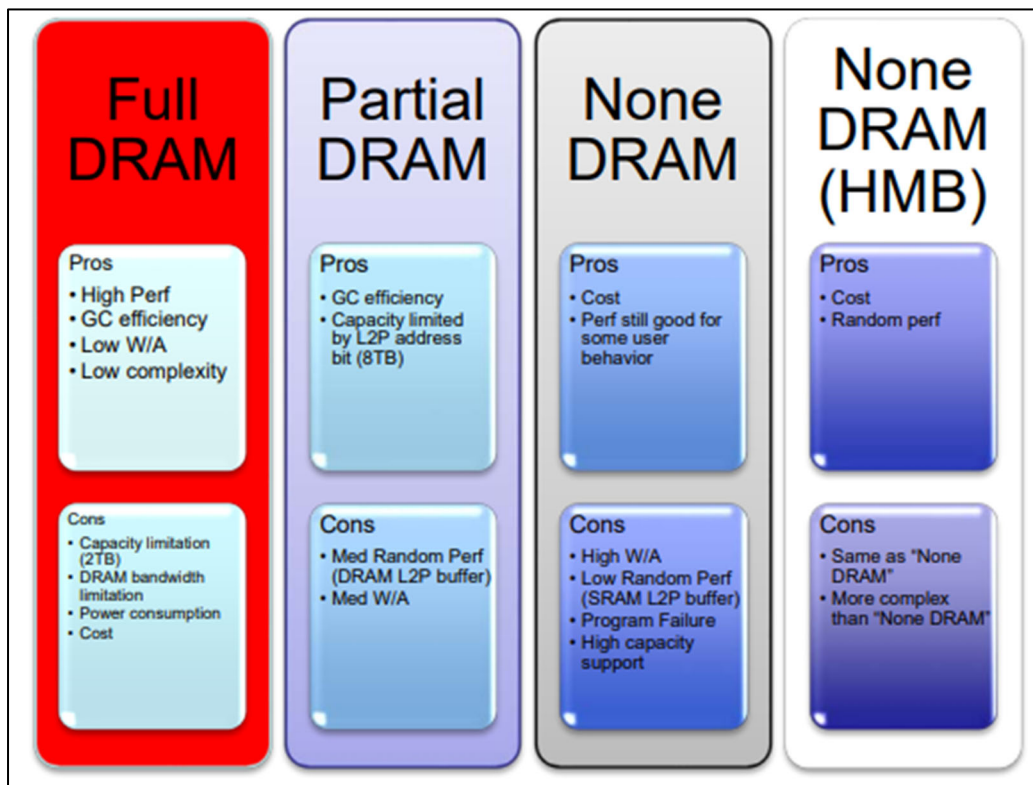
146. The Accused Products include an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory. As explained with respect to Counts I and II above, the Accused Products include an FTL flash translation layer with an L2P table. Phison explains that the L2P table is stored in flash memory and in DRAM:

The most important information that gets cached to or retrieved from a DRAM is the mapping information that turns logical addresses into the physical locations of stored data within the NAND flash array. This information is stored in mapping tables called L2P (logical-to-physical) tables and is updated frequently as SSDs move data in and out of flash storage. During shutdowns, the L2P table is stored in flash memory, since DRAM quickly becomes inoperable without a continuous power supply.

On the other hand, during powered-on scenarios, the L2P table is uploaded to DRAM so that it can be constantly updated by the controller. The larger the DRAM size, the more free space available for the controller to play with. This generally means more flexible data placement and thus better reaction time upon receiving commands. In terms of typical data workloads, operations that call for so-called "random read" sequences benefit the most from ample DRAM space.

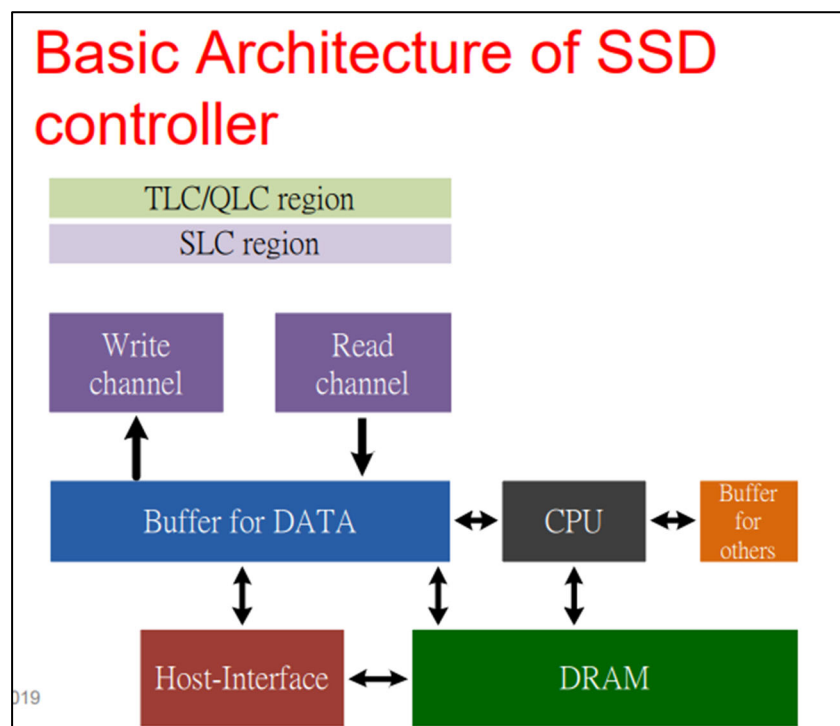
Ex. KK, <https://phisonblog.com/host-memory-buffer-2/>.

Similarly, for Silicon Motion controllers, the L2P table stored in Flash may be cached in DRAM or SRAM:



Ex. HHH, https://www.flashmemorysummit.com/Proceedings2019/08-05-Monday/20190805_PreConfG_Yang.pdf, at 8.

147. The Accused Products include a controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory. For example, the controller in the Accused Products controls access to the MLC and SLC memory and the DRAM, storing data in the flash memory and retaining data in the DRAM:



Ex. HHH, https://www.flashmemorysummit.com/Proceedings2019/08-05-Monday/20190805_PreConfG_Yang.pdf, at 3.

**DRAM cache with data redundancy:
no data loss during data transfers**

Silicon Motion's new PCIe FerriSSD features an embedded DRAM which has a self-error detection and correction code (ECC) capability. This DRAM provides for secure, frequent read/write cache requests, and stores logical-to-physical address mapping information.

When the PCIe FerriSSD communicates with the host system and data is written to or read from the NAND Flash memory array, the DRAM temporarily stores the internal Flash mapping tables, as well as the user data that is being written or read.

This provides insurance in case a sudden defect occurs in the NAND Flash storage medium during the data programming process: the PCIe FerriSSD can use the redundant data in the DRAM to complete the data programming process to the NAND Flash array without delay to the host, eliminating the risk of data loss during any transfer of data between NAND Flash and host.

Ex. MM,

https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf, at 2.

148. In the Accused Products, the controller performs a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation is performed thereon by comparing the stored data to the retained data in the random access volatile memory. For example, the controller in the Accused Products performs a data integrity test by comparing data stored in the flash memory with data retained in RAM. For instance, the controller compares data—either user data or data from the logical-to-physical (L2P) table—in RAM with that stored in the NAND flash memory and uses the data to eliminate the risk of data loss in case of any error.

**DRAM cache with data redundancy:
no data loss during data transfers**

Silicon Motion's new PCIe FerriSSD features an embedded DRAM which has a self-error detection and correction code (ECC) capability. This DRAM provides for secure, frequent read/write cache requests, and stores logical-to-physical address mapping information.

When the PCIe FerriSSD communicates with the host system and data is written to or read from the NAND Flash memory array, the DRAM temporarily stores the internal Flash mapping tables, as well as the user data that is being written or read.

This provides insurance in case a sudden defect occurs in the NAND Flash storage medium during the data programming process: the PCIe FerriSSD can use the redundant data in the DRAM to complete the data programming process to the NAND Flash array without delay to the host, eliminating the risk of data loss during any transfer of data between NAND Flash and host.

Ex. MM,

https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf, at 2.

**Full end-to-end data path protection:
no bit errors sent to host**

Conventional SSDs may employ error detection and correction circuitry at the far ends of the data path: at the front-end host interface and at the back-end

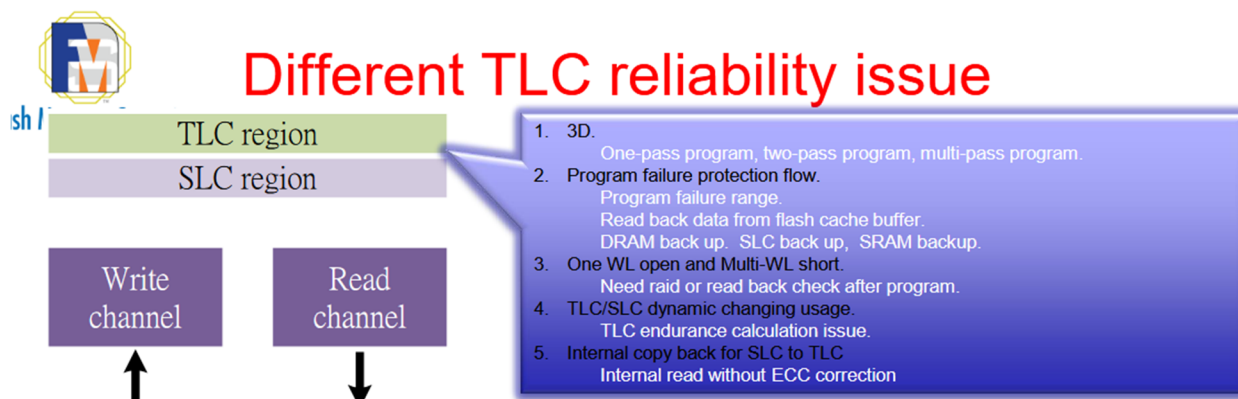
NAND interface. This omits an important gap at the internal SRAM and/or DRAM transfer buffers, and other circuit paths. Data errors that occur between the NAND interface and the host, such as soft error bits, are often extremely difficult to identify and duplicate.

While conventional SSDs may have some internal error detection circuitry, the new PCIe FerriSSD storage solutions incorporate full data recovery engines to provide enhanced data integrity throughout the entire Host-to-NAND-to-Host data path.

The PCIe FerriSSD data recovery algorithm can effectively detect any error in the SSD data path, including hardware errors, firmware errors and memory errors arising in SRAM, DRAM or NAND. The PCIe FerriSSD implements an additional redundant back-up in NAND – the SMI Ferri Group Page Raid – which reinforces the protection against the risk of uncorrectable error in the NAND storage medium.

Ex. MM,

https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf, at 2.



Ex. OOO,

https://files.futurememorystorage.com/proceedings/2017/20170807_PreConfH_Yang.pdf, at 4.

NANDXtend™ Technology

The SM2259 and SM2259XT employs the company's proprietary NANDXtend™ ECC technology consisting of LDPC hard and soft decoding as well as RAID protection that together enhance the P/E cycles of 3D NAND - extending the SSD lifespan and ensuring data integrity. The new generation NANDXtend™ includes 2KB LDPC engine with advanced firmware algorithm delivers higher power efficiency, decoding efficiency and correction capability to maintain consistent data throughout and provide a better user experience, even as error bits increase throughout the product lifecycle of NAND Flash.



Ex. FF, https://www.siliconmotion.com/download/q/a/SM2259_XT_PB_EN_201910.pdf.

Silicon Motion's SM689 and SM681 FerriSSDs supports enhanced reliability and data integrity features for use in demanding automotive, commercial, enterprise and industrial applications. Its set of features includes:

- End-to-end data path protection, which applies error correction code (ECC) to the SSD's SRAM and DRAM buffers as well as to the primary NAND Flash memory array
- DRAM data cache to ensure data programming and enable data redundancy, without delaying host processor operations
- Hybrid Zone which enables a single disk to be partitioned into single-level cell (SLC) and multi-level cell/three-level cell (MLC/TLC) zones, enabling faster access speeds and data retention
- Intelligent Scan/DataRefresh protects against the higher data loss from operating at high temperatures
- NANDXtend™ technology incorporating Silicon Motion's proprietary 4th generation high-performance LDPC ECC engine with RAID, ensuring better data integrity even in extreme physical environments

Ex. XX, <https://www.prnewswire.com/news-releases/silicon-motion-announces-worlds-first-pcie-nvme-single-chip-ssds-with-enterprise-grade-data-protection-features-300604092.html>.

End to End Data Path Protection

Silicon Motion's SSD controller solutions incorporate full data error detection with recovery engines to provide enhanced data integrity throughout the entire Host-to-NAND-to-Host data path. The data recovery algorithm can effectively detect any error in the SSD data path, including hardware (i.e. ASIC) errors, firmware errors, and memory errors arising in SRAM, DRAM, or NAND.

Ex. YY, <https://www.siliconmotion.com/products/client/detail>.

149. Likewise, SK's proprietary controllers retain stored data in RAM, including for use in data integrity checks. While public documentation is limited, SK's patent applications disclose this functionality. For example, U.S. Patent Application Pub. No. 2024/0289040, discussed under Count I above, states:

[0034] In some embodiments, the local memory processor **218** temporarily stores data to be written into, or data read from, the memory channels **204** in an SRAM buffer **224** of the controller **202**. Alternatively, in some embodiments, the local memory processor **218** is coupled to the HMB controller **226**, and temporarily stores the data to be written into, or the data read from, the memory channels **204** in a host memory buffer (HMB) **228** via the HMB controller **226** or host interface controller **222**. The HMB **228** is external to the controller **202**, and is main memory used by the processor module **102** (FIG. 1). In some embodiments, the HMB **228** is one of SRAM, DRAM, 3D XPOINT, and magnetoresistive RAM (MRAM), or other RAM devices. Further, in some embodiments, the memory system **200** includes an SSD coupled to a DRAM based HMB **228**. Alternatively, in some embodiments, the memory system **200** includes an SSD coupled to an HMB **228**, which does not include DRAM.

Ex. AAA, U.S. Pat. App. Pub. No. 2024/0289040, [0034].

data **304** includes a plurality of integrity data items. The user data **302** and the integrity data **304** are temporarily stored in an SRAM buffer **224** of a controller **202** of a memory system **200** (e.g., an SSD **112**) or an HMB **228** external to the controller **202** (FIG. 2). In some embodiments, the user data **302** and the integrity data **304** are stored in two separate regions of the SRAM buffer **224**. After storing the user data **302** and the integrity data **304** temporarily in the SRAM buffer **224** or the HMB **228**, the controller **202** moves the user data **302** and the integrity data **304** into the memory block **306** of the memory system **200** (e.g., an SSD **112**). In some situations, the memory block **306** is entirely filled with the user data **302** and the integrity data **304** copied from the SRAM buffer **224** or the HMB **228**. Alternatively, in some

Ex. AAA, U.S. Pat. App. Pub. No. 2024/0289040, [0035].

validation in a memory system (e.g., SSDs, HDDs). User data and associated integrity data is stored in two distinct memory blocks that are located in two distinct memory blocks of the memory system. After the user data and integrity data is stored, the user data is read back, and validity of the user data is checked with respect to the integrity data. In accordance with a validation of the user

Ex. AAA, U.S. Pat. App. Pub. No. 2024/0289040, [0003].

150. In the Accused Products, the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories. For example, the Accused Products' controllers employ wear leveling and garbage collection techniques that transfer blocks within the flash memory in a way that maximizes lifetime.

Special Features	Trim Support Supported	S.M.A.R.T Support Supported	GC (Garbage Collection) Supported
	Encryption Support AES 256-bit Encryption, TCG Pyrite Supported		Device Sleep Mode Supported

Ex. PPP, https://ssd.skhynix.com/platinum_p41/.

**DRAM cache with data redundancy:
no data loss during data transfers**

Silicon Motion's new PCIe FerriSSD features an embedded DRAM which has a self-error detection and correction code (ECC) capability. This DRAM provides for secure, frequent read/write cache requests, and stores logical-to-physical address mapping information.

Ex. MM,

https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf, at 2.

151. The Accused Products' controllers use a mapping table to keep track of the relationship between the logical blocks and the physical addresses of the flash memory. The controllers use address tables that maximize lifetime using garbage collection, wear leveling, and SLC caching algorithms.

solid-state drives (SSDs). An SSD typically has an address indirection table that maps logical addresses associated with a host device to physical addresses of NAND flash memory in the SSD. Each memory unit of the SSD needs to be addressable in the address indirection table. Memory units can be grouped into larger block sizes and addressed with fewer addresses. However, as a capacity of the SSD increases, its memory units are addressed with more physical addresses, and more bits are inevitably needed to represent each physical address of the SSD. Long physical

Ex. OO, '848 patent at 1:26-35.

FIG. 5A is a diagram of a sequence of physical addresses corresponding to a sequence of logical addresses, in accordance with some embodiments.

FIG. 5B-5D are diagrams of three example data structures of an L2P address indirection table, in accordance with some embodiments.

FIG. 6A is a diagram illustrating a process of extracting a physical address from an L2P address indirection table, in accordance with some embodiments.

FIG. 6B is a diagram illustrating a process of updating a physical address 302 that is stored in an L2P address indirection table, in accordance with some embodiments.

FIG. 7 is a diagram of an example data structure of an L2P address indirection table including integrity data, in accordance with some embodiments.

FIG. 8 is a flow diagram of a method for compressing addresses stored in an L2P address indirection table, in accordance with some embodiments.

Ex. OO, '848 patent at 3:21-38.

In one embodiment, every time a new host block is opened for writing, it is opened in SLC mode. As soon as a write idle threshold is met, the content from SLC blocks are processed/moved (e.g., garbage collected) to TLC blocks. The SLC blocks are simply accounted as if they were TLC block in terms of endurance (i.e., one SLC erase operation is counted as if it is a TLC erase operation). Moreover, TLC

Ex. EEE, '250 patent at 6:59-65.

In contrast to traditional systems that process writes as they are received and therefore mixes data with different lifetimes in the same blocks, in one example, classification engine **130** enables system **100** to separate data based on the lifetime of the data associated with the write requests. In one example, classification engine **130** is a software engine executed on host platform **110**, such as a module of filesystem **126**. In one example, classification engine **130** is a driver of interface **128** that receives data from filesystem **126**, and separates the data into different classes within write buffer **140**. In one example, classification engine is implemented in firmware either in interface hardware. In one example, classification engine **130** is implemented in controller **152** when write buffer **140** is part of nonvolatile storage device **150**.

Ex. PP, '623 patent at 5:8-22.

An SSD may include a static SLC NAND buffer to improve burst write performance for writing data to the SSD followed by writing the data to MLC (for example, TLC or QLC) NAND via direct writes to MLC NAND along with eviction of the data from the static SLC NAND buffer. Another approach for providing faster data access is called dynamic SLC wherein a portion of MLC NAND is used in SLC mode and then dynamically converted to MLC mode when additional user-capacity is needed. Neither of these

techniques account for caching of most frequently accessed data (hot data) in fast media (for example, SLC NAND).

Ex. III, '782 patent at 1:59-2:2.

Block translation in Markers table

In the last step of each case, it's necessary to arrange logical blocks in the Markers table, and in the case of these controllers, this step is quite simple and looks similar for every model of these controllers.

Structures of Service area

SiliconMotion controllers have exactly the same structure of the Service area.



Ex. NN, <https://support.rusolut.com/portal/en/kb/articles/silicon-motion-data-recovery>.

Global wear-leveling to extend
the product life cycle

Ex. YY, <https://www.siliconmotion.com/products/client/detail>.

SILICON MOTION SM2256 CONTROLLER WITH SAMSUNG TLC NAND REVIEW

Sean Webster February 25, 2015 6 Comments

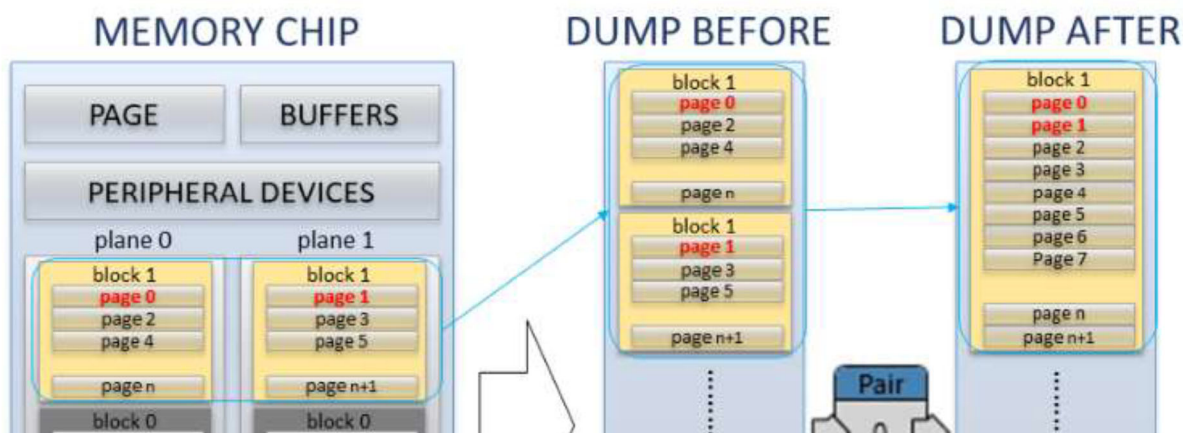
Controllers are the heart and soul of every SSD. Without one, an SSD would be a useless PCB with some components slapped on it. It is responsible for everything from garbage collection and wear leveling to error correction and hardware encryption. In

Ex. QQQ, <https://www.thessdreview.com/our-reviews/silicon-motion-sm2256-controller-with-samsung-tlc-nand-review/>.

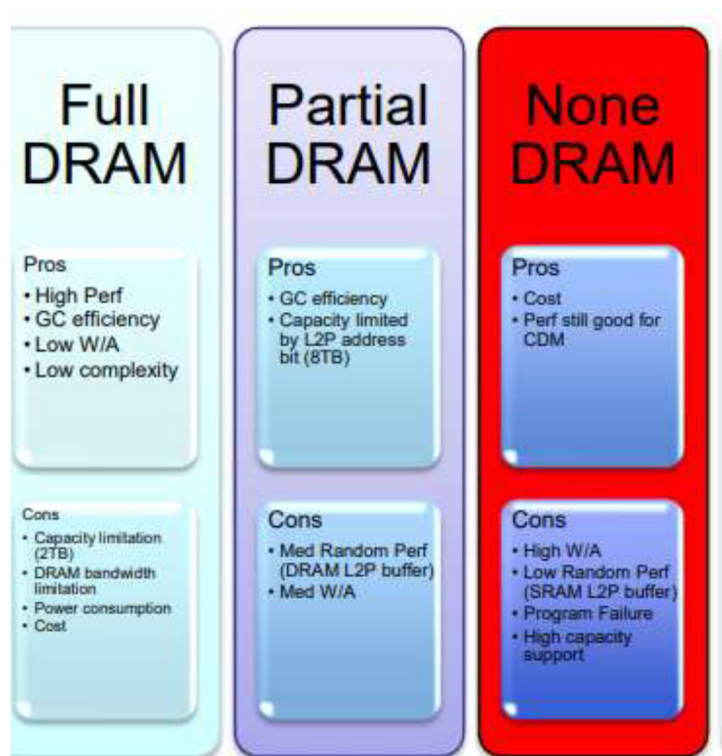
The flash memory is organized by page and block, where a page is the smallest program unit and a block is the smallest erase unit.

Multi-Plane Page allocation

Parallel allocation of physical pages is the most popular mode used by the controllers to speed up I/O operations. While using this mode controller is allocating physical pages parallelly to the planes of NAND memory. This mode is used by the majority of NAND controllers.



Ex. NN, <https://support.rusolut.com/portal/en/kb/articles/silicon-motion-data-recovery>.



Ex. OOO, https://files.futurememorystorage.com/proceedings/2017/20170807_PreConfH_Yang.pdf, at 6-9.

152. In the Accused Products, a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance. For example, the Accused Products remap data to new physical addresses after failing a data integrity test which compared data stored in the flash memory with data retained in the DRAM in order to achieve enhanced endurance. When defects in memory are found, valid data in the cells is rewritten. Because a block cannot be rewritten until it is erased, the valid data is remapped to a different physical range of addresses when writing,

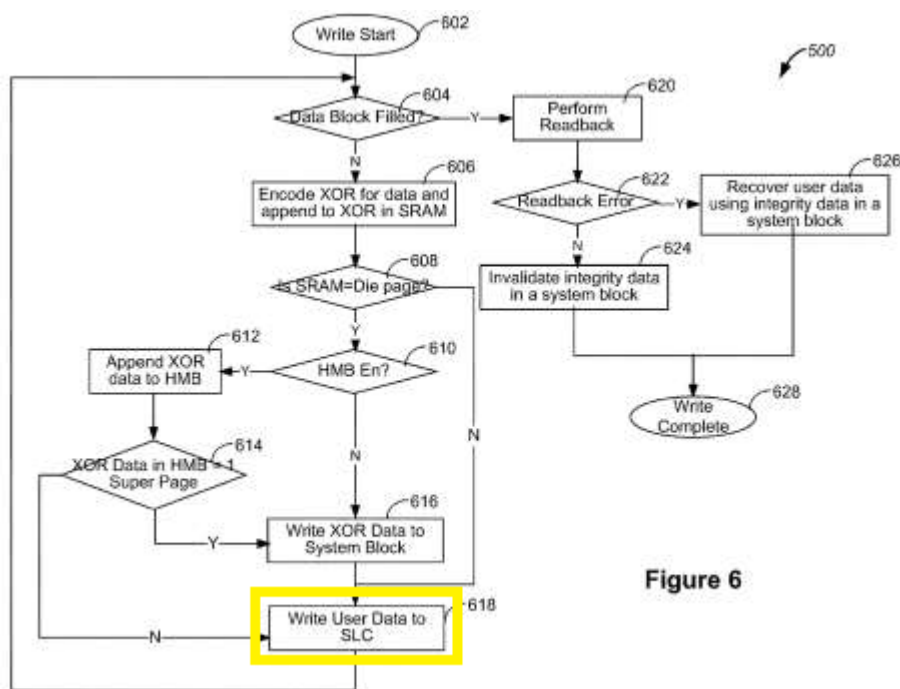
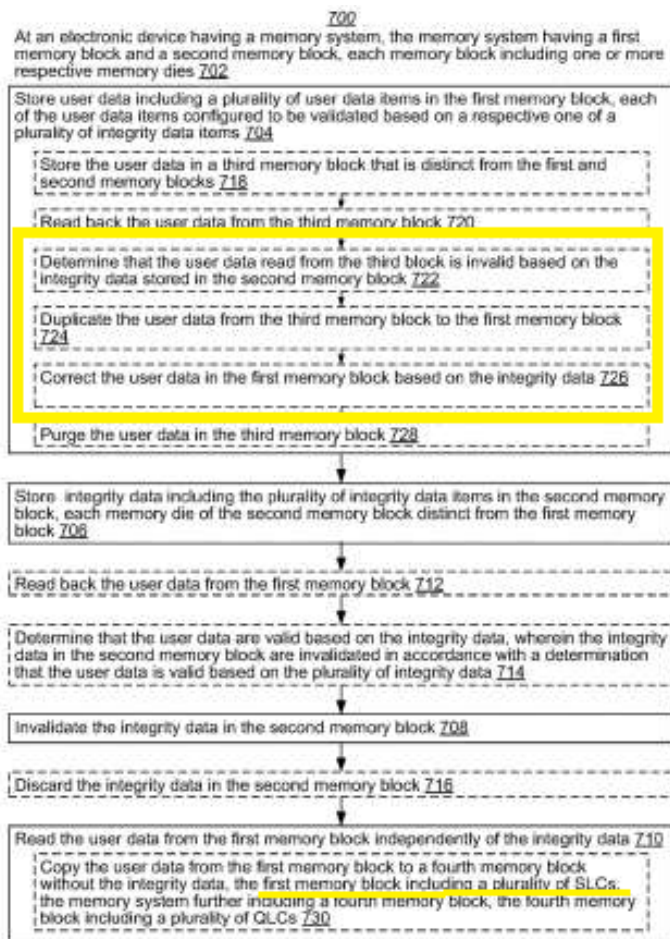


Figure 6

Ex. AAA, U.S. Pat. App. Pub. No. US 2024/0289040, Fig. 6 (highlight added).



Ex. AAA, U.S. Pat. App. Pub. No. US 2024/0289040, Fig. 7 (highlights added).

153. The various data integrity tests and subsequent remapping functionality of the Phison and Silicon Motion controllers is further explained in Count I above.

154. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

155. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

156. Defendants indirectly infringe the '300 patent, as provided in 35 U.S.C. § 271(b), including by inducing infringement by third parties such as computer manufacturers—*e.g.*, Dell, Apple, or Lenovo. The third parties who make, have made, use, have used, import, have imported, export, have exported, offer to sell, have offered to sell, sell, and/or have sold products that incorporate SK Accused Products have directly infringed and continue to directly infringe each of the claims as specified above. On information and belief, and based on the websites and marketing information cited herein, SK induces this direct infringement through its affirmative acts of manufacturing, selling, distributing, and/or otherwise making available the Accused Products to third parties, and providing direction, instruction, documentation, and other information to third parties suggesting they use the Accused Products in an infringing manner. SK performs these affirmative acts with knowledge or willful blindness of the '300 patent and with the intent, or willful blindness, that the induced third parties directly infringe the '300 patent.

157. Defendants' infringement is willful. As described under Count I above, Defendants were aware of Vervain's patents and of their infringement. Defendants have continued their infringing conduct and disregarded an objectively high likelihood of infringement. Defendants' infringing activities have been, and continue to be, willful, wanton, and deliberate, such that Vervain is entitled to enhanced damages under 35 U.S.C. § 284.

158. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '300 patent by Defendants.

159. Vervain is entitled to all rights to recover for present, past, and future infringement for each of the patents-in-suit. Vervain is entitled to recover to the full extent allowable under 35 U.S.C. §§ 284-287, including for up to six years prior to the filing of the complaint. There is no

marking issue under 35 U.S.C. § 287 or otherwise which would limit damages, and Vervain has complied with all relevant statutes for maximum recovery under the law.

COUNT V: INFRINGEMENT OF U.S. PATENT NO. 11,830,546

160. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

161. SK has directly infringed and continues to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '546 patent by making, using, offering for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). SK has also induced infringement of at least claim 1 of the '546 patent in violation of 35 U.S.C. § 271(b). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

162. The Accused Products meet all the limitations of at least claim 1 of the '546 patent. Specifically, claim 1 of the '546 patent recites:

A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space for associated Write access operations to the memory elements and Read access operations from the memory elements;

a bank of nonvolatile memory, including:

a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element, and

at least one SLC memory module including at least one SLC nonvolatile memory element;

at least one random access volatile memory element;

a flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the memory elements;

the controller having associated controller memory for storing received data therein, the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of the received data therein as stored data, the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one of the MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile memory as retained data associated with stored data;

the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after the at least a Write access operation performed thereon by reading the stored data to the controller memory and comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed on the stored data by the controller results in a remapping of address space to a different physical range of addresses and transfer of data corresponding to the retained data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test.

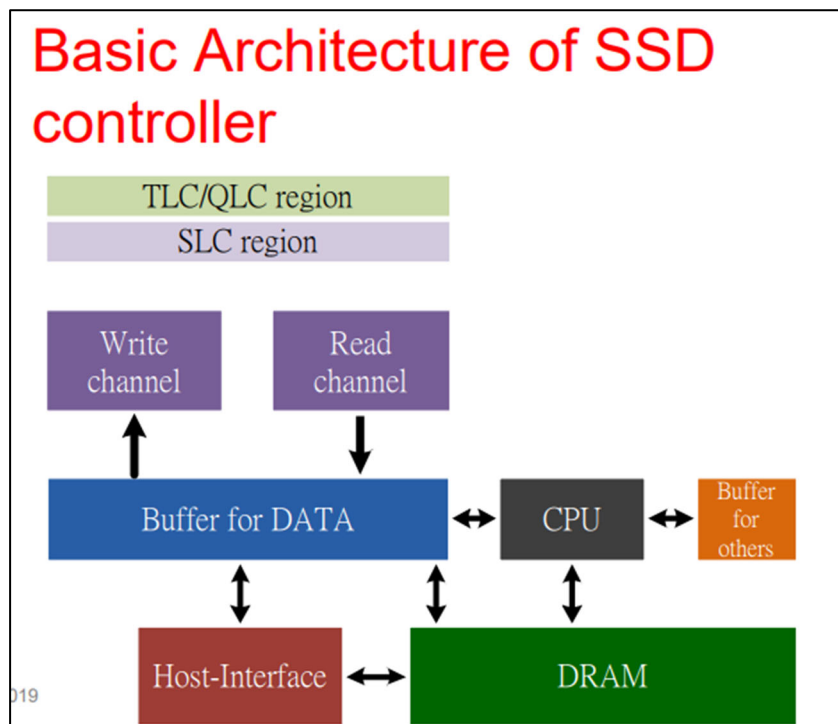
Ex. E, '546 patent at 7:27-8:34.

163. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

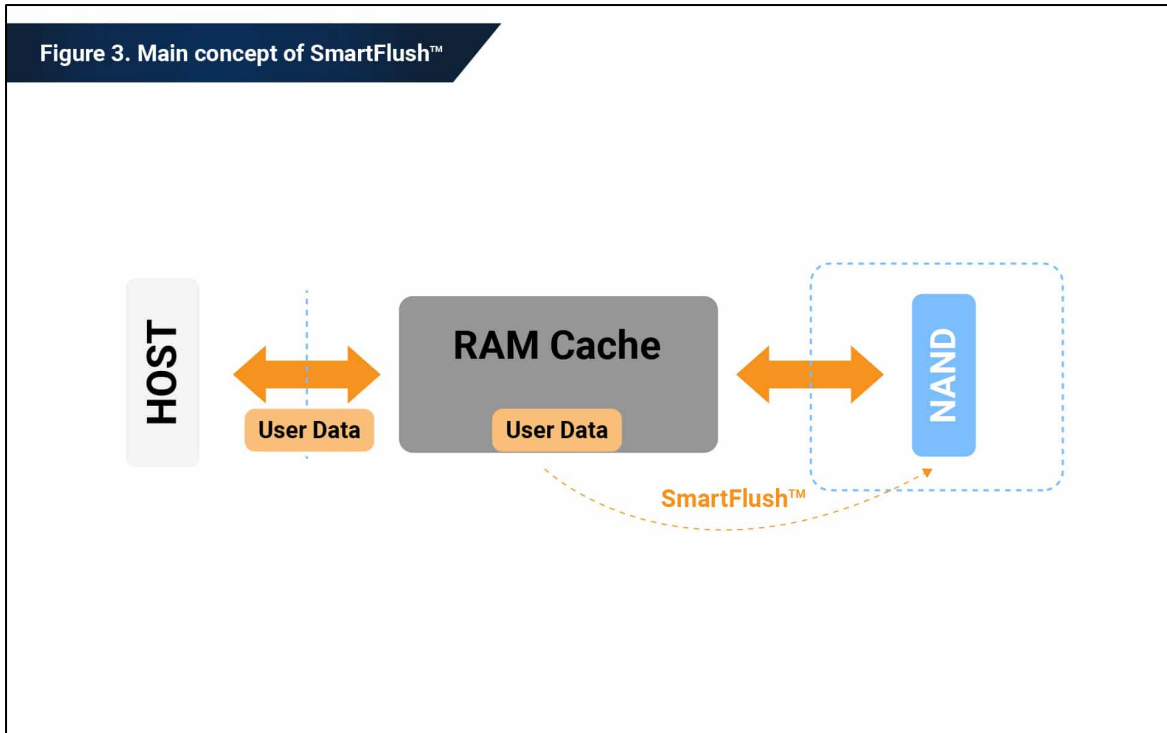
164. The Accused Products include memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level

cell (MLC) space and single level cell (SLC) space. For example, as explained in Count IV above, SK's products use both MLC and SLC memory space, as well as volatile memory space (*e.g.*, for RAM).

165. The Accused Products include at least one controller to operate memory elements and associated memory space for associated Write access operations to the memory elements and Read access operations from the memory elements. For example, the controllers in the Accused Products handle read and write operations to flash memory.



Ex. HHH, https://www.flashmemorysummit.com/Proceedings2019/08-05-Monday/20190805_PreConfG_Yang.pdf, at 3.



Ex. KKK, <https://phisonblog.com/smartflush/>.

166. The Accused Products include a bank of nonvolatile memory, including a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element, and at least one SLC memory module including at least one SLC nonvolatile memory element. For example, as explained in Count IV above, the Accused Products include both SLC and MLC nonvolatile memory.

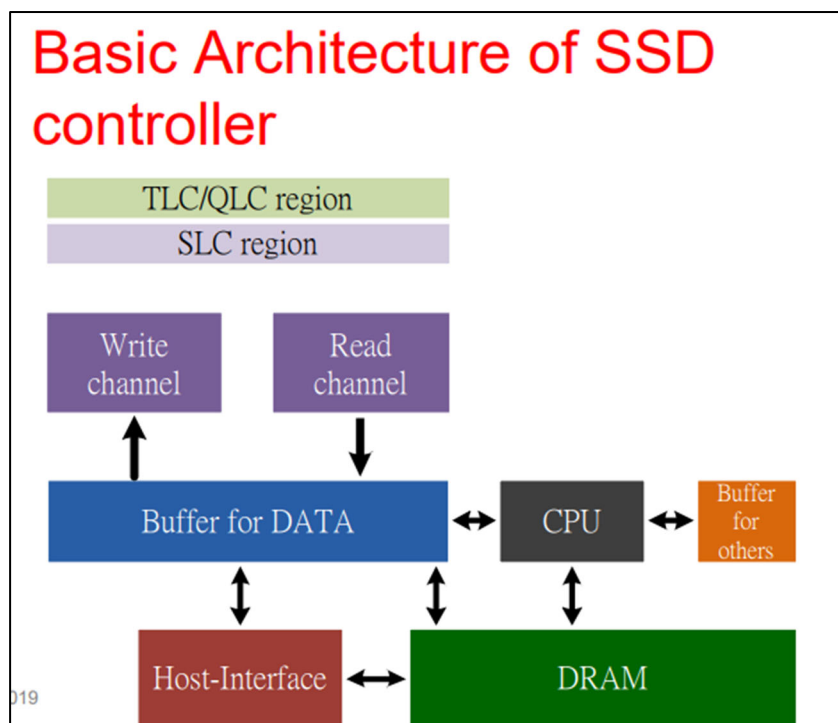
167. The Accused Products include at least one random access volatile memory element. For example, as explained in Count IV above, the Accused Products contain some form of RAM such as DRAM or SRAM. In addition, SK instructs users to combine many of the Accused Products with a host system that has available random access memory and a flash translation layer for the flash storage products' use.

168. The Accused Products include a flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of

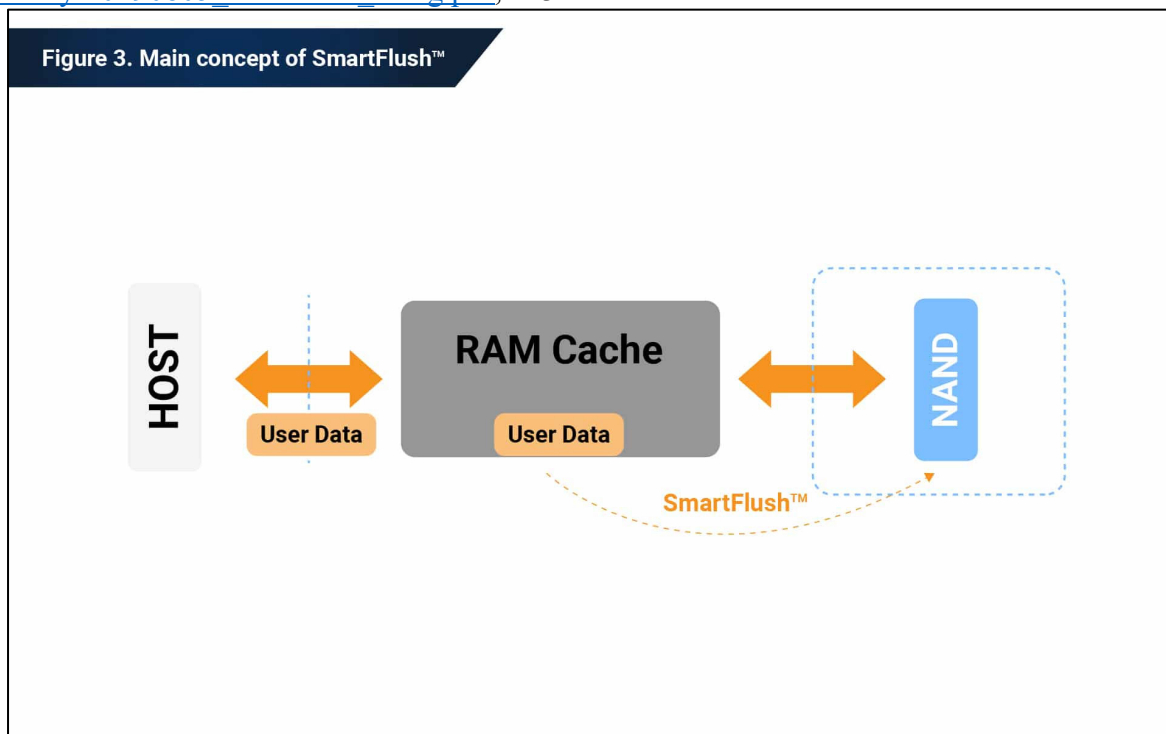
the memory elements. For example, as shown with respect to Count IV above, the Accused Products maintain an address table in flash memory.

169. The controller in the Accused Products has associated controller memory for storing received data therein, the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of the received data therein as stored data, the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one of the MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile memory as retained data associated with stored data. For example, as shown with respect to Count IV above, the Accused Products cache written data in RAM.

170. The controller in the Accused Products performs a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after the at least a Write access operation performed thereon by reading the stored data to the controller memory and comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation. For example, as shown with respect to Count IV above, the Accused Products perform a data integrity test by comparing stored data and retained data. In addition, the controller provides controller memory such as buffers or caches to store retained data:



Ex. HHH, https://www.flashmemorysummit.com/Proceedings2019/08-05-Monday/20190805_PreConfG_Yang.pdf, at 3.



Ex. KKK, <https://phisonblog.com/smartflush/>.

171. In the Accused Products, the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories. For example, as shown with respect to Count IV above, the Accused Products use wear leveling and garbage collection, in conjunction with an L2P table, to map logical and physical addresses as necessitated by the system to maximize lifetime.

172. In the Accused Products, a failure of the data integrity test performed on the stored data by the controller results in a remapping of address space to a different physical range of addresses and transfer of data corresponding to the retained data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test. For example, as shown with respect to Count IV above, data is remapped when it fails the data integrity test after a comparison.

173. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

174. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

175. Defendants indirectly infringe the '546 patent, as provided in 35 U.S.C. § 271(b), including by inducing infringement by third parties such as computer manufacturers—*e.g.*, Dell, Apple, or Lenovo. The third parties who make, have made, use, have used, import, have imported, export, have exported, offer to sell, have offered to sell, sell, and/or have sold products that incorporate SK Accused Products have directly infringed and continue to directly infringe each of

the claims as specified above. On information and belief, and based on the websites and marketing information cited herein, SK induces this direct infringement through its affirmative acts of manufacturing, selling, distributing, and/or otherwise making available the Accused Products to third parties, and providing direction, instruction, documentation, and other information to third parties suggesting they use the Accused Products in an infringing manner. SK performs these affirmative acts with knowledge or willful blindness of the '546 patent and with the intent, or willful blindness, that the induced third parties directly infringe the '546 patent.

176. Defendants' infringement is willful. As described under Count I above, Defendants were aware of Vervain's patents and of their infringement. Defendants have continued their infringing conduct and disregarded an objectively high likelihood of infringement. Defendants' infringing activities have been, and continue to be, willful, wanton, and deliberate, such that Vervain is entitled to enhanced damages under 35 U.S.C. § 284.

177. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '546 patent by Defendants.

178. Vervain is entitled to all rights to recover for present, past, and future infringement for each of the patents-in-suit. Vervain is entitled to recover to the full extent allowable under 35 U.S.C. §§ 284-287, including for up to six years prior to the filing of the complaint. There is no marking issue under 35 U.S.C. § 287 or otherwise which would limit damages, and Vervain has complied with all relevant statutes for maximum recovery under the law.

COUNT VI: INFRINGEMENT OF U.S. PATENT NO. 12,119,054

179. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

180. SK has directly infringed and continues to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '054 patent by making, using, offering for sale,

selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). SK has also induced infringement of at least claim 1 of the '054 patent in violation of 35 U.S.C. § 271(b). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

181. The Accused Products meet all the limitations of at least claim 1 of the '054 patent. Specifically, claim 1 of the '054 patent recites:

A system for storing data comprising:

an MLC non-volatile memory space including at least one MLC non-volatile memory element;

an SLC non-volatile memory module space including at least one SLC non-volatile memory element;

a controller coupled to the at least one MLC non-volatile memory element and the at least one SLC non-volatile memory element wherein the controller is adapted to;

(a) maintain an address map of the MLC and SLC non-volatile memory spaces, the address map comprising a list of logical address ranges accessible by a computer system, the computer system having at least one processor, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory element or within the at least one MLC non-volatile memory element; and

(b) determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory element, fails a data integrity test performed at the controller during a read operation, reading stored data from the MLC non-volatile memory space containing the at least one MLC non-volatile memory element, and, in an event of such a failure, the controller remaps the entry to a next available equivalent range of physical addresses within the at least one SLC non-volatile memory element.

Ex. F, '054 patent at 7:37-67.

182. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

183. The Accused Products include memory space containing nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space. For example, as explained in Counts I and V above, the Accused Products include MLC and SLC memory elements that are mapped to memory space.

184. The Accused Products include at least one controller coupled to the at least one MLC non-volatile memory element and the at least one SLC non-volatile memory element. The Accused Products include controllers, for example the controllers identified in paragraph 51 above, and those controllers are coupled to MLC and SLC non-volatile memory elements as explained in Count I above.

185. The Accused Products' controllers are adapted to maintain an address map of the MLC and SLC non-volatile memory spaces, the address map comprising a list of logical address ranges accessible by a computer system, the computer system having at least one processor, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory element or within the at least one MLC non-volatile memory element. For example, as explained in Counts I and IV above, the controllers perform mapping using L2P tables with a minimum quanta of addresses.

186. The Accused Products' controllers are adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory element, fails a data integrity test performed at the controller during a read

operation, reading stored data from the MLC non-volatile memory space containing the at least one MLC non-volatile memory element, and, in an event of such a failure, the controller remaps the entry to a next available equivalent range of physical addresses within the at least one SLC non-volatile memory element. For example, as explained in Counts I and IV above, the controllers perform a variety of data integrity tests, and a variety of data refresh or remapping operations that write from MLC to SLC in response to data integrity problems.

187. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

188. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

189. Defendants indirectly infringe the '054 patent, as provided in 35 U.S.C. § 271(b), including by inducing infringement by third parties such as computer manufacturers—*e.g.*, Dell, Apple, or Lenovo. The third parties who make, have made, use, have used, import, have imported, export, have exported, offer to sell, have offered to sell, sell, and/or have sold products that incorporate SK Accused Products have directly infringed and continue to directly infringe each of the claims as specified above. On information and belief, and based on the websites and marketing information cited herein, SK induces this direct infringement through its affirmative acts of manufacturing, selling, distributing, and/or otherwise making available the Accused Products to third parties, and providing direction, instruction, documentation, and other information to third parties suggesting they use the Accused Products in an infringing manner. SK performs these

affirmative acts with knowledge or willful blindness of the '054 patent and with the intent, or willful blindness, that the induced third parties directly infringe the '054 patent.

190. Defendants' infringement is willful. As described under Count I above, Defendants were aware of Vervain's patents and of their infringement. Defendants have continued their infringing conduct and disregarded an objectively high likelihood of infringement. Defendants' infringing activities have been, and continue to be, willful, wanton, and deliberate, such that Vervain is entitled to enhanced damages under 35 U.S.C. § 284.

191. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '054 patent by Defendants.

192. Vervain is entitled to all rights to recover for present, past, and future infringement for each of the patents-in-suit. Vervain is entitled to recover to the full extent allowable under 35 U.S.C. §§ 284-287, including for up to six years prior to the filing of the complaint. There is no marking issue under 35 U.S.C. § 287 or otherwise which would limit damages, and Vervain has complied with all relevant statutes for maximum recovery under the law.

COUNT VII: INFRINGEMENT OF U.S. PATENT NO. 12,224,005

193. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

194. SK has directly infringed and continues to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '005 patent by making, using, offering for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). SK has also induced infringement of at least claim 1 of the '005 patent in violation of 35 U.S.C. § 271(b). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing

activities, products, and services, including, for example, on the basis of information obtained during discovery.

195. The Accused Products meet all the limitations of at least claim 1 of the '005 patent. Specifically, claim 1 of the '005 patent recites:

An apparatus for storing data in a nonvolatile memory, the apparatus comprising:

a controller configured to erase a group of physical memory cells in the nonvolatile memory;

the controller configured to write multiple bits of information to each of a first group of physical memory cells in the nonvolatile memory;

the controller configured to map a logical address range to a physical address range for the first group of physical memory cells in the nonvolatile memory;

the controller configured to determine if the first group of physical memory cells fails a data integrity test;

if the first group of physical memory cells fails the data integrity test, the controller writes at least some of the information stored in the first group of physical memory cells to a second group of physical memory cells in the nonvolatile memory, the controller writing a single bit of information per cell in the second group of physical memory cells; and

the controller configured to map the logical address range to a second physical address range for the second group of physical memory cells.

Ex. G, '005 patent at 7:37-8:3.

196. To the extent the preamble is a limitation, the Accused Products include an apparatus for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

197. The Accused Products include at least one controller configured to erase a group of physical memory cells in the nonvolatile memory; to write multiple bits of information to each of a first group of physical memory cells in the nonvolatile memory; and to map a logical address range to a physical address range for the first group of physical memory cells in the nonvolatile

memory. For example, these controller functions of writing, erasing, and mapping, were explained in Counts I and IV above.

198. The Accused Products include at least one controller configured to determine if a group of physical memory cells fail a data integrity test. For example, as explained in Count I above, the controllers include data integrity features such as “IntelligentScan,” “DataRefresh,” “Read disturbance,” and other forms of error correction.

199. The Accused Products’ controllers write data to SLC (i.e., “the second group of physical memory cells” which hold “a single bit of information”) in response to data integrity errors in MLC (i.e., “the first group of physical memory cells” which hold “multiple bits of information”). For example, the controllers employ the SLC write buffer, SLC caching technology, and data refresh features explained in Count I above.

200. The Accused Products’ controllers are configured to map the logical address range to a second physical address range for the second group of physical memory cells. For example, as explained in Count I above, the controllers utilize and maintain address tables such as L2P tables to direct the host to the proper physical blocks following a rewrite operation.

201. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

202. Defendants’ infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

203. Defendants indirectly infringe the ’005 patent, as provided in 35 U.S.C. § 271(b), including by inducing infringement by third parties such as computer manufacturers—*e.g.*, Dell,

Apple, or Lenovo. The third parties who make, have made, use, have used, import, have imported, export, have exported, offer to sell, have offered to sell, sell, and/or have sold products that incorporate SK Accused Products have directly infringed and continue to directly infringe each of the claims as specified above. On information and belief, and based on the websites and marketing information cited herein, SK induces this direct infringement through its affirmative acts of manufacturing, selling, distributing, and/or otherwise making available the Accused Products to third parties, and providing direction, instruction, documentation, and other information to third parties suggesting they use the Accused Products in an infringing manner. SK performs these affirmative acts with knowledge or willful blindness of the '005 patent and with the intent, or willful blindness, that the induced third parties directly infringe the '005 patent.

204. Defendants' infringement is willful. As described under Count I above, Defendants were aware of Vervain's patents and of their infringement. Defendants have continued their infringing conduct and disregarded an objectively high likelihood of infringement. Defendants' infringing activities have been, and continue to be, willful, wanton, and deliberate, such that Vervain is entitled to enhanced damages under 35 U.S.C. § 284.

205. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '005 patent by Defendants.

206. Vervain is entitled to all rights to recover for present, past, and future infringement for each of the patents-in-suit. Vervain is entitled to recover to the full extent allowable under 35 U.S.C. §§ 284-287, including for up to six years prior to the filing of the complaint. There is no marking issue under 35 U.S.C. § 287 or otherwise which would limit damages, and Vervain has complied with all relevant statutes for maximum recovery under the law.

REQUEST FOR A JURY TRIAL

207. Vervain requests a jury trial of all issues in this action so triable.

PRAYER FOR RELIEF

WHEREFORE, Vervain respectfully requests:

- A. That Judgment be entered that Defendants have infringed one or more claims of the Asserted Patents, literally and under the doctrine of equivalents, and indirectly;
- B. The Judgment be entered that Defendants' infringement of the Asserted Patents was willful, and that Defendants' continued infringement is willful;
- C. That, in accordance with 35 U.S.C. § 283, Defendants and all its affiliates, employees, agents, officers, directors, attorneys, successors, and assigns and all those acting on behalf of or in active concert or participation with any of them, be preliminarily and permanently enjoined from (1) infringing the Asserted Patents and (2) making, using, selling, offering for sale, and importing into the United States, the Accused Products;
- D. An award of damages sufficient to compensate Vervain for Defendants' infringement under 35 U.S.C. § 284;
- E. An award of enhanced damages for Defendants' willful patent infringement pursuant to 35 U.S.C. § 284.
- F. That the case be found exceptional under 35 U.S.C. § 285 and that Vervain be awarded its reasonable attorneys' fees;
- G. Costs and expenses in this action;
- H. An award of pre-judgment and post-judgment interest; and
- I. Such other and further relief as the Court may deem just and proper.

Dated: February 3, 2026.

Respectfully submitted,

/s/ Alan L. Whitehurst

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