**PUBLIC VERSION**

[redacted]

**UNITED STATES INTERNATIONAL TRADE COMMISSION**
**WASHINGTON, D.C.**

| **In the Matter of:** | |
|---|---|
| **CERTAIN NAND AND DRAM MEMORY CHIPS** | **Investigation No. 337-TA-____** |

# COMPLAINT OF MONOLITHIC 3D™ INC. UNDER SECTION 337 OF THE TARIFF ACT OF 1930, AS AMENDED

## COMPLAINANT


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[redacted]

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| O | Copy of Prosecution Histories for Priority Application(s) of U.S. Patent No. 11,862,503 |
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## I. INTRODUCTION

1. This Complaint is filed by MonolithIC 3D™ Inc. ("MonolithIC 3D" or "Complainant"), pursuant to Section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337 ("Section 337"), based on the unlawful offer for sale for importation into the United States, sale for importation into the United States, importation into the United States, and/or sale within the United States after importation of certain NAND and DRAM memory chips ("Accused Products") by proposed Respondents: KIOXIA Holdings Corporation, KIOXIA Corporation, KIOXIA America, Inc., KIOXIA Engineering Corporation, KIOXIA Iwate Corporation, KIOXIA Systems Co., Ltd., and KIOXIA Semiconductor Taiwan Corporation (collectively, "KIOXIA"); and SK hynix Inc., SK hynix America Inc., and SK hynix Memory Solutions America Inc. (collectively, "SK hynix") (altogether, the "Proposed Respondents").

2. The Proposed Respondents' Accused Products directly and/or indirectly infringe one or more claims of U.S. Patent Nos. 12,035,531 ("the '531 Patent, attached as **Exhibit 1**), 12,125,737 ("the '1-737 Patent, attached as **Exhibit 2**), 12,243,765 ("the '765 Patent, attached as **Exhibit 3**), 11,342,214 ("the '214 Patent, attached as **Exhibit 4**), 11,476,181 ("the '181 Patent, attached as **Exhibit 5**), 11,594,473 ("the '473 Patent, attached as **Exhibit 6**), 11,862,503 ("the '503 Patent, attached as **Exhibit 7**), and 12,225,737 ("the '2-737 Patent, attached as **Exhibit 8**) (collectively, "the Asserted Patents"), in violation of Section 337(a)(1)(B).

3. The Accused Products directly and/or indirectly infringe at least the following claims of the Asserted Patents in violation of Section 337(a)(1)(B)(i)–(ii) and 35 U.S.C. §§ 271(a)–(c) and (g), either literally or under the doctrine of equivalents:

| Asserted Patent | Asserted Independent Claims | Asserted Dependent Claims |
|---|---|---|
| '531 Patent | **8, 15** | 9, 10, 13, 14, 20 |
| '1-737 Patent | **1, 15** | 2, 4, 5, 7, 16, 17, 18, 20 |
| '765 Patent | **1, 8, 15** | 2, 4, 5, 7, 9, 10, 11, 12, 14 16, 17, 18, 20 |
| '214 Patent | **1, 15** | 2, 3, 4, 5, 7, 16, 17, 18, 20 |
| '181 Patent | **1, 2, 4, 11** | 5, 6, 7, 8, 9, 12, 13, 14, 15 |
| '473 Patent | **1, 5, 9, 13,** | 2, 3, 6, 7, 11, 12, 15, 16 |
| '503 Patent | **1, 15** | 2, 3, 4, 5, 6, 16, 17, 18, 19 |
| '2-737 Patent | **1, 15** | 2, 3, 6, 7, 16, 17, 18, 19, 20 |

4. As required by Sections 337(a)(2)–(3), an industry exists and/or is in the process of being established in the United States as the result of activities and investments in the United States relating to products that practice the Asserted Patents. These activities include the current and ongoing significant and substantial domestic investments in plant, equipment, labor, capital, engineering, and research and development of MonolithIC 3D's licensee, [redacted] and its NAND and DRAM memory products.

5. As set forth in this Complaint, each of the Proposed Respondents imports into the United States, sells for importation into the United States, and/or sells within the United States after importation Accused Products that directly and/or indirectly infringe the Asserted Patents.

6. Complainant seeks limited exclusion orders ("LEO") barring from entry the Accused Products imported, sold for importation, and/or sold within the United States after importation by the Proposed Respondents in violation of Section 337.

7. Complainant also seeks, as relief, permanent cease and desist orders ("CDO") against the Proposed Respondents prohibiting the sale, offer for sale, advertising, marketing, packaging, distribution, maintenance of inventory, or solicitation of any sale of imported Accused Products, whether through traditional "brick and mortar" retailers, distributors, the Internet, or other e-commerce platform(s). Complainant also requests that the Commission impose a bond on the Proposed Respondents' importation of the Accused Products that infringe any claim of the

Asserted Patents to protect Complainant from further injury during the 60-day Presidential review period.

## II. THE PARTIES

### A. Complainant MonolithIC 3D™ Inc.

8. Complainant MonolithIC 3D™ Inc. is a corporation organized and existing under the laws of the State of Texas, with its principal place of business located at 825 Watter's Creek Boulevard, Building M, Suite 250, Allen, Texas 75013.

9. MonolithIC 3D is an innovator in computer memory, logic, and electro-optics. MonolithIC 3D was originally founded and incorporated in 2009 under the name NuPGA by Zvi Or-Bach, the President and CEO of MonolithIC 3D. NuPGA's mission was to develop programmable logic technology with density, speed, and power approaching application-specific integrated circuits ("ASICs"). While developing improved field-programmable gate array ("FPGA") technology, the NuPGA team discovered a path for practical monolithic 3D integrated circuits ("IC"). Recognizing that this breakthrough and its many related innovations represented a paradigm shift for the entire semiconductor industry, Mr. Or-Bach changed the company strategy to focus on monolithic 3D-ICs and renamed the company to MonolithIC 3D™ Inc.

10. MonolithIC 3D's business involves researching, developing, and licensing technology, including NAND and DRAM technology. MonolithIC 3D has more than 300 U.S. patents related to multi-level IC technology, including over 90 U.S. patents related to 3D NAND flash memory technology and over 30 patents related to high bandwidth memory ("HBM") technology.

### B. The Proposed Respondents

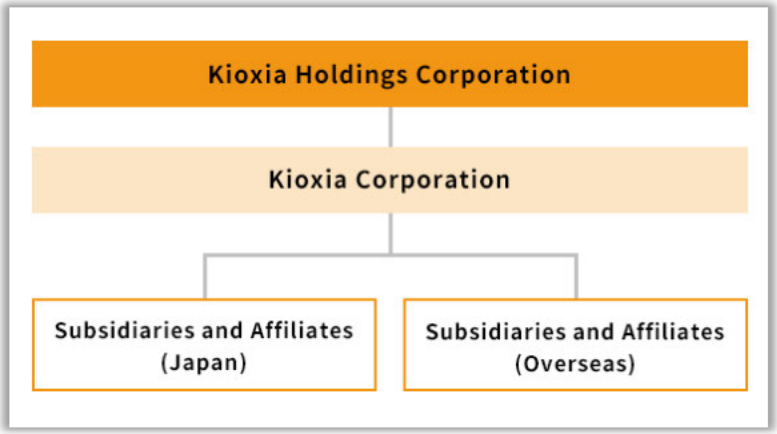
11. On information and belief, the Proposed Respondents include original equipment manufacturers, manufacturers, importers, sellers, re-sellers, and distributors, including agents

[redacted]

therefor, that import, sell for importation, offer for sale, and/or sell within the United States after importation Accused Products that infringe one or more claims of the Asserted Patents.

### 1. The KIOXIA Respondents

12. On information and belief, according to KIOXIA Holdings Corporation's Annual Securities Report from April 1, 2024 to March 31, 2025 (the "KIOXIA Annual Securities Report"), Proposed Respondent KIOXIA Holdings Corporation ("KIOXIA Holdings") is a corporation organized under the laws of Japan with its principal place of business located at 1-21, Shibaura 3-chome, Minato-ku, Tokyo, Japan. *See* **Ex. 9** at 1, 8. On information and belief, KIOXIA Holdings is the parent company of KIOXIA Corporation (and all its subsidiaries and affiliates), which is involved in at least the research, development, design, production, and marketing of KIOXIA's Accused Products:




**Ex. 10** at 2. On information and belief, KIOXIA Holdings is involved in the importation, sale for importation into the United States, and/or sale within the United States after importation of KIOXIA's Accused Products. *See* § V.A, ¶¶ 62–70 *infra*.

13. On information and belief, Proposed Respondent KIOXIA Corporation ("KIOXIA Corp.") is a corporation organized under the laws of Japan with its principal place of business located at 3-1-21, Shibaura, Minato-ku, Tokyo 108-0023, Japan. *See* **Ex. 11** at 1. According to its

website, "KIOXIA Corporation is a wholly-owned subsidiary of KIOXIA Holdings Corporation." **Ex. 12** at 3. According to the KIOXIA Annual Securities Report, KIOXIA Corp. is responsible for the "[r]esearch, development, design, production, and marketing of Memory and SSD products," including KIOXIA's Accused Products. **Ex. 9** at 72. On information and belief, KIOXIA Corp. is involved in the importation, sale for importation into the United States, and/or sale within the United States after importation of KIOXIA's Accused Products. *See* § V.A, ¶¶ 62–70 *infra*.

14. On information and belief, Proposed Respondent KIOXIA America, Inc. ("KIOXIA America") is a corporation organized under the laws of California with its principal place of business located at 2610 Orchard Parkway, San Jose, California 95134. *See* **Ex. 13** at 1. According to the KIOXIA Annual Securities Report, KIOXIA America is responsible for the "[m]arketing of Memory and SSD products," including KIOXIA's Accused Products. **Ex. 9** at 72. On information and belief, KIOXIA America is involved in the importation, sale for importation into the United States, and/or sale within the United States after importation of KIOXIA's Accused Products. *See* § V.A, ¶¶ 62–70 *infra*. On information and belief, according to its website, KIOXIA America has sales offices in the United States in at least the following locations, where it conducts sales and marketing activities for the Accused Products: San Jose, California; Irvine, California; Folsom, California; and Round Rock, Texas. *See* **Ex. 14** at 1.

15. On information and belief, Proposed Respondent KIOXIA Engineering Corporation ("KIOXIA Engineering") is a corporation organized under the laws of Japan with its principal place of business located at Nagoya Fushimi K Square Building, 6$^{th}$ Floor, 14-19 Nishiki 2-chome, Naka-ku, Nagoya 460-0003, Japan. *See* **Ex. 15** at 1. According to the KIOXIA Annual Securities Report, KIOXIA Engineering is responsible for the "[d]evelopment, design, production of Memory products," including KIOXIA's Accused Products. **Ex. 9** at 72. On information and

belief, KIOXIA Engineering is involved in the importation, sale for importation into the United States, and/or sale within the United States after importation of KIOXIA's Accused Products. *See* § V.A, ¶¶ 62–70 *infra*.

16. On information and belief, Proposed Respondent KIOXIA Iwate Corporation ("KIOXIA Iwate") is a corporation organized under the laws of Japan with its principal place of business located at 5-29 Kita Kogyo-Danchi, Kitakami-shi, Iwate, Japan. *See* **Ex. 16** at 1. According to the KIOXIA Annual Securities Report, KIOXIA Iwate is responsible for the "[p]roduction of Memory products," including KIOXIA's Accused Products. **Ex. 9** at 72. On information and belief, KIOXIA Iwate is involved in the importation, sale for importation into the United States, and/or sale within the United States after importation of KIOXIA's Accused Products. *See* § V.A, ¶¶ 62–70 *infra*.

17. On information and belief, Proposed Respondent KIOXIA Systems Co., Ltd. ("KIOXIA Systems") is a corporation organized under the laws of Japan with its principal place of business located at STE Building, 2-5-1 Kasama, Sakae-ku, Yokohama, Kanagawa Prefecture, 247-8585, Japan. *See* **Ex. 17** at 2. According to the KIOXIA Annual Securities Report, KIOXIA Systems is responsible for the "[d]esign and development of Memory products, and customer support," including KIOXIA's Accused Products. **Ex. 9** at 72. On information and belief, KIOXIA Systems is involved in the importation, sale for importation into the United States, and/or sale within the United States after importation of KIOXIA's Accused Products. *See* § V.A, ¶¶ 62–70 *infra*.

18. On information and belief, Proposed Respondent KIOXIA Semiconductor Taiwan Corporation ("KIOXIA Semiconductor") is a corporation organized under the laws of Taiwan with its principal place of business located at 3 F-5, No. 168, Sec. 3, Nanjing Road, Zhongshan District,

Taipei City 104105, Taiwan. *See* **Ex. 18** at 1. According to the KIOXIA Annual Securities Report, KIOXIA Semiconductor is responsible for the "[p]roduction management of subcontracted production in the post-process of Memory," including KIOXIA's Accused Products. **Ex. 9** at 72. On information and belief, KIOXIA Semiconductor is involved in the importation, sale for importation into the United States, and/or sale within the United States after importation of KIOXIA's Accused Products. *See* § V.A, ¶¶ 62–70 *infra*.

19. On information and belief, Proposed Respondents KIOXIA Holdings, KIOXIA Corp., KIOXIA America, KIOXIA Engineering, KIOXIA Iwate, KIOXIA Systems, and KIOXIA Semiconductor (collectively, "KIOXIA") manufacture, import into the United States, sell for importation, market, offer for sale, sell, and/or distribute within the United States certain Accused Products that infringe, literally and/or under the doctrine of equivalents, one or more claims of the Asserted Patents. *See* § V.A, ¶¶ 62–70 *infra*; § VI.A, ¶¶ 89–91 *infra*.

**2. The SK hynix Respondents**

20. On information and belief, Proposed Respondent SK hynix Inc. ("SKHI") is a corporation organized under the laws of South Korea with its principal place of business located at 2091, Gyeongchung-daero, Bubal-eub, Icheon-si, Gyeonggi-do, South Korea 17336. *See* **Ex. 19** at 2. According to its website, SKHI's "[a]rea of business" is the "[m]anufacture and sales of semiconductor devices," which include the Accused Products. *Id.* On information and belief, SKHI is involved in the importation, sale for importation into the United States, and/or sale within the United States after importation of SK hynix's Accused Products. *See* § V.B, ¶¶ 71–88 *infra*. SKHI is named on the product packaging for the SK hynix Accused Products that are manufactured abroad and imported, sold for importation into the United States, and/or sold within the United States after importation. *See* § V.B, ¶ 77 *infra*.

[redacted]

21. On information and belief, Proposed Respondent SK hynix America Inc. ("SKHA") is a corporation organized under the laws of California with its principal place of business located at 3103 North 1st Street, San Jose, California 95134. *See* **Ex. 20** at 1. On information and belief, SKHA is involved in the development, distribution, and marketing of the Accused Products. *See* **Ex. 21** at 1. On information and belief, SKHA is involved in the importation, sale for importation into the United States, and/or sale within the United States after importation of SK hynix's Accused Products. *See* § V.B, ¶¶ 71–88 *infra*. On information and belief, according to its website, SKHA has sales offices in the United States in at least the following locations, where it conducts sales activities relating to the Accused Products: San Jose, California; Seattle, Washington; Austin, Texas; Houston, Texas; and Raleigh, North Carolina. *See* **Ex. 22** at 1–2.

22. On information and belief, Proposed Respondent SK hynix Memory Solutions America Inc. ("SKHMS") is a corporation organized under the laws of Delaware with its principal place of business located at 3103 North 1st Street, San Jose, California 95134. *See* **Ex. 23** at 1. On information and belief, according to its website, SKHMS "is a research and development (R&D) subsidiary of SK hynix, a global leader in semiconductor manufacturing," which includes research and development of the Accused Products. **Ex. 24** at 11. On information and belief, SKHMS is involved in the importation, sale for importation into the United States, and/or sale within the United States after importation of SK hynix's Accused Products. *See* § V.B, ¶¶ 71–88 *infra*. According to its website, "SKHMS America operates in San Jose, California, USA, and specializes in customized NAND-based storage solutions," which includes the Accused Products. **Ex. 24** at 11.

23. On information and belief, Proposed Respondents SKHI, SKHA, and SKHMS (collectively, "SK hynix") manufacture, import into the United States, sell for importation, market, offer for sale, sell, and/or distribute within the United States certain Accused Products that infringe, literally and/or under the doctrine of equivalents, one or more claims of the Asserted Patents. *See* § V.B, ¶¶ 71–88 *infra*; § VI.B, ¶¶ 93–95 *infra*.

## III. THE TECHNOLOGY AND PRODUCTS AT ISSUE

24. Pursuant to 19 C.F.R. §§ 210.10(b)(1) and 210.12(a)(12), the categories of products accused of infringing one or more of the Asserted Patents are certain 3D NAND memory chips and high bandwidth memory ("HBM") DRAM chips. The Proposed Respondents infringe the Asserted Patents through the sale for importation into the United States, importation into the United States, and/or sale within the United States after importation of such Accused Products. Exemplary identifications of such infringing products are provided in Sections V and VI below.

25. Proposed Respondent KIOXIA's Accused Products include products comprising 3D memory, including at least all KIOXIA 3D NAND memory products. KIOXIA's Accused Products infringe all Asserted Patents. Proposed Respondent SK hynix's Accused Products include products comprising 3D memory, including at least all SK hynix 3D NAND memory products and all SK hynix HBM products. All SK hynix Accused Products (3D NAND memory products and HBM products) infringe the '531 Patent, the '1-737 Patent, and the '765 Patent. The SK hynix 3D NAND memory products also infringe the '214 Patent, the '181 Patent, the '473 Patent, and the '503 Patent. The table below is a preliminary identification of Accused Products and the Asserted Patents they infringe.

[redacted]

| Respondent | 3D NAND Products Infringed Patents | HBM DRAM Products Infringed Patents |
|---|---|---|
| KIOXIA | SSD Products:<br>CM Series; PM Series;<br>RM Series; FL Series;<br>CD Series; XD Series;<br>BG Series; XG Series<br><br>NAND Storage Products:<br>3D Flash Memory (*e.g.*, BiCS Flash | |
| | All Asserted Patents Infringed | |
| SK hynix | SSD Products:<br>PEB000 series; PS1000 series;<br>PE9000 series; PE8000 Series;<br>PE6000 Series; SE5000 Series;<br>PCB01/PVC10 series;<br>PC801/BC901 series;<br>PC/BC711 series<br><br>NAND Storage Products:<br>UE400 products;<br>UD310/220 products;<br>UD310A/210A UFS products;<br>eMMC 5.1 series eMMC products | HBM3;<br>HBM3E (*e.g.*, H5UG series);<br>HBM2E (*e.g.*, H5WR series); |
| | Patents Infringed:<br>'531 Patent<br>'1-737 Patent<br>'765 Patent<br>'214 Patent<br>'181 Patent<br>'473 Patent<br>'503 Patent | Patents Infringed:<br>'531 Patent<br>'1-737 Patent<br>'765 Patent |

26. The table above is not an exhaustive list of Accused Products. Discovery is necessary to identify all products sold for importation into the United States, imported into the United States, and/or sold within the United States after importation that infringe the Asserted Patents. Complainant reserves the right to supplement its allegations, add Accused Products, further amend this Complaint, and to add proposed respondents in the future, if necessary, based on discovery received during the Investigation.

## IV. THE ASSERTED PATENTS

27. Certified copies of the Asserted Patents are attached as **Exhibits 1** through **8**. Certified copies of the assignment documents for the Asserted Patents are attached as **Exhibits 25** through **32**. [1] MonolithIC 3D is the sole and exclusive owner of all rights, title, and interest in the Asserted Patents and holds the exclusive right to take all actions necessary to enforce its rights to the Asserted Patents.

### A. The '531 Patent

#### 1. Identification of the Patent and Ownership

28. The '531 Patent, titled "3D Semiconductor Device and Structure With Logic and Memory," issued on July 9, 2024, naming Zvi Or-Bach and Jin-Woo Hanas inventors. **Ex. 1** at 1. The '531 Patent is based on U.S. Patent Application No. 18/516,958, filed November 22, 2023, which is a continuation-in-part of application No. 17/665,560, filed on Feb. 6, 2022, which is a continuation-in-part of application No. 17/524,737, filed on Nov. 11, 2021, now Pat. No. 11,296,115, which is a continuation-in-part of application No. 17/396,711, filed on Aug. 8, 2021, now Pat. No. 11,233,069, which is a continuation-in-part of application No. 17/063,397, filed on Oct. 5, 2020, now Pat. No. 11,114,464, which is a continuation-in-part of application No.

[1] To the extent certified copies of the Asserted Patents, prosecution histories, and assignments are not included, they have been ordered and will be promptly filed once received.

16/526,763, filed on Jul. 30, 2019, now Pat. No. 10,847,540, which is a continuation-in-part of application No. 15/990,611, filed on May 26, 2018, now Pat. No. 10,418,369, which is a continuation of application No. 15/333,138, filed on Oct. 24, 2016, now Pat. No. 10,014,318. The '531 Patent is further entitled to priority based on provisional application No. 62/307,568, filed on Mar. 14, 2016, provisional application No. 62/286,362, filed on Jan. 23, 2016, provisional application No. 62/276,953, filed on Jan. 10, 2016, provisional application No. 62/271,251, filed on Dec. 27, 2015, provisional application No. 62/266,610, filed on Dec. 12, 2015, and provisional application No. 62/246,054, filed on Oct. 24, 2015. The '531 Patent expires on Oct. 24, 2036. A certified copy of the '531 Patent is attached as **Exhibit 1**. This complaint is accompanied by a certified copy of the prosecution history for the '531 Patent, three additional copies of the prosecution history, and one copy of the prosecution histories for the priority applications for the '531 Patent. *See* **Ex. 1**; **Appx. A**; **Appx. I**.

**2. Nontechnical Description of the Patent**

29. The '531 Patent relates to the general field of Integrated Circuit (IC) devices and fabrication methods, and more particularly to multilayer or Three Dimensional Integrated Memory Circuit (3D-Memory) devices and fabrication methods. The '531 Patent describes, for example, a 3D semiconductor device including: a first level including a single crystal layer, a memory control circuit which includes a plurality of first transistors; a first metal layer overlaying the single crystal layer; a second metal layer overlaying the first metal layer; a third metal layer overlaying the second metal layer; second transistors which include a metal gate are disposed atop the third metal layer; third transistors disposed atop the second transistors; a fourth metal layer disposed atop the third transistors; and a memory array including word-lines, the memory array includes at least four memory mini arrays, each including at least four rows by at least four columns of memory cells,

where each of the memory cells includes at least one of the second transistors or at least one of the third transistors, the memory control circuit includes at least one Look Up Table circuit ("LUT").

#### 3. Foreign Patents, Foreign or Domestic Patent Applications (Not Already Issued As a Patent), and Foreign or Domestic Patent Applications (Denied, Abandoned, or Withdrawn) Corresponding to the Patent

30. The following pending domestic patent applications correspond to the '531 Patent: U.S. Patent Application Nos. 19/243,077 and 19/345,854. To the best of Complainant's knowledge, information, and belief, there are no foreign patents issued or foreign or other domestic patent applications pending, filed, abandoned, withdrawn, or rejected corresponding to the '531 Patent.

#### 4. Licensees

31. All licensees to the '531 Patent are identified in **Confidential Exhibit 33C.** There are no other known licensees related to the '531 Patent.

### B. The '1-737 Patent

#### 1. Identification of the Patent and Ownership

32. The '1-737 Patent, titled "3D Semiconductor Device and Structure With Metal Layers and Memory Cells," issued on October 22, 2024, naming Zvi Or-Bach, Brian Cronquist, and Deepak C. Sekar as inventors. **Ex. 2** at 1. The '1-737 Patent is based on U.S. Patent Application No. 18/736,423, filed June 6, 2024, which is a Continuation-in-part of application No. 18/677,553, filed on May 29, 2024, which is a continuation-in-part of application No. 18/424,790, filed on Jan. 27, 2024, now Pat. No. 12,068,187, which is a continuation-in-part of application No. 18/382,468, filed on Oct. 20, 2023, now Pat. No. 11,923,230, which is a continuation-in-part of application No. 18/228,675, filed on Aug. 1, 2023, now Pat. No. 11,830,757, which is a continuation-in-part of application No. 18/092,337, filed on Jan. 1, 2023, now Pat. No. 11,784,082, which is a

continuation-in-part of application No. 17 /942,109, filed on Sep. 9, 2022, which is a continuation-in-part of application No. 17 /340,004, filed on Jun. 5, 2021, now Pat. No. 11,482,438, which is a continuation-in-part of application No. 16/537,564, filed on Aug. 10, 2019, now Pat. No. 11,004,719, which is a continuation-in-part of application No. 15/460,230, filed on Mar. 16, 2017, now Pat. No. 10,497,713, which is a continuation-in-part of application No. 14/821,683, filed on Aug. 7, 2015, now Pat. No. 9,613,844, which is a continuation-in-part of application No. 13/492,395, filed on Jun. 8, 2012, now Pat. No. 9,136,153, which is a continuation-in-part of application No. 13/273,712, filed on Oct. 14, 2011, now Pat. No. 8,273,610, which is a continuation-in-part of application No. 13/016,313, filed on Jan. 28, 2011, now Pat. No. 8,362,482, which is a continuation-in-part of application No. 12/970,602, filed on Dec. 16, 2010, now Pat. No. 9,711,407, which is a continuation-in-part of application No. 12/949,617, filed on Nov. 18, 2010, now Pat. No. 8,754,533, said application No. 17 /340,004 is a continuation-in-part of application No. 17/147,320, filed on Jan. 12, 2021, now Pat. No. 11,004,719, which is a continuation-in-part of application No. 16/537,564, filed on Aug. 10, 2019, which is a continuation-in-part of application No. 15/460,230, filed on Mar. 16, 2017, now Pat. No. 10,497,713, which is a continuation-in-part of application No. 14/821,683, filed on Aug. 7, 2015, now Pat. No. 9,613,844, which is a continuation-in-part of application No. 13/492,395, filed on Jun. 8, 2012, now Pat. No. 9,136,153, which is a continuation of application No. 13/273,712, filed on Oct. 14, 2011, now Pat. No. 8,273,610, which is a continuation-in-part of application No. 13/016,313, filed on Jan. 28, 2011, now Pat. No. 8,362,482, which is a continuation-in-part of application No. 12/970,602, filed on Dec. 16, 2010, now Pat. No. 9,711,407, which is a continuation-in-part of application No. 12/949,617, filed on Nov. 18, 2010, now Pat. No. 8,754,533. The ’1-737 Patent expires on November 18, 2030. A certified copy of the ’1-737 Patent

is attached as **Exhibit 2**. This complaint is accompanied by a certified copy of the prosecution history for the '1-737 Patent, three additional copies of the prosecution history, and one copy of the prosecution histories for the priority applications for the '1-737 Patent. *See* **Ex. 2**; **Appx. B**; **Appx. J**.

### 2. Nontechnical Description of the Patent

33. The '1-737 Patent relates to the general field of Integrated Circuit (IC) devices and fabrication methods, and more particularly to multilayer or Three Dimensional Integrated Circuit (3D IC) devices and fabrication methods. The '1-737 Patent describes, for example, a 3D semiconductor device, the device including: a first level including a first single crystal layer, the first level including first transistors, where each of the first transistors includes a single crystal channel; a first metal layer; a second metal layer overlaying the first metal layer; a second level including second transistors, first memory cells including at least one second transistor, and overlaying the second metal layer, a third level including third transistors and overlaying the second level, a fourth level including fourth transistors, second memory cells including at least one fourth transistor, and overlaying the third level, where the first level includes memory control circuits which control writing to the second memory cells, and at least one Phase-Lock-Loop ("PLL") circuit or at least one Digital-Lock-Loop ("DLL") circuit.

### 3. Foreign Patents, Foreign or Domestic Patent Applications (Not Already Issued As a Patent), and Foreign or Domestic Patent Applications (Denied, Abandoned, or Withdrawn) Corresponding to the Patent

34. The following pending domestic patent application corresponds to the '1-737 Patent: U.S. Patent Application No. 19/351,203. To the best of Complainant's knowledge, information, and belief, there are no foreign patents issued, or foreign or other domestic patent applications pending, filed, abandoned, withdrawn, or rejected corresponding to the '1-737 Patent.

[redacted]

#### 4. Licensees

All licensees to the '1-737 Patent are identified in **Confidential Exhibit 33C.** There are no other known licensees related to the '1-737 Patent.

### C. The '765 Patent

#### 1. Identification of the Patent and Ownership

35. The '765 Patent, titled "3D Semiconductor Device and Structure With Metal Layers and Memory Cells," issued on March 4, 2025, naming Zvi Or-Bach, Brian Cronquist, and Deepak C. Sekar as inventors. **Ex. 3** at 1. The '765 Patent is based on U.S. Patent Application No. 18/829,079, filed September 9, 2024, which is a Continuation-in-part of application No. 18/736,423, filed on Jun. 6, 2024, now Pat. No. 12,125,737, which is a continuation-in-part of application No. 18/677,553, filed on May 29, 2024, now Pat. No. 12,144,190, which is a continuation-in-part of application No. 18/424,790, filed on Jan. 27, 2024, now Pat. No. 12,068,187, which is a continuation-in-part of application No. 18/382,468, filed on Oct. 20, 2023, now Pat. No. 11,923,230, which is a continuation-in-part of application No. 18/228,675, filed on Aug. 1, 2023, now Pat. No. 11,830,757, which is a continuation-in-part of application No. 18/092,337, filed on Jan. 1, 2023, now Pat. No. 11,784,082, which is a continuation-in-part of application No. 17/942,109, filed on Sep. 9, 2022, now Pat. No. 12,154,817, which is a continuation-in-part of application No. 17 /340,004, filed on Jun. 5, 2021, now Pat. No. 11,482,438, which is a continuation-in-part of application No. 16/537,564, filed on Aug. 10, 2019, which is a continuation-in-part of application No. 15/460,230, filed on Mar. 16, 2017, now Pat. No. 10,497,713, which is a continuation-in-part of application No. 14/821,683, filed on Aug. 7, 2015, now Pat. No. 9,613,844, which is a continuation-in-part of application No. 13/492,395, filed on Jun. 8, 2012, now Pat. No. 9,136,153, which is a continuation of application No. 13/273,712, filed on Oct. 14, 2011, now Pat. No. 8,273,610, which is a continuation-in-part of application No.

13/016,313, filed on Jan. 28, 2011, now Pat. No. 8,362,482, which is a continuation-in-part of application No. 12/970,602, filed on Dec. 16, 2010, now Pat. No. 9,711,407, which is a continuation-in-part of application No. 12/949,617, filed on Nov. 18, 2010, now Pat. No. 8,754,533, said application No. 17/340,004 is a continuation-in-part of application No. 17/147,320, filed on Jan. 12, 2021, now Pat. No. 11,004,719, which is a continuation-in-part of application No. 16/537,564, filed on Aug. 10, 2019, which is a continuation-in-part of application No. 15/460,230, filed on Mar. 16, 2017, now Pat. No. 10,497,713, which is a continuation-in-part of application No. 14/821,683, filed on Aug. 7, 2015, now Pat. No. 9,613,844, which is a continuation-in-part of application No. 13/492,395, filed on Jun. 8, 2012, now Pat. No. 9,136,153, which is a continuation of application No. 13/273,712, filed on Oct. 14, 2011, now Pat. No. 8,273,610, which is a continuation-in-part of application No. 13/016,313, filed on Jan. 28, 2011, now Pat. No. 8,362,482, which is a continuation-in-part of application No. 12/970,602, filed on Dec. 16, 2010, now Pat. No. 9,711,407, which is a continuation-in-part of application No. 12/949,617, filed on Nov. 18, 2010, now Pat. No.8,754,533. The ’765 Patent expires on November 18, 2030. A certified copy of the ’765 Patent is attached as **Exhibit 3**. This complaint is accompanied by a certified copy of the prosecution history for the ’765 Patent, three additional copies of the prosecution history, and one copy of the prosecution histories for the priority applications for the ’765 Patent. *See* **Ex. 3**; **Appx. C**; **Appx. K**.

**2. Nontechnical Description of the Patent**

36. The ’765 Patent relates to the general field of Integrated Circuit (IC) devices and fabrication methods, and more particularly to multilayer or Three Dimensional Integrated Circuit (3D IC) devices and fabrication methods. The ’765 Patent describes, for example, a 3D semiconductor device, the device including: a first level including a first single crystal layer and including first transistors which each includes a single crystal channel; a first metal layer; a second

metal layer overlaying the first metal layer; a second level including second transistors, first memory cells including at least one second transistor, and overlaying the second metal layer; a third level including third transistors and overlaying the second level; a fourth level including fourth transistors, second memory cells including at least one fourth transistor, and overlaying the third level, where at least one of the second transistors includes a metal gate, where the first level includes memory control circuits which control writing to the second memory cells, and at least one Phase-Lock-Loop ("PLL") circuit or at least one Digital-Lock-Loop ("DLL") circuit.

#### 3. Foreign Patents, Foreign or Domestic Patent Applications (Not Already Issued As a Patent), and Foreign or Domestic Patent Applications (Denied, Abandoned, or Withdrawn) Corresponding to the Patent

37. The following pending domestic patent application corresponds to the '765 Patent: U.S. Patent Application No. 19/351,203. To the best of Complainant's knowledge, information, and belief, there are no foreign patents issued, or foreign or other domestic patent applications pending, filed, abandoned, withdrawn, or rejected corresponding to the '765 Patent.

#### 4. Licensees

38. All licensees to the '765 Patent are identified in **Confidential Exhibit 33C.** There are no other known licensees related to the '765 Patent.

### D. The '214 Patent

#### 1. Identification of the Patent and Ownership

39. The '214 Patent, titled "Methods for Producing a 3D Semiconductor Memory Device and Structure," issued on May 24, 2022, naming Zvi Or-Bach, Brian Cronquist, and Deepak C. Sekaras inventors. **Ex. 4** at 1. The '214 Patent is based on U.S. Patent Application No. 17/692,146, filed March 10, 2022, which is a continuation-in-part of application No. 17/543,510, filed on Dec. 6, 2021, which is a continuation-in-part of application No. 17/340,004, filed on Jun.

5, 2021, which is a continuation-in-part of application No. 17/147,320, filed on Jan. 12, 2021, now Pat. No. 11,004,719, which is a continuation-in-part of application No. 16/537,564, filed on Aug. 10, 2019, said application No. 17 /340,004 is a continuation-in-part of application No. 16/537,564, which is a continuation-in-part of application No. 15/460,230, filed on Mar. 16, 2017, now Pat. No. 10,497,713, which is a continuation-in-part of application No. 14/821,683, filed on Aug. 7, 2015, now Pat. No. 9,613,844, which is a continuation-in-part of application No. 13/492,395, filed on Jun. 8, 2012, now Pat. No. 9,136,153, which is a continuation of application No. 13/273,712, filed on Oct. 14, 2011, now Pat. No. 8,273,610, which is a continuation-in-part of application No. 13/016,313, filed on Jan. 28, 2011, now Pat. No. 8,362,482, which is a continuation-in-part of application No. 12/970,602, filed on Dec. 16, 2010, now Pat. No. 9,711,407, which is a continuation-in-part of application No. 12/949,617, filed on Nov. 18, 2010, now Pat. No. 8,754,533. The ’214 Patent expires on November 18, 2030. A certified copy of the ’214 Patent is attached as **Exhibit 4**. This complaint is accompanied by a certified copy of the prosecution history for the ’214 Patent, three additional copies of the prosecution history, and one copy of the prosecution histories for the priority applications for the ’214 Patent. *See* **Ex. 4**; **Appx. D**; **Appx. L**.

**2. Nontechnical Description of the Patent**

40. The ’214 Patent relates to the general field of Integrated Circuit (IC) devices and fabrication methods, and more particularly to multilayer or Three Dimensional Integrated Circuit (3D IC) devices and fabrication methods. The ’214 Patent describes, for example, A method for producing a 3D memory device, the method including: providing a first level including a first single crystal layer; forming a plurality of first transistors each including a single crystal channel; forming a first metal layer and a second metal layer, where the first level includes the plurality of first transistors, the first metal layer, and the second metal layer; forming at least one second level

disposed above the second metal layer; performing a first etch step including etching first holes within the second level; forming at least one third level above the at least one second level; performing a second etch step including etching second holes within the third level; and performing additional processing steps to form a plurality of first memory cells within the second level and a plurality of second memory cells within the third level, where memory cells each include one memory transistor.

#### 3. Foreign Patents, Foreign or Domestic Patent Applications (Not Already Issued As a Patent), and Foreign or Domestic Patent Applications (Denied, Abandoned, or Withdrawn) Corresponding to the Patent

41. To the best of Complainant's knowledge, information, and belief, there are no foreign patents issued, or foreign or domestic patent applications pending, filed, abandoned, withdrawn, or rejected corresponding to the '214 Patent.

#### 4. Licensees

42. All licensees to the '214 Patent are identified in **Confidential Exhibit 33C.** There are no other known licensees related to the '214 Patent.

### E. The '181 Patent

#### 1. Identification of the Patent and Ownership

43. The '181 Patent, titled "3D Semiconductor Device and Structure With Metal Layers," issued on October 18, 2022, naming Zvi Or-Bach, Deepak C. Sekar, and Brian Cronquist as inventors. **Ex. 5** at 1. The '181 Patent is based on U.S. Patent Application No. 17/850,819, filed June 27, 2022, which is a Continuation-in-part of application No. 17/492,577, filed on Oct. 2, 2021, now Pat. No. 11,410,912, which is a continuation-in-part of application No. 17 /313,986, filed on May 6, 2021, now Pat. No. 11,164,811, which is a continuation-in-part of application No. 16/852,506, filed on Apr. 19, 2020, now Pat. No. 11 088 050 which is a continuation-in-part of

application No. 16/536,606, filed on Aug. 9, 2019, now Pat. No. 10,665,695, which is a continuation-in-part of application No. 16/004,404, filed on Jun. 10, 2018, now Pat. No. 10,600,888, which is a continuation-in-part of application No. 15/917,629, filed on Mar. 10, 2018, now Pat. No. 10,038,073, which is a continuation-in-part of application No. 15/622,124, filed on Jun. 14, 2017, now Pat. No. 9,954,080, which is a continuation-in-part of application No. 14/880,276, filed on Oct. 11, 2015, now Pat. No. 9,691,869, which is a continuation-in-part of application No. 14/472,108, filed on Aug. 28, 2014, now Pat. No. 9,305,867, which is a continuation of application No. 13/959,994, filed on Aug. 6, 2013, now Pat. No. 8,836,073, which is a continuation of application No. 13/441,923, filed on Apr. 9, 2012, now Pat. No. 8,557,632. The '181 Patent expires on April 9, 2032. A certified copy of the '181 Patent is attached as **Exhibit 5**. This complaint is accompanied by a certified copy of the prosecution history for the '181 Patent, three additional copies of the prosecution history, and one copy of the prosecution histories for the priority applications for the '181 Patent. *See* **Ex. 5**; **Appx. E**; **Appx. M**.

**2. Nontechnical Description of the Patent**

44. The '181 Patent relates to the general field of Integrated Circuit (IC) devices and fabrication methods, and more particularly to multilayer or Three Dimensional Integrated Circuit (3D IC) devices and fabrication methods. The '181 Patent describes, for example, A 3D semiconductor device including: a first level including a single crystal silicon layer and a plurality of first transistors each including a single crystal channel; a first metal layer overlaying the plurality of first transistors; a second metal layer overlaying the first metal layer; a third metal layer overlaying the second metal layer; a second level, where the second level overlays the first level and includes a plurality of second transistors; a fourth metal layer overlaying the second level; and a connective path between the fourth metal layer and either the third metal layer or the second metal layer, where the connective path includes a via disposed through the second level

and has a diameter of less than 500 nm and greater than 5 nm, where the third metal layer is connected to provide a power or ground signal to at least one of the second transistors.

### 3. Foreign Patents, Foreign or Domestic Patent Applications (Not Already Issued As a Patent), and Foreign or Domestic Patent Applications (Denied, Abandoned, or Withdrawn) Corresponding to the Patent

45. The following pending domestic patent application corresponds to the '181 Patent: U.S. Patent Application No. 19/369,245. To the best of Complainant's knowledge, information, and belief, there are no foreign patents issued, or foreign or other domestic patent applications pending, filed, abandoned, withdrawn, or rejected corresponding to the '181 Patent.

### 4. Licensees

46. All licensees to the '181 Patent are identified in **Confidential Exhibit 33C.** There are no other known licensees related to the '181 Patent.

## F. The '473 Patent

### 1. Identification of the Patent and Ownership

47. The '473 Patent, titled "3D Semiconductor Device and Structure with Metal Layers and a Connective Path," issued on February 28, 2023, naming Zvi Or-Bach, Deepak C. Sekar, and Brian Cronquist as inventors. **Ex. 6** at 1. The '473 Patent is based on U.S. Patent Application No. 17/941,891, filed September 9, 2022, which is a continuation-in-part of application No. 17/850,819, filed on Jun. 27, 2022, now Pat. No. 11,476,181, which is a continuation-in-part of application No. 17/492,577, filed on Oct. 2, 2021, now Pat. No. 11,410,912, which is a continuation-in-part of application No. 17/313,986, filed on May 6, 2021, now Pat. No. 11,164,811, which is a continuation-in-part of application No. 16/852,506, filed on Apr. 19, 2020, now Pat. No. 11,088,050, which is a continuation-in-part of application No. 16/536,606, filed on Aug. 9, 2019, now Pat. No. 10,665,695, which is a continuation-in-part of application No.

16/004,404, filed on Jun. 10, 2018, now Pat. No. 10,600,888, which is a continuation-in-part of application No. 15/917,629, filed on Mar. 10, 2018, now Pat. No. 10,038,073, which is a continuation-in-part of application No. 15/622,124, filed on Jun. 14, 2017, now Pat. No. 9,954,080, which is a continuation-in-part of application No. 14/880,276, filed on Oct. 11, 2015, now Pat. No. 9,691,869, which is a continuation-in-part of application No. 14/472,108, filed on Aug. 28, 2014, now Pat. No. 9,305,867, which is a continuation of application No. 13/959,994, filed on Aug. 6, 2013, now Pat. No. 8,836,073, which is a continuation of application No. 13/441,923, filed on Apr. 9, 2012, now Pat. No. 8,557,632. The '473 Patent expires on April 9, 2032. A certified copy of the '473 Patent is attached as **Exhibit 6**. This complaint is accompanied by a certified copy of the prosecution history for the '473 Patent, three additional copies of the prosecution history, and one copy of the prosecution histories for the priority applications for the '473 Patent. *See* **Ex. 6**; **Appx. F**; **Appx. N**.

**2. Nontechnical Description of the Patent**

48. The '473 Patent relates to general field of Integrated Circuit (IC) devices and fabrication methods, and more particularly to multilayer or Three Dimensional Integrated Circuit (3D IC) devices and fabrication methods. The '473 Patent describes, for example, a 3D semiconductor device including: a first level including a single crystal silicon layer and a plurality of first transistors, the plurality of first transistors each including a single crystal channel; a first metal layer overlaying the plurality of first transistors; a second metal layer overlaying the first metal layer; a third metal layer overlaying the second metal layer; a second level is disposed above the third metal layer, where the second level includes a plurality of second transistors; a fourth metal layer disposed above the second level; and a connective path between the fourth metal layer and either the third metal layer or the second metal layer, where the connective path includes a via

disposed through the second level, where the via has a diameter of less than 800 nm and greater than 5 nm, and where at least one of the plurality of second transistors includes a metal gate.

#### 3. Foreign Patents, Foreign or Domestic Patent Applications (Not Already Issued As a Patent), and Foreign or Domestic Patent Applications (Denied, Abandoned, or Withdrawn) Corresponding to the Patent

49. The following pending domestic patent application corresponds to the '473 Patent: U.S. Patent Application No. 19/369,245. To the best of Complainant's knowledge, information, and belief, there are no foreign patents issued, or foreign or other domestic patent applications pending, filed, abandoned, withdrawn, or rejected corresponding to the '473 Patent.

#### 4. Licensees

50. All licensees to the '473 Patent are identified in **Confidential Exhibit 33C.** There are no other known licensees related to the '473 Patent.

### G. The '503 Patent

#### 1. Identification of the Patent and Ownership

51. The '503 Patent, titled "Method for Producing a 3D Semiconductor Device and Structure With Memory Cells and Multiple Metal Layers," issued on January 12, 2024, naming Zvi Or-Bach, Deepak C. Sekar, and Brian Cronquist as inventors. **Ex. 7** at 1. The '503 Patent is based on U.S. Patent Application No. 18/106,757, filed February 7, 2023, which is a continuation-in-part of application No. 17/846,012, filed on Jun. 22, 2022, now Pat. No. 11,610,802, which is a continuation-in-part of application No. 17/536,097, filed on Nov. 29, 2021, now Pat. No. 11,521,888, which is a continuation-in-part of application No. 17/140,130, filed on Jan. 3, 2021, now Pat. No. 11,211,279, which is a continuation-in-part of application No. 16/537,564, filed on Aug. 10, 2019, which is a continuation-in-part of application No. 15/460,230, filed on Mar. 16, 2017, now Pat. No. 10,497,713, which is a continuation-in-part of application No. 14/821,683,

filed on Aug. 7, 2015, now Pat. No. 9,613,844, which is a continuation-in-part of application No. 13/492,395, filed on Jun. 8, 2012, now Pat. No. 9,136,153, which is a continuation of application No. 13/273,712, filed on Oct. 14, 2011, now Pat. No. 8,273,610, which is a continuation-in-part of application No. 13/016,313, filed on Jan. 28, 2011, now Pat. No. 8,362,482, which is a continuation-in-part of application No. 12/970,602, filed on Dec. 16, 2010, now Pat. No. 9,711,407, which is a continuation-in-part of application No. 12/949,617, filed on Nov. 18, 2010, now Pat. No. 8,754,533. The '503 Patent expires on February 28, 2031. A certified copy of the '503 Patent is attached as **Exhibit 7**. This complaint is accompanied by a certified copy of the prosecution history for the '503 Patent, three additional copies of the prosecution history, and one copy of the prosecution histories for the priority applications for the '503 Patent. *See* **Ex. 7**; **Appx. G**; **Appx. O**.

**2. Nontechnical Description of the Patent**

52. The '503 Patent relates to the general field of Integrated Circuit (IC) devices and fabrication methods, and more particularly to multilayer or Three Dimensional Integrated Circuit (3D IC) devices and fabrication methods. The '503 Patent describes, for example, a method for producing a 3D semiconductor device including: providing a first level including a first single crystal layer; forming a first metal layer on top of first level; forming a second metal layer on top of the first metal layer; forming at least one second level above the second metal layer; performing a first lithography step on the second level; forming a third level on top of the second level; performing a second lithography step on the third level; perform processing steps to form first memory cells within the second level and second memory cells within the third level, where first memory cells include at least one second transistor, and the second memory cells include at least one third transistor; and deposit a gate electrode for the second and the third transistors.

[redacted]

### 3. Foreign Patents, Foreign or Domestic Patent Applications (Not Already Issued As a Patent), and Foreign or Domestic Patent Applications (Denied, Abandoned, or Withdrawn) Corresponding to the Patent

53. The following pending domestic patent application corresponds to the ’503 Patent: U.S. Patent Application No. 18/798,708. To the best of Complainant’s knowledge, information, and belief, there are no foreign patents issued, or foreign or other domestic patent applications pending, filed, abandoned, withdrawn, or rejected corresponding to the ’503 Patent.

### 4. Licensees

54. All licensees to the ’503 Patent are identified in **Confidential Exhibit 33C.** There are no other known licensees related to the ’503 Patent.

## H. The ’2-737 Patent

### 1. Identification of the Patent and Ownership

55. The ’2-737 Patent, titled “Method for Producing 3D Semiconductor Devices and Structures With Transistors and Memory Cells,” issued on February 2, 2025, naming Deepak C. Sekar and Zvi Or-Bach as inventors. **Ex. 8** at 2. The ’2-737 Patent is based on U.S. Patent Application No. 18/596,623, filed March 6, 2024, which is a Continuation of application No. 18/234,368, filed on Aug. 15, 2023, now Pat. No. 11,956,976, which is a continuation-in-part of application No. 18/105,041, filed on Feb. 2, 2023, now Pat. No. 11,793,005, which is a continuation-in-part of application No. 17 /898,475, filed on Aug. 29, 2022, now Pat. No. 11,600,667, which is a continuation-in-part of application No. 17/850,840, filed on Jun. 27, 2022, now Pat. No. 11,462,586, which is a continuation-in-part of application No. 17/718,932, filed on Apr. 12, 2022, now Pat. No. 11,469,271, which is a continuation-in-part of application No. 17 /683,322, filed on Feb. 28, 2022, now Pat. No. 11,335,731, which is a continuation-in-part of application No. 17 /572,550, filed on Jan. 10, 2022, now Pat. No. 11,315,980, which is a

continuation-in-part of application No. 17 /542,490, filed on Dec. 5, 2021, now Pat. No. 11,257,867, which is a continuation-in-part of application No. 17 /402,526, filed on Aug. 14, 2021, now Pat. No. 11,227,897, which is a continuation-in-part of application No. 17/223,822, filed on Apr. 6, 2021, now Pat. No. 11,133,351, which is a continuation-in-part of application No. 17/114,155, filed on Dec. 7, 2020, now Pat. No. 11,018,191, which is a continuation-in-part of application No. 17/013,823, filed on Sep. 7, 2020, now Pat. No. 10,896,931, which is a continuation-in-part of application No. 16/409,813, filed on May 11, 2019, now Pat. No. 10,825,864, which is a continuation-in-part of application No. 15/803,732, filed on Nov. 3, 2017, now Pat. No. 10,290,682, which is a continuation-in-part of application No. 14/555,494, filed on Nov. 26, 2014, now Pat. No. 9,818,800, which is a continuation of application No. 13/246,157, filed on Sep. 27, 2011, now Pat. No. 8,956,959, which is a continuation of application No. 13/173,999, filed on Jun. 30, 2011, now Pat. No. 8,203,148, which is a continuation of application No. 12/901,890, filed on Oct. 11, 2010, now Pat. No. 8,026,521. The ’2-737 Patent expires on October 11, 2030. A certified copy of the ’2-737 Patent is attached as **Exhibit 8**. This complaint is accompanied by a certified copy of the prosecution history for the ’2-737 Patent, three additional copies of the prosecution history, and one copy of the prosecution histories for the priority applications for the ’2-737 Patent. *See* **Ex. 8**; **Appx. H**; **Appx. P**.

**2. Nontechnical Description of the Patent**

56. The ’2-737 Patent relates to applications of monolithic 3D integration to at least semiconductor chips performing logic and memory functions. The ’2-737 Patent describes, for example, a method for producing a 3D semiconductor device including: providing a first level, including a single crystal layer; forming memory control circuits in and/or on the first level which include first single crystal transistors and at least two interconnection metal layers; forming at least one second level disposed above the memory control circuits; performing a first etch step into the

second level; forming at least one third level on top of the second level; performing additional processing steps to form first memory cells within the second level and second memory cells within the third level, where each of the first memory cells include at least one second transistor including a metal gate, where each of the second memory cells include at least one third transistor; and performing bonding of the first level to the second level, where the bonding includes oxide to oxide bonding.

### 3. Foreign Patents, Foreign or Domestic Patent Applications (Not Already Issued As a Patent), and Foreign or Domestic Patent Applications (Denied, Abandoned, or Withdrawn) Corresponding to the Patent

57. The following pending domestic patent application corresponds to the '2-737 Patent: U.S. Patent Application No. 19/351,167. To the best of Complainant's knowledge, information, and belief, there are no foreign patents issued, or foreign or other domestic patent applications pending, filed, abandoned, withdrawn, or rejected corresponding to the '2-737 Patent.

### 4. Licensees

58. All licensees to the '2-737 Patent are identified in **Confidential Exhibit 33C.** There are no other known licensees related to the '2-737 Patent.

## V. SPECIFIC INSTANCES OF IMPORTATION AND SALE

59. On information and belief, the Proposed Respondents are importing and will continue to import, sell for importation, and/or sell within the United States after importation the Accused Products.

60. The specific instances of importation and sale of the Accused Products set forth below are illustrative and non-exhaustive examples of the Proposed Respondents' unlawful importation and sale of the Accused Products that directly and/or indirectly infringe the Asserted Patents, literally and/or under the doctrine of equivalents. These instances are exemplary in nature

and not intended to restrict the scope of any exclusion order or other remedy the Commission may order.

61. The Proposed Respondents' Accused Products are available for sale and have been purchased in the United States. *See* § V.A–B *infra*. In addition, publicly available information demonstrates that the Proposed Respondents' Accused Products are manufactured abroad and imported, sold for importation into the United States, and/or sold within the United States after importation. *See id.*

### A. KIOXIA

62. On information and belief, KIOXIA imports, sells for importation, and/or sells within the United States after importation Accused Products, including the exemplar KIOXIA BiCS8 3D TLC (model number T2BIGB5A2V) product, that infringe one or more claims of the Asserted Patents.

63. On information and belief, KIOXIA's Accused Products that infringe one or more claims of the Asserted Patents are manufactured abroad in Japan and incorporated as components into products that are manufactured abroad in Taiwan, including the Corsair MP700 Elite, and then imported, sold for importation, and/or sold within the United States after importation. *See* ¶¶ 66–70 *infra*. On information and belief, KIOXIA has reason to know that its Accused Products will be incorporated as components into products that are imported, sold for importation, and/or sold within the United States after importation, as KIOXIA specifically and knowingly sells its Accused Products to customers in the United States and/or companies that sell their products in the United States, such as Corsair Memory, Inc. *See* ¶¶ 66–70 *infra*. For example, according to the KIOXIA Annual Securities Report, from April 1, 2024 to March 31, 2025, KIOXIA reported total revenue of 1,706,460 in millions of Yen, of which 991,147 in millions of Yen was from sales of its "SSD & Storage" devices. **Ex. 9** at 20. Revenues from U.S. sales comprise a significant portion of

KIOXIA's revenue. For example, from April 1, 2024 to March 31, 2025, KIOXIA reported "[r]evenue from external customers" in "North America and Europe" of 853,608 million Yen. *Id.* "Revenues in the United States for the year ended March 31, 2025 and 2024 are 758,666 million yen and 393,909 million yen respectively." *Id.* In addition, KIOXIA states that "much of its revenue depends on a limited number of customers and industries," including U.S. companies, and its "[r]elationships with these customers, including those who are influenced by international circumstances such as U.S.-China trade frictions and U.S. tariff policies, may materially affect the Group's business, operating result, and financial position." *Id.* at 89. Furthermore, KIOXIA has sales offices in the United States in at least the following locations, where, on information and belief, it conducts sales activities relating to tis Accused Products: San Jose, California; Irvine, California; Folsom, California; and Round Rock, Texas. *See* **Ex. 14** at 1.

64. According to a press release, KIOXIA's "[f]ifth-generation BiCS FLASH™ was developed jointly with technology and manufacturing partner Western Digital Corporation" and is "manufactured at Kioxia's Yokkaichi Plant and the newly built Kitakami Plant" in Japan. **Ex. 34** at 2.

65. According to the KIOXIA Annual Securities Report, "Kioxia Corporation and the Group's three manufacturing joint ventures are scheduled to receive a grant of up to approximately 92.9 billion yen from the Japanese government for the production of flash memory at the Yokkaichi Plant (approximately 6.8 billion yen has not been received as of March 31, 2025). In addition, Kioxia Corporation, Kioxia Iwate Corporation, and the Group's three manufacturing joint ventures are scheduled to receive a grant of up to 150.0 billion yen from the Japanese government for the production of flash memory at the Yokkaichi and Kitakami Plants (approximately 119.8 billion yen has not been received as of March 31, 2025)." **Ex. 9** at 84.

[redacted]

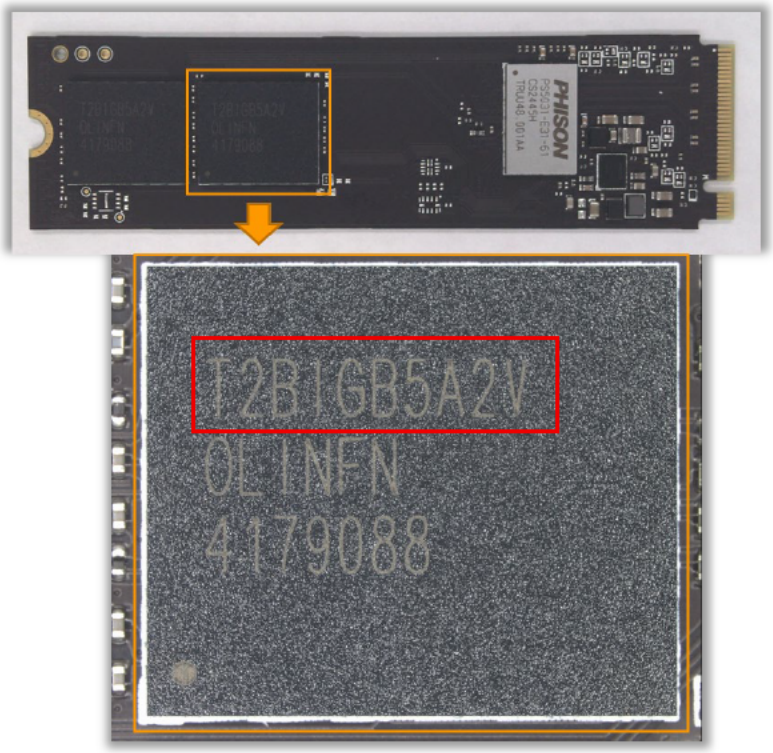
66. On information and belief, KIOXIA's Accused Products are incorporated into products that are also imported, sold for importation into the United States, and/or sold within the United States after importation, such as the Corsair MP700 Elite. For example, the Corsair MP700 Elite is sold with an exemplar KIOXIA Accused Product, the KIOXIA BiCS8 3D TLC (model number T2BIGB5A2V), incorporated into it:

| Specifications: Corsair MP700 Elite 2 TB SSD | |
|---|---|
| Brand: | Corsair |
| Model: | CSSD-F2000GBMP700EHS<br>CSSD-F2000GBMP700ENH (w/o heatsink) |
| Capacity: | 2000 GB (1863 GB usable)<br>48 GB additional overprovisioning |
| Controller: | Phison E31T |
| Flash: | Kioxia 218-Layer 3D TLC BiCS8<br>T2BIGB5A2V |

**Ex. 35** at 2.

67. Photographs of the KIOXIA BiCS8 3D TLC (model number T2BIGB5A2V) that are incorporated into the Corsair MP700 Elite are shown below:

[redacted]




68. KIOXIA's Accused Products are manufactured abroad and available for sale in the United States. On September 20, 2025, the Corsair MP700 Elite product, which incorporates the representative KIOXIA BiCS8 3D TLC (model number T2BIGB5A2V) product, was purchased in the United States on www.amazon.com for $202.58. *See* **Ex. 36** at 1. The Corsair MP700 Elite product was delivered in the United States and received at an address in Summit, New Jersey on September 21, 2025. *See id.*; *see* **Ex. 36-1**.

69. Photos of the product packaging for the Corsair MP700 Elite that was purchased are shown below:

[redacted]


70. The product packaging for the Corsair MP700 Elite product, which incorporates the representative KIOXIA BiCS8 3D TLC (KIOXIA model number T2BIGB5A2V) product, identifies "Corsair Memory, Inc." (*see* ¶ 63 *supra*) and states the product was "Made in Taiwan," demonstrating that KIOXIA's Accused Products are imported:

[redacted]


**B. SK hynix**

71. On information and belief, SK hynix imports, sells for importation, and/or sells within the United States after importation Accused Products, including the exemplar SK hynix Platinum P51 SSD (3D NAND) and H5UG7HME03X020R HBM3 (HBM) products, that infringe one or more claims of the Asserted Patents.

72. On information and belief, SK hynix's Accused Products that infringe one or more claims of the Asserted Patents are manufactured abroad in South Korea and incorporated as components into products that are manufactured abroad in South Korea and Taiwan, including the SK hynix Platinum P51 SSD product and the Nvidia GH200 Grace Hopper Superchip, and then imported, sold for importation, and/or sold within the United States after importation.

73. In a press release available on its website, SK hynix states that, "[b]oasting leading semiconductor memory companies including SK hynix, South Korea heads the memory field in terms of production capacity. The nation commands a majority share of DRAM fabrication

capacity, well ahead of its nearest rivals. South Korea is also the joint leading producer of NAND flash, alongside Japan, where companies like Kioxia play a major role." **Ex. 37** at 3.

74. In another press release dated October 27, 2025, "SK hynix is said to have brought in the first equipment to the Cheongju M15X fab (factory), which it is building as a DRAM production base including High Bandwidth Memory (HBM)." **Ex. 38** at 1.

75. SK hynix's Accused Products are manufactured abroad in South Korea and available for sale in the United States.

**1. SK hynix 3D NAND Product**

76. On September 19, 2025, the SK hynix Platinum P51 SSD product was purchased in the United States on www.newegg.com for $186.56. *See* **Ex. 39** at 1. The product was delivered in the United States and received at an address in Short Hills, New Jersey on September 22, 2025. *See id.*; *see* **Ex. 39-1**.

77. Photos of the product packaging for the SK hynix Platinum P51 SSD product that was purchased are shown below:

[redacted]


78. The product packaging for the SK hynix Platinum P51 SSD product states the product was "Made in Korea," demonstrating that SK hynix's Accused Products are imported:

[redacted]

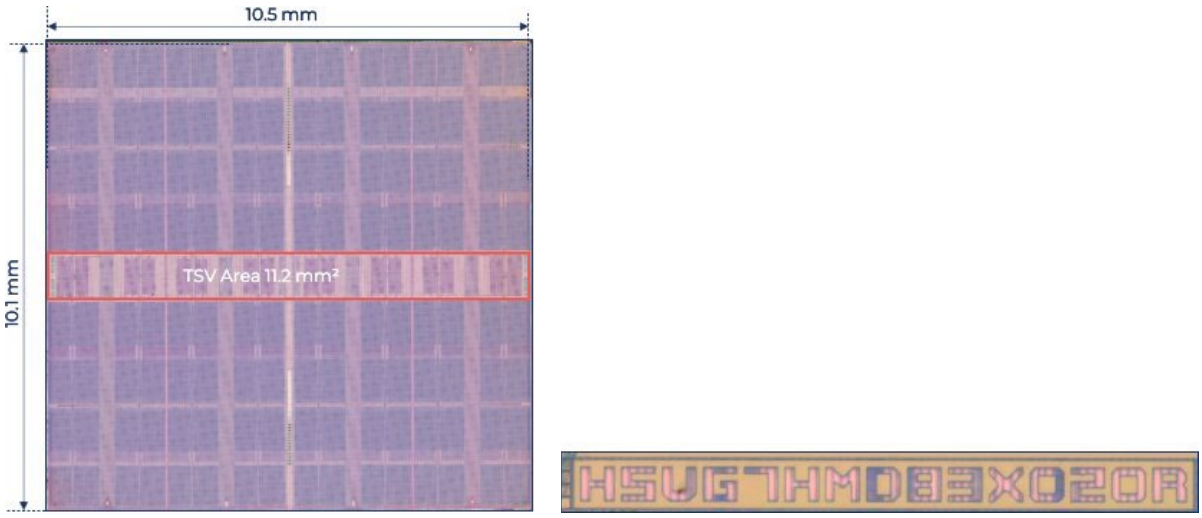
**2. SK hynix HBM Product**

79. On information and belief, the Nvidia GH200 Grace Hopper Superchip comprises the representative SK hynix HBM product (H5UG7HME03X020R) and is manufactured abroad and imported into the United States. On information and belief, SK hynix has reason to know that its HBM products will be incorporated as components into products that are imported, sold for importation, and/or sold within the United States after importation, as SK hynix specifically and knowingly sells its Accused Products to customers in the United States and/or companies that sell their products in the United States, such as Nvidia. SK hynix has sales offices in the United States in at least the following locations, where, on information and belief, it conducts sales activities relating to its HBM products: San Jose, California; Seattle, Washington; Austin, Texas; Houston, Texas; and Raleigh, North Carolina. *See* **Ex. 22** at 1–2; *see also id.* at 1 ("We are securing our place as the leader of the global IT ecosystem of the world"). "SK hynix has already 'sold out' this year's HBM volumes and is said to be the first among the three memory companies to finish preparations for mass production of HBM4 (6th generation) and is negotiating volumes with Nvidia." **Ex. 38** at 2.

80. For example, "[a]ccording to Nvidia, the new edition of the GH200 is the world's first processor to include HBM3e memory. . . . HBM3e is manufactured by SK hynix Inc. using a 10-nanometer process." **Ex. 40** at 2. Furthermore, "[t]he SK hynix H5VG7HMD83X020R was found inside NVIDIA's Grace Hopper Superchip used in the use in Quanta Computer Inc's S74G-2U QuantaGrid server for artificial intelligence (AI) and high-performance computing (HPC) applications. The NVIDIA GH100-888K-A1 Hopper GPU . . . contain[s] six SK hynix 16 GB 4th generation HBM3 DRAM sub-packages from which the SK hynix H5VG7HMD83X020R die, manufactured using the SH hynix's D1z process, was extracted for analysis. . . ." **Ex. 41** at 1. The

[redacted]

die marking on the Nvidia GH100-888K-A1 Hopper GPU shows that it contains the SK hynix H5VG7HMD83X020R:




81. On information and belief, the SK hynix HBM products are manufactured abroad in South Korea at SK hynix's facilities in Icheon and/or Cheongju and shipped to Taiwan for assembly in Nvidia GH200 superchips before being imported into the United States. For example, according to a SK hynix press release, SK hynix "plans to focus on the mass production of next-generation DRAM, including HBM," at its "M15X fab in Cheongju," which "reflects the company's strategic intent to significantly expand its DRAM production capacity beyond Icheon and into Cheongju." **Ex. 42** at 5.

82. Furthermore, on information and belief, the Nvidia GH200 Grace Hopper Superchip comprising the representative SK hynix HBM product is manufactured abroad in Taiwan. For example, based on Nvidia's press releases, the GH200 is manufactured and assembled in Taiwan: "Taiwan manufacturers are among the many system manufacturers worldwide bringing to market a wide variety of systems powered by different combinations of NVIDIA accelerators and processors. These include AAEON, Advantech, Aetina, ASRock Rack, ASUS, GIGABYTE, Ingrasys, Inventec, Pegatron, QCT, Tyan, Wistron and Wiwynn — all featured in Huang's

COMPUTEX keynote address today as key partners." **Ex. 43** at 1. For example, Nvidia further identifies TSMC's 4N manufacturing process as responsible for fabricating the Grace Hopper GPUs: "Built with over 80 billion transistors using a cutting edge TSMC 4N process, Hopper features five groundbreaking innovations that fuel the NVIDIA H200 and H100 Tensor Core GPUs and combine to deliver incredible speedups over the prior generation on generative AI training and inference." **Ex. 44** at 1.

83. Chip markings on the GH200 further indicate Taiwan as the country of origin based on the "TW" identifier, excerpted below. On information and belief, all GH200 chips are thereafter imported from Taiwan.


*Nvidia GH200 Package Front View*
*©Yole Group 2025*

84. On information and belief, Nvidia GH200 chips comprising the representative SK hynix HBM product are imported, sold for importation into the United States, and/or sold within the United States after importation. For example, the Quanta S74G-2U Grace Hopper Superchip System, which comprises the Nvidia GH200 chip that comprises the representative SK hynix HBM product, is available for sale online by Core 4 Solutions for $39,995.00. *See* **Ex. 45** at 1. According to Core 4 Solutions' website, two Quanta S74G-2U Grace Hopper Superchip Systems are currently in stock in the United States as of January 28, 2026. *See id.* On information and belief, the Quanta S74G-2U Grace Hopper Superchip System is available for purchase in the United States as of January 28, 2026. *See* **Ex. 46**.

85. On information and belief, Core 4 Solutions also sells products on www.ebay.com, including the Quanta S74G-2U Grace Hopper Superchip System, which comprises the Nvidia GH200 chip that comprises the representative SK hynix HBM product. *See* **Ex. 47**. On information and belief, the same two Quanta S74G-2U Grace Hopper Superchip Systems that are available for sale on Core 4 Solutions' website are also advertised for sale by Core 4 Solutions on its eBay business page as of January 28, 2026. *Compare* **Exs. 45–46** with **Exs. 47–48**. According to Core 4 Solutions' eBay business page, two Quanta S74G-2U Grace Hopper Superchip Systems are currently in stock in the United States as of January 28, 2026. *See id.* The two Quanta S74G-2U Grace Hopper Superchip Systems are located in "Eden Prairie, Minnesota, United States" and can be delivered to locations within the United States with "[f]ree 2-4 day delivery." *See* **Ex. 48** at 1.

86. On information and belief, Nvidia sells the Nvidia GH200 chip that comprises the representative SK hynix HBM product to customers in the United States. For example, Nvidia's

sales partners include at least AMAX[2] (an affiliate of Hon Hai, headquartered in Fremont, California), Cambridge Computer[3] (based in Waltham, Massachusetts), Exxact Corp. [4] (based in Fremont, California), and Supermicro[5] (based in San Jose, California), all of which sell the Nvidia GH200 chip in the United States. *See* **Ex. 49**; **Ex. 50**; **Ex. 51**; **Ex. 52**; **Ex. 53**.

87. As a further example, Exxact Corp. has provided a quote for the sale of a Grace Hopper System that contains the Nvidia GH200 Grace Hopper chip. *See* **Ex. 54**. The Grace Hopper System is offered for sale for $40,536.99 and ships from Exxact Corp.'s U.S. facility, located at 46221 Landing Parkway, Fremont, California 94538. *See id.*

88. On information and belief, Nvidia further sells GH200 chips directly to U.S. customers through enterprise sales representatives. *See* **Ex. 55**.

## VI. UNLAWFUL AND UNFAIR ACTS OF THE PROPOSED RESPONDENTS

89. On information and belief, the Proposed Respondents import into the United States, sell for importation into the United States, and/or sell within the United States after importation Accused Products in violation of Section 337 by infringement of one or more claims of the Asserted Patents, either literally or under the doctrine of equivalents. The following table summarizes the Asserted Patent claims infringed by each individual Proposed Respondent:

[2] *See* https://www.amax.com/product/acelemax-axg-ar222/?utm_source=nvidia (showing AMAX sells Nvidia GH200 chips and servers comprising Nvidia GH200 chips to U.S. customers); *see also* https://marketplace.nvidia.com/en-us/enterprise/search/?search=Gh200&page=1&locale=en-us&limit=15.

[3] *See* https://www.cambridgecomputer.com/gracehopper/ (stating Cambridge Computer provides a "GH200 Grace Hopper Superchip Early Adopter Program," selling GH200 chips with a list price of $52,000 and a 40% discount on "seed units" to U.S. customers).

[4] *See* https://www.exxactcorp.com/category/NVIDIA-Grace?page=1 (showing Exact Corp. sells Nvidia GH200 chips to U.S. customers through its website).

[5] *See* https://www.supermicro.com/zh_tw/pressreleases/supermicro-starts-shipments-nvidia-gh200-grace-hopper-superchip-based-servers (announcing that Supermicro "starts shipments of Nvidia GH200 Grace Hopper Superchip-Based servers" on October 18, 2023).

[redacted]

| Patent[6] | Claims Asserted Against KIOXIA Accused Products | Claims Asserted Against SK hynix 3D NAND Products | Claims Asserted Against SK hynix HBM Products |
|---|---|---|---|
| '531 Patent | **8**-10, 13-14 | **8**-10, 13-14 | **8**-10, 13-**15**, 20 |
| '1-737 Patent | **1**-2, 4, 5, 7 | **1**-2, 4, 5, 7 | **1**-2, 4, 5, 7, **15**-18, 20 |
| '765 Patent | **15**-18, 20 | **1**, 2, 4, 5, 7 | **1**, 2, 4, 5, 7, **15**-18, 20 |
| '214 Patent | **1**-5, 7, **15**-18, 20 | **1**-5, 7, **15**-18, 20 | - |
| '181 Patent | **1**, **2**, **4**-9, **11**-15 | **1**, **2**, **4**-9, **11**-15 | - |
| '473 Patent | **1**-3, **5**-7, **9**, 11-**13**, 15, 16 | **5**, 6-**9**, 11-**13**, 15, 16 | - |
| '503 Patent | **1**- 6, **15**-19 | **1**- 6, **15**-19 | - |
| '2-737 Patent | **1**-3, 6, 7, **15**-20 | - | - |

### A. KIOXIA

90. On information and belief, KIOXIA imports, sells for importation, and/or sells within the United States after importation Accused Products, such as the KIOXIA BiCS8 3D TLC (model number T2BIGB5A2V) product, that directly and indirectly infringe via inducement, literally and/or under the doctrine of equivalents, at least the claims of the Asserted Patents identified in the chart in paragraph 89, in violation of 35 U.S.C. § 271(a)–(c) and (g) and Section 337(a)(1)(B)(i)-(ii).

91. KIOXIA is not licensed to any of the Asserted Patents.

92. Claim charts comparing the asserted claims of the Asserted Patents to a representative KIOXIA Accused Product, the KIOXIA BiCS8 3D TLC (model number T2BIGB5A2V) product, on an exemplary basis, and including photographs and drawings where applicable, are attached as **Exhibits 56** through **63**. KIOXIA has been on notice of its infringement of the Asserted Patents since at least November 26, 2025, the filing of the related district court case against KIOXIA. *See* § VIII, ¶ 97 *supra*.

[6] Independent claims in bold.

[redacted]

### B. SK hynix

93. On information and belief, SK hynix imports, sells for importation, and/or sells within the United States after importation Accused Products, such as the SK hynix Platinum P51 SSD (3D NAND) and H5UG7HME03X020R HBM3 (HBM) products, that directly and indirectly infringe via inducement, literally and/or under the doctrine of equivalents, the claims of the Asserted Patents identified in the chart in paragraph 89, in violation of 35 U.S.C. § 271(a)–(c) and (g) and Section 337(a)(1)(B)(i)-(ii).

94. SK hynix is not licensed to any of the Asserted Patents.

95. Claim charts comparing the asserted claims of the ’531 Patent, ’1-737 Patent, ’765 Patent, ’214 Patent, ’181 Patent, ’473 Patent, and ’503 Patent to a representative SK hynix Accused Product, the SK hynix Platinum P51 SSD (3D NAND) product, and including photographs and drawings where applicable, are attached as **Exhibits 64** through **70**. Claim charts comparing the asserted claims of the ’531 Patent, ’1-737 Patent, and ’765 Patent to a representative SK hynix Accused Product, the H5UG7HME03X020R HBM3 (HBM) product, and including photographs and drawings where applicable, are attached as **Exhibits 71** through **73**. SK hynix has been on notice of its infringement of the Asserted Patents since at least November 26, 2025, the filing of the related district court cases against SK hynix. *See* § VIII, ¶ 97 *supra*.

## VII. CLASSIFICATION OF THE ACCUSED PRODUCTS UNDER THE HARMONIZED TARIFF SCHEDULE

96. On information and belief, the Proposed Respondents’ infringing Accused Products are imported into the United States under at least the following headings and subheadings of the Harmonized Tariff Schedule of the United States (“HTSUS”): 8542.32.0036 and 8542.32.0051. These HTSUS classifications are intended for illustration only and are not intended to restrict the scope of this Investigation or any exclusion order or other remedy ordered by the Commission.

[redacted]

## VIII. RELATED LITIGATION

97. The Asserted Patents are currently the subject of the following litigations:

- *MonolithIC 3D™ Inc. v. KIOXIA Corporation*, Case No. 2:25-cv-001160 (E.D. Tex.), filed on November 26, 2025;
- *MonolithIC 3D™ Inc. v. SK hynix Inc.*, Case No. 2:25-cv-001167 (E.D. Tex.), filed on November 26, 2025; and
- *MonolithIC 3D™ Inc. v. SK hynix Inc.*, Case No. 2:25-cv-001176 (E.D. Tex.), filed on November 26, 2025.

98. To Complainant's knowledge, the alleged unfair methods of competition and unfair acts, or the subject matter thereof, are not and have not been the subject of any other court or agency litigation.

## IX. THE DOMESTIC INDUSTRY

99. In accordance with Sections 337(a)(2) and (a)(3), a domestic industry exists and/or is in the process of being established in the United States in connection with each of the Asserted Patents comprising quantitatively and qualitatively investments in the United States in (A) plant and equipment related to products that practice the Asserted Patents, (B) employment of labor and capital related to products that practice the Asserted Patents, and (C) substantial investments in engineering and research and development of the Asserted Patents and products that practice the Asserted Patents.

100. MonolithIC 3D relies upon its licensee, [redacted] to satisfy the domestic industry requirement. In particular, a domestic industry exists and/or is in the process of being established as a result of [redacted]

[redacted]

significant investment in plant and equipment, significant employment of labor and capital, and substantial investments in engineering and research and development with respect to its at least [redacted], which are represented by the representative [redacted] and the representative [redacted], and include at least [redacted] ("Domestic Industry Products") that practice and are protected by the Asserted Patents. 19 U.S.C. § 1337(a)(3)(A)–(C). On [redacted], MonolithIC 3D and [redacted]. Pursuant to Commission Rule 210.12(a)(9)(iv), Complainant has attached as **Confidential Exhibit 74C** a copy of the patent license agreement. By virtue of a license granted by MonolithIC 3D, [redacted] is fully licensed to practice the Asserted Patents. A domestic industry exists under Section 337(a)(2) and 337(a)(3) at least based on [redacted] significant and substantial investments since [redacted].

### A. Technical Prong

101. [redacted] makes significant and substantial investments in plant and equipment, labor and capital, and engineering and research and development with respect the Domestic Industry Products, which practice at least the following claims of the Asserted Patents:

| Asserted Patents | Exemplary Practiced Claims (3D NAND Products)[7] | Exemplary Practiced Claims (HBM Products) |
|---|---|---|
| '531 Patent | **8,** 10, 14 | **8,** 9, 13, 14, **15**, 16, 20 |
| '1-737 Patent | **1, 6** | **1,** 2, 4, 5, 7, **15**, 16-18, 20 |
| '765 Patent | **1**, 6 | **1**, 2, 4, 5, 7, **8**, 9-12, 14-18, 20 |
| '214 Patent | **1,** 2-5, 7, **15**, 16-18, 20 | - |
| '181 Patent | **1**, **2**, **4**, 5-9, **11**, 12-15 | - |

[7] Independent claims in bold.

| Asserted Patents | Exemplary Practiced Claims (3D NAND Products)[7] | Exemplary Practiced Claims (HBM Products) |
|---|---|---|
| '473 Patent | **5**, 7, **9**, 11, 12, **13**, 16 | - |
| '503 Patent | **1**, 3, 5, **15**, 17, 19 | - |
| '2-737 Patent | **15**, 16-19 | - |

102. Claim charts demonstrating how the exemplary Domestic Industry Products practice these claims of the Asserted Patents are attached as **Confidential Exhibits 75C** through **85C**.

**B. Economic Prong**

103. A domestic industry as defined by 19 U.S.C. § 1337(a)(3)(A)–(C) exists in the United States with respect to the Domestic Industry Products that practice the Asserted Patents. [redacted] has made significant investments in plant and equipment, significant employment of labor and capital, and substantial investments in exploitation of the Asserted Patents in the United States with respect to the Domestic Industry Products.

104. [redacted] is fully licensed to practice each of the Asserted Patents. *See* **Confidential Ex. 74C**.

105. [redacted] has invested—and continues to invest—millions of dollars in the United States in labor and capital, plant and equipment, and research and development relating to the Domestic Industry Products. Details relating to [redacted] domestic expenditures on plant and equipment, labor and capital, and research and development are set forth in **Confidential Exhibit 86C**.

106. [redacted] domestic investments and activities are significant and substantial both in absolute terms and relative to [redacted] overall operations. [redacted] investments and activities are attributable to the Domestic Industry Products and represent significant domestic

added value, particularly where the protected articles are designed, developed, engineered, and tested in the United States.

107. Alternatively, a domestic industry as defined by 19 U.S.C. § 1337(a)(2) is "in the process of being established" with respect to the Domestic Industry Products that practice the Asserted Patents. [redacted] domestic investments and activities demonstrate it is taking the necessary steps to establish a domestic industry in the United States and that there is a significant likelihood that the domestic industry requirement will be satisfied in the future. *See* **Confidential Exhibit 86C**.

## X. RELIEF REQUESTED

108. The Proposed Respondents have infringed and will continue to infringe the Asserted Patents as specified in Sections V and VI above unless the Commission prohibits the importation into the United States, the sale for importation, and the sale within the United States after importation of the Accused Products.

109. Accordingly, Complainant respectfully requests that the United States International Trade Commission:

(a) institute an immediate investigation pursuant to Section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, into the Proposed Respondents' violations of Section 337 arising from the importation into the United States, the sale for importation into the United States, and/or the sale within the United States after importation of certain NAND and DRAM memory chips;

(b) schedule and conduct a hearing, pursuant to 19 U.S.C. § 1337(c), for purposes of receiving evidence and hearing argument concerning whether the Proposed Respondents have violated Section 337 and, following the hearing, find that the Proposed Respondents have violated Section 337;

[redacted]

(c) issue a permanent limited exclusion order, pursuant to 19 U.S.C. § 1337(d)(1), excluding from entry into the United States certain NAND and DRAM memory chips by the Proposed Respondents or any of their affiliate companies, parents, subsidiaries, licensees, or other related business entities, or their successors or assigns that infringe, literally and/or under the doctrine of equivalents, one or more claims of the Asserted Patents, including, without limitation, the Accused Products identified in this Complaint and the exhibits hereto;

(d) issue permanent orders, pursuant to 19 U.S.C. § 1337(f), directing the Proposed Respondents and any of their principals, stockholders, officers, directors, employees, agents, distributors, controlled (whether by stock ownership or otherwise) and majority-owned business entities, successors, and assigns to cease and desist from importing, selling, offering for sale, marketing, advertising, demonstrating, packaging, warehousing inventory for distribution, distributing, licensing, transfer, soliciting of any sale, or using in the United States certain NAND and DRAM memory chips that infringe, literally and/or under the doctrine of equivalents, one or more claims of the Asserted Patents, including, without limitation, the Accused Products identified in this Complaint and the exhibits hereto;

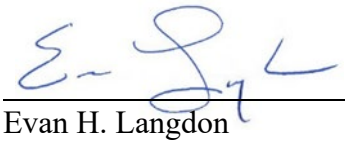
(e) impose a bond, pursuant to 19 U.S.C. § 1337(j), on the Proposed Respondents' importation of NAND and DRAM memory chips that infringe any claim of the Asserted Patents sufficient to protect Complainant from further injury during the 60-day Presidential review period; and

[redacted]

(f) grant all such other and further relief as is appropriate under the law, based upon the facts complained of herein and as determined by the Investigation.

Dated: February 17, 2026

Respectfully submitted,



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