IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND-ODESSA DIVISION

WECREVENTION, INC.,		§	
	Plaintiff,	§	No. 7:25-CV-458
v.		§	**JURY TRIAL DEMANDED**
APPLE INC.,		§	
	Defendant.	§	

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff, WeCrevention, Inc. ("WeCrevention" or "Plaintiff") for its Complaint against Apple, Inc. ("Apple" or "Defendant"), alleges as follows:

THE PARTIES

1. WeCrevention is incorporated under the laws of the State of Texas, with places of business located at 5900 Balcones Dr Ste 100, Austin, TX 78731 and 5851 Legacy Circle, 6th Floor, Plano, Texas 75024.

2. Defendant Apple, Inc. is a corporation organized and existing under the laws of California, with one or more regular and established places of business in this District at least at 12545 Riata Vista Circle, Austin, Texas 78727; 12801 Delcour Drive, Austin, Texas 78727; 6800 W Parmer Lane, Austin, Texas 78729, and 3121 Palm Way, Austin, Texas 78758. Apple may be served with process through its registered agent, the CT Corp System, at 1999 Bryan St., Ste. 900 Dallas, Texas 75201-3136. In November 2019, Apple stated that it had approximately 7,000 employees in Austin and that it expected to open, in 2022, a $1 billion, 3 million-square-foot

campus with capacity for 15,000 employees.[1] In August 2025, Apple stated that "construction continues on Apple's second campus in Austin," and that "Apple has more than 13,000 team members across Texas, including thousands already working from the three completed office buildings, which exceed 1 million square feet," and that "[t]he three buildings currently under construction include an expansive new R&D lab space for Apple's Hardware Engineering, Hardware Technology, and Software Engineering teams."[2] Apple is registered to do business in the State of Texas and has been since at least May 16, 1980.

JURISDICTION AND VENUE

3. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq*. This Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331, 1332, 1338, and 1367.

4. This Court has specific and personal jurisdiction over the Defendant consistent with the requirements of the Due Process Clause of the United States Constitution and the Texas Long Arm Statute. Upon information and belief, the Defendant has sufficient minimum contacts with the forum because Defendant transacts substantial business in the State of Texas and in this Judicial District. Further, Defendant has, directly or through subsidiaries or intermediaries, committed and continues to commit acts of patent infringement in the State of Texas and in this Judicial District as alleged in this Complaint, as alleged more particularly below.

5. Venue is proper in this Judicial District pursuant to 28 U.S.C. §§ 1400(b) and 1391(b) and (c) because Defendant is subject to personal jurisdiction in this Judicial District, has committed acts of patent infringement in this Judicial District, and has a regular and established

[1] *See* https://www.apple.com/newsroom/2019/11/apple-expands-in-austin/.
[2] *See* https://www.apple.com/newsroom/2025/08/apple-increases-us-commitment-to-600-billion-usd-announces-ambitious-program/.

place of business in this Judicial District. Defendant, through its own acts, makes, uses, sells, and/or offers to sell infringing products within this Judicial District, regularly does and solicits business in this Judicial District, and has the requisite minimum contacts with the Judicial District such that this venue is a fair and reasonable one.

PATENTS-IN-SUIT

6. On December 1, 2015, the United States Patent and Trademark Office ("USPTO") duly and legally issued U.S. Patent No. 9,201,834 ("the '834 Patent") entitled "Reconfigurable high speed memory chip module and electronic device with a reconfigurable high speed memory chip module." A true and correct copy of the '834 Patent is attached hereto as Exhibit A.

7. On May 4, 2021, the USPTO duly and legally issued U.S. Patent No. US 10,998,017 (the '017 Patent) entitled "Dynamic random access memory applied to an embedded display port." A true and correct copy of the '017 Patent is attached hereto as Exhibit B.

8. On February 6, 2024, the USPTO duly and legally issued U.S. Patent No. 11,894,098 (the '098 Patent) entitled "Dynamic random access memory applied to an embedded display port." A true and correct copy of the '098 Patent is attached hereto as Exhibit C.

9. On November 26, 2024, the USPTO duly and legally issued U.S. Patent No. 12,154,652 (the '652 Patent) entitled "Dynamic random access memory applied to an embedded display port." A true and correct copy of the '652 Patent is attached hereto as Exhibit D.

10. On October 20, 2015, the USPTO duly and legally issued U.S. Patent No. 9,164,942 (the '942 Patent) entitled "High speed memory chip module and electronics system device with a high speed memory chip module." A true and correct copy of the '942 Patent is attached hereto as Exhibit E. The '834 Patent, the '017 Patent, the '098 Patent, the '652 Patent, and the '942 Patent shall be collectively known as the "Patents-in-Suit."

11. WeCrevention is the sole and exclusive owner of all right, title, and interest in and to the Patents-in-Suit, and holds the exclusive right to take all actions necessary to enforce its rights to the Patents-in-Suit, including the filing of this patent infringement lawsuit. WeCrevention also has the right to recover all damages for infringement of the Patents-in-Suit as appropriate under the law.

12. WeCrevention has at all times complied with the marking provisions of 35 U.S.C. § 287 with respect to the Patents-in-Suit. On information and belief, any and all prior assignees and licensees have also complied with the marking provisions of 35 U.S.C. § 287.

INFRINGEMENT ALLEGATIONS

13. The inventions claimed in the Patents-in-Suit are generally directed to electronics devices comprising memory chips, as well as memory chip modules. The ’834 Patent was developed by Weng-Dah Ken, Chao-Chun Lu, and Jan-Mye Sung. The ’017 Patent, the ’098 Patent, and the ’652 Patent were developed by Der-Min Yuan, Yen.-An Chang, and Wei-Ming Huang. The ’942 Patent was developed by Weng-Dah Ken and Nicky Lu. Apple has manufactured, used, marketed, distributed, sold, offered for sale, exported from, and imported into the United States, products that infringe the Patents-in-Suit. These products include at least all versions and variants of Apple products that include LPDDR5 DRAM since September of 2019, including without limitation, the iPhone 14 or later (*e.g.*, iPhone 14; iPhone 14 Pro; iPhone 14 Pro Max; iPhone 15; iPhone 15 Plus; iPhone 15 Pro; iPhone 15 Pro Max; iPhone 16; iPhone 16 Plus; iPhone 16 Pro; and iPhone 16 Pro Max; iPhone Air; iPhone 17 Pro; and iPhone 17 Pro Max), the MacBook (*e.g.*, MacBook Air (M2, 2022); MacBook Air (M3, 2024); 13-inch MacBook Pro (M2, 2022); MacBook Pro (14-inch, M3 Pro or M3 Max, Nov 2023); and MacBook Pro (16-inch,

M3 Max, late 2023), and the iPad (*e.g.*, iPad (11th generation); iPad Air; and iPad Pro) ("the Accused Products").

14. Upon information and belief, Apple has had knowledge and notice of the Patents-in-Suit, and its infringement thereof, since the patents issued. Apple, as a technology company, regularly monitors memory module technology advances, and it monitored or was otherwise aware of Plaintiff's patented inventions, especially due to their impact on Apple's own technology and consumer electronics business. Alternatively, to the extent that Apple avoided or otherwise lacked actual knowledge of the Patents-in-Suit and its infringement thereof, it was willfully blind. Upon information and belief, to the extent it lacked actual knowledge of infringement, prior to the filling of this action, Apple deliberately avoided learning of infringement, despite subjectively believing that there was a high probability that it infringed Plaintiff's patents, and specifically the Patents-in-Suit, and was therefore willfully blind. Upon information and belief, Apple has adopted a policy or practice of not reviewing the patents of others, including those related to Apple's specific industry and of Plaintiff in particular, thereby remaining willfully blind to its infringement of the Patents-in-Suit. Upon information and belief, Apple lacks written policies disseminated to employees regarding monitoring or avoidance of patent infringement by Apple and lacks mechanisms for employees to report patents which they believe Apple may infringe. Upon information and belief, Apple and its employees understood that there was a high likelihood that patents filed on innovations by Plaintiff read on the Accused Products.

15. At least as of the commencement of this action, Apple has both actual knowledge and notice of the Patents-in-Suit, and it continues to willfully infringe the Patents-in-Suit.

COUNT I
(Infringement of the '834 Patent)

16. Paragraphs 1 through 15 are incorporated by reference as if fully set forth herein.

17. WeCrevention has not licensed or otherwise authorized Apple to make, use, offer for sale, sell, or import any products that embody the inventions of the ’834 Patent.

18. Apple has and continues to directly infringe the ’834 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States products that satisfy each and every limitation of one or more claims of the ’834 Patent.

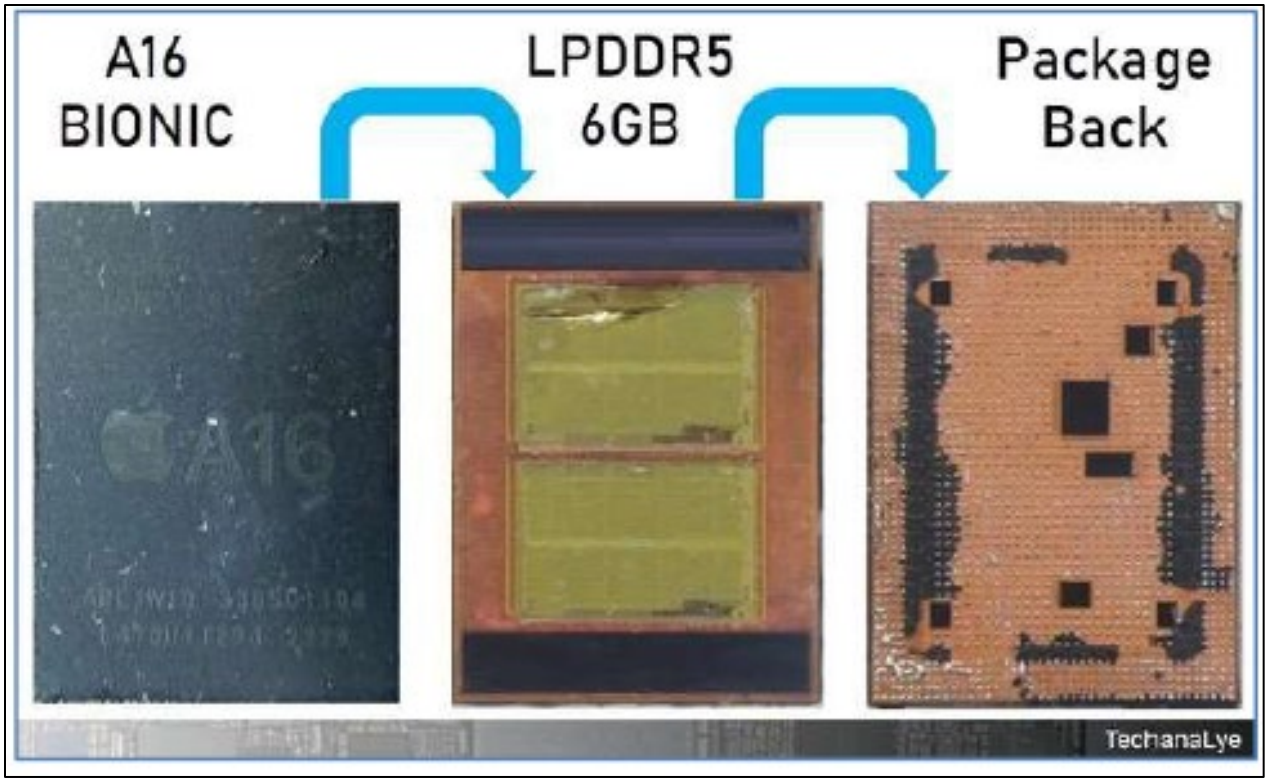
19. Apple directly infringes at least claim 21 of the ’834 Patent by making, using, offering to sell, selling, and/or importing into the United States products that comprise an electronics device with a reconfigurable high speed memory chip module, the electronics system device comprising: an application-specific integrated circuit (ASIC) processor; a type of memory cell array group, wherein the type of memory cell array group comprises multiple memory cell array ICs; a first transmission bus coupled to the type of memory cell array group having a first programmable transmitting or receiving data rate, a first programmable transmitting or receiving signal swing corresponding to firmware or software comprised in the ASIC processor; a logic unit coupled to the first transmission bus for accessing the type of memory cell array group through the first transmission bus; and a second transmission bus coupled between the logic unit and the ASIC processor having a second programmable transmitting or receiving data rate, a second programmable transmitting or receiving signal swing associated to the firmware or the software comprised in the ASIC processor.

20. The Accused Products include an electronics device with a reconfigurable high speed memory chip module. For example, the iPhone 14 Pro, which is believed to be representative of all accused products for purposes of Plaintiff’s infringement allegations, is a smartphone, which

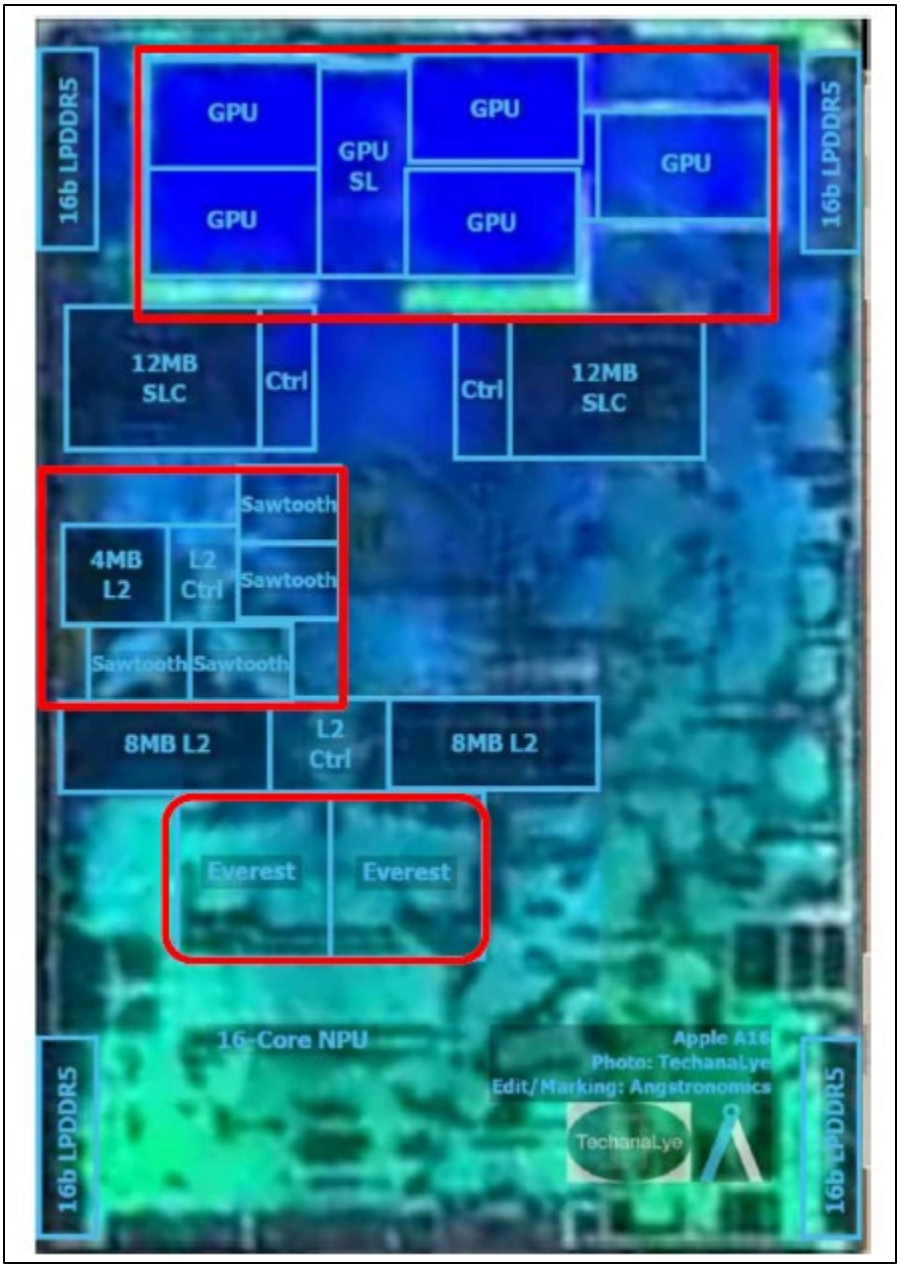
is an electronics device. The iPhone 14 Pro includes an A16 Bionic System-On-Chip ("A16") with on-board 6 GB LPDDR5 DRAM, which is a reconfigurable high speed memory chip module.

See https://www.macrumors.com/2022/09/16/iphoen-14-pro-faster-6gb-lpddr5-memory/.

21. The Accused Products further include an application-specific integrated circuit ("ASIC") processor. For example, Apple's iPhone 14 Pro includes an A16 Bionic chip ("A16") that includes an ASIC processor that having at least two "Everest" high-performance cores, four "Sawtooth" energy-efficient cores, and five GPU cores, as shown below.

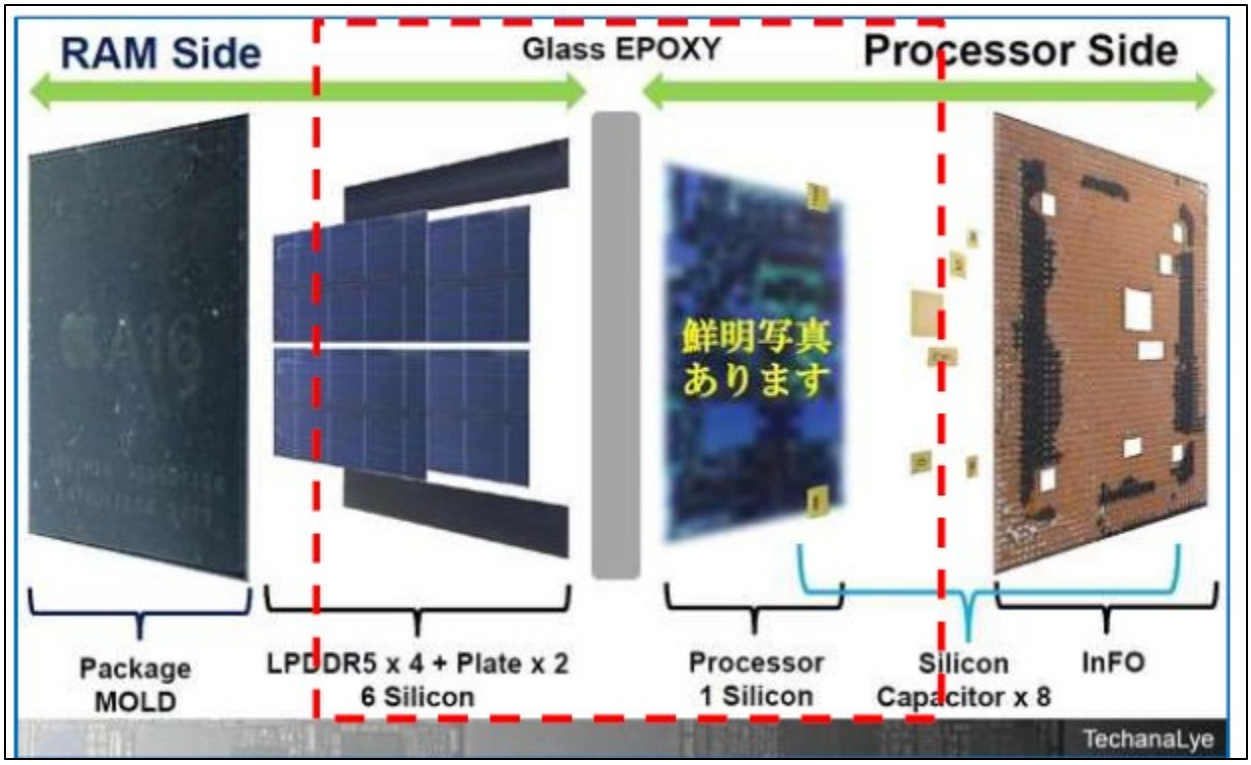


See https://eetimes.itmedia.co.jp/ee/articles/2210/25/news048.html.



See https://www.angstronomics.com/p/apple-a16-die-analysis (annotated).

22. The Accused Products further include a type of memory cell array group, wherein the type of memory cell array group comprises multiple memory cell array ICs. For example, the LPDDR5 DRAM of the A16 includes a cell array group comprised of multiple memory cell array ICs. The LPDDR5 DRAM is coupled to the "Processor Silicon" of the A16 through Glass Epoxy, as shown below.



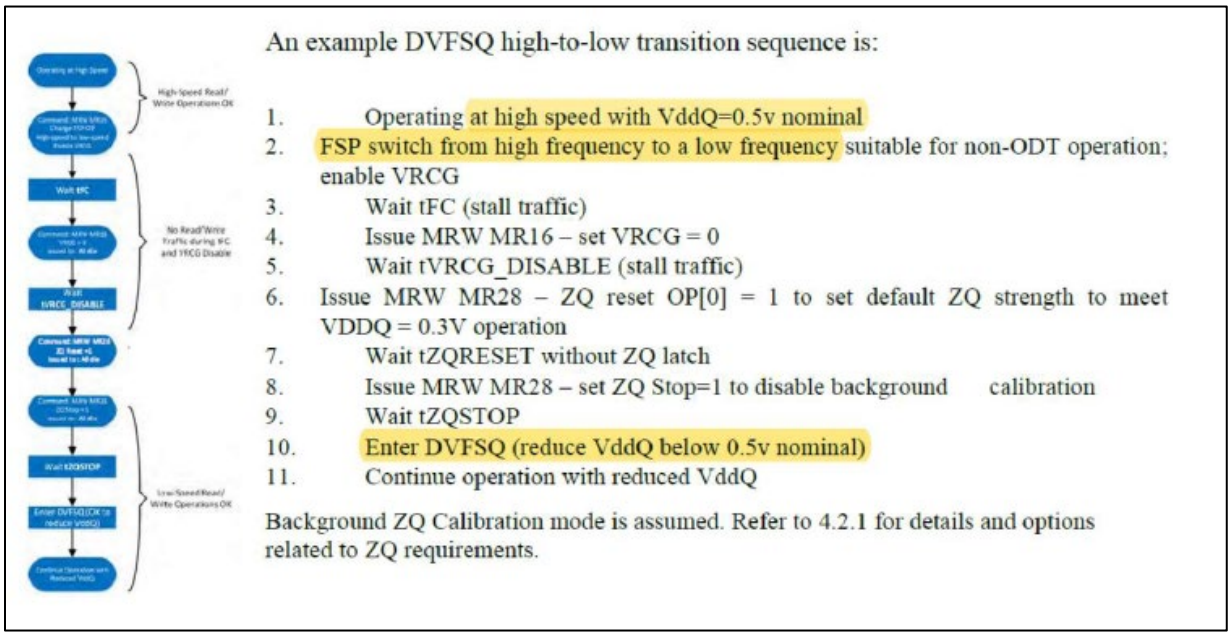
See https://eetimes.itmedia.co.jp/ee/articles/2210/25/news048.html.

23. On information and belief, the Accused Products comprise a first transmission bus coupled to the type of memory cell array group having a first programmable transmitting or receiving data rate, a first programmable transmitting or receiving signal swing corresponding to firmware or software comprised in the ASIC processor. For example, Apple's iPhone 14 Pro A16 includes a memory bus coupled to the memory cell array group of the LPDDR5 DRAM, as well as an integrated memory controller ("IMC") which is programmable via firmware or software stored in the ASIC to change the transmitting or receiving data rate and signal swing associated with the memory bus. For example, upon information and belief:

> "The transistor count has gone up a few percent to 16 billion (from 15 billion), and it's likely that most of that higher budget is spent in the new display engine (which manages the iPhone 14 Pro's display down to 1Hz in always-on display mode and can crank it up to 2,000 nits in bright sunlight), **memory controller**, and image signal processor."

See https://www.macworld.com/article/1073243/a16-processor-cpu-gpu-lpddr5-memory-performance.html (emphasis added).

24. LPDDR5 DRAM, such as that of the A16, supports Dynamic Voltage and Frequency Scaling ("DVFS") consisting of two modes ("DVFSC" and "DVFSQ"), which allows the memory operating frequency and voltages to be controllably adjusted, such as by lowering one or both of these parameters to reduce energy consumption during times when high performance is not required. *See* JEDED Standard – Lower Power Double Data Rate 5 (LPDDR5) Specification, JESD209-5B, June 2021 at 414; *see also* JESD209-5C at 430. In DVFSQ mode "LPDDR5 devices can allow the VDDQ to be ramped during operation including Read/Write transactions. Exact speeds and levels are to be determined by the system builder." JESD509-5B at 416; *see also* JESD209-5C at 435.



See JESD509-5B at 416; *see also* JESD209-5C at 436.Since the I/O circuitry of the LPDDR5 DRAM is coupled to the memory bus of the A16, frequency and VDDQ adjustment necessarily result in signal frequency and voltage scaling on the memory bus.

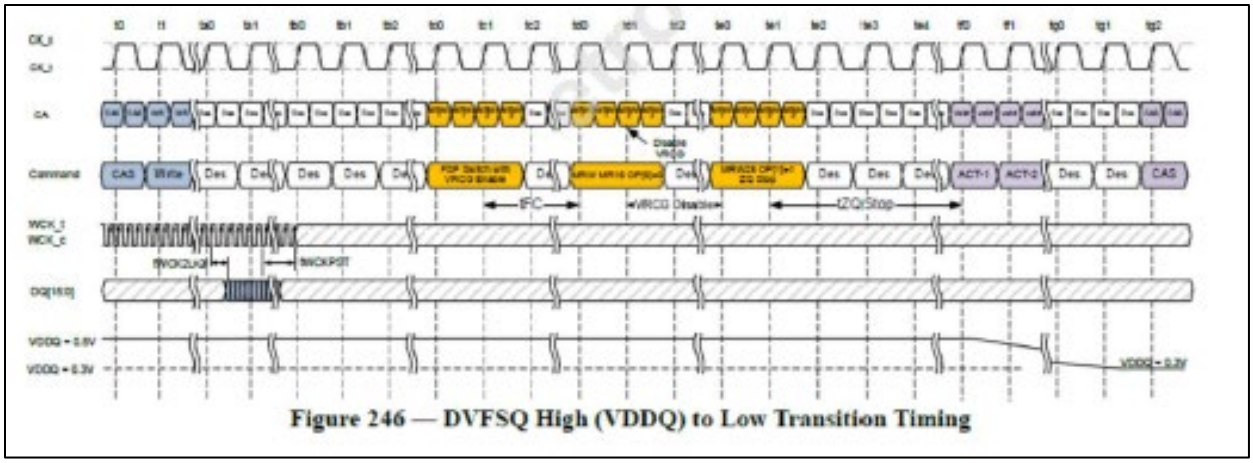


Figure 246 — DVFSQ High (VDDQ) to Low Transition Timing

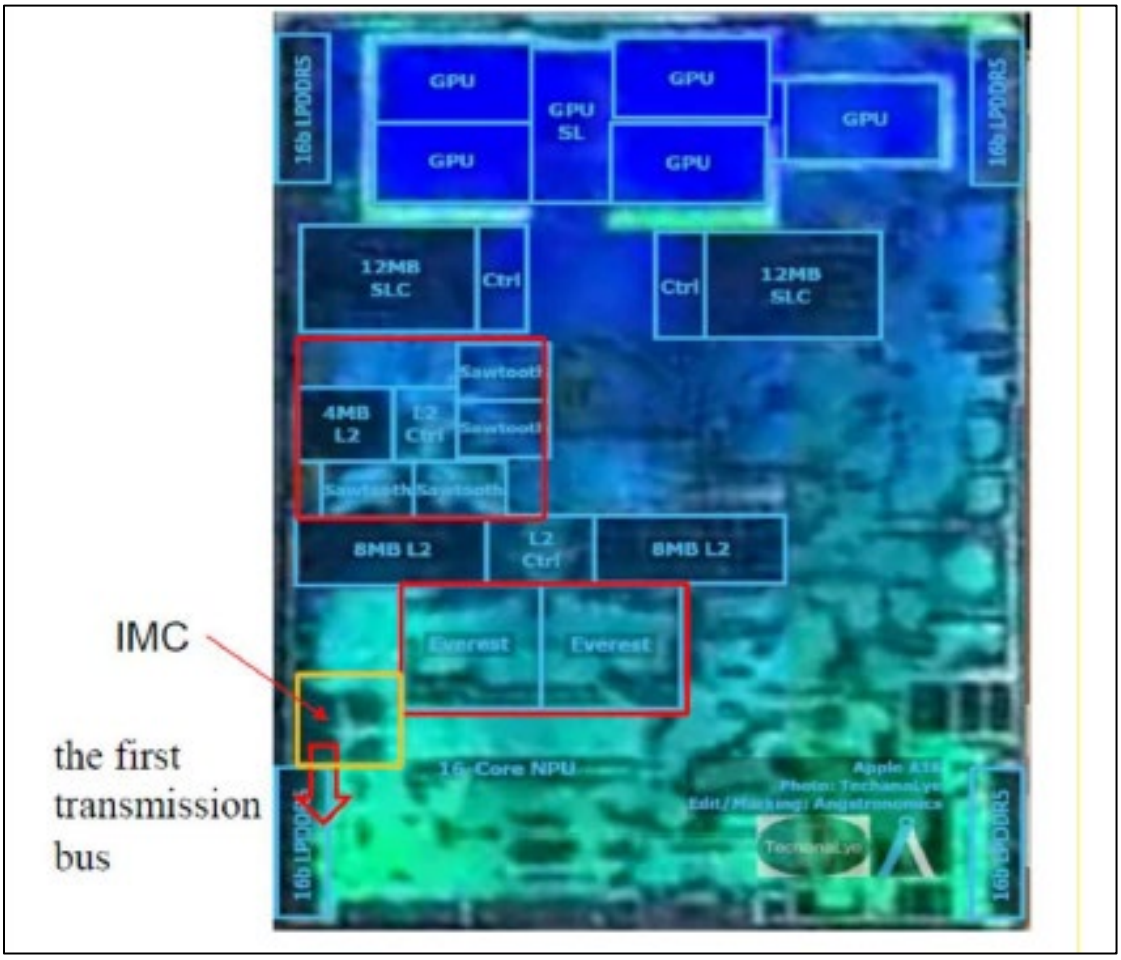
See JESD209-5B at 417; *see also* JESD209-5C at 436.

25. On information and belief, the Accused Products further include a logic unit coupled to the first transmission bus for accessing the type of memory cell array group through the first transmission bus. For example, on information and belief, the IMC of the A16 Bionic processor is coupled to the memory bus (*i.e.*, a first transmission bus) for accessing the LPDDR5 DRAM and:

> "The transistor count has gone up a few percent to 16 billion (from 15 billion), and it's likely that most of that higher budget is spent in the new display engine (which manages the iPhone 14 Pro's display down to 1Hz in always-on display mode and can crank it up to 2,000 nits in bright sunlight), **memory controller**, and image signal processor."

See https://www.macworld.com/article/1073243/a16-processor-cpu-gpu-lpddr5-memory-performance.html.

26. On information and belief, a configuration of that the IMC is shown below.



See https://www.angstronomics.com/p/apple-a16-die-analysis (annotated).

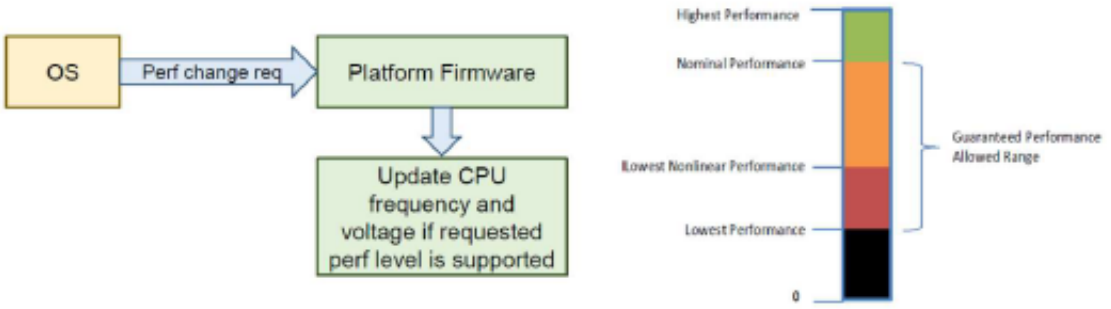
27. On information and belief, the Accused Products further comprise a second transmission bus coupled between the logic unit and the ASIC processor having a second programmable transmitting or receiving data rate, a second programmable transmitting or receiving signal swing associated to the firmware or the software comprised in the ASIC processor. For example, Apple's iPhone 14 Pro's A16 comprises an ARMv8.6-A CPU. *See* https://github.com/llvm/llvm-project/blob/main/llvm/unittests/TargetParser/TargetParserTest.cpp.

28. On information and belief, the ASIC processor of the A16 accesses the LPDDR5 DRAM through the IMC via a second transmission bus coupled between the IMC and the ASIC processor.

29. On information and belief, the A16 supports Collaborative Processor Performance Control ("CPPC") or a similar mechanism that allows for programmable alteration of on-chip parameters, such as operating frequency and/or voltage, associated with one or more CPU/GPU cores of the A16. *See* https://neoverse-reference-design.docs.arm.com/en/latest/features/power/cppc-test.htm. CPPC, for instance, is used for transmitting or receiving signal swings with firmware or software, as shown below.

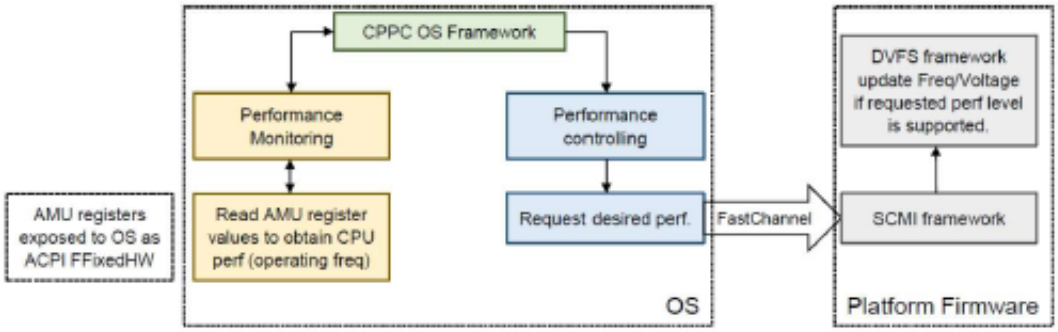
Introduction to CPPC

- A mechanism for the OS to manage the performance of the processor core on a contiguous and abstract performance scale.



CPPC for ARM Platform

- Consist of two part:
  - Monitoring Processor Performance
  - Controlling Processor Performance



An example of DVFS Configuration in Platform

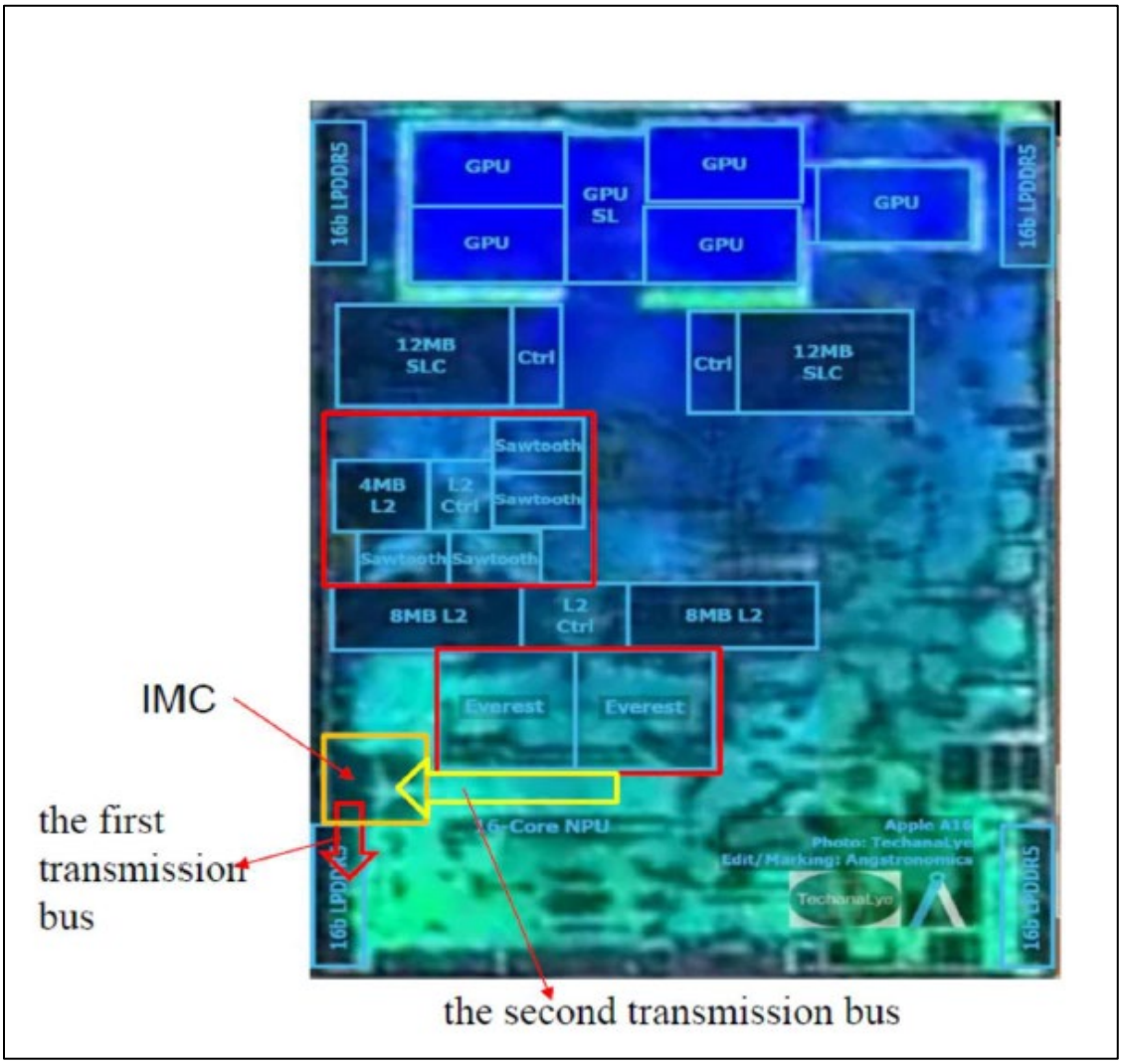
- The DVFS configuration should have voltage/frequency mapping for performance level.
- The Performance level to frequency mapping in ACPI should match with the SCP firmware DVFS configuration.

```
static struct mod_dvfs_opp opps[] = {
    { .level =  65UL, .frequency = 1313 * FWK_KHZ, .voltage = 800 },
    { .level =  75UL, .frequency = 1531 * FWK_KHZ, .voltage = 850 },
    { .level =  85UL, .frequency = 1750 * FWK_KHZ, .voltage = 900 },
    { .level = 105UL, .frequency = 2100 * FWK_KHZ, .voltage = 950 },
    { .level = 130UL, .frequency = 2600 * FWK_KHZ, .voltage = 1000 },
    { 0 }
};
```

See https://static.linaro.org/connect/lvc21/presentations/lvc21-219.pdf.

30. Additionally, on information and belief, the "Everest" high-performance cores could access LPDDR5 DRAM through the IMC, and therefore there is a second transmission bus coupled between the IMC and the high-performance cores.

31. Since the operating frequency and voltage of one or more cores and other circuitry of the A16 are believed to be adjustable, the transmitting or receiving data rate and signal swing of the second transmission bus connected to these cores and circuitry are inherently adjustable as well. On information and belief, these parameters are adjustable via the firmware or software in the A16.



See https://www.angstronomics.com/p/apple-a16-die-analysis (annotated).

32. Apple indirectly infringes one or more claims of the ’834 Patent by knowingly and intentionally inducing others, including Apple customers and end-users of the Accused Products and products that include the Accused Products, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States products that include infringing technology, such as the Accused Products.

33. Apple indirectly infringes one or more claims of the ’834 Patent, as provided by 35 U.S.C. § 271(b), by inducing infringement by others, such as Apple’s customers and end-users, in this Judicial District and elsewhere in the United States. For example, Apple’s customers and end-users directly infringe, either literally or under the doctrine of equivalents, through their use of the inventions claimed in the ’834 Patent. Apple induces this direct infringement through its affirmative acts of manufacturing, selling, distributing, and/or otherwise making available the Accused Products, and providing instructions, documentation, and other information to customers and end-users urging them to use the Accused Products in an infringing manner, including technical support, marketing, product manuals, advertisements, and online documentation. Because of Apple’s inducement, Apple’s customers and end-users use Accused Products and directly infringe the ‘834 Patent in a way Apple intends. Apple performs these affirmative acts with knowledge of the ’834 Patent and with the intent, or willful blindness, that the induced acts directly infringe the ’834 Patent.

34. Apple indirectly infringes one or more claims of the ’834 Patent, as provided by 35 U.S.C. § 271(c), by contributing to direct infringement by others, such as customers and end-users, in this Judicial District and elsewhere in the United States. Apple’s affirmative acts of selling and offering to sell the Accused Products in this Judicial District and elsewhere in the United States and causing the Accused Products to be manufactured, used, sold and offered for sale contributes

to others' use and manufacture of the Accused Products, such that the '834 Patent is directly infringed by others. The accused components within the Accused Products are material to the invention of the '834 Patent, are not staple articles or commodities of commerce, have no substantial non-infringing uses, and are known by Apple to be especially made or adapted for use in the infringement of the '834 Patent. Apple performs these affirmative acts with knowledge of the '834 Patent and with intent, or willful blindness, that they cause the direct infringement of the '834 Patent.

35. WeCrevention has suffered damages as a result of Defendant's direct and indirect infringement of the '834 Patent in an amount to be proved at trial.

COUNT II
(Infringement of the '017 Patent)

36. Paragraphs 1 through 35 are incorporated by reference as if fully set forth herein.

37. WeCrevention has not licensed or otherwise authorized Apple to make, use, offer for sale, sell, or import any products that embody the inventions of the '017 Patent.

38. Apple has and continues to directly infringe the '017 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States products that satisfy each and every limitation of one or more claims of the '017 Patent.

39. For example, Apple directly infringes at least claim 1 of the '017 Patent by making, using, offering to sell, selling, and/or importing into the United States products that comprise a dynamic random access memory ("DRAM"), comprising: a DRAM core cell, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V; and a peripheral circuit electrically connected to the DRAM core cell,

wherein the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is lower than 1.1V, and wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell; wherein the first voltage and the second voltage are capable of making the DRAM be applied to an embedded display port (eDP).

40. The Accused Products include a dynamic random access memory (DRAM) powered by external voltage source. For example, the iPhone 14 Pro includes rechargeable battery to supply voltage and 6 GB LPDDR5 DRAM, which is a dynamic random access memory. *See* https://www.macrumors.com/2022/09/16/iphoen-14-pro-faster-6gb-lpddr5-memory.

41. The Accused Products further include a DRAM core cell, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V. *See*, *e.g.*, JESD209-5B at Table 6; *see also* JESD209-5C at 430-439. The LPDDR5 DRAM of the A16 supports DVFS, including a DVFSC mode which permits the IMC to change the power supply voltage to peripheral circuitry and certain portions of the core. JESD209-5B at 414-416; *see also* JESD209-5C at 430-439. Specifically, when DVFSC mode is enabled, power may be provided from either a high voltage rail VDD2H or a low voltage rail VDD2L, both of which are typically less than 1.1V.

> "LPDDR5 Dynamic Voltage and Frequency Scaling (DVFS) consists of two modes intended to reduce the LPDRAM energy consumption. The two modes are **DVFSC (DVFS Core)** and DVFSQ (DVFS VDDQ)."
>
> "In DVFSC mode, when enabled by MR19 OP[1:0]=01B, the LPDRAM may operate internal circuitry from either the **VDD2H rail or the VDD2L rail**."

See JESD209-5B at 414 (emphasis added); *see also* JESD209-5C at 430.

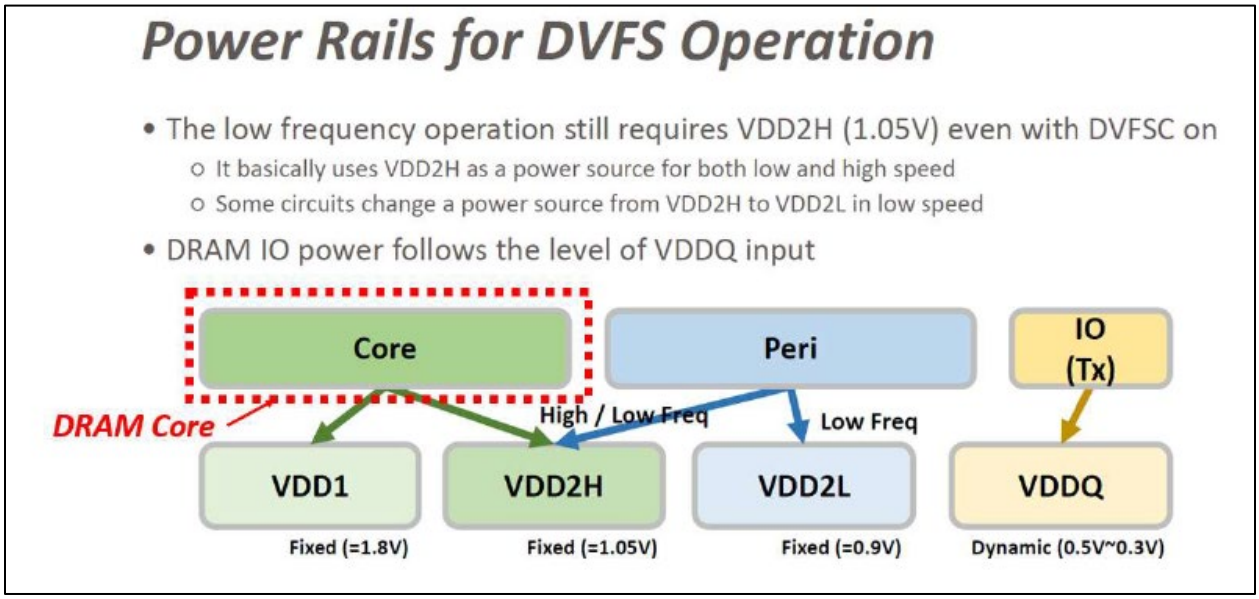
42. In DVFSC, the LPDDR5 DRAM operates circuitry from either the VDD2H or the VDD2L rail, voltage ranges for the two rails are shown below.

11.1 Recommended DC Operating Conditions

Table 396 — Recommended Voltage o

			Low Freq Voltage Spec Freq:DC to 2 MHz			
DRAM	Symbol		Min	Typ	Max	Unit
Core 1 Power	VDD1		1.7	1.8	1.95	V
Core 2 Power/Input Buffer Power	VDD2H		1.01	1.05	1.12	V
	VDD2L	Single Core Power Rail (MR13 OP[7]=1_B)	1.01	1.05	1.12	V
		Dual Core Power Rail (MR13 OP[7]=0_B)	0.87	0.9	0.97	
I/O Buffer Power	VDDQ	SPEC Range-1	0.47	0.5	0.57	V
		Spec Range-2	0.27	0.3	0.37	V
		Allowable Range	0.27	N/A	0.57	V

See JESD209-5B at Table 396 (annotated); *see also* JESD209-5C at Table 409.



See A. Chang, "JEDEC LPDDR5 Workshop – Commands & New Features," 2019 ("LPDDR5 Workshop") at 3 (annotated).

43. The Accused Products further comprise a peripheral circuit electrically connected to the DRAM core cell, wherein the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is lower than 1.1V. For example, the LPDDR5 DRAM includes buffers and other data path circuits (*i.e.*, peripheral circuits) connected to the DRAM core cell. When DVFSC mode is enabled, power is supplied via VDD2H or VDD2L, both of which are typically below1.1V. JEDED Standard – Lower Power Double Data Rate 5 (LPDDR5) Specification, JESD209-5B, June 2021 at 414; *see also* JESD209-5C at 430.

> "In DVFSC mode, when enabled by MR19 OP[1:0]=01B, the LPDRAM may operate internal circuitry from either the VDD2H rail or the VDD2L rail)."

See JESD209-5B at 414 (emphasis added); *see also* JESD209-5C at 430

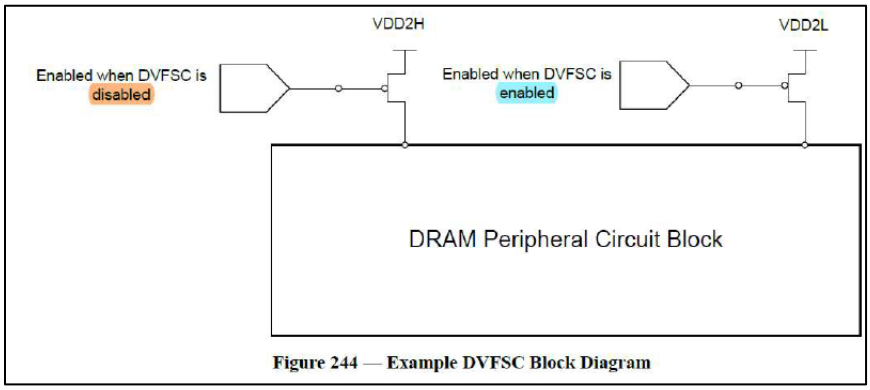
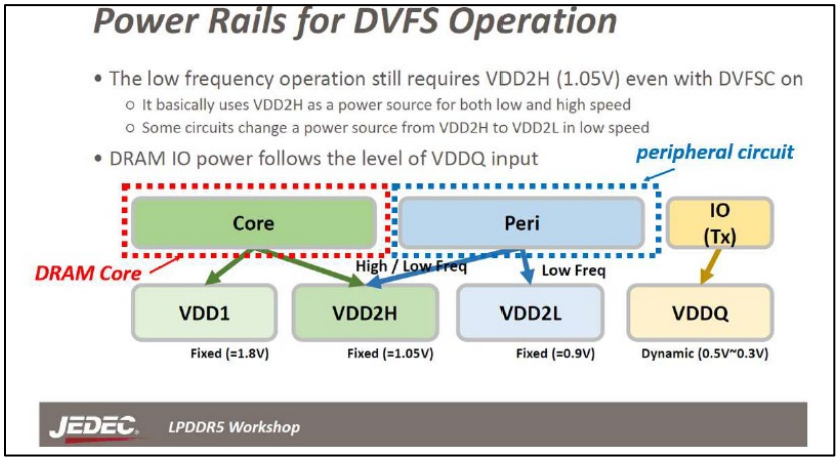


Figure 244 — Example DVFSC Block Diagram

See JESD209-5B at 416; *see also* JESD209-5C at 434.



See LPDDR5 Workshop at 3 (annotated)

44. The Accused Products further comprise wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell. For example, on information and belief, DRAM core cells and the corresponding peripheral circuits of the LPDDR5 DRAM within the A16 are typically formed on a single chip with the peripheral circuit being external to the DRAM core cells.

45. The Accused Products further comprise wherein the first voltage and the second voltage are capable of making the DRAM be applied to an embedded display port (eDP). On information and belief, the LPDDR5 DRAM of A16 may be applied to an embedded display port (eDP). On information and belief, the accused Apple devices utilize an eDP protocol at least to communicate with the USB-C displays.

46. Apple indirectly infringes one or more claims of the ’017 Patent by knowingly and intentionally inducing others, including Apple customers and end-users of the Accused Products and products that include the Accused Products, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States products that include infringing technology.

47. Apple indirectly infringes one or more claims of the ’017 Patent, as provided by 35 U.S.C. § 271(b), by inducing infringement by others, such as Apple’s customers and end-users, in this Judicial District and elsewhere in the United States. For example, Apple’s customers and end-users directly infringe, either literally or under the doctrine of equivalents, through their use of the inventions claimed in the ’017 Patent. Apple induces this direct infringement through its affirmative acts of manufacturing, selling, distributing, and/or otherwise making available the Accused Products, and providing instructions, documentation, and other information to customers

and end-users urging them to use the Accused Products in an infringing manner, including technical support, marketing, product manuals, advertisements, and online documentation. Because of Apple's inducement, Apple's customers and end-users use Accused Products and directly infringe the '017 Patent in a way Apple intends. Apple performs these affirmative acts with knowledge of the '017 Patent and with the intent, or willful blindness, that the induced acts directly infringe the '017 Patent.

48. Apple indirectly infringes one or more claims of the '017 Patent, as provided by 35 U.S.C. § 271(c), by contributing to direct infringement by others, such as customers and end-users, in this Judicial District and elsewhere in the United States. Apple's affirmative acts of selling and offering to sell the Accused Products in this Judicial District and elsewhere in the United States and causing the Accused Products to be manufactured, used, sold and offered for sale contributes to others' use and manufacture of the Accused Products, such that the '017 Patent is directly infringed by others. The accused components within the Accused Products are material to the invention of the '017 Patent, are not staple articles or commodities of commerce, have no substantial non-infringing uses, and are known by Apple to be especially made or adapted for use in the infringement of the '017 Patent. Apple performs these affirmative acts with knowledge of the '017 Patent and with intent, or willful blindness, that they cause the direct infringement of the '017 Patent.

49. WeCrevention has suffered damages as a result of Defendant's direct and indirect infringement of the '017 Patent in an amount to be proved at trial.

COUNT III
(Infringement of the '098 Patent)

50. Paragraphs 1 through 49 are incorporated by reference as if fully set forth herein

51. WeCrevention has not licensed or otherwise authorized Apple to make, use, offer for sale, sell, or import any products that embody the inventions of the ’098 Patent.

52. Apple has and continues to directly infringe the ’098 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States products that satisfy each and every limitation of one or more claims of the ’098 Patent.

53. For example, Apple directly infringes at least claim 1 of the ’098 Patent by making, using, offering to sell, selling, and/or importing into the United States products that comprise a dynamic random access memory (DRAM), comprising: a DRAM core cell comprised in the DRAM, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V; and a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell, and the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is lower than 1.1V, and wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell, and wherein the first voltage is different from the second voltage.

54. The Accused Products include a dynamic random access memory (DRAM) powered by external voltage source. For example, the iPhone 14 Pro includes rechargeable battery to supply voltage and 6 GB LPDDR5 DRAM, which is a dynamic random access memory. *See* https://www.macrumors.com/2022/09/16/iphoen-14-pro-faster-6gb-lpddr5-memory.

55. The Accused Products further include a DRAM core cell comprised in the DRAM, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V. *See* JESD209-5B at Table 6; *see also* JESD209-5C at 430-439. The LPDDR5 DRAM supports Dynamic Voltage and Frequency Scaling (DVFS), in particular, LPDDR5 DRAM supports DVFS Core (DVFSC), which changes the power supply voltage to the core. JESD209-5B at 414-416; JESD209-5C at 430-439.

> "LPDDR5 Dynamic Voltage and Frequency Scaling (DVFS) consists of two modes intended to reduce the LPDRAM energy consumption. The two modes are **DVFSC (DVFS Core)** and DVFSQ (DVFS VDDQ)."
>
> "In DVFSC mode, when enabled by MR19 OP[1:0]=01B, the LPDRAM may operate internal circuitry from either the **VDD2H rail or the VDD2L rail**."

See JESD209-5B at 414 (emphasis added); *see also* JESD209-5C at 430.

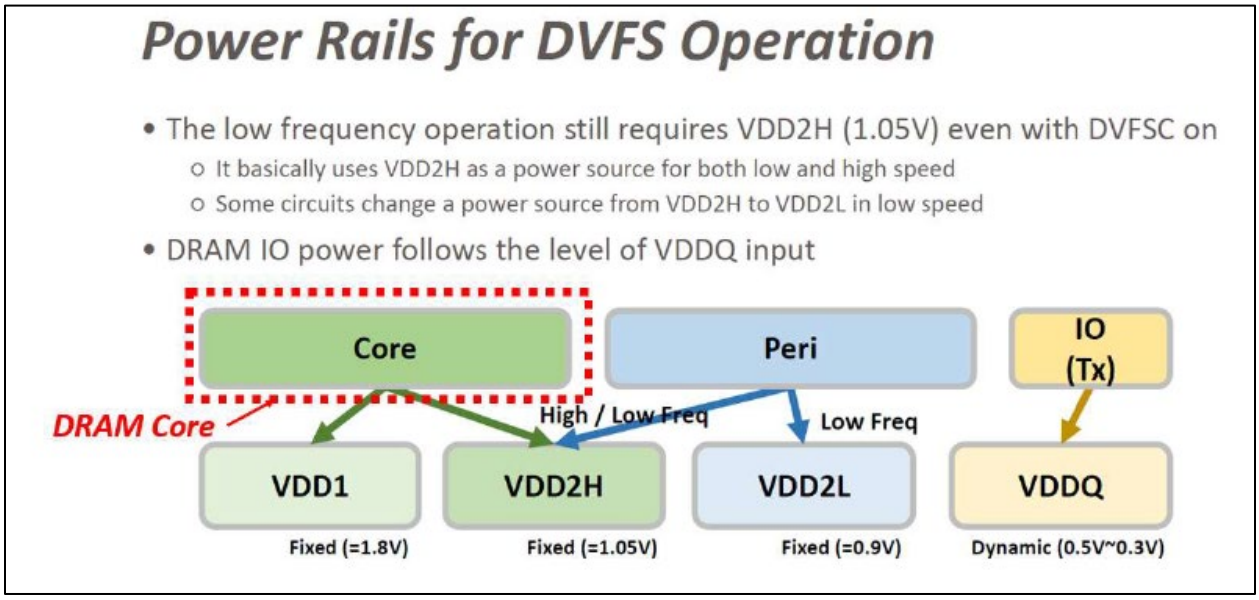
56. In DVFSC, the LPDDR5 DRAM operates circuitry from either the VDD2H or the VDD2L rail, voltage ranges for the two rails are shown below.

11.1 Recommended DC Operating Conditions

Table 396 — Recommended Voltage o

			Low Freq Voltage Spec Freq:DC to 2 MHz			
DRAM	Symbol		Min	Typ	Max	Unit
Core 1 Power	VDD1		1.7	1.8	1.95	V
Core 2 Power/Input Buffer Power	VDD2H		1.01	1.05	1.12	V
	VDD2L	Single Core Power Rail (MR13 OP[7]=1_B)	1.01	1.05	1.12	V
		Dual Core Power Rail (MR13 OP[7]=0_B)	0.87	0.9	0.97	
I/O Buffer Power	VDDQ	SPEC Range-1	0.47	0.5	0.57	V
		Spec Range-2	0.27	0.3	0.37	V
		Allowable Range	0.27	N/A	0.57	V

See JESD209-5B at Table 396 (annotated); *see also* JESD209-5C at Table 408. However, even when the LPDDR5 DRAM is operated in the low frequency/power mode, VDD2H still provides power to certain critical circuitry of the DRAM core.



See LPDDR5 Workshop at 3 (annotated).

57. The Accused Products further include a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell, and the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is lower than 1.1V. For example, the LPDDR5 DRAM of the A16 includes buffers and other data path circuits (*i.e.*, peripheral circuits) connected to the DRAM core cell. When the DVFSC mode is enabled, power is supplied to the peripheral circuits via VDD2H or VDD2L both of which are typically below 1.1V. *See* JESD209-5B at Table 396; *see also* JESD209-5C at Table 408.

58. The Accused Products further comprise wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell, and wherein the first voltage is different from the second voltage. On information and belief, DRAM core cell and peripheral circuit of the LPDDR5 DRAM within the A16 are formed on a single chip, and the peripheral circuit is external to the DRAM core cell, and wherein the first voltage is different from the second voltage. For example, when DVFSC mode is enabled and the LPDDR5 DRAM is operated in a low frequency/power mode, a first voltage VDD2H supplied to certain portions of the core is different from a second voltage VDD2L supplied to the peripheral circuit.

59. Apple indirectly infringes one or more claims of the ’098 Patent by knowingly and intentionally inducing others, including Apple customers and end-users of the Accused Products and products that include the Accused Products, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States products that include infringing technology.

60. Apple indirectly infringes one or more claims of the ’098 Patent, as provided by 35 U.S.C. § 271(b), by inducing infringement by others, such as Apple’s customers and end-users, in this Judicial District and elsewhere in the United States. For example, Apple’s customers and end-users directly infringe, either literally or under the doctrine of equivalents, through their use of the inventions claimed in the ’098 Patent. Apple induces this direct infringement through its affirmative acts of manufacturing, selling, distributing, and/or otherwise making available the Accused Products, and providing instructions, documentation, and other information to customers and end-users urging them to use the Accused Products in an infringing manner, including technical support, marketing, product manuals, advertisements, and online documentation. Because of Apple’s inducement, Apple’s customers and end-users use Accused Products and directly infringe the ‘098 Patent in a way Apple intends. Apple performs these affirmative acts with knowledge of the ’098 Patent and with the intent, or willful blindness, that the induced acts directly infringe the ’098 Patent.

61. Apple indirectly infringes one or more claims of the ’098 Patent, as provided by 35 U.S.C. § 271(c), by contributing to direct infringement by others, such as customers and end-users, in this Judicial District and elsewhere in the United States. Apple’s affirmative acts of selling and offering to sell the Accused Products in this Judicial District and elsewhere in the United States and causing the Accused Products to be manufactured, used, sold and offered for sale contributes to others’ use and manufacture of the Accused Products, such that the ’098 Patent is directly infringed by others. The accused components within the Accused Products are material to the invention of the ’098 Patent, are not staple articles or commodities of commerce, have no substantial non-infringing uses, and are known by Apple to be especially made or adapted for use in the infringement of the ’098 Patent. Apple performs these affirmative acts with knowledge of

the ’098 Patent and with intent, or willful blindness, that they cause the direct infringement of the ’098 Patent.

62. WeCrevention has suffered damages as a result of Defendant’s direct and indirect infringement of the ’098 Patent in an amount to be proved at trial.

COUNT IV
(Infringement of the ’652 Patent)

63. Paragraphs 1 through 62 are incorporated by reference as if fully set forth herein.

64. WeCrevention has not licensed or otherwise authorized Apple to make, use, offer for sale, sell, or import any products that embody the inventions of the ’652 Patent.

65. Apple has and continues to directly infringe the ’652 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States products that satisfy each and every limitation of one or more claims of the ’652 Patent.

66. For example, Apple directly infringes at least claim 1 of the ’652 Patent by making, using, offering to sell, selling, and/or importing into the United States products that comprise a dynamic random access memory (DRAM), comprising: a DRAM core cell comprised in the DRAM, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V; and an input/output circuit comprised in the DRAM, wherein the input/output circuit is electrically connected to the DRAM core cell, and the input/output circuit is supplied with a third voltage to make the input/output circuit operate at the third voltage, wherein the third voltage is lower than 1.1V, and wherein the DRAM core cell and the input/output circuit are formed on a single chip, the input/output circuit is external to the DRAM core cell, and the first voltage is different from the third voltage.

67. The Accused Products include a dynamic random access memory (DRAM) powered by external voltage source. For example, the iPhone 14 Pro includes rechargeable battery to supply voltage and 6 GB LPDDR5 DRAM, which is a dynamic random access memory. *See* https://www.macrumors.com/2022/09/16/iphoen-14-pro-faster-6gb-lpddr5-memory.

68. The Accused Products further include a DRAM core cell comprised in the DRAM, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V. *See* JESD209-5B at Table 6; *see also* JESD209-5C at 430-439. The LPDDR5 DRAM of the A16 includes multiple volatile DRAM memory core cells and supports DVFS. In particular, LPDDR5 DRAM supports DVFS Core (DVFSC), which permits the IMC to change the power supply voltage to the peripheral circuitry and certain portions of the core. JESD209-5B at 414-416; *see also* JESD209-5C at 430-439. Specifically, when DVFSC mode is enabled, power may be provided from either a high voltage rail VDD2H or a low voltage rail VDD2L, both of which are typically less than 1.1V

> "LPDDR5 Dynamic Voltage and Frequency Scaling (DVFS) consists of two modes intended to reduce the LPDRAM energy consumption. The two modes are **DVFSC (DVFS Core)** and DVFSQ (DVFS VDDQ)."
>
> "In DVFSC mode, when enabled by MR19 OP[1:0]=01B, the LPDRAM may operate internal circuitry from either the **VDD2H rail or the VDD2L rail**."

See JESD209-5B at 414 (emphasis added); *see also* JESD209-5C at 430

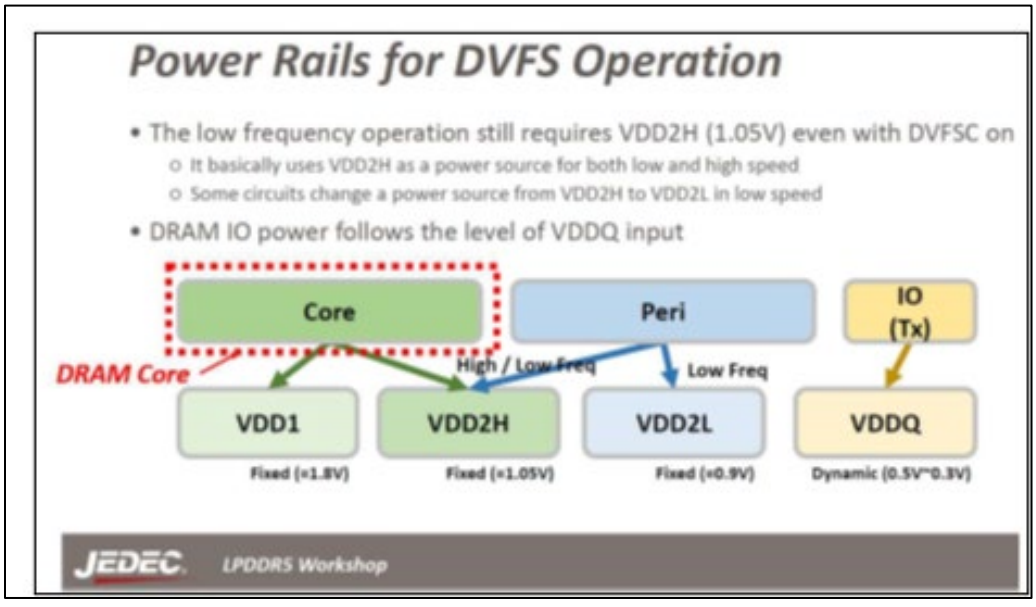
69. In DVFSC, the LPDDR5 DRAM operates circuitry from either the VDD2H or the VDD2L rail, voltage ranges for the two rails are shown below.

11.1 Recommended DC Operating Conditions

Table 396 — Recommended Voltage o

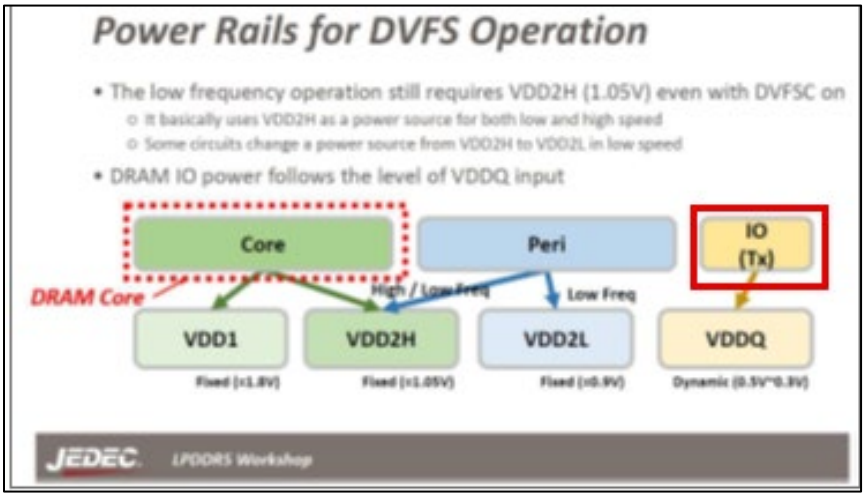
			Low Freq Voltage Spec Freq:DC to 2 MHz			
DRAM	Symbol		Min	Typ	Max	Unit
Core 1 Power	VDD1		1.7	1.8	1.95	V
Core 2 Power/Input Buffer Power	VDD2H		1.01	1.05	1.12	V
	VDD2L	Single Core Power Rail (MR13 OP[7]=1_B)	1.01	1.05	1.12	V
		Dual Core Power Rail (MR13 OP[7]=0_B)	0.87	0.9	0.97	
I/O Buffer Power	VDDQ	SPEC Range-1	0.47	0.5	0.57	V
		Spec Range-2	0.27	0.3	0.37	V
		Allowable Range	0.27	N/A	0.57	V

See JESD209-5B at Table 396 (Annotated); *see also* JESD209-5C at Table 408. However, even when the LPDDR5 DRAM is operated in the low frequency/power mode, VDD2H still provides power to certain critical circuitry of the DRAM core.

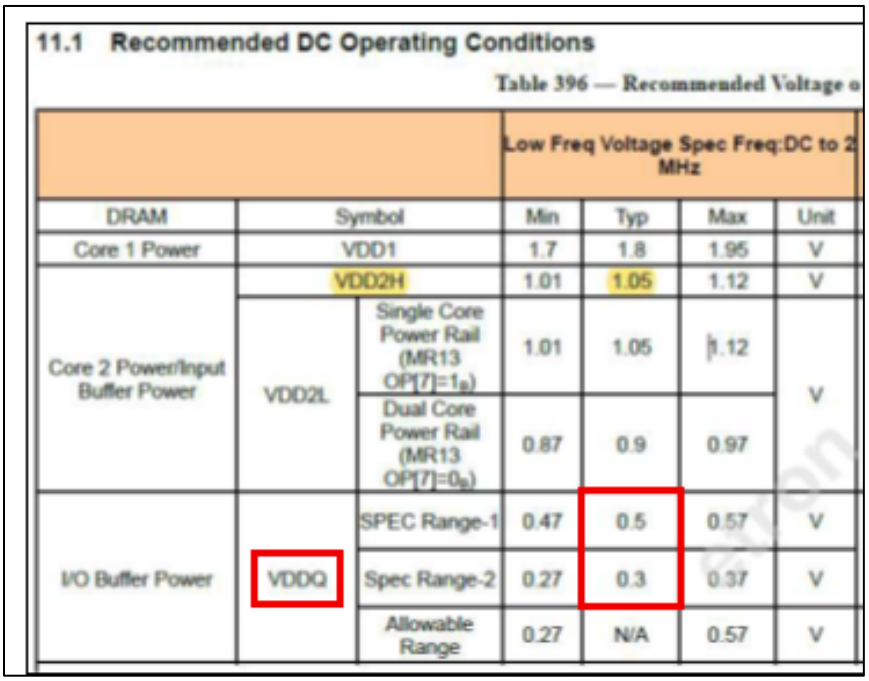


See LPDDR5 Workshop at 3. (Annotated)

70. The Accused Products further comprise an input/output circuit comprised in the LPDDR5 DRAM, wherein the input/output circuit is electrically connected to the DRAM core cell, and the input/output circuit is supplied with a third voltage to make the input/output circuit operate at the third voltage, wherein the third voltage is lower than 1.1V. For example, the LPDDR5 DRAM includes an I/O circuit (an "an input/output circuit") that is electrically connected to the DRAM core cell which operates a voltage lower than 1.1 V, (*i.e.*, VDDQ), as shown below.



See LPDDR5 Workshop at 3 (Annotated).



11.1 Recommended DC Operating Conditions

Table 396 — Recommended Voltage o

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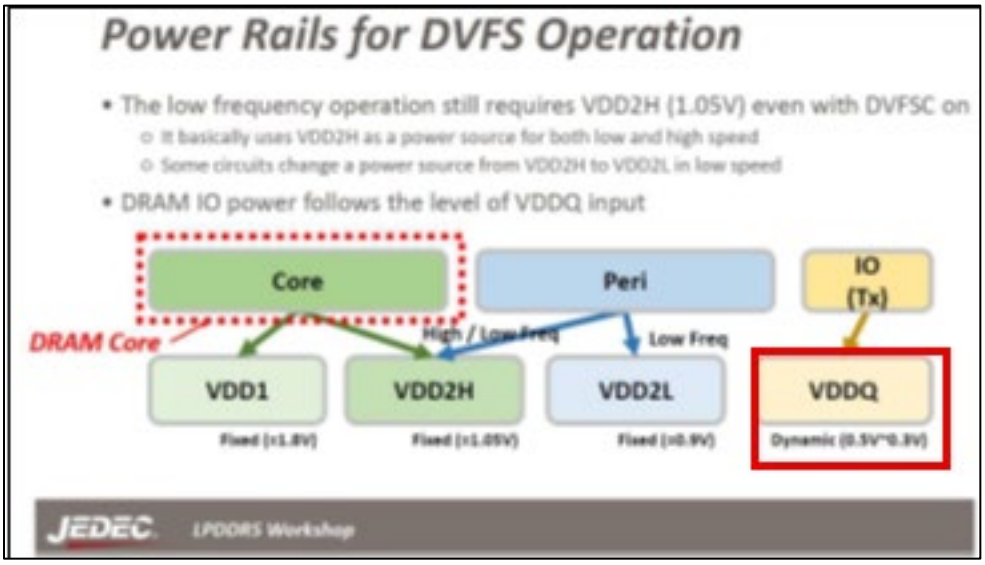
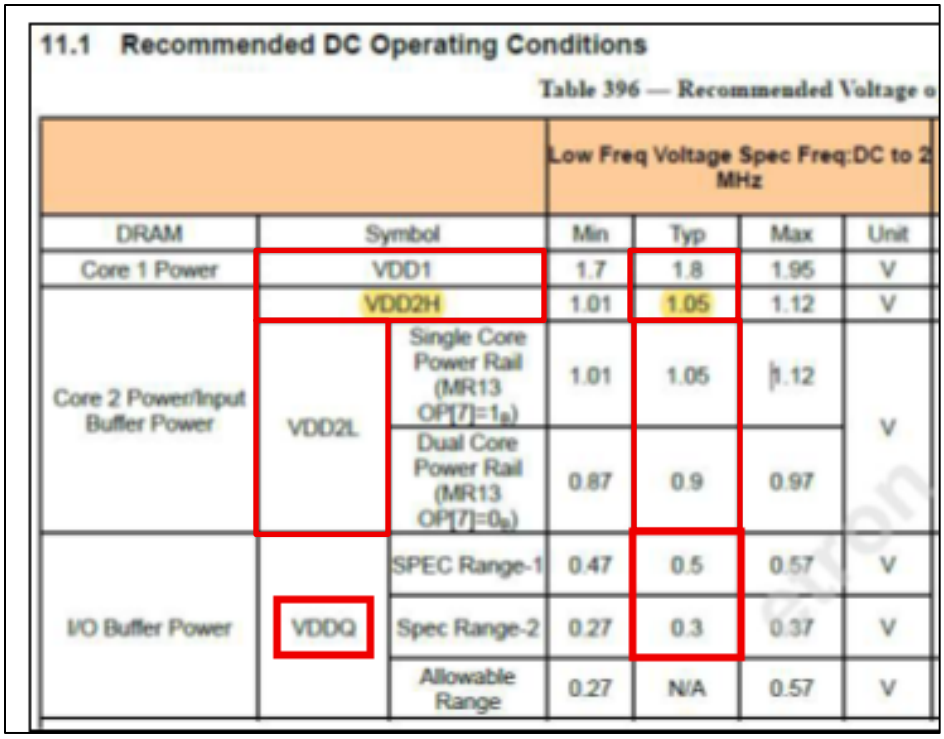
DRAM	Symbol		Min	Typ	Max	Unit
Core 1 Power	VDD1		1.7	1.8	1.95	V
Core 2 Power/Input Buffer Power	VDD2H		1.01	1.05	1.12	V
	VDD2L	Single Core Power Rail (MR13 OP[7]=1$_B$)	1.01	1.05	1.12	V
		Dual Core Power Rail (MR13 OP[7]=0$_B$)	0.87	0.9	0.97	
I/O Buffer Power	VDDQ	SPEC Range-1	0.47	0.5	0.57	V
		Spec Range-2	0.27	0.3	0.37	V
		Allowable Range	0.27	N/A	0.57	V

See JESD209-5B at Table 396 (annotated via red box); *see also* JESD209-5C at Table 408.



See LPDDR5 Workshop at 3 (annotated)

71. The Accused Products further comprise wherein the DRAM core cell and the input/output circuit are formed on a single chip, the input/output circuit is external to the DRAM core cell, and the first voltage is different from the third voltage. For example, on information and belief, DRAM core cells and I/O circuits of the LPDDR5 DRAM within the A16 are formed on a single chip with the I/O circuits being external to the DRAM core cell. The DRAM core cells are supplied with power from rails (*i.e.*, VDD1, VDD2H, VDD2L) that are separate and distinct from the I/O circuit (*i.e.*, VDDQ).



11.1 Recommended DC Operating Conditions

Table 396 — Recommended Voltage o

			Low Freq Voltage Spec Freq:DC to 2 MHz			
DRAM	Symbol		Min	Typ	Max	Unit
Core 1 Power	VDD1		1.7	1.8	1.95	V
Core 2 Power/Input Buffer Power	VDD2H		1.01	1.05	1.12	V
	VDD2L	Single Core Power Rail (MR13 OP[7]=1$_B$)	1.01	1.05	1.12	V
		Dual Core Power Rail (MR13 OP[7]=0$_B$)	0.87	0.9	0.97	
I/O Buffer Power	VDDQ	SPEC Range-1	0.47	0.5	0.57	V
		Spec Range-2	0.27	0.3	0.37	V
		Allowable Range	0.27	N/A	0.57	V

See JESD209-5B at Table 396 (annotated via red box); *see also* JESD209-5C at Table 408.

72. Further, the DRAM core cells operate at a first voltage lower than 1.1V (*e.g.*, VDD2H = 1.05V or VDD2L =0.9V) and the I/O circuit operates at a third voltage lower than 1.1V (*e.g.*, VDDQ at 0.3–0.5V). Thus, the first voltage is different from the third voltage. *See* JESD209-5B at 414-416; *see also* JESD209-5C at 430-439 and Table 408.

73. Apple indirectly infringes one or more claims of the ’652 Patent by knowingly and intentionally inducing others, including Apple customers and end-users of the Accused Products and products that include the Accused Products, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States products that include infringing technology.

74. Apple indirectly infringes one or more claims of the ’652 Patent, as provided by 35 U.S.C. § 271(b), by inducing infringement by others, such as Apple’s customers and end-users, in this District and elsewhere in the United States. For example, Apple’s customers and end-users

directly infringe, either literally or under the doctrine of equivalents, through their use of the inventions claimed in the '652 Patent. Apple induces this direct infringement through its affirmative acts of manufacturing, selling, distributing, and/or otherwise making available the Accused Products, and providing instructions, documentation, and other information to customers and end-users urging them to use the Accused Products in an infringing manner, including technical support, marketing, product manuals, advertisements, and online documentation. Because of Apple's inducement, Apple's customers and end-users use Accused Products in a way Apple intends and directly infringe the '652 Patent. Apple performs these affirmative acts with knowledge of the '652 Patent and with the intent, or willful blindness, that the induced acts directly infringe the '652 Patent.

75. Apple indirectly infringes one or more claims of the '652 Patent, as provided by 35 U.S.C. § 271(c), by contributing to direct infringement by others, such as customers and end-users, in this Judicial District and elsewhere in the United States. Apple's affirmative acts of selling and offering to sell the Accused Products in this Judicial District and elsewhere in the United States and causing the Accused Products to be manufactured, used, sold and offered for sale contributes to others' use and manufacture of the Accused Products, such that the '652 Patent is directly infringed by others. The accused components within the Accused Products are material to the invention of the '652 Patent, are not staple articles or commodities of commerce, have no substantial non-infringing uses, and are known by Apple to be especially made or adapted for use in the infringement of the '652 Patent. Apple performs these affirmative acts with knowledge of the '652 Patent and with intent, or willful blindness, that they cause the direct infringement of the '652 Patent.

76. WeCrevention has suffered damages as a result of Defendant's direct and indirect infringement of the '652 Patent in an amount to be proved at trial.

COUNT V
(Infringement of the '942 Patent)

77. Paragraphs 1 through 76 are incorporated by reference as if fully set forth herein

78. WeCrevention has not licensed or otherwise authorized Apple to make, use, offer for sale, sell, or import any products that embody the inventions of the '942 Patent.

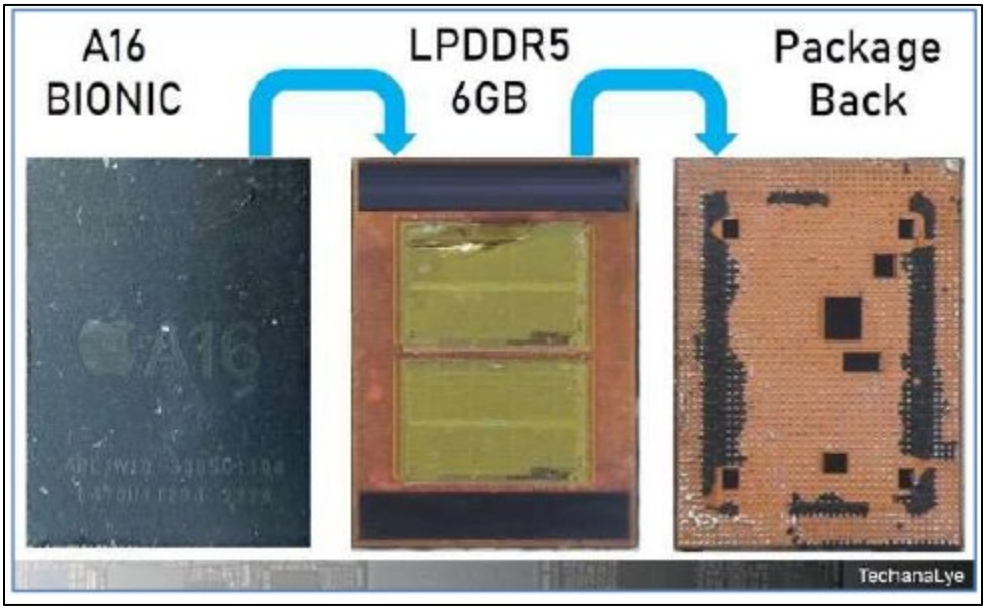
79. Apple has and continues to directly infringe the '942 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States products that satisfy each and every limitation of one or more claims of the '942 Patent.

80. For example, Apple directly infringes at least claim 19 of the '942 Patent by making, using, offering to sell, selling, and/or importing into the United States products that comprise an electronics system device with a high speed memory chip module, the device comprising: an ASIC processor; a type of memory cell array group, wherein the type of memory cell array group comprises multiple memory cell array ICs, each of the memory cell array ICs has an (I/O) data bus; and a logic unit for accessing the type of memory cell array group through a first transmission bus, wherein the first transmission bus is used for transmitting a first set of parallel data along with the memory cell array ICs, and bus width of the first transmission bus is wider than bus width of an (I/O) data bus of each of the memory cell array ICs, wherein the logic unit is further used for converting the first set of parallel data of the first transmission bus into a second set of parallel data through a second transmission bus, and transmits the second set of parallel data to the ASIC processor; wherein the ASIC processor executes a predetermined function

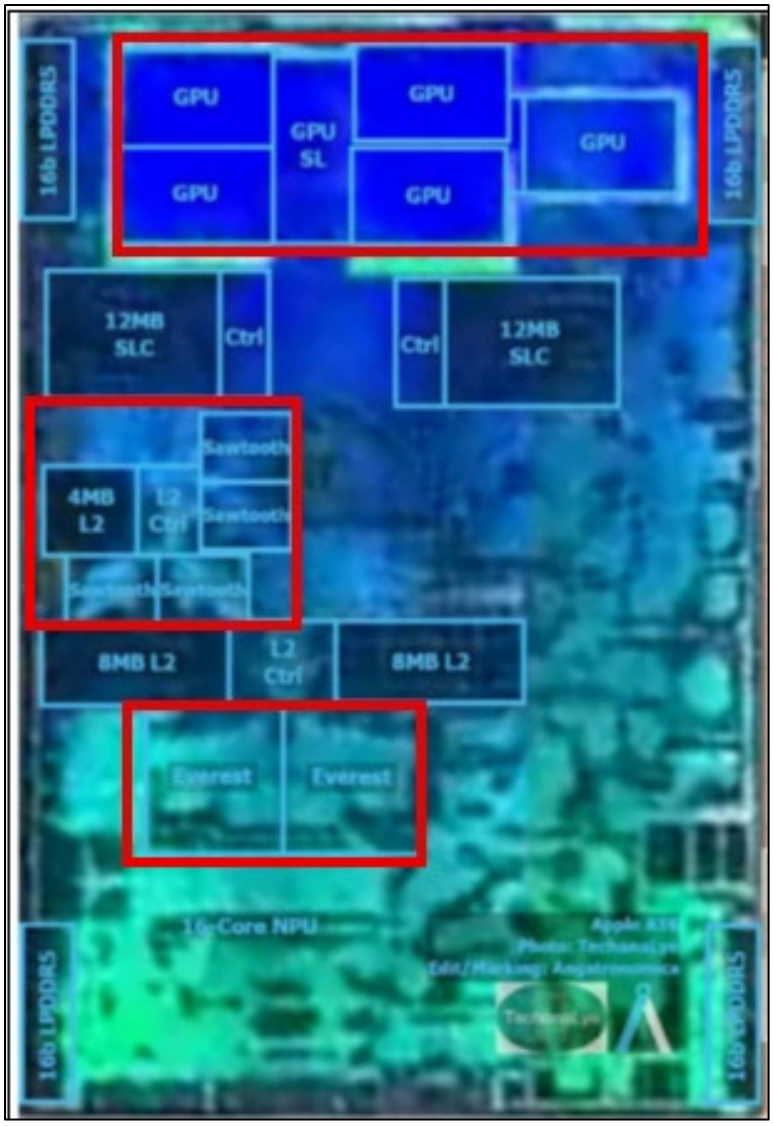
corresponding to the second set of parallel data while the ASIC processor is under operating condition, wherein bit width of the first set and the second set of parallel data are different.

81. The Accused Products comprise an electronics system device with a high speed memory chip module. For example, the iPhone 14 Pro is a smartphone (*i.e.*, an electronics system device), which has an A16 that includes a 6 GB LPDDR5 DRAM (*i.e.*, high speed memory chip module). *See* https://www.macworld.com/article/1073243/a16-processor-cpu-gpu-lpddr5-memory-performance.html.

82. The Accused Products further include an ASIC processor. For example, the iPhone 14's A16 includes an ASIC processor having at least two "Everest" high-performance cores, four "Sawtooth" energy-efficient cores, and five GPU cores, as shown below.

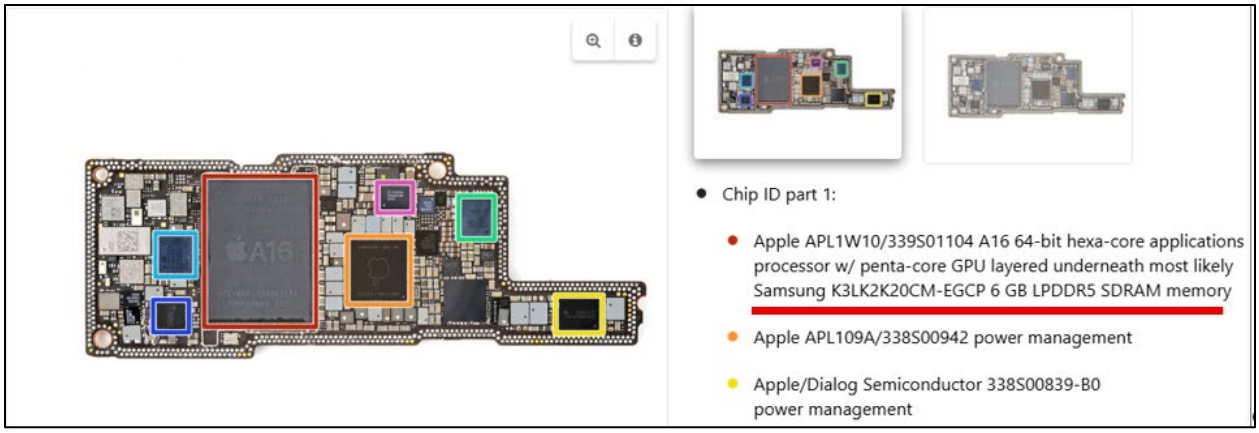


See https://eetimes.itmedia.co.jp/ee/articles/2210/25/news048.html.



See https://www.angstronomics.com/p/apple-a16-die-analysis.

83. On information and belief, the Accused Products further comprise a type of memory cell array group, wherein the type of memory cell array group comprises multiple memory cell array ICs, each of the memory cell array ICs has an (I/O) data bus. For example, on information and belief, the LPDDR5 DRAM of the iPhone 14 Pro A16 includes a 6 GB Samsung K3LK2K20CM LPRRD5 or similar memory having a memory cell array group with multiple memory cell array ICs, each of which has an (I/O) data bus. The memory cell array ICs and their (I/O) data busses are organized to produce a combined x64 width data bus.



See https://www.ifixit.com/Guide/iPhone+14+Pro+Max+Chip+ID/153224; *see also* https://semiconductor.samsung.com/dram/lpddr/lpddr5/k3lk2k20cm-jhcp/.

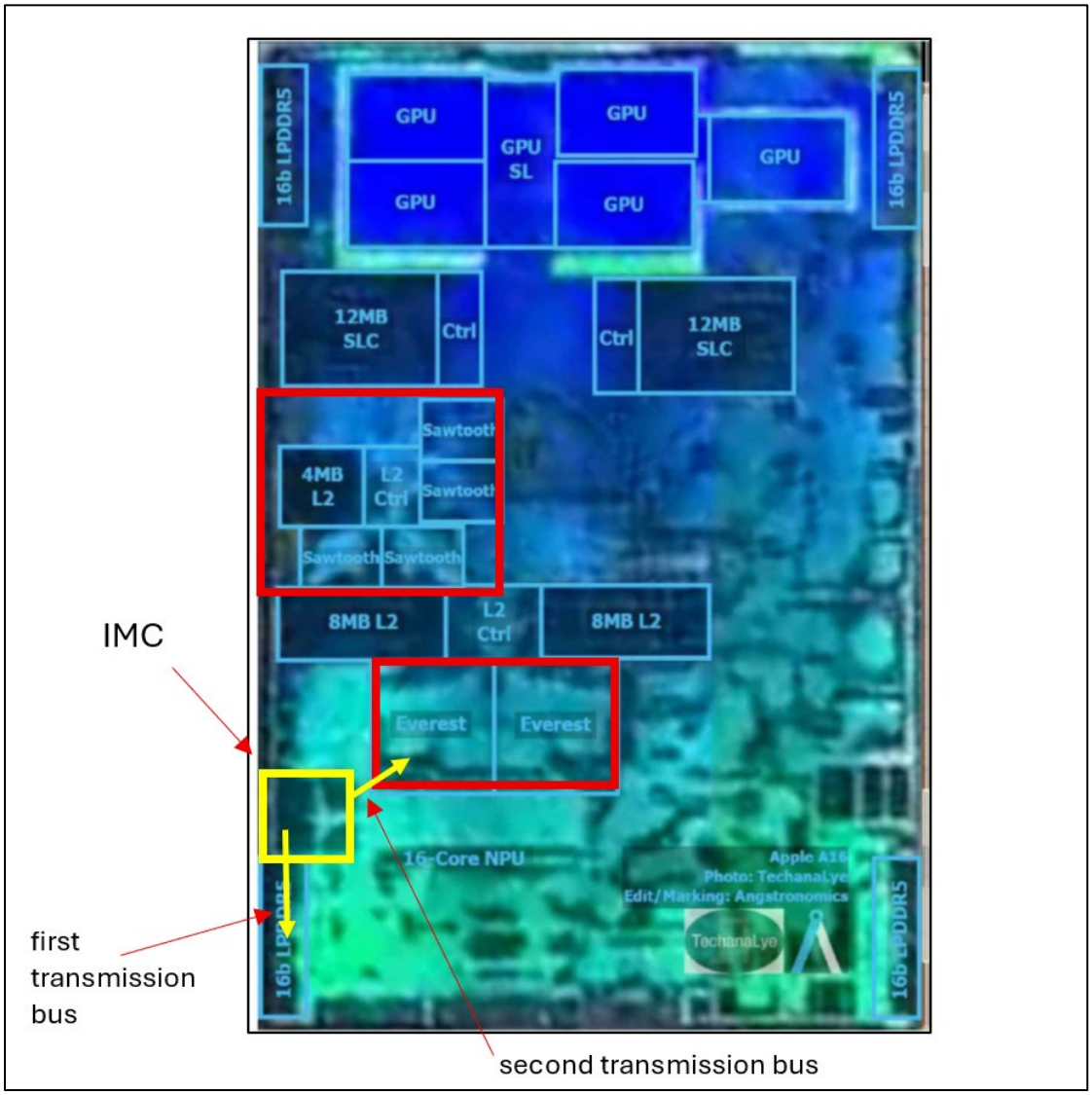
84. Further, JEDEC-compliant LPDDR5 devices expose per-die/per-channel I/O buses, which are typically x16 bit per channel. *See* https://www.synopsys.com/articles/key-features-about-lpddr5.html; *see also* https://www.systemverilog.io/design/lpddr5-tutorial-physical-structure/.

85. On information and belief, the Accused Products further comprise a logic unit for accessing the type of memory cell array group through a first transmission bus, wherein the first transmission bus is used for transmitting a first set of parallel data along with the memory cell array ICs, and bus width of the first transmission bus is wider than bus width of an (I/O) data bus of each of the memory cell array ICs, wherein the logic unit is further used for converting the first set of parallel data of the first transmission bus into a second set of parallel data through a second transmission bus, and transmits the second set of parallel data to the ASIC processor . For example, the A16 of the iPhone 14 Pro includes an integrated memory controller ("IMC") (*i.e.*, a "logic unit") for accessing the type of memory cell array group through a first transmission bus and for transmitting data to the ASIC processor through a second data bus.

> "The transistor count has gone up a few percent to 16 billion (from 15 billion), and it's likely that most of that higher budget is spent in the new display engine (which manages the iPhone 14 Pro's display down to 1Hz in always-on display mode and can crank it up to 2,000 nits in bright sunlight), **memory controller**, and image signal processor."

See https://www.macworld.com/article/1073243/a16-processorcpu-gpu-lpddr5-memory-performance.html (Emphasis Added).

86. On information and belief, the IMC is located between the processor cores of the ASIC and the LPDDR5, as shown below.

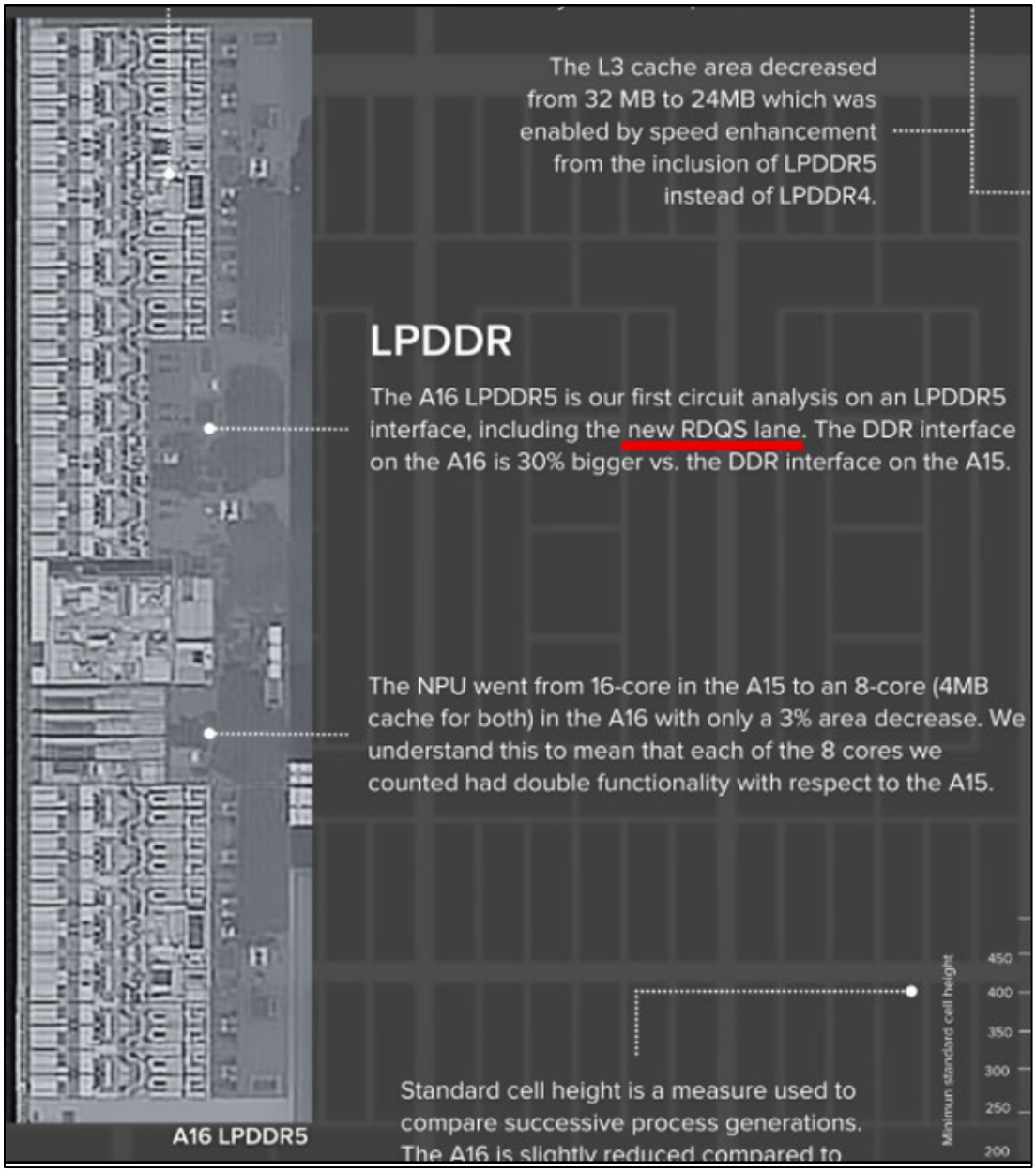


See https://www.angstronomics.com/p/apple-a16-die-analysis (annotated)

87. Furthermore, on information and belief, the bus width of the first transmission bus (*i.e.*, up to x64) is wider than the bus width of an (I/O) data bus of each of the memory cell array ICs (*i.e.*, x16). *See* https://www.ifixit.com/Guide/iPhone+14+Pro+Max+Chip+ID/153224; *see also* https://www.synopsys.com/articles/key-features-about-lpddr5.html.

88. Furthermore, on information and belief, the IMC converts the first set of parallel data of the first transmission bus into a second set of parallel data through the second transmission bus, for example, via an ARM AMBA interconnect (*e.g.*, AXI or its successors). *See* https://www.amd.com/en/products/adaptive-socs-and-fpgas/intellectual-property/axi_interconnect.html; *see also* https://anysilicon.com/understanding-amba-bus-architecture-protocols/

89. On information and belief, the Accused Products further comprise wherein the ASIC processor executes a predetermined function corresponding to the second set of parallel data while the ASIC processor is under operating condition, wherein bit width of the first set and the second set of parallel data are different. On information and belief, the ASIC of the A16 executes predetermined functions corresponding to second sets of parallel data. For example, the ASIC of the A16 performs predetermined functions during certain operating conditions (*e.g.*, camera ISP, GPU rendering, Neural Engine inference) using data fetched from the LPDDR5 DRAM. Further, on information and belief, the width of the first set of parallel data (*i.e.*, x64) and the second set of parallel data (*e.g.*, x128/256 on AXI) are different.



See http://blog.svc.techinsights.com/wp-content/uploads/2023/06/apple-a16-infographic.jpg.

90. Apple indirectly infringes one or more claims of the ’942 Patent by knowingly and intentionally inducing others, including Apple customers and end-users of the Accused Products and products that include the Accused Products, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States products that include infringing technology.

91. Apple indirectly infringes one or more claims of the ’942 Patent, as provided by 35 U.S.C. § 271(b), by inducing infringement by others, such as Apple’s customers and end-users, in this Judicial District and elsewhere in the United States. For example, Apple’s customers and end-users directly infringe, either literally or under the doctrine of equivalents, through their use of the inventions claimed in the ’942 Patent. Apple induces this direct infringement through its affirmative acts of manufacturing, selling, distributing, and/or otherwise making available the Accused Products, and providing instructions, documentation, and other information to customers and end-users urging them to use the Accused Products in an infringing manner, including technical support, marketing, product manuals, advertisements, and online documentation. Because of Apple’s inducement, Apple’s customers and end-users use Accused Products and directly infringe the ’942 Patent in a way Apple intends. Apple performs these affirmative acts with knowledge of the ’942 Patent and with the intent, or willful blindness, that the induced acts directly infringe the ’942 Patent.

92. Apple indirectly infringes one or more claims of the ’942 Patent, as provided by 35 U.S.C. § 271(c), by contributing to direct infringement by others, such as customers and end-users, in this Judicial District and elsewhere in the United States. Apple’s affirmative acts of selling and offering to sell the Accused Products in this Judicial District and elsewhere in the United States and causing the Accused Products to be manufactured, used, sold and offered for sale contributes to others’ use and manufacture of the Accused Products, such that the ’942 Patent is directly infringed by others. The accused components within the Accused Products are material to the invention of the ’942 Patent, are not staple articles or commodities of commerce, have no substantial non-infringing uses, and are known by Apple to be especially made or adapted for use in the infringement of the ’942 Patent. Apple performs these affirmative acts with knowledge of

the ’942 Patent and with intent, or willful blindness, that they cause the direct infringement of the ’942 Patent.

93. WeCrevention has suffered damages as a result of Defendant’s direct and indirect infringement of the ’942 Patent in an amount to be proved at trial.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury for all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, WeCrevention prays for relief against Apple as follows:

a. Entry of judgment declaring that Apple has directly and/or indirectly infringed one or more claims of the Patents-in-Suit;

b. Entry of judgment declaring that Apple’s infringement of the Patents-in-Suit is willful;

c. An order awarding damages sufficient to compensate WeCrevention for Defendant’s infringement of the Patents-in-Suit, but in no event less than a reasonable royalty, together with pre-judgment and post-judgment interest and costs;

d. Entry of judgment declaring that this case is exceptional and awarding WeCrevention its costs and reasonable attorneys’ fees under 35 U.S.C. § 285;

e. An accounting for acts of infringement;

f. Such other equitable relief which may be requested and to which the Plaintiff is entitled; and

g. Such other and further relief as the Court deems just and proper.

Dated: October 7, 2025

Respectfully submitted,

/s/Alfred R. Fabricant w/ permission
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