UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC., and
MICRON SEMICONDUCTOR PRODUCTS, INC.,
Petitioner

v.

PALISADE TECHNOLOGIES, LLP,
Patent Owner.

Case No. IPR2025-01560
U.S. Patent No. 8,996,838

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,996,838

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I. INTRODUCTION

Micron Technology, Inc. and Micron Semiconductor Products, Inc. (collectively, "Petitioner" or "Micron") request *inter partes* review ("IPR") of Claims 1-3, 8, 11-14, and 19-20 of U.S. Patent No. 8,996,838 ("the '838 Patent") (Ex-1001), currently assigned to Palisade Technologies, LLP ("PO").

II. MANDATORY NOTICES, STANDING, AND FEES

A. Mandatory Notices Under 37 C.F.R. § 42.8

Real Parties-in-Interest: Petitioner identifies the following real parties-in-interest: Micron Technology, Inc. and Micron Semiconductor Products, Inc.

Related Matters: PO has asserted the '838 Patent against the real parties-in-interest in *Palisade Technologies, LLP v. Micron Tech., Inc.*, No. 7:24-cv-00262 (W.D. Tex. Oct. 16, 2024).

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B. Grounds for Standing

Petitioner certifies that the '838 Patent is available for review, and Petitioner is not barred or estopped from requesting review.

C. Fee Authorization

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-0639.

III. PRECISE RELIEF REQUESTED

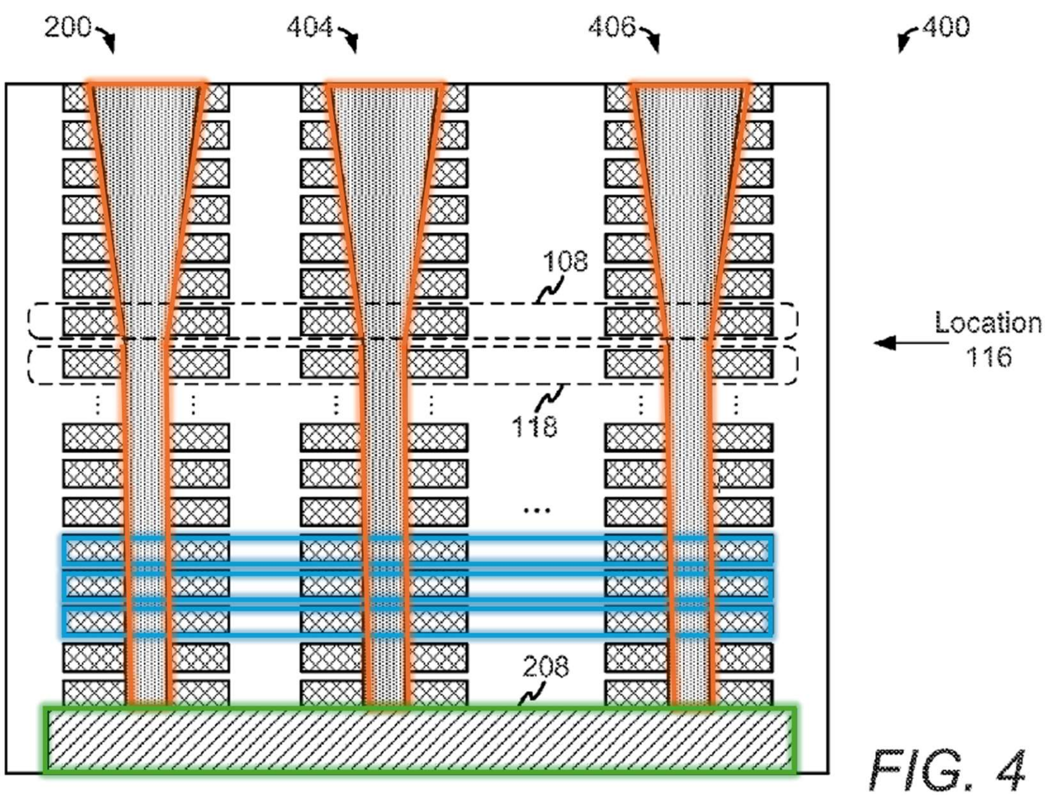
Petitioner requests cancellation of the challenged claims based on the following grounds:

Ground	Summary
1	Claims 1-2, 8, 11-13, and 19-20 are obvious over U.S. Patent Application Pub. No. 2012/0254680 ("Oh") (Ex-1005)
2	Claims 1-2, 8, 11-13, and 19-20 are obvious over Oh (Ex-1005) in view of U.S. Patent No. 8,730,738 ("Oh '738") (Ex-1015)
3	Claims 1-3, 8, 11-14, and 19-20 are obvious over U.S. Patent No. RE47,866 ("Tokiwa") (Ex-1006)
4	Claims 1-3, 8, 11-14, and 19-20 are obvious over Tokiwa (Ex-1006) in view of Oh '738 (Ex-1015)

IV. THE CHALLENGED PATENT

A. The ’838 Patent

The ’838 Patent generally relates to 3D memory structures, such as nonvolatile 3D NAND flash memory. Ex-1001, 3:33-37. Figure 4 (annotated below) illustrates that the 3D memory of the ’838 patent includes one or more physical “layers” (blue) disposed above a silicon substrate (green). *Id.*, 3:46-47. The memory layers may be monolithically formed above a silicon substrate. *Id.*, 27:26-33, Cls. 11 and 20. The 3D memory may further include one or more columns (orange) that extend through the memory layers, oriented in a direction perpendicular to that of the memory layers. *Id.*, 3:39:43.



Id., Fig. 4.

The columns are formed by an "etch process" that forms a cavity or "memory hole" through the memory layers. *Id*., 12:8-11. After the etch process, "the etched region may be filled with one or more materials to form" the columns. *Id*., 12:11-14. "Depending on the particular etch process and the number of layers formed on the substrate, the [column] may have a 'tapered' profile." *Id*., 1:63-65. For example, if the etching process begins from the top and reaches down to a substrate, more etching is performed at the top layers than the bottom, which can cause the resulting column to be wider at the top than the bottom. *Id*., 1:65-2:4, Cls. 2 and 13. The columns (orange) in Figure 4 (annotated) are wider at the top layers relative to the bottom, illustrating the tapering effect that the etching process described by the '838 Patent can produce. *Id*., 15:4-14.

The tapered profile of the columns "can affect device performance, such as performance characteristics of storage elements connected to the structure." *Id*., 2:7-9. For example, the '838 Patent explains that data reliability may be worse for data stored on layers for which the column is wider compared to layers for which the column is narrower. *Id*., 9:24-25. Additionally, layers with a wider column may have different voltage requirements for reading or writing data than layers with a narrower column. *Id*., 13:27-67 ("[B]iasing [a] control gate [with a wider column] may cause the conductive channel [] to conduct less current as compared to applying the voltage to [a] control gate [with a narrower column].").

The ’838 Patent describes compensating for the effects caused by a tapered column in a memory device “by selectively performing encoding operations, write operations, read operations, and/or decoding operations.” *Id*., 11:45-55. For example, data stored on layers with wider column can be encoded and decoded using longer “codewords” to compensate for the reduced data reliability of those layers. *Id*., 9:17-38. Additionally, different voltages can be used to read and write data to layers with a wider column compared to those with a narrower column. *Id*., 7:7-12, 10:21-27. The ’838 Patent discloses that a memory device can perform any subset or all of these methods to compensate for the tapered columns and improve device performance. *Id*., 11:45-55.

The alleged invention of the ’838 Patent relates to identifying, storing and accessing information that identifies “a location associated with a variation” of the tapered columns. *See, e.g.*, *id*. Cls. 1 and 12. The “location” identifies where the variation in the width of the columns begins through tapering. *Id*., 12:24-35, Cls. 1, 2, 12, and 13. For example, in Figure 2 (annotated below), location 116 (purple) identifies the location where column 202 (orange) begins to taper. *Id*. The column 202 (orange) “is not tapered below the location” (purple), but is tapered above the location. *Id.* The location is defined as being between layers 204 and 206, which corresponds to a distance above the substrate. *Id.*, 5:17-21, 12:24-35.

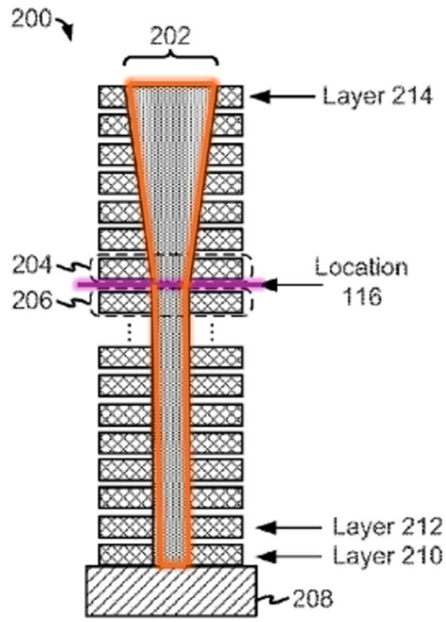


FIG. 2

Id., Fig. 2 (annotated).

The '838 Patent further discloses that the data storage device has a controller configured to determine the location, shown in Figure 1 below. *Id.*, 18:26-32.

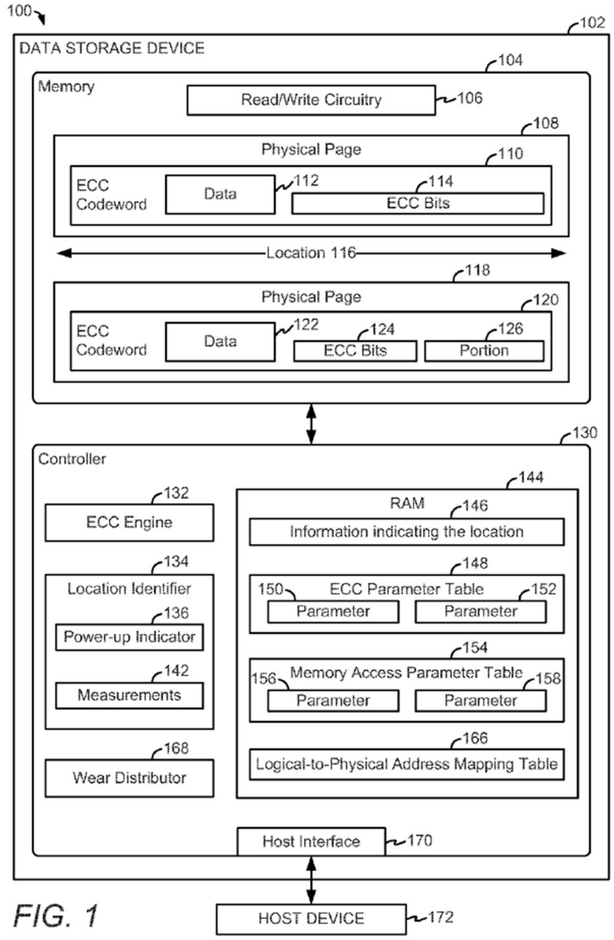


FIG. 1

Id., Fig. 1.

The controller includes a "location identifier 134" that determines the location by measuring a parameter for two adjacent layers, and comparing them to see if they are substantially the same. *Id*. 5:22-38, 18:60-19:19, Cls. 3 and 14. For example, referring to Figure 2 above, the controller can measure a first parameter for layer 210, and second parameter for layer 212. *Id*. The '838 Patent explains that a variety of parameters may be used by the location identifier, such as the number of programming pulses used by the read/write circuitry for each layer, a programming voltage of the programming pulses, a pulse duration or width of the programming pulses, or another parameter or combination of parameters. *Id*., 5:39-55, 19:7-14, Cls. 4 and 15. By comparing the parameters, the controller determines the location associated with the variation. *Id*., 5:56-68, 19:15-19. In one example, if the difference between the two parameters does not satisfy a threshold, the controller determines that the location associated with the variation is above layer 212, and keeps searching by comparing parameters between other layers. *Id*., 19:44-53, cls. 5 and 16. Once layers are identified for which the difference between the parameters satisfies the threshold, the controller determines that the location associated with the variation is between those two layers. *Id*., 19:20-28, Cls. 6 and 17. Once the location is determined, information identifying the location is generated and stored. *Id*., 19:58-62, Cls. 7 and 19.

The memory device can be configured to determine the location when the device is initially powered on. *Id*., 6:1-16, Cls. 9 and 18. After performing the operations, the value of a power-up indicator can be updated to indicate that the device has been previously powered up, indicating that the location determination has already occurred. *Id*. 6:16-20, Cl. 10.

The memory device's controller is operationally coupled to the memory. *Id*., 4:10-11. The controller can access the information identifying the location from the memory. *Id*., 7:66-8:10, Cl. 8. The '838 Patent discloses, but does not claim, using the location information to perform selective encoding, decoding, read, and write operations. *Id.*, 11:45-55. For example, the controller could use the location information to use a "short" error correction codeword for layers below the location, and an "extended" error correction codeword for layers above the location. *Id.*, 9:17-25. As another example, the controller could use the location information to apply different read and write voltages for layers above and below the location. *Id.*, 7:7-12, 10:21-27. By identifying and accounting for the location, the '838 Patent alleges that the "accuracy of operations at the data storage device [] can be improved." *Id.*, 12:36-37.

B. Prosecution History of the '838 Patent

The '838 file history is submitted as Ex-1004. The application was granted an expedited Track One review. The Examiner did not issue any rejections. *See generally* Ex-1004.

The prior art applied to the claims in this petition was not before the USPTO during prosecution of the '838 Patent. *See generally id*. Thus, this petition presents substantially new arguments that were not considered during prosecution.

C. Level of Ordinary Skill in the Art

A person of ordinary skill in the art at the relevant time ("POSITA") would have had a bachelor's degree in computer engineering, electrical engineering, computer science, or a closely related field, and at least two years of experience in the design, development, implementation, or management of memory devices and systems, or the equivalent, with additional education substituting for experience and vice versa. Ex-1002 ¶36.

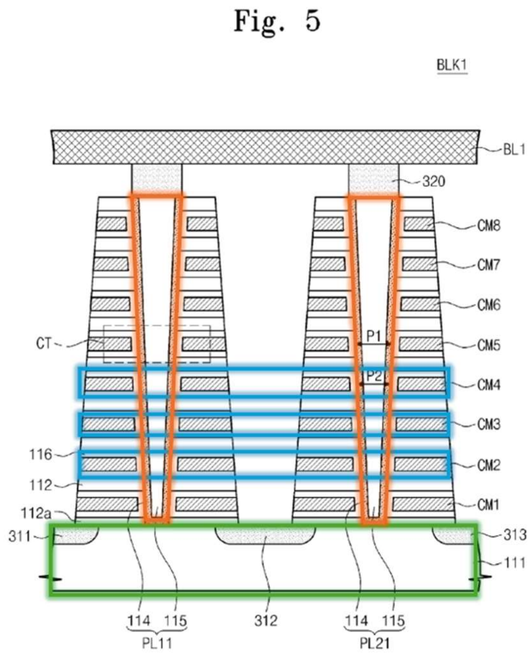
V. BRIEF DESCRIPTION OF THE APPLIED PRIOR ART REFERENCES

This petition presents three references, none of which were of record during prosecution. *See generally* Ex-1004.

A. Oh (Ex-1005)

Oh is a patent application that was filed Mar. 27, 2012, and published Oct. 4, 2012. Ex-1005. Oh qualifies as prior art under at least AIA § 102(a)(1)-(2). Ex-1002 ¶¶81-82.

Oh relates to nonvolatile memory devices, and specifically 3D memory devices "containing memory layers stacked on a substrate." Ex-1005 ¶¶2, 6. The 3D memory may include pillars that penetrate through the memory layers, and may have a tapered profile. *Id*. ¶¶9-10. Figure 5 (annotated below) illustrates that Oh's 3D memory includes a substrate (green), memory layers stacked on the substrate (blue), and pillars that penetrate the layers of memory (orange), and these pillars may have a taper effect. *Id*. ¶¶108, 121-122.



Id., Fig. 5 (annotated).

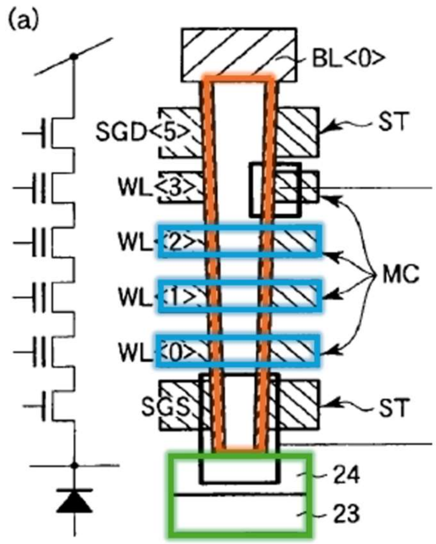
Oh discloses that reliability of data storage is affected by the variation of the shape of the column structures. *Id*. ¶¶153-154, 164. When the memory controller determines that memory cells in a particular area have low reliability, it considers that area a "bad area." *Id*. ¶65. "[M]emory cells included in the bad area are not be used." *Id*. When bad memory cells are detected, the entire memory layer containing those cells is considered a bad area, along with at least one additional layer closer to the substrate. *Id*. ¶155.

Information about the bad area is stored in either the address management register, or directly in the memory cell array. *Id*. ¶¶71, 78. When translating logical addresses into physical addresses, the address management circuit uses the information about the bad area to avoid mapping to physical addresses corresponding to bad areas. *Id*. ¶77.

B. Tokiwa (Ex-1006)

Tokiwa is a reissue patent that was filed on Feb. 4, 2016 and reissued on Feb. 18, 2020. Ex-1006. It is a reissue of U.S. Patent No. 8,228,773, which was filed as an application on Jun. 21, 2011 and issued on Jul. 24, 2012. *Id.* Tokiwa qualifies as prior art under at least AIA § 102(a)(1)-(2). Ex-1002 ¶¶86-87.

Tokiwa relates to "three-dimensionally stacked nonvolatile semiconductor memory." Ex-1006, 1:35-36. The three-dimensional memory includes a semiconductor substrate and "four or more conductive layers stacked on the semiconductor substrate… in such a manner as to be insulated from one another." *Id*., 2:22-27. The memory also includes at least one "semiconductor column which extends through the four or more conductive layers," which are referred to as "active areas." *Id*., 4:45-50. Figure 5(a) (annotated below) illustrates that Tokiwa's memory includes a substrate (green), memory layers stacked on the substrate (blue), and tapered pillars that penetrate the layers of memory (orange).



Id., Fig. 5 (annotated).

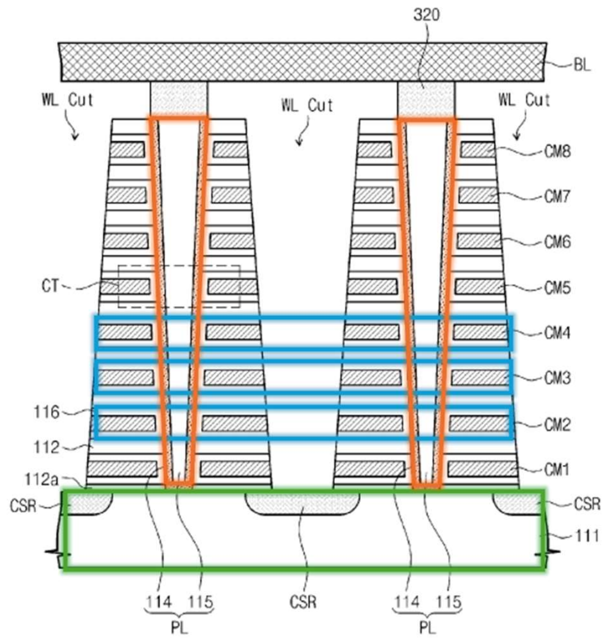
Tokiwa explains that the taper of the active layers causes variations in the speed of writing to memory cells on the different memory layers. *Id*., 9:47-57. To compensate for these variations, Tokiwa discloses retaining "information for generating supply potentials which are adjusted in intensity for the respective [layers] so that write potentials or nonselection potentials suitable for the plurality of [layers] may be supplied." *Id*., 10:4-18. In other words, Tokiwa's memory stores voltages appropriate to be applied to each layer, and uses those voltages when performing read or write operations to memory cells on those layers. *See, e.g., id*., 11:51-13:44.

C. Oh ’738 (Ex-1015)

Oh ’738 is a U.S. Patent originally issued on May 20, 2014. It issued from a patent application filed on Aug. 17, 2011. Oh ’738 qualifies as prior art under at least AIA § 102(a)(2). Ex-1002 ¶¶90-91.

Oh ’738 relates to a memory structure with memory cells “stacked in a direction perpendicular to the substrate to form a three-dimensional [memory] structure.” Ex-1015, 9:18-22. Oh’s 3D memory structure includes pillars extending through the memory layers. *Id.*, 11:44-12:10, Figs. 4-6. The “cross-sectional areas of pillars PL may vary according to a distance from a substrate.” *Id*. 15:31-32. Figure 6 (annotated below) illustrates that Oh ’738’s 3D memory includes a substrate (green), memory layers stacked on the substrate (blue), and tapered pillars that penetrate the layers of memory (orange).

Fig. 6

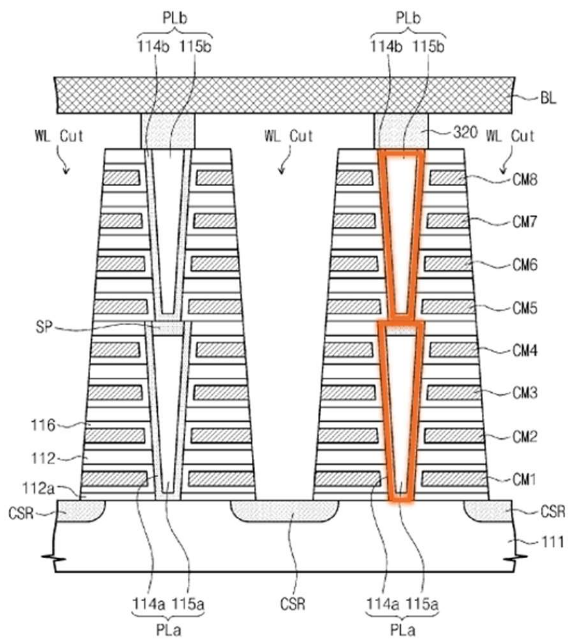


Id., Fig. 6 (annotated).

Oh '738 discloses that the variable cross-sectional areas of the pillars at each layer impacts the electrical properties of the layer associated with the pillar at that area. Ex-1015, 15:31-56, 17:5-13, 21:45-61. "When a cross-sectional area of a pillar decreases… [the] program speed of memory cells may increase." *Id*., 15: 53-56. To account for these electrical variations caused by the variations of the pillar, Oh '738 discloses using a time controller to "determine a voltage applying time according to widths of pillars PL." *Id*., 16:7-17.

Oh '738 also discloses that the 3D memory structure can include sub pillars "stacked in a direction perpendicular to a substrate." Ex-1015, 25:31-47. The sub pillars may be connected by semiconductor pads. *Id*., 25:60-67. The area where two sub pillars meet, joined by a semiconductor pad, "may constitute dummy word lines and dummy memory cells." *Id*., 26:1-11.

Fig. 30



Id., Fig. 30 (annotated).

VI. CLAIM CONSTRUCTION

To resolve the grounds presented herein, Petitioner does not believe that any term requires explicit construction because the prior art discloses the claim limitations in a manner consistent with the '838 Patent and under any construction. The Board "need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'" *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). Therefore, no construction is necessary to resolve whether the prior invalidates the challenged claims. Petitioner interprets the claim terms according to the *Phillips* claim construction standard. 37 C.F.R. § 42.100(b).[1]

VII. DETAILED EXPLANATION OF THE UNPATENTABILITY GROUNDS

The '838 Patent contains 20 claims. This Petition challenges Claims 1-3, 8, 11-14, and 19-20. The subject matter of the challenged claims is disclosed by the prior art as shown below.

A. Ground 1: Claims 1, 2, 8, 11, 12, 13, 19, and 20 Are Obvious Over Oh.

1. Claim 1

a. Element 1[pre]: A method comprising:

To the extent the preamble is limiting, Oh discloses the preamble. *See* Ex-1002 ¶98. Oh discloses "a method," because it states that its embodiments relate to "a bad area managing **method** of a nonvolatile memory device." Ex-1005 ¶2 (emphasis added).

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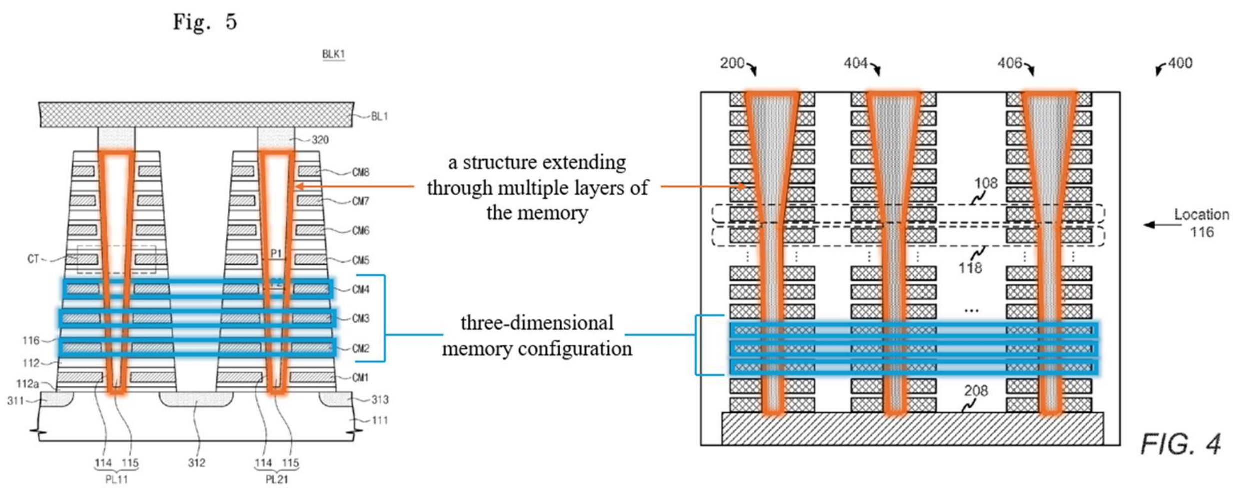
[1] The parties disputed a single term—"information identifying a location associated with a variation of the structure"—in the underlying district court case. The court has adopted "plain and ordinary meaning" as the proper construction, and Micron has applied that construction herein. *See* Ex-1016 (Claim Construction Order), 40-49.

b. Element 1[a]: in a data storage device that includes a memory having a three-dimensional (3D) memory configuration and including a structure extending through multiple layers of the memory, performing:

Element 1[a] requires a data storage device that includes 1) a memory having a three-dimensional (3D) memory configuration; and 2) a structure extending through multiple layers of the memory. As illustrated by a comparison of Oh's Figure 5 and the '838 Patent's Figure 4 (both annotated below), and explained in detail below, Oh discloses or teaches a data storage device with both of these requirements.



Oh, Figure 5 **'838 Patent, Figure 4**

Id., Fig. 5; Ex-1001, Fig. 4; *see also* Ex-1002 ¶¶99-103.

First, Oh discloses a "nonvolatile **memory device** including a plurality of memory blocks," which is the claimed "data storage device." Ex-1005 ¶6 (emphasis added); *see also* Ex-1005 ¶60 ("The nonvolatile memory device [] **stores data** in the memory cell array.") (emphasis added).

As illustrated above, Oh's data storage device includes "a memory having a three-dimensional (3D) memory configuration." For example, Oh discloses that "the memory cells are arranged on the substrate in row and column directions and stacked along a direction perpendicular to the substrate, **so that they form a three-dimensional structure**." *Id*. ¶88 (emphasis added); *see also id*. ¶6 (disclosing "a nonvolatile memory device including a plurality of memory blocks, each memory block containing **memory layers stacked on a substrate**") (emphasis added). This three-dimensional stacking of memory cells/layers is the claimed three-dimensional memory configuration.

Oh's data storage device also includes "a structure extending through multiple layers of the memory," as illustrated above. For example, Oh discloses that "[e]ach memory block may include **a semiconductor pillar** that penetrates the memory layers of the memory block." *Id*. ¶9 (emphasis added); *see also id*. ¶11 ("The sub-memory block may include a semiconductor pillar that penetrates the memory layers."). The semiconductor pillar is the claimed "structure" because it extends through multiple memory layers, as required by Claim 1.

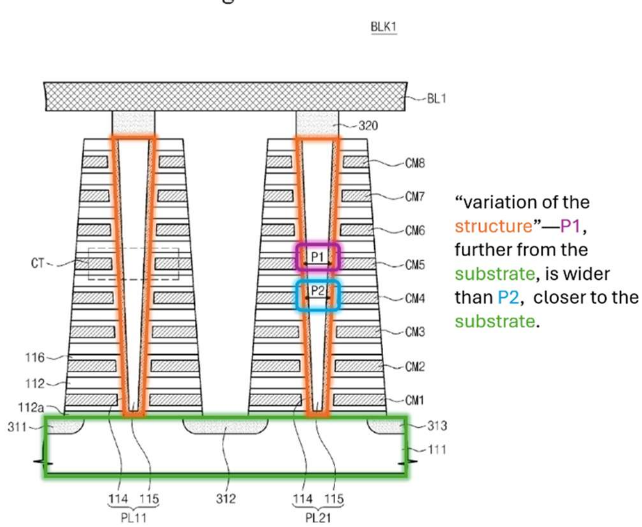
Thus, Oh discloses or teaches element 1[a].

c. Element 1[b]: storing information at the data storage device, the information identifying a location associated with a variation of the structure; and

Element 1[b] requires the structure having a variation, information identifying a location associated with that variation, and storing that information at the data storage device. Oh discloses or teaches these three requirements. *See* Ex-1002 ¶¶104-115.

First, Oh discloses that its semiconductor pillar (i.e., the claimed "structure") includes "a **first width that is wider than a second width** of the semiconductor pillar." Ex-1005 ¶10 (emphasis added); *see also id.* ¶164 ("Diameters of semiconductor pillars corresponding to memory layers are different from one another."). Figure 5 (annotated below) illustrates the claimed variation because the pillar (orange) is narrower closer to the substrate (green) and wider further from the substrate.

Fig. 5



Id., Fig. 5, ¶153. A POSITA would have understood that this width variation was the claimed "variation of the structure" because the variation is described the same way in the '838 Patent, which repeatedly characterizes the variation as tapering. Ex-

1002 ¶106; Ex-1001, 2:34, 5:12-13, 12:26-28, 13:28-38, 13:41-45 14:19-20; Ex-1005 ¶154. Thus, Oh discloses the claimed "variation of the structure."

Second, Oh discloses or teaches the claimed "information identifying a location associated with a variation of the structure." Oh's memory device identifies a "bad area." Ex-1005 ¶65. When a particular bad memory cell is detected, the "memory layer including the detected bad memory cell is treated as a bad area." *Id*., ¶155. Oh refers to information identifying the bad area as "bad area information." *Id*. ¶71. As explained below, Oh's "bad area information" is the claimed "information identifying a location associated with a variation of the structure."

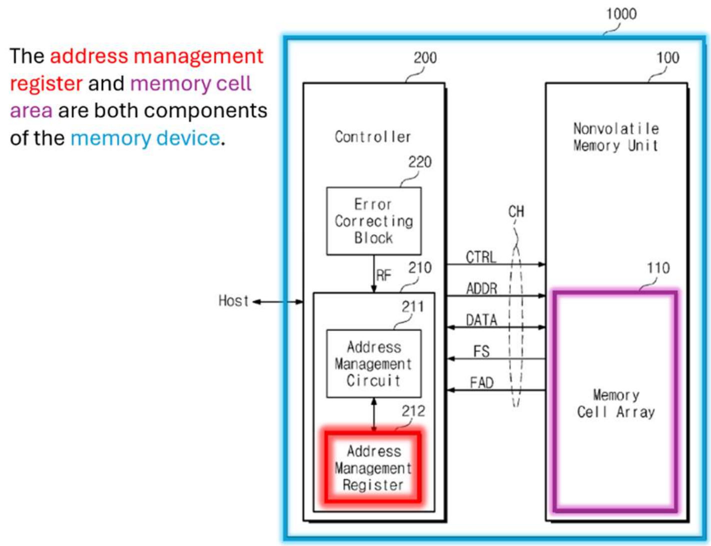
A POSITA would have understood Oh's bad area information to be "information identifying a location," because the bad area information identifies a location in the same way as the '838 Patent. Ex-1002 ¶109.

Consistent with the District Court's plain and ordinary meaning construction, the information identifying a location can be associated with any variation of the structure. Ex-1016, 40-49. Oh's bad area information identifies a location associated with a variation in the width of the structure. Oh discloses that a "bad area," is "an area of which the reliability is judged to be low." Ex-1005 ¶65. The reliability of a particular memory cell is determined by the variations in the width of the pillar at that layer. *Id*. ¶164 ("Diameters of semiconductor pillars corresponding to memory layers are different from one another. Accordingly, threshold voltages and

reliabilities of the first and second memory cells may differentiate." (emphasis added)); *see also id*. ¶¶153-154 ("[T]he **reliability** of data stored in a memory cell is lowered when its channel area decreases." (emphasis added)). Since the bad area information identifies a location with low reliability, and reliability is determined by variations in the width of the pillar structures, the bad area information "identif[ies] a location associated with a variation of the structure." Thus Oh's "bad area information" is the claimed "information identifying a location associated with a variation of the structure."

Third, Oh discloses "storing" the bad area information "at the data storage device." Oh stores the bad area information in "the address management register" or "the memory cell array" Ex-1005 ¶¶71, 78. Figure 1 (annotated below) shows that both the address management register and the nonvolatile memory portion are part of the memory device (i.e., the claimed "data storage device"). Thus, Oh discloses or teaches "storing [the] information at the data storage device."

Fig. 1



Id., Fig. 1; *see also id*. ¶60 ("Referring to FIG. **1**, a nonvolatile memory device **1000** includes a nonvolatile memory portion **100** [which includes memory cell array 110] and a controller **200** [which includes address management register 212].").

Accordingly, Oh teaches or discloses Element 1[b].

d. Element 1[c]: accessing the information.

Oh discloses accessing the bad area information. *See* Ex-1002 ¶¶114-115. For example, Oh discloses that "[t]he address management circuit [] **loads** bad area information… and manages the bad area information." Ex-1005 ¶79 (emphasis added). In this context, a POSITA would have understood that loading information is synonymous with accessing information. Ex-1002 ¶114. Moreover, Oh discloses that the address management circuit makes its address mapping decisions "based upon bad area information." Ex-1005 ¶77. A POSITA would have understood that using the stored bad area information in this way would have required accessing it. Ex-1002 ¶114. Accordingly, Oh discloses or teaches Element 1[c].

Thus, Oh renders Claim 1 obvious.

2. Claim 12

a. Element 12[pre]: A data storage device comprising:

Oh discloses or teaches Element 12[pre] for the same reasons as Element 1[a]. *Supra* § VII.A.1.b; *see also* Ex-1002 ¶116; Ex-1020.

b. Element 12[a]: a memory having a three-dimensional (3D) memory configuration and including a structure extending through multiple layers of the memory;

Oh discloses or teaches Element 12[a] for the same reasons as Element 1[a]. *Supra* § VII.A.1.b; *see also* Ex-1002 ¶117; Ex-1020.

c. Element 12[b]: a controller coupled to the memory, wherein the controller is configured to access information that is stored at the memory, the information identifying a location associated with a variation of the structure.

Oh discloses or teaches "the information identifying a location associated with a variation of the structure" for the same reasons as Element 1[b]. *Supra* § VII.A.1.c; *see also* Ex-1002 ¶118; Ex-1020.

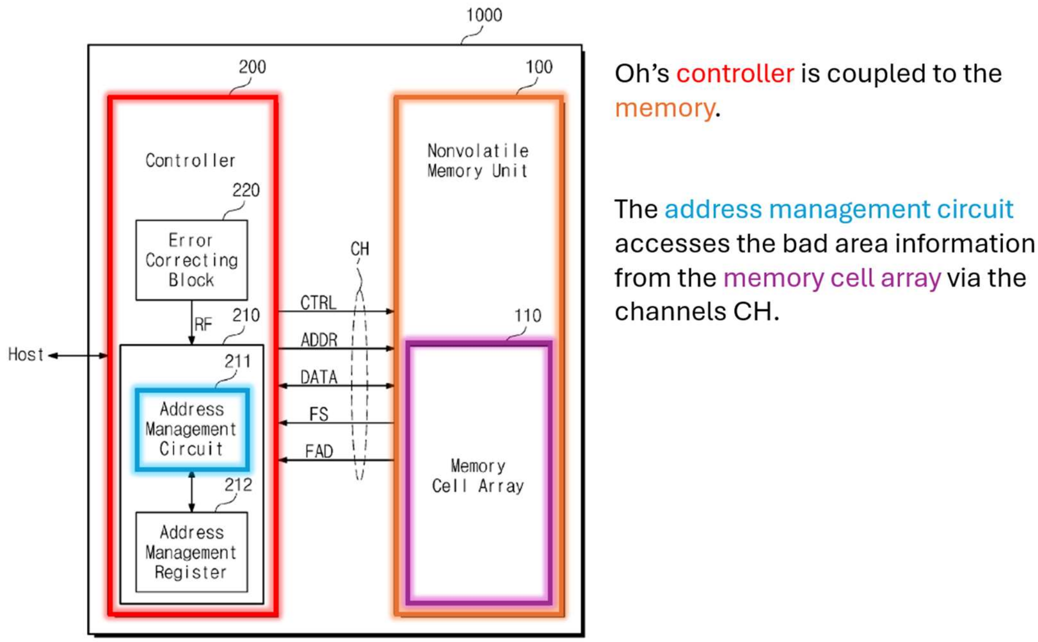
Oh also discloses or teaches the remainder of Element 12[b], which requires "a controller coupled to the memory" and that the "controller is configured to access information that is stored at the memory." *See* Ex-1002 ¶¶119-123. *First*, Oh discloses a controller that is coupled to the memory. For example, Oh discloses that "[t]he controller [] is coupled with a host and the nonvolatile memory portion." Ex-1005 ¶62.

Second, Oh discloses storing information at the memory, and a controller configured to access the information stored at the memory. As discussed with reference to Element 1[b], Oh discloses, as one option, storing the information at the memory cell array, which is part of the claimed "memory." *Supra* § VII.A.1.c; *see also* Ex-1005 ¶78 ("[T]he bad area information may be stored in the **memory cell array**." (emphasis added)), Fig. 1. The controller includes an address management circuit, which "**loads** bad area information stored in the memory cell array." *Id*., ¶¶65-66, 79 (emphasis added). As discussed in reference to Element 1[c], *supra* § VII.A.1.d, a POSITA would have understood that loading information is synonymous with accessing information in this context. Ex-1002 ¶114. Since Oh discloses accessing the information from memory, it is necessarily "configured to access the information that is stored at the memory."

Additionally, as discussed with reference to Element 1[b] the bad area information accessed by the controller is "the information identifying a location associated with a variation of the structure." *Supra* § VII.A.1.c. Therefore, the information stored at the memory and accessed by the controller is the claimed information.

Figure 1 (annotated below) illustrates how Oh's controller is both coupled to the memory and is configured to access information that is stored at the memory.

Fig. 1



Id., Fig. 1, ¶¶60-66, 79. Accordingly, Oh discloses or teaches the remainder of Element 12[b].

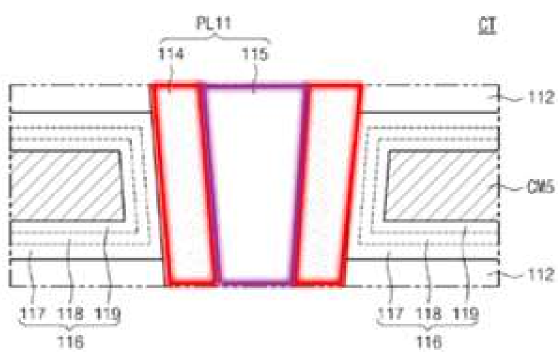
Thus, Oh renders Claim 12 obvious.

3. Claim 2: The method of claim 1, wherein the structure includes a conductive channel and a charge trap structure, and wherein the variation corresponds to a difference between a first width of the structure at a first distance from a substrate of the memory and a second width of the structure at a second distance from the substrate, the second distance greater than the first distance.

a. Oh discloses the conductive channel and a charge trap structure.

Oh discloses or teaches this element's requirement that the structure includes a charge trap structure and a conductive channel. *See* Ex-1002 ¶¶124-126. Figure 6 (annotated below) illustrates that Oh's pillar structures include a channel film including a conductive material (red) and an inner "information storage" structure made of an insulation material (purple). *Id*. ¶¶113-115, 121. As further described below, the channel film (red) is the claimed "conductive channel" and the inner information storage structure made of an insulation material (purple) is the claimed "charge trap structure."

Fig. 6



Id., Fig. 6 (annotated).

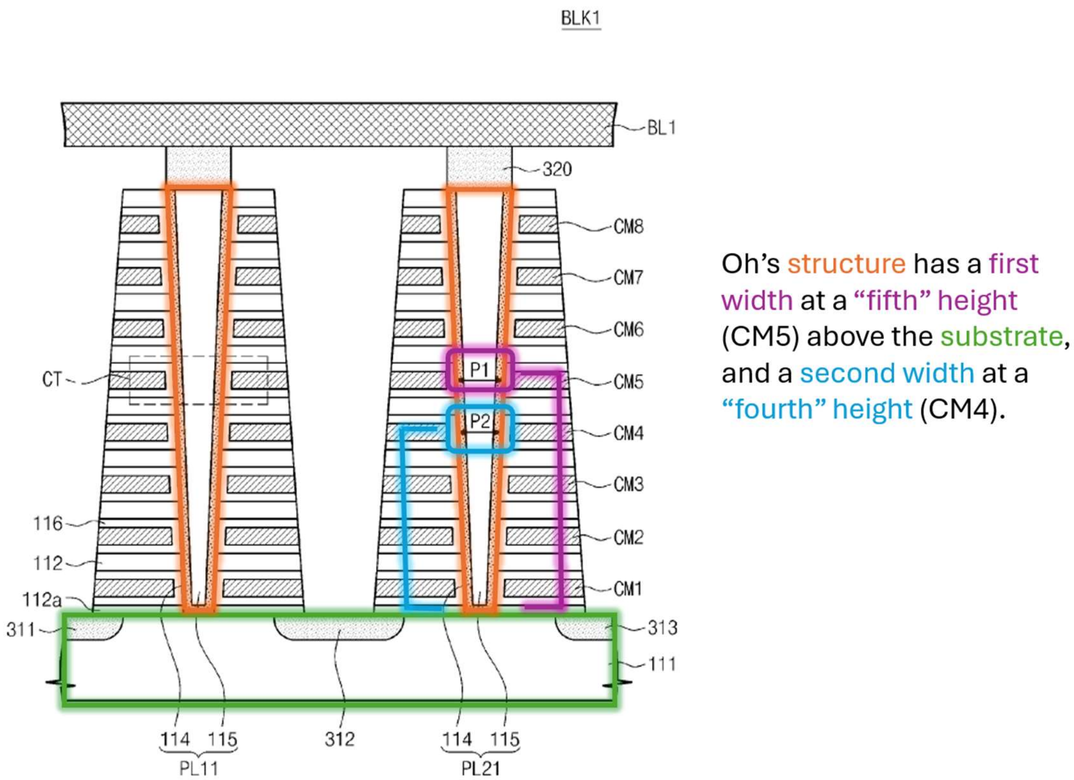
As illustrated above, Oh discloses that the semiconductor pillars are made of two parts, "a channel film [] and an inner material." Ex-1005 ¶113. "The channel films [] include a semiconductor material . . . having a first conductive type," so the channel film is a conductive channel. *Id*. ¶114. The inner material is made of "insulation material such as a dielectric material," which act as "information storage films." *Id*. ¶¶115, 121. A POSITA would have understood that the insulation material to store information in a 3D memory device is the same as a charge trap structure. Ex-1002 ¶125 (citing Ex-1012, explaining that an inner insulating material is used as a charge trap structure in the pillar of a 3D memory). Moreover, this is consistent with how the ’838 Patent describes the charge trap structure. *See* Ex-1001, 13:2-3 (“The charge trap structure may include an insulating material.”).

Accordingly, Oh discloses or teaches that the structure includes a conductive channel and a charge trap structure.

b. Oh discloses that the variation corresponds to a difference between the widths of the structure at two distances from the substrate.

Oh also discloses this element’s requirement that the variation corresponds to a difference between the widths of the structure at different heights above the substrate. *See* Ex-1002 ¶¶127-128. Oh discloses that “[t]he semiconductor pillar may include a **first width that is wider than a second width** of the semiconductor pillar.” Ex-1005 ¶10 (emphasis added). In the example described with reference to Figure 5, the “first width” (P1) corresponds to a “fifth height” above the substrate, and the “second width” (P2) corresponds to a “fourth height.” *Id*. ¶153. In other words, Oh’s semiconductor pillar is “tapered”—the width varies at different heights above the substrate, as required by Element 2[b]. Figure 5 (annotated below) illustrates how oh discloses or teaches Element 2[b].

Fig. 5



Id., Fig. 5.

Thus, Oh renders Claim 2 obvious.

4. Claim 8: The method of claim 1, wherein the data storage device further includes a controller that is operationally coupled to the memory, wherein the information is stored at the memory, and wherein the controller accesses the information from the memory.

Oh discloses or teaches Claim 8 for the same reasons described with reference to Element 12[b]. *Supra* § VII.A.2.c; *see also* Ex-1002 ¶¶129-130; Ex-1020. The only difference between Element 12[b] and Claim 8 is that Element 12[b] requires a controller "configured to access information," while Claim 8 requires that the controller "accesses the information." *See* Ex-1020. As described with reference to

Element 12[b], Oh discloses a controller that is configured to access and actually does access the information from the memory. *Supra*, § VII.A.2.c.

Thus, Oh renders Claim 8 obvious.

5. Claim 11: The method of claim 1, wherein the memory is a non-volatile memory that is monolithically formed in one or more physical levels of arrays of memory cells having an active area disposed above a silicon substrate, and wherein the data storage device further includes circuitry associated with operation of the memory cells.

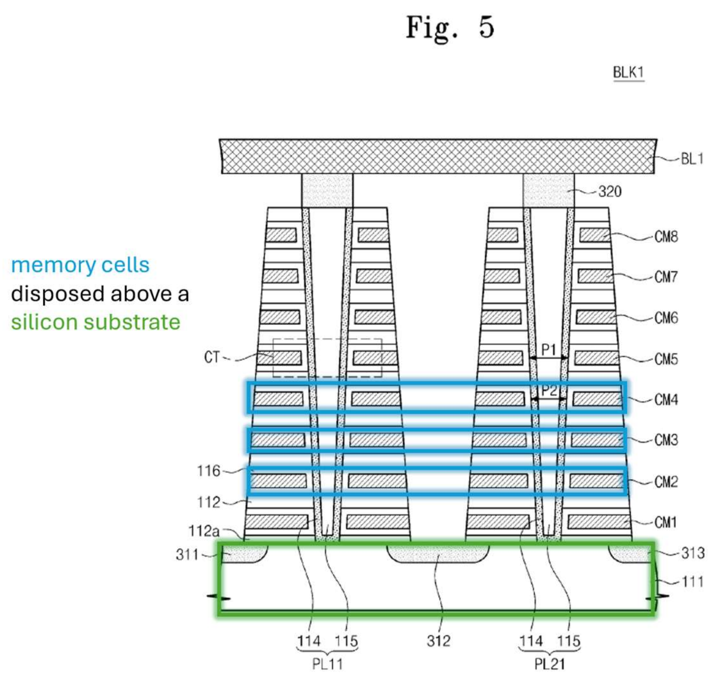
a. Oh discloses the required memory structure and formation.

The first portion of Claim 11 requires: 1) "the memory is a non-volatile memory"; 2) the memory "is monolithically formed in one or more physical levels of arrays of memory cells"; and 3) the memory has "an active area disposed above a silicon substrate." Oh discloses or teaches each of these requirements. *See* Ex-1002 ¶¶131-134.

First, Oh discloses a nonvolatile memory. For example, Oh discloses "a **nonvolatile memory device** including a plurality of memory blocks." Ex-1005 ¶6 (emphasis added); *see also id*. ¶¶15, 60.

Second, Oh discloses or teaches that the memory is monolithically formed in one or more physical levels of arrays or memory cells. According to the '838 Patent, a "monolithic" three dimensional memory array is one where "one or more memory device levels are formed above a single substrate." Ex-1001, 35:24-26. Oh discloses a single substrate with multiple layers stacked on the substrate. *Id*. ¶¶6, 15, 18, 88, 122, 124, 172. A POSITA would have understood this to mean that Oh's memory device is monolithically formed. Ex-1002 ¶133 (citing Ex-1014, explaining that a monolithic memory device is one with "successive layers of transistors and interconnect on one substrate"). Moreover, Oh discloses that "[t]he plurality of memory layers may be **stacked**" and that "[e]ach memory layer includes a plurality of **memory cells**." Ex-1005 ¶¶88 (emphases added); *see also id*. ¶6 (disclosing "a nonvolatile memory device including a plurality of memory blocks, each memory block containing memory layers **stacked** on a substrate") (emphasis added).

Third, Oh discloses or teaches "an active area disposed above a silicon substrate." As shown by Figure 5 (annotated below), Oh discloses a nonvolatile memory device "containing memory layers stacked on a substrate." Ex-1005 ¶¶2, 6, Fig. 5; *see also* Ex-1005 ¶¶15, 18, 88, 122, 124, 172.

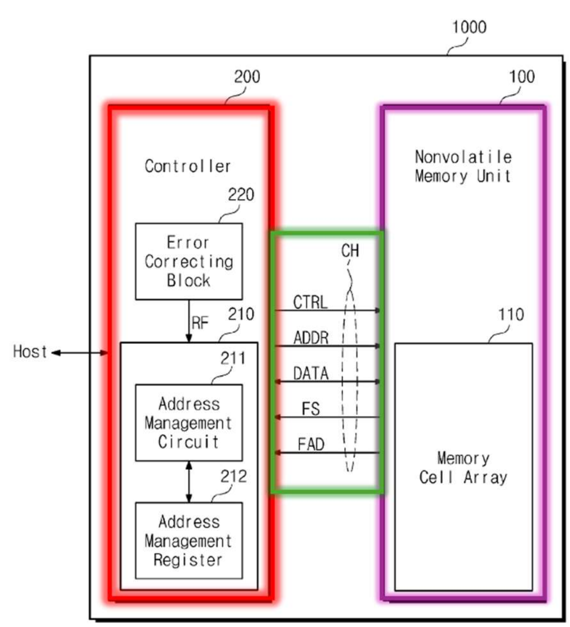


Id., Fig. 5, ¶¶108, 121-122. Additionally, each memory layer includes conductive material. *Id*. ¶117, Fig. 4. A POSITA would have understood that this means the memory layers are an "active area" Ex-1002 ¶134 (citing Ex-1014, explaining that the layers formed above the substrate are commonly called "active layers."). Moreover, Oh discloses that its substrate is made of silicon. Ex-1005 ¶128 ("[T]he channel films . . . may include the same p-type **silicon** as the substrate.") (emphasis added). Therefore, Oh discloses or teaches the memory formation and structural requirements of Claim 11.

b. Oh discloses the required circuitry associated with the operation of the memory cells.

Oh discloses or teaches that the data storage device further includes circuitry associated with operation of the memory cells. Ex-1002 ¶¶135-136. The '838 Patent explains that "circuitry" refers to the connections between memory elements that allow them accomplish functions such as reading and programming. Ex-1001, 35:51-60. Oh discloses memory elements, such as a controller and nonvolatile memory, that are coupled to each other and configured to communicate via "channels." Ex-1005 ¶62. The signals sent on these channels perform the functions prompt the nonvolatile memory to perform read, program or erase operations. *Id.* ¶65. Thus Oh's "channels" are the circuitry required by Claim 11. Figure 1 (annotated below) illustrates the channels (green) of the Oh memory device, that enables the controller (red) to communicate with the nonvolatile memory unit (purple).

Fig. 1



Id., Fig. 1. Accordingly, Oh discloses or teaches that "the data storage device further includes circuitry associated with operation of the memory cells."

Thus, Oh renders Claim 11 obvious.

6. Claim 13: The data storage device of claim 12, wherein the structure includes a conductive channel and a charge trap structure, and wherein the variation is a difference between a first width of the structure at a first distance from a substrate of the memory and a second width of the structure at a second distance from the substrate, the second distance greater than the first distance.

Oh renders Claim 13 obvious for the same reasons as Claim 2. *Supra* § VII.A.3; *see also* Ex-1002 ¶137; Ex-1020.

7. Claim 19: The data storage device of claim 12, wherein the controller is further configured to generate the information in response to determining the location and to store the information at the memory.

Claim 19 requires the controller to be configured: 1) to generate the information in response to determining the location; and 2) to store the information at the memory. Oh's controller meets both of these requirements. *See* Ex-1002 ¶¶138-141.

First, Oh discloses or teaches that the controller is configured to generate the information in response to determining the location. For example, Oh discloses that if a certain number of erroneous bits exists at read, the error correcting block generates a read fail signal. Ex-1005 ¶74 ("If the number of erroneous bits exceeds the limited number, the error correcting block [] generates a read fail signal."). In response to this signal, the address management circuit part of the controller "detects that the selected page includes bad memory cells." *Id*. ¶75. Then, "the control logic [] **generates** a fail address FAD indicating an address" of the failed area. *Id*. ¶102 (emphasis added). Thus, Oh's controller generates the information in response to determining the location.

Second, Oh teaches that the controller is configured to store the information at the memory. For example, Oh discloses that, when a bad area information is generated, "the **controller [] stores** the updated bad area information in a **nonvolatile memory** portion []." *Id*. ¶236. Since the controller *actually* stores the information at the memory, it is necessarily configured to do so. Accordingly, Oh meets the second requirement.

Thus, Oh renders Claim 19 obvious.

8. Claim 20: The data storage device of claim 12, wherein the memory is a non-volatile memory that is monolithically formed in one or more physical levels of arrays of memory cells having an active area disposed above a silicon substrate, and further comprising circuitry associated with operation of the memory cells.

Oh renders Claim 20 obvious for the same reasons as Claim 11. *Supra* § VII.A.5; *see also* Ex-1002 ¶142; Ex-1020.

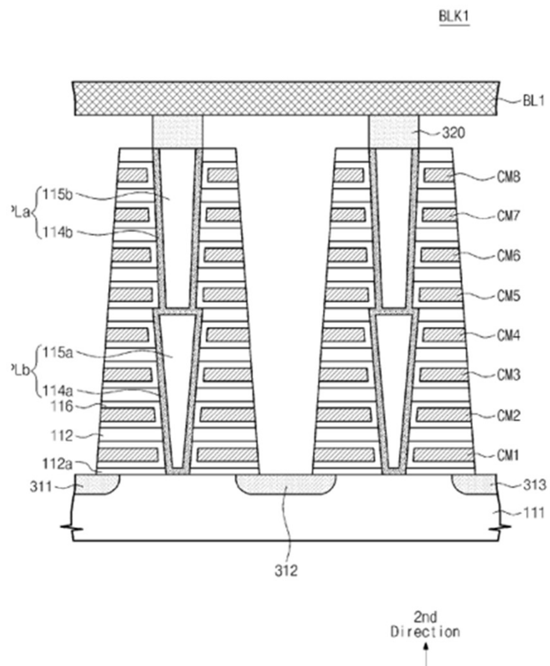
B. Ground 2: Claims 1, 2, 8, 11, 12, 13, 19, and 20 Are Obvious Over Oh in view of Oh ’738.

Claims 1, 2, 8, 11, 12, 13, 19, and 20 are obvious in light of Oh alone. *Supra* § VII.A. Claims 1 and 12 are further obvious over Oh in view of Oh ’738. *See* Ex-1002 ¶143.

1. Motivation to Combine Oh and Oh ’738

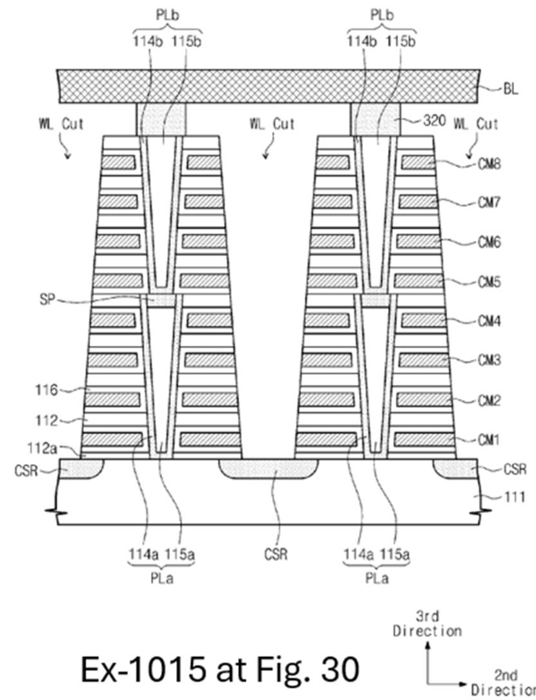
A POSITA would have been motivated to modify Oh in view of Oh ’738’s teaching that the layers adjacent to the area where sub pillars meet are dummy areas. *See* Ex-1002 ¶¶144-148. Oh and Oh ’738 are directed to the same area of technology, include the same inventors, were both assigned to Samsung Electronics, and were filed around the same time. *See, e.g.*, Ex-1005, Cover; Ex-1015, Cover. Specifically, both disclose 3D memory with similar structures. *See, e.g.*, Ex-1005 ¶6 (disclosing “a nonvolatile memory device including a plurality of memory blocks, each memory block containing memory layers stacked on a substrate”); Ex-1015, 9:18-22 (disclosing a memory structure with memory cells “stacked in a direction perpendicular to the substrate to form a three-dimensional memory structure”). For example, Oh’s Figure 17 and Oh ’738’s Figure 30 disclose nearly identical structures, as shown below:

Fig. 17



Ex-1005 at Fig. 17

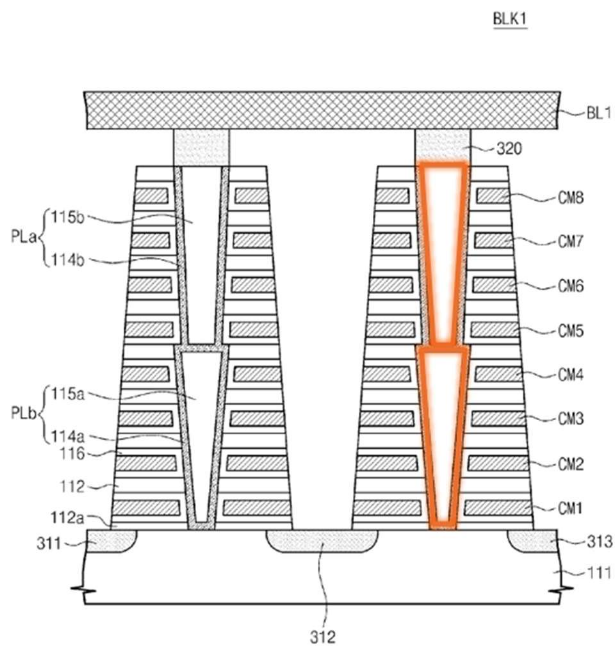
Fig. 30



Ex-1015 at Fig. 30

The semiconductor pillars extending through the memory layers are a critical component of a 3D memory device. *See, e.g.*, Ex-1005 ¶113. While having more vertical layers is a desirable feature in 3D memory, limitations in the etching process used to create the vertical pillars make it difficult to create tall pillars with a consistent width. Ex-1002 ¶145. One known solution to add more layers without exacerbating differences in the width of the pillars is to create multiple sub pillars, so only a subset of layers has to be etched at once. *Id*. Oh demonstrates the results of such a process—a device where the layers are penetrated by multiple sub pillars instead of just one pillar.

Fig. 17



Ex-1005, Fig. 17 (annotated).

Oh ’738 teaches techniques for connecting the sub pillars, such as by using a semiconductor pad. Ex-1015, 25:60-67. However, Oh ’738 recognizes that the memory layers adjacent to this connection point may be “dummy” areas. *Id*., 26:1-8. As detailed in Ground 1, Oh utilizes its technique to identify “bad areas,” but does not specifically focus on the particular layers around the sub pillar connection points. *See* Section VIII.A.1.c, *supra*.

Combining Oh’s teachings of detecting a bad area in 3D memory with Oh ’738’s teaching that the layers adjacent to the area where sub pillars meet are likely to be bad areas would have resulted in an improved memory device. Storing information about layers with low reliability so they are not used is central to the invention of Oh. Ex-1005 ¶65. A POSITA would have recognized that storing information about a known bad area—the area where two sub pillars meet—would have improved Oh's performance by enabling the memory device to avoid storing data in that area. Ex-1002 ¶147.

A POSITA would have had a reasonable expectation of success when modifying Oh according to Oh '738's teaching. *See* Ex-1002 ¶148. Oh's disclosure already includes structure with stacked sub pillars so a POSITA would have recognized the teachings of Oh '738 would be easily implemented in a similar structure. *See* Ex-1005, Fig. 17. Oh is about detecting bad areas, and the teaching of Oh '738 points out one particular area that is likely to be a bad area. Ex-1005 ¶65; Ex-1015, 26:1-8. Thus, a POSITA would have expected that Oh would detect the area identified by Oh '738 as a likely bad area. Ex-1002 ¶148. Moreover, the references share the same inventors, were filed around the same time, and were both assigned to Samsung. See, e.g., Ex-1005, Cover; Ex-1015, Cover. All of these facts would give a POSITA confidence that the systems and methods described would work well together and combining their teachings would result in an operable and improved device.

2. Claim 1

As discussed in Section VII.A.1, supra, all elements of Claim 1 are obvious over Oh alone. *See* Ex-1002 ¶149.

a. Element 1[b]: storing information at the data storage device, the information identifying a location associated with a variation of the structure

To the extent Element 1[b] is not obvious over Oh alone, it is obvious over Oh in light of Oh '738. *See* Ex-1002 ¶150-156. Element 1[b] requires the structure having a variation, information identifying a location associated with that variation, and storing that information at the data storage device. Oh in view of Oh '738 discloses or teaches these three requirements.

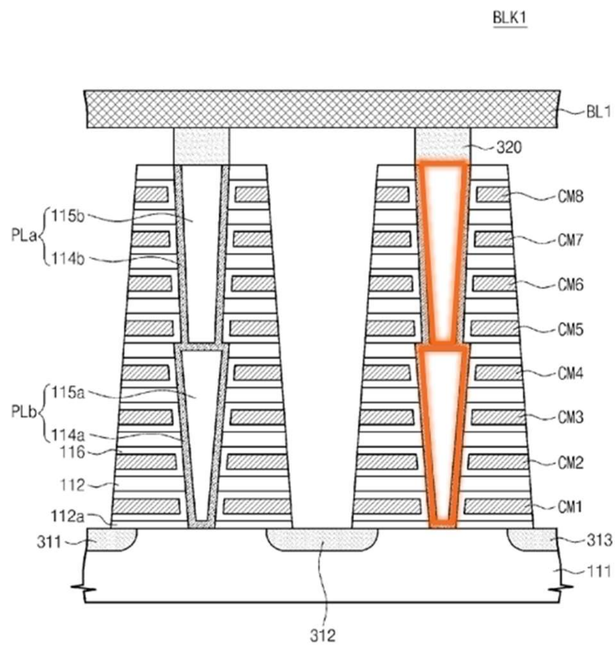
First, Oh alone discloses the structure having the claimed variation, as discussed in Section VII.A.1.c, *supra*. Oh '738 similarly identifies vertical pillars having a tapering variation. See Ex-1015, 15:31-32 ("cross-sectional areas of pillars PL may vary according to a distance from a substrate").

Second, Oh in view of Oh '738 discloses "information identifying a location associated with a variation of the structure." As discussed in more detail in Section VII.A.1.c, *supra*, Oh's "bad area information" identifies a layer, which identifies a location in the same sense as the '838 Patent. Oh's bad area information identifies a location "associated with a variation of the structure," because it is an area where reliability is low, which is caused by the varying width of the structure. *See* Section VIII.A.1.c, *supra*.

To the extent that Oh does not disclose or teach "information identifying a location associated with a variation of the structure," Oh in view of Oh '738 does.

As demonstrated in the figure below, Oh discloses that each pillar can include multiple "sub pillars," stacked on each other in the vertical direction.

Fig. 17



Ex-1005, Fig. 17 (annotated); *see also id.*, ¶184 ("each semiconductor pillar PL . . . includes a first sub semiconductor pillar PLa and a second sub semiconductor pillar PLb"). Oh '738 discloses a virtually identical structure. Ex-1015, 25:31-59, Figs. 29, 30. At the location where the pillars meet, the different tapers of the sub pillars cause the width to suddenly change. *See* Ex-1005, Fig. 17; Ex-1015, Fig. 30. Oh '738 discloses that semiconductor pads ("SP") can electrically connect the upper and lower pillars. Ex-1015, 25:60-67. Further, Oh discloses that the layers "adjacent to semiconductor pads SP may constitute . . . dummy memory cells." *Id.*, 26:1-8. In other words, the layers associated with structural variation where two sub pillars meet are bad areas. Thus, a POSITA would expect Oh, which identifies layers as "bad areas" when it includes a bad memory cell, to generate "bad area information" identifying the memory layers associated with CM4 and CM5 in Figure 17 (above) as "bad areas." See Ex-1001 ¶¶65, 71, 155; Ex-1002 ¶153. This bad area information identifies where the taper of the structures suddenly changes, which is "a location associated with a variation of the structure."

Thus, Oh in view of Oh '738 discloses or teaches "information identifying a location associated with a variation of the structure."

Third, Oh alone discloses storing the claimed information. *See* Section VII.A.1.c, *supra*.

Thus, Oh in view of Oh '738 renders Claim 1 obvious.

3. Claim 12

As discussed in Section VII.A.2, *supra*, all elements of Claim 12 are obvious over Oh alone. *See* Ex-1002 ¶157-158. To the extent that Oh alone does not disclose "information identifying a location associated with a variation of the structure," Oh in view of Oh '738 does, for the same reasons discussed in Section VII.B.2.a, *supra*.

Thus, Oh in view of Oh '738 renders Claim 12 obvious.

C. Ground 3: Claims 1, 2, 3, 8, 11, 12, 13, 14, 19, and 20 are obvious over Tokiwa.

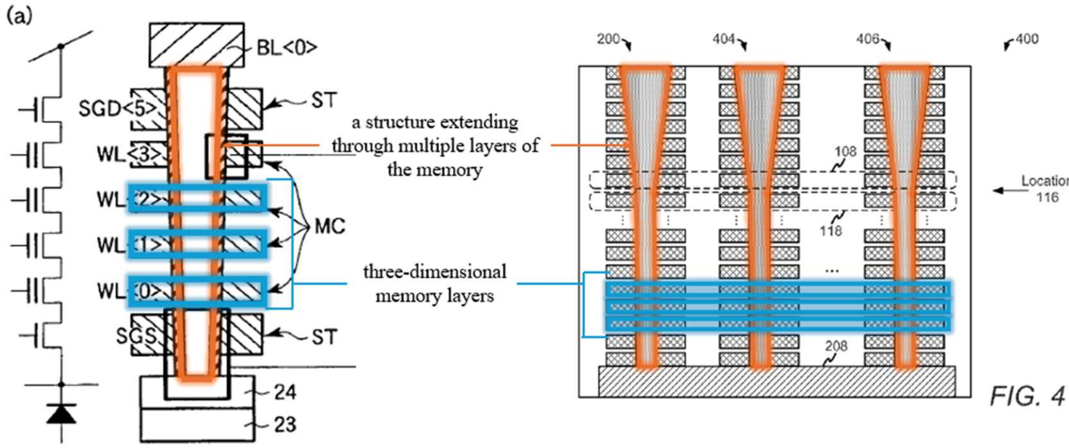
1. Claim 1

a. Element 1[pre]: A method comprising:

To the extent the preamble is limiting, Tokiwa discloses the preamble. *See* Ex-1002 ¶159. Tokiwa discloses "a method," because it discloses, for example, "a circuit configuration and **a method** . . . wherein the potentials to be supplied to the word lines are adjusted to potentials suitable therefor." Ex-1006, 11:45-48 (emphasis added).

b. Element 1[a]: in a data storage device that includes a memory having a three-dimensional (3D) memory configuration and including a structure extending through multiple layers of the memory, performing:

Element 1[a] requires a data storage device that includes 1) a memory having a three-dimensional (3D) memory configuration; and 2) a structure extending through multiple layers of the memory. As illustrated by a comparison of Tokiwa's Figure 5(a) and the '838 Patent's Figure 4 (both annotated below), and explained more fully below, Tokiwa discloses or teaches a data storage device with both of these requirements.



Tokiwa, Figure 5(a) | '838 Patent, Figure 4

Id., Fig. 5; Ex-1001, Fig. 4; *see also* Ex-1002 ¶¶160-163.

First, Tokiwa discloses or teaches a data storage device. Tokiwa discloses a bit cost scalable (BiCS) memory chip, which is the claimed "data storage device." Ex-1006, 1:38-41, 6:59-62. This memory chip is a "data storage device" because a host can "input/output data to/from the memory chip." *Id*., 7:39-48; *see also id*., 7:52-53 ("**Data is stored** in a nonvolatile manner in each of the memory cells.") (emphasis added).

As illustrated above, Tokiwa's memory chip has the required "three-dimensional (3D) memory configuration." For example, Tokiwa discloses "**a three-dimensionally stacked** nonvolatile semiconductor memory," Ex-1006, 1:35-36 (emphasis added); *see also id*., 1:51-56 ("the number of cells constituting a NAND array is longitudinally increased due to the increase in the number of stacked layers, thereby obtaining a memory capacity far above the limit of the memory capacity of a two-dimensionally structured NAND-type flash memory.")

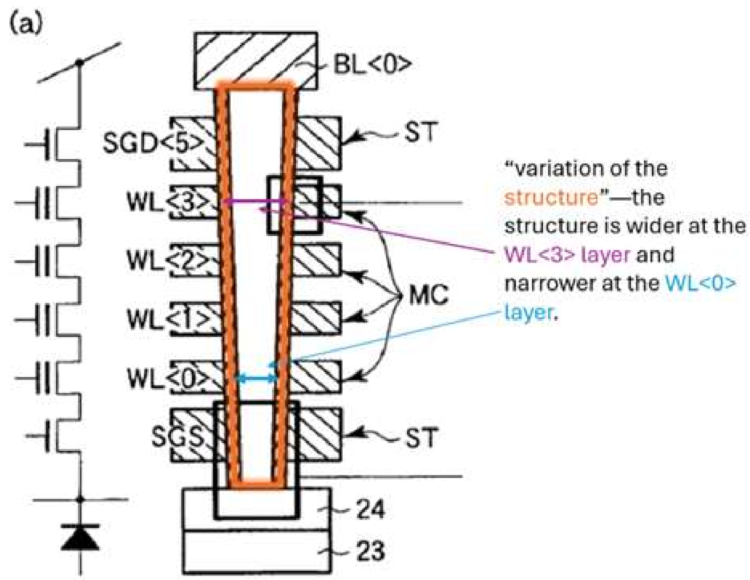
Second, Tokiwa's memory chip includes the claimed "structure extending through multiple layers of the memory," as illustrated above. For example, Tokiwa discloses "a semiconductor column which extends through the four or more conductive layers." *Id*., 2:30-32; *see also id*., 6:1-3 ("[T]he columnar active layers AA are formed in the hole extending through the plurality of stacked conductive layers and insulating layers."). These columns are even formed through the same or similar etching process that is disclosed in the '838 Patent. *Compare* Ex-1001, 12:8-17, *with* Ex-1006, 6:1-26. Thus, Tokiwa's semiconductor columns are the claimed "structure extending through multiple layers of the memory."

Accordingly, Tokiwa discloses or teaches Element 1[a].

c. Element 1[b]: storing information at the data storage device, the information identifying a location associated with a variation of the structure; and

Element 1[b] requires the structure having a variation, information identifying a location associated with that variation, and storing that information at the data storage device. Tokiwa discloses or teaches these three requirements. *See* Ex-1002 ¶¶164-174.

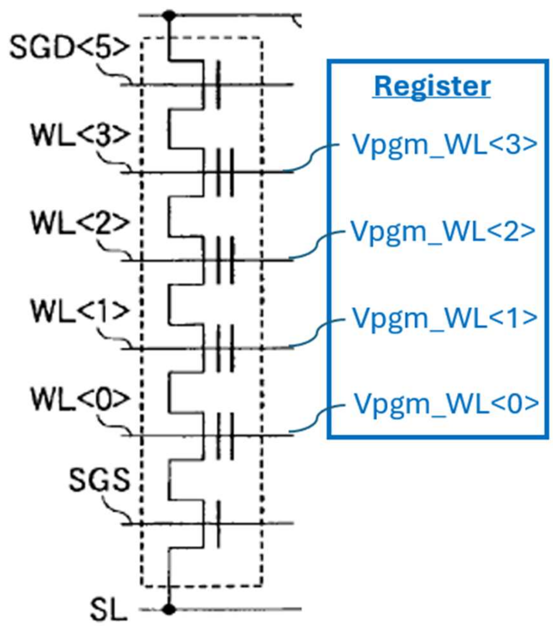
First, Tokiwa discloses that the structure has the claimed variation. Tokiwa discloses that its "columnar active layers" are formed in a hole formed by an etching method that extends through the layers. Ex-1006, 6:1-6. Tokiwa explains that "when the hole is formed by the reactive ion etching (RIE) method, the sectional shape of the hole tends to be tapered if the aspect ratio of the hole is high." *Id*. Because the etching method forms a tapered hole, "the active layers [] embedded in this hole are also **tapered**." *Id*., 6:6-7 (emphasis added); *see also id*., 6:15-18 ("[T]here may be a dimensional difference in shape between the memory cell provided on the upper side . . . and the memory cell provided on the lower side."). Figure 5(a) (annotated below) illustrates how Tokiwa's structures are tapered.



Id., Fig. 5 (annotated). A POSITA would have understood that this width variation was the claimed "variation of the structure" because the variation is described the same way in the '838 Patent. Ex-1002 ¶166 (citing Ex-1001, 13:28-45 and Ex-1006, 9:47-57). The '838 Patent itself repeatedly describes the variation as tapering. *See,* *e.g.*, Ex-1001, 2:34, 5:12-13, 12:26-28; 14:19-20. Thus, Tokiwa's variation through tapering discloses the claimed "variation of the structure."

Second, Tokiwa teaches the claimed "information identifying a location associated with a variation of the structure." The variation, as described above, is a variation through tapering. Ex-1006, 6:6-7. Tokiwa explains that this structural tapering causes variations in the speed of read and write operations at the different layers if the "same potential" is applied to the word lines during reading or writing of data. *Id*., 9:47-57. Tokiwa teaches "it is possible to compensate for variations in electric properties of the memory cells due to the three-dimensional structure" by determining and applying a potential suitable for the layer that is being read from or written to. *Id*., 11:28-42. This ensures that the reading and writing time for each layer is consistent. *Id*.

To apply the appropriate potential for each word line given the width of the structure at that layer, Tokiwa discloses storing the information regarding the correct potential for each word line in a register. *Id*., 10:4-12 ("[T]he register circuit 33 retains, as one kind of setting information, information for generating supply potentials[,] which are adjusted in intensity for the respective word lines so that the write potentials… suitable for the plurality of word lines… may be supplied.") ; *see also id*., 8:3-10 (describing the register as retaining "values corresponding to a write potential suitable for each of the plurality of word lines"); 10:15-27 (providing an example of using the register circuit). Figure 9 (annotated below) illustrates the potential values stored in the register, and how they correlate to each word line.



Id., Fig. 9 (annotated). As described below, the potential values stored in the register is the claimed "information identifying a location associated with a variation of the structure."

As shown in the annotated Figure, each potential value identifies a "location," because it is associated with a word line, which is associated with a particular memory layer above the substrate. See *id*., 9:47-57. The '838 Patent identifies a location in the same way—by defining a height above the substrate. For example, the '838 Patent describes the claimed "location" as "a region of the structure" that "correspond[s] to a distance within the memory [] from a surface of a substrate." Ex-1001, 12:26-27, 5:17-21; see also 15:31-40 ("[T]he location [] defines a level. . . .

The level [] may define a plane that intersects each of the [memory blocks] at a level k, where k is a positive integer indicating a distance between the substrate [] and the location.”).

The “location” identified by the register circuit information is “associated with a variation of the structure.” Under the District Court’s “plain and ordinary meaning” construction, information that is associated with any variation of the structure meets the claim language. Ex-1016, 40-49. As described above, the potential value appropriate for each word line accounts for variations in the width of the pillar. Thus, each potential value is information identifying a location (a layer) associated with a variation of the structure (the width at that layer).

Thus, Tokiwa discloses or teaches “information identifying a location associated with a variation of the structure.”

Third, Tokiwa discloses “storing” the register circuit information “at the data storage device,” as claimed. For example, Tokiwa teaches that the register circuit “**retains**, as one kind of setting information, values corresponding to a write potential suitable for each of the plurality of word lines.” Ex-1006, 8:3-10 (emphasis added). To the extent Patent Owner argues the claimed information must be stored in the 3D memory array, Tokiwa also discloses this as an alternative. *Id.*, 16:11-20 (“[A] potential code corresponding to this potential (trimming value) is written into the setting information area . . . of the memory cell array.”); *see also id.*, 18:35-41

("[T]he reference code indicating the supply potential . . . [is] stored in the register circuit [] and the memory cell array."). Figure 8 (annotated below) shows that both the memory cell array and the register circuit, or RAM,[2] are components of Tokiwa's "BiCS memory chip," which is the data storage device.

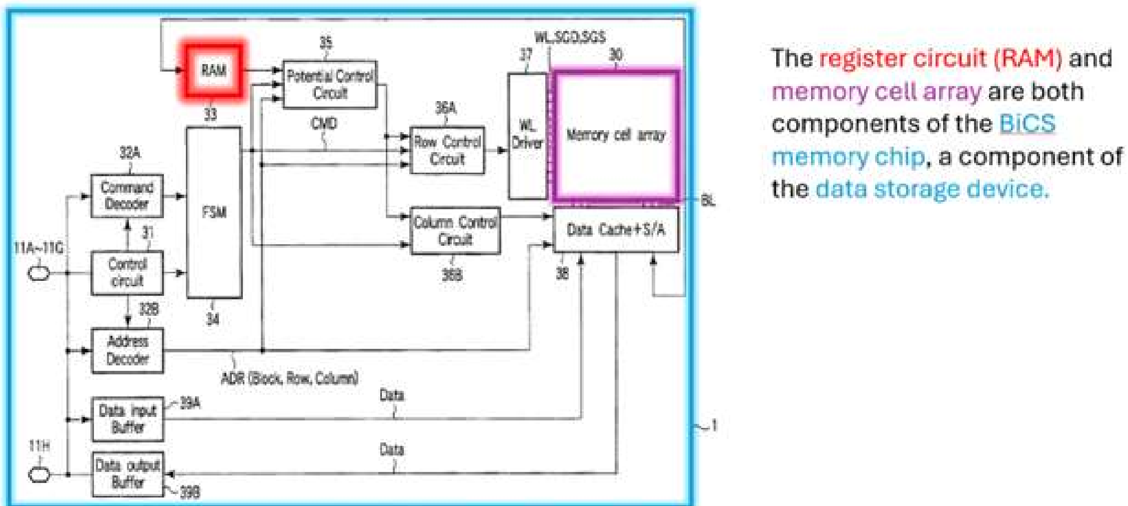


FIG. 8

Id., Fig. 8; *see also id.*, 7:49-8:67.

Accordingly, Tokiwa teaches or discloses element 1[b].

d. Element 1[c]: accessing the information.

Tokiwa discloses or teaches the claimed "accessing the information." *See* Ex-1002 ¶¶175-176. For example, Tokiwa discloses that "[a] potential control circuit 35 **reads** the setting information for the supply potentials retained in the register circuit 33 in accordance with an input address signal, and supplies the word lines…with the

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[2] The register circuit, labeled 33 in Figure 8, is also called a RAM. *Id.*, 8:3 ("A register circuit (e.g., a RAM) 33 ...").

potentials suitable therefor." Ex-1006, 10:11-15 (emphasis added). A POSITA would have understood that by "reading" the setting information, the information is inherently being "accessed." Ex-1002 ¶175. Tokiwa further describes that the suitable potentials retained in the registers are "output to" the potential control circuit, which selects the appropriate potential based on the address for the desired operation. *Id*., 11:66-12:19. Accordingly, Tokiwa discloses or teaches Element 1[c].

Thus, Tokiwa renders Claim 1 obvious.

2. Claim 12

a. Element 12[pre]: A data storage device comprising:

Tokiwa discloses or teaches Element 12[pre] for the same reasons as Element 1[a]. *Supra* § VII.C.1.b; *see also* Ex-1002 ¶177; Ex-1020.

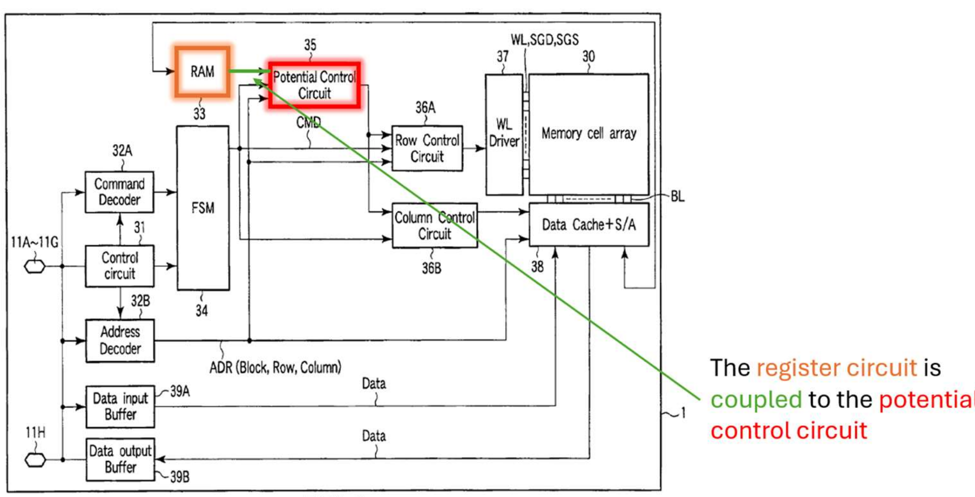
b. Element 12[a]: a memory having a three-dimensional (3D) memory configuration and including a structure extending through multiple layers of the memory;

Tokiwa discloses or teaches Element 12[a] for the same reasons as Element 1[a]. *Supra* § VII.C.1.b; *see also* Ex-1002 ¶178; Ex-1020.

c. Element 12[b] a controller coupled to the memory, wherein the controller is configured to access information that is stored at the memory, the information identifying a location associated with a variation of the structure.

Tokiwa discloses or teaches "information identifying a location associated with a variation of the structure," for the same reasons as Element 1[b]. *Supra* § VII.C.1.c; *see also* Ex-1002 ¶179; Ex-1020.

Tokiwa also teaches the remainder of Element 12[b], which requires "a controller coupled to the memory" and that the "controller is configured to access information that is stored at the memory." *See* Ex-1002 ¶¶180-183. For example, Tokiwa discloses that "[T]he potential control circuit [] **reads** the setting information for the supply potentials retained in the register circuit." Ex-1006, 10:11-13 (emphasis added); *see also* Ex-1006, 10:28-32, 10:53-60. As discussed in relation to Element 1[b], the setting information retained in the register circuit is the claimed information. *Supra* § VII.C.1.c. Since the potential control circuit actually accesses ("reads") this information, it is necessarily configured to do so. Therefore, the potential control is the claimed controller "configured to access information that is stored at the memory." Figure 8 (annotated below) illustrates that the potential control circuit (red) is coupled (green) to the register circuit, or RAM (orange).



F I G. 8

Id., Fig. 8 (annotated).

To the extent Patent Owner argues that the information must be accessed from the memory cell array, Tokiwa also teaches this alternative. For example, Tokiwa discloses that "a potential code corresponding to this potential (trimming value) is written into the setting information area (not shown) ***of the memory cell array 30*** in the BiCS memory chip 1." *Id.*, 16:15-20 (emphasis added); *see also id.*, 18:35-41 ("[T]he reference code indicating the supply potential . . . [is] stored in the register circuit [] and the memory cell array."). Figure 8 (annotated below) illustrates that the memory cell array (purple) is coupled (green) to the register circuit (red) through the data cache.

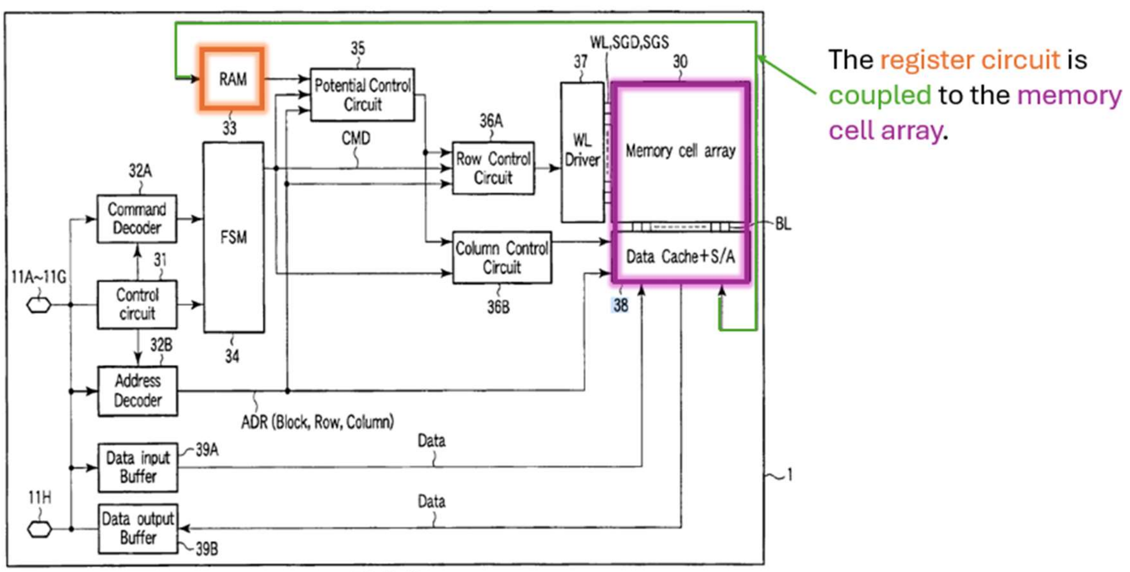


FIG. 8

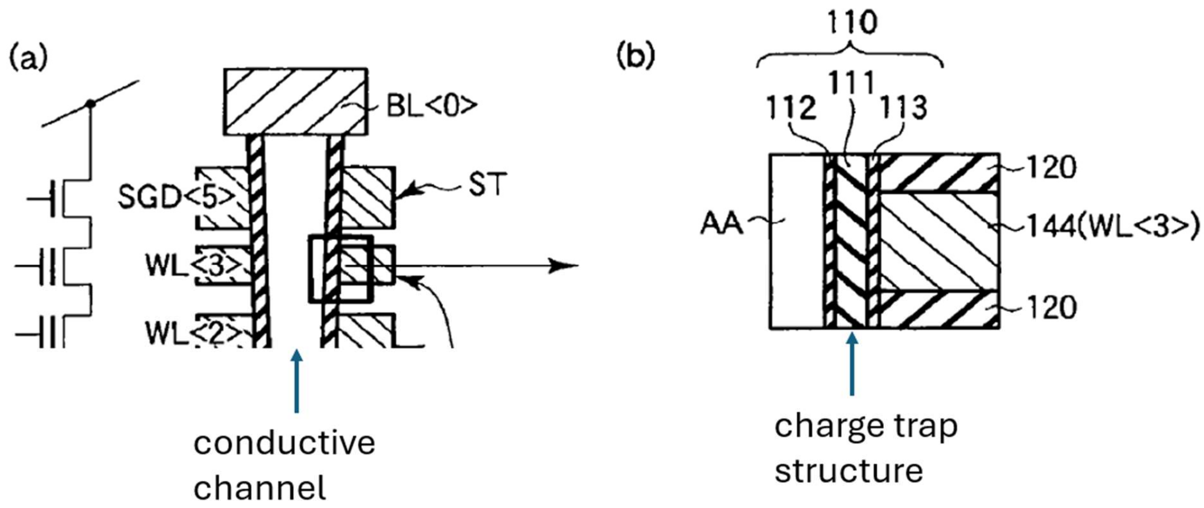
Id., Fig. 8 (annotated). While Tokiwa does not expressly disclose how the information is accessed from the memory cell array, it would have been obvious to a POSITA that the RAM loads this setting information from the memory cell array, for example on power up. *See* Ex-1002 ¶182. Thus, when the potential control circuit accesses the information from the register circuit as described above, it is accessing information stored in the memory cell array.

Thus, Tokiwa renders Claim 12 obvious.

3. Claim 2: The method of claim 1, wherein the structure includes a conductive channel and a charge trap structure, and wherein the variation corresponds to a difference between a first width of the structure at a first distance from a substrate of the memory and a second width of the structure at a second distance from the substrate, the second distance greater than the first distance.

a. Tokiwa discloses the conductive channel and a charge trap structure.

Tokiwa discloses or teaches this element's requirement that the structure includes both a charge trap structure and a conductive channel. *See* Ex-1002 ¶¶184-187. As shown in Figure 5 (annotated below), which illustrates detail in the semiconductor pillar discussed above with reference to Element 1[b], Tokiwa's structure has both.



Id., Fig. 5 (annotated).

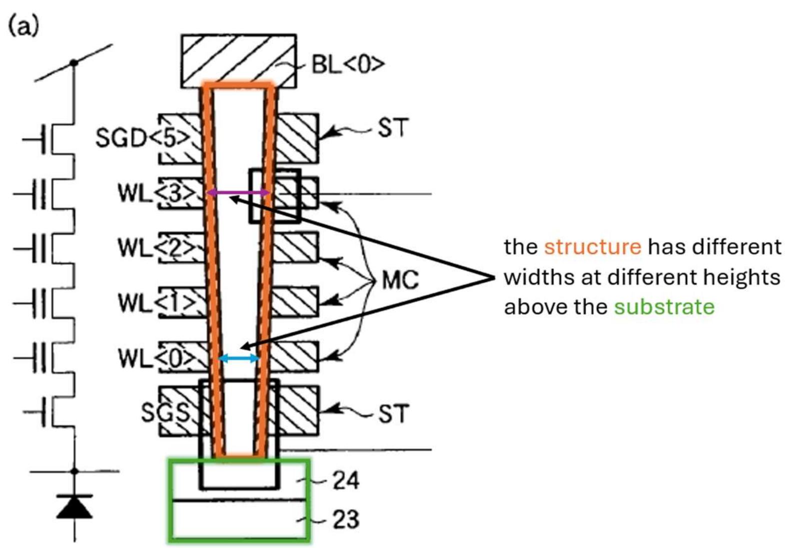
As illustrated above, Tokiwa discloses that "the memory cell MC includes, for example, an oxide-nitride-oxide (ONO) film 110 having a structure in which a **charge storage layer** 111 is held between two insulating films (oxide) 112, 113." *Id.*, 5:42-45 (emphasis added); *see also id.*, 5:53-55 ("The insulating film 113 functions as a block insulating film for preventing the leakage of a **charge trapped** by the charge storage layer 111.") (emphasis added). This charge storage layer is the claimed charge trap structure.

The portion of the structure that is not part of the ONO film is called the "active layer AA." *Id.*, 5:45-47, Fig. 5. The active layer AA is the claimed "conductive channel." For example, Tokiwa discloses the need for an insulating film between the ONO charge trap structure and the active layer "for preventing the leakage of a charge into the active area AA." *Id.*, 5:48-51. A POSITA would have understood that the active area is a conductive channel. Ex-1002 ¶186 (citing Ex-1014, explaining that conductive areas of memory devices are commonly referred to as "active."). Accordingly, the active layer AA is the claimed "conductive channel."

Accordingly, Tokiwa discloses or teaches that the structure includes a conductive channel and a charge trap structure.

b. Tokiwa discloses that the variation corresponds to a difference between the widths of the structure at two distances from the substrate.

Tokiwa discloses that the structure has different widths at different heights, as illustrated in Figure 5 (annotated below).



Ex-1006, Fig. 5 (annotated); *see also* Ex-1002 ¶¶ 188-190. As illustrated above, Tokiwa discloses that "the active layers AA tend to be **tapered**" such that the "pillar diameter . . . of the active layer AA at the [higher layers] tends to be equal to or more than a pillar diameter . . . of the active layer AA at the [lower layers]." Ex-1006, 6:14-26 (emphasis added); *see also* Ex-1006, 6:6-7 ("[T]he active layers AA embedded in this hole are also **tapered**.") (emphasis added). Accordingly, Tokiwa discloses the claimed variation of the structure.

Thus, Tokiwa renders Claim 2 obvious.

4. Claim 3: measuring a first parameter of a first storage element associated with a first layer of the memory; measuring a second parameter of a second storage element associated with a second layer of the memory; determining whether a difference between the first parameter and the second parameter satisfies a threshold.

Tokiwa discloses or teaches Claim 3. *See* Ex-1002 ¶¶191-195. Tokiwa describes a method of "trimming processing," which is "an operation wherein . . . a write potential which allows writing of data to be finished within a predetermined time is set as a write potential suitable for each of the word lines." Ex-1006, 14:3-10. In this method, an "initial write potential" is used to write data "into the selected cell connected to the selected word line." *Id*., 14:36-39. For each layer, "[t]he writing time is judged." *Id*., 14:41-42. In determining a writing time for each layer, Tokiwa measures a parameter for each—including a first parameter of a first layer and a second parameter of a second layer—as required by Claim 3.

For each layer, after measuring the time, Tokiwa's method determines "whether the data has been written within a predetermined [time]." *Id*., 14:40-41. "When writing of the data is completed within the predetermined writing time (predetermined period), the initial write potential [] is judged to be a potential suitable as the write potential." *Id*., 14:57-61. On the other hand, "[w]hen writing of the data is not completed with the predetermined period, the initial write potential… is judged to be unsuitable" and "is replaced with another value" to be retested. *Id*., 14:64-15:11. Tokiwa determines whether there is a difference in the writing time parameters for the different layers by comparing each of them to the same "predetermined period." *Id*. For example, Tokiwa's method might determine that the initial write potential writes data within the predetermined time for a first layer, but takes longer than that for a second layer. *Id*., 14:40-15:11. In this way, it determines that there is a difference in the writing time between the first and second layers—even without directly comparing those times—because it compares both to the same predetermined time. Thus, Tokiwa discloses Claim 3.

To the extent Tokiwa does not disclose or teach Claim 3, the method described in Claim 3 would have been obvious for a POSITA to try based on the disclosure of Tokiwa. Ex-1002 ¶193-194. Comparing the parameters to a universal "predetermined period" and comparing them to each other directly are different ways of achieving the same result—determining whether there are differences between the parameters. Moreover, it would have been obvious to a POSITA that one natural way of determining "a predetermined" time to use as a baseline would be to use the access time of the first word line as a baseline. In that case comparing subsequent layers to that baseline would be comparing a parameter associated with one layer (i.e., the tested layer W(n)) with a parameter associated with a second layer (i.e., the baseline layer W(0)).

Thus, Tokiwa renders Claim 3 obvious.

5. Claim 8: The method of claim 1, wherein the data storage device further includes a controller that is operationally coupled to the memory, wherein the information is stored at the memory, and wherein the controller accesses the information from the memory.

Tokiwa discloses or teaches Claim 8 for the same reasons described with reference to Element 12[b]. *Supra* § VII.C.2.c; *see also* Ex-1002 ¶¶196-197; Ex-1020. The only difference between Element 12[b] and Claim 8 is that Element 12[b] requires a controller "configured to access information," while Claim 8 requires that the controller "accesses the information." *See* Ex-1020. As described with reference to Element 12[b], Oh discloses a controller that is configured to access and actually does access the information from the memory. *Supra* § VII.C.2.c.

Thus, Oh renders Claim 8 obvious.

6. Claim 11: The method of claim 1, wherein the memory is a non-volatile memory that is monolithically formed in one or more physical levels of arrays of memory cells having an active area disposed above a silicon substrate, and wherein the data storage device further includes circuitry associated with operation of the memory cells.

a. Tokiwa discloses the required memory structure and formation.

The first portion of Claim 11 requires: 1) "the memory is a non-volatile memory"; 2) the memory "is monolithically formed in one or more physical levels of arrays of memory cells"; and 3) the memory has "an active area disposed above a silicon substrate." Tokiwa discloses or teaches each of these requirements. *See* Ex-1002 ¶¶198-201.

First, Tokiwa discloses a nonvolatile memory. For example, Tokiwa states that its invention "relates to a three-dimensionally stacked **nonvolatile semiconductor memory**." Ex-1006, 1:35-36.

Second, Tokiwa discloses or teaches that the memory is monolithically formed in one or more physical levels of arrays or memory cells. According to the '838 Patent, a "monolithic" three dimensional memory array is one where "one or more memory device levels are formed above a single substrate." Ex-1001, 35:24-26. Tokiwa discloses a "three-dimensionally stacked" memory with "four or more conductive layers **stacked on the semiconductor substrate** in the memory cell array." *Id.*, 1:35-36, 2:25-26 (emphasis added); *see also id.*, 2:51-53. A POSITA would have understood this to mean that Tokiwa's memory device is monolithically formed in one or more physical levels of arrays or memory cells. Ex-1002 ¶200 (citing Ex-1014, explaining that a monolithic memory device is one with "successive layers of transistors and interconnect on one substrate").

Third, Tokiwa discloses or teaches that its memory has "an active area disposed above a silicon substrate." Tokiwa discloses that its memory includes "four or more **conductive layers** stacked on the semiconductor substrate." *Id*., 2:25-27 (emphasis added). A POSITA would understand these conductive layers to be an active area. Ex-1002 ¶201 (citing Ex-1014, explaining that the layers formed above the substrate in a 3D memory are commonly called "active" layers). Moreover it would have been obvious to a POSITA to choose silicon as the material for a semiconductor substrate in a memory device. *Id*. Therefore, Tokiwa discloses or teaches the memory formation and structural requirements of Claim 11.

b. Tokiwa discloses the required circuitry associated with the operation of the memory cells.

Tokiwa discloses a data storage device that "includes circuitry associated with operation of the memory cells. *See* Ex-1002 ¶¶202-203. For example, Figure 8 (annotated below) "shows the **configuration of the circuits** for supplying potentials to the word lines." Ex-1006, 11:55-56 (emphasis added). The word lines are each associated with a memory cell. *See id*., Fig. 5.

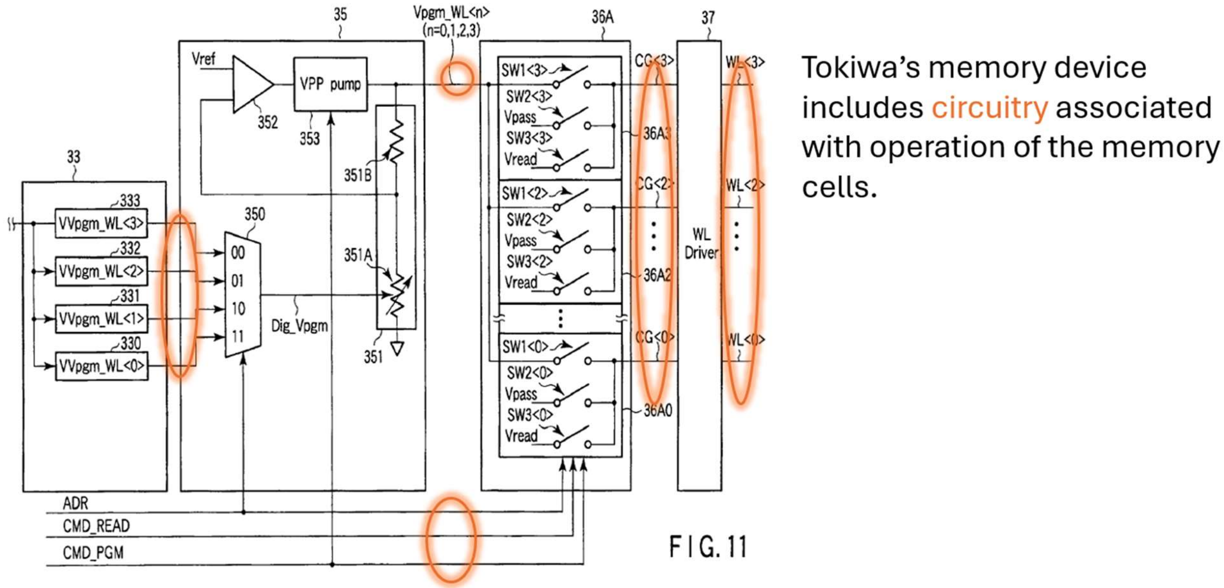


FIG. 11

Id., Fig. 11. Accordingly, Tokiwa discloses or teaches that "the data storage device further includes circuitry associated with operation of the memory cells."

Thus, Tokiwa renders Claim 11 obvious.

7. Claim 13: The data storage device of claim 12, wherein the structure includes a conductive channel and a charge trap structure, and wherein the variation is a difference between a first width of the structure at a first distance from a substrate of the memory and a second width of the structure at a second distance from the substrate, the second distance greater than the first distance.

Tokiwa renders Claim 13 obvious for the same reasons as Claim 2. *Supra* § VII.C.3; *see also* Ex-1002 ¶204; Ex-1020.

8. Claim 14: wherein the controller is further configured to measure a first parameter of a first storage element associated with a first layer of the memory, to measure a second parameter of a second storage element associated with a second layer of the memory, and to determine whether a difference between the first parameter and the second parameter satisfies a threshold.

Tokiwa renders Claim 14 obvious for the same reasons as Claim 3. *Supra* § VII.C.4; *see also* Ex-1002 ¶205; Ex-1020.

9. Claim 19: wherein the controller is further configured to generate the information in response to determining the location and to store the information at the memory.

Claim 19 requires the controller to be configured: 1) to generate the information in response to determining the location; and 2) to store the information at the memory. Tokiwa's controller meets both of these requirements. *See* Ex-1002 ¶¶206-209.

First, Tokiwa discloses or teaches a controller configured to generate the information in response to determining the location. As described in relation to Element 1[b], variations in the width of the structure mean that different write potentials should be supplied to each layer. *Supra* § VII.C.1.c. Tokiwa discloses that "[w]hen writing of the data is not completed within the predetermined period, the initial write potential . . . provided immediately before the writing is judged to be unsuitable." Ex-1006, 14:64-67. When this happens "the value provided immediately before the writing is **replaced with another value**." *Id.*, 15:2-4 (emphasis added). This process is repeated until a suitable potential is identified, which "is treated as a potential suitably supplied to the word line . . . which has been subjected to the trimming processing." *Id.*, 16:10-14. Thus, Tokiwa generates information in response to determining the location of a variation.

Second, Tokiwa discloses storing the information at the memory. After generating a suitable potential for a word line as described above, the value "is written into the setting information area [] of the memory cell array." *Id.*, 16:16-18.

Thus, Tokiwa renders Claim 19 obvious.

10. Claim 20: The data storage device of claim 12, wherein the memory is a non-volatile memory that is monolithically formed in one or more physical levels of arrays of memory cells having an active area disposed above a silicon substrate, and further comprising circuitry associated with operation of the memory cells.

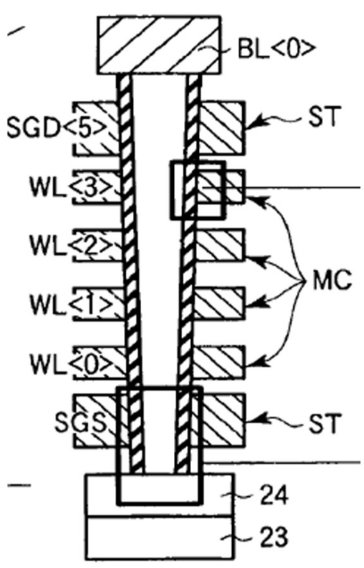
Tokiwa renders Claim 20 obvious for the same reasons as Claim 11. *Supra* § VII.C.6; *see also* Ex-1002 ¶210; Ex-1020.

D. Ground 4: Claims 1, 2, 3, 8, 11, 12, 13, 14, 19, and 20 are obvious over Tokiwa in view of Oh '738.

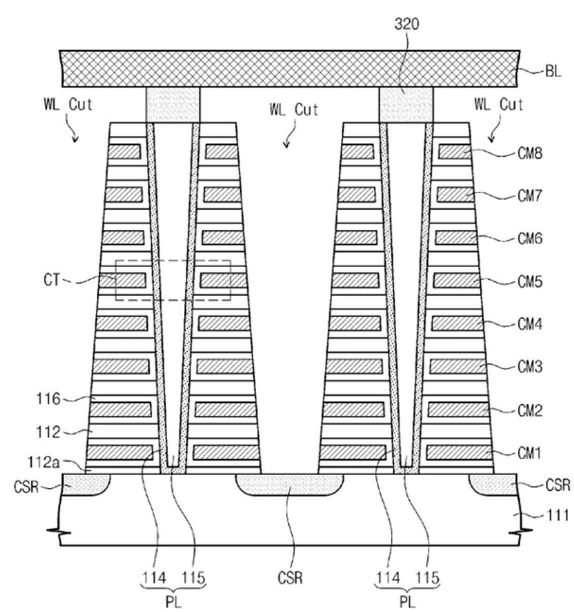
Claims 1, 2, 3, 8, 11, 12, 13, 19, and 20 are obvious in light of Tokiwa alone. *Supra*, § VII.C. Claims 1 and 12 are further obvious over Tokiwa in view of Oh '738. *See* Ex-1002 ¶211.

1. Motivation to Combine Tokiwa and Oh ’738

A POSITA would have been motivated to modify Tokiwa in view of Oh ’738’s teaching that a 3D memory device can include vertically stacked sub pillars instead of just one monolithic pillar. *See* Ex-1002 ¶¶212-215. Tokiwa and Oh ’738 are directed to the same area of technology as both disclose 3D memory with similar structures. *See, e.g.*, Ex-1006, 2:22-27 (disclosing “[a] three-dimensionally stacked nonvolatile semiconductor memory” including “four or more conductive layers stacked on the semiconductor substrate”); Ex-1015, 9:18-22 (disclosing a memory structure with memory cells “stacked in a direction perpendicular to the substrate to form a three-dimensional memory structure”). For example, Tokiwa’s Figure 5 and Oh ’738’s Figure 6 disclose nearly identical structures, as shown below:



Ex-1006, Fig. 5

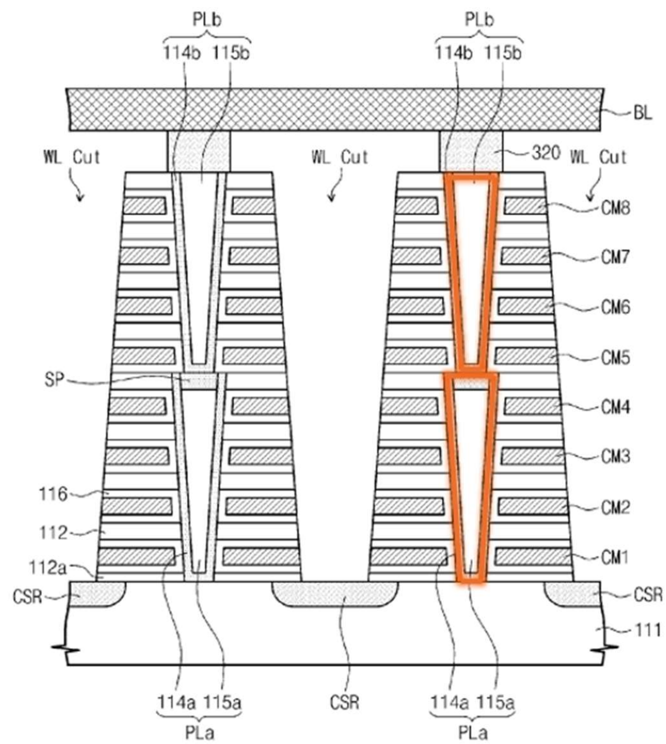


Ex-1015, Fig. 6

Moreover, Tokiwa and Oh '738 are directed to solving the same problem: accounting for electrical variations between the memory layers when programming those layers. *See, e.g.*, Ex-1006, 9:47-53 ("[V]ariations in the parameters of physical shapes such as the sizes (pillar diameters) of the active layers AA . . . cause variations in the potential application time necessary for reading from the respective memory cells."); Ex-1015, 15:46-56 ("When a cross-sectional area of a pillar decreases . . . program speed of memory cells may increase.").

The semiconductor pillars extending through the memory layers are a critical component of a 3D memory device. *See, e.g.*, Ex-1006, 4:45-59, 5:39-59. While having more vertical layers is a desirable feature in 3D memory, limitations in the etching process used to create the vertical pillars make it difficult to create tall pillars with a consistent width. Ex-1002 ¶213. One known solution to add more layers without exacerbating differences in the width of the pillars is to create multiple sub pillars, so only a subset of layers has to be etched at once. *Id*. Oh '738 demonstrates the result of such a process—a device where the layers are penetrated by multiple sub pillars instead of just one pillar.

Fig. 30



Ex-1015, Fig. 30.

A POSITA would have been motivated to modify Tokiwa with Oh's teaching that multiple sub pillars can be used instead of just one pillar because this would result in an improved memory device with greater storage capacity. Ex-1002 ¶214. Using sub pillars allows the device to have more layers, which increases the amount of data that the device can store. *Id*. Moreover, it decreases the tapering effect, allowing the conductive materials in the memory layers to have a more consistent width than they otherwise would. *Id*.

A POSITA would have had an expectation of success when modifying Tokiwa with Oh's sub pillar teaching. Ex-1002 ¶215. Using multiple sub pillars instead of one monolithic pillar was a known method for improving 3D memory devices by increasing the number of memory layers that could be stacked. *Id*. Moreover, Tokiwa and Oh '738 are directed at solving the same problem—accounting for electrical variations between the memory layers caused by the variable width of the structures. *Compare* Ex-1006, 9:47-10:18; *with* Ex-1015, 15:31-56. Thus, a POSITA would have expected the problem to be solvable whether applying the method to a structure with one monolithic pillar or multiple sub pillars.

2. Claim 1

As discussed in Section VII.C.1, *supra*, all elements of Claim 1 are obvious over Tokiwa alone. *See* Ex-1002 ¶216

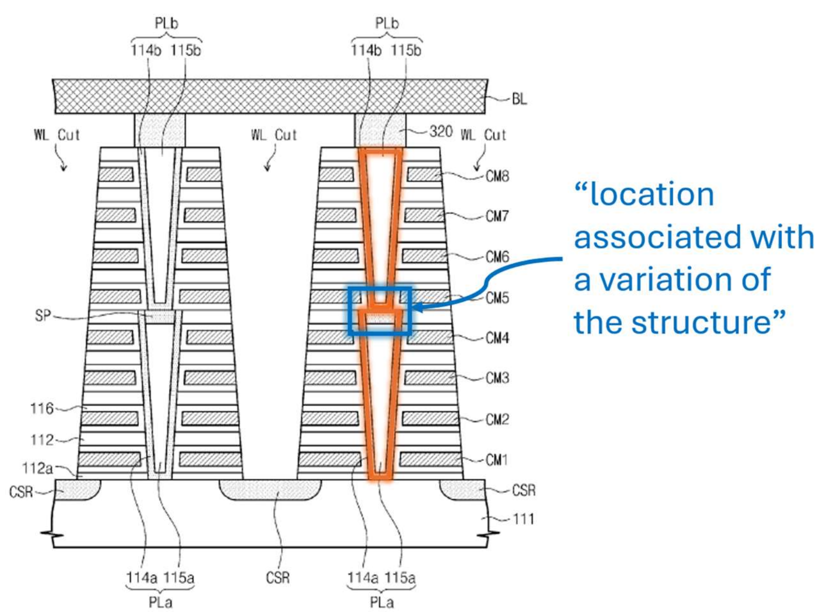
a. Element 1[b]: storing information at the data storage device, the information identifying a location associated with a variation of the structure

To the extent Element 1[b] is not obvious over Tokiwa alone, it is obvious over Tokiwa in light of Oh '738. *See* Ex-1002 ¶217-222. Element 1[b] requires the structure having a variation, information identifying a location associated with that variation, and storing that information at the data storage device. Tokiwa in view of Oh '738 discloses or teaches these three requirements.

First, Tokiwa alone discloses the structure having the claimed variation. *Supra* § VII.C.1.c. Oh '738 similarly identifies vertical pillars having a tapering variation. *See* Ex-1015, 15:31-32 ("cross-sectional areas of pillars PL may vary according to a distance from a substrate").

Second, Tokiwa in view of Oh '738 discloses "information identifying a location associated with a variation of the structure." For example, Oh '738 discloses a 3D memory structure in which 2 tapered pillars are stacked on top of each other. Ex-1015, 25:31-67, Fig. 30. At the location where the pillars meet, the different tapers of the sub pillars cause the width to suddenly change. Thus, this area is "a location associated with a variation of the structure."

Fig. 30



Id., Fig. 30 (annotated). Applying this teaching regarding the Oh '738's stacked tapered pillar structure to Tokiwa's register circuit would result in a register circuit that specifically identifies the location where the two pillars meet. Because Tokiwa's register circuit information varies with the width of the pillar (Ex-1006, 13:55-14:2) potential values would start relatively low at layer CM1, increase up to CM4, then suddenly drop at CM5. Thus, the register circuit would identify the structural variation that begins between layers CM4 and CM5. This is identical to the way the '838 Patent identifies the location—between two layers. Ex-1001, 12:24-35 ("the location 116 is between the storage elements 204, 206 because the structure 202 begins 'tapering' approximately between the storage elements 204, 206.").

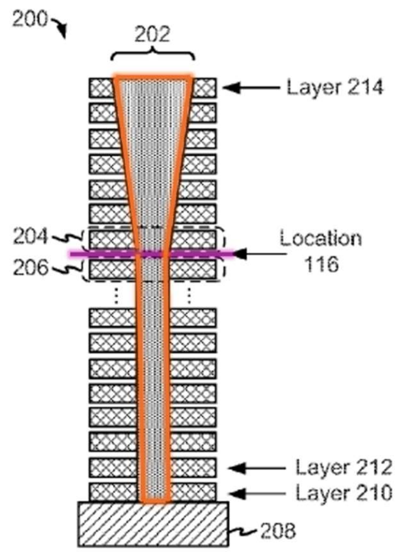


FIG. 2

Id., Fig. 2 (annotated).

Thus, Tokiwa in view of Oh '738 discloses "information identifying a location associated with a variation of the structure."

Third, Tokiwa alone discloses storing the claimed information. *Supra* § VIII.A.1.c.

Thus, Tokiwa in view of Oh '738 renders Claim 1 obvious.

3. Claim 12

As discussed in Section VII.C.2, *supra*, all elements of Claim 12 are obvious over Tokiwa alone. *See* Ex-1002 ¶¶223-224. To the extent that Tokiwa alone does not disclose "information identifying a location associated with a variation of the structure," Tokiwa in view of Oh '738 does, for the same reasons discussed in Section VII.D.2.a, *supra*.

Thus, Tokiwa in view of Oh '738 renders Claim 12 obvious.

VIII. CONCLUSION

The unpatentability grounds presented above are reasonably likely to prevail, and IPR should be instituted for Claims 1-3, 8, 11-14, and 19-20 of the '838 Patent based on each of the grounds specified in this Petition.

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CERTIFICATE OF WORD COUNT

Under 37 C.F.R. § 42.24(d), Petitioner certifies that this petition includes 12,068 words, as measured by Microsoft Word, exclusive of the table of contents, mandatory notices under § 42.8, certificates of service, word count, and exhibits.

CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))

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