

**UNITED STATES PATENT AND TRADEMARK OFFICE**

---

**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

---

**SAMSUNG ELECTRONICS CO., LTD. AND  
SAMSUNG ELECTRONICS AMERICA, INC.,**  
Petitioners

v.

**MAXELL CORPORATION,**  
Patent Owner

Inter Partes Review No.: IPR2025-01309

**PETITION FOR *INTER PARTES* REVIEW OF  
U.S. PATENT NO. U.S. 7,577,417 UNDER 35 U.S.C. §§ 311-319  
AND 37 C.F.R. §§ 42.1-100, ET SEQ**

**TABLE OF CONTENTS**

	<b>Page</b>
I. INTRODUCTION .....	5
II. STATEMENT OF PRECISE RELIEF REQUESTED .....	5
III. THE '417 PATENT .....	5
A. Summary of the '417 Patent.....	5
B. File History and Priority Date of the '417 Patent .....	6
IV. SUMMARY OF PRIOR ART.....	7
A. EX1004 - Belt.....	7
B. EX1005 - Foster .....	7
C. EX1006 - Norris .....	7
D. EX1007 - Alberth .....	7
V. CLAIM CONSTRUCTION UNDER 37 C.F.R. § 42.104(B)(3).....	7
A. Claim Construction Standards.....	7
B. Person of Ordinary Skill in the Art .....	8
VI. GROUND 1: CLAIMS 1-2, 4-7 ARE RENDERED OBVIOUS BY BELT, FOSTER AND NORRIS .....	9
A. Claim 1 .....	9
1. [1pre].....	9
2. [1a] .....	10
3. [1b].....	11
4. [1c] .....	17
5. [1d].....	23
B. Claim 2 .....	26
C. Claim 4 .....	31
1. [4a] .....	31
2. [4b].....	35
D. Claim 5 .....	37
E. Claim 6 .....	39

F.	Claim 7 .....	41
VII.	GROUND 2: CLAIM 3 IS RENDERED OBVIOUS BY BELT, FOSTER, NORRIS AND ALBERTH .....	41
A.	Claim 3 .....	41
VIII.	DISCRETIONARY DENIAL IS NOT WARRANTED.....	46
IX.	MANDATORY NOTICES UNDER 37 C.F.R. §§ 42.8(B)(1)-(4).....	47
A.	Real Party-In-Interest .....	47
B.	Related Matters.....	47
C.	Lead and Backup Counsel.....	47
D.	Service Information.....	47
X.	CONCLUSION.....	48

**INDEX OF EXHIBITS**

<b>Exhibit No.</b>	<b>Description</b>
1001	U.S. Patent No. 7,577,417
1002	File History of U.S. Patent No. 7,577,417
1003	Declaration of R. Jacob Baker in Support of Petition for <i>Inter Partes</i> Review of U.S. Patent No. 7,577,417
1004	U.S. Patent 5,303,171 (“Belt”)
1005	U.S. Patent 6,223,293 (“Foster”)
1006	U.S. Patent 5,630,148 (“Norris”)
1007	U.S. Patent 6,094,565 (“Alberth”)

**CHART OF CLAIMS**

**[1pre]** A mobile terminal capable of being changed from an open condition into a closed condition, comprising:

**[1a]** a processor which executes program processing; and

**[1b]** a clock controller capable of changing a frequency of a clock signal to be fed to the processor;

**[1c]** wherein the clock controller controls the frequency of the clock signal so as to become a first frequency when the mobile terminal is in the open condition, and controls the frequency of the clock signal so as to become a second frequency lower than the first frequency when the mobile terminal is in the closed condition, and

**[1d]** wherein the clock controller controls the frequency of the clock signal so as to become a frequency higher than the second frequency when a specific processing is executed even if the mobile terminal is in the closed condition, and controls the frequency of the clock signal so as to become the second frequency after the execution of the specific processing is completed.

**[2]** The mobile terminal according to claim 1, wherein the specific processing is a processing having an effect on a response to a request from the user.

**[3]** The mobile terminal according to claim 1, wherein the specific processing is an image decoding processing or an address retrieval processing or a character conversion processing.

**[4pre]** The mobile terminal according to claim 1, further comprising

**[4a]** an input unit which allows a user of the mobile terminal to set the frequency of the clock signal,

**[4b]** wherein when the frequency is set by the user using the input unit, the first frequency is the frequency set by the user using the input unit.

**[5]** The mobile terminal according to claim 4, wherein the user can set the frequency of the clock signal in every processing using the input unit.

**[6]** The mobile terminal according to claim 1, further comprising a display which exhibits a display corresponding to the magnitude of the frequency of the clock signal.

**[7]** The mobile terminal according to claim 1, wherein the mobile terminal has a folded structure.

## I. INTRODUCTION

Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (“Petitioners”) request *inter partes* review of claims 1-7 (“Challenged Claims”) of U.S. Patent No. 7,577,417 (“’417 patent,” EX1001), owned by Maxell Corporation (“PO”).

In accordance with 37 C.F.R. § 42.104(a), Petitioner certifies that U.S. Patent 7,577,417 is available for *inter partes* review and that Petitioner is not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in this Petition.

This petition relies upon the declaration of R. Jacob Baker, Ph.D., P.E. (EX1003), and copies large portions of that declaration herein.

## II. STATEMENT OF PRECISE RELIEF REQUESTED

In accordance with 35 U.S.C. § 311, Petitioner requests cancelation of claims 1-7 of the ’417 patent in view of the following grounds:

Ground	Claims	Stat. Basis	Prior Art
1	1-2, 4-7	35 U.S.C. § 103	Belt, Foster and Norris
2	3	35 U.S.C. § 103	Belt, Foster, Norris and Alberth

## III. THE ’417 PATENT

### A. Summary of the ’417 Patent

The ’417 patent discloses a central processing unit (CPU) for a mobile terminal, such as a cell phone, that provides “both enhancement in processing

speed and reduction in current consumption” through a “clock control means capable of changing the frequency of a clock signal received from an oscillator under control by a [CPU].” EX1001, 1:44-48. The mobile terminal includes a folding condition detector for detecting when the device is in a folded (closed) condition or in an unfolded (open condition), such that the clock frequency can be changed to a low frequency in the closed condition to reduce power consumption. *Id.*, 5:35-38 and 58-62. When executing a specific processing even in the closed condition, the frequency of the clock is caused to change to a higher frequency, thereby enhancing processing speed, and then goes to a low frequency when the specific processing is completed. *Id.*, 5:62-6:2. The ’417 patent further states that the clock signal received by the CPU may either be raised or lowered in frequency—in response to a user request or processing—thereby increasing processing speed or increasing battery life, respectively. *Id.*, 3:7-27 (user requesting a change in CPU clock frequency), 4:32-40 (changing clock frequency in response to “specific processing”).

**B. File History and Priority Date of the ’417 Patent**

The ’417 patent claims priority as a continuation of U.S. 10/405,368 filed April 3, 2003 (now abandoned), and to JP 2002-100735 filed April 3, 2002.<sup>1</sup>

---

<sup>1</sup> Petitioners do not challenge the April 3, 2002 priority date for purposes of this IPR petition, however reserve their right to challenge whether any issued claims are entitled to that date either in litigation or in another IPR.

Issued claim 1 was allowed only after the inclusion of the last wherein clause.

EX1002, 20-26 (Applicant Amendment, March 2, 2009)

#### **IV. SUMMARY OF PRIOR ART**

##### **A. EX1004 - Belt**

U.S. Patent 5,303,171 (“Belt”), filed on 4/3/1992, issued on 4/12/1994, is prior art under pre-AIA 35 U.S.C. § 102(a) and (b).

##### **B. EX1005 - Foster**

U.S. Patent 6,223,293 (“Foster”), filed on 2/16/1995, issued on 4/24/2001, is prior art under pre-AIA 35 U.S.C. § 102(a) and (b).

##### **C. EX1006 - Norris**

U.S. Patent 5,630,148 (“Norris”), filed on 2/28/1996, issued on 5/13/1997, is prior art under pre-AIA 35 U.S.C. § 102(a) and (b).

##### **D. EX1007 - Alberth**

U.S. Patent 6,094,565 (“Alberth”), filed on 6/30/1997, issued on 7/25/2000, is prior art under pre-AIA 35 U.S.C. § 102(a) and (b).

#### **V. CLAIM CONSTRUCTION UNDER 37 C.F.R. § 42.104(B)(3)**

##### **A. Claim Construction Standards**

The Challenged Claims are interpreted using the same claim construction standard that is used to construe the claim in a civil action in federal district court, which is the “ordinary and customary meaning” as understood by a POSITA. 37

C.F.R. § 42.100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312, 1327 (Fed. Cir. 2005).

For purposes of this petition, Petitioners propose that each claim term in the Challenged Claims be given its “ordinary and customary meaning,” and that no specific construction of any claim term is required because the prior art relied on in this Petition meets each of the claim terms under any reasonable construction. Petitioners’ proposal to adopt the “ordinary and customary meaning” in this petition in no way limits their rights to assert a different claim construction of any claim term for any other purpose, including litigation or another IPR petition.

There is a presumption that the limitations “processor,” and “clock controller” and “input unit” do not invoke means-plus function because the limitations do not recite “means.” Petitioners therefore apply plain and ordinary meaning constructions for “processor,” and “clock controller” and “input unit.” EX1003, ¶53.

#### **B. Person of Ordinary Skill in the Art**

A person of ordinary skill in the art at the time of the alleged invention of the ’417 patent (April 2002) (“POSITA”) has a working knowledge of power management, gained through a degree in Electrical/Computer Engineering or an equivalent degree, and at least one year of experience in the field of power management.” Additional graduate education could substitute for professional

experience, and significant experience in the field could substitute for formal education. EX1003, ¶¶44-47.

**VI. GROUND 1: CLAIMS 1-2, 4-7 ARE RENDERED OBVIOUS BY BELT, FOSTER AND NORRIS**

**A. Claim 1**

**1. [1pre]**

To the extent that the preamble is limiting, Belt discloses “a mobile terminal (laptop computer system 10) capable of being changed from an open condition into a closed condition, comprising.”<sup>2</sup> EX1003, ¶¶56-57.

Belt discloses a portable computer in the form of “a computer system [] includes a housing, a lid supported on the housing for movement between open and closed positions[.]” EX1004, 1:64-67; *see also id.*, 1:13-17 (“Portable computers of the type commonly referred to as ‘laptop’ computers and ‘notebook’ computers are becoming very popular [and] [t]hey typically include a housing with a lid which is movable between open and closed positions[.]”), 2:40-43 (Fig.1 “show[s] a block diagram of a ‘notebook’ type laptop computer system 10”), 4:67-5:3.

---

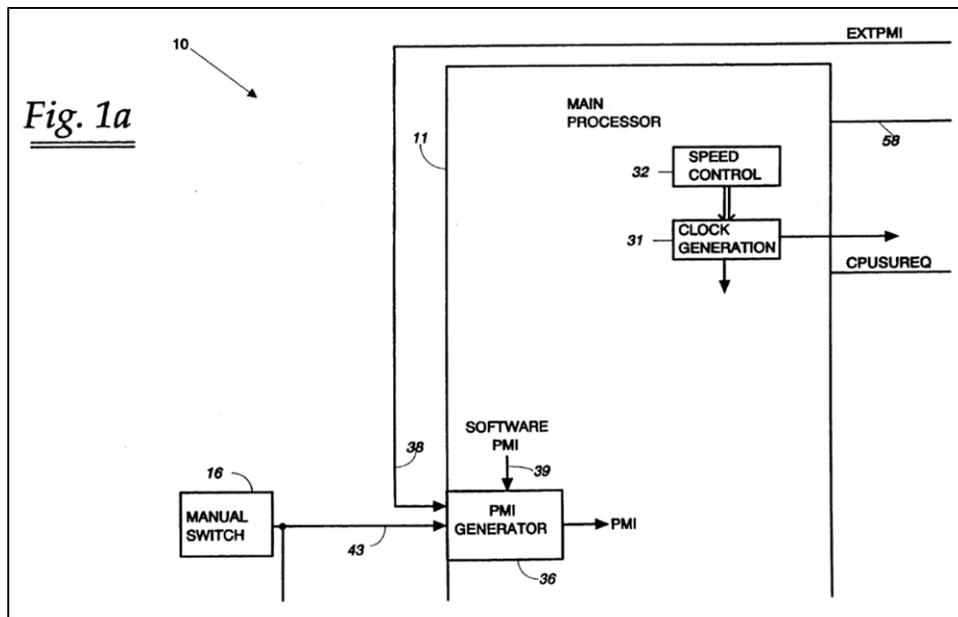
<sup>2</sup> The discussion for each claim limitation herein begins with a quote of the claim language in which parentheticals have been added to include exemplary arguments and evidence. However, Petitioner relies on all arguments and evidence provided with respect to a limitation (and any cross-referenced sections).

Belt's computer system 10 is indisputably within the scope of the limitation as the '417 patent similarly states that its mobile terminal can be in "a folded (closed) condition or in an unfolded (open position)." EX1001, 5:35-38, cl.7.

2. [1a]

Belt discloses "a processor which executes program processing (main processor 11)." EX1003, ¶¶58-60.

Belt discloses its "laptop computer system 10 includes a main processor 11." EX1004, 2:43-45, 2:54-67 (main processor 11 may be "implemented with an Intel 386SL, which is a conventional component commercially available"); Fig. 1a (reproduced below):



Belt also discloses that main processor 11 executes program processing. *Id.*, 2:35-37 ("Figs. 4-8 are flowcharts of selected program segments executed by a

main processor of the system of Fig. 1.”), 7:47-49 (“the special interrupt handling routine executed by the main processor 11”), 9:22-30. In further discussing the execution of program processing, Belt interchangeably refers to “main processor 11” as “processor 11,” “the processor” (numerically unidentified), and “CPU” (numerically unidentified). *Id.*, 3:47-49 (“[t]he processor 11 has several conventional modes of operation, one of which is ... *the program running in the processor 11* has access to all operational capabilities of the processor 11”) (emphasis added), 3:54-61 (“application program which is running in one of the protected modes” on “processor 11”), 7:68-8:2 (“the processor changes the register 32 in order to force the CPU to run at its fastest clock speed, so that the PMI routine will execute as fast as possible.”), 8:22-24 (“CPU continues with the execution of the program which was interrupted.”).

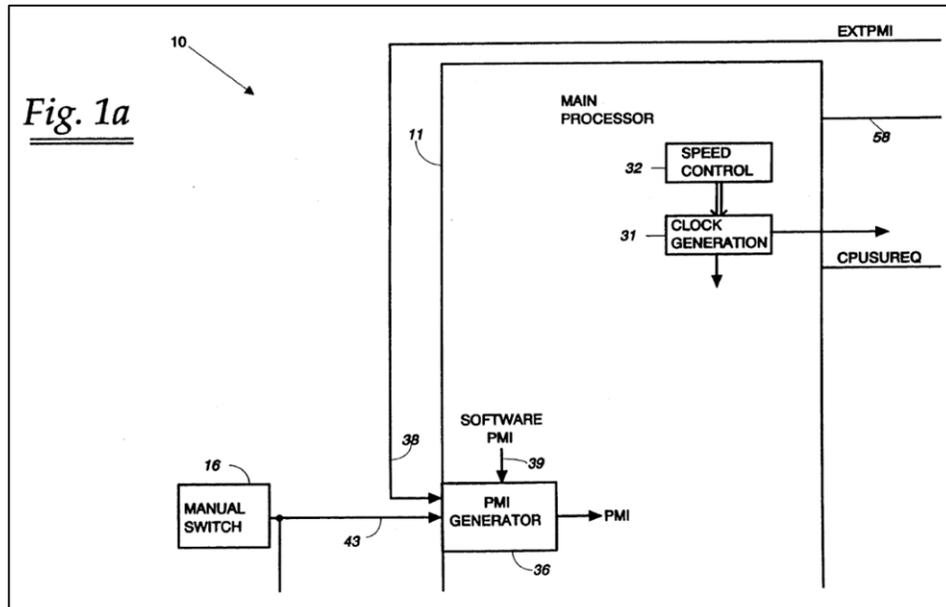
### 3. [1b]

Belt alone discloses, or in combination with Norris renders obvious, “a clock controller (Belt’s clock generator 31 and speed control register 32, Norris’ clock generator circuit 14) capable of changing a frequency of a clock signal to be fed to the processor (main processor 11).” EX1003, ¶¶61-72.

Belt discloses “the main processor 11 includes a clock generator 31 which generates respective clocks for various components of the system, *including the*

processor 11 itself, and which is controlled by a speed control register 32.”

EX1004, 3:1-5 (emphasis added). *See also* Fig. 1a (reproduced below):



Belt further discloses:

The processor 11 and some other system components are of a type which use more power when running at a higher clock speed than when running at a lower clock speed. Therefore, clocks can be set to a **higher speed** when rapid processing is required despite the fact that a larger amount of power is drawn from the system battery during a given time period, whereas when processing speed is not critical a **lower clock speed** can be used in order to reduce the amount of power being drawn from the battery.

*Id.*, 3:5-14 (emphasis added); *see also id.*, 7:63-67 (main processor 11

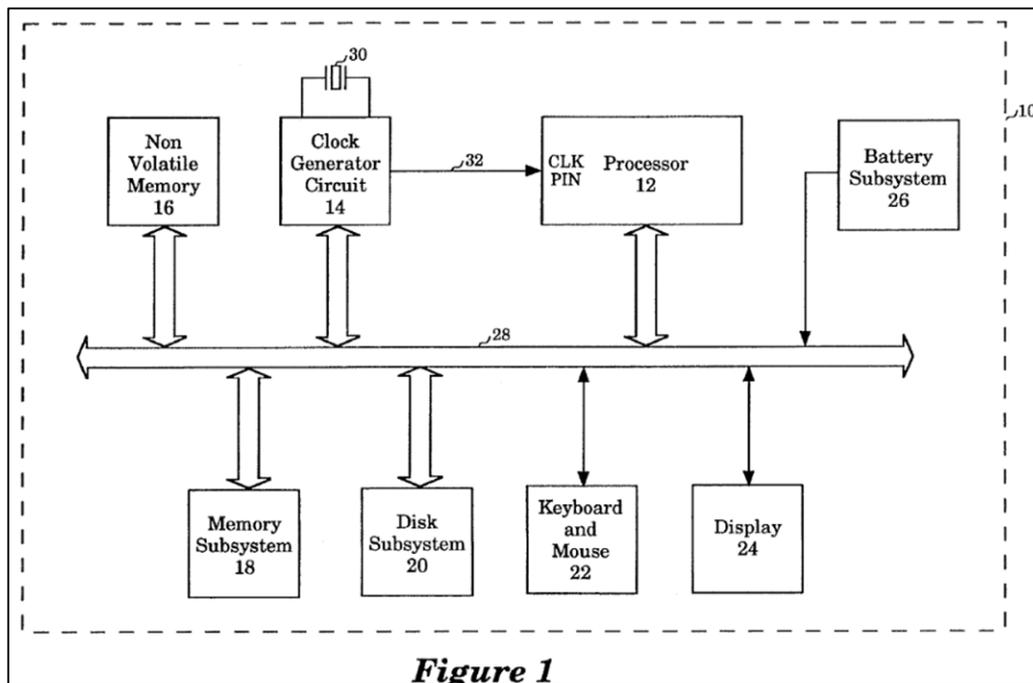
“unlocks configuration registers so that they can be altered, such as the control register 32 which can be used to change the speed of the clock.”),

7:67-8:2 (“the processor changes the register 32 in order to force the CPU to run at its fastest clock speed, so that the PMI routine will execute as fast as

possible.”), Fig. 4 (showing the clock signals exiting clock generator 31 and being fed (internally) to main processor 11 and (externally) to other components); EX1003, ¶¶64.

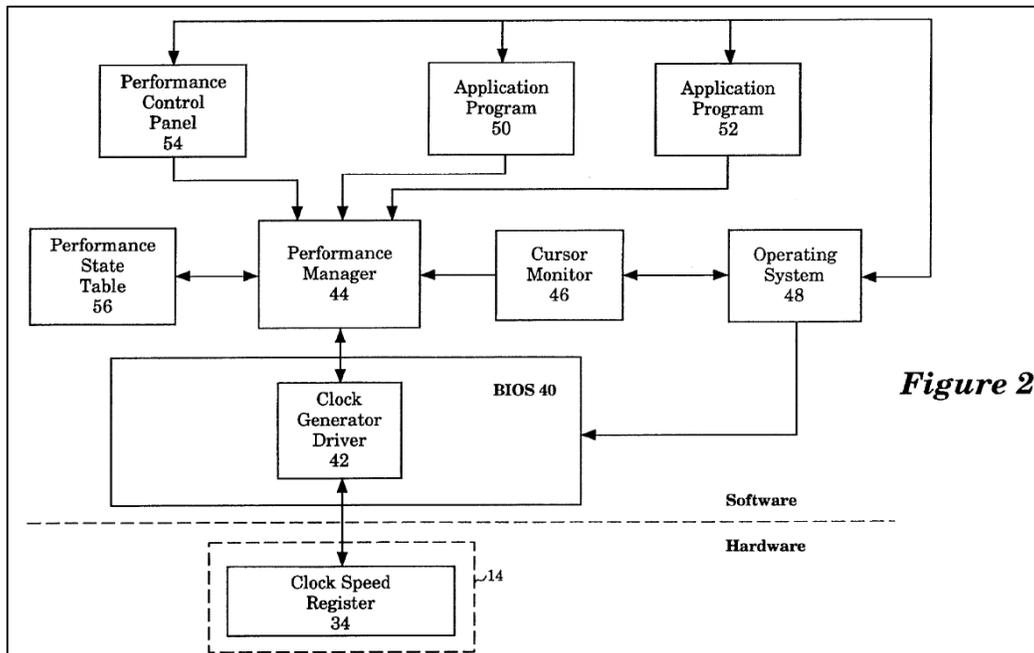
Notwithstanding Belt’s express disclosure, to the extent the Board interprets “to be fed” in a manner that requires the clock controller of claim 1 to be external to processor, the above disclosures of Belt, in view of Norris, renders such a configuration obvious. EX1003, ¶¶65-72.

Norris discloses “a computer system comprising a clock generator circuit having a clock speed register and circuitry for generating a processor clock signal at a frequency determined by the clock speed register.” EX1006, 2:43-58; *see also id.*, Abstract, 3:58-63 (“clock generator circuit 14 generates a processor clock 32 for the processor 12”), Fig. 1 (reproduced below).



**Figure 1**

Norris further discloses its computer system 10 also comprises “a performance manager 44” which is executable software that “processes requests from application programs 50 and 52 to change the performance state for the processor 12.” EX1006, 4:48-56, Fig. 2 (reproduced below):



Performance manager 44, in response to a request for the processor to enter either a high, medium, or low performance state, determines “the processor clock 32 frequencies that correspond to the high, medium and low performance states of the processor 12” and then “invokes the routines of the clock generator driver 42 to program the clock speed register 34 for the specified frequency of the processor clock 32.” *Id.*, 4:57-5:4.

It would have been obvious to a POSITA to combine the teachings of Belt and Norris to arrange Belt’s clock generator 31 and/or speed control register 32

outside of Belt's main processor 11, as taught by Norris, so that the clock signal generated by clock generator 31 is externally fed to the main processor 11.

EX1003, ¶¶69-72.

Belt and Norris are directed to the same field of endeavor and are analogous prior art to the '417 patent since each relates to power management techniques for portable computer systems that balance performance and battery life by dynamically adjusting a processor's clock speed. *See* EX1001, 1:32-40 ("if the CPU is driven at a high frequency, there has been a tendency toward an increase in current consumption although a processing speed is enhanced" which causes "risk of premature depletion of the battery capacity occurring when the clock signal has been automatically switched over to the high-speed side without knowledge of the user."); EX1004, 3:8-14 ("clocks can be set to a higher speed when rapid processing is required despite the fact that a larger amount of power is drawn from the system battery during a given time period, whereas when processing speed is not critical a lower clock speed can be used in order to reduce the amount of power being drawn from the battery."); EX1006, Abstract, 1:10-2:20 (explaining the problem in the art was that high clock speeds reduced battery life, but slow clock speeds degraded user performance), 2:25-27 ("One object of the present invention is manage a balance between performance and power consumption in a computer system.")

A POSITA would have understood the problem to be solved, namely, how to provide a variable frequency clock signal for a processor as disclosed in Belt for microprocessors that rely on external clock signals to operate. To overcome this problem, Norris discloses a computer system with clock generator circuit 14 that is external to the processor 12, wherein the clock signal 32 is fed (from the external source) to the processor 12. EX1006, 3:58-63, Fig. 1. Doing so reflects a design choice regarding whether the source of the clock signals is located in the processor or external to the processor. A POSITA would have been motivated to implement the solution of Norris in the Belt device so that the invention of Belt could be implemented using microprocessors that are designed to operate using clock signals that are externally fed to the processor. Indeed, because Belt teaches that its clock generator and speed control register not only respectively generates and controls a clock signal for the processor, but also for “various components of the system” (EX1004, 3:1-5), a POSITA would have found arranging the clock generator 31 and/or speed control register 32 outside the processor to be an obvious and necessary design choice when such components are not included within a processor. EX1003, ¶71.

A POSITA would have had a reasonable expectation of success in combining the teachings of Belt and Norris as both references disclose a computer architecture arrangement in which software, in conjunction, with a control register,

is capable of changing the frequency of the clock supplied to a processor. EX1003, ¶72. Implementing Norris’s teaching of an external (to the processor) control register and clock generator in Belt’s laptop computer system 10 involves modifications of only routine skill in the art. *Id.* Moreover, modifying Belt as described above would have involved known methods of chip design and therefore, would have yielded predictable results. *Id.*

#### 4. [1c]

Belt alone discloses or renders obvious, or in combination with Foster renders obvious, “wherein the clock controller controls the frequency of the clock signal so as to become a first frequency when the mobile terminal is in the open condition, and controls the frequency of the clock signal so as to become a second frequency lower than the first frequency when the mobile terminal is in the closed condition.” EX1003, ¶¶73-86.

Belt discloses its laptop computer system 10 has a lid which is movable between the open and closed positions. *See* §VI.A.1 (preamble). Lid switch 68 indicates whether the lid is open or closed, and sends an appropriate signal accordingly. EX1004, 5:7-9.

Belt discloses embodiments wherein the user can configure the system such that when the lid of laptop computer system 10 is closed, the system turns off the

backlight and/or produces an audible beep “without stopping the system from operating.” *Id.*, 6:42-50 (options 2 or 3):

“If it was determined at block 111 that the lid is closed, then control proceeds to block 121, where a check is made to determine what is to happen when the lid is closed. In particular, the user is allowed to configure the system set-up information to specify that a lid close is to (1) place the system in the suspend mode, (2) turn off the backlight without stopping the system from operating, or (3) produce an audible beep and turn off the backlight without stopping system operation.”

Belt’s disclosure of a scenario in which the lid of laptop computer system 10 is closed but the system continues operating alone teaches, or at least renders obvious, this limitation. Specifically, a POSITA would have understood that in this scenario, for system operations to continue, the processor would have an operating clock. EX1003, ¶76. Importantly, however, Belt teaches that it would be advantageous for battery performance for a processor to have a lower clock speed when processing speed is not critical. EX1004, 3:5-14. Accordingly, a POSITA would have further understood that when the lid to Belt’s laptop computer system 10 is closed, higher processing speeds are not critical because the system would not be in active use. EX1004, 1:17-21 (the keyboard and display of portable computer 10 are hidden when the lid is closed); EX1003, ¶76. Therefore, a POSITA would have also understood or at least found it obvious that when Belt’s laptop computer system 10 is closed, Belt’s clock controller (*see* limitation 1[b],

§VI.A.3) would control the frequency of the clock signal to main processor 11 to be a lower clock speed to increase battery performance as taught by Belt, relative to the clock speed when the lid is in the open position. EX1003, ¶77.

On the other hand, when the lid of Belt's laptop computer system 10 is open and the system is being used, Belt teaches it would then be advantageous for the processor to operate at higher clock speeds to rapidly process information.

EX1004, 3:5-14. Accordingly, a POSITA would have further understood or at least found it obvious that when the lid of Belt's laptop computer system 10 is open, Belt's clock controller (*see* limitation 1[b], §VI.A.3) would control the frequency of the clock signal to main processor 11 to be a higher clock speed (relative to the clock speed when the lid is closed) to rapidly process information as taught by Belt. *Id.*; EX1003, ¶78.

Additionally, the combination of Belt and Foster also renders this limitation obvious.

Belt discloses another embodiment wherein the user can configure the system such that when the lid of laptop computer system 10 is closed, the system is placed in a suspend mode. *Id.*, 6:42-50 (option 1):

“If it was determined at block 111 that the lid is closed, then control proceeds to block 121, where a check is made to determine what is to happen when the lid is closed. In particular, the user is allowed to configure the system set-up information to specify that a lid close is to (1) place the system in the suspend mode, (2) turn

off the backlight without stopping the system from operating, or (3) produce an audible beep and turn off the backlight without stopping system operation.”

Specifically, when Belt’s laptop computer system 10 has its lid open, it is in “a first operational mode in which the processor executes instructions” (i.e., the claimed “first frequency”) and in “respons[e] to movement of the lid to its closed position ... switching the processor to its second operation mode,” “in which the processor is halted in a reduced power state...”. EX1004, 1:64-2:9. This other operation mode is also referred to as a suspend mode, which involves “placing the main processor 11 in a low power mode in which its clock is turned off and program execution is halted” and “remains in this mode until an event occurs which is intended to cause it to resume operation”—e.g., “if the lid is opened, the lid switch 68 will, through the signal processing circuit 13, cause the resume control circuit 41 to produce a resume reset, which in turn causes the processor 11 to begin executing the reset handler routine of FIG. 7.” *Id.*, 10:58-68.

Foster discloses that in addition to a suspend mode—which is substantively similar, if not identical, to the suspend mode of Belt—the Intel 386SL processor may provide “an idle mode” in which “the CPU clock is slowed significantly” from 20 Mhz to 5Hz. *See* EX1005, 79:61-80:1; *compare id.*, with EX1005, 60:18-20 (disclosing stopping the processor’s clock in the suspend mode of Foster).

Foster discloses that the idle mode is much simpler than the suspend mode, and it

is possible to resume to run mode in a shorter time than required for the suspend mode. *Id.*, 80:7-9.

It would have been obvious to a POSITA to combine the teachings of Belt and Foster to modify Belt to enter, when the lid of laptop computer system 10 is closed, an idle mode such that a lower frequency clock signal (relative to the clock frequency when the lid is open) is fed to Belt's main processor. EX1003, ¶¶83-86.

Belt and Foster are directed to the same field of endeavor and are analogous prior art to the '417 patent since each relates to performance-based processor clocking power management techniques for portable computer systems. *See* §VI.A.3 (discussing the Belt and the '417 patent being analogous art); EX1005, 19:9-11 ("Power consumption within the processor 311 is dependent on its clock speed, and in particular is lower for lower clock speeds."), 28:11-18 ("In a situation where the user is operating on battery power and is running a program which does not require fast processor speed, intentionally reducing the processor speed will reduce power consumption and thus permit the user to operate the system longer before the battery requires recharging."). Notably, Belt incorporates

by reference U.S. App. No. 07/752,342, the application to which Foster claims priority as a continuation thereof. EX1004, 2:57-63; EX1005, 1:6-7.<sup>3</sup>

As set forth in Foster, a POSITA would have understood the problem of Belt's suspend mode was that it would take longer to exit from that suspend mode into a run mode, which would perceptibly degrade performance. EX1003, ¶85; *see also* EX1005, 79:61-80:17. To overcome this problem, Foster expressly discloses the solution of an "idle mode" in which "the CPU clock is slowed significantly" from 20 Mhz to 5Hz. *See* EX1005, 79:61-80:1. A POSITA would have been motivated to implement Foster's idle mode in lieu of Belt's suspend mode because, as disclosed in Foster, the idle mode "is much simpler than the suspend or standby modes" and doing so would make it "possible [for the computer system] to resume to run mode in a shorter time than required for the other modes." *Id.*, 79:61-80:17; EX1003, ¶85.

A POSITA would have had a reasonable expectation of success in making this modification since Belt and Foster's computer systems are substantively similar and each are based on the Intel 386SL. EX1003, ¶86. Implementing Foster's idle mode in lieu of Belt's suspend mode involves modifications of only

---

<sup>3</sup> Based on this incorporation by reference, Belt and Foster may be considered a single reference.

routine skill in the art. *Id.* Moreover, modifying Belt as described above would have involved known programming methods and therefore, would have yielded predictable results. *Id.*

**5. [1d]**

Belt alone discloses, or in combination with Foster renders obvious, “wherein the clock controller controls the frequency of the clock signal so as to become a frequency higher than the second frequency when a specific processing is executed (PMI Handler routine of Belt, or incoming call processing of Foster) even if the mobile terminal is in the closed condition, and controls the frequency of the clock signal so as to become the second frequency after the execution of the specific processing is completed.” EX1003, ¶¶87-94.

Belt alone discloses that when the lid is closed and laptop computer system 10 is in running at a low clock frequency (i.e., user configured operational closed-lid mode with lower clock frequency in Belt—see limitation 1[d], §VI.A.4), and a PMI interrupt occurs, processor 11 “automatically begins execution of the PMI handler routine.” EX1004, 7:46-55, Fig. 4. As part of this routine, “the processor changes the register 32 in order to force the CPU to run at its fastest clock speed, so that the PMI routine will execute as fast as possible” (i.e., “the clock controller controls the frequency of the clock signal so as to become a frequency higher than the second frequency when a specific processing is executed”). *Id.* 7:67-8:2. After

the PMI handler routine is completed, “the main processor restores to register 32 the clock speed which was in effect when the PMI occurred” (i.e. user configured operational closed-lid mode with lower clock frequency in Belt, or Belt’s suspend mode modified by Foster’s idle mode). *Id.*, 8:11-15. Therefore, Belt teaches controlling the frequency of the clock signal so as to become the second (lower) frequency after the execution of the specific processing is completed.

Additionally, the combination of Belt and Foster, wherein Belt’s suspend mode is implemented as Foster’s idle mode (*see* limitation 1[d], §VI.A.5), renders this limitation obvious. EX1003, ¶¶89-94.

Belt discloses that “if the system is in the suspend mode and the modem 22 receives an incoming telephone call, the modem ring indicator signal MDMRI on line 43 will cause the resume control circuit 41 to produce a resume reset,” but if it is determined that the lid is still closed, “the main processor 11 will return to the suspend mode.” EX1004, 11:14-28.

Foster, on the other hand, discloses that when its system is in suspend mode, its processor may “configure[] itself as to which interrupts will wake it up from the suspend mode” such as an “interrupt event from the serial or modem ports, as well as the power management interrupt from the system control processor SCP 316.” EX1005, 60:10-20. Upon receiving such interrupt, Foster discloses that the processor “must restore the main processor 311 to its normal mode of functioning

[(i.e., “the clock controller controls the frequency of the clock signal so as to become a frequency higher than the second frequency”)], or else incoming characters from a serial line or from a telephone lines may be lost” (the processing of incoming characters, i.e., “specific processing.”) *Id.* Once the incoming characters from the serial line or telephone line are processed, “[t]hen a command within a main processor 311 is executed so that it stops its CPU clock and enters suspend mode” (i.e., “and controls the frequency of the clock signal so as to become the second frequency after the execution of the specific processing is completed”). *Id.*

It would have been obvious to a POSITA to further combine the teachings of Belt and Foster to modify Belt’s incoming call procedure when the lid is closed with that of Foster’s so that the clock frequency of Belt’s main processor increases so that incoming characters from a serial line or from a telephone line can be processed and not lost. EX1003, ¶¶92-94.

Belt and Foster are analogous prior art to the ’417 patent for the reasons set forth in limitation 1[c], which are incorporated by reference herein. *See* §VI.A.4. A POSTIA would have understood that the problem with Belt’s closed-lid/suspend mode incoming call procedure is that the incoming call information will not be processed since the system remains in suspend mode. EX1005, 60:10-20; EX1003, ¶93. A POSITA would therefore have been motivated to implement Foster’s

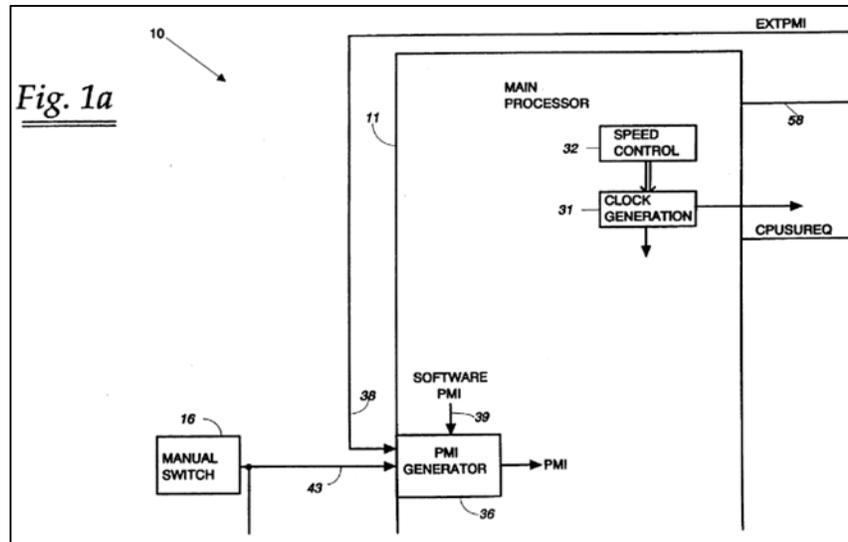
suspend mode incoming call procedure in Belt so that Belt's processor 11 is returned to "its normal mode of functioning" so that "incoming characters from a serial line or from a telephone lines [are not] lost" and after processing the call, returning to idle mode to further conserve battery. EX1005, 60:10-20; EX1003, ¶93.

And, for the reasons set forth in limitation 1[c], a POSITA would have had a reasonable expectation of success in combining the teachings of Belt and Foster as both references disclose substantively similar computer architectures, and both disclose an incoming call procedure as noted above. Modifying Belt's closed-lid/suspend mode incoming call procedure with Foster's suspend mode incoming call procedure would have involved known programming techniques and therefore, would have yielded predictable results. EX1003, ¶94.

**B. Claim 2**

Belt alone discloses, or in combination with Foster (with or without Norris) renders obvious, "the mobile terminal according to claim 1 (*see* claim 1— §§VI.A.1-5), wherein the specific processing (Belt's PMI handler routine, and Belt implementing Foster's hot key processing) is a processing having an effect on a response to a request from the user (a user actuating Belt's switch 16, and actuating on Belt's external keyboard Foster's hot key)" EX1003, ¶¶95-105.

Belt alone discloses that its laptop computer system 10 includes “a manually operable power control switch 16.” EX1004, 2:45-46, Fig. 1a (reproduced below).



Actuation of switch 16 (i.e., a request from the user) generates a PMI interrupt. *Id.*, 3:22-31. Belt discloses that when a PMI interrupt occurs from any source, the processor 11 “automatically begins execution of the PMI handler routine.” *Id.*, 7:46-55. The specific processing disclosed by Belt is its PMI handler routine. *See* limitation 1[d], §VI.A.5. Therefore, Belt’s PMI handler routine is a processing having an effect on a response to request from the user (actuation of switch 16) as recited in claim 2. EX1003, ¶¶96-97.

It should be noted that Belt discloses notebook computers at this time had a keyboard and display that were hidden and protected when the lid is in the closed position. EX1004, 1:15-21. However, Belt does not disclose hiding its power switch 16 in the closed position. Therefore, a POSITA would have understood the

power switch 16 could be actuated when the computer is in the closed position.

EX1003, ¶98.

Additionally, Belt and Foster each disclose that their respective laptop computer systems can be connected to an external keyboard, mouse, and display.

EX1004, 4:57-64, Fig. 1b; EX1005, 20:49-58, Fig. 13b.

Foster discloses that “[w]hen the processor detects one of several special multi-key combinations [from the internal keyboard], it actuates the EXTPMI line to the main processor,” (i.e., “a request from the user”) which initiates a PMI, “so that any program in progress is immediately interrupted, a special function is carried out” (i.e., “the specific processing). *See* EX1005, 27:61-28:10, 39:63-66 (“a HK bit which indicates that a hot key multi-key combination has been pressed on the keyboard and was the reason for the PMI.”).

With respect to an external keyboard, although Foster discloses that “[h]ot keys are recognized only for the internal keyboard and not an external keyboard” and that “[i]f a hot key actuation were received from an external keyboard, it *could* be discarded” (EX1005, 41:60-63), a POSITA would have understood that the external keyboard hot key could also not be discarded, which would be advantageous when the external keyboard is primarily being used. EX1003, ¶101. Indeed, Foster discloses that an external keyboard or mouse can send information to the SCP such that it “executes the interrupt service routine shown in Fig. 30.”

EX1005, 41:44-48, 42:1-9 (recognizing external mouse actuation), 71:43-67

(external keyboard interrupt handler routine).

As explained previously, Belt and Foster are each analogous art to the '417 patent. *See* limitation 1[b], §VI.A.3 (describing analogousness of Belt and the '417 patent), limitation 1[c], §VI.A.4 (same re Belt, Foster, and the '417 patent).

A POSITA would have understood the problem involved, namely, the need to allow the user of the Belt device the ability to change the clock frequency when desired—including when an external keyboard is primarily being used. To overcome this problem, Foster discloses the solution of providing various mechanisms for the user to change the clock frequency as desired. A POSITA would have been motivated to implement in Belt's laptop computer system 10 of the Belt-Foster combination (with or without Norris) Foster's hot key processor speed setting which advantageously allows a user to selectively prioritize "maximum performance" to rapidly execute "processor intensive functions [] being performed" or "maximum power conservation" when the device is running on battery to prolong operational usability, or "balance between" the two. EX1005, 28:13-18 ("intentionally reducing the processor speed will reduce power consumption and thus permit[s] the user to operate the system longer"); EX1003, ¶¶102-103.

The modification to Belt could be implemented, for example, by adding Foster's hot key processor speed setting to Belt's PMI handler routine, whereby the hot key is entered through an external keyboard as taught, and rendered obvious, by Foster as described above. Indeed, as Belt discloses, the user can configure the laptop computer system 10 to remain in operation even when the lid is closed. *See* limitation 1[c], §VI.A.4. Therefore, when the lid of laptop computer system 10 is closed, but the system remains operational and connected to an external keyboard, mouse, and display, a POSITA would have understood that the user may still use laptop computer system 10 in a conventional matter via these external peripherals and, in doing so, desire to increase or decrease the processing speed depending on the situation. EX1003, ¶104.

Regarding the implementation of Foster's hot key processor speed setting in Belt's laptop computer system 10, for the reasons set forth in limitation 1[c] (§VI.A.4), a POSITA would have had a reasonable expectation of success in combining the teachings of Belt and Foster as both references disclose substantively similar computer architectures, and both disclose an EXTPMI as noted above. Implementing Foster's hot key processor speed setting in Belt's laptop computer system 10 would have involved known programming techniques and therefore, would have yielded predictable results. EX1003, ¶105.

**C. Claim 4**

**1. [4a]**

Belt in combination with Foster or Norris renders obvious “the mobile terminal according to claim 1 (*see* claim 1—§§VI.A.1-5), further comprising an input unit (Belt’s laptop computer system implementing Foster’s hot key functionality, or Norris’s performance control panel 54 and control panel 70, or in-BIOS performance state table 56) which allows a user of the mobile terminal to set the frequency of the clock signal.” EX1003, ¶¶106-116.

Belt discloses laptop computer system 10 includes a “[BIOS] program.” EX1004, 5:45-46. Belt further discloses a “power management interrupt (PMI) generator 36, which generates a special PMI interrupt in response to several conditions,” including an external PMI (EXT PMI) from an external source. EX1004, 3:22-28. In the event of a PMI, “the processor sets up a special stack for use by the PMI handler, and unlocks configuration registers so that they can be altered, such as the control register 32 which can be used to change the speed of the clock.” *Id.*, 7:64-67.

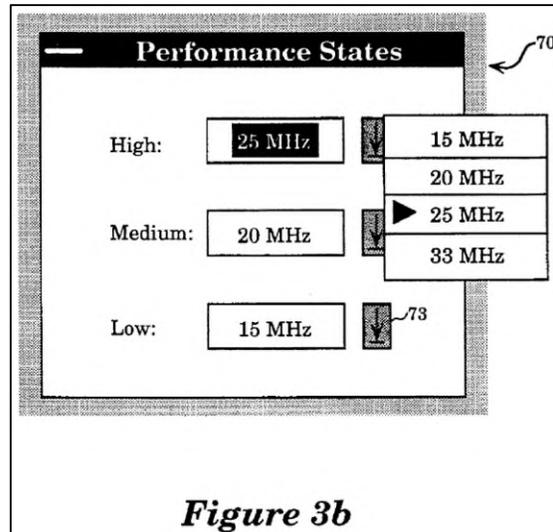
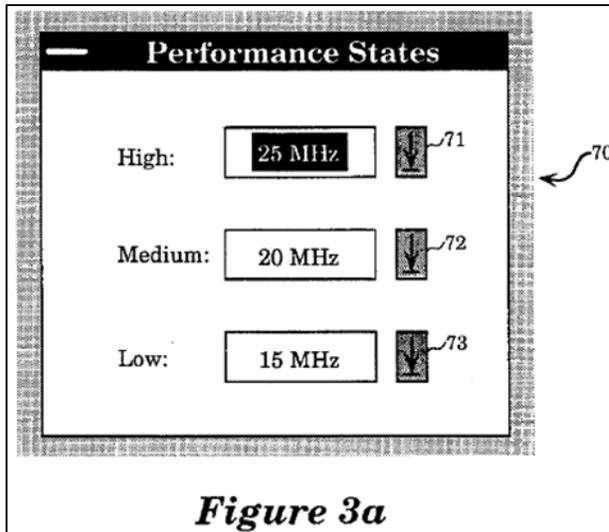
Foster discloses that “[w]hen the processor detects one of several special multi-key combinations, it actuates the EXTPMI line to the main processor,” which initiates a PMI, “so that any program in progress is immediately interrupted, a special function is carried out[.]” *See* EX1005, 27:61-28:10, 39:63-66 (“a HK bit

which indicates that hot key multi-key combination has been pressed on the keyboard and was the reason for the PMI.”). As part of this PMI routine, “processor 311 unlocks certain internal configuration registers so that they can be altered, such as the control register 388 which can be used to change the speed of the CPU clock.” *Id.*, 23:23-26. Foster further discloses that certain special multi-key combinations, which are input by a user via a keyboard and initiates a PMI via an EXTPMI line, indicates that the special function to be carried out is either to have the “CPU to run at a slow clock speed,” or at a “fast processor speed.” *Id.*, 28:11-13 (hot key for slow clock speed), 28:29-36 (hot key for fast clock speed).

Norris discloses in one embodiment a “performance control panel 54 is an application program that enables a user of the computer system 10 to select from a set of predetermined frequencies of the processor clock 32 that correspond to the high, medium, and low performance states of the processor 12. The performance control panel 54 employs the display and interactive input functions provided by the operating system 48 to generate the control panel 70 and to enter the processor clock frequencies.” EX1006, 5:30-37; *id.*, 5:56-59 (“The user employs a set of pulldown menu areas ... to select a desired processor clock 32 frequency for each” [of the performance states]”).

Norris further discloses that after a user selects the frequency for the high, medium, low performance states, the “performance control panel 54 transfers the

clock speeds selected through the control panel 70 to the performance manager 44”  
which, in turn, “stores the selected clock frequencies for the high, medium, and



low performance states in the performance state table 56” and “then uses the clock generator driver 42 to write the appropriate value into the clock speed register 34 to set the selected processor clock 32 frequency.” EX1006, 6:5-16; Figs. 3a, 3b (reproduced below).

In another embodiment, Norris discloses that “the clock speeds for the performance state table 56 are selected by a clock speed function in the BIOS 40 that enables user selections of clock speeds via command input.” *Id.*, 6:17-20.

It would have been obvious to a POSITA to combine the teachings of Belt and Foster or Norris to implement in the Belt-Foster or Belt-Norris combination either Foster’s hot key processor speed setting technique or Norris’s performance control panels 54 and 70 or user selectable in-BIOS performance state table 56

such that a user can manually set the frequency of the clock signal fed to main processor 11 to increase battery life or performance as desired. EX1003, ¶112.

As explained previously, Belt, Foster, and Norris are each analogous art to the '417 patent. *See* limitation 1[b], §VI.A.3 (describing analogousness of Belt, Norris, and the '417 patent), limitation 1[c], §VI.A.4 (same re Belt, Foster, and the '417 patent).

A POSITA would have understood the problem involved, namely, the need to allow the user of the Belt device the ability to change the clock frequency when desired. To overcome this problem, Foster and Norris disclose the solution of providing various mechanisms for the user to change the clock frequency as desired. A POSITA would have been motivated to implement in Belt's laptop computer system 10 either Foster's hot key processor speed setting technique or Norris's performance control panel as each advantageously allows a user to selectively prioritize "maximum performance" to rapidly execute "processor intensive functions [] being performed" or "maximum power conservation" when the device is running on battery to prolong operational usability, or "balance between" the two. EX1006, 5:60-7:4 (allowing a user to select maximum performance, maximum power conservation, or balance between them, as desired), EX1005, 28:13-18 ("intentionally reducing the processor speed will reduce power

consumption and thus permit[s] the user to operate the system longer”). EX1003, ¶114.

Regarding the Belt-Foster combination, for the reasons set forth in limitation 1[c], a POSITA would have had a reasonable expectation of success in combining the teachings of Belt and Foster as both references disclose substantively similar computer architectures, and both disclose an EXTPMI as noted above. Implementing Foster’s hot key processor speed setting in Belt’s laptop computer system 10 would have involved known programming techniques and therefore, would have yielded predictable results. EX1003, ¶115.

Regarding the Belt-Norris combination, for the reasons set forth in limitation 1[b], a POSITA would have had a reasonable expectation of success in combining the teachings of Belt and Norris as both references disclose similar implementations for changing the clock frequency (through a control register), and both disclose a BIOS as noted above. Implementing Norris’s performance control panel 54 or user selectable in-BIOS performance state table 56 in Belt’s laptop computer system 10 would have involved known programming techniques and therefore, would have yielded predictable results. EX1003, ¶116.

## 2. [4b]

Belt in combination with Foster or Norris renders obvious “wherein when the frequency is set by the user using the input unit (*see* limitation 4[a] —

§§VI.C.1-2), the first frequency is the frequency set by the user using the input unit.” EX1003, ¶¶117-124.

Petitioner incorporates by reference the discussion of the disclosures in Belt, Foster, and Norris in limitation 4[a] is if fully set forth herein. *See* limitation 4[a].

As explained in limitation 1[c] (§VI.A.4), Belt discloses main processor 11 operates at higher clock speeds (the first frequency) to rapidly process information. EX1004, 3:5-14.

Foster discloses that a user can input a hot key combination to set the main processor 11 to have a “fast processor speed.” EX1005, 28:29-36.

Norris discloses that a user sets, among other performance states, the high performance state for the processor 12 via control panel 70 generated by performance control panel 54. EX1006, 5:30-37; *id.*, 5:56-59. Norris further discloses that “[i]f maximum performance for the processor 12 is always desired, then the user selects the fastest processor clock 32 frequency for the high, medium, and low processor states of the processor 12.” *Id.*, 5:60-63.

As explained in limitation 4[a], it would have been obvious to a POSITA to combine the teachings of Belt and Foster or Norris. The same reasoning applies to the limitation 4[b]. EX1003, ¶¶112-116, 122.

Accordingly, in the Belt-Foster combination, in implementing in Belt’s laptop computer system 10 Foster’s hot key technique in which a user sets main

processor 11 to have a fast processor speed, a POSITA would have understood that “fast processor speed” is Belt’s first (i.e., higher) frequency. *See* limitation 1[c], §VI.A.4; EX1003, ¶123.

In the Belt-Norris combination, in implementing in Belt’s laptop computer system 10 Norris’s performance control panel 54 or user selectable in-BIOS performance state table 56 in which a user sets main processor 11 to set a frequency for a high performance state or the fastest processor clock 32 frequency for each performance state, as taught by Norris, a POSITA would have understood that “high performance state” or the fastest processor clock 32 frequency is Belt’s first (i.e., higher) frequency. *See* limitation 1[c], §VI.A.4; EX1003, ¶124.

**D. Claim 5**

The Belt and Norris combination renders obvious “the mobile terminal according to claim 4 (*see* claim 4—§§VI.C.1-2), wherein the user can set the frequency of the clock signal in every processing using the input unit.” EX1003, ¶¶125-130.

As set forth in claim limitation [4a], Norris discloses that after a user selects the frequency for the high, medium, low performance states, the “performance control panel 54 transfers the clock speeds selected through the control panel 70 to the performance manager 44” which, in turn, “stores the selected clock frequencies for the high, medium, and low performance states in the performance state table

56” and “then uses the clock generator driver 42 to write the appropriate value into the clock speed register 34 to set the selected processor clock 32 frequency.”

EX1006, 6:5-16; Figs. 3a, 3b (reproduced below).

In another embodiment, Norris discloses that “the clock speeds for the performance state table 56 are selected by a clock speed function in the BIOS 40 that enables user selections of clock speeds via command input.” *Id.*, 6:17-20.

As set forth in claim limitation [4b], Norris discloses, without limitation, that “[i]f maximum performance for the processor 12 is always desired, then the user selects the fastest processor clock 32 frequency for the high, medium, and low processor states of the processor 12.” EX1006, 5:60-63.

As explained in limitation 4[a], it would have been obvious to a POSITA to combine the teachings of Belt and Norris to allow the user to set the frequency of the clock signal (using Norris’ performance control panel 54 or clock speed function in the BIOS 40). The same reasoning applies to claim 5, where the user is setting the frequency of the clock signal for every processing using the input unit so that maximum performance can be achieved when desired as taught by Norris. *Id.*; EX1003, ¶¶112-116, 129.

Accordingly, in the Belt-Norris combination wherein a user selects maximum performance for processor 12 is always desired, as taught by Norris, a POSITA would have therefore understood that all—and so, *every*—processing by

processor 12 would be processed at the fastest processor clock 32 frequency.

EX1003, ¶130.

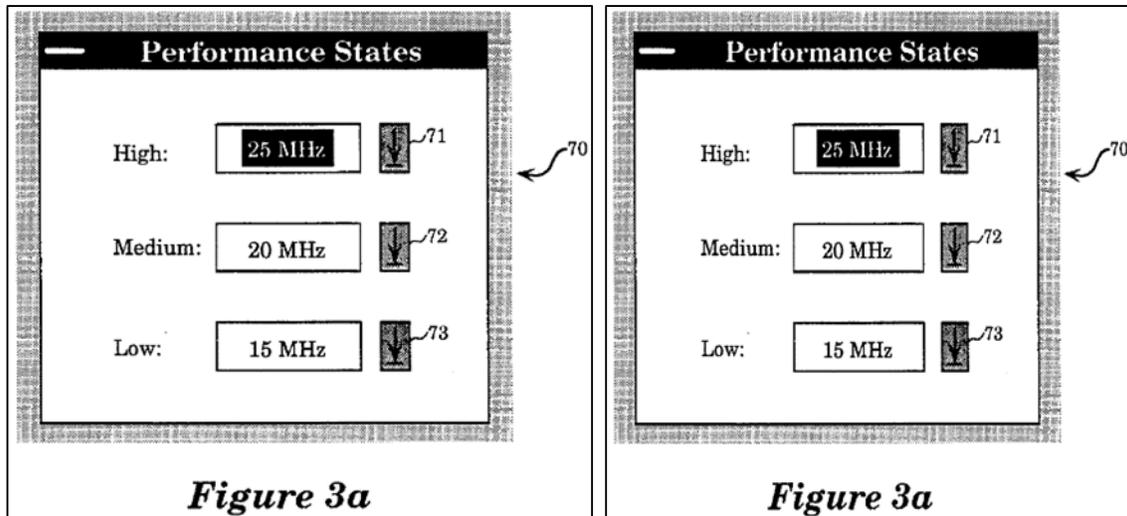
**E. Claim 6**

The Belt-Norris combination renders obvious “the mobile terminal according to claim 1 (*see* claim 1—§§VI.A.1-5), further comprising a display which exhibits a display corresponding to the magnitude of the frequency of the clock signal (Belt’s laptop computer system 10 implementing Norris’s performance control manager 54 and control panel 70).” EX1003, ¶¶131-136.

Belt discloses that laptop computer system 10 includes a “display.” EX1004, 2:48-50, 4:67-5:2.

Norris discloses that “performance control panel 54 employs *the display and interactive input functions provided by the operating system 48 to generate the control panel 70* and to enter the processor clock frequencies.” EX1006, 5:30-37 (emphasis added); *id.*, 5:56-59 (“The user employs a set of pulldown menu

areas ... to select a desired processor clock 32 frequency for each” [of the performance states]”), Figs. 3a & 3b (reproduced below).



As shown above in Figures 3a and 3b the control panel 70 displays information “corresponding to the magnitude of the frequency of the clock signal” grammatically (as “high,” “medium,” or low”) and numerically (respectively, in Fig. 3a, e.g., 25MHz, 20Mhz, and 15Mhz). Figs. 3a & 3b; EX1003, ¶¶133-134.

As explained in limitation 4[a], it would have been obvious to a POSITA to combine the teachings of Belt and Norris to allow the user to set the frequency of the clock signal. The same reasoning applies to claim 6, where a display provides the user with a GUI that facilitates the setting of the frequency of the clock signal for the performance states using the input unit so that the desired frequency for each performance state could be set as taught by Norris. *Id.*; EX1003, ¶¶112-116, 135.

Accordingly, in the Belt-Norris combination in implementing Norris's performance control manager 54 in Belt's laptop computer system 10, performance control manager 54 would cause Belt's display to display control panel 70, as taught by Norris. EX1003, ¶136.

**F. Claim 7**

Belt discloses “the mobile terminal according to claim 1 (*see* claim 1—§§VI.A.1-5), wherein the mobile terminal has a folded structure.” EX1003, ¶¶137-138.

*See* claim 1[pre] (§ VI.A.1); EX1004, 1:64-67; *see also id.*, 1:13-17 (“Portable computers of the type commonly referred to as ‘laptop’ computers and ‘notebook’ computers are becoming very popular [and] [t]hey typically include a housing with a lid which is movable between open and closed positions[.]”).

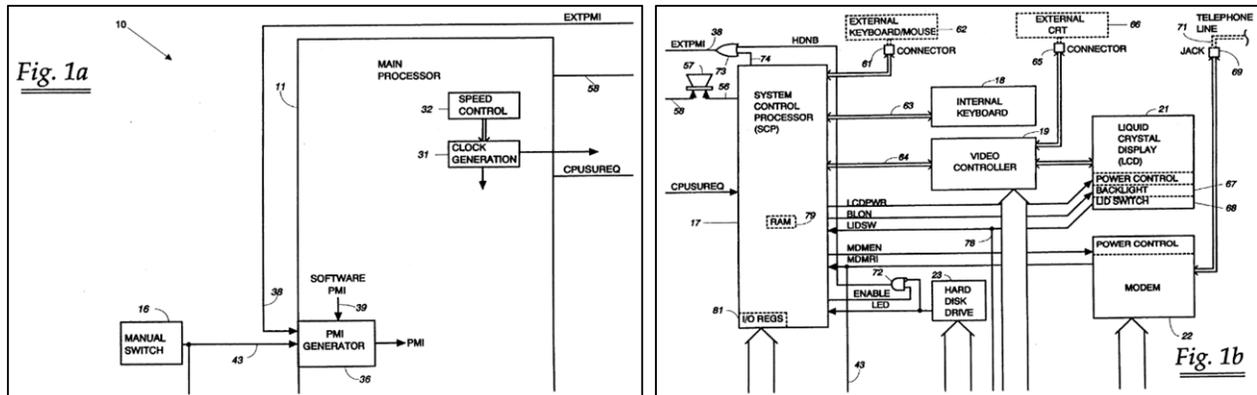
**VII. GROUND 2: CLAIM 3 IS RENDERED OBVIOUS BY BELT, FOSTER, NORRIS AND ALBERTH**

**A. Claim 3**

The Belt, Foster, Norris and Alberth combination renders obvious “the mobile terminal according to claim 1 (*see* claim 1—§§VI.A.1-5), wherein the specific processing is an image decoding processing or an address retrieval processing or a character conversion processing.” EX1003, ¶¶139-150.

Belt discloses a speaker 57 that produces an audible beep in response to “a signal produced by the main processor 11 on a line 58.” EX1004, 4:44-46; *see also*

*id.*, Figs. 1a (line 58 connected to main processor 11), Fig. 1b (line 58 connected to speaker 57). Figs. 1a and 1b are reproduced below:



Belt further discloses that “if the system is in the suspend mode and the modem 22 receives an incoming telephone call, the modem ring indicator signal MDMRI on line 43 will cause the resume control circuit 41 to produce a resume reset,” but if it is determined that “the lid is still closed[,]” “the main processor 11 will return to the suspend mode.” *Id.*, 11:14-28.

Foster discloses that a conventional modem contains, for example, “user data stored within EEPROMs 4012.” EX1005, 75:67-76:2. Foster further discloses that “when the modem is [woken] up...the modem is fully programmed to continue normal operation and to respond to an incoming telephone call ... in accordance with the configuration programmed into the modem 332 by whatever program is running within the main processor 311.” *Id.*, 77:65-78:4. In one such example, Foster discloses that the modem is programmed, in part, to “come up

with the speaker turned on so that any dialing noises are presented in the speaker of the computer.” *Id.*, 78:4-9.

As discussed in limitation 1[d] (*see* §VI.A.5), in the Belt-Foster combination, it would have been obvious to modify Belt’s modem with the teachings of Foster’s modem such that modem 22 of Belt’s laptop computer system 10 processes incoming characters from a serial line or from a telephone line even when the lid of Belt’s laptop computer system 10 is closed.

Alberth, however, discloses “a closeable communication device 102 [that] has housing portions 110 and 112” that are moveable between an open position and a closed position. EX1007, 2:54-62; *id.*, 2:63-3:3; *see also id.*, 2:48-53 (“Although illustrated in a cellular telephone, the apparatus and method described hereinbelow will also find application in cordless telephones, two-way radios, pagers, personal digital assistants, and the like, and ‘device’ as used herein shall refer to each of these and their equivalents.”). Alberth further discloses that the closeable communication device 102 further includes “memory 305 [which] permanently stores operating instructions and user definable information, such as caller information in the form of an electronic phone book of names and associated telephone numbers[.]” *Id.*, 4:55-58; *id.*, 4:62-65 (memory 305 may include EEPROM).

Alberth further discloses a “smart call indication” technique in which a controller—which “includes a microprocessor (not shown) for executing the operational instructions [and] processing the aforementioned received signals” (5:3-6)—“retrieves the caller identification information of the incoming call ... and compares the caller identification information to caller information, such as telephone numbers, stored in the memory 305[.]” *Id.*, 7:12-18. “If a match between the caller identification information and the stored caller information is found,” an indication corresponding to a found match is produced. *Id.*, 7:18-21. If no match is found, a corresponding indication is produced. *Id.*, 7:27-30. Alberth discloses that these indications may be a ringer “emitting distinctive tones” for the match found and match not found determinations. *Id.*, 7:34-39; *id.*, 8:53-56 (“The smart call feature embodied in steps 402, 424, 430, 432, 434, 436, 438, and 440 of the method of FIG. 4 provides a user with incoming call information when the housing 105 is in the closed position”).

A POSITA would have understood that Alberth’s “smart call indication,” also referred to as caller ID, is within the scope of “address retrieval”<sup>4</sup> in view of the cellular phone embodiment of the ’417 patent. EX1003, ¶146.

---

<sup>4</sup> The phrase “address retrieval” appears only once in the ’417 patent at 2:65-3:2 and merely mirrors the language in the claim.

As explained previously, Belt, Foster, and Norris are each analogous art to the '417 patent. *See* limitation 1[b], §VI.A.3 (describing analogousness of Belt, Norris, and the '417 patent), limitation 1[c], §VI.A.4 (same re Belt, Foster, and the '417 patent). Alberth is also analogous to the '417 patent because Alberth is directed to “a closeable communication device and method of operating the same that increases the usability of the device in the closed position by, for example, supporting desirable user features and minimizing power consumption.” EX1007, 1:63-67, EX1003, ¶147.

A POSITA would have understood the problem involved, namely, the need to allow the user of the Belt device the ability to determine when a known caller is calling Belt's device, even when in a closed condition. EX1003, ¶148. A POSITA would have been motivated to implement, in Belt's laptop computer system 10 in the Belt-Foster-Norris combination, Alberth's smart call indication technique to allow a user to identify, when a device is in a closed position, whether an incoming call is from a known caller. EX1007, 9:6-9 (“This allows the user to view caller identification information of the incoming call on the display 134 of the device 102, which is hidden in the closed position 200[.]”); EX1003, ¶148. Further, because neither Belt nor Foster teach specifically how an incoming call is processed (EX1005, 77:65-78:4), a POSITA would have turned to art related to processing incoming calls, like that of Alberth, for such specifics. EX1003, ¶148.

The modification to Belt could be implemented, for example, by causing Belt's speaker 57 to output a sound, as described in Norris, corresponding to a caller's phone number matching that stored in memory, as taught by Alberth. EX1007, 7:34-39; EX1003, ¶149.

A POSITA would have had a reasonable expectation of success in making this modification since, as noted above, Belt's modem, in view of Foster's teachings of the same, includes components and functionality similar to those described in Alberth (EEPROM memory for storing user data and incoming call processing performed by a processor). EX1003, ¶150. Implementing Alberth's smart call indication techniques involve modifications of only routine skill in the art. *Id.* Moreover, implementing Alberth's smart call indication techniques in the Belt-Foster-Norris combination as described above would have involved known programming methods and therefore, would have yielded predictable results. *Id.*

### **VIII. DISCRETIONARY DENIAL IS NOT WARRANTED**

Pursuant to Acting Director Coke M. Stewart's March 26, 2025, Memorandum regarding Interim Processes for PTAB Workload Management, Petitioner understands that discretionary denial issues if any will be raised in a separate brief to be filed by Patent Owner. If Patent Owner files such a brief, Petitioner intends to respond in an opposition brief consistent with Acting Director Coke M. Stewart's March 26, 2025, Memorandum regarding Interim Processes for

PTAB Workload Management. Accordingly, Petitioner will not address discretionary denial issues in this Petition.

**IX. MANDATORY NOTICES UNDER 37 C.F.R. §§ 42.8(B)(1)-(4)**

**A. Real Party-In-Interest**

Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. are the real parties-in-interest.

**B. Related Matters**

The '417 patent is subject to the following actions: *Maxell, Ltd. v. Samsung Electronics Co., Ltd.*, Case No. 5-25-CV-00052 (E.D. Tex.).

**C. Lead and Backup Counsel**

<b>Lead Counsel</b>	<b>Backup Counsel</b>
Alan A. Limbach Reg. No. 39749 DLA Piper LLP (US) 3203 Hanover Street, Suite 100 Palo Alto, CA 94304-1123 Phone: + 1 650 833 2433 Fax: + 1 650 687 1182 Alan.Limbach@us.dlapiper.com	Chris Katsantonis Reg. No. 78,388 DLA Piper LLP (US) 444 West Lake Street, Suite 900 Chicago, IL 60606 Phone: 312.368.2127 Fax: 312.251.5727 chris.katsantonis@dlapiper.com

**D. Service Information**

Service information for lead and backup counsel is provided in the designation of lead and backup counsel above. Petitioner consents to electronic service to lead and back-up counsel and to: DLA-Maxell-2-IPRs@us.dlapiper.com

**X. CONCLUSION**

All Challenged Claims of the '417 patent should be found unpatentable for the reasons discussed in this Petition.

Respectfully submitted,

*/Alan A. Limbach/*

Alan A. Limbach

Reg. No. 39,749

DLA Piper LLP (US)

3203 Hanover Street, Suite 100

Palo Alto, CA 94304-1123

Phone: + 1 650 833 2433

Fax: + 1 650 687 1182

Alan.Limbach@us.dlapiper.com

*Attorney for Petitioners*

**CERTIFICATE OF WORD COUNT**

Pursuant to 37 C.F.R. § 42.24(d), Petitioner certifies that this petition includes 8,898 words, as measured by Microsoft Word, exclusive of the table of contents, mandatory notices under § 42.8, certificates of service, word count, claim listing, and exhibits.

Date: August 28, 2025

*/Alan A. Limbach/*

Alan A. Limbach

Reg. No. 39,749

DLA Piper LLP (US)

3203 Hanover Street, Suite 100

Palo Alto, CA 94304-1123

Phone: + 1 650 833 2433

Fax: + 1 650 687 1182

Alan.Limbach@us.dlapiper.com

*Attorney for Petitioners*

**CERTIFICATE OF SERVICE**

The undersigned certifies pursuant to 37 C.F.R. §§ 42.6(e) and 42.105 that on August 28, 2025, a true and correct copy of the Petition for *Inter Partes* Review of U.S. Patent No. 7,577,417 was served was served by emailing a copy of the same (by agreement) to the following attorneys for the Patent Owner:

Robert G. Pluta – rpluta@mayerbrown.com

Saqib Siddiqui – ssiddiqui@mayerbrown.com

A courtesy copy was sent to the counsel below via electronic mail:

maxell-samsung-service@mayerbrown.com

Respectfully submitted,

/Alan A. Limbach/

Alan A. Limbach

Reg. No. 39,749

DLA Piper LLP (US)

3203 Hanover Street, Suite 100

Palo Alto, CA 94304-1123

Phone: + 1 650 833 2433

Fax: + 1 650 687 1182

Alan.Limbach@us.dlapiper.com

*Attorney for Petitioners*