IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Tuominen et al.	
U.S. Patent No.:	7,609,527	Attorney Docket No. 50095-0191IP1
Issue Date:	October 27, 2009	
Appl. Serial No.:	11/907,795	
Filing Date:	October 17, 2007	
Title:	ELECTRONIC MODULE	

DECLARATION OF DR. R. JACOB BAKER

I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Dated: 2/5/2025 By: _____
R. JACOB BAKER, PH.D., P.E.

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I, R. Jacob Baker, Ph.D., P.E., do hereby declare:

1. I have been engaged by Fish & Richardson P.C. ("Fish") on behalf of Apple, Inc. ("Apple" or "Petitioner") to provide my independent analysis of issues relating to the patentability of claims of U.S. Patent No. 7,609,527.

2. I am being compensated for my work in this matter at my standard hourly rate for consulting services. My compensation in no way depends on the outcome of this proceeding or the content of my testimony.

I. MATERIALS CONSIDERED

3. In preparing this Declaration, I considered the following materials:

- U.S. Patent No. 7,609,527 (APPLE-1001), and its accompanying prosecution history (APPLE-1002)
- U.S. Patent No. 5,616,520 to Nishiuma et al. ("Nishiuma") (APPLE-1004)
- U.S. Publication No. 2002/0149117 to Shibata et al. ("Shibata") (APPLE-1005)
- U.S. Publication No. 2002/0159242 to Nakatani et al. ("Nakatani") (APPLE-1007)
- Japanese Patent Publication No. 2001-085473 to Onda with Certified Translation ("Onda") (APPLE-1008)

- Japanese Patent Publication No. 11-191574 to Matsuda with Certified Translation ("Matsuda") (APPLE-1009)
- U.S. Patent No. 4,912,844 to Parker ("Parker") (APPLE-1010)
- U.S. Publication No. 2003/0034557 to Gupta et al. ("Gupta") (APPLE-1011)
- Japanese Patent Publication No. 2002-280713 to Yoneyama with Certified Translation ("Yoneyama") (APPLE-1013)
- U.S. Patent No. 5,719,438 to Beilstein et al. ("Beilstein") (APPLE-1014)
- U.S. Patent No. 5,866,942 to Suzuki et al. ("Suzuki") (APPLE-1015)
- U.S. Publication No. 2004/0007774 to Crane et al. ("Crane") (APPLE-1016)
- U.S. Patent No. 4,774,633 to Dehaine et al. ("Dehaine") (APPLE-1017)
- U.S. Patent No. 7,297,572 to Salmon ("Salmon") (APPLE-1018)
- U.S. Publication No. 2003/0047806 to Stelzl et al. ("Stelzl") (APPLE-1019)
- U.S. Patent No. 4,068,022 to Glick ("Glick") (APPLE-1020)
- J.A. Scarlett, *The Multilayer Printed Circuit Board Handbook*, Electrochemical Publications Limited, 8 Barns Street, Ayr Scotland © 1985 (APPLE-1021)

- J.A. Scarlett, *An Introduction to Printed Circuit Board Technology*, Electrochemical Publication Limited, 8 Barns Street, Ayr Scotland © 1984 (APPLE-1022)
- U.S. Publication No. 2003/0090883 to Asahi ("Asahi") (APPLE-1025)
- Rudolf F. Graf, *Modern Dictionary of Electronics*, Newnes, 7th ed. © 1999 (APPLE-1031)
- Alan Freedman, *Computer Desktop Encyclopedia*, Osborne/McGraw-Hill, 9th ed. © 2001 (APPLE-1032)
- Frank Hargrave, *Hargrave's Communications Dictionary*, IEEE Press © 2001 (APPLE-1033)
- William D. Callister, Jr., Materials Science and Engineering: An Introduction, 5th Ed., John Wiley & Sons, Inc. © 2000 (APPLE-1035)
- Simon Thomas, *3D-Integration: Trends and Opportunities – An Overview* (Materials Research Society 2003) (APPLE-1036)
- R. Kujala, et. al., *Solderless Interconnection and Packaging Technique for Embedded Active Components* (IEEE 1999) (APPLE-1037)
- U.S. Patent Publication No. 2001/0026010 to Horiuchi ("Horiuchi") (APPLE-1038)

- U.S. Patent No. 6,038,133 to Nakatani et al. ("Nakatani-II") (APPLE-1039)
- U.S. Patent No. 5,250,843 to Eichelberger ("Eichelberger") (APPLE-1040)
- International Patent Application WO1996012296 to Suwa et al. and Certified Translation ("Suwa") (APPLE-1041)
- Japanese Patent Application No. 2002-83926 to Enomoto et al. and Certified Translation ("Enomoto") (APPLE-1042)
- European Patent Publication No. EP1069616 to Kurita ("Kurita") (APPLE-1043)
- Exhibit 10 to Complaint for Patent Infringement – Infringement Claim Chart for '527 Patent (February 5, 2024), Case No. 1-24-cv-00129 (WDTX), Document 1-10 (APPLE-1105)

II. QUALIFICATIONS AND BACKGROUND

4. I am currently a Professor Emeritus of Electrical and Computer Engineering at the University of Nevada, Las Vegas (UNLV). My curriculum vitae is provided (as Appendix A).

5. I have been teaching electrical engineering at UNLV since 2012. Prior to this position, I was a Professor of Electrical and Computer Engineering at Boise

State University from 2000. Prior to my position at Boise State University, I was an Associate Professor of Electrical Engineering between 1998 and 2000 and Assistant Professor of Electrical Engineering between 1993 and 1998 at the University of Idaho. I have been teaching electrical engineering since 1991.

6. I received a Bachelor of Science and Master of Science degrees in Electrical Engineering from UNLV, in 1986 and 1988, respectively. In 1993, I also received a Ph.D. in Electrical Engineering from the University of Nevada, Reno. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapon tests at the Nevada Test Site. During this time, I designed, and oversaw the fabrication and manufacture of over 30 electronic and electronic-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame and bit-syncs, data converters, streak-camera sweep circuits, Pockels cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics.

7. From 1997 to 1999, I served as a Consultant for Tower Semiconductor, in the design of CMOS integrated circuit cells for various modem chips, interfaces, and serial buses, including charging circuits based upon power up-down circuits using an MOS or bandgap reference, pre-amplifiers, and

comparators. I was also a Senior Designer at Micron Technology from 1994 to 2008, working on the development of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, CMOS Image Sensors (CISs), and power supply design. My more recent industry experience includes working with Freedom Photonics on the integration, fabrication, and design of optoelectronics with CMOS integrated circuits, including the design of compact optical transceiver for range finding applications, Geiger mode SiGe receiver for long-range communications, and packaging and testing of numerous chips fabricated in both CMOS and SiGe technologies. I have worked as a consultant at other companies designing electronic circuits, including Sun, Oracle, Contour Semiconductor, Lockheed-Martin, and OmniVision.

8. I have taught courses in integrated circuit design (analog, digital, mixed signal, memory circuit design, etc.), linear circuits, microelectronics, communication systems, power electronics, and fiber optics. I have been the main advisor to over 100 Master's and Doctoral students.

9. I am the author of several books covering the area of integrated circuit design including: DRAM Circuit Design: Fundamental and High-Speed Topics (two editions), CMOS Circuit Design, Layout, and Simulation (four editions), and CMOS Mixed-Signal Circuit Design (two editions). I have also authored, or

coauthored, more than 100 papers and presentations in the areas of electronic circuit design. I am the named inventor on over 150 granted U.S. patents.

10. I have received numerous awards for my work, including the Frederick Emmons Terman (the "Father of Silicon Valley") Award. The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator's contributions to the profession.

11. I am a Fellow of the IEEE for contributions to memory circuit design. I have also received the IEEE Circuits and Systems Education Award (2011).

12. I have received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001), all from Boise State University.

13. I have also received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor award four of the years I have been at UNLV.

14. In forming my opinions, I have relied on my knowledge and experience in designing, developing, and researching integrated circuit packaging and my knowledge of electrical circuit design and fabrication and electrical engineering fundamentals. I am not an attorney and offer no legal opinions, but in

the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person having ordinary skill in the art.

III. RELEVANT LEGAL STANDARDS

15. I have been asked to provide my opinions as to whether claims 1-6 of the ’527 Patent would have been obvious to a person of ordinary skill in the art as of the earliest claimed priority date of the ’527 patent (February 26, 2003) (“Critical Date”).

16. I am an engineer by training and profession. The opinions I express in this declaration involve the application of my technical knowledge and experience to the evaluation of certain prior art with respect to the ’527 patent. In addition, I understand that the following legal principles apply.

17. It is my understanding that, in determining whether claims of the ’527 patent are obvious in this proceeding, the claim terms are generally given their ordinary and customary meaning as understood by a person of ordinary skill in the relevant art. A person of ordinary skill in the art would read the claim terms in the context of the entire patent specification in which they appear, as well as the prosecution history of the patent.

18. It is my understanding that a claim is unpatentable under 35 U.S.C. § 103 if the claimed subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time of the alleged invention. I also understand

that an obviousness analysis takes into account the scope and content of the prior art, the differences between the claimed subject matter and the prior art, and the level of ordinary skill in the art at the time of the invention.

19. In determining the scope and content of the prior art, it is my understanding that a reference is considered relevant prior art if it falls within the field of the inventor's endeavor. In addition, a reference is prior art if it is reasonably pertinent to the particular problem with which the inventor was involved. A reference is reasonably pertinent if it logically would have commended itself to an inventor's attention in considering his problem. If a reference relates to the same problem as the claimed invention, that supports use of the reference as prior art in an obviousness analysis.

20. To assess the differences between prior art and the claimed subject matter, it is my understanding that 35 U.S.C. § 103 requires the claimed invention to be considered as a whole. This "as a whole" assessment involves showing that one of ordinary skill in the art at the time of invention, confronted by the same problems as the inventor and with no knowledge of the claimed invention, would have selected the elements from the prior art and combined them in the claimed manner.

21. It is my further understanding that several rationales may be applied for combining references or modifying a reference to show obviousness of claimed subject matter. These rationales include: combining prior art elements according to known methods to yield predictable results; simple substitution of one known element for another to obtain predictable results; a predictable use of prior art elements according to their established functions; applying a known technique to a known device (method or product) ready for improvement to yield predictable results; choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify a prior art reference or to combine prior art teachings to arrive at the claimed invention.

IV. TECHNOLOGY BACKGROUND

A. Semiconductor Components for Multi-chip Modules

22. Persons of ordinary skill in the art (POSITAs) have continuously looked for solutions to provide multiple component integration into electronic modules to provide higher levels of system functionality without added signal delay and power dissipation in order to integrate components (such as transistors) in integrated circuits in accordance with Moore's law. APPLE-1036, Abstract; *see also generally* APPLE-1021 (describing background of multilayer printed circuit boards). As Simon Thomas explained, "[t]he growth of the semiconductor industry

has historically depended on the integration of more components on a chip through transistor and interconnects scaling and manufacturing technology." APPLE-1036, 1. "Three-dimensional integration (3D) of components" including "stacking chips/packages, stacking wafers, and fabrication of multiple device layers on the same wafer" offer pathways toward enhanced integration of components with smaller footprints. *Id.*, 1, 2, 4 (reporting that "stacked chip devices are in production" as of the 2003 publication of the conference proceedings).

23. Thomas describes that functionality has increased through "System-on-Chip (SoC) and System in Package (SiP) approaches." *Id*.

> In addition, the increasing drive to integrate diverse component technologies for enhanced SoC functionality, presents a multitude of technical and business challenges. For example, a single chip SoC for a cell phone handset could require GaAs, MEMS, digital, analog, power, and passives technologies. RF circuits integrated with microprocessor in a 3D format, to facilitate wireless communication, has attracted major interest. Another motivation for 3D is the need to reduce footprint of the packaged device, especially for portable applications. There are multiple technology approaches for 3-D integration, currently at varying levels of maturity and each with its own unique strengths and issues. These approaches include [Fig: 1]: - Stacked chips or stacked packages - Stacked wafers through wafer bonding - Device fabrication in multiple planes on the same wafer.

APPLE-1036, 2.

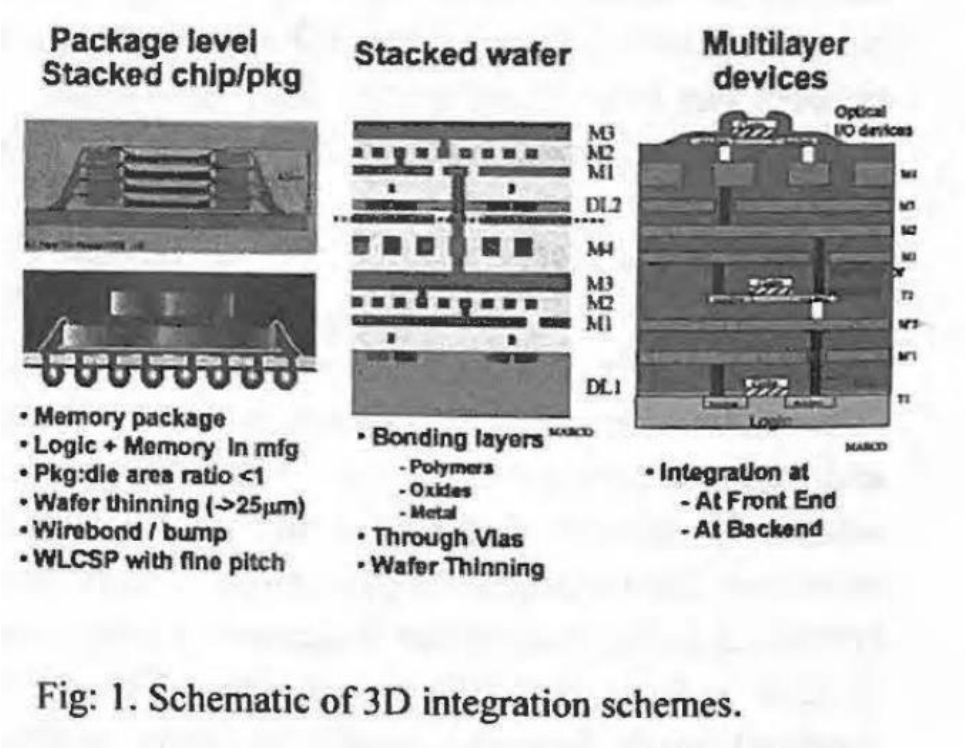


Fig: 1. Schematic of 3D integration schemes.

APPLE-1036, 2

24. Nakatani-II exemplifies how stacking multiple wafers on top of each other was a well-known technique for achieving multiple component integration in a module. For example, Nakatani-II's Figure 4 shows a three-layered "built-in module":

> Referring to FIG. 4, the circuit component built-in module 400 in Embodiment 4 includes an insulating substrate 401 comprising insulating substrates 401a, 401b and 401c, wiring patterns 402a, 402b, 402c and 402d formed on one principal plane and in the internal portion of the insulating substrate 401, a circuit component 403 arranged in the internal portion of the insulating substrate 401 and connected to the wiring patterns 402a, 402b or 402c, and an inner via 404 for electrical

connection between the wiring patterns 402a, 402b, 402c and 402d.

APPLE-1039, 11:12-22.

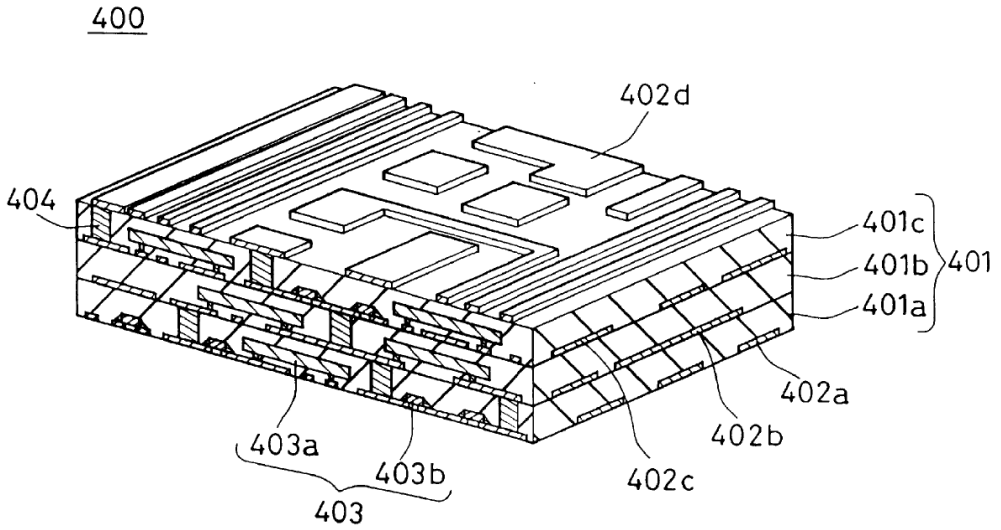


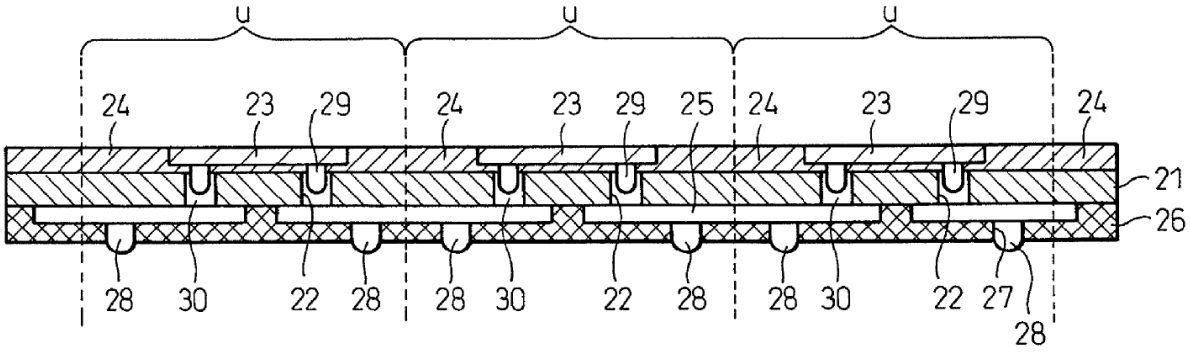
FIG. 4

APPLE-1039, FIG. 4

25. "A plurality of semiconductor devices… may be stacked in layers… to form a thin multilayer semiconductor device" in U.S. Patent Application Publication No. 2001/0026010 to Horiuchi et al. ("Horiuchi"). APPLE-1038, [0105]. Horiuchi describes a method including producing an initial structure containing multiple electrical components which are then "cut into semiconductor package units 'u'… to obtain individual semiconductor devices 20." *Id.*, [0101], [0115], [0127], [0143], [0154]. For example, Horiuchi's Figure 9 (reproduced

below) shows semiconductor elements 23 which are bonded and mounted to the top surface of tape substrate 21 "by heating the semiconductor elements 23 to a temperature near the melting point of the low melting point metal 30 and pushing the connection terminals 29 into the low melting point metal 30 in the through holes 22." *Id.*, [0094]. "A sealing resin layer 24 covering the top surface of the tape substrate 21" is then ground and polished to a predetermined thickness. *Id.*, [0097]-[0099]. After the grinding and polishing, the external connection terminals 28 are formed and the "assembly is cut into semiconductor package units 'u' at the positions shown by the broken lines in FIG. 9 to obtain individual semiconductor devices." *Id.*, [0100]-[0101].

Fig.9



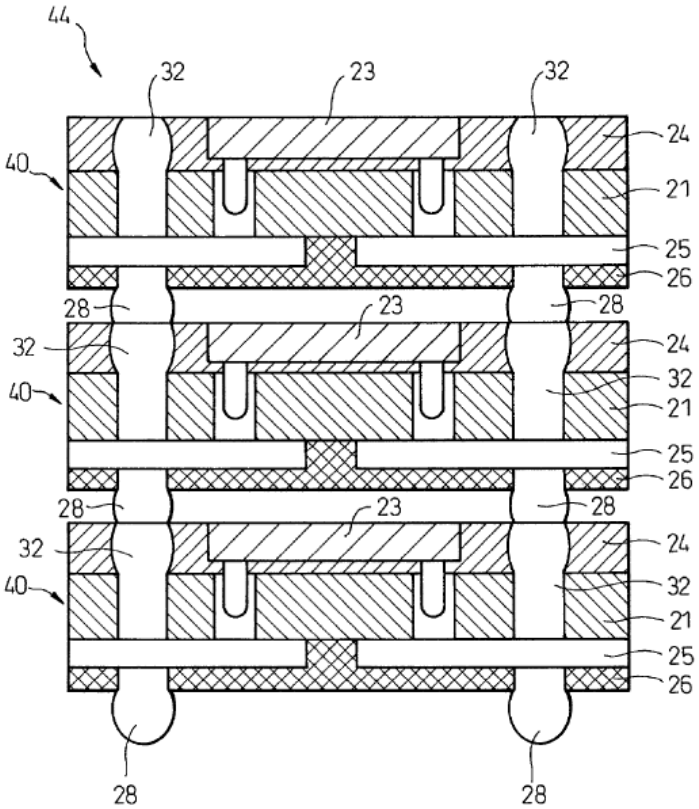
APPLE-1038, FIG. 9

26. Following the cutting procedure, Horiuchi's cut semiconductor devices "may be stacked in layers as shown in FIG. 11 to form a thin multilayer semiconductor device 44" by:

> connecting the top ends of the low melting point metal conductors 32 of a bottom semiconductor device 40 and the bottom ends of the external connection terminals 28 of a top semiconductor device 40, a single semiconductor device 4 comprised of an integral circuit including a plurality of semiconductor elements 23 (in this example, three) in a multilayer structure is formed.

APPLE-1038, [0105].

Fig.11



APPLE-1038, FIG. 11

27. As Thomas notes, "[a]nother interesting concept of multilayer device integration is to build active devices within an interconnect level." APPLE-1036, 6-7. This type of technology had "become increasingly attractive" during the 90's. APPLE-1037, 1. For example, in 1999, A. Kujala, R. Tuominen, and J.K. Kivilahti, explained that, "General Electric (GE) introduced high density interconnection technology for embedded chips. HDI technology is a 'chip first' solution where active components are placed in cavities formed in a ceramic or embedded into plastic encapsulant." APPLE-1037, 1. As shown below in Figure 2, the chips are interconnected through laser ablated vias. *Id*., 2. "The HDI technology enables the fabrication of complex [multi-chip modules] with a very high packaging density and low interconnect impedance" while providing "good protection both mechanically and chemically." *Id*.

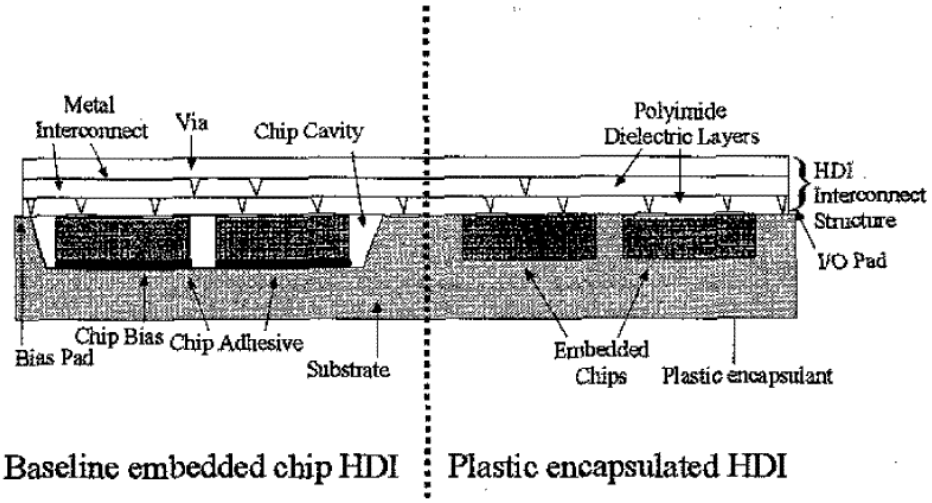


Fig. 2 Schematic presentation of embedded HDI chips [5].

APPLE-1037, FIG. 2

28. Kujala et al. further describe that in conventional fabrication methods, "[h]igh interconnection density is achieved with MCM [multi chip module] technology where fine patterned copper layers and dielectric layers are fabricated on various substrates [and] [i]ntegrated circuits are then connected to MCM substrate with wire bond, TAB or flip chip solder bumps." APPLE-1037, 1. They then describe methods that use "gold bump[s] interconnected to copper wire" for fabrication of MCM components using solderless methods. *Id.*, 3-4.

29. As additional examples, Nakatani, Eichelberger, Suwa, and Nakatani-II show mounting multiple chips in a single layer. Specifically, due to the increased demand for smaller-sized higher-density circuit boards, Nakatani

discloses "at least two electric elements (203) such as semiconductor chips or surface acoustic wave devices … mounted on wiring patterns." APPLE-1007, Abstract, [0003], [0017] ("In FIG. 7, numeral 601 denotes surface acoustic wave devices…"), [0127]; *see also infra* §XI.A. Nakatani's "first wiring patterns 609 and [] metal bumps 605 are electrically connected" using "heat and ultrasonic wave[s]" to melt the metal bumps 605 for the connection of the components (surface acoustic wave devices 601) with the circuit board. *Id*., [0016], [0020], [0125]. Nakatani describes that by including a plurality of components in a single layer, the semiconductor package's thickness is improved by having the multiple thin chips successfully mounted on a thinner substrate. *Id*., [0011]-[0012].

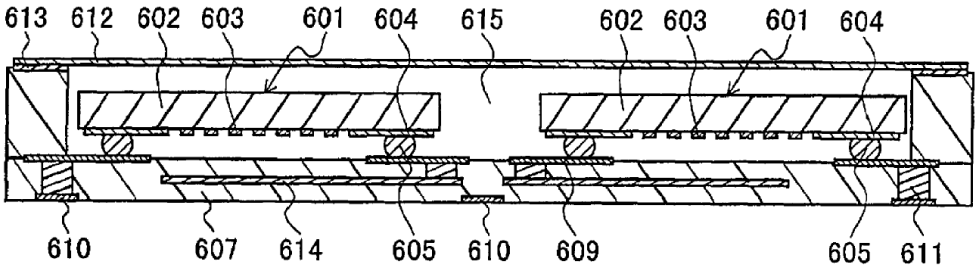
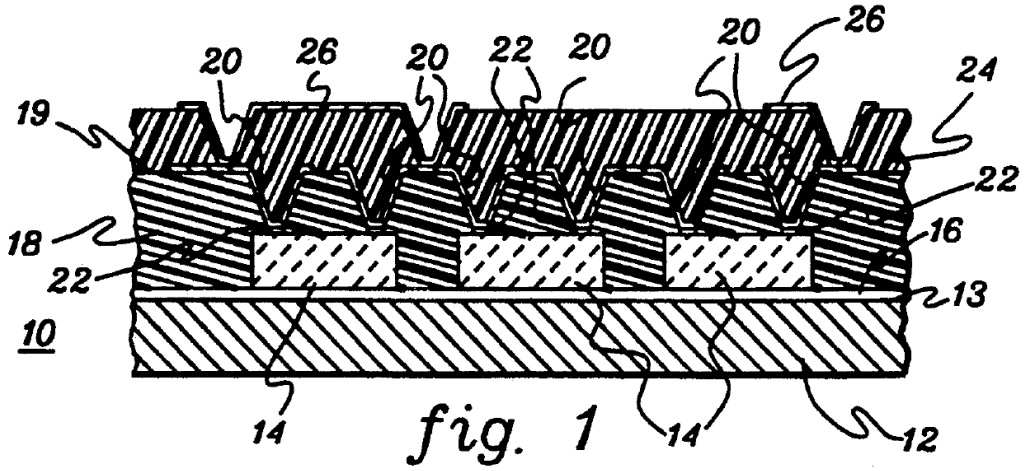


FIG . 7
PRIOR ART

APPLE-1007, FIG. 7

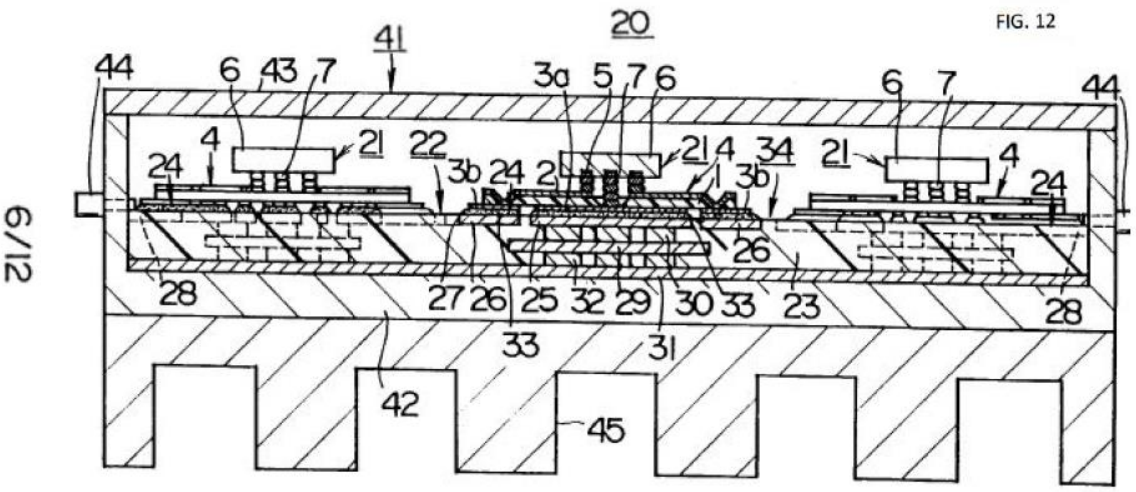
30. Similarly, U.S. Patent No. 5,250,843 to Eichelberger discloses a "multichip integrated circuit package comprises a substrate having a flat upper surface to which is affixed one or more integrated circuit chips having interconnection pads." APPLE-1040, Abstract. As shown below in Figure 1, Eichelberger's multichip module includes multiple semiconductor components 14 arranged in one single layer. Eichelberger's multichip module structure has high I/O capacity with optimal heat removal, has been optimized for speed, and has the ability to incorporate an assortment of components of varying thickness and functions into the module. *Id*., 1:17-27.



APPLE-1040, FIG. 1

31. International Patent Application WO1996012296 to Suwa et al. ("Suwa") also discloses a multi-chip module. *See* APPLE-1041. Suwa's multi-chip module (MCM) 20 is provided with a plurality of chip assemblies 21 "in

which the IC chip 6 is facedown-bonded to the tape 4." *Id.*, 12. "A plurality (four in the illustrated example) of the chip assemblies 21 is used in the MCM 20, and passive elements and active elements are incorporated into each chip assembly 21." *Id.*, 12-13. In Suwa's multi-chip module (MCM) 20, the chip assemblies are arranged in an opening formed in the base 42 and hermetically sealed by a cap 43. *Id.*, 15, FIG. 12.



APPLE-1041, FIG. 12

32. Suwa describes that since the IC chips 6, are "mounted on the wiring board 22 via the tape 4 with a thickness of approximately 50 μm, the level difference between the wiring board 22 and the IC chip 6 can be extremely minimalized, and therefore a drop in the impedance can be suppressed when a

high-speed signal is transmitted, and impedance matching of the highspeed signal line 2b can be easily ensured." APPLE-1041, 16. Furthermore, Suwa describes that since "IC chip 6 is surface-mounted in the wiring board 22 in the chip assembly 21, no cavity needs to be formed in the wiring board 22, and therefore the manufacturing costs of the wiring board 22 as well as of the MCM 20 can be reduced." *Id*.

33. As I explained above, Nakatani-II also exemplifies multiple components in a single insulating substrate layer. As shown in Figure 1, Nakatani-II's circuit components 103 are "connected to the wiring pattern 102b and arranged in the insulating substrate 101, and an inner via 104 for electric connection between the wiring patterns 102a and 102b." APPLE-1039, 6:67-7:3.

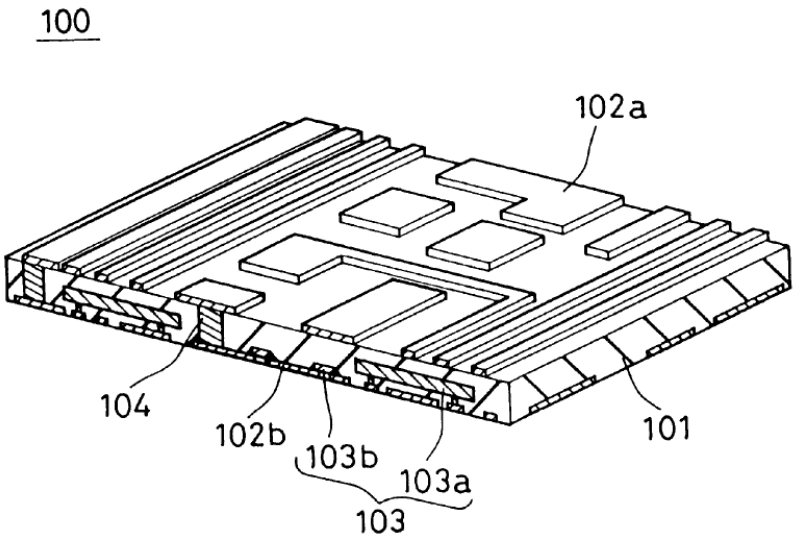


FIG. 1

APPLE-1039, FIG. 1

34. In summary, it was well-recognized by POSITAs to mount a plurality of chips on a substrate, and further to stack a plurality of chip modules accordingly.

B. Bonding Techniques

35. Preparation of a semiconductor package or chip requires that components be electrically connected to wiring patterns on a printed circuit board or other substrate, so that the package or chip can be supplied with power and be grounded, as well as connecting the package or chip to other components. APPLE-1022, 6 ("A printed circuit board is a piece of plastic material on which electronic

components can be mounted for mechanical support, and which also electrically interconnects all the components it supports by means of a pattern of metal tracks on its outer surfaces and sometimes on inside layers"). By the Critical Date, a variety of techniques for bonding components to wiring of printed circuit boards were well known and in use, including solderless techniques including ultrasonic bonding and thermocompression. *See e.g.*, APPLE-1037 (1999 article in IEEE reporting on "Solderless Interconnection and Packaging Technique for Embedded Active Components"). The '527 patent does not purport to have invented these techniques, and indeed, ultrasonic and thermocompression bonding techniques (i.e., "solderless techniques") were well-known years before the filing date of the '527 patent. *Id.*; APPLE-1001, 6:46-48 ("Methods and equipment for ultrasonic bonding are commercially available."), 6:63-65 ("Methods and equipment for thermo-compression bonding are also commercially available").

i. Ultrasonic Bonding

36. The '527 patent offers the following description of ultrasonic bonding:

> The ultrasonic method then refers to a method, in which two pieces containing metal are pressed against each other while vibration energy at an ultrasound frequency is brought to the area of the joint. Due to the effect of the ultrasound and the pressure created between the surfaces to be joined, the pieces to be joined are bonded metallurgically. Methods and equipment

> for ultrasonic bonding are commercially available. Ultrasonic bonding has the advantage that a high temperature is not required to form a bond.

APPLE-1001, 6:41-49.

Ultrasonic bonding techniques combine ultrasonic vibrations and heat or pressure to bond two metal components to one another. For example, Matsuda describes a technique that combines ultrasonic methods with thermocompression. Matsuda describes that electrodes 4 of a semiconductor chip are aligned with metal bumps 5 (e.g., Ni or Au) formed on a substrate and then the pieces are "subjected to pressure by a bonding tool while applying ultrasonic vibrations and heat." APPLE-1009, [0007], [0006], [0012]. "The bumps 5 are deformed to form an Au/Al alloy on the contact surface, and the chip electrodes 4 and bumps 5 are thermocompressed." *Id.*, [0007], [0013], FIGS. 2A-B.

ii. Thermo-compression Bonding

37. Similarly, the '527 patent gives the following description related to thermo-compression bonding methods:

> The term thermo-compression method refers in turn to a method, in which two pieces containing metal are pressed against each other while thermal energy is brought to the area of the joint. The effect of the thermal energy and the pressure created between the surfaces to be joined cause the pieces to be joined to be bonded metallurgically. Methods and equipment for thermo-compression bonding are also commercially available.

Id., 6:58-65.

38. Glick explains that " [t]hermocompression bonding is a solid-phase bonding technique which forms the bond between two members by inducing a suitable amount of material flow in one or both members." APPLE-1020; 3:33-36. "[M]aterial flow [between the two members] is induced by the application of heat and pressure, which are maintained for a suitable length of time so that adhesion takes place without the presence of a liquid phase." *Id.*, 3:36-39.

V. PERSON OF ORDINARY SKILL IN THE ART

39. It is my understanding that when interpreting the claims of the '527 patent I must do so based on the perspective of one of ordinary skill in the art at the time of the alleged invention ("POSITA"). For purposes of my analysis in this declaration, I have been asked to assume that the priority date of the '527 patent is February 26, 2003 ("Critical Date"). I understand that the factors considered in determining the ordinary level of skill in a field of art include the level of education and experience of persons working in the field; the types of problems encountered in the field; the teachings of the prior art, and the sophistication of the technology at the time of the alleged invention. I understand that a POSITA is not a specific real individual, but rather is a hypothetical individual having the qualities reflected by the factors above. I understand that a POSITA would also have knowledge from the teachings of the prior art, including the art cited below.

40. Taking these factors into consideration, it is my opinion that one of ordinary skill in the art would have had a Bachelor's degree in electrical engineering, materials science, applied physics, or a related technical field, and 2-3 years of experience in the research, design, development, or testing of circuit board or microcircuit components, or the equivalent. Additional graduate education could substitute for professional experience, or additional professional experience could substitute for formal education.

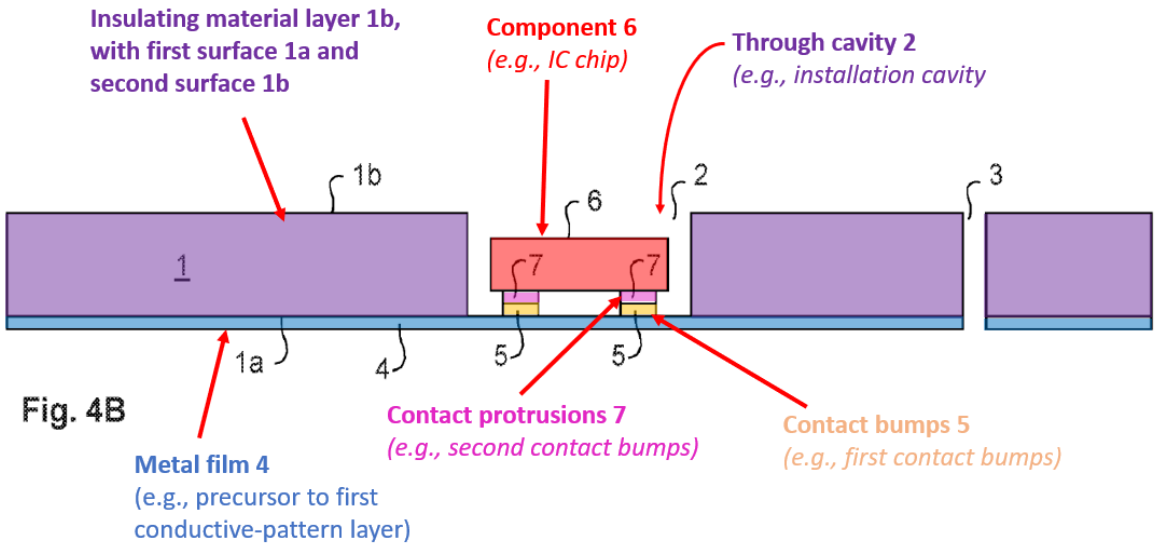
41. I have possessed the qualifications of a POSITA since the Critical Date of the '527 patent, and long before. *See supra* §II.

VI. OVERVIEW OF THE SUBJECT PATENT US 7,609,527, "THE '527 PATENT"

42. The '527 patent is titled Electronic Module. It was filed on October 17, 2007 as a continuation of U.S. Application No. 10/546,820 (filed on August 25, 2005; now U.S. Patent No. 7,299,546). APPLE-1001, Cover. Although not listed on the cover of the '527 patent, the U.S. priority application was filed as a U.S. national stage entry of PCT/FI04/00101 (filed February 25, 2004). APPLE-1002, 53. The '527 application also claims priority to Finnish Application No. 20030292, filed on February 26, 2003. *Id.*

43. The '527 patent describes "an electronic module which includes one or more components embedded in an installation base." APPLE-1001, 1:16-18.

The ’527 patent describes that “it is thus possible to manufacture a circuit board, inside which components are embedded.” *Id.*, 3:56-57. In the method, “[a]n unpatterned metal film 4, which acts as the conducting surface of the installation base for the components 6 to be installed and connected, is made on the first surface 1a of the insulating substance layer 1.” *Id.*, 6:22-26. “[C]onductive patterns 14 are formed from the conductive layer 4 … for example, using one of the selective etching methods that are widely used and well known in the circuit-board industry.” *Id.*, 10:28-35, FIGS. 6A-6C.



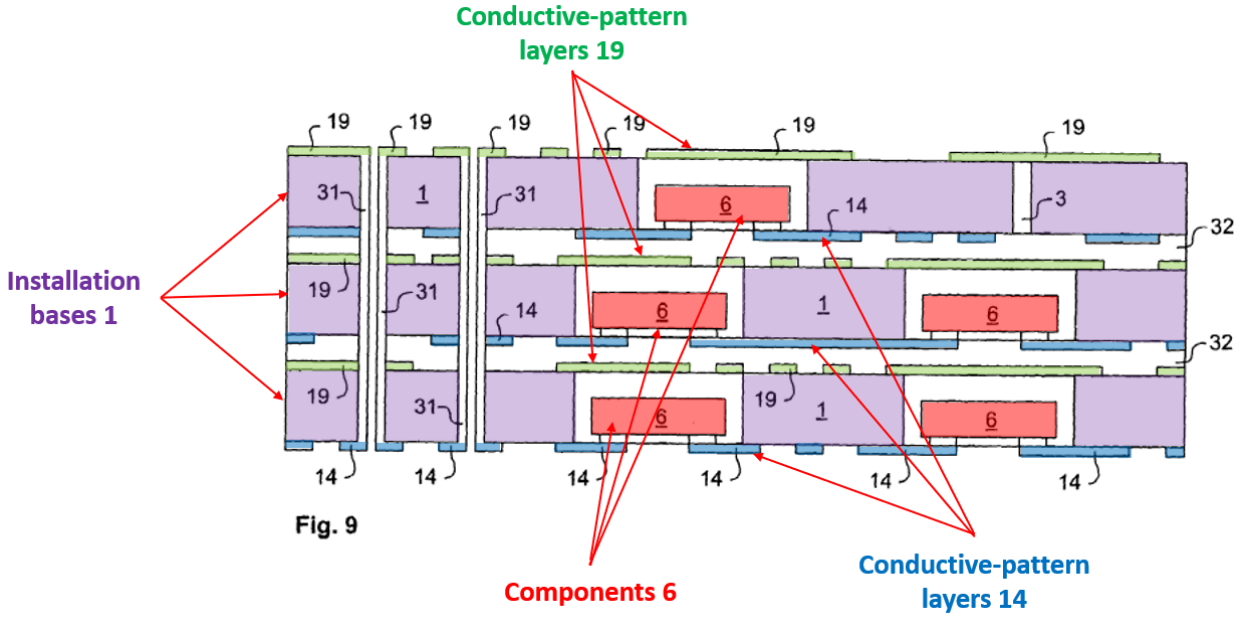
APPLE-1001, FIG. 4B (annotated)

44. As shown above, the “component 6, which includes contact bumps 7 in the connection zones of the component, is connected to the installation base.” *Id.*, 9:19-21. “[C]ontact bumps 5 are also formed on top of the conductive layer 4

[and t]he contact bumps 7 of the component are then connected to the contact bumps 5 of the installation base [by] the ultrasonic or thermo-compression methods." *Id.*, 9:36-41. Although not shown in FIG. 4B, "a conductive film 9, from which conductive patterns 19 can be formed later, can also be made on the second surface 1b of the insulating material layer 1." *Id.*, 7:33-35, FIGS. 7A-7C, 8A-8C.

45. The specification further explains that, through use of the contact bumps, "[s]oldering is not needed in the connections of the components, [and] instead an electrical connection between the connection zones on the surface of the component and the metal membrane of the installation base is created, for example, by ultrasonic welding, thermo-compression, or some other such method, in which the temperatures required to achieve electrical connections, though high, are of short duration and local." *Id.*, 4:19-26. These techniques purportedly facilitate manufacturing of "smaller structures" that allow components to be "placed closer together." *Id.*, 4:51-52; *see also id.*, 5:8-11.

46. The '527 patent further describes with reference to FIG. 9, "a multi-layered electronic module, which includes three installation bases 1 laminated on top of each other, together with their components 6, and a total of six conductive-pattern layers 14 and 19." *Id.*, 11:53-56.



APPLE-1001, FIG. 9 (annotated)

VII. PROSECUTION HISTORY OF THE '527 PATENT

47. I have reviewed the file history of U.S. Application No. 11/907,795 ("the '795 application), from which the '527 patent issued.

48. I understand that the application was rejected only one time during prosecution. In the only Office Action issued during prosecution of the application, the Examiner rejected the original claims of the '527 patent as being anticipated by the Asahi reference (APPLE-1025). APPLE-1002, 58-68. In response, the Applicant amended the claims to add further limitations related to the connections between the component and the first conductive-pattern layer. For example, the amendments to independent claim 1 are shown below. *Id.*, 84-90. Similar amendments were made to the other independent claims.

1. (Currently Amended) An electronic module, comprising:

a first conductive-pattern layer having a first surface,

first solid contact bumps solderlessly made on the first surface of the first conductive-pattern ~~layer.~~ layer and metallurgically and electrically connected thereto,

a component having flat contact zones,

second solid contact bumps solderlessly made on the flat contact zones and metallurgically and electrically connected thereto, and

an insulating-material layer on the first surface of the first conductive-pattern layer,

wherein the component is embedded in the insulating-material layer and wherein the second solid contact bumps made on the flat contact zones of the component are metallurgically, ~~metallurgically and~~ electrically and solderlessly connected to the first solid contact bumps made on the first surface of the first conductive-pattern layer.

APPLE-1002, 84

49. Along with the amendments, the Applicant submitted remarks arguing that "the Asahi reference definitely fails to disclose using two contact bumps, that is, the first and second contact bumps to form a single contact between the component and the conductive-pattern layer," and that Asahi instead relies on "[c]onductive adhesives and anisotropic conductive films which are used between the bump and the conductive-pattern do not form metallurgical contact between the attached structures." APPLE-1002, 92; *see also id.*, 91-93.

50. Following the Applicant's response to the first Office Action, the Examiner allowed the application, and referenced the first and second contact

bumps in the reasons for allowance. In particular, the Examiner's reasons for allowance stated: "the best prior art references… fail[] to teach or fairly suggest … the component is embedded in the insulating-material layer and wherein the second solid contact bumps made on the flat contact zones of the component are metallurgically, electrically and solderlessly connected to the first solid contact bumps made on the first surface of the first conductive-pattern layer." APPLE-1002, 102-105.

51. However, as I will discuss below, all features recited in the Challenged Claims are disclosed in one or more of Nishiuma, Yoneyama, Nakatani, Shibata, and Onda, none of which were considered by the Office or cited in the Office Action, and the claimed combinations of these features would have been obvious before the Critical Date.

VIII. CLAIM CONSTRUCTION

52. I do not believe that any term requires explicit construction. I understand that claim terms in an *inter partes* review proceeding are given their plain and ordinary meaning in light of the specification and file history. For purposes of my analysis in this declaration, I have applied claim interpretations consistent with the patent owner's allegations of infringement against Apple in the parallel district court proceeding. *See* APPLE-1105.

53. I reserve the right to offer opinions on any claim constructions proposed in this proceeding or to offer opinions on additional constructions that are raised in the parallel district court proceeding.

IX. OVERVIEW OF CONCLUSIONS FORMED

54. This expert Declaration explains the conclusions that I have formed based on my analysis. To summarize those conclusions:

- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-2, 4-6, 11-13, 15-16, 19, 21, 25 and 27 of the ’527 patent are rendered obvious by Nishiuma.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 7-8 and 17-18 of the ’527 patent are rendered obvious by Nishiuma in view of Nakatani.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 20 and 26 of the ’527 patent are rendered obvious by Nishiuma in view of Nakatani and Yoneyama.

- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 3 and 14 of the '527 patent are rendered obvious by Nishiuma in view of Shibata.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-27 of the '527 patent are rendered obvious by Yoneyama in view of Onda.

55. Nishiuma, Nakatani, Shibata, Yoneyama, and Onda are all analogous art to the '527 patent in that they are all in the same field of endeavor and/or reasonably pertinent to the problems said to be addressed by the '527 patent. For example, each of the prior art references applied in Grounds 1A-2 below describe techniques for manufacturing and packaging electronic modules. APPLE-1001, 1:13-28 (describing the field of the invention: "The present invention relates to an electronic module… which includes one or more components embedded in an installation base"); APPLE-1004, 1:11-17 ("The present invention relates to a semiconductor integrated circuit device fabrication technique and a semiconductor integrated circuit device obtained by the technique, and particularly to a technique for connecting a semiconductor chip to a printed wiring board by face down bonding of a semiconductor chip to a wiring substrate using metallic bumps"); APPLE-1007, [0001] ("The present invention relates to a module containing

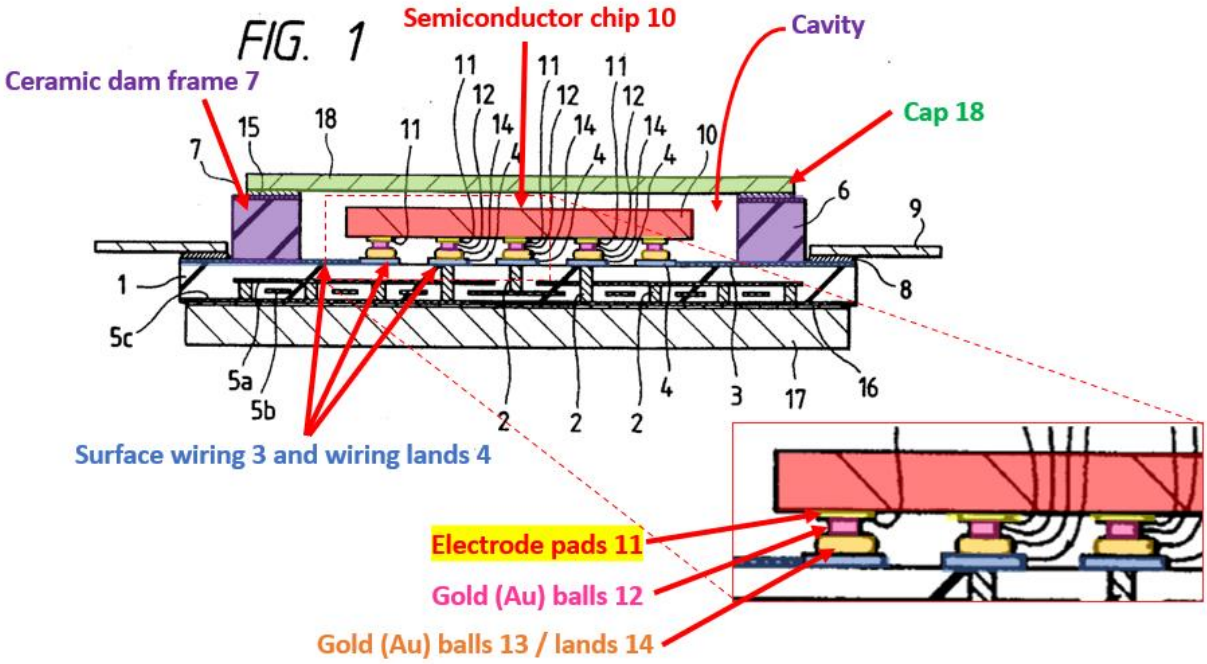
electric elements such as semiconductor chips or surface acoustic wave devices… [in particular] an electric element built-in module [and] a method for manufacturing such an electric element built-in module"): APPLE-1005, [0001] ("The invention relates to a so-called chip-on-chip … type semiconductor device, in which a plurality of semiconductor chips is electrically interconnected as opposed to each other, and a method for manufacturing the same."): APPLE-1013, Title ("Circuit board with embedded electronic components and manufacturing method therefor"), Problem ("To obtain a circuit board with embedded electronic component that makes circuit design easier without increasing the number of vias for connection to outside components"), [0001] ("The present invention relates to a circuit board with embedded electronic components and a method for manufacturing the same"); APPLE-1008, Title ("Wiring substrate, semiconductor device, electronic devices using these, and manufacturing methods for these").

X. GROUND 1A – NISHIUMA RENDERS OBVIOUS CLAIMS 1-2, 4-6, 11-13, 15-16, 19, 21, 25 AND 27

A. Overview of Nishiuma (APPLE-1004)

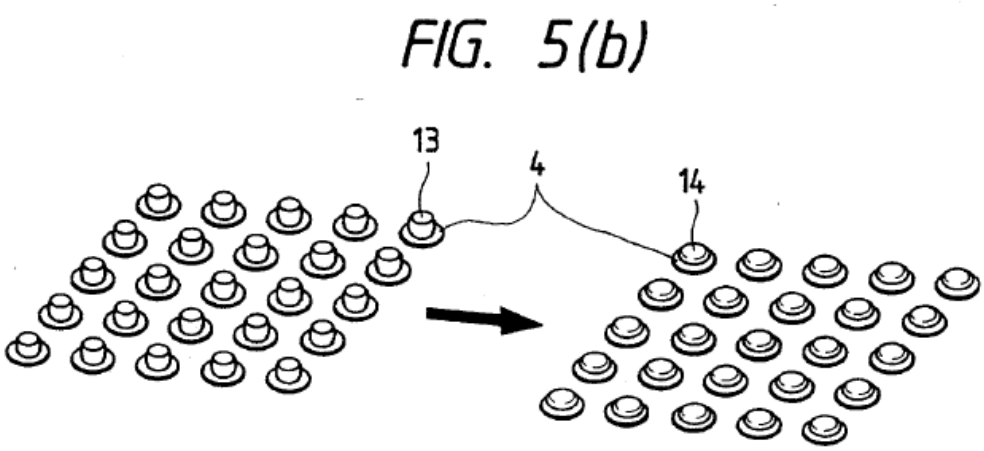
56. Nishiuma describes a "semiconductor integrated circuit device" formed as "a package structure fabricated by sealing a semiconductor chip 10 mounted on a wiring substrate 1 with a cap 18." APPLE-1004, Abstract, 6:66-7:2. Nishiuma's ceramic "square dam frame 6" "forms a cavity in which the

semiconductor chip 10 is mounted." APPLE-1004, 7:48-54. Nishiuma's "cap 18" is bonded to "the frame 6 through a sealing metallize 7 and brazing filler metal 15." *Id.*, 7:51-55.



APPLE-1004, FIG. 1 (annotated and modified to include excerpt)

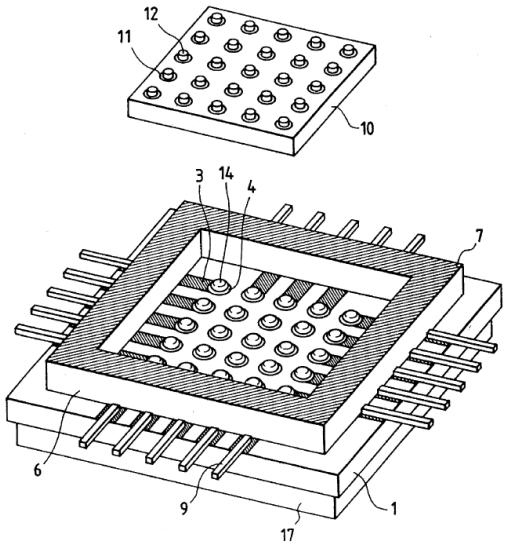
57. As shown in FIG. 1, Nishiuma's wiring substrate 1 includes surface wiring 3 and wiring lands 4 made of "thick films of refractory metal." APPLE-1004, 7:67-8:3. Nishiuma's gold (Au) balls 13 (not shown in FIG. 1) are bonded to wiring lands 4 "using heat or ultrasonic energy or both" and flattened to form Au lands 14. *Id.*, 8:18-19, 8:28-29, 9:4-6.



APPLE-1004, FIG. 5(b)

58. Nishiuma's "semiconductor chip 10" includes "electrode pads 11" that are "made of [gold] similarly to the integrated circuit wirings." APPLE-1004, 8:10-16. Au balls 12 are "bonded to the electrode pads 11 of the semiconductor chip 10" using "heat or ultrasonic energy or both" and are then bonded to Au lands 14 by "thermocompression bonding" to achieve an electrical connection between the semiconductor chip and the surface wiring. *Id.*, 8:17-19, 9:13-16, 7:43-47.

FIG. 4



APPLE-1004, FIG. 4

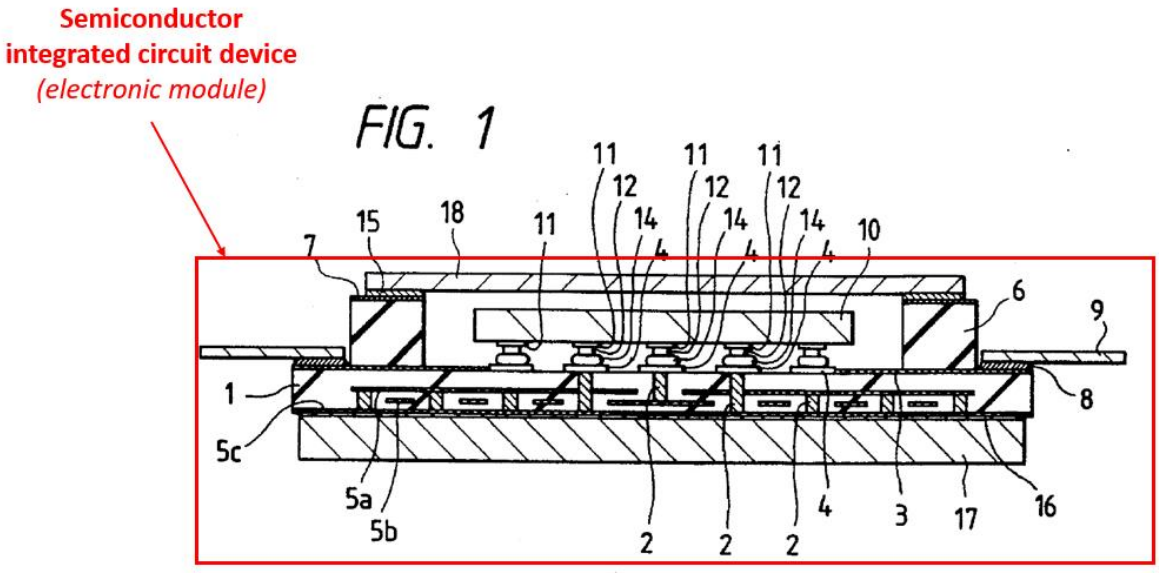
B. Analysis

iii. Claim 1

[1pre] An electronic module, comprising:

59. To the extent the preamble is limiting, Nishiuma renders [1pre] obvious. Nishiuma describes a semiconductor integrated circuit device that constitutes an "***electronic module***" as claimed. APPLE-1004, 1:11-17 ("The present invention relates to a semiconductor integrated circuit device fabrication technique and a semiconductor integrated circuit device obtained by the technique, and particularly to a technique for connecting a semiconductor chip to a printed wiring board by face down bonding of a semiconductor chip to a wiring substrate

using metallic bumps"); *cf.* APPLE-1001, 1:18-23 ('527 patent describing that an electronic module "can be a module like a circuit board, which includes several components [such as] semiconductor components"). For example, Nishiuma's FIG. 1 depicts that "the semiconductor integrated circuit device of this embodiment has a package structure fabricated by sealing semiconductor chip 10 mounted on a wiring substrate 1 with a cap 18." APPLE-1004, 6:66-7:2.



APPLE-1004, FIG. 1 (annotated)

Nishiuma's semiconductor integrated circuit device falls within the '527 patent's definition of an electronic module. APPLE-1001, 1:18-23.

60. Additionally or alternatively, as I will discuss more below with regard to independent claims 19 and 25, the broad definition of "electronic module" given

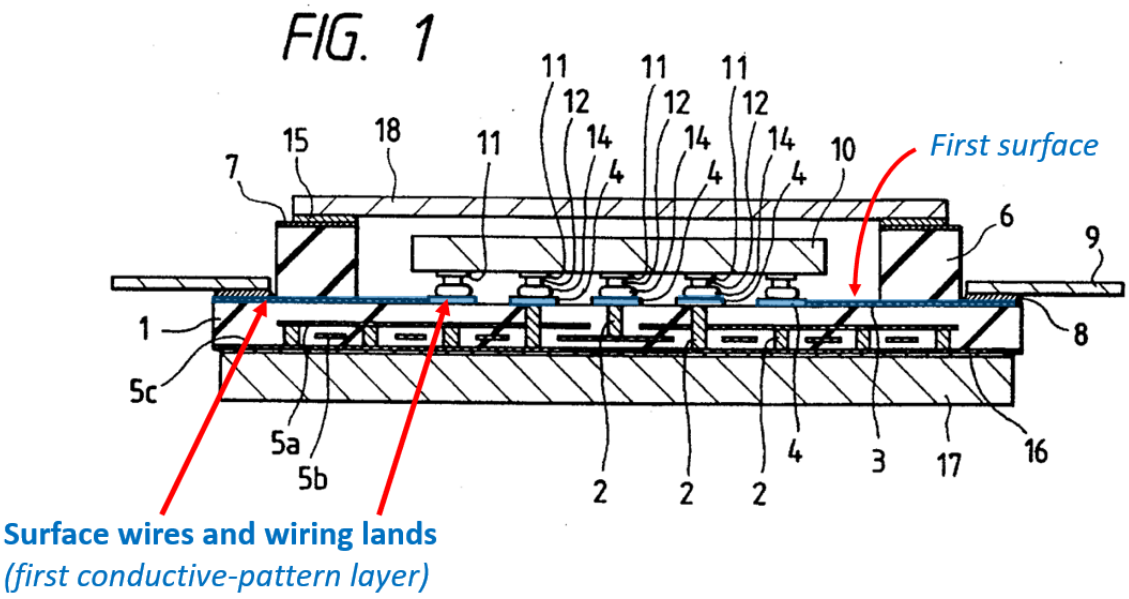
by the '527 patent allows Nishiuma's semiconductor integrated circuit device to be understood to include two modules – a printed circuit board providing a first electronic module and a semiconductor chip with wiring patterns positioned on the circuit board as a second electronic module. APPLE-1001, 1:18-23. In this additional or alternative mapping, the semiconductor chip with wiring patterns of the circuit board provides the claimed electronic module, as I will discuss below.

[1a] a first conductive-pattern layer having a first surface,

61. Nishiuma renders obvious element [1a]. For example, Nishiuma describes that on the surface of the printed wiring board "a plurality of surface wires 3 and a plurality of wiring 1 and electrodes 4 are formed." APPLE-1004, 7:7-10, 7:14-16, FIG. 1. The surface of the printed wiring board 1 including surface wires 3 can further include wiring lands 4. *Id.*

62. Nishiuma's surface wires and wiring lands form a pattern on the printed wiring board for establishing connection to components. After forming the wires and the lands on the board, the wires and lands would have one surface in contact with the printed wiring board and an opposite surface pointed away from the board ("***a first surface***"). *See* APPLE-1004, 7:13-15 (describing that "The surfaces of the surface wiring 3 and wiring lands 4 are plated with Ni and Au in the order from the bottom" implying that the wiring and lands have surfaces.).

Accordingly, Nishiuma's plurality of surface wires and wiring lands collectively provide the claimed "***first conductive-pattern layer***" having "***a first surface***" atop the surface wiring and wiring lands.



APPLE-1004, FIG. 1 (annotated)

63. Nishiuma describes that the surface wires 3 and wiring lands 4 together cooperate to form a conductive layer for the transmission of power and information signals. APPLE-1004, 7:16-18; ("The surface wirings 3 are wirings for input/output signals, GND, and power source, one end of each of wirings is connected to one of the wiring lands 4."), 7:11-14 ("surface wiring 3[and] lands 4 … are made of thick films of a refractory metal"); *cf.*, APPLE-1001, 6:50-57 (describing layers that can include "several metals as layers, accumulations, zones,

or metal alloys"). Additionally, Nishiuma makes clear that the surface wires and lands are formed from the same materials, and by the same screen-printing technique. For example, Nishiuma describes that "[t]he surface wiring 3 and wiring land 4 of thick films of a refractory metal such as W plated with Ni and Au are formed on the surface of the printed wiring board 1 by a known screen printing method." APPLE-1004, 7:67-8:3; *see also* 7:7-16. From Nishiuma's description of the common function, materials, and manufacturing process of the surface wiring and lands, a POSITA would have understood that the surface wiring and lands together provide a "***first conductive-pattern layer***." The dispersed arrangement of electrodes and contact points provided by the surface wires and wiring lands provide additional forms patterning the conductive layer, as I will discuss further below. Because the lands and surface wires cooperate to provide a common functionality, a POSITA would have recognized that the lands and surface wires provide a "first … layer" as claimed.

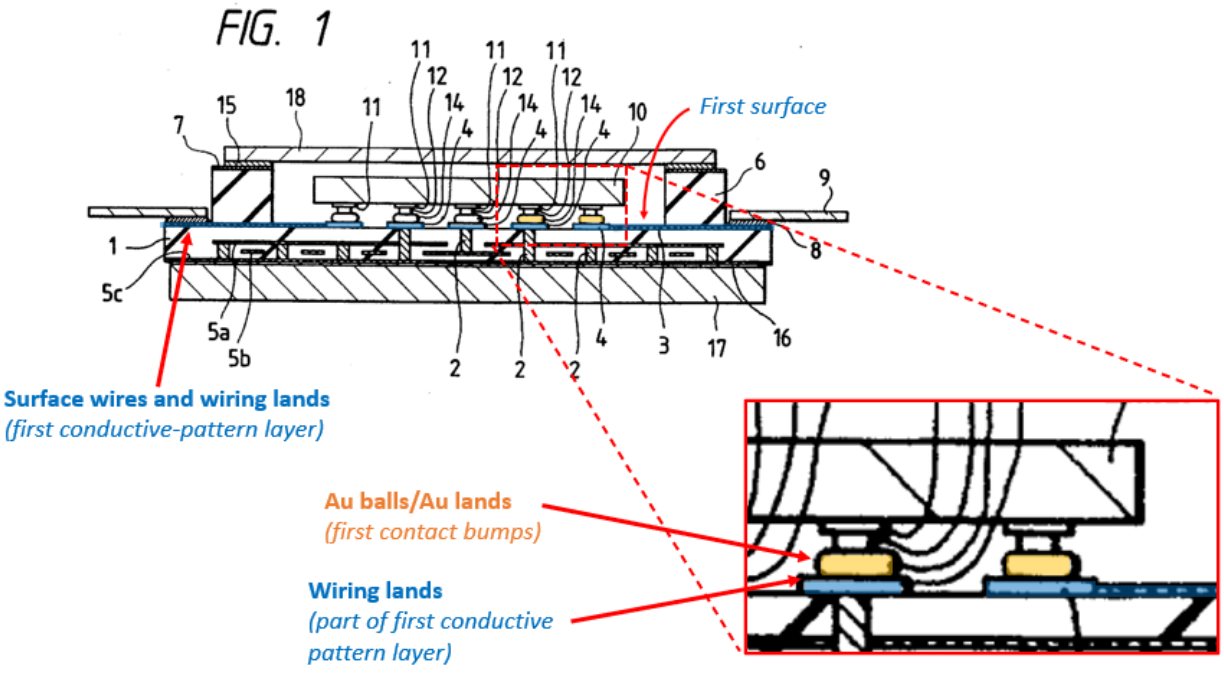
64. Additionally, the surface wires 3 and wiring lands 4, being formed of metal, are electrically conductive. APPLE-1004, 4:31-33 ("it is possible to provide the input/output signal paths of the printed circuit substrate only by forming surface wirings…"); *see also* APPLE-1022, 9 ("A printed circuit board is a piece of plastic material on which electronic components can be mounted for mechanical

support, and which also electrically interconnects all the components it supports by means of a pattern of metal tracks on its outer surfaces and sometimes on inner layers."). Nishiuma describes that the surface wiring and lands are formed from tungsten and plated with nickel and gold—all of these materials being known to be electrically conductive. APPLE-1004, 7:11-16; APPLE-1035, 133. For example, the electrical resistivity of tungsten is about 5.3×10^{-8} Ω-m, for nickel it is about 0.95×10^{-7} Ω-m, and for gold 2.35×10^{-8} Ω-m. *Id.* Resistivity is the inverse of conductivity, and thus a low resistivity indicates a material that readily allows an electrical current. *Id.*, 133, 12.

65. The arrangement of individual electrodes and discrete contact points provided by the metal surface wires 3 and wiring lands 4 form patterning in the conductive layer as claimed. Nishiuma describes that as part of the preparation of the printed wiring board "[t]he surface wiring 3 and wiring land 4 of thick films of a refractory metal such as W plated with Ni and Au are formed on the surface of the printed wiring board 1 by a known screen printing method." APPLE-1004, 7:66-8:3. Screen printing the surface wiring and lands enables the creation of a pattern of wires on the printed wiring board to provide connection to devices, such as a semiconductor chip.

[1b] first solid contact bumps solderlessly made on the first surface of the first conductive-pattern layer and metallurgically and electrically connected thereto,

66. Nishiuma renders obvious element [1b]. For example, Nishiuma describes that "Au balls 13 are bonded to the wiring lands 4 of the printed wiring board 1…." APPLE-1004, 8:28-29. After bonding the Au balls 13 to the wiring lands 4, "Au lands 14 are formed by pressing and flattening the Au balls 13…." *Id.*, 8:46-48. The Au balls 13 before pressing/flattening and/or Au lands 14 after pressing/flattening provide "***first solid contact bumps***" made on a first surface of the wiring lands 4 (***first surface of the first conductive-pattern layer***) as claimed.



APPLE-1004, FIG. 1 (modified to include close-up, annotated)

67. As shown in FIG. 1, Nishiuma's Au balls provide bumps on the surface wires and wiring lands for contacting bumps formed on the component (i.e., Au bumps 12). APPLE-1004, 7:38-47, 8:28-29, 8:34-44, 9:13-25, FIG. 1. Nishiuma describes that the Au balls have a diameter and height, and are then formed into Au lands 14 "by pressing and flattening the Au balls bonded to the wiring lands 4 of the printed wiring board." *Id.*, 8:28-33, 8:45-47. Nishiuma's description of the balls being flattened into lands 14 to provide a larger diameter and smaller height than the Au balls 13 provides that the gold balls, and subsequently the gold lands formed from flattening the balls, are solid as claimed.

68. Nishiuma describes that the "Au balls 13 are bonded to the wiring lands 4" "using heat or ultrasonic energy or both or a thermo-compression bonding." APPLE-1004, 2:60-3:21, 8:17-19, 8:28-29. A POSITA would have understood and found obvious that Nishiuma's "ball-bonding method" is a ***solderless*** method in which gold balls are bonded directly to the wiring lands. *Id.*, 7:43-47. Rather than relying on solder, Nishiuma's describes a ball-bonding method that uses heat and a pressing tool to apply pressure to provide a strong bond between the gold ball and the gold plating of the surface land. *Id.*, 9:17-22, 7:43-47, 8:28-29.

69. Indeed, Nishiuma explicitly touts that the "[a]ccording to the present invention, since ***solder, which is prone to thermal fatigue, is not used***, reliability of the connection part between the semiconductor chip and the wiring substrate is improved." APPLE-1004, 4:10-13[1]; *see also id.*, 4:25-31, 9:27-59, 10:23-56. Thus, Nishiuma is explicit in describing the connections as being formed by a solderless method.

70. A POSITA likewise would have understood and found obvious that the bonding of the gold balls to the wiring lands results in a ***metallurgical and electrical connection*** between the balls (***first solid contact bumps***) and the top of the wiring lands (***first surface of the first conductive-pattern layer***). The '527 patent describes that to form a metallurgical bond between items, the material of the item must contain "enough of at least one metal." APPLE-1001, 6:50-54. Nishiuma's bonding of the gold balls to the wiring lands (formed of tungsten plated with nickel and gold) clearly couples two items both of which include metal in an amount necessary to form a bond between the items, and further to establish an electrical connection between them. APPLE-1004, 7:11-16, 7:42-47, 8:28-29.

71. Indeed, the heat, ultrasonic energy, and thermo-compression techniques described in Nishiuma each provides metallurgical bonding that allows

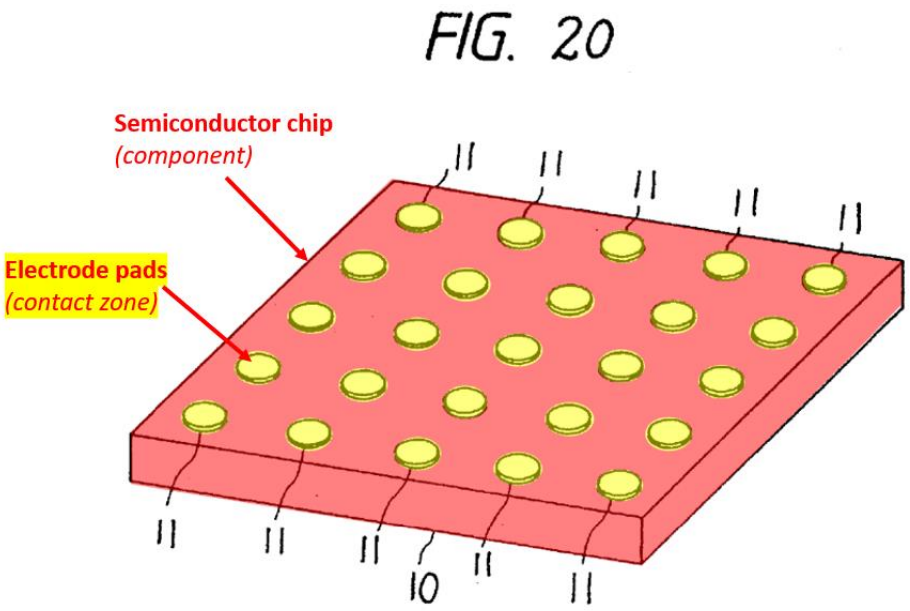
[1] All emphasis added unless indicated otherwise.

an electrical current to flow between the semiconductor chip and board wiring through the Au and wiring lands. *See* APPLE-1004, 10:19-21 ("improve the reliability of connection …"), 7:43-47 ("The wiring lands 4 of the printed wiring board 1 is ***electrically connected*** to the electrode pads 11 of the semiconductor chip 10 by bonding the Au lands 14 to the Au balls 12 by a thermo-compression bonding."). The '527 patent notably describes the same solderless processes including "ultrasonic welding" and "thermo-compression" as those described in Nishiuma, which yield the metallurgical and electrical connections as claimed. *See supra* §IV.B; *see also* APPLE-1001, 6:41-49, 4:19-65; APPLE-1004, 8:17-19, 8:28-29, 14:37-46.

[1c] a component having flat contact zones,

72. Nishiuma renders obvious element [1c]. For example, Nishiuma describes a "semiconductor integrated circuit device" formed as "a package structure fabricated by sealing a semiconductor chip 10 mounted on a wiring substrate 1 with a cap 18." APPLE-1004, Abstract, 6:66-7:2. Nishiuma describes that the semiconductor chip 10 (***component***) includes electrode pads 11 (***flat contact zones***) that, for example, can be "made of Au similarly to the integrated circuit wirings." *Id.*, 8:13-16, FIG. 1; *see also id.*, 7:2-6, 8:13-16 ("electrode pads

11 are formed by boring holes in the surface protection film"), 17:46-48, FIGS. 3-4 Abstract.

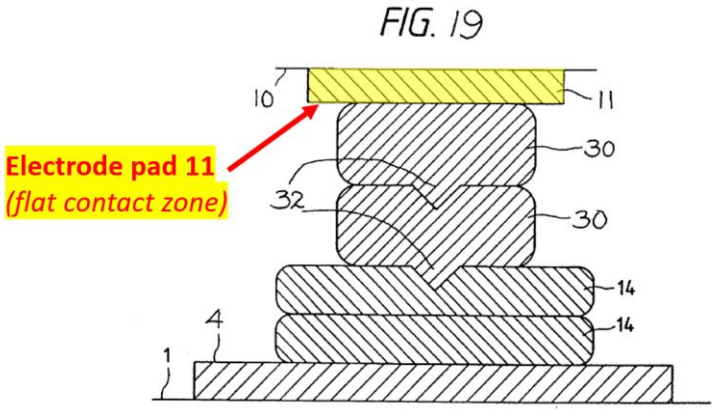


APPLE-1004, FIG. 20 (annotated)

73. The plain meaning of the claim term "flat contact zone" should be interpreted as requiring a surface lacking curvature, and should not be interpreted to be limited to contact zones that do not protrude from the surrounding surfaces of the component.

74. As shown in the cross-sectional view in FIGS. 19 and 20, Nishiuma's electrode pads 11 have flat surfaces that lack curvature. APPLE-1004, 8:10-16 (describing that "electrode pads 11 are formed by boring holes in the surface protection film" covering the element forming surface of the chip). This is

consistent with the plain meaning of the word "flat." Additionally, nothing in the plain language of the claims, the '527 patent's specification or the prosecution history indicates that the term "flat" should be understood to have another meaning, and in particular does not indicates that a flat contact zone must not protrude from the surface of the component. Indeed, the term "flat" appears in the '527 patent specification only in the phrase "flat contact zones" and without additional description of additional characteristics required of a "flat" contact zone. APPLE-1001, 3:8-27; 9:46-55. The Applicant did not require in the claims that the contact zone have other properties (such as not protruding relative to a surface of the component) and accordingly, such other properties should not be read into the claim language. Nishiuma's electrode pad 11 having a surface that lacks curvature provides the claimed "flat contact zones."

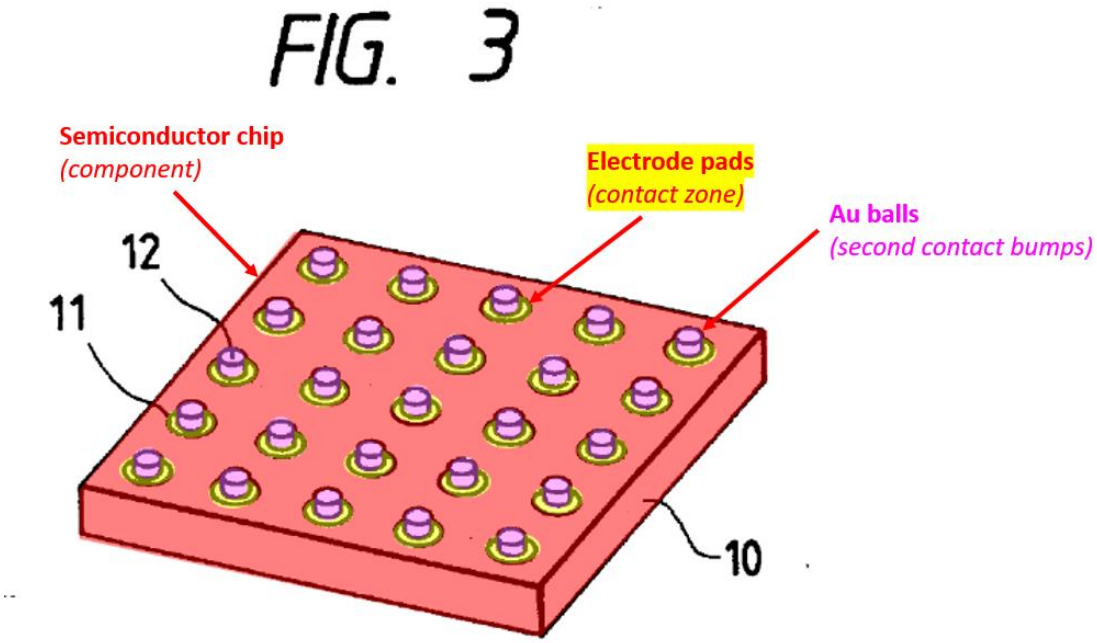


APPLE-104, FIG. 19 (annotated)

75. To the extent that the claim language is interpreted to require contact zones that are not raised relative to the surrounding component surfaces, Nishiuma provides this well-known feature. For example, Nishiuma discloses that "electrode pads 11 are formed by boring holes in the surface protection film" covering the element forming surface of the chip, which would have resulted in electrode pads that do not protrude from the chip's surface. APPLE-1004, 8:10-16. Although Nishiuma's figures depict electrode pads as extending from the surface of the component, Nishiuma's disclosure is agnostic as to the particularities of the semiconductor chip describing that it has electrode pads for bonding but without disclosing any criticality related to the shape, position, or protrusion of the electrode pads – a POSITA reading Nishiuma would have understood that electrode pads of the component could be selected depending on the intended application, for example to reduce chip thickness. Further, IC chips having non-raised electrode pads were well-known by the Critical Date and it would have been obvious to a POSITA to apply such electrode pads in Nishiuma's device as an obvious design choice. *See e.g.*, APPLE-1008, FIGS. 1B, 5A-C, 6A-B, 7A-B, 9A-B, 10A-B (all depicting electrode pads 2 as flush with surrounding surfaces of the component and not protruding from the surface of the component).

[1d] second solid contact bumps solderlessly made on the flat contact zones and metallurgically and electrically connected thereto, and

76. Nishiuma renders obvious element [1d]. For example, Nishiuma describes "Au balls 12 having a diameter smaller than that of the Au lands 14 [that] are bonded to the electrode pads 11 on the element forming surface of the semiconductor chip 10." APPLE-1004, 7:41-43, 8:17-19. Au balls 12 constitute "***second solid contact bumps***" made on the electrode pads 11 (***contact zones***) of the semiconductor chip (***component***) as claimed.



APPLE-1004, FIG. 3 (excerpted, annotated)

77. As shown in FIG. 3, Nishiuma's Au balls 12 provide bumps on the electrode pads 11 that are intended to contact bumps formed on the printed wiring board (i.e., Au bumps 13 / Au lands 14). APPLE-1004, 7:38-47, 8:28-29, 8:34-44, 9:13-25, FIG. 1. Nishiuma describes that the Au balls have a diameter and height and that the diameter and height can be adjusted by changing the diameter of the wire used to form the balls. APPLE-1004, 8:30-33. Nishiuma's description of the diameter and height of the balls and disclosure that the balls are formed by a gold wire provides that the gold balls are solid, as claimed.

78. Nishiuma describes that the "Au balls 12 are bonded to the electrode pads 11 of the semiconductor chip 10 by a known ball-bonding method using heat or ultrasonic energy or both." APPLE-1004, 8:17-19; *see also id.*, 2:64-67 ("The metal balls can be bonded to the electrode pads … using heat or ultrasonic energy, or both or a thermo-compression bonding."), 10:56-65, 17:19-22. As described above, a POSITA would have understood and found obvious that Nishiuma's "ball-bonding method" is a ***solderless*** method in which gold balls are bonded directly to the electrode pads. *Id*. As described above, Nishiuma's ball-bonding method relies on heat and a pressing tool to apply pressure to provide a strong bond between the gold ball and electrode. *Supra*, §X.B.[1b]; *see also* APPLE-1004, 9:17-22, 7:43-47, 8:28-29.

79. Indeed, Nishiuma explicitly touts that the "[a]ccording to the present invention, since ***solder, which is prone to thermal fatigue, is not used***, reliability of the connection part between the semiconductor chip and the wiring substrate is improved." APPLE-1004, 4:10-13; *see also id.*, 4:25-31, 9:27-59, 10:23-56. Thus, Nishiuma is explicit in describing the connections as being formed by a solderless method.

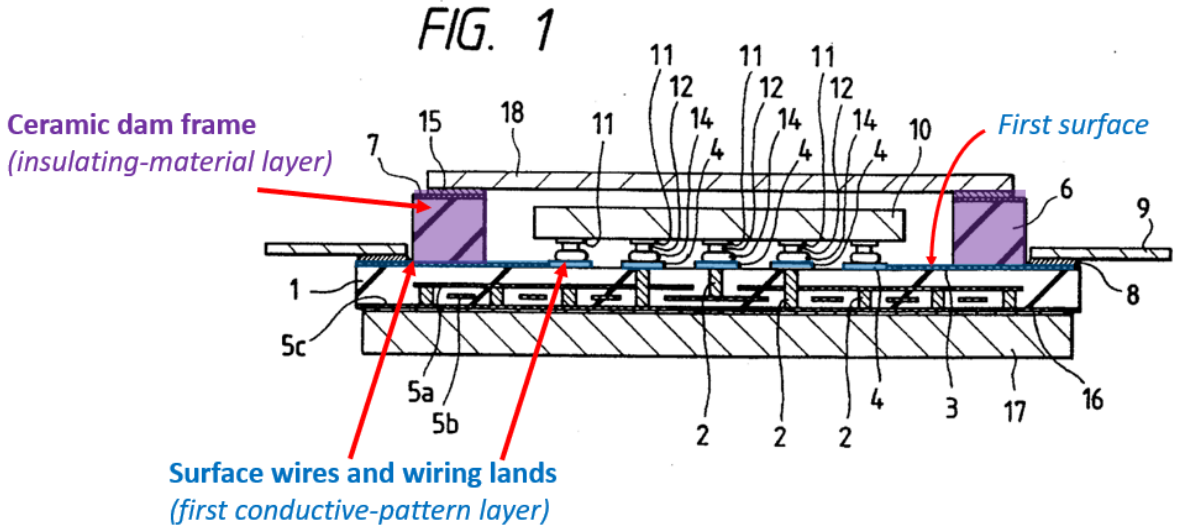
80. A POSITA similarly would have understood and found obvious that the bonding of the gold balls to the electrode pads results in a ***metallurgical and electrical connection*** between the balls (***second solid contact bumps***) and the pads (***flat contact zones***). Nishiuma's bonding of the gold balls to the electrode pads (formed from a metal, as a POSITA would have understood is conventional) clearly couples two items both of which include metal in an amount necessary to form a bond between the items, and further to establish an electrical connection between them. APPLE-1004, 7:11-16, 7:42-47, 8:28-29.

81. Indeed, the heat, ultrasonic energy, and thermo-compression techniques described in Nishiuma each provides metallurgical bonding that allows an electrical current to flow between the semiconductor chip and board wiring through the gold balls and electrode pads. APPLE-1004, 10:19-21, 7:41-47 ("electrically connected"). The '527 patent notably describes the same solderless

processes including "ultrasonic welding" and "thermo-compression" as those described in Nishiuma, which yield the metallurgical and electrical connections as claimed. *See supra*, §IV.B; *see also* APPLE-1001, 6:41-49, 4:19-65; APPLE-1004, 8:17-19, 8:28-29, 14:37-46.

[1e] an insulating-material layer on the first surface of the first conductive-pattern layer,

82. Nishiuma renders obvious element [1e]. For example, Nishiuma describes that "[a] square dam frame 6 for sealing is formed around the semiconductor chip 10 on the wiring board 1." APPLE-1004, 7:48-55, 8:5-9. As shown in FIG. 1, dam frame 6 is disposed on a top surface of the surface wiring 3 (***first surface of the first conductive-pattern layer***) of the printed wiring board 1. APPLE-1004, FIG. 1. Because Nishiuma's dam frame 6 is formed on a top surface of the surface wirings 3, the ceramic dam frame is on the first surface of the first-conductive pattern layer. *Id.*



APPLE-1004, FIG. 1 (annotated)

83. Nishiuma further describes that "[t]he dam frame 6 is made of ceramic such as alumina or aluminum nitride," which are electrical insulators. APPLE-1004, 7:49-51. A POSITA would have recognized that Nishiuma's ceramic dam frame 6 is an insulator because alumina and aluminum nitride are well-known electronic insulators. *Id.*; APPLE-1035, 43 ("Most polymers and ionic ceramics are insulating materials at room temperature"), 134 (showing high electrical resistivity in a variety of insulators including aluminum oxides ("alumina")); APPLE-1010, 1:9-17 (ceramic is "a suitable electrically insulating material"); APPLE-1011, [0006] (chip carrier packages can be formed from ceramic and alumina insulators). A POSITA would have further found it obvious to implement Nishiuma's ceramic dam frame as an insulator to prevent electrical

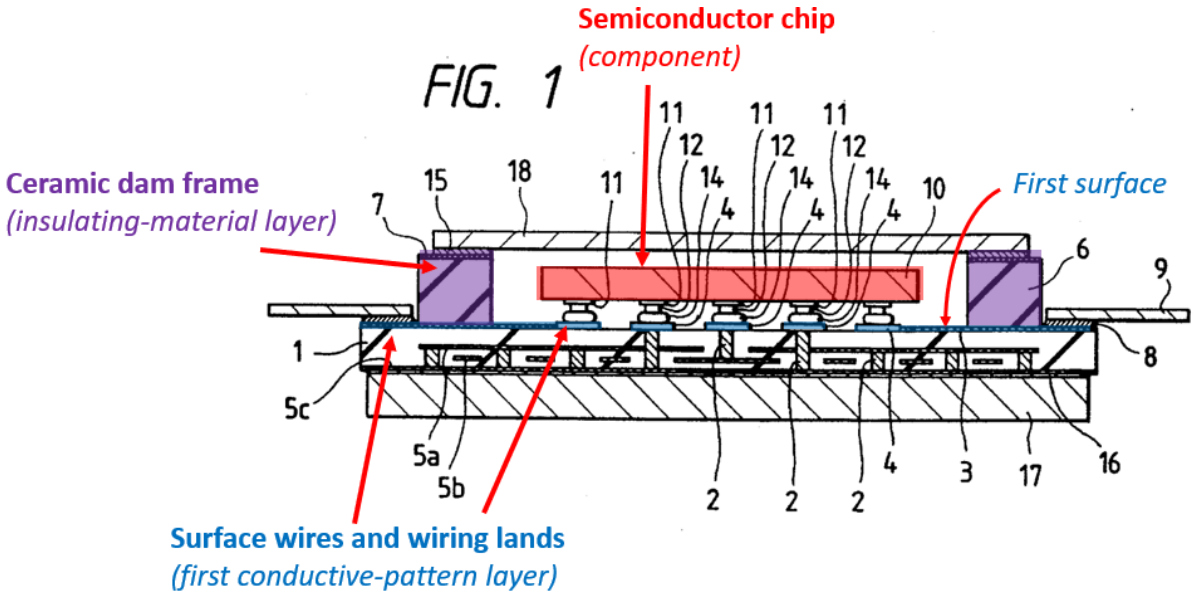
signals from wiring 3 from conducting to other components contacted by dam frame 6 or causing undesirable electrical short circuiting.

84. Accordingly, Nishiuma's dam frame provides an "***insulating-material layer***" as claimed.

[1f-i] wherein the component is embedded in the insulating-material layer

85. Nishiuma renders obvious element [1f-i]. For example, Nishiuma describes that "[t]he sealing dam frame 6 forms a cavity in which the semiconductor chip 10 is mounted." APPLE-1004, 7:53-54. As shown in FIG. 1, Nishiuma's device thus provides a semiconductor chip (***component***) embedded in the ceramic dam frame (***insulating-material layer***). APPLE-1004, FIGS. 1, 6.

86. Nishiuma's semiconductor chip 10 mounted within a cavity of the sealing dam frame 6 is embedded within the dam frame in the same way as discussed in the '527 patent. For example, the '527 patent discusses that a component is "embedded entirely inside the installation base" when the "insulating-material layer 1…[is] thicker than the component to be installed. APPLE-1001, 7:58-61, 7:62-67 (describing that in cases where thicker component protrude out from the insulating-material layer these components are still "embedded into the installation base"), 3:50-55.

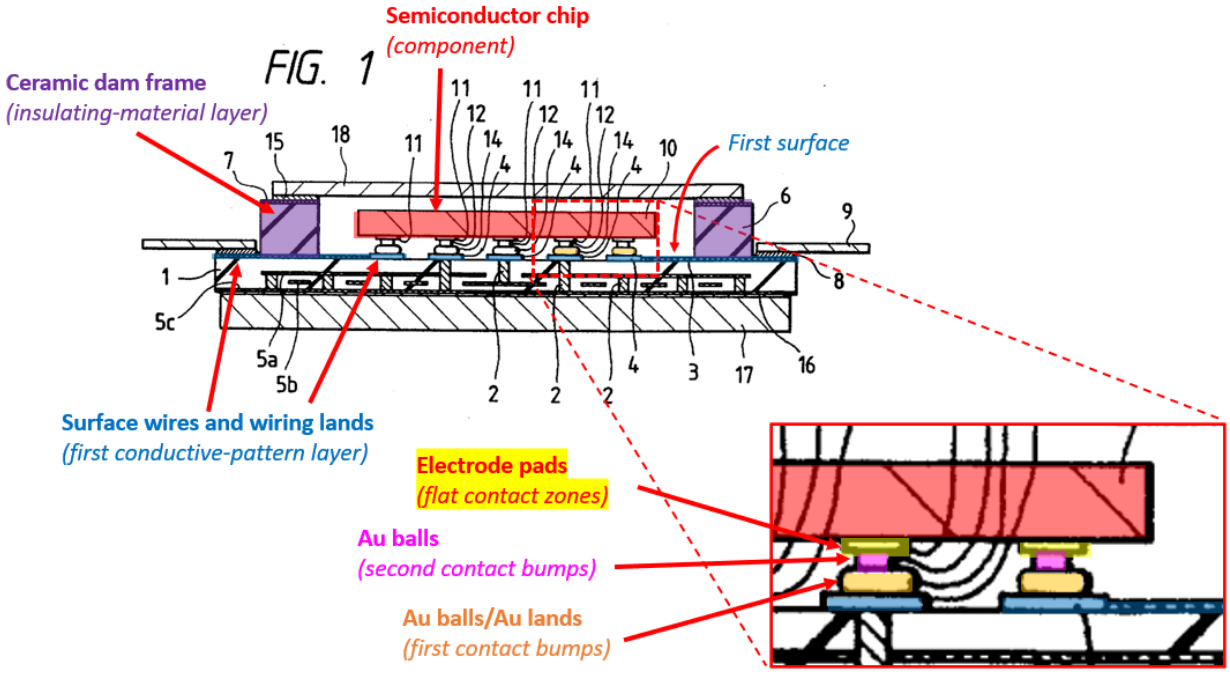


APPLE-1004, FIG. 1 (annotated)

87. Nishiuma's FIG. 1 shows that the dam frame provides the cavity in which the semiconductor chip is enclosed, and thus the semiconductor chip (***component***) is embedded in the ceramic dam frame (***insulating-material layer***) as claimed. APPLE-1004, FIG. 1; *see also id.*, FIGS. 2-4, 6, 11-12, 15-17, 38 (Nishiuma's FIGS. showing that the cavity formed by the ceramic dam frame completely surrounds a perimeter of the semiconductor chip).

[1f-ii] and wherein the second solid contact bumps made on the flat contact zones of the component are metallurgically, electrically and solderlessly connected to the first solid contact bumps made on the first surface of the first conductive-pattern layer.

88. Nishiuma renders obvious element [1f-ii]. For example, Nishiuma teaches that the Au balls 12 (***second solid contact bumps***) formed on the semiconductor electrode pads (***flat contact zones of the component***) are connected to the Au lands 14 (***first solid contact bumps***) formed on the surface wiring and wiring lands of the circuit board (***first surface of the first-conductive pattern layer***) after bonding Au lands 14 to Au ball 12. APPLE-1004, 7:43-47, 9:13-22, FIG. 1.



APPLE-1004, FIG. 1 (modified to include closeup, annotated)

89. A POSITA would have understood and found obvious that Nishiuma's "thermo-compression bonding" between Au balls 12 and Au lands 14 is a ***solderless*** method that achieves ***electrical and metallurgical connection*** between the two gold balls. APPLE-1004, 4:10-12 ("According to the present invention, since solder, which is prone to thermal fatigue, is not used, reliability of the connection part between the semiconductor chip and the wiring substrate is improved"), 9:13-9:22 ("All Au balls 12 are simultaneously bonded to all Au lands 14 by heating the semiconductor chip 10 and printed wiring board 1 up to [approximately] 300C and pressing the tool … against the back of the semiconductor chip 10 from the top"), 8:17-19, 11:13-18, 13:11-13, 14:13-34,

FIGS. 28a-c. Indeed, as discussed above, Nishiuma is explicit that the described ball-bonding method using heat and compression is accomplished without the use of solder. APPLE-1004, 4:10-12.

90. Nishiuma further explains that "[t]he wiring lands 4 of the printed wiring board 1 is electrically connected to the electrode pads 11 of the semiconductor chip 10 by bonding the Au lands 14 to the Au balls 12 by a thermo-compression bonding." APPLE-1004, 7:43-47. Nishiuma thus discloses that the wiring lands (***first conductive pattern layer***) are electrically connected to the (***flat contact zones***) through the Au lands (***first solid contact bumps***) and the Au balls (***second solid contact bumps***). *Id.* To achieve this electrical connection between the electrodes and the wiring lands, each of the elements forming that pathway must also be electrically connected to one another – including the Au lands (***first solid contact bumps***) and the Au balls (***second solid contact bumps***). A POSITA would have appreciated that the thermo-compression bonding method provides this electrical connection so that the device can function, and further that the bonding method provides a metallurgical connection between the two sets of gold balls/lands for a strong coupling of the semiconductor chip to the substrate.

91. Bonding of the Au balls on the electrode pads to Au lands on the surface wiring/lands results in a ***metallurgical and electrical connection***, which is

confirmed by the '527 patent's own description of thermocompression bonding as a solderless method of forming metallurgical and electrical connections. APPLE-1001, 6:41-49; APPLE-1004, 8:17-19, 8:28-29, 9:13-26, 14:37-46; *see also supra* §IV.B. As a result of the solderless connection, the electrode pads (***contact zones***) are effectively metallurgically and electrically connected to the surface wiring and wiring lands of the circuit board (***first surface of the first-conductive pattern layer***) after bonding Au lands 14 to Au ball 12. APPLE-1004, 7:43-47, 9:13-22, FIG. 1.

iv. Claim 2

[2a] The electronic module of claim 1, wherein the insulating-material layer comprises a first surface and a second surface, the first surface being against the first conductive-pattern layer,

92. Nishiuma renders obvious claim [2]. For example, with regard to element [2a], as described above, Nishiuma teaches that the ceramic dam frame (***insulating-material layer***) has a first surface against the surface wiring/lands (***first conductive pattern layer***) of the printed wiring board and a second surface opposite the first surface. APPLE-1004, 7:48-50 ("A square dam frame 6 for sealing is formed around the semiconductor chip 10 on the wiring board 1"), FIG. 1; *supra* §X.B.[1e] (Ground 1A). The first and second surfaces of Nishiuma's dam

frame (***insulating-material layer***) are shown, for example, in the annotated version of Nishiuma's FIG. 10 below. *Infra,* §X.B.[2b] (Ground 1A).

[2b] and the electronic module comprises a second conductive-pattern layer on the second surface of the insulating-material layer.

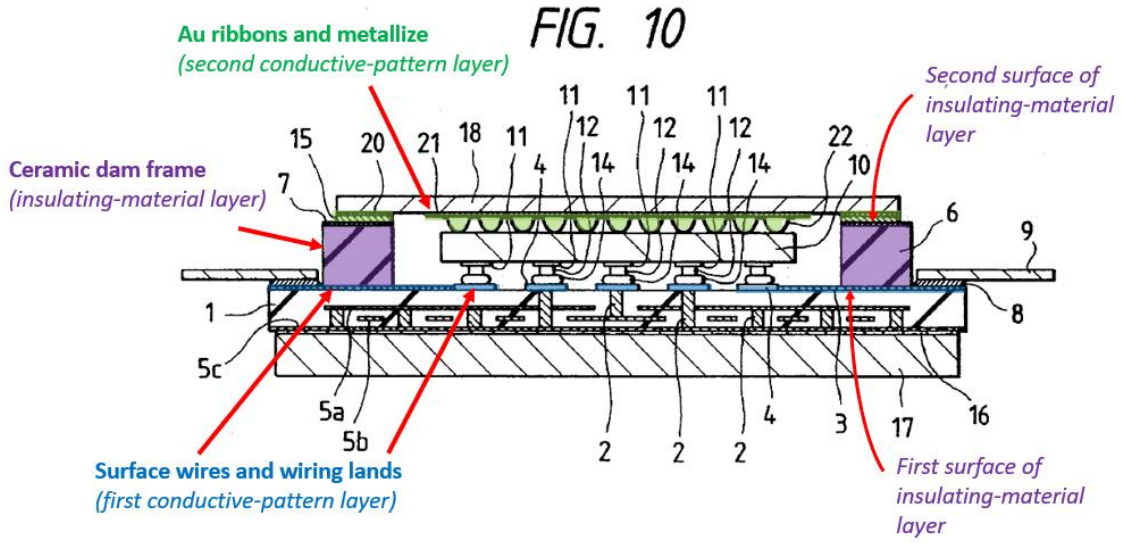
93. With regard to element [2b], Nishiuma further describes that, "the semiconductor integrated circuit device of this embodiment has a package structure fabricated by sealing a semiconductor chip 10 mounted on a wiring substrate 1 with a cap 18." APPLE-1004, 6:66-7:2, 7:48-60. Nishiuma's "cap 18 is bonded to the surface of the frame 6 through a sealing metallize 7 and brazing filler metal 15 for sealing." APPLE-1004, 7:51, 9:31-38, 16:38-40.

94. Nishiuma further describes a configuration of the package structure that includes "a heat conductive media of Au ribbons… in the space between the back of the semiconductor chip 10 … and the bottom of [the] cap 18 to cool the semiconductor chip 10 by conducting heat through the cap." *Id.*, 7:58-60, 11:18-24, 11:25-28 ("Both ends of the Au ribbons 22 are bonded to a heat conductive medium forming metallize 21 provided on the bottom of the cap 18[] …"), 11:29-12:37; FIG. 10. Nishiuma's sealing metallize 7, brazing filler 15, Au ribbons 22, and metallize 21 are provided to seal the semiconductor chip within the cavity of the ceramic dam frame, with the metallize 7 and filler 15 positioned between the

cap 18 and the ceramic dam frame 6 and the ribbons 22 and metallize 21 positioned between the cap 18 and chip 10. APPLE-1004, 7:51-53, 11:19-12:37; *cf.*, APPLE-1001, 6:50-57. Nishiuma describes that the sealing metallize 7 and brazing filler metal 15, optionally along with the Au ribbons 22 and metallize 21, cooperate together to seal and dissipate heat from the semiconductor chip. *See* APPLE-1004, 11:30-12:7 (describing "[t]he process for forming the heat conductive media of the semiconductor integrated circuit device"), FIGS. 11-14 (illustrating the steps of the process). Because Nishiuma describes that these components cooperate to connect the cap 18 to the frame and chip for a common purpose, a POSITA would have understood them as forming a layer (e.g., a "second … layer" as claimed). Nishiuma's sealing metallize and brazing filler metal, optionally along with the Au ribbons and metallize 21 on the bottom of the cap 18, provide a "***second conductive-pattern layer***" as claimed.

95. As shown in FIG. 10 below, Nishiuma's second conductive-pattern layer, including at least sealing metallize 7 and brazing filler metal 15, is positioned on the second surface of the dam frame 6 opposite the first surface that abuts the surface wiring 3, and thus is formed on the second surface of the insulating-material layer. APPLE-1004, FIG. 10. A POSITA also would have understood the Au ribbons as shown in FIG. 10 to be a variant of the same

embodiment of the device shown in FIG. 1 since the Au ribbons are an addition to the device depicted in FIG. 1.



APPLE-1004, FIG. 10 (annotated)

96. Nishiuma's metallize, brazing filler metal, and Au ribbons are all formed from electrically and thermally conductive metals. APPLE-1004, 11:36-42. For example, Nishiuma describes "sealing metallize 7 is a thick film of a refractory metal such as W plated with, for example, Ni and Au and the brazing filler metal 15 for sealing is made of, for example, Au—Sn alloy containing approx.. 20% Sn or hard solder." *Id.*, 7:56-61, 11:40-42. As described above, tungsten, nickel, and gold are all electrically conductive materials (*supra* §X.B.[1a] Ground 1A), and these materials also have acceptable thermal conductivities. APPLE-1035, 127-128, 133. For example, the electrical resistivity of tungsten is

about 5.3 x 10^{-8} Ω-m, for nickel it is about 0.95 x 10^{-7} Ω-m, and for gold 2.35 x 10^{-8} Ω-m. *Id.* The electrical resistivity of commercially pure tin is 1.11 x 10^{-7} Ω-m. *Id.*, 133. Resistivity is the inverse of conductivity, and thus a low resistivity indicates a material that readily allows an electrical current. *Id.*, 133, 12. Similarly, the thermal conductivity of these materials at room temperature is 315 W/m-K for gold, 155 W/m-K for tungsten, 70 W/m-K for nickel, 60.7 W/m-K for commercially pure tin. *Id.*, 127-128; *see also* APPLE-1004, 3:11-20 (describing Au ribbons as "heat conductive material"). A POSITA would have appreciated that the materials of the metallize, brazing filler metal, and Au ribbons are both electrically and thermally conductive.

97. Further, the metallize, brazing filler metal, and Au ribbons are patterned both to form a square shape around the perimeter of the cavity and a ribbon shape over the semiconductor chip. APPLE-1004, 11:36-42, FIG. 10. Nishiuma shows the cap with Au ribbons in FIG. 10, but also discloses that the cap include gold ribbons, wires or bumps. *Id.*, 3:11-13 The '527 patent is not specific about the type of conductivity that the conductive-pattern layer has, and a POSITA would have understood that electrical conductivity and thermal conductivity are both types of conductivity, and further that they are both types of conductivity that could be important to the preparation of a semiconductor device. Accordingly, the

metallize, brazing filler metal, and Au ribbons, having a pattern of material that is electrically and thermally conductive, provides a ***second conductive-pattern layer***.

98. To the extent it is argued that FIG. 10 represents an embodiment distinct from FIG. 1, it would nonetheless have been obvious to a POSITA to implement Nishiuma's cap with the heat conductive Au ribbons as described with regard to FIG. 10 in the FIG. 1 embodiment to "decrease the thermal resistance of the semiconductor chip" and prevent thermal stresses on the chip and the connection between the chip and the printed circuit board, as Nishiuma expressly describes. APPLE-1004, 11:64-12:37, 3:11-20. A POSITA would have had a reasonable expectation of success in implementing Nishiuma's semiconductor package structure with the Au ribbons and metallize shown in FIG. 10 because Nishiuma teaches that these embodiments are compatible, and because a POSITA would have understood that the addition of thermally conductive patterns to a cap of a semiconductor device package to dissipate heat is well-known in the art. APPLE-1004, 11:18-19 ("FIG. 10 shows a semiconductor integrated circuit device similar to the one shown in FIG. 1"), 3:11-20 ("A hermetically sealing cap can be included, preferably with a heat conductive material such as gold ribbons, gold wires, gold bumps [] bonded to the cap by a ribbon or wire bonding method [and t]he cap is encased over the semiconductor chip so that the heat conductive

material contacts the main surface of the semiconductor chip to transfer heat away from the chip through the heat conductive material and the cap."), 17:32-42; *see also* APPLE-1014, 19:44-54 (describing thermal management solutions for hermetically sealed semiconductor chip cavities, including cooling fins, heat transfer through cap, and heat sink attached to the chip), FIG. 26; APPLE-1015, 8:34-35 ("To further enhance the heat dissipating effect, a heat sink 39 is formed on the metal cap 28"), FIG. 11; APPLE-1016, [0144] ("the semiconductor die could be capped with a thermally conductive plastic or metal heat sink cap…[to] prevent[] contamination and dissipate heat"), [0145] ("As semiconductor designs become more powerful, heat dissipation becomes critical to the design of semiconductor packages"), [0146], FIGS. 4-5.

v. Claim 4

[4] The electronic module of claim 1, wherein the component is a microcircuit.

99. Nishiuma renders obvious claim [4]. For example, Nishiuma describes a "semiconductor integrated circuit device" formed as "a package structure fabricated by sealing a semiconductor chip 10 mounted on a wiring substrate 1 with a cap 18." APPLE-1004, Abstract, 6:66-7:2. Nishiuma's semiconductor chip (***component***) is a microcircuit that includes semiconductor material and an integrated circuit like the microcircuits described in the '527 patent

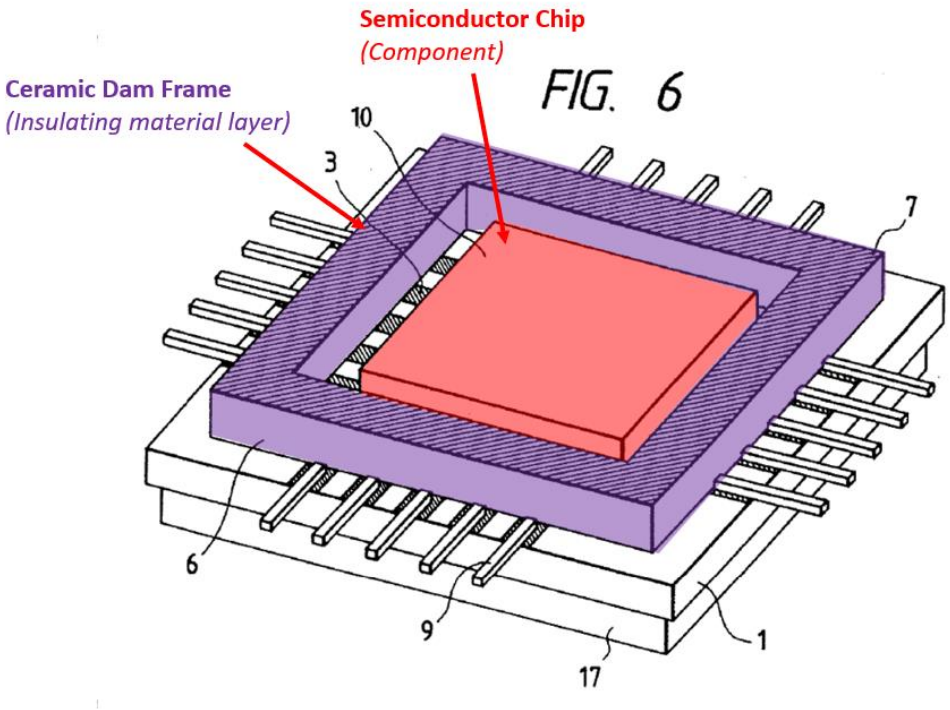
itself. For example, Nishiuma discloses that the component can be "a compound semiconductor chip made of[] … GaAs and having a semiconductor integrated circuit operated on radio frequencies." APPLE-1004, 17:23-30; *see also id.*, 7:2-6, 8:10-16.

100. Nishiuma's disclosure of a semiconductor chip with semiconductor integrated circuit is similar to the microcircuits that the '527 patent describes. For example, the '527 patent discusses that "the installation base in microcircuit manufacturing techniques, i.e., the substrate, is of a semiconductor material." APPLE-1001, 1:41-49. Indeed, a POSITA would have understood that "microcircuit" was a well-known term for "[a] miniaturized, electronic circuit, such as is found on an integrated circuit." APPLE-1032, 3; *see also* APPLE-1033, 3 (definition of 'microcircuit': "A synonym for integrated circuit (IC)"); APPLE-1031, 3 (including a definition of 'microcircuit' of "An integrated circuit"); APPLE-1017, 4:14-20 ("an electronic microcircuit card, of the type incorporating a contact assembly of package which has on one face a metal layer having the contacts of the card and which includes at least one integrated circuit."). Accordingly, Nishiuma's semiconductor chip with semiconductor integrated circuit provides a microcircuit.

vi. Claim 5

[5] The electronic module of claim 1, wherein the component is entirely protected inside the insulating-material layer.

101. Nishiuma renders obvious claim [5]. As described above, Nishiuma's semiconductor chip (e.g., chip 10) is sealed within a cavity formed in the ceramic dam frame. *Supra* §§X.B.[1e]-[1f-i] (Ground 1A); APPLE-1004, 66-7:2; 7:48-8:2, 18:1-5, FIGS. 1, 6. Nishiuma's semiconductor chip (***component***) is thus entirely protected inside the ceramic dam frame (***insulating-material layer***) as the dam frame surrounds the semiconductor chip and the semiconductor chip is also sealed between the printed wiring board and cap. APPLE-1004, FIGS. 1-4, 6-7, 9-13, 15-18, 38.



APPLE-1004, FIG. 6 (annotated)

102. Indeed, Nishiuma's disclosure of a semiconductor chip surrounded by a ceramic dam frame and sealed between a printed wiring board and the cap is similar to the '527 patent's description of what it means for a component to be "entirely protected" as claimed. For example, in the '527 patent's preferred embodiment shown in FIG. 4B below, the component 6 is positioned in a cavity 2 formed by the insulating-material 1.

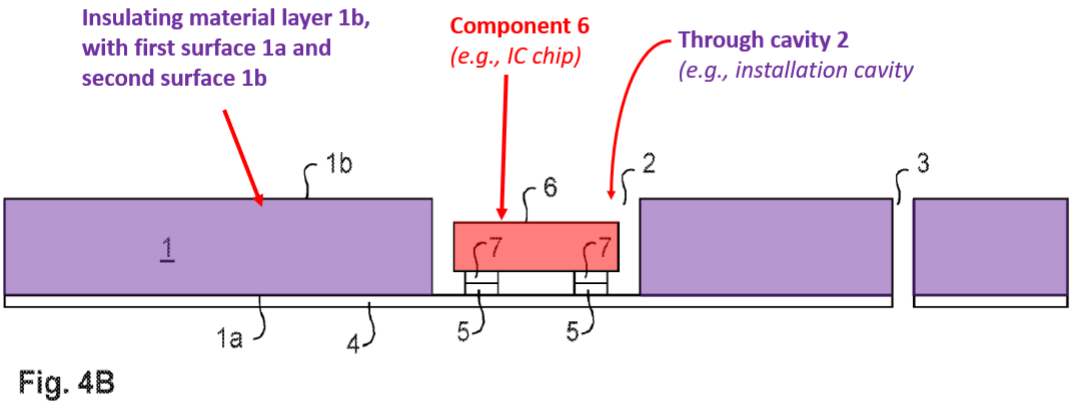
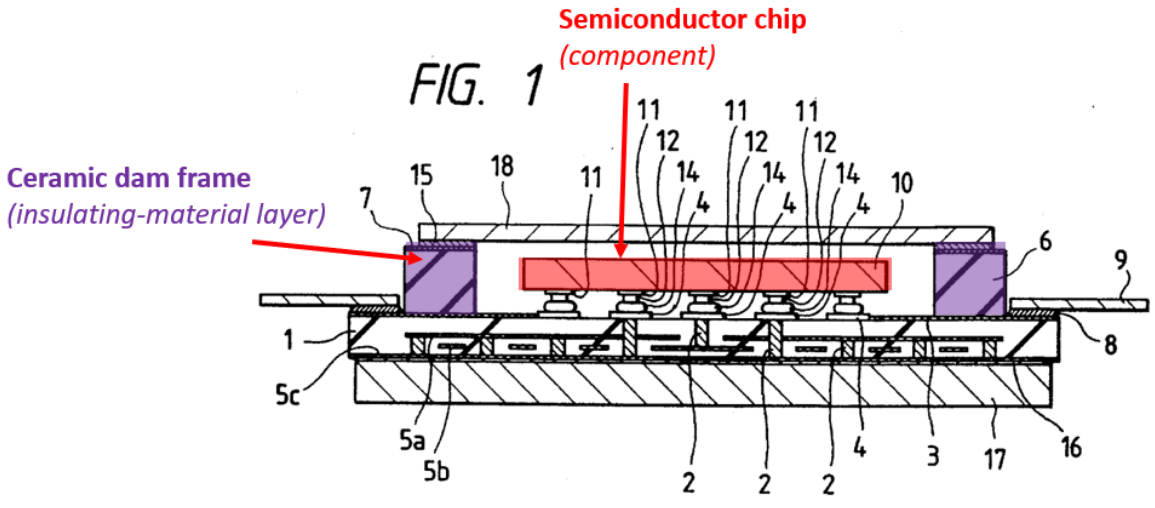


Fig. 4B

APPLE-1001, FIG. 4B (annotated)

103. Nishiuma's semiconductor chip is similarly surrounded by the ceramic dam frame, just as the component in the '527 patent is surrounded by insulating material, and is thus entirely protected inside the insulating-material layer. APPLE-1004, 66-7:2; 7:48-8: 5, FIGS. 1-4, 6-7, 9-13, 15-18, 38.



APPLE-1004, FIG. 1 (annotated)

vii. Claim 6

[6a] The electronic module of claim 1, wherein the insulating-material layer comprises a first surface and a second surface, the first surface being against the first conductive-pattern layer,

104. *See supra* §X.B.[2a] (Ground 1A Claim Element [2a]).

[6b] and the electronic module comprises a conductive film on the second surface of the insulating-material layer for protecting the component against electromagnetic radiation.

105. Nishiuma renders obvious claim element [6b]. For example, as described above, Nishiuma's device includes a cap 18 that is "bonded to the surface of the frame 6 through a sealing metallize 7 and brazing filler metal 15 for sealing." APPLE-1004, 7:51-54. "The sealing metallize 7 is of a thick film of a refractory metal such as W plated with, for example, Ni, and Au and the brazing filler metal 15 for sealing is made of, for example Au—Sn alloy containing approx. 20% Sn or hard solder." *Id.*, 7:55-59. "The cap 18 is of a metallic plate of, for example 42-alloy plated with Au." *Id.*, 7:58-60; *see also id.*, 7:48-60, 11:32-42, 11:56-62.

106. Nishiuma's description of the cap, sealing metallize, and brazing filler material is similar to the '527 patent's discussion of the conductive film. The '527

patent discusses that a "conductive film 9, can … be exploited in many ways, such as additional space for conductive patterns and to protect the components 6 and the entire module against electromagnetic radiation [or with] the aid of a second conductive film 9 the structure can be reinforced and warping of the installation base, for example, can be reduced." APPLE-1001, 7:40-46. Nishiuma's cap provides a space for a pattern of Au ribbons and seals the semiconductor chip within the ceramic dam frame, reinforcing the structure. APPLE-1004, 6:66-72, 7:48-54, 11:18-28, 11:43-62. Accordingly, Nishiuma's cap 18, sealing metallize 7, and brazing filler metal 15, whether taken individually or collectively, provide a "***conductive film***" on the second surface of the dam frame 6 (***insulating-material layer***).

107. Alternatively, and to the extent (i) element [6b] does not require direct contact between the conductive film and the second surface of the insulating-material layer or (ii) Nishiuma's dam frame 6 together with metallize 7 and brazing filler metal 15 are collectively taken as the claimed "***insulating-material layer***," cap 18 alone—or even just the Au plating on cap 18—each also constitutes a "***conductive film***" on the second surface of the insulating-material layer as claimed, since they are all formed of conductive materials. The '527 patent describes, for example, that a "metal film [] can also be a surfaced metal film, or

some other film including several layers or several materials" APPLE-1001, 6:27-29. Nishiuma's cap 18 or Au plating on the cap 18 provides a conductive film on the insulating-material layer, consistent with the '527 patent's treatment of the word 'film.'

108. The language in [6b] that recites "for protecting the component against electromagnetic radiation" is an intended use of the conductive film that imparts no additional structural limitation that would not already be met by a conductive film. Regardless, each of the structures described in the preceding paragraph – the cap 14, sealing metallize 7, and brazing filler metal 15; the cap alone; or the cap with the Au plating – that provide the claimed conductive film in Nishiuma do serve to protect the semiconductor chip (***component***) against electromagnetic radiation. Indeed, a POSITA would have understood and found obvious the metallic materials of Nishiuma's conductive film—such as the gold-plated copper cap—naturally protect the chip from electromagnetic radiation due to the EM shielding properties of the disclosed metals. APPLE-1018, 15:47-16:14; APPLE-1019, [0025].

109. For example, a POSITA would have been aware that the use of a metal layer positioned above an electronic module shields the component. APPLE-1018, 15:52-16:9 ("The metal layer provides a shield at the top surface" of

the module which is "preferably aluminum …[though o]ther metals… can be used"), 16:9-14 ("One micron of aluminum provides good hermetic protection plus some electromagnetic shielding, at reasonable cost. Depending on the severity of the electromagnetic environment, it may be desirable to substantially increase the thickness for effective shielding performance."); APPLE-1019, [0025] (describing of a "metallic cover layer" such as a "metallic cap… employed as shielding layers against electromagnetic radiation"). Kurita, for example, describes that it was well-known to use a metal plate with larger surface area than the semiconductor component, "connected to the ground potential" so that the "electromagnetic noise that would normally infiltrate into the semiconductor device 47 from outside the multi-layer substrate 65 is absorbed by the shield section 28 [so that the EM noise] does not penetrate into the semiconductor device 47." APPLE-1043, [0112], [0114]-[0116]. A POSITA would have found it obvious that Nishiuma's structures including the cap 14, sealing metallize 7, and brazing filler metal 15; the cap alone; or the cap with the Au plating, shield the component from electromagnetic radiation and thus "protect[] the component against electromagnetic radiation" as claimed.

viii. Claim 11

[11] The electronic module of claim 1 wherein the metallurgically electrical connection are ultrasonic or thermo-compression connections.

110. Nishiuma renders obvious claim [11]. For example, as explained above (*supra* §§X.B Ground 1A Elements [1b], [1d], [1f-ii]), Nishiuma describes that the Au balls 13 and 12 are bonded to the electrode pads of the component and to the surface wiring, respectively, by "using heat or ultrasonic energy or both" or a "thermo-compression bonding" (APPLE-1004, 8:19; *see also* 2:64-67, 10:56-60, 17:19-23) and that "[t]he wiring lands 4 of the printed wiring board 1 is electrically connected to the electrode pads 11 of the semiconductor chip 10 by bonding the Au lands 14 to the Au balls 12 by a thermo-compression bonding." *Id.*, 7:43-47, 2:60-3:21, 8:28-29, 4:10-12, 9:17-9:22, 8:17-19, 14:13-34, FIGS. 28a-c.

111. As also described above, Nishiuma's thermo-compression and ultrasonic bonding techniques result in a metallurgical and electrical connection in the same manner as described in the '527 Patent. APPLE-1001, 6:41-63; APPLE-1004, 8:17-19, 8:28-29, 9:13-26, 14:37-46.

ix. Claim 12

[12] The electronic module of claim 11 wherein the metallurgically electrical connections are facilitated by the presence of one or more metals selected from the group consisting of copper, aluminum, gold and tin.

112. Nishiuma renders obvious claim [12]. APPLE-1001, 6:41-49, 6:61-63, 6:50-54. For example, as explained above (*supra* §§X.B Ground 1A Elements [1b], [1d], [1f-ii]), Nishiuma describes how connections between the Au balls 13, Au balls 12, electrode pads, and surface wiring are achieved through ultrasonic connection or thermo-compression bonding techniques. APPLE-1004, 7:43-47, 2:60-3:21, 8:28-29, 4:10-12, 9:17-9:22, 8:17-19, 10:56-60, 17:19-2314:13-34, FIGS. 28a-c.

113. Nishiuma's Au balls 12, Au balls 13 and Au lands 14 are all formed from gold, and the connections involving Au balls 12, Au balls 13, Au lands 14 are thus all facilitated by the presence of gold. In particular, the use of gold in the Au balls 12 and 13 and Au lands would allow for simple connection of the gold material through the thermo compression and/or ultrasonic techniques described by Nishiuma. *Supra* §IV.B; APPLE-1020, 3:33-36 (describing that in thermocompression techniques "material flow [between the two members] is induced by the application of heat and pressure, which are maintained for a

suitable length of time so that adhesion takes place without the presence of a liquid phase.").

114. Accordingly, the connections between Nishiuma's Au balls 13, Au balls 12, electrode pads, and surface wiring formed through ultrasonic and/or thermocompression bonding techniques are facilitated by the presence of gold.

x. Claim 13

[13pre] An electronic module, comprising:

115. *See supra* §X.B.[1pre] (Ground 1A Element [1pre]).

[13a] a first conductive-pattern layer having a first surface,

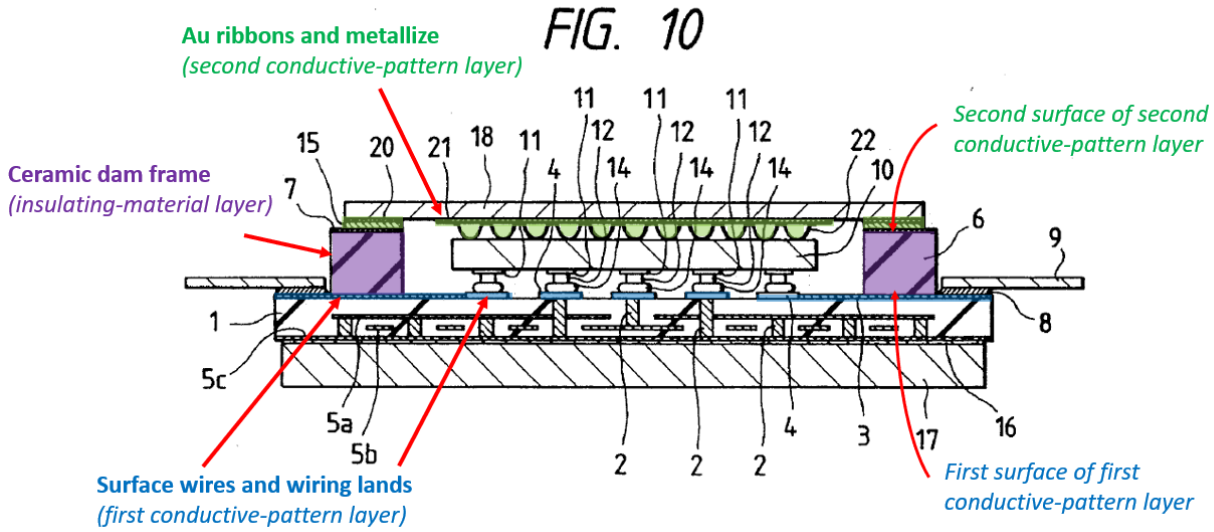
116. *See supra* §X.B.[1a] (Ground 1A Element [1a]).

[13b] a second conductive-pattern layer having a second surface,

117. *See supra* §X.B.[2b] (Ground 1A Claim [2b]). As described above, Nishiuma's sealing metallize and brazing filler metal, optionally along with the Au ribbons and metallize 21 on the bottom of the cap 18, provide a "***second conductive-pattern layer***" which has ***a second surface*** as claimed. APPLE-1004, 7:51-60, 9:31-38, 11:18-12:37, 16:38-40, FIG. 10.

[13c] an insulating-material layer between the first surface of the first conductive-pattern layer and the second surface of the second conductive-pattern layer,

118. *See supra* §§X.B (Ground 1A Element [1e], Claim [2a]-[2b]). As described above, Nishiuma's square dam frame is formed on the wiring board 1 (***"first conductive-pattern layer"***) and is covered by a cap "bonded to the surface of the frame 6 through a sealing metallize 7 and brazing filler metal 15 for sealing" (***"second conductive-pattern layer"***). APPLE-1004, 7:51; *see also id.*, 7:48-55, 8:5-9, 9:31-38, 16:38-40. As shown below in FIG. 10, Nishiuma's square dam frame ("insulating-material layer") is ***between the first surface of the first conductive-pattern layer and the second surface of the second conductive-pattern layer***, as claimed. APPLE-1004, FIG. 1.



APPLE-1004, FIG. 1 (annotated)

[13d] first solderless contact bumps made on the first surface of the first conductive-pattern layer and metallurgically and electrically connected thereto,

119. *See supra* §X.B.[1b] (Ground 1A Element [1b]).

[13e] a component having fiat contact zones embedded in the insulating-material layer,

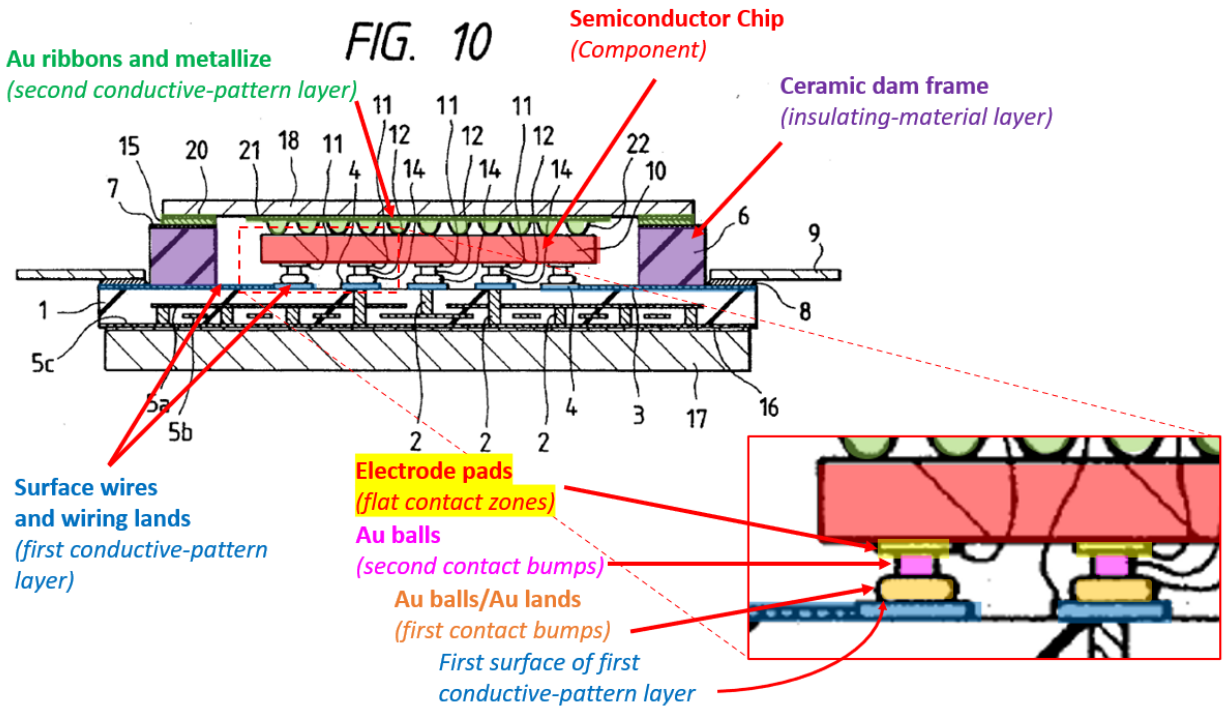
120. *See supra* §§X.B.[1c], [1f-i] (Ground 1A Elements [1c] and [1f-i]).

[13f] second solderless contact bumps made on the flat contact zones and metallurgically and electrical connected thereto, and

121. *See supra* §X.B.[1d] (Ground 1A Element [1d]).

[13g] wherein the flat contact zones of the component are metallurgically, electrically and solderlessly connected to the first solderless contact bumps made on the first surface of the first conductive-pattern layer by means of the second solderless contact bumps made on said flat contact zones.

122. *See supra* §X.B.[1f-i]-[1f-ii] (Ground 1A Elements [1f-i]-[1f-ii]). As described above, Nishiuma describes that "[t]he wiring lands 4 of the printed wiring board 1 is electrically connected to the electrode pads 11 of the semiconductor chip 10 by bonding the Au lands 14 to the Au balls 12 by a thermo-compression bonding." *Id.*, 7:43-47, 10:34-43.



APPLE-1004, FIG. 10 (modified to include closeup, annotated)

123. Accordingly, Nishiuma describes that the electrode pads (***flat contact zones***) are metallurgically, electrically and solderlessly connected to the Au lands 14 (***first solderless contact bumps***) by the Au balls 12 (***second solderless contact bumps***), as shown in FIG. 10. *Supra*, §X.B.[1f-ii] (Ground 1A Element [1f-ii]).

xi. Claim 15

[15] The electronic module of claim 14, wherein the component is a microcircuit.

124. *See supra* §X.B.[4] (Ground 1A Claim [4]).

xii. Claim 16

[16] The electronic module of claim 13, wherein the second conductive-pattern layer is configured to protect the component against electromagnetic radiation.

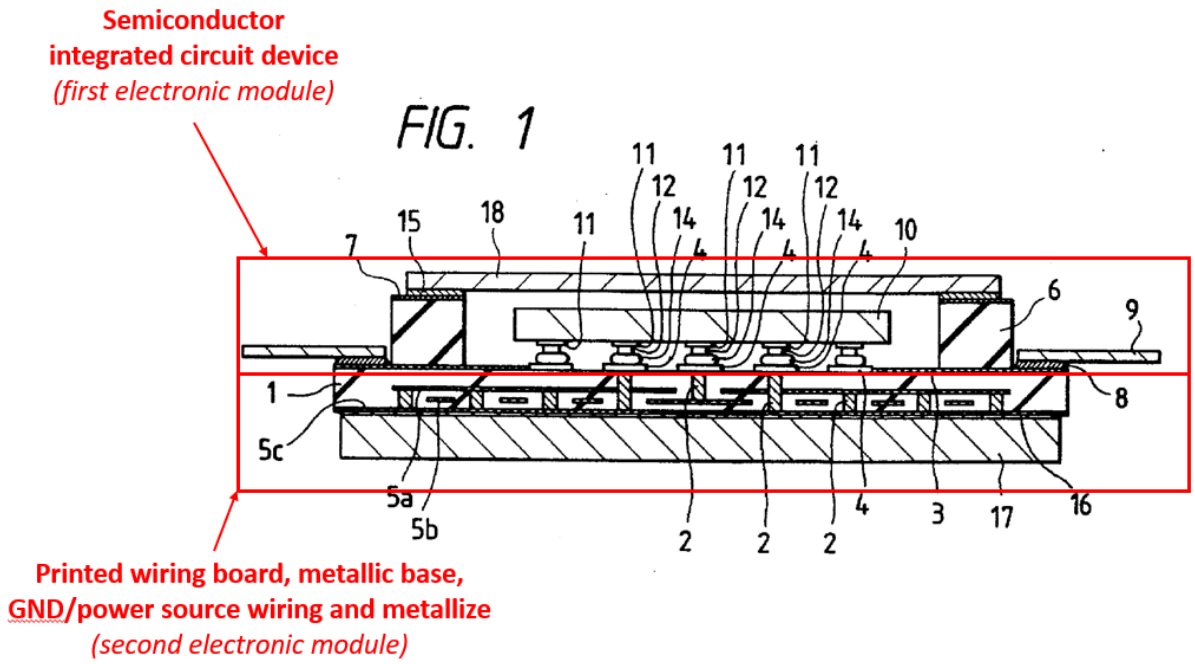
125. *See supra* §X.B.[6b] (Ground 1A Claim [6b]). As described above with respect to element [6b], Nishiuma's sealing metallize and brazing filler metal, and optionally or alternatively the metallize 21 on the bottom of the cap 18, are configured to protect the semiconductor chip (***"component"***) from electromagnetic radiation. APPLE-1004, 7:48-60, 11:32-42, 11:56-62; *see also* APPLE-1018, 15:47-16:14; APPLE-1019, [0025], APPLE-1043, [0112], [0114]-[0116].

xiii. Claim 19

[19pre] A multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein at least one of the modules of said plurality comprises:

126. The preamble of claim 19 is not limiting on the elements of the claim. However, to the extent the preamble is limiting, Nishiuma renders [19pre] obvious. As described above, Nishiuma's semiconductor integrated circuit device including a semiconductor chip provides an electronic module. *Supra* §X.B.[1pre] (Ground 1A Element [1pre]); APPLE-1004, 6:66-7:2.

127. Nishiuma's printed wiring board "in which the GND wiring 5a and the power source wiring 5b are formed," optionally with the GND metallize 5c and/or metallic base 17, provides a second electronic module on which the semiconductor chip is attached. APPLE-1004, 6:66-7:2 ("the semiconductor integrated circuit device of this embodiment has a package structure fabricated by sealing semiconductor chip 10 mounted on a wiring substrate 1 with a cap 18."). Indeed, the '527 patent permits this mapping of the Nishiuma reference by providing a broad definition of an electronic module, discussing that an electronic module "can be a module like a circuit board, which includes several components [such as] semiconductor components." APPLE-1001, 1:18-23.



APPLE-1004, FIG. 1 (annotated)

128. For purposes of the mappings to the elements of claim 19, Nishiuma's semiconductor integrated circuit device including semiconductor chip (a first ***"electronic module"***) mounted on a printed circuit board (a second ***"electronic module"***) comprises ***a multi-layered electronic module***, and at least the first electronic module includes the features described in the limitations of claim 19, as claimed ("wherein at least one of the modules of said plurality comprises…").

[19a] a first conductive-pattern layer having a first surface,

129. *See supra* §X.B.[1a] (Ground 1A Element [1a]).

[19b] first solderless contact bumps made on the first surface of the first conductive-pattern layer,

130. *See supra* §X.B.[1b] (Ground 1A Element [1b]).

[19c] an insulating-material layer on the first surface of the first conductive-pattern layer, and

131. *See supra* §X.B.[1e] (Ground 1A Element [1e]).

[19d] a component embedded in the insulating-material layer and having flat contact zones,

132. *See supra* §§X.B.[1c], [1f-i] (Ground 1A Elements [1c] and [1f-i]).

[19e] second solderless contact bumps made on the flat contact zones of the component,

133. *See supra* §X.B.[1d] (Ground 1A Element [1d]).

[19f] wherein, the flat contact zones of the component are metallurgically and electrically connected to the first conductive-pattern layer via the first solderless contact bumps made on the first surface of the first conductive-pattern layer and the second solderless contact bumps made on the flat contact zones of the component.

134. *See supra* §X.B.[1f-ii] (Ground 1A Element [1f-ii]).

xiv. Claim 21

[21] The multi-layered electronic module according to claim 19, wherein the electronic modules are electrically connected to each other in order to form a multilayered functioning totality.

135. As described above, Nishiuma's semiconductor chip is attached to Nishiuma's printed wiring board. *Supra* §§X.B.[1pre], [19pre] (Ground 1A Elements [1pre] and [19pre]); *see e.g.*, APPLE-1004, 6:66-7:2 ("the semiconductor integrated circuit device of this embodiment has a package structure fabricated by sealing semiconductor chip 10 mounted on a wiring substrate 1 with a cap 18."). As also described above, in the mapping of claim 22, Nishiuma's semiconductor

integrated circuit device including semiconductor chip provides a first *"**electronic module**"* and is mounted on a printed circuit board which provides a second *"**electronic module**."*

136. Nishiuma's semiconductor chip is electrically connected to the GND and power wiring of the printed wiring board through the through-holes 2. APPLE-1004, 7:16-24 ("surface wirings 3 are wirings for input/output signals, GND, and power source, one end of each wirings is connected to one of the wiring lands 4. The wiring for GND is electrically connected to the GND wiring 5a thought a through-hole 2 and the wiring for power source is electrically connected to the power source wiring 5b through the through-holes 2."). Accordingly, in this mapping, the semiconductor chip (a first ***electronic module***) is ***electrically connected*** to the printed wiring board (a second ***electronic module***) to form Nishiuma's full semiconductor integrated circuit device—that is, ***a multilayered functioning totality***.

xv. Claim 25

[25pre] A multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein at least one of the modules of said plurality comprises:

137. *See supra* §X.B.[19pre] (Ground 1A Element [19pre]).

[25a] a first conductive-pattern layer having a first surface,

138. *See supra* §X.B.[1a] (Ground 1A Element [1a]).

[25b] a second conductive-pattern layer having a second surface,

139. *See supra* §§X.B.[2a]-[2b], [13b] (Ground 1A Claim [2a]-[2b], Element [13b]).

[25c] an insulating-material layer between the first surface of the first conductive-pattern layer and the second surface of the second conductive-pattern layer,

140. *See supra* §§X.B.[1e], [2a]-[2b], [13c] (Ground 1A Element [1e], Claim [2a]-[2b], Element [13c]).

[25d] first solid contact bumps solderlessly made on the first surface of the first conductive-pattern layer and metallurgically and electrically connected thereto,

141. *See supra* §X.B.[1b] (Ground 1A Element [1b]).

[25e] a component having flat contact zones embedded in the insulating-material layer,

142. *See supra* §§X.B.[1c], [1f-i] (Ground 1A Elements [1c] and [1f-i]).

[25f] second solid contact bump solderlessly made on the flat contact zones and metallurgically and electrically connected thereto, and

143. *See supra* §X.B.[1d] (Ground 1A Element [1d]).

[25g] wherein the first solid contact bumps such that the flat contact zones of the component are metallurgically and electrically connected to the first conductive pattern layer via respective first and second solid contact bumps.

144. *See supra* §X.B.[1f-ii] (Ground 1A Element [1f-ii]).

xvi. Claim 27

[27] The multi-layered electronic module according to claim 25, wherein the electronic modules are electrically connected to each other in order to form a multi-layered functioning totality.

145. *See supra* §X.B.[21] (Ground 1A Claim [21]).

XI. GROUND 1B – NISHIUMA-NAKATANI RENDERS OBVIOUS CLAIMS 7-8 AND 17-18

A. Nakatani Overview (APPLE-1007)

146. Nakatani describes "a conventional surface acoustic wave device built-in module" which may include multiple devices. APPLE-1007, [0016], [0024], Abstract, [0118], [0123], [0127]. For example, Nakatani's FIG. 7 shows the conventional device having a circuit board 607, first wiring patterns 609, second wiring patterns 610, via holes 611, and two surface acoustic wave devices 601 positioned within a concave portion 615. APPLE-1007, [0017], [0019], [0118]-[0119], [0124]-[0135], FIGS. 5, 6A-C.

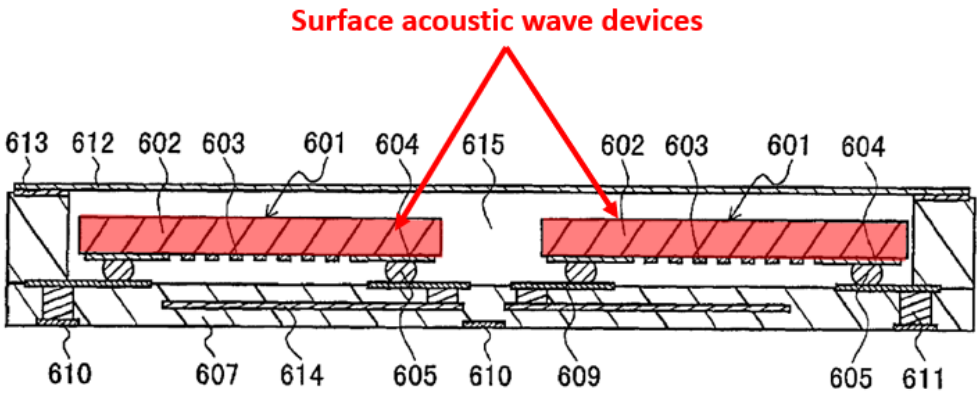


FIG . 7
PRIOR ART

APPLE-1007, FIG. 7

B. Combination of Nishiuma and Nakatani

147. Nishiuma describes that "semiconductor device components, including the capacitors[,] can be mounted on the surface of the printed wiring substrate." APPLE-1004, 4:37-40, 9:65-10:3 ("because it is also possible to mount chip parts including capacitors on the surface of the printed wiring board 1…"). A POSITA would have understood from Nishiuma's description of "components" and "chip parts" mounted on the printed wiring board, that Nishiuma describes the use of multiple components within a cavity on a wiring board. Although Nishiuma does not show the use of multiple components in any figures, Nishiuma suggests

that multiple components can be connected to the wiring substrate but provides few details in this regard.

148. A POSITA would have looked to references like Nakatani to investigate the option of mounting additional IC chips or other components in an installation cavity similar to Nishiuma's. APPLE-1007, [0018]-[0020], [0118], [0127] FIGS. 5-7; *supra*, §XI.A. For example, as described above, Nakatani describes modules that include multiple semiconductor chips or other electronic elements. APPLE-1007, Title ("Module with Built-In Electronic Elements and Method of Manufacture Thereof"), Abstract ("At least two electric elements (203) such as semiconductor chips or surface acoustic wave devices are mounted on wiring patterns (201)"), [0016] ("a structure of a conventional surface acoustic wave device built-in module including two surface acoustic wave devices"), [0072] ("semiconductor chips are contained in electric elements"), [0086], FIGS. 5-7.

149. It would have been obvious to implement Nishiuma's device in accordance with Nakatani's suggestion for mounting not just one but multiple IC chips in an installation cavity such that the IC chips would be electrically connected via a conductive pattern-layer. Multiple reasons would have prompted a POSITA to pursue this combination before the Critical Date. *Id.*

150. First, a POSITA would have been motivated to mount additional IC chips like Nishiuma's semiconductor chips 10 or Nakatani's surface acoustic wave ("SAW") chips in the cavity of Nishiuma's electronic module to expand the capabilities and overall processing power of the module. By adding additional components, such as additional semiconductor chips, to the module, the processing power associated with the module would be increased (for example, potentially doubled by the inclusion of two semiconductor chips as compared to one). Alternatively, adding additional components could also be used to add functionalities to a module based on the selection of which components to be added. While a single semiconductor chip would provide a certain amount of functionality and processing power, the ability to mount additional chips in the cavity of the same module as taught in Nakatani would advantageously support an increase in the functionality and/or processing power of the module through inclusion of additional chip(s).

151. Second, a POSITA would have been motivated to mount additional IC chips like Nishiuma's semiconductor chips 10 or Nakatani's SAW chips in the cavity of Nishiuma's electronic module because the "demand for higher performance and miniaturization of electronic equipment" has increased the desire for "higher density and higher function[ing]" semiconductor packages. APPLE-

1007, [0002]-[0003], [0027], [0075]. A POSITA would have understood the drive to increase the density of components in a module and optimize performance through increased functionalities, and would have been motivated to implement Nishiuma's semiconductor integrated circuit device with Nakatani's teaching to include multiple components as a result. Nakatani describes that the semiconductor package's thickness is improved and the package is more compact by having multiple thin chips mounted on a substrate. APPLE-1007, [0001], [0024]-[0025], [0027].

152. Third, providing additional IC chips in the cavity of Nishiuma's electronic module would have been obvious as a predictable application of a known technique of implementing multiple components in a module as taught by Nakatani to a known system as taught by Nishiuma to achieve entirely predictable results. As described above, the use of multiple components in a module was well-known by the Critical Date. *Supra* §IV.A; *see also, e.g.,* APPLE-1041, FIG. 12; APPLE-1039, FIG. 1.

153. Fourth, the combination would have been obvious because it involves the mere duplication of parts without no new or unexpected result. The addition of multiple components withing the cavity only requires adjusting a size of the cavity to accommodate more components as was conventional by the Critical Date.

Supra §IV.A. The additional components would have been coupled within the cavity in the same way as the first component, and a POSITA would have understood that there is no unexpected result in doing so.

154. The effect of having a plurality of Nishiuma's components would have been a predictable design choice to increase an ultra-thin semiconductor module's capability, and such design choice would have been well within the skill of the POSITA as shown by Nakatani. For example, a POSITA would have understood that the spacing between the components determines thermal interactions between the components, and that heat flow between components is calculated from the thermal conductivity of the module multiplied by the temperature gradient between hot and cool chips. It would have been well within the level of skill of the POSITA to determine an appropriate spacing between the components to keep heat transport low so as not to impede functionality of the components. The required spacing between components to avoid unintended results from thermal interactions are based on well-established engineering principles that a POSITA would have understood.

155. A POSITA would have reasonably expected success implementing the combination for all of the reasons described above, especially given that Nakatani describes coupling electronic components in a similar cavity and using a similar

technique as described by Nishiuma. APPLE-1004, 2:60-67, 8:16-9:21; Figs. 1, 39; APPLE-1007, [0016]-[0023], [0118]-[0126], FIGS. 5-7. A POSITA would have reasonably expected success in implementing the combination because, as explained above, the addition of multiple components, as taught by Nakatani, to a cavity, as taught by Nishiuma, would simply require the application of well-known engineering principles to determine appropriate spacing and positioning of the components, which would have been well within the level of skill of the POSITA.

C. Analysis

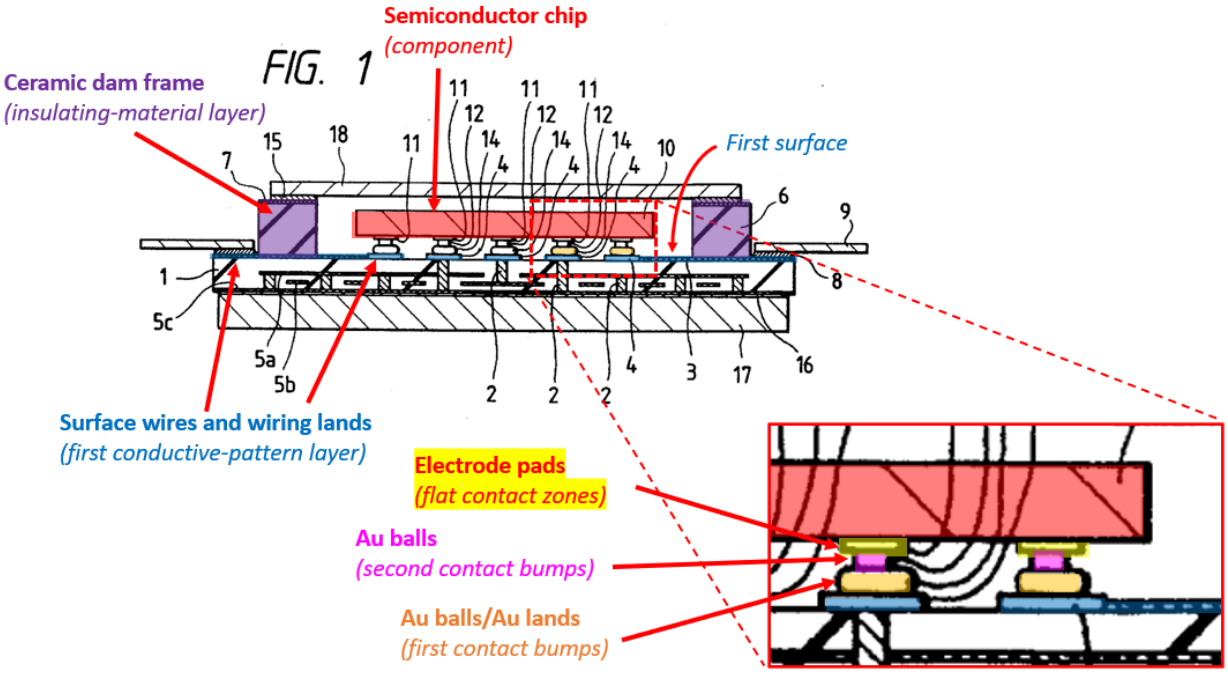
i. Claim 7

[7] The electronic module of claim 1, comprising a plurality of components having flat contact zones metallurgically and electrically connected to the first solid contact bumps made on the first surface of the first conductive-pattern layer by means of said second solid contact bumps.

156. Nishiuma-Nakatani renders obvious claim [7]. For example, in the combination, Nishiuma's device predictably includes at least two IC chips based on Nakatani's suggestion. *Supra* §XI.B. Accordingly, in the combination, the module includes ***a plurality of components***, as claimed.

157. Nishiuma's techniques for mounting a single semiconductor chip 10 in the cavity is therefore predictably extended to each of the multiple IC chips (***plurality of components***) in the module. As explained above (*see* §X.B Ground

1A Elements of Claim 1), each chip includes electrode pads (***flat contact zones***) electrically connected to Au lands (***first solid contact bumps***) on the printed wiring substrate (***first conductive-pattern layer***) by Au balls 12 (***second solid contact bumps***) so that each chip realizes the benefits of the connections described for a single chip in Nishiuma. *Supra* §XI.B (Nishiuma-Nakatani Combination); APPLE-1004, 2:60-67, 8:16-9:21, 4:37-40, 9:65-10:3, Figs. 1, 39; APPLE-1007, [0026] ("at least two electric elements (203) such as semiconductor chips or surface acoustic wave devices… mounted on wiring patterns"), [0127] ("a plurality of the surface acoustic wave devices 501 … may be mounted together"), [0016]-[0023], FIGS. 4-7.



APPLE-1004, FIG. 1 (modified to include closeup, annotated)[2]

[2] Nishiuma's FIG. 1 shows only one semiconductor chip in the cavity, however, in the combination each of the multiple semiconductor chips is coupled to the wiring board in the same way described by Nishiuma and shown in FIG. 1.

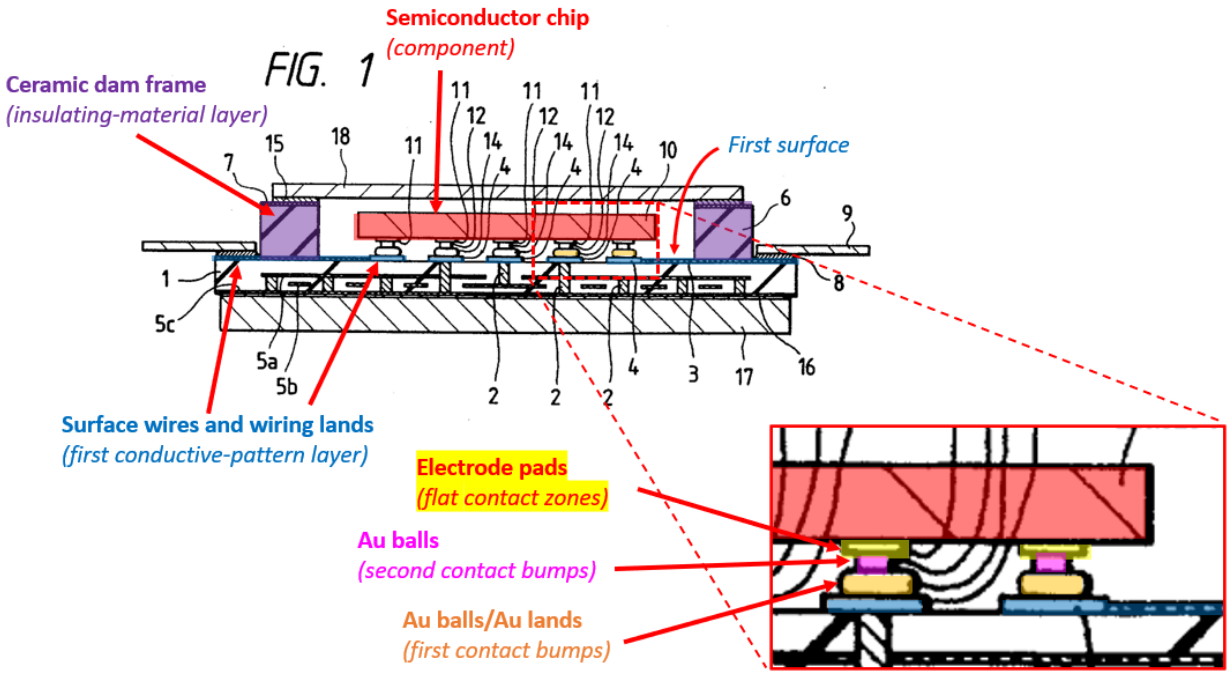
ii. Claim 8

[8] The electronic module of claim 7, wherein the plurality of components are electrically connected to each other by means of the first conductive-pattern layer.

158. Nishiuma-Nakatani renders obvious claim [8]. For example, in the combination, Nishiuma's device predictably includes at least two IC chips based on Nakatani's suggestion, which are each connected to the printed wiring substrate, and thus electrically connected to each other. *Supra* §XI.B (Nishiuma-Nakatani Combination); APPLE-1004, 1:11-17, 2:36-50, 4:37-40, 7:38-47, 9:13-25; Figs. 1, 39; APPLE-1007, [0019] ("A plurality of surface acoustic wave device 601 built into the module shown in FIG. 7 and the external circuit are connected via [first and second wiring patterns, internal circuit and via holes]"), [0020] ("After the surface acoustic wave devices 601 are positioned and placed on the circuit board 607, the first wiring patterns 609 and the metal bumps 605 are electrically connected"), [0028], [0127], FIGS. 4-7.

159. Consistent with Nakatani's teachings, the plurality of IC chips in the combination would be electrically connected to each other by means of the surface wiring, as Nishiuma teaches. For example, Nishiuma's FIG. 1 shows the

mechanism by which a semiconductor chip is connected to the surface wiring and wiring lands (first conductive-pattern layer).



APPLE-1004, FIG. 1 (modified to include closeup, annotated)[3]

160. It would have been obvious to a POSITA that both semiconductor chips in the combination would be coupled to the surface wiring and wiring lands (first conductive-pattern layer), and would thus be electrically connected to one another by means of the first conductive-pattern layer. Electrically connecting the

[3] Nishiuma's FIG. 1 shows only one semiconductor chip in the cavity, however, in the combination each of the multiple semiconductor chips is coupled to the wiring board in the same way described by Nishiuma and shown in FIG. 1.

multiple semiconductor chips to each other would also allow the improvement in functionality of the device, as taught by Nakatani. APPLE-1007, [0002]-[0003], [0024]-[0027], [0075].

161. A POSITA also would have found provision of an electrical connection between a pair of IC chips to be an obvious design choice that would be readily achieved using the conventional wiring patterns and interconnection techniques described in each of Nakatani and Nishiuma. APPLE-1004, 7:16-26. For example, a POSITA would have electrically connected the IC chips in the combination to facilitate communication of data signals between the chips, which was well-known by the Critical Date. *Supra* §IV.A.

iii. Claim 17

[17] The electronic module of claim 13, comprising a plurality of components having flat contact zones and second solderless contact bumps made on the flat contact zones, the flat contact zones being metallurgically and electrically connected to the first contact bumps made on the first surface of the first conductive-pattern layer by means of said second solderless contact bumps.

162. *See supra* §XI.C.[7] (Ground 1B Claim [7]).

iv. Claim 18

[18] The electronic module of claim 17, wherein the plurality of components includes at least one microcircuit, and the plurality of components are electrically connected to each other by means of the first conductive-pattern layer.

163. *See supra* §X.B.[4] (Ground 1A Claim [4]), §XI.C.[8] (Ground 1B Claim [8]). For the same reasons described above in Ground 1A, in the Nishiuma-Nakatani combination at least one of the plurality of components is a microcircuit, and further as described with respect to claim 8, the components in the combination are electrically connected to each other by means of the first conductive-pattern layer.

XII. GROUND 1C – NISHIUMA-NAKATANI-YONEYAMA RENDERS OBVIOUS CLAIMS 20 AND 26

A. Combination of Nishiuma, Nakatani and Yoneyama

164. Nishiuma describes a multi-layered electronic module including a printed wiring board "in which the GND wiring 5a and the power source wiring 5b are formed," optionally with the GND metallize 5c and/or metallic base 17 (one "electronic module") on which a semiconductor chip (another "electronic module") is attached. *Supra* §X.B.[19pre] (element [19pre]); APPLE-1004, 6:66-7:2, FIGS. 1, 9-10, 18. Nishiuma describes an integrated circuit device, but is not specific as

to the function of the device. APPLE-1004, title ("Semiconductor integrated circuit device…"), 6:66-7:6, 8:10-12.

165. A POSITA would have looked to references like Yoneyama (*see infra* §XIV.A) to investigate potential functions of integrated circuit devices, including memory circuits. APPLE-1013, [0018]. For example, Yoneyama describes a multi-component structure using "identical IC chips" has "a potential future application [] in memory modules." *Id.* It would have been obvious to implement Nishiuma-Nakatani's device in accordance with Yoneyama's suggestion to implement multiple integrated circuit devices as memory circuits. Multiple reasons would have prompted a POSITA to pursue this combination before the Critical Date.

166. First, a POSITA would have recognized that it was obvious to try to implement Nishiuma-Nakatani's integrated circuits as memory circuits, as Yoneyama teaches, because a memory circuit is one of a limited number of broad (and well-known) classes of possible functions of the integrated circuit. APPLE-1013, [0018]; APPLE-1032, 4 (second type of chip listed under "Types of Chips by Function"). A POSITA would have understood that the semiconductor chips and integrated circuit chips described by both Nishiuma and Yoneyama have applications "as processors and memory in computers and countless consumer and

industrial products," and it would have been obvious to a POSITA to implement the chips as memory as a result. APPLE-1032, 4 (definition of "chip"); APPLE-1017, 2:37-40.

167. Second, a POSITA would have understood that Nishiuma's flip chip bonding techniques would have provided high-connection density and improved electrical performance to a memory circuit and would have found it obvious to implement Nishiuma-Nakatani's integrated circuits as memory circuits for this reason. Nishiuma's flip-chip bonding technique provides high connection density through the bumps patterned on the chip and substrate which allow for faster operating speed. APPLE-1004, 2:38-54 ("decreasing transmission loss of high-frequency signal due to the wiring structure of a printed wiring board or substrate…improving the reliability of connection…decreasing thermal resistance of a semiconductor chip"), 1:18-33. A POSITA would have recognized that memory circuits benefit from high connection density, and would have been motivated to implement Nishiuma-Nakatani's integrated circuits as memory circuits as a result.

168. Third, implementing integrated circuits as multiple memory circuits as taught by Yoneyama would have been obvious as a predictable application of a known technique of implementing memory circuits to a known system as taught by

Nishiuma-Nakatani to achieve entirely predictable results of a semiconductor device with memory circuits. Indeed, semiconductor chips like Nishiuma's commonly included multiple memory circuits (e.g., registers, cache, RAM) to facilitate efficient data retrieval and processing before the Critical Date. *See e.g.*, APPLE-1032, 4. A POSITA would have understood that memory circuits were well-known and conventional by the Critical Date and would have further understood that implementing Nishiuma-Nakatani's multi-module system as memory circuits would have only required a simple arrangement of elements without substantial changes to the Nishiuma-Nakatani device.

169. A POSITA would have reasonably expected success implementing the combination for all of the reasons described above.

B. Analysis

v. Claim 20

[20] The multi-layered electronic module according to the claim 19, comprising a plurality of memory circuits.

170. Nishiuma-Nakatani-Yoneyama renders claim [20] obvious. For example, in the combination, multiple integrated circuits, as taught by Nishiuma and Nakatani, are implemented as memory circuits, as suggested by Yoneyama. *Supra* §XII.A (Nishiuma-Nakatani-Yoneyama Combination); APPLE-1013, [0018]. For example, each semiconductor chip positioned in the cavity and

connected to the printed wiring board, as Nishiuma teaches, would be implemented as a memory circuit, as Yoneyama suggests.

171. Accordingly, Nishiuma-Nakatani-Yoneyama renders obvious a multi-layered electronic module comprising a plurality of memory circuits, as claimed.

vi. Claim 26

[26] The multi-layered electronic module according to claim 25, comprising a plurality of memory circuits.

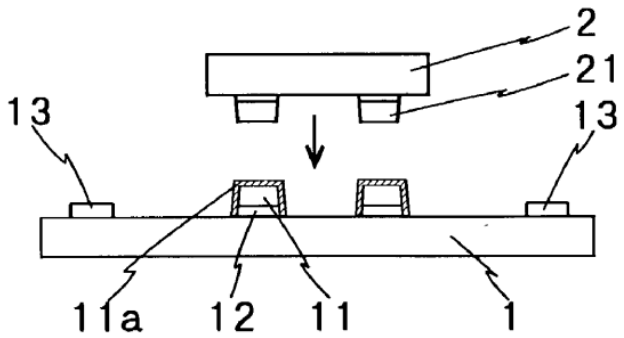
172. *See supra* §XII.B.[20] (Ground 1C Claim [20]).

XIII. GROUND 1D – NISHIUMA-SHIBATA RENDERS OBVIOUS CLAIMS 3 AND 14

A. Shibata Overview (APPLE-1005)

173. Shibata describes a method for coupling semiconductor chips using a bump electrode formed on an electrode terminal of the semiconductor chip. APPLE-1005, [0011]. Shibata's bump electrodes use metals with a relatively low melting point to alloy one metal with another inside the bump to prevent adverse effects from high temperature on the semiconductor elements. APPLE-1005, [0011].

FIG. 1B



APPLE-1005, FIG. 1B

174. Shibata describes that the first and second bump electrodes 11 and 21 can be joined by "a third metal layer having a lower melting point" which "melts at a relatively low temperature and diffuses into the bump electrode or the electrode terminal to thereby provide diffusive joining." *Id.*, [0014], [0032] ("it is preferable that the metals are made of Au and the low-melting point metal layer is made of Sn or an Au—Sn alloy"), [0082]. For example, in FIG. 1B, above, "[a]n Sn coating 11a is provided on the bump electrode 11 made of Au." *Id.*, [0053].

B. Combination of Nishiuma and Shibata

175. Nishiuma describes techniques for solderlessly bonding the electrodes of a semiconductor chip to a printed wiring board using Au balls. APPLE-1004, 7:43-47, 9:13-22, FIG. 1. A POSITA would have understood that connections between components and substrates may be improved by the addition of other

metals to promote joining or to absorb thermal stresses between the component and substrate and would have looked to similar references like Shibata for details about how to implement such additional metal layers. APPLE-1005, [0060], [0014], [0022], [0084].

176. Shibata describes using layers of metals with low melting-points between the contact bumps to improve the connection between the bumps. APPLE-1005, [0053], [0011]-[0014], [0032], [0074]. For example, Shibata describes that joining the bumps by alloying provide a highly reliable semiconductor device that will not separate the bumps when they are heated during other stages of the manufacturing process. *Id.*, [0060]. A POSITA would have been motivated to implement Nishiuma's semiconductor device with Shibata's teachings to join gold contact bumps using a layer of low melting-temperature material to improve the diffusive joining between the contact bumps. APPLE-1005, [0014], [0022], [0084], [0074].

177. In the Nishiuma-Shibata combination, a semiconductor integrated circuit device, per Nishiuma, is implemented with an additional metal layer on at least one contact bump, as Shibata teaches to improve the connection between the contact bumps. APPLE-1004, 8:10-9:16, FIG. 1; APPLE-1005, [0053], [0011]-

[0014], [0032]. A POSITA would have been motivated to implement this combination for multiple reasons.

178. First, a POSITA would have understood that the addition of a metal layer between the contact bumps, as taught by Shibata, improves the connection between the bumps by improving the diffusive joining of the component to the surface wiring through the bumps and absorbing thermal stresses. APPLE-1005, [0014] ("rather than directly forming an alloy with the bump electrode or the electrode terminal, by providing, for example, the third metal layer having a low melting point such as the alloy formed by the first and second metal, the third metal layer melts at a relatively low temperature and diffuses into the bump electrode or the electrode terminal to thereby provide diffusive joining"), [0022] ("the low-melting point metal layer includes a joining portion which at least partially has an alloy formed thereon due to alloying of the first and second metal or a boundary portion which is joined in a diffusive manner owing to the provision of the third metal"), [0060] (use of metal layers in bonding contact bumps "leads to very high reliabilities of the semiconductor device"), [0074], [0084]; APPLE-1004, 10:57-11:18.

179. Second, a POSITA would have understood from Nishiuma's disclosure that multiple layers of gold balls can be used in forming the contact

bump to absorb height differences that Shibata's method of using an additional metal layer between gold balls would be complementary to Nishiuma's method. APPLE-1004, 10:57-11:12, 13:5-10, FIG. 9. Nishiuma describes that in some cases a "height variation" of wiring lands "can be absorbed by the deformation of the Au balls 12a and 12b" along with the deformation of Au balls 13. *Id.*, 11:5-8. By using multiple layers of stacked Au balls (12a and 12b in FIG. 9), these differences in height can be accommodated during the thermocompression bonding procedure to provide reliable connection between the semiconductor and the lands. *Id.* Similarly, Shibata's teaching to use an additional metal layer between the contact bumps would also have the effect of limiting any impact of height variations in the wiring lands or contact bumps. *See* APPLE-1005, FIGS. 1B-4, 12.

180. Third, implementing an additional metal layer on at least one of the contact bumps in the combination would have been obvious as a predictable application of a known technique of using additional metals to improve the connection between contact bumps as taught by Shibata to a known system as taught by Nishiuma to achieve entirely predictable results. A POSITA would have understood that the addition of layers of metal materials between wiring patterns and a component to be electrically connected to a substrate were well-known and

conventional by the Critical Date. Such material layers were conventionally added for a variety of reasons including improved bonding, reducing cost, and improving conductivity. *See e.g.,* APPLE-1020, 2:56-3:11. Because such layers were conventional, a POSITA would have understood that the addition of a metal layer on Nishiuma's contact bump would have simply been the implementation of a known method as taught by Shibata.

181. The combination further would have been obvious and a POSITA would have had a reasonable expectation of success implementing the combination for all of the reasons described above and given that Nakatani describes coupling electronic components using a similar technique as described by Shibata. APPLE-1004, 2:60-67, 8:16-9:21, 17:14-17; Figs. 1, 39; APPLE-1005, [0051]-[0052], FIG. 1B.

C. Analysis

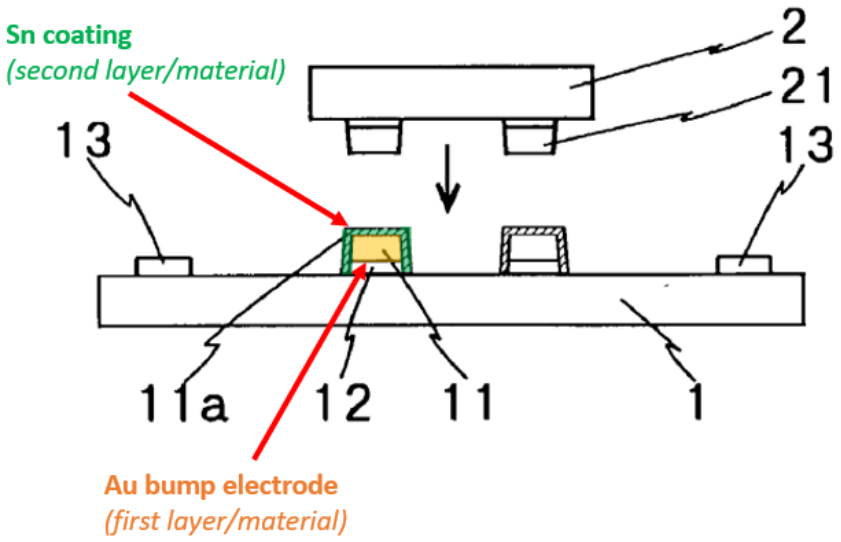
vii. Claim 3

[3] The electronic module of claim 1, wherein the first solid contact bumps include a layered structure, containing at least two layers of at least two different materials.

182. Nishiuma-Shibata renders obvious claim [3]. For example, in the combination, a layer of low melting temperature metal, such as tin, is layered over at least one of the gold bumps of Nishiuma to improve bonding between the gold

bumps. *Supra* §IV.D.2 (Nishiuma-Shibata Combination); APPLE-1005, [0032], [0053], [0074]. As shown in FIG. 1B, below, in the combination, "[a]n Sn coating 11a is provided on the bump electrode 11 made of Au." APPLE-1005, [0053].

FIG. 1B



APPLE-1005, FIG. 1B (annotated)

183. Accordingly, in the combination, Nishiuma's Au ball 13 / Au land 14 is coated with a layer of low melting temperature metal, such as tin, according to Shibata's teaching, and thus the first contact bumps include a layered structure containing at least two layers (a gold layer and a tin layer) of at least two different materials (gold and tin).

viii. Claim 14

[14] The electronic module of claim 13, wherein the first solderless contact bumps include a layered structure, containing at least two layers of at least two different materials.

184. *See supra* §XIII.C.[3] (Ground 1C Claim [3]).

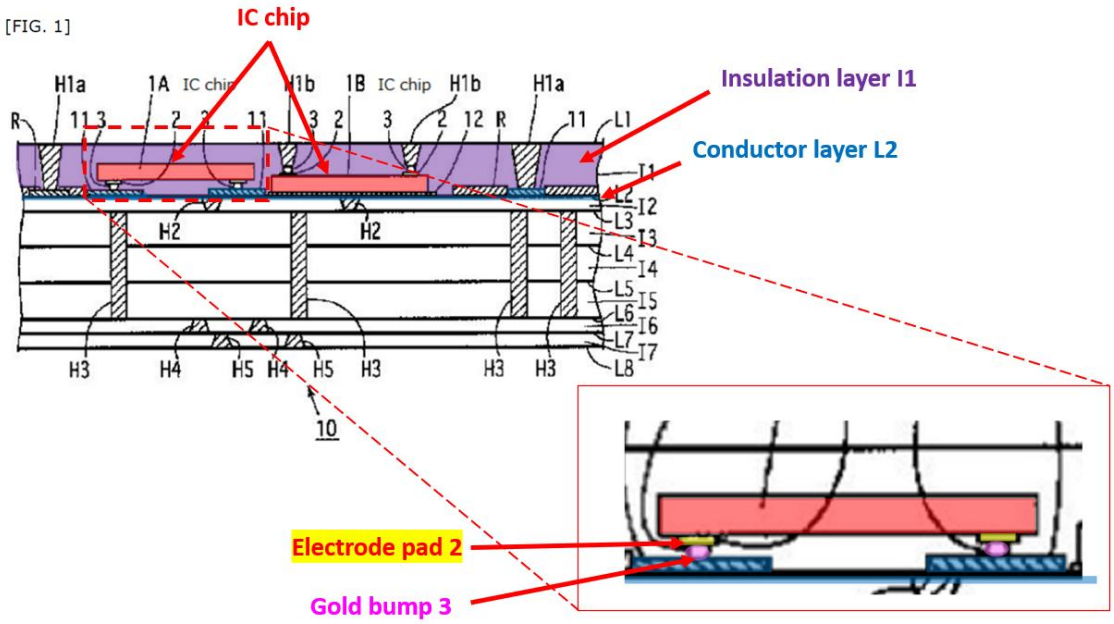
XIV. GROUND 2 – YONEYAMA-ONDA RENDERS OBVIOUS CLAIMS 1-27

A. Yoneyama Overview (APPLE-1013)

185. Yoneyama describes "a circuit board … in which electronic components such as a semiconductor integrated circuit chip with active surfaces on which a plurality of external connection electrodes have been formed[] … are mounted inside." APPLE-1013, [0001].

186. In one configuration illustrated by FIG. 1, Yoneyama describes that the "circuit board has eight conductor layers L1-L8 on which circuit patterns have been formed, and each conductor layer is finished with an electric insulation layer I1-I7." APPLE-1013, [0011], [0013]-[0015], [0017], [0042], FIGS. 1-2, 5-6. Two or more components such as IC chips in this configuration are, respectively, "mounted face-down and face-up on a single wiring board" such that the active surfaces of the components face in opposite directions. *Id.*, [0027], FIG. 1. According to Yoneyama, "the size of electronic devices incorporating a circuit

board of the present invention can be reduced" by decreasing the number of vias and wires required to connect the oppositely oriented chips to the circuit board. *Id.*, [0027], [0030] ("easily manufacture circuit boards … in which high-density mounting is performed").



APPLE-1013, FIG. 1 (annotated)

187. Yoneyama's FIG. 1 shows a circuit board 10 in which "IC chips 1A and 1B are embedded in a multilayer substrate … and solder bumps or gold bumps 2 are formed on multiple electrode pads on their active surfaces." *Id.*, [0033][4]. "IC

[4] There is some discrepancy in Yoneyama regarding the reference numerals used to refer to electrode pads and bumps. The Reference Numbers section (page

chip 1A is mounted on pad 11 of the circuit pattern formed on the surface of conductor layer L2 in the face-down state described above…[i]n other words, IC chip 1A is mounted by flip-chip bonding by way of bumps 2 to a pad 11, and IC chip 1B is mounted face-up with its bumps 2 facing upward, and its back side fixed to a pad 11 via a connection material 12 such as silver paste or anisotropic conductive film (ACF)." *Id.*, [0034].

188. Yoneyama describes another configuration with respect to FIG. 6, which shows a "multilayer mounting structure" in which IC chips are mounted in successively stacked modules. Yoneyama describes that such a multilayer structure can use "a circuit board 20 in which IC chips 1 are embedded inside while face-down" or "use a circuit board 30 in which IC chips 1 are flip-chip bonded while face-up." APPLE-1013, [0016], FIG. 6; *see also id.*, [0010]-[0018], FIG. 5.

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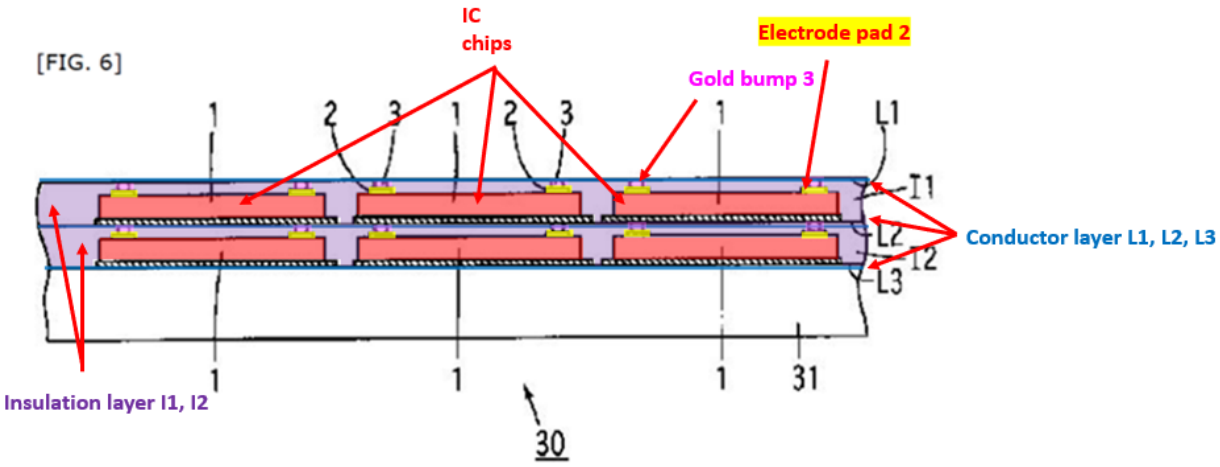
14 of Yoneyama) clarify electrode pad 2 and bump 3, consistent with the figures.

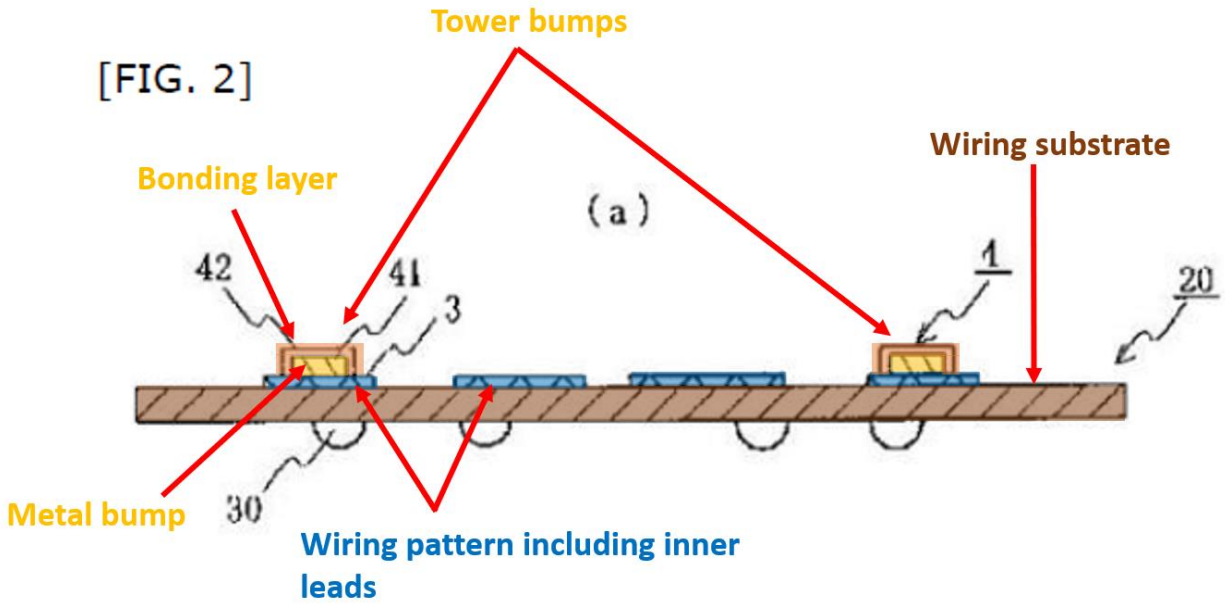


APPLE-1013, FIG. 6 (annotated)

B. Onda Overview (APPLE-1008)

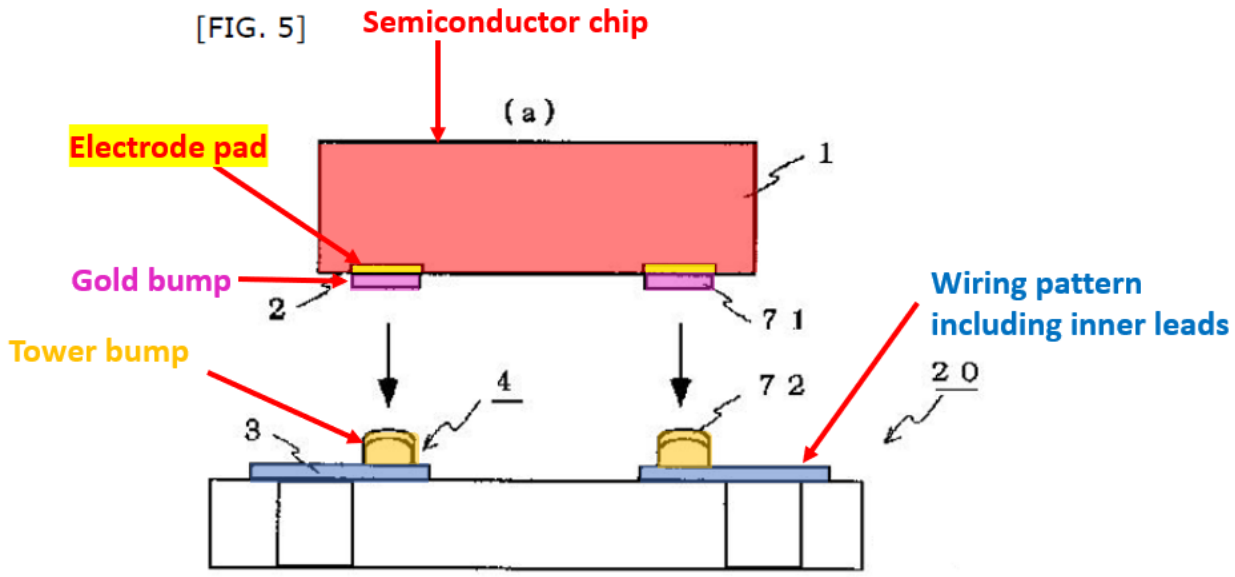
189. Onda describes techniques for connecting a wiring substrate to a semiconductor chip in which "tower bumps 4 are formed on the connecting portions [of the wiring pattern] to connect with the semiconductor chip." APPLE-1008, [0045], [0039]-[0042], [0070], FIGS. 1-10. "The tower bumps 4 are composed of a metal bump 41 and a bonding layer 42 that bonds to [] electrode pads 2 of the semiconductor chip 1." APPLE-1008, [0045], [0056], [0063],

[0073]-[0075], [0078], [0101].



APPLE-1008, FIG. 2

190. For example, in Figure 5(a), Onda illustrates the process of mounting a "semiconductor chip 1 on the manufactured wiring substrate 20." *Id.*, [0067]-[0070]. "[A]fter preparing the wiring substrate 20… and aligning the plurality of electrode pads 2 and tower bumps 4 formed on the main surface of the semiconductor chip 1, the semiconductor chip 1 is fixed" to the wiring layer using heat and pressure. *Id.*, [0068]; *see also* [0069]-[0083], [0092]-[0098], Figs. 6(a), 8(a), 9(a) (showing similar manufacturing methods that couple bumps on the semiconductor chip with tower bumps on the wiring layer).



APPLE-1008, FIG. 5

C. Combination of Yoneyama and Onda

191. Yoneyama describes that to connect an IC chip to the conductor layer, "IC chip 1A is mounted on pad 11 of the circuit pattern formed on the surface of conductor layer L2 in the face-down state described above…[i]n other words, IC chip 1A is mounted by flip-chip bonding by way of bumps 2 to pad 11." APPLE-1013, [0034], [0012]. However, Yoneyama does not limit the described connection between the IC chip and the circuit pattern to this arrangement, and a POSITA would have understood that other connection schemes would also be suitable for electrically connecting the bumps to the pads of the circuit pattern on the conductor layer. A POSITA would have been aware of other conventional

solutions for bonding a component to a circuit pattern and would have considered other options to achieve known benefits associated with those options.

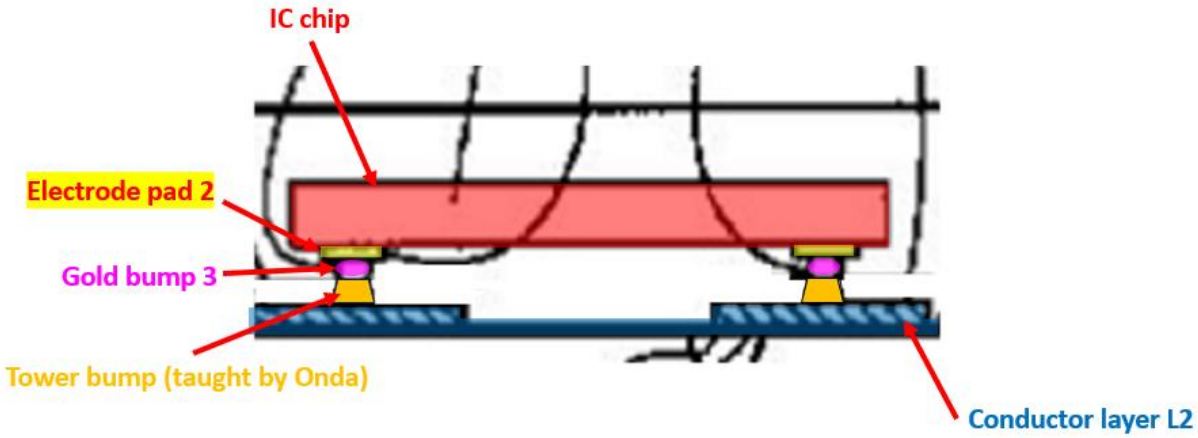
192. Recognizing that devices commonly are connected to wiring patterns of printed circuit board by conductive contact bumps formed on the device electrode pads and conductive bumps formed on the wiring, a POSITA would have turned to references like Onda to investigate the implementation of pairs of conductive bumps for electrically connecting Yoneyama's IC chip to the circuit pattern on the conductor layer. *See e.g.*, APPLE-1005, [0011]-[0012], FIGS. 1-5, 12.

193. Like Yoneyama, Onda describes techniques for coupling a device's electrode pads to wiring of a circuit board, although Onda makes the electrical connection using conductive bumps formed on both the wiring substrate and on the electrode pads of the device. APPLE-1008, [0039], [0045]-[0046], [0072]-[0074], [0085]-[0086], [0093]-[0094], [0100]-[0101], [0107]-[0108], [0114]-[0115], FIGS. 5-9. For example, Onda describes that a tower bump is formed on the wiring pattern of the PCB to provide an electrical connection to the semiconductor device and to buffer thermal stresses. *See* APPLE-1008, [0046] ("Alternatively, in the above-described method for manufacturing the electric element built-in module, a bump is formed on the connection electrode of the electric element, and

the electric element may be mounted on the wiring pattern by connecting the bump and the wiring pattern in an ultrasonic manner. This makes it possible to reduce a thermal load on the electric element.").

194. Onda describes that two conductive bumps can be used to couple a device to a wiring substrate: "gold plating (gold bumps) 71 are formed on each electrode pad 2 [of the device and the] wiring layer of the substrate including inner leads 3 is provided with tower bumps 4 consisting of copper bumps 4 consisting of copper bumps (metal bumps 41)." APPLE-1008, [0073]. Integration of Onda's technique for forming contact bumps on the substrate and on the device with Yoneyama eliminates any need for adhesives or anisotropic conductive film in the bonding, and therefore the Yoneyama-Onda combination can be implemented without adhesives/ACF. Although Yoneyama describes that in certain cases "a bonding adhesive or anisotropic conductive film (ACF) is applied to predetermined positions on the conductor layer L2," adhesive or ACF would not be required with the integration of Onda's teaching to connect a device and substrate by a pair of conductive contact bumps. *See* APPLE-1013, [0047], [0012]. Instead, in the combination, Onda's tower bump formed on the conductor layer L2 is connected to the electrode pad of the IC chip by a gold bump formed on the electrode pad. *Id.*,

[0039], [0045]-[0046], [0072]-[0074], [0085]-[0086], [0093]-[0094], [0100]-[0101], [0107]-[0108], [0114]-[0115], FIGS. 1, 5-9.



APPLE-1013, FIG. 1 (excerpted and annotated, modified to include Onda's teaching to use two conductive bumps to electrically couple the chip to the wiring pattern)

195. It would have been obvious to a POSITA to implement the combination of tower bumps and electrode bumps as taught by Onda into Yoneyama's device in place of the single metal bump described by Yoneyama for a number of reasons.

196. First, a POSITA would have understood that using electrode bumps (gold bumps) on the device and tower bumps on the circuit pattern to electrically connect the device to the printed circuit board would improve the ease of making the connection between the component and the wiring pattern. Onda describes that

in conventional methods, "bumps in the form of protrusions are formed on the main surface of the semiconductor chip 1 on electrode pads 2 to make connection to the inner lead 3 easier and improve the reliability of the connection." APPLE-1008, [0005]. Onda's suggestion of tower bumps formed on the circuit board would further simplify the method of providing electrical connection between the device and circuit board, because the bumps aid in the alignment of the device with electrical contact points of the printed circuit board.

197. Second, a POSITA would have understood that the addition of a metal tower bump to electrically connect an IC chip to circuit wiring of a conductor layer would improve the device's resistance to thermal stresses. APPLE-1008, [0012], [0015], [0041], [0046]. For example, Onda describes that "the wiring substrate [is] characterized in that electrical connections of the semiconductor devices and the wiring pattern and tower bumps that buffer the thermal stress generated between the insulating substrate and the semiconductor chip have been provided on the wiring patterns where the semiconductor chip is mounted on the insulating substrate." *Id.*, [0012]. A POSITA would have understood that the addition of metal balls between the component and substrate would improve resistance to thermal stresses because the metal balls would be able to absorb thermal stresses

that would otherwise be on a direct connection between the component and printed board. APPLE-1005, [0060], [0014], [0022], [0084].

198. For example, Onda describes that providing a tower bump on the circuit board for connection to the bumps on the semiconductor chip may "prevent[] cracking of semiconductor chips due to thermal stress." APPLE-1008, [0010]; *see also id.*, [0008]-[0012], [0070]; APPLE-1011, [0004] ("Reliability concerns often arise in flip-chip-on-board technology; for instance, due to a mismatch between the coefficients of thermal expansion between the semiconductor chip and the substrate, the solder joints may fatigue."), [0014] (describing thermal mismatch between a conventional substrate and chip carrier).

199. Third, a POSITA would have understood that providing conductive bumps to electrically connect the device and the circuit board would allow for the selection and use of materials that increase the strength of the connection between the device and circuit board. APPLE-1008, [0076]. The selection of materials with high resistance to thermal stresses and which provide strong bonds between the component and printed wiring board could absorb stresses and shocks and provide a more reliable connection between the component and printed wiring board less susceptible to common failures.

200. Fourth, implementing a circuit board embedded with IC chips electrically coupled to the circuit board by conductive bumps formed on the wiring and on the device electrodes would have been obvious as a predictable application of a known technique for coupling devices to a printed circuit board as taught by Onda to a known system as taught by Yoneyama to achieve entirely predictable results. A POSITA would have understood that using two sets of contact bumps (one on the component and one on the substrate) was a well-known method for electrically connecting a component to circuit board by the Critical Date, and a POSITA would have understood that implementing this conventional method would predictably achieve an electrical connection between the device and substrate wiring, just as Onda teaches.

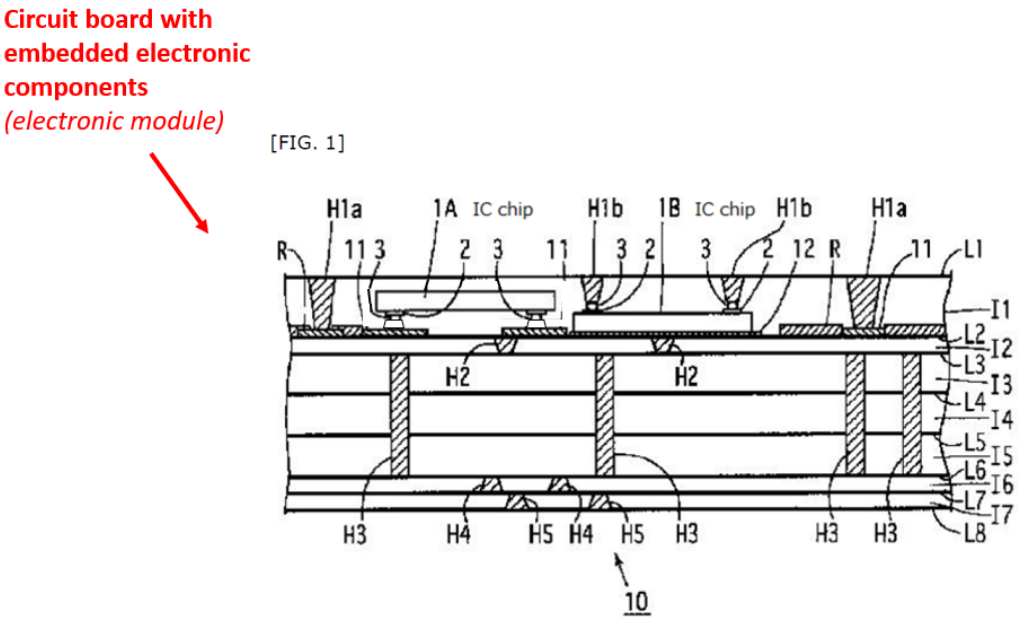
201. The combination further would have been obvious and a POSITA would have had a reasonable expectation of success implementing the combination for all of the reasons above and given as the similarities between the connection methods described by Yoneyama and the techniques suggested by Onda. APPLE-1013, [0012]-[0016], [0033]-[0034], Figs. 1, 6; APPLE-1008; [0068]-[0083], [0092]-[0098].

D. Analysis

i. Claim 1

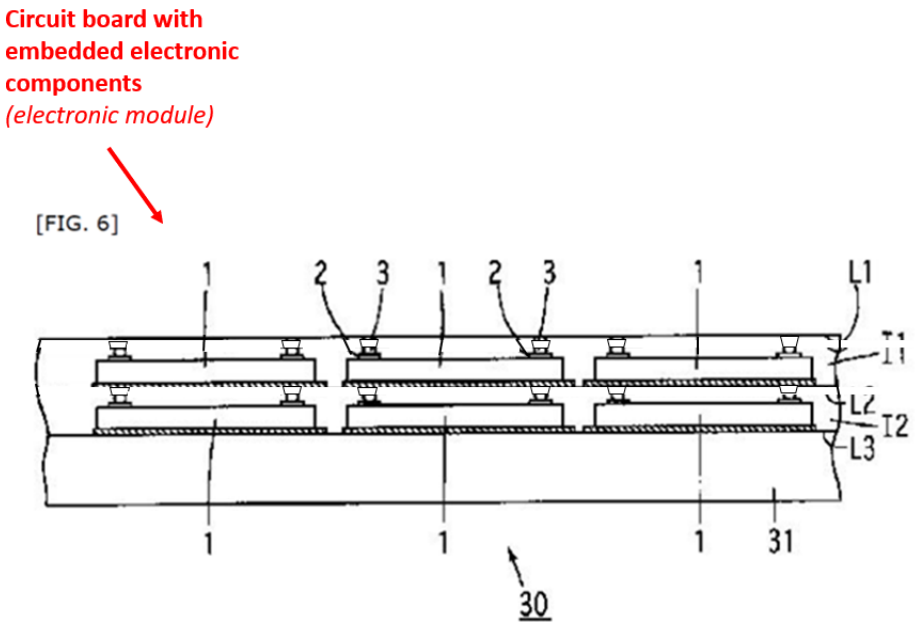
[1pre] An electronic module, comprising:

202. To the extent the preamble is limiting, Yoneyama-Onda renders [1pre] obvious. Yoneyama describes "a circuit board with embedded electronic components" such as IC chips that constitutes an "***electronic module***" as claimed. APPLE-1013, [0058], [0001] ("The present invention relates to a circuit board with embedded components and a method for manufacturing the same, in which electronic components such as a semiconductor integrated circuit chip with active surfaces on which a plurality of external connection electrodes have been formed, for example, are mounted inside"), [0020], [0025], [0031]-[0034]; *cf.* APPLE-1001, 1:18-23 ('527 patent describing that an electronic module "can be a module like a circuit board, which includes several components [such as] semiconductor components").



APPLE-1013, FIG. 1 (annotated, modified to include tower bumps as taught by Onda)

203. Yoneyama's configuration shown in FIG. 6 also provides an electronic module. APPLE-1013, [0016]-[0017]. Yoneyama describes that FIG. 6 shows "a circuit board 30 in which IC chips 1 are flip-chip bonded while face-up." *Id.*, [0016]. FIG. 6 shows that the IC chips 1 each are connected to a conductor layer by gold bumps formed on the electrode pads. *See* FIG. 6, reference numbers section on p. 14 of APPLE-1013. The version of FIG. 6 below has been modified to also include tower bumps to form the connection between the gold bumps and the conductor layer, as Onda teaches. *Supra* §XIV.C.



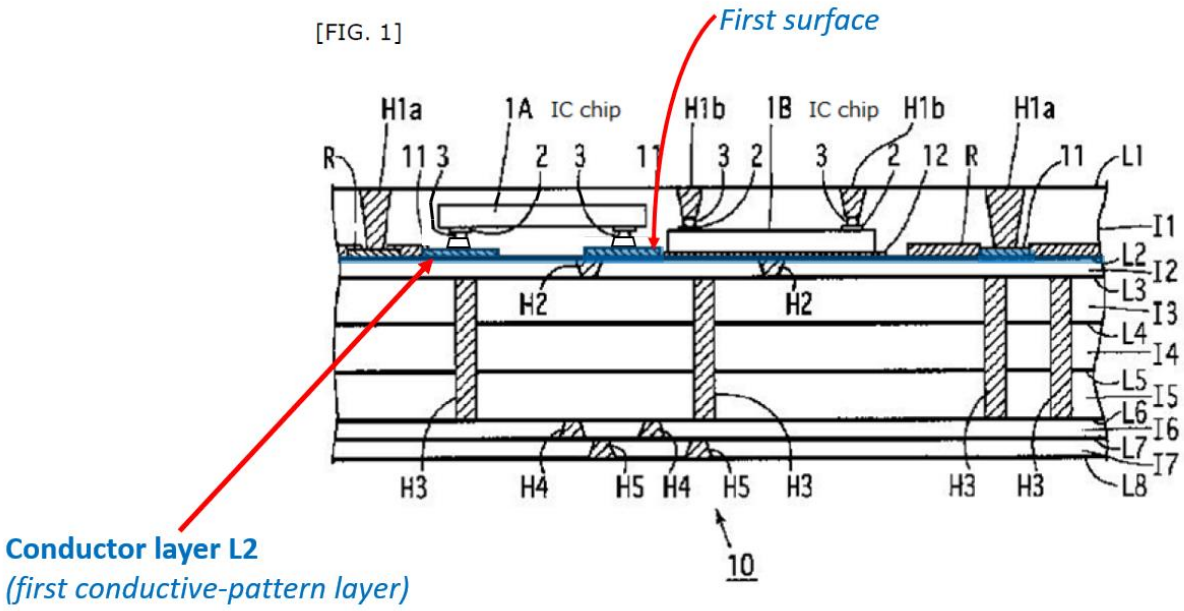
APPLE-1013, FIG. 6 (annotated, modified to include tower bumps as taught by Onda)

204. As I will discuss further below with regard to element [19pre], in an additional or alternative mapping, each layer of the stack shown in FIG. 6 can be mapped to the electronic module recited in [1pre].

[1a] a first conductive-pattern layer having a first surface,

205. Yoneyama-Onda renders [1a] obvious. For example, Yoneyama describes that "[e]ach conductor layer L1-L8 has the required circuit pattern" and that circuit patterns can include electrode pads 11. APPLE-1013, [0015], [0036] ("The electrical structure consists of a plurality of pads 11 and wiring circuits formed in the conductor layer L2."); *see also id.*, [0034]-[0037], [0042], [0051],

[0011]-[0012]. Yoneyama's conductor layer L2 including pads 11 is a conductive circuit pattern and provides a "***first conductive-pattern layer with a first surface***" as claimed. *Id*., [0036].

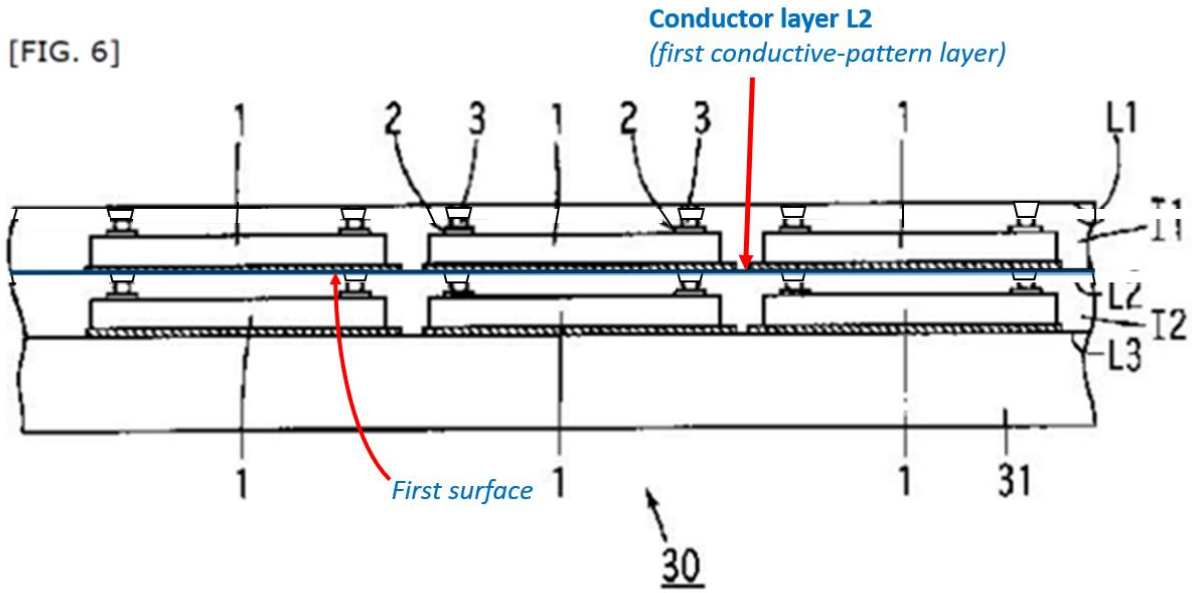


APPLE-1013, FIG. 1 (annotated, modified to include tower bumps as taught by Onda)

206. A POSITA would have understood Yoneyama's conductor layer L2 including pads 11 and circuit pattern to provide a "first… layer" as claimed, because the pads and circuit pattern cooperate to form a conductive layer for transmission of power and information signals. APPLE-1013, [0015], [0036]; *cf.*,

APPLE-1001, 6:50-57 (similarly describing layers comprised of multiple components).

207. Yoneyama's FIG. 6 configuration also provides "***first conductive-pattern layer with a first surface***" as claimed, for example, in conductor layer L2. In FIG. 6, the first surface of the conductor layer L2 is the surface facing the IC chip's electrode pads 2 and gold bumps 3. APPLE-1013, FIG. 6.

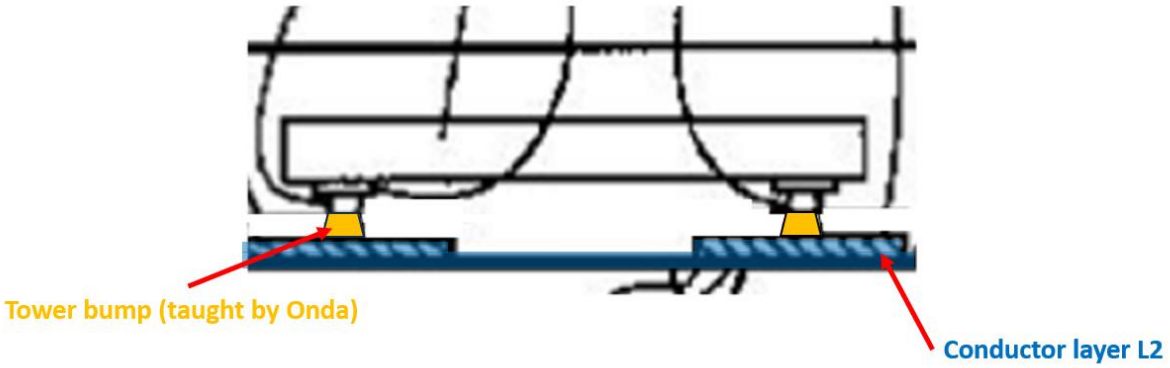


APPLE-1013, FIG. 6 (annotated, modified to include tower bumps as taught by Onda)

[1b] first solid contact bumps solderlessly made on the first surface of the first conductive-pattern layer and metallurgically and electrically connected thereto,

208. Yoneyama-Onda renders [1b] obvious. For example, Yoneyama describes that an IC chip is mounted to pads of a conductive layer using gold bumps. APPLE-1013, [0034] ("IC chip 1A is mounted on pad 11 of the circuit pattern formed on the surface of conductor layer Ls in the face-down state … [such that] IC chip 1A is mounted by flip-chip bonding by way of bumps [3] to a pad 11"), [0036]. To the extent that Yoneyama does not expressly disclose electrically connecting the IC chip to the conductor layer via gold bumps and contact bumps formed on the pads of the conductor layer, Onda teaches this conventional solution for bonding a component to a circuit board. APPLE-1008, [0039] ("tower bumps 4 are provided in the wiring layer of the substrate… to connect with the semiconductor chip 1"), [0073] ("Electrode pads 2 are arranged … on the element formation surface of the semiconductor chip 1, and gold plating (gold bumps) 71 are formed on each electrode pad 2. The wiring layer of the substrate … is provided with tower bumps 4 consisting of copper bumps (metal bumps 41) that have been tin plated 72 (bonding layer 42)"), [0044]-[0045], [0070], [0081]-[0082], [0101]-[0102], [0108]-[0109], FIGS. 5-10.

209. As described above, it would have been obvious and a POSITA would have been motivated by multiple reasons to implement Yoneyama's IC chip bonded to the conductive layer pad using two conductive bumps, including a tower bump ("***first contact bumps***") formed on the pad of the conductive layer ("***first surface of the first conductive pattern layer***") as suggested by Onda. *Supra* §IV.E.3 (Yoneyama-Onda Combination).



APPLE-1013, FIG. 1 (excerpted and annotated, modified to include tower bumps as taught by Onda)

210. Onda describes that in a "post-bumping method," "metal bumps 41 are formed on the wiring pattern including inner leads 3 by metal plating (electroless or electroplating)." APPLE-1008, [0062], [0050], [0059]-[0064], [0121]FIGS. 4A-D. Onda's metal plating process is thus a ***solderless*** process for making the tower bumps on the conductive layer. Rather than using solder to couple tower bumps to the wiring pattern, Onda describes using metal plating

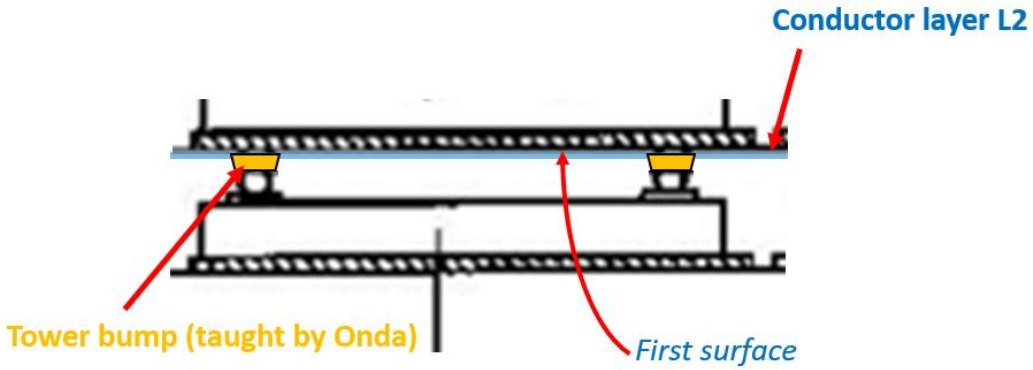
techniques which do not rely on solder to form the bond between the bumps and the pattern. *Id.*

211. Onda describes that "tower bumps 4 should be made of a conductive material that does not undergo a phase transformation at high temperatures," and a POSITA would have understood that the tower bumps, being formed of conductive materials, are ***metallurgically and electrically connected*** to Yoneyama's conductive layer to couple the IC chip to the conductive layer. APPLE-1008, [0099] ("an example of electrical connection between a semiconductor device and a wiring substrate using gold-gold bonding will be described"), [0014], [0039], [0042], [0045], [0057], [0101]-[0106]. Yoneyama's wiring circuits formed on conductor layers "are formed by etching copper foil or by plating." APPLE-1013, [0012]. Similarly, Onda's wiring pattern is "wired with a conductive material such as copper or indium titanium oxide." APPLE-1008, [0037], [0053]-[0058], [0061], [0086], [0094], [0101], [0108]. It would have been obvious to a POSITA that the metal plating technique described by Onda for bonding the tower bumps to the wiring pattern would be equally applicable to Yoneyama's copper wiring pattern as to Onda's. APPLE-1013, [0012]; APPLE-1008, [0037], [0061]. A POSITA would have had a reasonable expectation of success in applying Onda's metal

plating tower bump bonding technique in Yoneyama's system at least because of the similar wiring materials used.

212. A POSITA would have understood that the bond between the gold (or other metal) tower bump taught by Onda and Yoneyama's copper wiring of the conductive layer achieved by metal plating would provide a metallurgical and electrical connection between the tower bump and the wiring circuit due to the materials used in the tower bump and wiring circuit. Accordingly, a POSITA would have understood that the tower bumps formed on the circuit wiring provide the "***first solid contact bumps solderlessly made on the first surface of the first conductive-pattern layer and metallurgically and electrically connected thereto***" as claimed.

213. Yoneyama's FIG. 6 configuration also provides "first solid contact bumps solderlessly made on the first surface of the first conductive-pattern layer and metallurgically and electrically connected thereto."



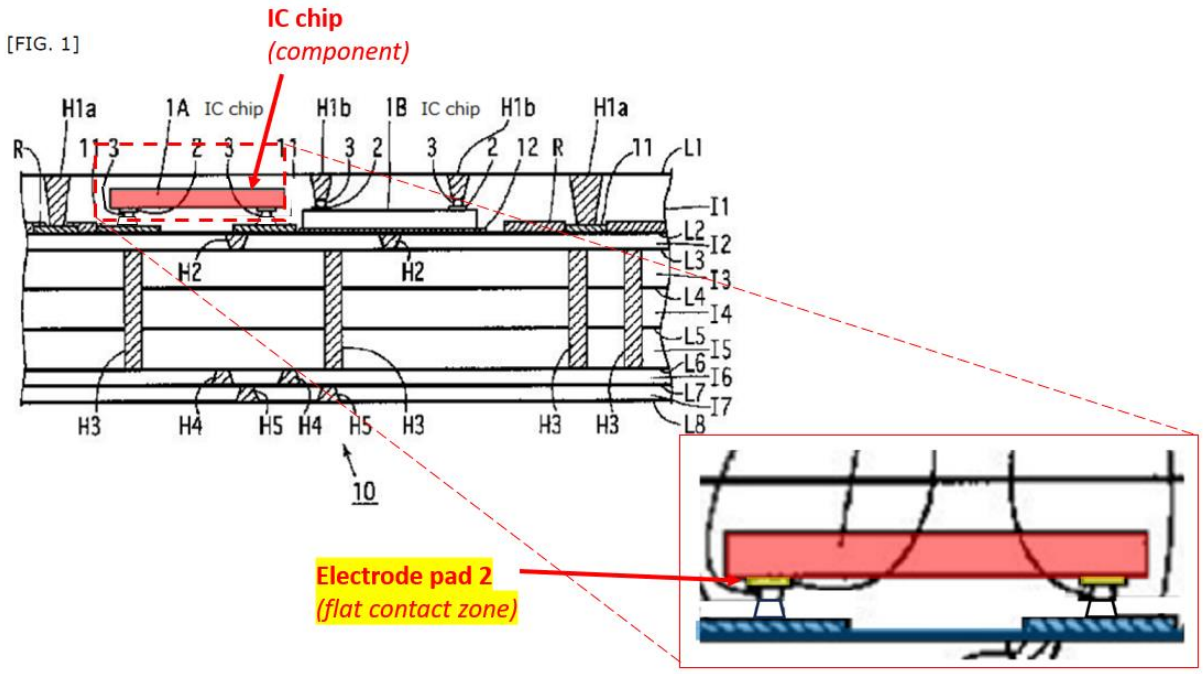
APPLE-1013, FIG. 6 (excerpted and annotated, modified to include tower bumps as taught by Onda)

214. In the combination, Yoneyama's IC chip is coupled to the conductor layer L2 by a tower bump, as taught by Onda. *Supra* §XIV.C (Yoneyama-Onda Combination). Yoneyama describes with regard to FIG. 6, that "a plurality of IC chips 1 are mounted face-up by flip chip bonded[ing]…on conductor layer L3" and that these chips are bonded to "conductor layer L2 on which a wiring pattern has been formed." APPLE-1013, [0017], FIG. 6. A POSITA would have understood that the connection between the tower bump and wiring pattern of the conductor layer is formed by the same process in the configuration shown in FIG. 6 as in the FIG. 1 configuration described above. *Supra* §XIV.C. Despite being depicted as below the L2 conductor layer, the tower bumps taught by Onda would be formed on the L2 conductor layer in the combination prior to bonding to the component,

just as Yoneyama describes that the wiring pattern is formed on the L2 layer prior to the bonding. APPLE-1013, [0017]. Accordingly, a POSITA would have understood that the tower bumps formed on the circuit wiring in FIG. 6 also provide the "***first solid contact bumps solderlessly made on the first surface of the first conductive-pattern layer and metallurgically and electrically connected thereto***" as claimed.

[1c] a component having flat contact zones,

215. Yoneyama-Onda renders [1c] obvious. For example, Yoneyama describes that "IC chips 1A and 1B are bare chips [having] multiple electrode pads on their active surfaces." APPLE-1013, [0033], [0044] (describing "external connection electrodes of IC chip 1A"), [0021] ("at least two electronic components with active surfaces on which a plurality of external connection electrodes have been arranged"), [0001], [0025]-[0026], [0006], [0008], [0044].



APPLE-1013, FIG. 1 (annotated, modified to include excerpt and tower bumps as taught by Onda)

216. As discussed above, nothing in the plain language of the claims, the '527 patent's specification or the prosecution history indicates that the term "flat" should be understood to have a meaning other than the plain meaning of the term; that is, lacking in curvature. In particular, the specification does not indicates that a flat contact zone must not protrude from the surface of the component. Indeed, the term "flat" appears in the '527 patent specification only in the phrase "flat contact zones" and without additional description of additional characteristics required of a "flat" contact zone. APPLE-1001, 3:8-27; 9:46-55. Accordingly,

The plain meaning of the claim term "flat contact zone" should be interpreted as requiring a surface lacking curvature, and should not be interpreted to be limited to contact zones that do not protrude from the surrounding surfaces of the component.

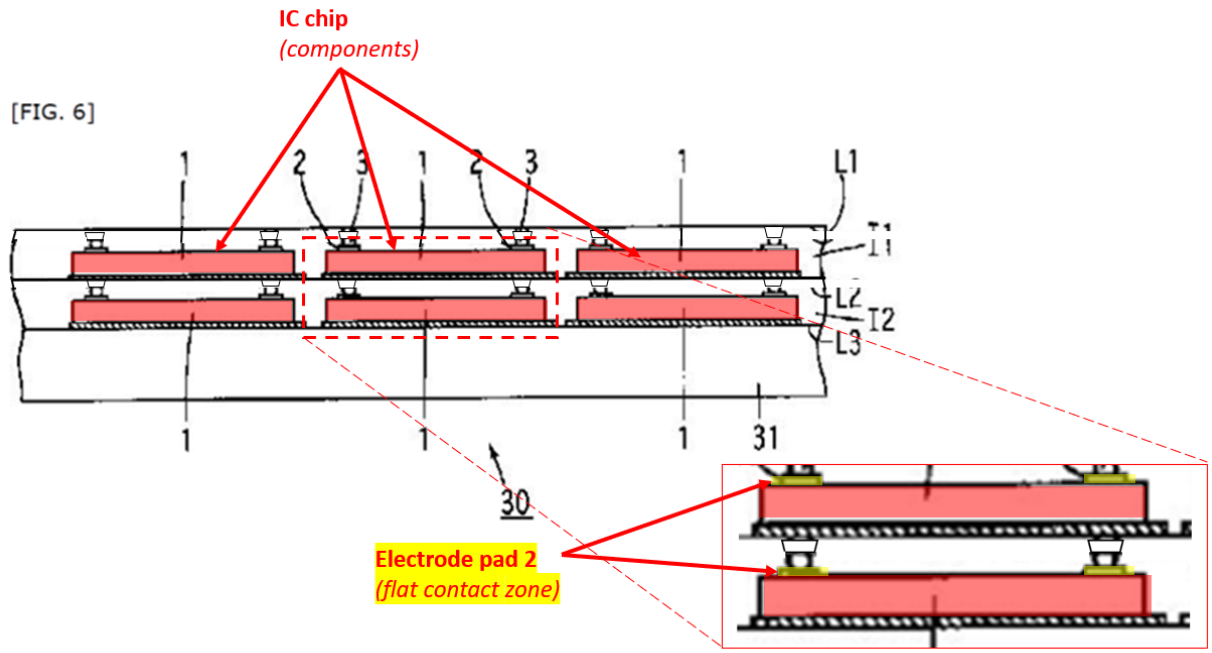
217. Yoneyama's electrode pads (also called external connection electrodes) meet the plain meaning of the term "flat" and provide "flat contact zones" at least because the electrodes lack curvature on their surfaces. APPLE-1013, FIG. 1.

218. The Applicant did not require in the claims that the contact zone have other properties (such as not protruding relative to a surface of the component) and accordingly, such other properties should not be read into the claim language. Accordingly, Yoneyama's IC chips and electrode pads provide the "***component having flat contact zones***" as claimed.

219. To the extent that the claim language is interpreted to require contact zones that are not raised relative to the surrounding component surfaces, Yoneyama provides this well-known feature. For example, although Yoneyama's figures depict electrode pads as extending from the surface of the component, Yoneyama's disclosure merely requires that the IC chips have "electrode pads 2 serving as connecting electrode" formed on the active surfaces of the chips. APPLE-1013, [0006]. Yoneyama does not describe any criticality related to the

shape, position, or protrusion of the electrode pads. Further, IC chips having non-raised electrode pads were well-known by the Critical Date and it would have been obvious to a POSITA to apply such electrode pads in Yoneyama's device.

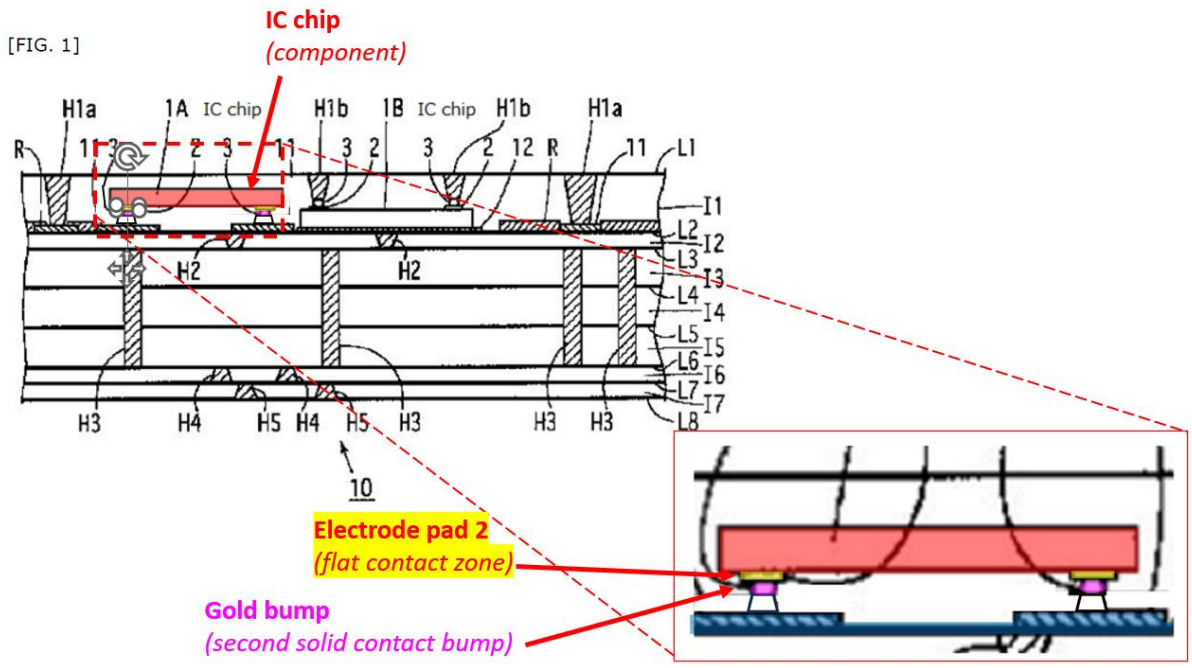
220. Yoneyama's FIG. 6 configuration also provides a "***component having flat contact zones***." The FIG. 6 configuration includes electrode pads 2 formed on the surfaces of the IC chips. APPLE-1013, FIG. 6. As in the configuration shown in FIG. 1, the electrode pads in the FIG. 6 configuration are flat on their surfaces, and accordingly provide "flat contact zones."



APPLE-1013, FIG. 6 (annotated, modified to include excerpt and tower bumps as taught by Onda)

[1d] second solid contact bumps solderlessly made on the flat contact zones and metallurgically and electrically connected thereto, and

221. Yoneyama-Onda renders [1d] obvious. For example, Yoneyama describes that "gold bumps… are formed on multiple electrode pads" of the IC chips. APPLE-1013, [0033], [0036] ("IC chip 1A is flip-chip bonded face-down so that bumps 2 are located on some pads 11"), [0008] ("IC chips 1 are flip-chip bonded with their active surfaces on which bumps 3 have been formed on a plurality of electrode pads 2, facing down"). Yoneyama's gold bumps formed on electrode pads of the semiconductor chip provide the "***second solid contact bumps made on the flat contact zones***" as claimed.



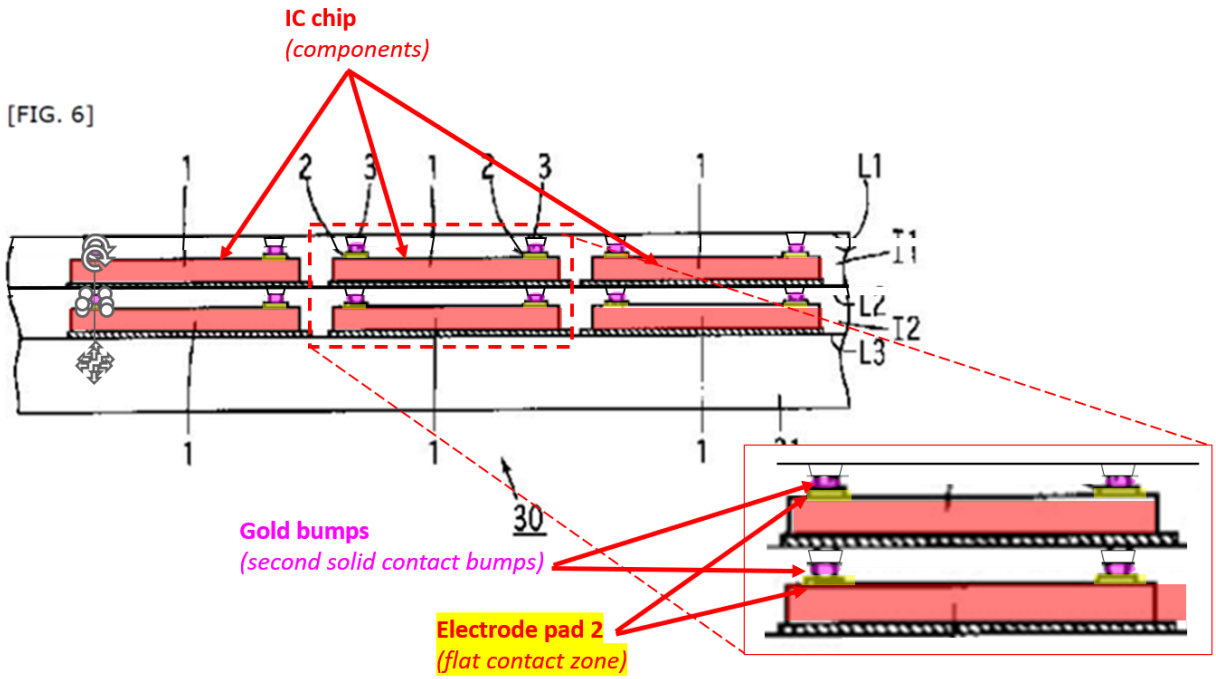
APPLE-1013, FIG. 1 (annotated, modified to include excerpt and tower bumps as taught by Onda)

222. Yoneyama's description that the bumps formed on the electrode pads may be *either* "solder bumps ***or*** gold bumps" confirms that the gold bumps are distinguished from solder bumps and are thus ***solderlessly*** formed on the electrode pads. APPLE-1013, [0033]. Yoneyama's description of the gold bumps being formed on "multiple electrode pads on [the IC chips'] active surfaces" confirms that the gold bumps are formed on the electrode pads ("***flat contact zones***") and are intended to provide an electrical connection to the IC chips through the "active surfaces." *Id.*

223. A POSITA would have also understood that the connection between the gold bumps and electrode pads is an ***electrical and metallurgical*** connection because the gold bumps and electrodes are both made of conductive metal materials bonded to each other. A POSITA would have understood that gold bumps are conductive because gold has high electrical conductivity. APPLE-1035, 133. A POSITA would have also understood that electrode pads are also made from metal materials, such as aluminum, and are electrically conductive. APPLE-1008, [0068] ("electrode pads 2, which are aluminum, may be metallized with other metals dependent on the connection method"), [0078] ("Applying gold plating to the electrode pads 2 of the semiconductor chip"); APPLE-1004, 8:10-16 (describing formation of electrode pads on the surface of the chip: "electrode pads 11 are formed by boring holes in the surface protection film. The electrode pads 11 are made of Au similarly to the integrated circuit wirings."); APPLE-1004, 4:10-13 (describing benefit of solderless connection techniques). Accordingly, Yoneyama-Onda provides "***second solid contact bumps solderlessly made on the flat contact zones and metallurgically and electrically connected thereto***."

224. Yoneyama's FIG. 6 configuration also provides "second solid contact bumps solderlessly made on the flat contact zones and metallurgically and

electrically connected thereto." APPLE-1013, FIG. 6. Yoneyama's IC chips in FIG. 6 include bumps 3 formed on electrode pads 2. *Id.*



APPLE-1013, FIG. 6 (annotated, modified to include excerpt and tower bumps as taught by Onda)

225. A POSITA would have understood that the connection between the metal bump 3 and electrode pad 2 is formed by the same process in the configuration shown in FIG. 6 as in the FIG. 1 configuration described above. Accordingly, a POSITA would have understood that the metal bumps formed on the electrode pads in FIG. 6 also provide the "***second solid contact bumps solderlessly made on the flat contact zones and metallurgically and electrically connected thereto***," as claimed.

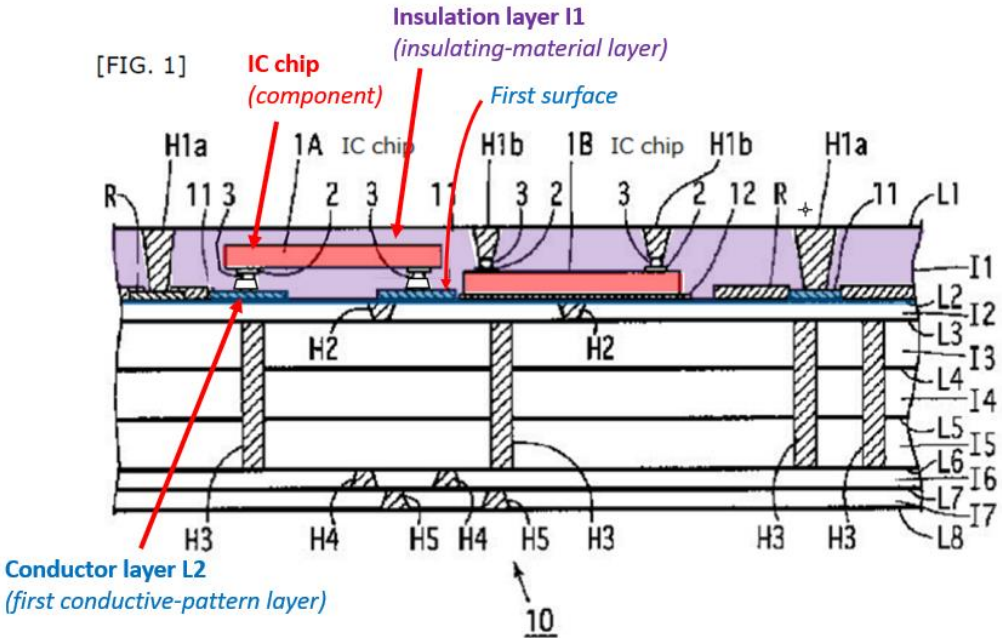
[1e]-[1f-i] an insulating-material layer on the first surface of the first conductive-pattern layer, wherein the component is embedded in the insulating-material layer

226. Yoneyama-Onda renders elements [1e]-[1f-i] obvious. For example, Yoneyama describes "forming an insulation layer I1 on the IC chips 1" over electrical conductor layer L2. APPLE-1013, Abstract, [0011], [0017], [0035], [0049]. Yoneyama's insulation layer I1 provides an "***insulating-material layer***" in which the IC chips (***component***) is ***embedded*** as claimed.

227. Yoneyama describes that "each conductor layer is finished with an electric insulation layer I1-I7 formed by printing an electric insulation resin between the conductor layers." *Id.*, [0011], [0001], [0017], [0021], [0026], [0035], [0049], FIG. 1. Each of Yoneyama's insulation layers are formed from insulating materials: "Each one of insulating layers I2 to I7 is composed of glass cloth impregnated with a thermosetting resin such as an epoxy resin, and insulation layer I1 is formed by mixing a large amount of filler with a thermosetting resin such as an epoxy resin." *Id.*, [0011]. Yoneyama's insulation layers are each formed on a conductor layer. *Id.*, FIG. 1. Accordingly, and as shown in FIG. 1, Yoneyama's insulation layer I1 (***insulating-material layer***) is formed on top surface (***first surface***) of electrical conductor layer L2 (***first conductive-pattern layer***).

Accordingly, Yoneyama's insulation layer I1 is formed "***on the first surface of the first conductive-pattern layer***" as claimed.

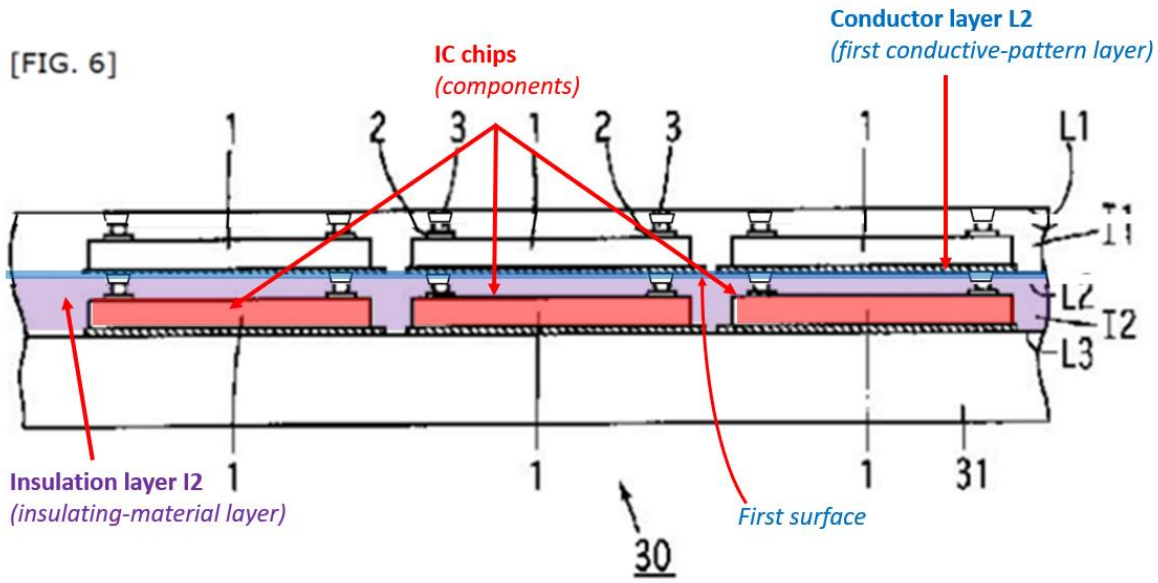
228. Yoneyama teaches the insulation layer I1 is formed on electrical conductor layer L2 over the IC chips such that the IC chips are embedded in the insulation layer. *Id.*, [0031] ("FIG. 1 is a cross-sectional side view of a circuit board with embedded electronic components"), [0001] ("embedded electronic components"), [0021] ("forming an insulation layer over the electronic components"), [0022]-[0026]. Accordingly, Yoneyama's "***component is embedded in the insulating-material layer***" as claimed.



APPLE-1013, FIG. 1 (annotated, modified to include tower bumps as taught by Onda)

229. Yoneyama's FIG. 6 configuration also provides "an insulating-material layer on the first surface of the first conductive-pattern layer, wherein the component is embedded in the insulating-material layer." APPLE-1013, [0016]-[0017]. Yoneyama describes that the "insulating resin" is added to the L3 layer around the component before "conductor layer L2" is bonded to the component. APPLE-1013, [0017]. A POSITA would have understood from Yoneyama's description of the positions of the various layers in FIG. 6, that the insulating resin forming layer I2 in FIG. 6 is thus on the first surface of the conductor layer L2 ("first conductive pattern layer"). Indeed, in FIG. 6, the insulation layer I2 is positioned between conductor layers L2 and L3, so that it is on a bottom surface of conductor layer L2 (***first surface of first conductive-pattern layer***).[5] *Id.*, FIG. 6. Additionally, insulation layer I2 surrounds Yoneyama's IC chips in FIG. 6, such that Yoneyama's FIG. 6 provides that the "***component is embedded in the insulating-material layer***" as claimed.

[5] Though insulation layer I2 is given here as an example, multiple insulation layers in Yoneyama's FIG. 6 configuration meet the requirements of claim limitations [1e]-[1f-i]. As another example, insulation layer I1 in FIG. 6 is also positioned between conductor layer L1 and L2 and on a bottom surface of conductor layer L1, and IC chips are embedded in insulation layer I1.



APPLE-1013, FIG. 6 (annotated, modified to include excerpt and tower bumps as taught by Onda)

[1f-ii] and wherein the second solid contact bumps made on the flat contact zones of the component are metallurgically, electrically and solderlessly connected to the first solid contact bumps made on the first surface of the first conductive-pattern layer.

230. Yoneyama-Onda renders [1f-ii] obvious. For example, Yoneyama describes that "IC chip 1A is flip-chip bonded face-down so that bumps 2 are located on some pads 11." APPLE-1013, [0036]. As described above, in the Yoneyama-Onda combination, bumps 2 formed on the IC chip electrodes (***second solid contact bumps made on the flat contact zones of the component***) as taught by Yoneyama are electrically connected to tower bumps 4 formed on the circuit

board (***first solid contact bumps made on the first surface of the first conductive-pattern layer***) as Onda teaches. *Supra* §XIV.C (Yoneyama-Onda combination); APPLE-1008, [0040], [0068].

231. Further, in the combination, the metal bumps and tower bumps are connected using heat and pressure, as taught by Onda. APPLE-1008, [0068] ("after preparing the wiring substrate 20… and aligning the plurality of electrode pads 2 and tower bumps 4 formed on the main surface of the semiconductor chip 1, the semiconductor chip 1 is fixed" after which "a heating tool is used to heat… and a pressurizing tool is used to apply pressure… to cause a metal diffusion reaction and establish a connection"); *see also* APPLE-1013, [0048] (describing that during bonding of the chip to the circuit board, "IC chip 1A is temporarily fixed by a bonding device, followed by final pressure bonding"), APPLE-1009, [0007], [0012]-[0013] (explaining a bonding process using ultrasonic vibrations, heat and thermocompression); *supra* §IV.B.

232. A POSITA would have understood and found obvious that the connection between the gold bumps and tower bumps – both formed from conductive metal materials – in the combination is a ***metallurgical and electrical*** connection which is made ***solderlessly***. APPLE-1013, [0033] ("solder bumps or gold bumps 2 are formed on multiple electrode pads on [the IC chip] active

surfaces"); APPLE-1008, [0017] ("the semiconductor chip is electrically connected to the wiring patterns via the tower bumps"), [0018] ("the tower bumps on the wiring substrate comprise metal bumps that buffer the thermal stress generated between the insulating substrate and the semiconductor chip, and a plating layer for bonding that establishes an electrical connection with the semiconductor chip provided on the metal bumps"). As described above, each of the tower bumps and gold bumps are formed from electrically conductive metals, and those metal bumps are solderlessly joined. *Supra* §§XIV.D.[1b], [1d] (Ground 2 Elements [1b] and [1d]); APPLE-1035, 133.

233. A POSITA would have appreciated that the bonding of the metal bumps of Yoneyama to the metal tower bumps of Onda results in a metallurgical and electrical connection between the bumps, in either of Yoneyama's configurations shown in FIGS. 1 or 6, at least because Yoneyama and Onda describe that the connection is made by a well-known solderless thermocompression process for forming the connection – in fact the same process described in the '527 patent as yielding metallurgically and electrically connected components. APPLE-1001, 6:41-49; APPLE-1013, [0048]; APPLE-1008, [0068]; *supra* §IV.B. The pressure-based bonding techniques described by Yoneyama and Onda for connecting the metal bumps and tower bumps align with the '527

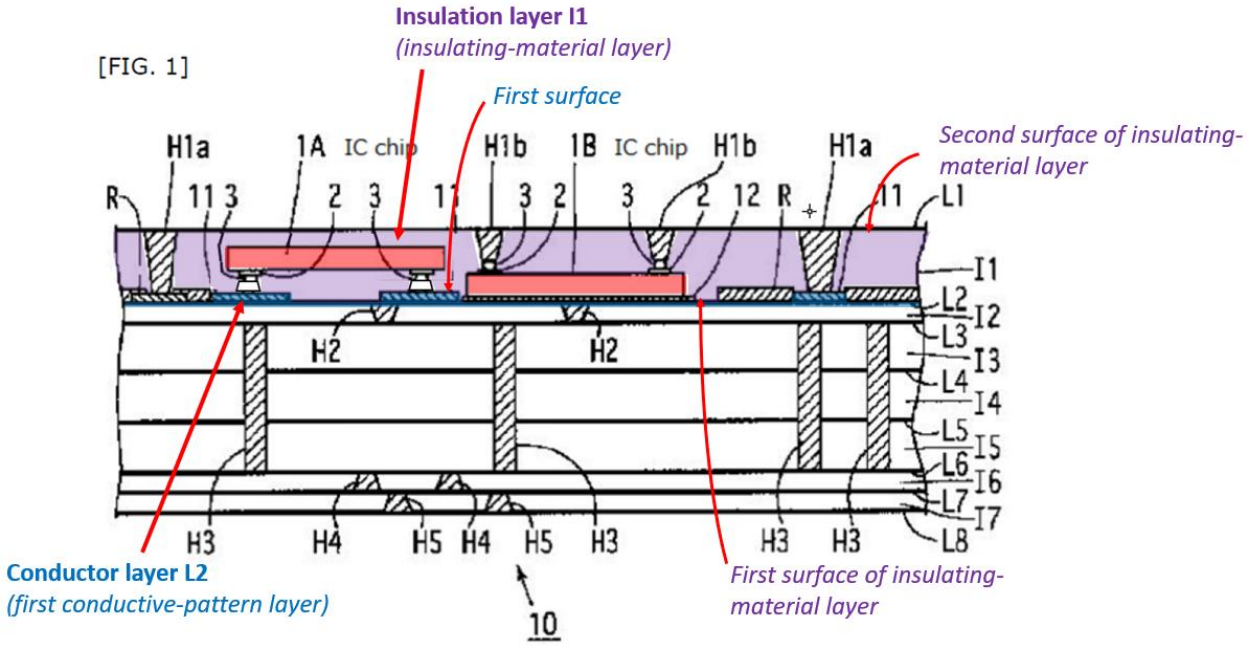
patent's description of thermocompression as a method "in which two pieces containing metal are pressed against each other while thermal energy is brought to the area… the effect of the thermal energy and the pressure created between the surfaces to be joined cause the pieces to be joined to be bonded metallurgically." APPLE-1001, 6:59-63. Accordingly, in the Yoneyama-Onda combination, "***the second solid contact bumps made on the flat contact zones of the component are metallurgically, electrically and solderlessly connected to the first solid contact bumps made on the first surface of the first conductive-pattern layer***," as claimed

234. As a result of the solderless connection between the tower bumps and the wiring circuit and between the metal bumps and the electrode pads, the electrode pads ("***flat contact zones***") are effectively metallurgically and electrically connected to the pads of the wiring circuit ("***first surface of the first-conductive pattern layer***") after bonding the metal bumps and tower bumps. APPLE-1013, [0048], FIGS. 1, 6; *supra* §XIV.D.[1b] (Ground 2 Element [1b] (explaining that the tower bumps are electrically and metallurgically connected to the wiring circuit)) and §XIV.D.[1d] (Ground 2 Element [1d] (explaining that the metal bumps are electrically and metallurgically connected to the electrode pads of the IC chip)).

ii. Claim 2

[2a] The electronic module of claim 1, wherein the insulating-material layer comprises a first surface and a second surface, the first surface being against the first conductive-pattern layer,

235. Yoneyama-Onda renders obvious claim [2]. For example, with regard to element [2a], Yoneyama describes that "an insulating resin is applied [to the surface of conductor layer L2] to form insulating layer I1, and then conductor layer L1 on which a wiring pattern has been formed is formed on the surface of insulating layer I1." APPLE-1013, [0017]; *supra* §XIV.[1e] (Ground 2 Element [1e]).

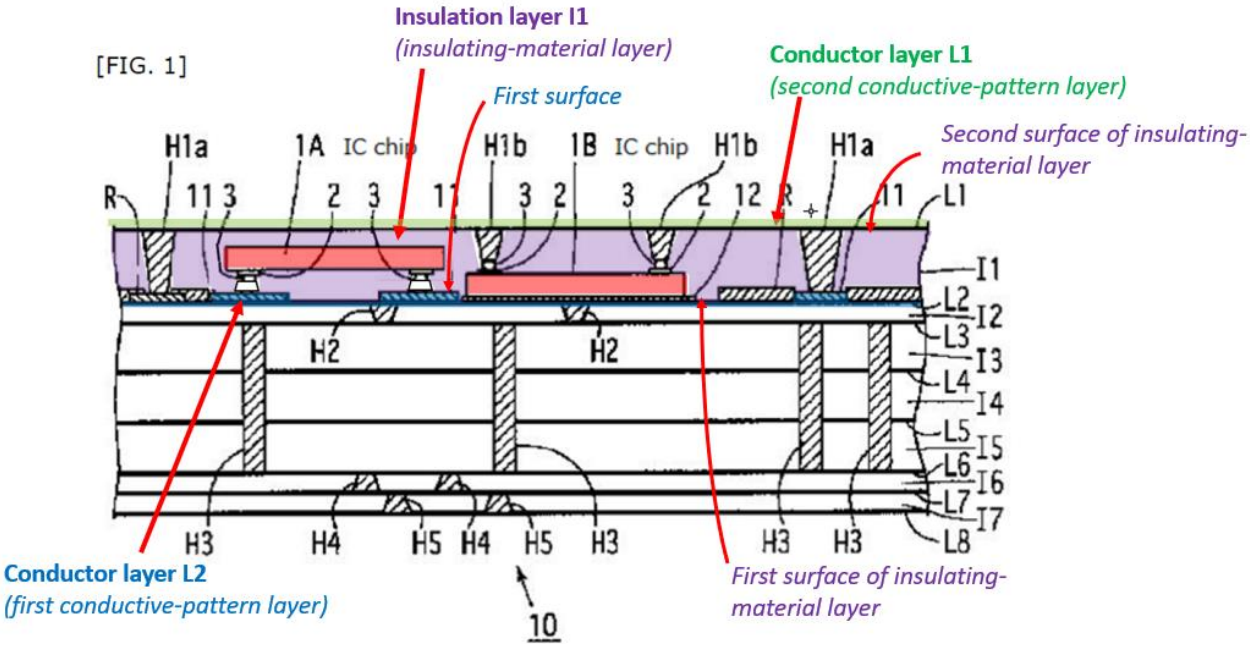


APPLE-1013, FIG. 1 (annotated, modified to include tower bumps taught by Onda)

236. Accordingly, Yoneyama describes that the insulating-material layer has a first surface where it is formed on conductor layer L2 and a second surface where conductor layer L1 will be formed. *Id.*, [0017], Figs. 1, 6.

[2b] and the electronic module comprises a second conductive-pattern layer on the second surface of the insulating-material layer.

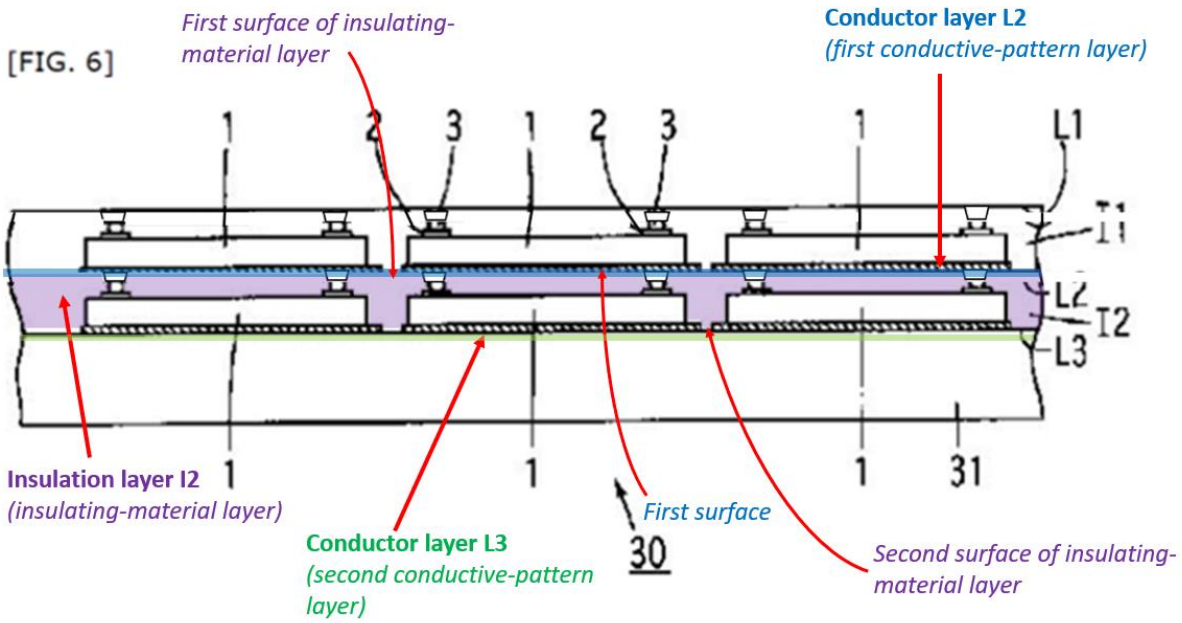
237. With regard to element [2b], Yoneyama describes that the insulating layer I1 is formed on conductor layer L2 and "conductor layer L1 on which a wiring pattern has been formed is formed on the surface of insulating layer I1." APPLE-1013, [0017]; *supra* §XIV.D.[2a] (Ground 2 Element [2a]).



APPLE-1013, FIG. 1 (annotated, modified to include tower bumps as taught by Onda)

238. As shown in FIG. 1, Yoneyama teaches that conductor layer L1 is formed on the second surface of the insulating-material layer. APPLE-1013, [0017], [0011], [0035], [0050], FIG. 1.

239. Yoneyama's FIG. 6 configuration also provides "a second conductive-pattern layer on the second surface of the insulating-material layer." As shown in FIG. 6, insulation layer I1 has a first surface against conductor layer L2 and a second surface against conductor layer L3. APPLE-1013, FIG. 6.



APPLE-1013, FIG. 6 (excerpted and annotated, modified to include tower bumps as taught by Onda)

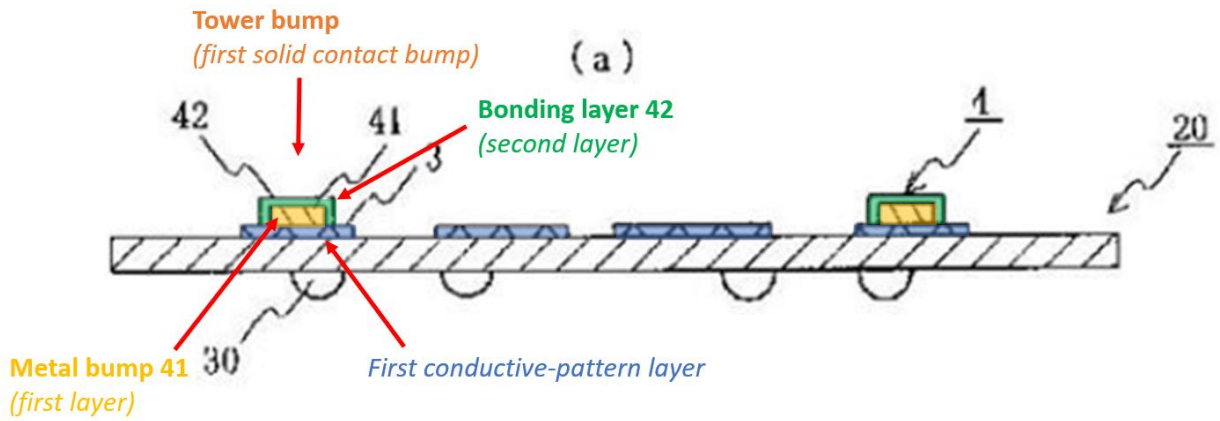
iii. Claim 3

[3] The electronic module of claim 1, wherein the first solid contact bumps include a layered structure, containing at least two layers of at least two different materials.

240. Yoneyama-Onda renders obvious claim [3]. For example, Onda describes that "tower bumps 4 should be made of a conductive material that does not undergo a phase transformation at high temperatures [such as] high-purity gold, copper, and nickel." APPLE-1008, [0042]. Onda further describes that "tower bumps 4 are composed of a metal bump 41 and a bonding layer 42 that bonds to the electrode pads 2 of the semiconductor chip 1…[g]old, solder, or tin

can be used, for example, in the bonding layer 42." APPLE-1008, [0045], [0062]-[0063]. As shown in Onda's FIG. 2 below, Onda teaches that tower bumps ("***first solid contact bumps***") can include a metal bump 41 (first layer) and a bonding layer 42 (second layer). Accordingly, in the Yoneyama-Onda combination, the first solid contact bumps include a layered structure, containing at least two layers, as claimed.

[FIG. 2]



APPLE-1008, FIG. 1B (annotated)

241. Onda discloses that the layered structure of the first contact bump includes a first layer (metal bump 41) of a first material (e.g., copper) and a second layer (bonding layer 42) of a second material (e.g., tin). *See* APPLE-1013, [0071]-[0080]. Onda offers other options for materials forming the bonding layer, including solder, gold, and aluminum. APPLE-1008, [0042], [0137], [0071]-

[0080] (describing gold-tin bonding using tin-plated copper bumps to connect to gold bumps on the semiconductor chip), [0099]-[0105] (describing gold-gold bonding using gold-plated copper bumps to connect to gold bumps on the semiconductor chip), [0106]-[0110] (describing gold-aluminum bonding using aluminum-plated copper bumps to connect to gold bumps on the semiconductor chip).

242. Additionally, Onda offers multiple options for materials forming each of the metal bump and the bonding layer, and it would have been obvious to a POSITA to select two different materials, for example, a gold metal bump (as Yoneyama describes) and a tin bonding layer, as Onda teaches. APPLE-1013, [0033] (describing the use of gold bumps for connecting the IC chips to the wiring circuit); APPLE-1008, [0042] (describing that tower bumps can be formed from materials like " high-purity gold, copper, and nickel"), [0137] ("a bonding layer 42 is formed on the metal bumps 41 [which] can be gold, tin, solder, etc., depending on the connection method used"), [0071]-[0080]. A POSITA would have been motivated to implement Onda's bonding layer to facilitate bonding between the tower bump and gold bump, and would have been further motivated to select materials for the tower bump components of metal bump and bonding layer that comprise different materials for a variety of reasons including cost-reduction by

selecting a bonding layer of gold and a metal bump layer of a less expensive material such as copper, as Onda describes. APPLE-1008, [0099]-[0105] (describing gold-gold bonding using gold-plated copper bumps to connect to gold bumps on the semiconductor chip); APPLE-1035, 138-139. A POSITA would have had a reasonable expectation of success in selecting combinations of materials for the metal bump and plating layer, because Onda describes the use of multiple combinations. A POSITA would have understood that the selection of materials involves trade-offs in material properties, cost, and other characteristics, and it would have been well within the level of skill of the POSITA to make such a decision.

243. Accordingly, in the Yoneyama-Onda combination, tower bumps (***first solid contact bumps***) include a metal bump and a bonding layer (***a layered structure***) with at least two layers of two different materials.

iv. Claim 4

[4] The electronic module of claim 1, wherein the component is a microcircuit.

244. Yoneyama-Onda renders obvious claim [4]. For example, Yoneyama describes "a circuit board with embedded electronic components" like "a semiconductor integrated circuit chip with active surfaces on which a plurality of external connection electrodes have been formed." APPLE-1013, [0001], [0004]

("semiconductor integrated circuit chips, bare chips, and semiconductor devices are referred to below as 'IC chips.'"), [0024] ("the electronic components are semiconductor integrated circuit chips").

245. Yoneyama's disclosure of a semiconductor integrated circuit chip is similar to the microcircuits that the '527 patent describes. For example, the '527 patent discusses that "the installation base in microcircuit manufacturing techniques, i.e., the substrate, is of a semiconductor material." APPLE-1001, 1:41-49. Indeed, a POSITA would have understood that "microcircuit" was a well-known term for "[a] miniaturized, electronic circuit, such as is found on an integrated circuit." APPLE-1032, 3; *see also* APPLE-1033, 3 (definition of 'microcircuit': "A synonym for integrated circuit (IC)"); APPLE-1031, 3, (including a definition of 'microcircuit' of "An integrated circuit"); APPLE-1017, 4:14-20 ("an electronic microcircuit card, of the type incorporating a contact assembly of package which has on one face a metal layer having the contacts of the card and which includes at least one integrated circuit."). Accordingly, Yoneyama-Onda's semiconductor integrated circuit chip provides a microcircuit.

v. Claim 5

[5] The electronic module of claim 1, wherein the component is entirely protected inside the insulating-material layer.

246. Yoneyama-Onda renders obvious claim [5]. For example, Yoneyama describes "a circuit board with embedded electronic components." APPLE-1013, [0002], [0020], [0021], Figs. 1, 6; APPLE-1001, 5:4-11, 7:19-32. In particular, Yoneyama describes a method for preparing the circuit board with embedded components in which "the second electrical insulating layer in the second step is formed by coating and then curing an insulating resin such that the thickness of the second electrical insulating layer is greater than the thickness of the fixed first electronic component and equal to or slightly less than the thickness of the second electronic component up to the plurality of external connection electrodes." APPLE-1013, [0026], [049] ("an insulating resin is printed on both mounted IC chips 1A and 1B to a thickness that is a little less than that of the IC chips 1A and 1B, and cured to form insulating layer.").

247. The electronic components embedded in the insulating layer of the circuit board in Yoneyama-Onda is similar to the "one or more components embedded in an installation base" in the '527 patent. APPLE-1001, 1:16-17, ("the components… are installed on their installation base, such as a circuit board,

during the manufacture of the base, so that the base structure[] is … manufactured around the component"), 7:59-61 ("The component can then be embedded entirely inside the installation base while the electronic module will be even on both surfaces"), FIGS. 4-9. Just as in the '527 patent, the IC chips in Yoneyama are positioned in the circuit board during manufacture so that the chips are embedded entirely in the board while the module has flat surfaces on the top and bottom. APPLE-1013, [0001] ("a circuit board with embedded electronic components… in which electronic components such as a semiconductor integrated circuit chip … are mounted inside"), [0021] ("mounting at least two electronic components… on a substrate surface on which a wiring circuit has been formed, forming an insulation layer over the electronic components, and forming an electrical conductor layer on the surface of the insulation layer."), [0016]-[0017], FIGS. 1, 6. Accordingly, just as the components embedded in the circuit board's insulation layer in the '527 patent are entirely protected inside the insulating-material layer, so too are the electronic components of Yoneyama-Onda entirely protected inside the insulating layer as claimed.

vi. Claim 6

[6a] The electronic module of claim 1, wherein the insulating-material layer comprises a first surface and a second surface, the first surface being against the first conductive-pattern layer,

248. *See supra* §XIV.D.[2a] (Ground 2 Element [2a]).

[6b] and the electronic module comprises a conductive film on the second surface of the insulating-material layer for protecting the component against electromagnetic radiation.

249. Yoneyama-Onda renders obvious claim element [6b]. For example, as described above, Yoneyama describes that a "conductor layer L1 on which a wiring pattern has been formed is formed on the surface of insulating layer I1." APPLE-1013, [0017]. Yoneyama further explains how the conductor layer L1 is formed by "a lamination method, such as laminating copper foil with resin or copper foil between prepregs, or a plating method is used." APPLE-1013, [0050], [0011] ("Conductor layer L1 is formed by laminating copper foil with a resin on conductor layer L2 or by plating the same conductor layer"). Copper foil with resin, between prepregs, or with plating provides a "***conductive film***" on the second surface of the insulating layer I1 (***insulating-material layer***).

250. This understanding of Yoneyama's copper foil with resin, between prepregs, or with plating is consistent with the disclosure of the '527 patent, which discusses that a "metal film [] can also be a surfaced metal film, or some other film including several layers or several materials" APPLE-1001, 6:27-29. The '527 patent also discusses that a "conductive film 9, can … be exploited in many ways, such as additional space for conductive patterns and to protect the components 6 and the entire module against electromagnetic radiation [or with] the aid of a second conductive film 9 the structure can be reinforced and warping of the installation base, for example, can be reduced." APPLE-1001, 7:40-46. Yoneyama's copper foil, like the conductive film of the '527 patent, is used to provide conductive wiring circuits by etching or plating the copper foil. APPLE-1013, [0036].

251. The language in [6b] that recites "for protecting the component against electromagnetic radiation" is an intended use of the conductive film that imparts no additional structural limitation that would not already be met by a conductive film. Regardless, each of the structures described in the preceding paragraph that provide the claimed conductive film in Yoneyama do serve to protect the IC chip (***component***) against electromagnetic radiation.

252. Indeed, a POSITA would have understood and found obvious the metallic materials of Yoneyama's conductive film—such as the copper foil—naturally protect the chip from electromagnetic radiation due to the EM shielding properties of the disclosed metals. APPLE-1018, 15:47-16:14 and APPLE-1019, [0025].

253. For example, a POSITA would have been aware that the use of a metal layer positioned above an electronic module shields the component. APPLE-1018, 15:52-16:9 ("The metal layer provides a shield at the top surface" of the module which is "preferably aluminum …[though o]ther metals… can be used"), 16:9-14 ("One micron of aluminum provides good hermetic protection plus some electromagnetic shielding, at reasonable cost. Depending on the severity of the electromagnetic environment, it may be desirable to substantially increase the thickness for effective shielding performance."); APPLE-1019, [0025] (describing of a "metallic cover layer" such as a "metallic cap… employed as shielding layers against electromagnetic radiation"). Kurita, for example, describes that it was well-known to use a metal plate with larger surface area than the semiconductor component, "connected to the ground potential" so that the "electromagnetic noise that would normally infiltrate into the semiconductor device 47 from outside the multi-layer substrate 65 is absorbed by the shield section 28 [so that the EM noise]

does not penetrate into the semiconductor device 47." APPLE-1043, [0112], [0114]-[0116]. A POSITA would have found it obvious that Yoneyama's structures including the copper foil with resin, between prepregs, or with plating, shield the IC chip from electromagnetic radiation and thus "protect[] the component against electromagnetic radiation" as claimed.

vii. Claim 7

[7] The electronic module of claim 1, comprising a plurality of components having flat contact zones metallurgically and electrically connected to the first solid contact bumps made on the first surface of the first conductive-pattern layer by means of said second solid contact bumps.

254. Yoneyama-Onda renders claim [7] obvious. For example, Yoneyama describes "a plurality of IC chips 1 are mounted face-up by flip-chip bonded of the surface of a substrate 31 made of a material described above on conductor layer L3 on which a wiring pattern [h]as been formed by a means used in semiconductor processing." APPLE-1013, [0017], [0025] ("a circuit board with embedded electronic components having a structure in which at least two first and second electronic components with active surfaces on which a plurality of external connection electrodes have been arranged are mounted on a substrate surface covered with an electrical conductor layer on which a wiring circuit has been

formed"). "Therefore, each electronic component mounted on each conductor layer is connected by way of vias H2, H3, and H4, which become components of electronic circuits." *Id.*, [0039]. Accordingly, Yoneyama discloses a plurality of components with flat contact zones mounted on the wiring circuit of the conductor layer.

255. Based on Yoneyama's disclosure, it would have been obvious to a POSITA that Yoneyama teaches the use of multiple IC chips embedded within a circuit board structure, where each of the IC chips may be connected according to the technique taught by the Yoneyama-Onda combination in which a pair of metal bumps couple the IC chips to the wiring pattern of the circuit board. *Supra* §XIV.C (Yoneyama-Onda Combination). Accordingly, Yoneyama-Onda provides "***a plurality of components having flat contact zones metallurgically and electrically connected to the first solid contact bumps made on the first surface of the first conductive-pattern layer by means of said second solid contact bumps***," as claimed.

viii. Claim 8

[8] The electronic module of claim 7, wherein the plurality of components are electrically connected to each other by means of the first conductive-pattern layer.

256. Yoneyama-Onda renders claim [8] obvious. For example, Yoneyama describes "the present invention is a circuit board with embedded electronic components obtained by mounting at least two electronic components with active surfaces on which a plurality of external connection electrodes have been arranged on a substrate surface on which a wiring circuit has been formed." APPLE-1013, [0021], FIG. 6. Yoneyama describes that "[e]ach conductor layer L1-L8 has the required circuit pattern, and the required chip-shaped electronic components are connected to these circuit patterns as necessary." *Id.*, [0015], [0042] (same). Yoneyama makes clear that "each electronic component mounted on each conductor layer is connected by way of vias H2, H3, and H4, which become components of electronic circuits." *Id.*, [0039].

257. It would have been obvious to a POSITA that Yoneyama's components, each coupled to the wiring circuit of the conductor layer ("***first conductive-pattern layer***") as described above, would have also been ***electrically***

connected to each other by means of the first conductive-pattern layer as claimed. *Supra* §XIV.D.[7] (Ground 2 Claim [7]).

258. Additionally, a POSITA also would have found that provision of an electrical connection between a pair of IC chips to be an obvious design choice that would be readily achieved using the conventional wiring patterns and interconnection techniques described in Yoneyama. *Id.* For example, a POSITA would have electrically connected Yoneyama's components to enable communication of data signals between the components. *See supra* §IV.A.

ix. Claim 9

[9] The electronic module of claim 1, wherein the insulating-material layer is a glass-fiber reinforced epoxy sheet.

259. Yoneyama-Onda renders obvious claim [9]. For example, Yoneyama describes that "[e]ach one of insulating layers I2 to I7 is composed of glass cloth impregnated with a thermosetting resin such as an epoxy resin." APPLE-1013, [0011], [0034] (same).

260. To the extent the presence of glass fibers are not explicitly disclosed in layer I1, they were nonetheless conventional and well-known, as evidenced by their use in Yoneyama's insulating layer I2-I7. *See e.g.*, APPLE-1021, 59 ("The multilayer printed circuit laminate consists of two or more copper clad epoxy glass

laminates… bonded together with prepreg which has, in turn, been manufactured from woven glass fabric and epoxy resin."), 60; APPLE-1022, 18. A POSITA would have understood from Yoneyama's description of the layer I2-I7 that insulating layers can be formed from glass cloth impregnated with a thermosetting resin such as an epoxy resin." APPLE-1013, [0011], [0034]. Despite Yoneyama not explicitly describing insulating layer I1 as being formed from the glass cloth and epoxy resin, it would have been obvious to a POSITA to implement Yoneyama's insulating layer I1 with the "large amount of filler" being a glass-reinforced epoxy sheet as in layers I2-I7, and a POSITA would have been motivated to do so to provide an economical insulating material between conductive layers and to realize production efficiencies and cost savings that ordinarily result from re-use of the same or similar materials across different parts of a device (especially since layers I2-I7 can already include a glass-reinforced epoxy sheet according to Yoneyama, and layer I1 can already include epoxy resin and fillers). APPLE-1013, [0035], [0011], [0034]; APPLE-1035, 141-142 (listing relative costs of epoxy, fiber materials, and composite materials such as epoxy prepregs). A POSITA would have reasonably expected success because doing so would have merely involved substitution of a known insulating material for another to yield predictable results. *See* APPLE-1013, [0035] (discussing both

materials as insulator materials for use in insulating layers); APPLE-1035, 98-100 (discussing requirements for materials used to encapsulate microelectronic packages), 141-142. Accordingly, Yoneyama-Onda render obvious implementing the insulating-material layer with a glass-fiber reinforced epoxy sheet.

x. Claim 10

[10] The electronic module of claim 1, wherein the insulating-material layer is a flexible organic sheet.

261. Yoneyama-Onda renders obvious claim [10]. For example, as described above, Yoneyama describes that "[e]ach one of insulating layers I2 to I7 is composed of glass cloth impregnated with a thermosetting resin such as an epoxy resin." APPLE-1013, [0011], [0034] (same). Yoneyama describes that the "insulating layer I1 is formed by mixing a large amount of filler with a thermosetting resin such as epoxy resin." *Id.*, [0011]. A POSITA would have appreciated that epoxy is an organic substance, and that an insulating layer formed with epoxy and filler material provides an organic layer having at least some flexibility and thus providing a flexible organic sheet. Accordingly, a POSITA would have understood that Yoneyama's description of the layer I1 provides the claimed flexible organic sheet – particularly as the '527 patent does not provide any definition of what characteristic makes a sheet "flexible."

262. To the extent that Yoneyama does not explicitly disclose the use of a flexible organic sheet in insulating layer I1, the use of flexible organic sheets as insulating materials were nonetheless conventional and well-known by the Critical Date. *See* APPLE-1042, [0031] ("For the insulating resin substrate used in the circuit board of the present invention, an organic insulating substrate can be used"), [0106]-[0107] (describing the use of a sheet-like resin between conductive layers of a circuit board); APPLE-1008, [0037]; APPLE-1007, [0012] (describing "a tape-like film of such as polyimide"), [0100] (describing materials suitable for use in an organic film for the support); APPLE-1009, [0005]-[0006] (describing a polyimide tape), [0012]; APPLE-1021, 45. As another example, Onda describes additional insulating materials that can be used in the insulation layer, including flexible sheets such as "a base film of polyimide or a liquid crystal polymer." APPLE-1008, [0037], [0045], [0052], [0060], [0073], [0086]. In view of Yoneyama's description of the insulating layers as comprising epoxy and the fact that the use of flexible organic sheets as insulating layers was well-known, it would have been obvious to a POSITA to implement Yoneyama's insulating layer I1 as a flexible organic sheet. Indeed, the '572 patent lists many potential materials that are suitable for forming the insulating material layer. APPLE-1001,

8:3-10 (describing suitable materials for the insulating-material layer including polyimide).

263. It would have been obvious to a POSITA to implement Yoneyama's insulating layer I1 with a flexible organic sheet given that such materials were well-known insulating materials, and a POSITA would have been motivated to do so to provide an economical insulating material between conductive layers and to expand the functionality of the printed circuit board by allowing the circuit board to flex and better conform to external stresses that would commonly occur in the handling of an electronic module. APPLE-1013, [0035]. Yoneyama describes that "[e]ach one of insulating layer I2 to I7 is composed of glass cloth impregnated with a thermosetting resin such as an epoxy resin, and insulation layer I1 is formed by mixing a large amount of filler with a thermosetting resin such as an epoxy resin so that stress relaxation can occur during curing." *Id.*, [0011]. While Yoneyama suggests that the circuit board be created as "a rigid and unbending substrate structure" (*id.*), it was well-known and conventional to implement one or more layers of a circuit board with a flexible layer to provide a flexi-rigid board. APPLE-1021, 24. For example, "it is possible to replace one or more of the rigid layers with a flexible layer, usually made on a polyimide base." *Id.*

264. The use of a flexible organic sheet also would have been an obvious design choice that a POSITA would have been selected to accommodate known uses and applications of electronic devices that benefit from additional flexion in the device. For example, such flexible layers provide a variety of functionalities, for example, by "extend[ing] beyond the profile of the rigid area of the board to serve as a connection to a component which is not co-planar with the board face," "act[ing] as a hinge between two rigid areas" or "carry[ing] electrical signals to a moving part of an equipment." *Id.* A POSITA would have been motivated to implement Yoneyama's insulating layer I1 as a flexible layer comprising a "flexible organic sheet" because doing so was well-known and conventionally implemented to add functionalities to the circuit board as I described. Furthermore, the replacement of the layer I1 with a flexible organic sheet would not necessarily reduce the characteristic of Yoneyama's board as providing "a rigid and unbending substrate structure," given that the underlying layers I2-I7 also provide rigid layers using a thermosetting resin. APPLE-1013, [0011].

265. A POSITA would have reasonably expected success because doing so would have merely involved substitution of a known insulating material for another to yield predictable results. APPLE-1001, 8:3-10. Accordingly,

Yoneyama-Onda render obvious that the insulating-material layer is a glass-fiber reinforced epoxy sheet.

xi. Claim 11

[11] The electronic module of claim 1 wherein the metallurgically electrical connection are ultrasonic or thermo-compression connections.

266. Regardless of the scope of the limitation "metallurgically electrical connections," Yoneyama-Onda renders obvious claim [12] at least because Yoneyama-Onda describes the preferred embodiments of the '527 patent. APPLE-1001, 6:41-49, 6:961-63, 6:50-54. For example, as explained above (*supra* §§XIV.D Ground 2 Elements [1b], [1d], [1f-ii]), in the Yoneyama-Onda combination, the metal bumps and the tower bumps are connected metallurgically and electrically using a thermo-compression method as Yoneyama and Onda describe. *Supra* §XIV.C (Yoneyama-Onda Combination); APPLE-1008, [0068] ("after preparing the wiring substrate 20… and aligning the plurality of electrode pads 2 and tower bumps 4 formed on the main surface of the semiconductor chip 1, the semiconductor chip 1 is fixed" after which "a heating tool is used to heat… and a pressurizing tool is used to apply pressure… to cause a metal diffusion reaction and establish a connection"); *see also* APPLE-1013, [0048] (describing that during bonding of the chip to the circuit board, "IC chip 1A is temporarily fixed by a

bonding device, followed by final pressure bonding"); APPLE-1009, [0007], [0012]-[0013] (explaining a bonding process using ultrasonic vibrations, heat and thermocompression). As described above, and as acknowledged in the ''527 patent, the use of thermocompression and ultrasonic bonding techniques were well-known by the Critical Date and were used to provide metallurgical and electrical connections between components and circuitry. *Supra* §IV.B; APPLE-1001, 6:46-48 ("Methods and equipment for ultrasonic bonding are commercially available."), 6:63-65 ("Methods and equipment for thermo-compression bonding are also commercially available").

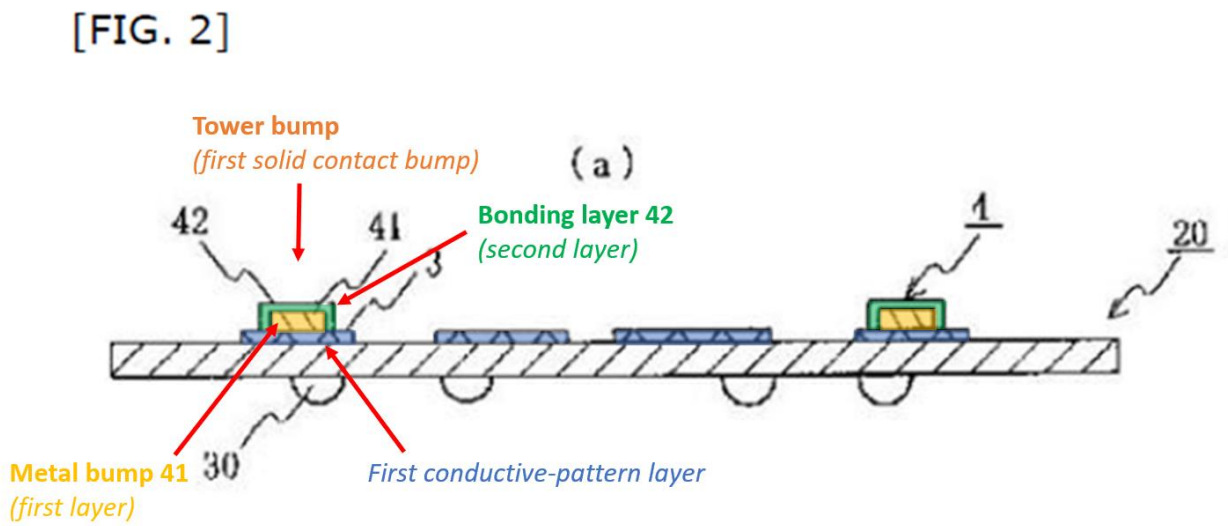
267. Based on the disclosures of Yoneyama and Onda regarding the use of bonding techniques using heat and pressure, Yoneyama-Onda provides that "***the metallurgically electrical connection are ultrasonic or thermo-compression connections***" as claimed.

xii. Claim 12

[12] The electronic module of claim 11 wherein the metallurgically electrical connections are facilitated by the presence of one or more metals selected from the group consisting of copper, aluminum, gold and tin.

268. Regardless of the scope of the limitation "metallurgically electrical connections," Yoneyama-Onda renders obvious claim [12]. For example, in the

combination, the tower bumps "comprise metal bumps that buffer the thermal stress generated between the insulating substrate and the semiconductor chip, and a plating layer for bonding that establishes an electrical connection with the semiconductor chip provided on the metal bumps" as Onda teaches. APPLE-1008, [0018], [0045], [0062]-[0063], FIG. 2; *supra* §XIV.C (Yoneyama-Onda Combination); *see also* §XIV.C.[3] (Ground 2 Claim [3]). Onda describes that "tower bumps 4 are composed of a metal bump 41 and a bonding layer 42 that bonds to the electrode pads 2 of the semiconductor chip 1…[g]old, solder, or tin can be used, for example, in the bonding layer 42." APPLE-1008, [0045], [0006].



APPLE-1008, FIG. 1B (annotated)

269. As an example, Onda describes "gold bumps are provided on the plurality of electrode pads, a tin plating layer for bonding is provided on the tower

bumps, and the electrical connections are composed of gold-tin junctions utilizing the melting point (217°C) at the first eutectic point due to the gold and tin." APPLE-1008, [0020], [0137] ("a bonding layer 42 is formed on the metal bumps 41 [which] can be gold, tin, solder, etc., depending on the connection method used"), [0071]-[0083], [0006], FIG. 6. Onda offers various options for materials forming the bonding layer between the tower bump and metal bump, including solder, gold, and aluminum. APPLE-1008, [0042], [0137], [0071]-[0080] (describing gold-tin bonding using tin-plated copper bumps to connect to gold bumps on the semiconductor chip), [0099]-[0105] (describing gold-gold bonding using gold-plated copper bumps to connect to gold bumps on the semiconductor chip), [0106]-[0110] (describing gold-aluminum bonding using aluminum-plated copper bumps to connect to gold bumps on the semiconductor chip). Yoneyama describes that "solder bumps or gold bumps 2 are formed on multiple electrode pads on [the IC chip] active surfaces." APPLE-1013, [0033].

270. Onda and Yoneyama describe the use of materials including gold, copper, tin and aluminum to connect the IC chip to the wiring pattern. Accordingly, Yoneyama-Onda teach that the connections between the metal bumps and tower bumps are facilitated by the presence of metals such as copper, aluminum, gold and tin, as claimed.

xiii. Claim 13

[13pre] An electronic module, comprising:

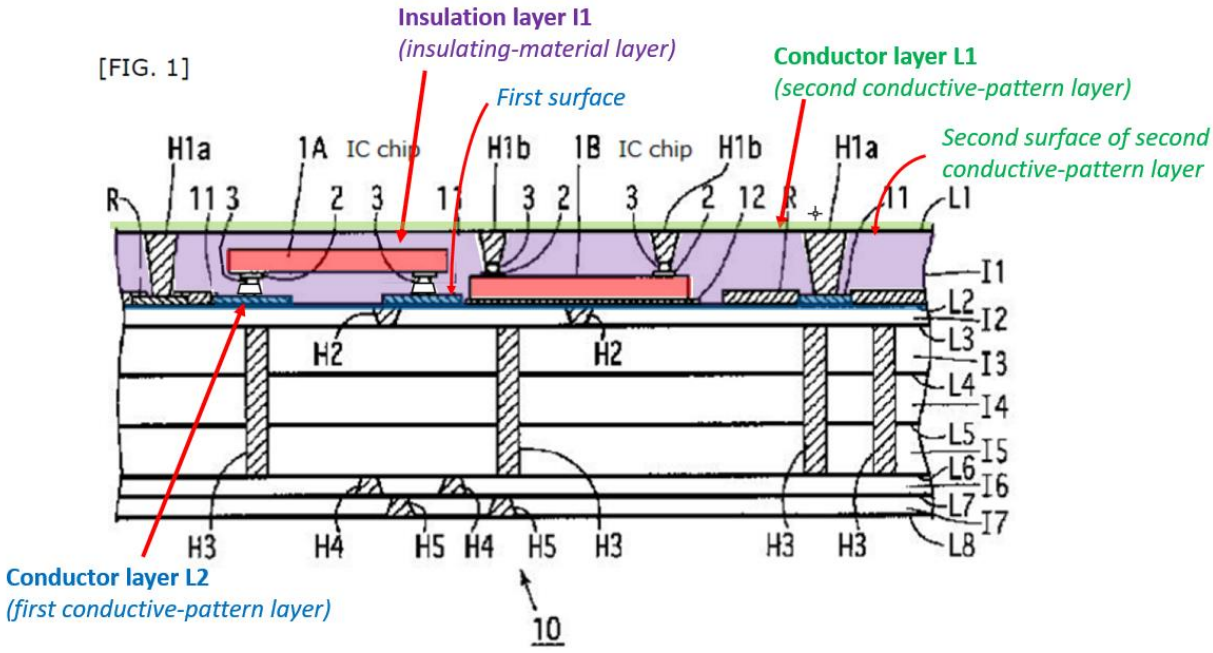
271. *See supra* §XIV.D.[1pre] (Ground 2 Element [1pre]).

[13a] a first conductive-pattern layer having a first surface,

272. *See supra* §XIV.D.[1a] (Ground 2 Element [1a]).

[13b] a second conductive-pattern layer having a second surface,

273. *See supra* §XIV.[2b] (Ground 2 Claim [2b]). As described above, Yoneyama's conductor layer L1 provides a "***second conductive-pattern layer***" which has ***a second surface*** as claimed. APPLE-1013, [0017], FIGS. 1, 6.

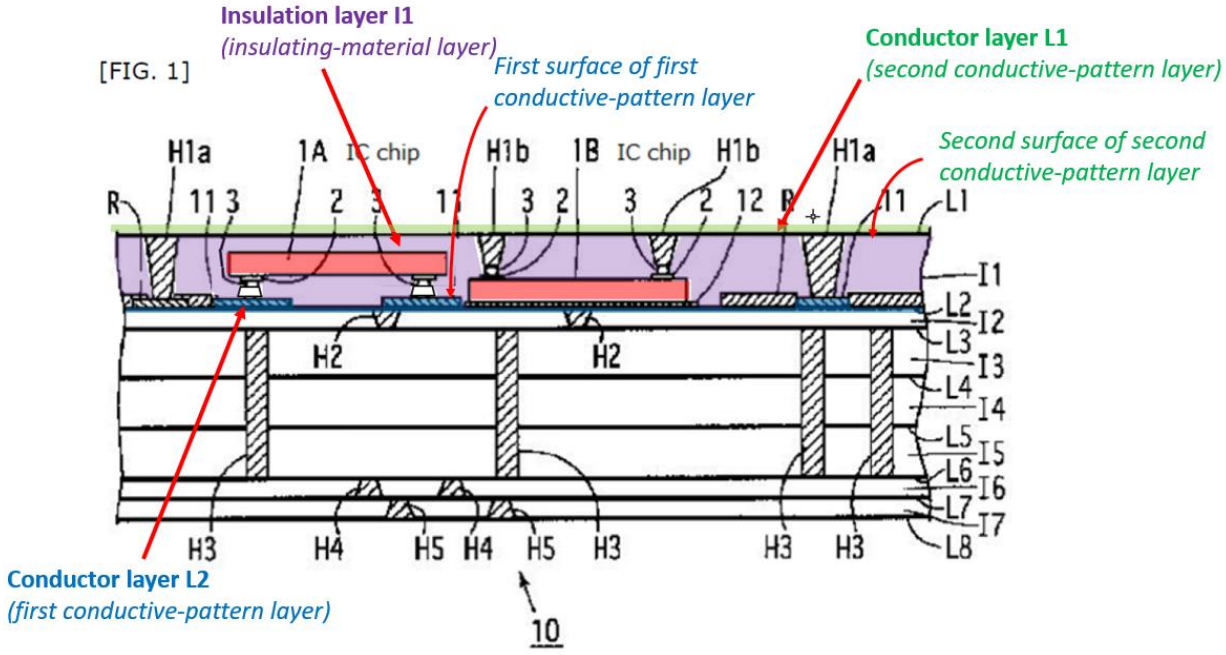


APPLE-1013, FIG. 1 (annotated, modified to include tower bumps as taught by Onda)

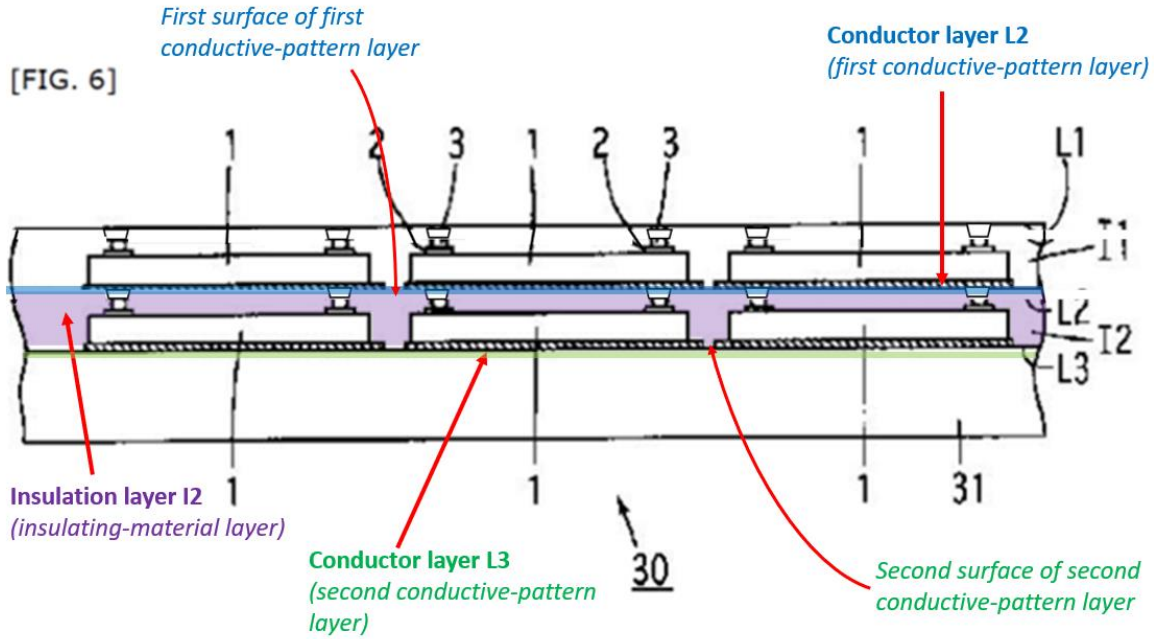
274. As shown above in FIG. 1, the conductor layer L1 has a second surface oriented toward the IC chips. Although not shown here (though *see infra* §XIV.D.[13c]), the second conductive-pattern layer in the configuration of FIG. 6 also has a second surface oriented toward the IC chips.

[13c] an insulating-material layer between the first surface of the first conductive-pattern layer and the second surface of the second conductive-pattern layer,

275. *See supra* §§XIV.D.[1e], [2a]-[2b] (Ground 2 Element [1e], Claim [2a]-[2b]). As described above, Yoneyama's insulating layer I1is formed on the conductive layer L2 (***"first conductive-pattern layer"***) and is covered by conductive layer L1 (***"second conductive-pattern layer"***). APPLE-1013, [0011], [0001], [0017], [0021], [0026], [0035], [0049], FIGS. 1, 6.



APPLE-1013, FIG. 1 (annotated, modified to include tower bumps as taught by Onda)



APPLE-1013, FIG. 6 (annotated, modified to include tower bumps as taught by Onda)

276. As shown above, in either of the configurations shown in FIGS. 1 and 6, Yoneyama's insulating layer I1 ("insulating-material layer") is ***between the first surface of the first conductive-pattern layer and the second surface of the second conductive-pattern layer***, as claimed. APPLE-1013, FIGS. 1, 6.

[13d] first solderless contact bumps made on the first surface of the first conductive-pattern layer and metallurgically and electrically connected thereto,

277. *See supra* §XIV.D.[1b] (Ground 2 Element [1b]).

[13e] a component having fiat contact zones embedded in the insulating-material layer,

278. *See supra* §§XIV.D.[1c], [1f-i] (Ground 2 Elements [1c] and [1f-i]).

[13f] second solderless contact bumps made on the flat contact zones and metallurgically and electrical connected thereto, and

279. *See supra* §XIV.D.[1d] (Ground 2 Element [1d]).

[13g] wherein the flat contact zones of the component are metallurgically, electrically and solderlessly connected to the first solderless contact bumps made on the first surface of the first conductive-pattern layer by means of the second solderless contact bumps made on said flat contact zones.

280. *See supra* §XIV.D.[1f-i]-[1f-ii] (Ground 2 Elements [1f-i]-[1f-ii]).

xiv. Claim 14

[14] The electronic module of claim 13, wherein the first solderless contact bumps include a layered structure, containing at least two layers of at least two different materials.

281. *See supra* §XIV.D.[3] (Ground 2 Claim [3]).

xv. Claim 15

[15] The electronic module of claim 14, wherein the component is a microcircuit.

282. *See supra* §XIV.D.[4] (Ground 2 Claim [4]).

xvi. Claim 16

[16] The electronic module of claim 13, wherein the second conductive-pattern layer is configured to protect the component against electromagnetic radiation.

283. *See supra* §XIV.D.[6b] (Ground 2 Claim [6b]).

xvii. Claim 17

[17] The electronic module of claim 13, comprising a plurality of components having flat contact zones and second solderless contact bumps made on the flat contact zones, the flat contact zones being metallurgically and electrically connected to the first contact bumps made on the first surface of the first conductive-pattern layer by means of said second solderless contact bumps.

284. *See supra* §XIV.D.[7] (Ground 2 Claim [7]).

xviii. Claim 18

[18] The electronic module of claim 17, wherein the plurality of components includes at least one microcircuit, and the plurality of components are electrically connected to each other by means of the first conductive-pattern layer.

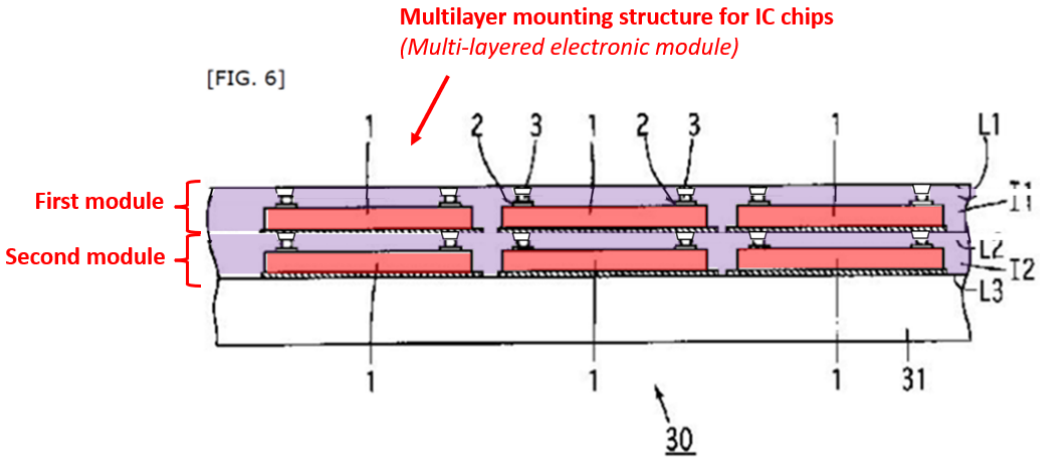
285. *See supra* §XIV.D.[4], [8] (Ground 2 Claims [4], [8]).

xix. Claim 19

[19pre] A multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein at least one of the modules of said plurality comprises:

286. The preamble of claim 19 is not limiting on the elements of the claim. However, to the extent that the preamble is found to be limiting, Yoneyama-Onda

renders obvious claim element [19pre]. For example, Yoneyama describes, with regard to the FIG. 6 configuration, a "multilayer mounting structure" in which "identical IC chips are stacked in multiple layers." APPLE-1013, [0016]-[0018], [0015] ("Each conductor layer L1-L8 has the required circuit pattern"), [0042] (same). Such multi-layer modules were well-known by the Critical Date. *Supra* §IV.A; APPLE-1039, 11:12-22, FIG. 4; APPLE-1038, [0105], FIG. 11; APPLE-1042, FIGS. 4-5.



APPLE-1013, FIG. 6 (annotated, modified to include tower bumps as taught by Onda)

287. For example, Yoneyama describes with regard to FIG. 6 "a plurality of IC chips 1 are mounted face-up by flip chip bonded of the surface of a substrate 31 made of a material described above on conductor layer L3 on which a wiring pattern [h]as been formed." *Id.*, [0017]. After an insulating layer is formed around

the IC chip, "conductor layer L2 on which a wiring pattern has been formed is formed on the surface of insulating layer I2 in the same manner as described above [and] a plurality of IC chips 1 are mounted face-up on the surface of conductor layer L2 by flip chip bonding." *Id*. Accordingly, Yoneyama-Onda provides "***a multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other***" as claimed. *Id.*, FIG. 6.

[19a] a first conductive-pattern layer having a first surface,

288. *See supra* §XIV.D.[1a] (Ground 2 Element [1a]).

[19b] first solderless contact bumps made on the first surface of the first conductive-pattern layer,

289. *See supra* §XIV.D.[1b] (Ground 2 Element [1b]).

[19c] an insulating-material layer on the first surface of the first conductive-pattern layer, and

290. *See supra* §XIV.D.[1e] (Ground 2 Element [1e]).

[19d] a component embedded in the insulating-material layer and having flat contact zones,

291. *See supra* §§XIV.D.[1c], [1f-i] (Ground 2 Elements [1c] and [1f-i]).

[19e] second solderless contact bumps made on the flat contact zones of the component,

292. *See supra* §XIV.D.[1d] (Ground 2 Element [1d]).

[19f] wherein, the flat contact zones of the component are metallurgically and electrically connected to the first conductive-pattern layer via the first solderless contact bumps made on the first surface of the first conductive-pattern layer and the second solderless contact bumps made on the flat contact zones of the component.

293. *See supra* §XIV.D.[1f-ii] (Ground 2 Element [1f-ii]).

xx. Claim 20

[20] The multi-layered electronic module according to the claim 19, comprising a plurality of memory circuits.

294. Yoneyama-Onda renders claim [20] obvious. For example, Yoneyama describes that a "future application [of the multilayer IC chip mounting structure] is in memory modules, since identical IC chips are stacked in multiple layers." APPLE-1013, [0018].

295. Further, it would have been obvious to implement Yoneyama-Onda as a plurality of memory circuits based on Yoneyama's suggestion, and a POSITA would have been motivated to do so for a variety of reasons, First, a POSITA

would have recognized that a memory circuit is one of a limited number of options of possible functions of the integrated circuit. APPLE-1013, [0018]; APPLE-1032, 4 (definition of "chip" including applications "as processors and memory in computers and countless consumer and industrial products"). Second, a POSITA would have understood that Yoneyama's high-density mounting would be advantageously used for memory circuits. APPLE-1013, [0030], [0058], [0003]; APPLE-1042, [0028]-[0029]. A POSITA would have recognized that memory circuits benefit from high connection density, and would have been motivated to implement Nishiuma-Nakatani's integrated circuits as memory circuits as a result.

296. Third, implementing integrated circuits as multiple memory circuits as taught by Yoneyama would have been obvious as a predictable application of a known technique. A POSITA would have understood that memory circuits were well-known and conventional by the Critical Date. APPLE-1032, 4; APPLE-1042, [0029]. A POSITA would have reasonably expected success implementing the combination for all of the reasons described above.

297. Accordingly, Yoneyama-Onda renders obvious a multi-layered electronic module comprising a plurality of memory circuits.

xxi. Claim 21

[21] The multi-layered electronic module according to claim 19, wherein the electronic modules are electrically connected to each other in order to form a multilayered functioning totality.

298. Yoneyama-Onda renders claim [21] obvious. For example, Yoneyama describes with respect to FIG. 5 that "[t]he other pads 21 on conductor layer L2 are connected to conductor layer L1 by way of vias H1 [and] conductor layer L2 is connected to conductor layer L3 by way of vias," such that each conductor layer is connected to adjacent layers by vias. APPLE-1013, [0013]. "Each conductor layer L1-L8 has the required circuit pattern, and the required chip-shaped electronic components are connected to these circuit patterns as necessary." *Id.*, [0015]; *see also id.*, [0042]. "Thus, vias are provided to ***electrically connect*** the necessary conductor layers through their respective insulation layers" so that the electronic modules are electrically connected to form a functioning totality. *Id.*, [0014]. Yoneyama accordingly describes that the electronic modules stacked on adjacent conductive layers are electrically connected to one another by vias so as to form a multilayered functioning totality.

299. Yoneyama's FIG. 6 configuration differs from FIG. 5 in that the IC chips in FIG. 6 are mounted face-up (*see* APPLE-1013, [0016]), but a POSITA

would have understood and found obvious that similar structures for interconnecting layers of the device as provided in FIG. 5 would similarly apply to FIG. 6 in order to provide a functioning multilayer device. A POSITA would have sought to electrically connect the electronic modules in Yoneyama's FIG. 6 configuration to achieve known and predictable advantages of such interconnections, including to enable communication between IC chips in different layers/modules of the device via electrical connections made through the inter-layer/module connections. *See e.g.*, APPLE-1042, FIG. 4.

xxii. Claim 22

[22pre] A multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein each of said plurality of electronic modules comprises:

300. *See supra* §XIV.D.[19pre] (Ground 2 Element [19pre]).

[22a] a first conductive-pattern layer having a first surface,

301. *See supra* §XIV.D.[1a] (Ground 2 Element [1a]).

[22b] first solderless contact bumps made on the first surface of the first conductive-pattern layer,

302. *See supra* §XIV.D.[1b] (Ground 2 Element [1b]).

[22c] an insulating material layer on the first surface of the first conductive-pattern layer, and

303. *See supra* §XIV.D.[1e] (Ground 2 Element [1e]).

[22d] a component embedded in the insulating-material layer, the component having flat contact zones,

304. *See supra* §§XIV.D.[1c], [1f-i] (Ground 2 Elements [1c] and [1f-i]).

[22e] second solderless contact bumps made on the flat contact zones of the component, and

305. *See supra* §XIV.D.[1d] (Ground 2 Element [1d]).

[22f] wherein the flat contact zones of the component are metallurgically, electrically and solderlessly connected to the first conductive-pattern layer by means of the second solderless contact bumps made on the flat contact zones and the first solderless contact bumps made on the first surface of the first conductive-pattern layer.

306. *See supra* §XIV.D.[1f-ii] (Ground 2 Element [1f-ii]).

xxiii. Claim 23

[23] The multi-layered electronic module according to claim 22, comprising a plurality of memory circuits.

307. *See supra* §XIV.D.[20] (Ground 2 Claim [20]).

xxiv. Claim 24

[24] The multi-layered electronic module according to claim 22, wherein the electronic modules are electrically connected to each other in order to form a multi-layered functioning totality.

308. *See supra* §XIV.D.[21] (Ground 2 Claim [21]).

xxv. Claim 25

[25pre] A multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein at least one of the modules of said plurality comprises:

309. *See supra* §XIV.D.[19pre] (Ground 2 Element [19pre]).

[25a] a first conductive-pattern layer having a first surface,

310. *See supra* §XIV.D.[1a] (Ground 2 Element [1a]).

[25b] a second conductive-pattern layer having a second surface,

311. *See supra* §§XIV.D.[2a]-[2b], [13b] (Ground 2 Claim [2a]-[2b], Element [13b]).

[25c] an insulating-material layer between the first surface of the first conductive-pattern layer and the second surface of the second conductive-pattern layer,

312. *See supra* §§XIV.D.[1e], [2a]-[2b], [13c] (Ground 2 Element [1e], Claim [2a]-[2b], Element [13c]).

[25d] first solid contact bumps solderlessly made on the first surface of the first conductive-pattern layer and metallurgically and electrically connected thereto,

313. *See supra* §XIV.D.[1b] (Ground 2 Element [1b]).

[25e] a component having flat contact zones embedded in the insulating-material layer,

314. *See supra* §§XIV.D.[1c], [1f-i] (Ground 2 Elements [1c] and [1f-i]).

[25f] second solid contact bump solderlessly made on the flat contact zones and metallurgically and electrically connected thereto, and

315. *See supra* §XIV.D.[1d] (Ground 2 Element [1d]).

[25g] wherein the first solid contact bumps such that the flat contact zones of the component are metallurgically and electrically connected to the first conductive pattern layer via respective first and second solid contact bumps.

316. *See supra* §XIV.D.[1f-ii] (Ground 2 Element [1f-ii]).

xxvi. Claim 26

[26] The multi-layered electronic module according to claim 25, comprising a plurality of memory circuits.

317. *See supra* §XIV.D.[20] (Ground 2 Claim [20]).

xxvii. Claim 27

[27] The multi-layered electronic module according to claim 25, wherein the electronic modules are electrically connected to each other in order to form a multi-layered functioning totality.

318. *See supra* §XIV.D.[21] (Ground 2 Claim [21]).

XV. ADDITIONAL REMARKS

319. I currently hold the opinions expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

XVI. LISTING OF CLAIMS

Claim 1	
[1pre]	An electronic module, comprising:
[1a]	a first conductive-pattern layer having a first surface,
[1b]	first solid contact bumps solderlessly made on the first surface of the first conductive-pattern layer and metallurgically and electrically connected thereto,
[1c]	a component having flat contact zones,
[1d]	second solid contact bumps solderlessly made on the flat contact zones and metallurgically and electrically connected thereto, and
[1e]	an insulating-material layer on the first surface of the first conductive-pattern layer,
[1f-i]	wherein the component is embedded in the insulating-material layer
[1f-ii]	and wherein the second solid contact bumps made on the flat contact zones of the component are metallurgically, electrically and solderlessly connected to the first solid contact bumps made on the first surface of the first conductive-pattern layer.
Claim 2	
[2a]	The electronic module of claim 1, wherein the insulating-material layer comprises a first surface and a second surface, the first surface being against the first conductive-pattern layer,
[2b]	and the electronic module comprises a second conductive-pattern layer on the second surface of the insulating-material layer.
Claim 3	

[3]	The electronic module of claim 1, wherein the first solid contact bumps include a layered structure, containing at least two layers of at least two different materials.
Claim 4	
[4]	The electronic module of claim 1, wherein the component is a microcircuit.
Claim 5	
[5]	The electronic module of claim 1, wherein the component is entirely protected inside the insulating-material layer.
Claim 6	
[6a]	The electronic module of claim 1, wherein the insulating-material layer comprises a first surface and a second surface, the first surface being against the first conductive-pattern layer,
[6b]	and the electronic module comprises a conductive film on the second surface of the insulating-material layer for protecting the component against electromagnetic radiation.
Claim 7	
[7]	The electronic module of claim 1, comprising a plurality of components having flat contact zones metallurgically and electrically connected to the first solid contact bumps made on the first surface of the first conductive-pattern layer by means of said second solid contact bumps.
Claim 8	
[8]	The electronic module of claim 7, wherein the plurality of components are electrically connected to each other by means of the first conductive-pattern layer.
Claim 9	
[9]	The electronic module of claim 1, wherein the insulating-material layer is a glass-fiber reinforced epoxy sheet.

Claim 10	
[10]	The electronic module of claim 1, wherein the insulating-material layer is a flexible organic sheet.
Claim 11	
[11]	The electronic module of claim 1 wherein the metallurgically electrical connection are ultrasonic or thermo-compression connections.
Claim 12	
[12]	The electronic module of claim 11 wherein the metallurgically electrical connections are facilitated by the presence of one or more metals selected from the group consisting of copper, aluminum, gold and tin.
Claim 13	
[13pre]	An electronic module, comprising:
[13a]	a first conductive-pattern layer having a first surface,
[13b]	a second conductive-pattern layer having a second surface,
[13c]	an insulating-material layer between the first surface of the first conductive-pattern layer and the second surface of the second conductive-pattern layer,
[13d]	first solderless contact bumps made on the first surface of the first conductive-pattern layer and metallurgically and electrically connected thereto,
[13e]	a component having fiat contact zones embedded in the insulating-material layer,
[13f]	second solderless contact bumps made on the flat contact zones and metallurgically and electrical connected thereto, and

[13g]	wherein the flat contact zones of the component are metallurgically, electrically and solderlessly connected to the first solderless contact bumps made on the first surface of the first conductive-pattern layer by means of the second solderless contact bumps made on said flat contact zones.
Claim 14	
[14]	The electronic module of claim 13, wherein the first solderless contact bumps include a layered structure, containing at least two layers of at least two different materials.
Claim 15	
[15]	The electronic module of claim 14, wherein the component is a microcircuit.
Claim 16	
[16]	The electronic module of claim 13, wherein the second conductive-pattern layer is configured to protect the component against electromagnetic radiation.
Claim 17	
[17]	The electronic module of claim 13, comprising a plurality of components having flat contact zones and second solderless contact bumps made on the flat contact zones, the flat contact zones being metallurgically and electrically connected to the first contact bumps made on the first surface of the first conductive-pattern layer by means of said second solderless contact bumps.
Claim 18	
[18]	The electronic module of claim 17, wherein the plurality of components includes at least one microcircuit, and the plurality of components are electrically connected to each other by means of the first conductive-pattern layer.
Claim 19	

[19pre]	A multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein at least one of the modules of said plurality comprises:
[19a]	a first conductive-pattern layer having a first surface,
[19b]	first solderless contact bumps made on the first surface of the first conductive-pattern layer,
[19c]	an insulating-material layer on the first surface of the first conductive-pattern layer, and
[19d]	a component embedded in the insulating-material layer and having flat contact zones,
[19e]	second solderless contact bumps made on the flat contact zones of the component,
[19f]	wherein, the flat contact zones of the component are metallurgically and electrically connected to the first conductive-pattern layer via the first solderless contact bumps made on the first surface of the first conductive-pattern layer and the second solderless contact bumps made on the flat contact zones of the component.
Claim 20	
[20]	The multi-layered electronic module according to the claim 19, comprising a plurality of memory circuits.
Claim 21	
[21]	The multi-layered electronic module according to claim 19, wherein the electronic modules are electrically connected to each other in order to form a multilayered functioning totality.
Claim 22	
[22pre]	A multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein each of said plurality of electronic modules comprises:

[22a]	a first conductive-pattern layer having a first surface,
[22b]	first solderless contact bumps made on the first surface of the first conductive-pattern layer,
[22c]	an insulating material layer on the first surface of the first conductive-pattern layer, and
[22d]	a component embedded in the insulating-material layer, the component having flat contact zones,
[22e]	second solderless contact bumps made on the fiat contact zones of the component, and
[22f]	wherein the flat contact zones of the component are metallurgically, electrically and solderlessly connected to the first conductive-pattern layer by means of the second solderless contact bumps made on the fiat contact zones and the first solderless contact bumps made on the first surface of the first conductive-pattern layer.
Claim 23	
[23]	The multi-layered electronic module according to claim 22, comprising a plurality of memory circuits.
Claim 24	
[24]	The multi-layered electronic module according to claim 22, wherein the electronic modules are electrically connected to each other in order to form a multi-layered functioning totality.
Claim 25	
[25pre]	A multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein at least one of the modules of said plurality comprises:
[25a]	a first conductive-pattern layer having a first surface,
[25b]	a second conductive-pattern layer having a second surface,

[25c]	an insulating-material layer between the first surface of the first conductive-pattern layer and the second surface of the second conductive-pattern layer,
[25d]	first solid contact bumps solderlessly made on the first surface of the first conductive-pattern layer and metallurgically and electrically connected thereto,
[25e]	a component having flat contact zones embedded in the insulating-material layer,
[25f]	second solid contact bump solderlessly made on the flat contact zones and metallurgically and electrically connected thereto, and
[25g]	wherein the first solid contact bumps such that the flat contact zones of the component are metallurgically and electrically connected to the first conductive pattern layer via respective first and second solid contact bumps.
Claim 26	
[26]	The multi-layered electronic module according to claim 25, comprising a plurality of memory circuits.
Claim 27	
[27]	The multi-layered electronic module according to claim 25, wherein the electronic modules are electrically connected to each other in order to form a multi-layered functioning totality.

APPENDIX A

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PROFESSIONAL SUMMARY

Russel Jacob Baker (R. Jacob Baker), Ph.D., P.E. (IEEE Student Member 1983, Member 1988, Senior Member 1997, and Fellow 2013) was born in Ogden, Utah, on October 5, 1964. He received the B.S. and M.S. degrees in electrical engineering from the University of Nevada, Las Vegas (UNLV) in 1986 and 1988. He received the Ph.D. degree in electrical engineering from the University of Nevada, Reno (UNR) in 1993. His Google Scholar profile is here and his ResearchGate profile is here.

From 1981-1987 he served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division). From 1985-1993 he worked for E. G. & G. Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapons tests at the Nevada Test Site. During this time he designed, and oversaw the fabrication and the electrical/mechanical manufacture of, over 30 electronic and electro-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame- and bit-syncs for high-speed imaging, data converters, streak-camera sweep circuits, Pockels cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics. From 1991-1993 he was an adjunct faculty member in the Departments of Electrical Engineering at UNLV and UNR. From 1993-2000 he served on the faculty in the Department of Electrical Engineering at the University of Idaho (UI), first as an untenured assistant professor and then from 1998 as a tenured associate professor. In 2000 he joined a new electrical and computer engineering (ECE) program at Boise State University (BSU) where he was promoted to professor in 2002. He then served as the ECE department chair from 2004-2007. At BSU he helped establish graduate programs in ECE including, in 2006, the university's second PhD degree. In 2012 he rejoined the faculty at UNLV as a tenured full professor of ECE. During his tenure at the UI, BSU, and UNLV he has been the major professor to more than 100 graduate students.

Dr. Baker has done consulting for over 200 companies. His research/development activities are in: photonics, circuit design for wireless and wired communications, analog-to-digital/digital-to-analog data conversion and transmission, optoelectronics (imagers, displays, LIDARs, APDs, SiPMs, and associated electronics), analog and digital integrated circuit design and fabrication, design of diagnostic electrical and electro-optic instrumentation for scientific research, integrated electrical/biological circuits and systems, array (memory, imagers, and displays) fabrication and design, design of digital processors for signal processing, CAD tool development and online tutorials, low-power interconnect and packaging (electrical and optical) techniques, design of wired/wireless communication and interface circuits, circuit design for the use and storage of renewable energy, power electronics and power supply design, and the delivery of online engineering education. As a result of this work, he is the named inventor on over 150 US patents and the author of over 100 publications.

He is a member of the honor societies Eta Kappa Nu and Tau Beta Pi, a licensed Professional Engineer, a popular lecturer that has delivered over 50 invited talks around the world, an IEEE Fellow, and the author of the books CMOS Circuit Design, Layout, and Simulation, CMOS Mixed-Signal Circuit Design, and a coauthor of DRAM Circuit Design: Fundamental and High-Speed Topics. He received the 2000 Best Paper Award from the IEEE Power Electronics Society,

the 2007 Frederick Emmons Terman Award, the 2011 IEEE Circuits and Systems Education Award, and the 2021 Wiley-IEEE Press Textbook Award for the 4th Edition of his book CMOS Circuit Design, Layout, and Simulation.

His service activities include the IEEE Press Editorial Board (1999-2004), editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015), the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), Distinguished Lecturer for the SSCS (2012-2015), Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the IEEE Solid-State Circuits Magazine, IEEE Kirchhoff Award Committee (2020-2023), and advisor for the student branch of the IEEE at UNLV (2013-2024).

INDUSTRY EXPERIENCE

2008 - present: Expert witness in intellectual property disputes in electrical, electro-optic, and computer engineering matters for: 1) district court and ITC patent disputes, 2) inter partes reviews at the PTAB, and 3) arbitrations and mediations.

2013 - 2022: Worked with Freedom Photonics, Santa Barbara, CA, on the integration, fabrication and design, of optoelectronics with CMOS integrated circuits. Work includes the design of compact optical transceivers for range finding applications, high-efficiency integrated silicon avalanche photodetectors for quantum key receivers, Geiger mode SiGe receivers for long-range communications, cryptography, and the fabrication of near-infrared focal plane arrays. Packaging and testing of numerous chips fabricated in both CMOS and SiGe technologies using LEDs, ILDs, PIN, APDs, and ROICs.

2017 - 2019: Worked with Vorpal Research Systems, Las Vegas, NV on the design of integrated circuit electronics and optoelectronics for optical transceivers used in LIDARs/LADARs.

2016 - 2019: Worked with Attollo Engineering on the design of transient digitizers for the capture of high-speed signals for range finders using LEDs and lasers in compact optical transceivers.

2013 - 2018: Working with Mission Support and Test Services, LLC (MSTS, formerly National Security Technologies, LLC, [NSTec]) on the Design and Fabrication of Integrated electrical/photonic application specific integrated circuit (ASIC) design for use in the implementation of diagnostic instrumentation.

2013 - 2015: Consultant for OmniVision. Working on integrating CMOS image sensors (CIS) with memory for very high-speed consumer imager products. Design specialty DRAM, high-speed interfaces between CIS and DRAM, packaging techniques to pair the CIS with DRAM.

2010 - 2013: Worked with Arete' Associates on the design of high-speed compressive transimpedance amplifiers for LADAR projects and the design of ROIC unit cells. Work funded by the U. S. Air Force.

2013: Cirque, Inc. Consulting on the design of analog-to-digital interfaces for capacitive touch displays and pads.

2012: Consultant at Lockheed-Martin Santa Barbara Focal Plane Array. CMOS circuit design and fabrication for the development and manufacture of infrared components and imaging systems with an emphasis on highest sensitivity Indium Antimonide (InSb) focal plane arrays (FPAs) in linear through large staring formats. Product groups include FPAs, integrated dewar assemblies (IDCAs), camera heads, high-speed interfaces between image processors and imaging systems, and infrared imaging systems.

2010 - 2012: Working with Aerius Photonics (and then FLIR Inc. when Aerius was purchase by FLIR) on the design of Focal Plane Arrays funded (SBIRs and STTRs) by the U.S. Air Force, Navy, and Army. Experience with readout integrated circuits (ROICs) and the design/layout of photodetectors in standard CMOS.

2009 - 2010: Sun Microsystems, Inc. (and then Oracle) VLSI research group. Provided consulting on memory circuit design/fabrication and proximity connection (PxC) interfaces to DRAMs and SRAMs for lower power, 3D packaging, for memory modules and controllers implemented with FPGAs and custom ASICs.

2009 - 2010: Contour Semiconductor, Inc. Design of NMOS voltage and current references as well as the design of a charge pump for an NMOS memory chip.

1994 - 2008: Affiliate faculty (Senior Designer), Micron Technology. Designed CMOS circuits for DRAMs including DLLs, PLLs for embedded processors, voltage references and regulators, data converters, field-emitting display drivers, sensing for MRAM (using delta-sigma data conversion topologies), SRAMs, RFIDs, CMOS active pixel imagers and sensors, power supply design (linear and switching), input buffers, etc. Worked on a joint research project

between Micron and HP labs in magnetic memory fabrication and design using the MTJ memory cell. Worked on numerous technologies ranging from LED lighting to medical imaging using CMOS image sensors (too many to list) resulting in numerous US patents (see following list). Considerable experience working with product engineering to ensure high-yield from the production line from fabrication to test. Co-authored a book on DRAM circuit design through the support of Micron. Gained knowledge in the entire memory design process from fabrication to packaging. Developed, designed, and tested circuit design techniques for multi-level cell (MLC) Flash memory using signal processing.

January 2008: Consultant for Nascentric located in Austin, TX. Provide directions on circuit operation (DRAM, memory, and mixed-signal) for fast SPICE circuit simulations.

May 1997 - May 1999: Consultant for Tower Semiconductor, Haifa, Israel. Designed CMOS integrated circuit cells for various modem chips, interfaces, and serial buses including USB circuits, charging circuits based upon power up/down circuits using an MOS or bandgap reference, pre-amplifiers, comparators, etc.

Summer 1998: Consultant for Amkor Wafer Fabrication Services, Micron Technology, and Rendition, Inc., Design PLLs and DLLs for custom ASICs and processors.

Summers 1994 - 1995: Micron Display Inc. Designing phase locked loop for generating a pixel clock for field emitting displays and a NTSC to RGB circuit on chip in NMOS. These displays are miniature color displays for camcorder and wrist watch size color television. Worked on the fabrication and design of video peripheral circuits for these displays.

September - October 1993: Lawrence Berkeley Laboratory. Designed and constructed a 40 A, 2 kV power MOSFET pulse generator with a 3 ns rise-time and 8 ns fall-time for driving Helmholtz coils.

Summer 1993: Lawrence Livermore National Laboratory, Nova Laser Program. Researched picosecond instrumentation, including time-domain design for impulse radar and imaging.

December 1985 - June 1993: (from July 1992 to June 1993 employed as a consultant while finishing up my Ph.D.), E.G.&G. Energy Measurements Inc., Nevada, Senior Electronics Design Engineer. Responsible for the design and manufacturing of instrumentation used in support of Lawrence Livermore National Laboratory's Nuclear Test Program. Responsible for designing and fabricating over 30 electronic and electro-optic instruments including: CCD camera design, communication networks, fiber optic transmitters employing high speed laser drive electronics, receivers employing envelop tracking for DC voltage restoration and regeneration of received information, receiver low noise amplifier design, frame synchronizers for re-assembling transmitted images, high-speed SRAM memory system design with battery back-up, calibration equipment design such as a tunnel diode pulse generator for testing compensation of oscilloscopes and DAC design for calibrating CCD readout electronics, power supply and battery charger designs, sweep circuits for streak cameras, Pockel's cell drive electronics, vertical amplifier design using HBTs for analog oscilloscopes used at the Nevada Test Site, and 10 kV ramp designs using a planar triode to name some of the designs.

This position provided considerable fundamental grounding in EE with a broad exposure ranging from the design of PC boards to, for example, the design of cable equalizers. Summarizing, gained experience in circuit design technologies including: bipolar, vacuum tubes (planar triodes for high voltages), hybrid integrated circuit fabrication and design, GaAs (high speed logic and HBTs), Mach-Zehnder interferometers, Pockels cells, krytrons, power MOSFETs, microwave techniques, power supplies, fiber optic transmitters/receivers, etc.

Summer 1985: Reynolds Electrical Engineering Company, Las Vegas, Nevada. Gained hands on experience in primary and secondary power system design, installation and trouble-shooting electric motors on mining equipment.

ACADEMIC EXPERIENCE

January 1991 – present: Professor of Electrical and Computer Engineering at the **University of Nevada, Las Vegas** from August 2012 to present. From January 2000 to July 2012 held various positions at **Boise State University** including: Professor (2003 – 2012), Department Chair (2004 - 2007), and tenured Associate Professor (2000 - 2003). From August 1993 to January 2000 was a tenured/tenure track faculty member at the **University of Idaho**: Assistant Professor (1993 - 1998) and then tenured Associate Professor (1998 - 2000). Lastly, from January 1991 to May 1993 held adjunct faculty positions in the departments of Electrical Engineering at the University of Nevada, Las Vegas and Reno. Additional details:

- Research is focused on analog and mixed-signal integrated circuit fabrication and design. Worked with multi-disciplinary teams (civil engineering, biology, materials science, etc.) on projects that have been funded by EPA, DARPA, NASA, Army, DMEA, Navy, and the AFRL.
- Current and past research and development interests are:
  - Design and packaging of electrical/optical systems (e.g., LiDARs/LADARs) using LEDs, semiconductor lasers, lens for focusing and directing light, integrated circuits, and associated control and communication systems/circuits.
  - Capacitive sensing techniques using delta-sigma modulation and interfacing to sensors
  - Design of high-voltage and energy switching circuits
  - Circuit design and fabrication for the control, use, and storage of renewable energy using thermoelectric generators
  - Design of electrical/biological/optical circuits and systems using electrowetting on dielectric for automating and controlling biological experiments
  - Design of readout integrated circuits (ROICs) for use with focal plane arrays (FPAs)
  - Heterogeneous integration of III-V photonic devices (e.g., FPAs and VCSELs) with CMOS
  - Methods (e.g., 3D packaging and capacitive interconnects) to reduce power consumption in semiconductor memories, memory modules, and digital systems using custom and non-custom (e.g., FPGAs) implementations
  - Analog and mixed-signal circuit fabrication and design for communication systems, synchronization, energy storage, data conversion, and interfaces
  - The design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g., magnetic, chalcogenide)
  - Reconfigurable electronics design and fabrication using nascent memory technologies such as the memristor to implement FPGAs
  - Finding an electronic, that is, no mechanical component, replacement for the hard disk drive using nascent fabrication technologies
  - Power electronics circuit design for consumers and consumer electronics including power management and adaptive control to reduce power consumption
  - Design of bandpass delta-sigma modulators for IQ demodulation in wireless communication systems in OFDM, WiFi, 802.11, Bluetooth, 3G, 4G, etc.
  - University prototyping, fabricating, and packaging of integrated circuits
- Led, as chair, the department in graduate curriculum (MS and PhD), program development, and ABET accreditation visits.
- Worked with established and start-up companies to provide technical expertise and identify employment opportunities for students.
- Held various leadership and service positions including: ECE chair, graduate coordinator, college curriculum committee (chair), promotion and tenure committee, scholarly activities committee, faculty search committee, university level search committees, etc. Collaborate with College of Engineering faculty on joint research projects.
- Taught courses in circuits, analog IC design, digital VLSI design and fabrication, fiber optics, and mixed-signal integrated circuit design to both on- and, via the Internet, off-campus students. Research emphasis in integrated circuit design using nascent technologies.

EDUCATION

- Ph.D. in Electrical Engineering; December 1993; University of Nevada, Reno, GPA 4.0/4.0. Dissertation Title: *Applying power MOSFETs to the design of electronic and electro-optic instrumentation.*
- M.S. and B.S. in Electrical Engineering: May 1986 and May 1988; University of Nevada, Las Vegas. Thesis Title: *Three-dimensional simulation of a MOSFET including the effects of gate oxide charge*.

MEMBERSHIPS IN PROFESSIONAL AND SCHOLARLY ORGANIZATIONS

IEEE (student, 1983; member, 1988; senior member, 1997; Fellow, 2013)
Member of the honor societies Eta Kappa Nu and Tau Beta Pi
Licensed Professional Engineer

HONORS AND AWARDS

- Consolidated Students of the University of Nevada, Las Vegas (CSUN) Faculty Award, 2017
- Tau Beta Pi UNLV Outstanding Professor of the Year in 2013, 2014, 2015 and 2016
- UNLV ECE Department Distinguished Professor of the Year in 2015
- IEEE Fellow for contributions to the design of memory circuits - 2013
- Distinguished Lecturer for the IEEE Solid-State Circuits Society, 2012 - 2015
- IEEE Circuits and Systems (CAS) Education Award - 2011
- Twice elected to the Administrative Committee of the Solid-State Circuits Society, 2011 - 2016
- Frederick Emmons Terman Award from the American Society of Engineering Education - 2007
- President's Research and Scholarship Award, Boise State University - 2005
- Honored Faculty Member - Boise State University Top Ten Scholar/Alumni Association 2003
- Outstanding Department of Electrical Engineering faculty, Boise State 2001
- Recipient of the IEEE Power Electronics Society's Best Paper Award in 2000
- University of Idaho, Department of Electrical Engineering outstanding researcher award, 1998-99
- University of Idaho, College of Engineering Outstanding Young Faculty award, 1996-97

SERVICE

Reviewer for IEEE transactions on solid-state circuits, circuits and devices magazine, education, instrumentation, nanotechnology, VLSI, etc. Reviewer for several American Institute of Physics journals as well (Review of Scientific Instruments, Applied Physics letters, etc.) Board member of the IEEE press (reviewed dozens of books and book proposals). Reviewer for the National Institutes of Health. Technology editor and then Editor-in-Chief for the Solid-State Circuits Magazine.

Led the Department on ABET visits, curriculum and policy development, and new program development including the PhD in electrical and computer engineering. Provided significant University and College service in infrastructure development, Dean searches, VP searches, and growth of academic programs. Provided university/industry interactions including starting the ECE department's advisory board. Held positions as the ECE department Master's graduate coordinator and coordinator for the Sophomore Outcomes Assessment Test (SOAT).

Also currently serves, or has served, on the IEEE Press Editorial Board (1999-2004), as a member of the first Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau, as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), as an Advisory Professor to the School of Electronic and Information Engineering at Beijing Jiaotong University, as a Distinguished Lecturer for the SSCS (2012-2015), as the Technical Program Chair for the IEEE 58th 2015 International Midwest Symposium on Circuits and Systems, MWSCAS 2015, as advisor for the student branch of the IEEE at UNLV (2013-2023), and as the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the *IEEE Solid-State Circuits Magazine*, and IEEE Kirchhoff Award Committee (2020-2023).

ARMED FORCES

From 1981 to 1987 served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division), Honorable Discharge. Military Occupational Specialty (MOS) was Machine Gunner (MOS 0331)

TEXTBOOKS AUTHORED

Baker, R. J., "CMOS Circuit Design, Layout and Simulation, Fourth Edition" *Wiley-IEEE Press*, 1234 pages. ISBN 9781119481515 (2019) **Over 50,000 copies of this book in print.** (Third Edition published in 2010, Revised Second Edition published in 2008, and Second Edition Published in 2005)

Baker, R. J., "CMOS Mixed-Signal Circuit Design," *Wiley-IEEE*, 329 pages. ISBN 978-0470290262 (second edition, 2009) and ISBN 9780471227540 (First Edition published in 2002)

Keeth, B., Baker, R. J., Johnson, B., and Lin, F., "DRAM Circuit Design: Fundamental and High-Speed Topics", *Wiley-IEEE*, 2008, 201 pages. ISBN: 9780470184752

Keeth, B. and Baker, R. J., "DRAM Circuit Design: A Tutorial", *Wiley-IEEE*, 2001, 201 pages. ISBN 0780360141

Baker, R. J., Li, H.W., and Boyce, D.E. "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE*, 1998, 904 pages. ISBN 9780780334168

BOOKS, OTHER (edited, chapters, etc.)

Saxena, V. and Baker, R. J., "Analog and Digital VLSI," chapter in the CRC Handbook on Industrial Electronics, edited by J. D. Irwin and B. D. Wilamowski, *CRC Press*, 2009 second edition.

Baker, R. J., "CMOS Analog Circuit Design," (A self-study course with study guide, videos, and tests.) IEEE Education Activity Department, 2000. ISBN 0-7803-4822-2 (with textbook) and ISBN 0-7803-4823-0 (without textbook)

Baker, R. J., "CMOS Digital Circuit Design," (A self-study course with study guide, videos, and tests.) *IEEE Education Activity Department*, 2000. ISBN 0-7803-4812-5 (with textbook) and ISBN 0-7803-4813-3 (without textbook)

Li, H.W., Baker, R. J., and Thelen, D., "CMOS Amplifier Design," chapter 22 in the CRC VLSI Handbook, edited by Wai-kai Chen, *CRC Press*, 1999 (ISBN 0-8493-8593-8) and the second edition in 2007 (ISBN 978-0-8493-4199-1)

INVITED TALKS AND SEMINARS

Have given over 50 invited talks and seminars at the following locations: AMD (Fort Collins), AMI semiconductor, Arizona State University, Beijing Jiaotong University, Boise State University, Carleton University, Carnegie Mellon, Columbia University, Dublin City University (Ireland), E.G.&G. Energy Measurements, Foveon, the Franklin Institute, Georgia Tech, Gonzaga University, Hong Kong University of Science and Technology, ICSEng Keynote, ICySSS keynote, IEEE Computing and Communication Workshop (CCWC), IEEE Electron Devices Conference (NVMTS), IEEE Workshop on Microelectronics and Electron Devices (WMED), Indian Institute of Science (Bangalore, India), Instituto de Informatica (Brazil), Instituto Tecnológico y de Estudios Superiores de Monterrey (ITESM, Mexico), Iowa State University, Lawrence Livermore National Laboratory, Lehigh University, Lockheed-Martin, Micron Technology, Nascentric, National Semiconductor, Princeton University, Rendition, Saintgits College (Kerala, India), Southern Methodist University, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Temple University, Texas A&M University, Tower Semiconductor (Israel), University of Alabama (Tuscaloosa), University of Arkansas, University of Buenos Aires (Argentina), University of Houston, University of Idaho, University of Illinois (Urbana-Champaign), Université Laval (Québec City, Québec), University of Macau, University of Maryland, Université de Montréal (École Polytechnique de Montréal), Xilinx (Ireland), University of Nevada (Las Vegas), University of Nevada (Reno), University of Toronto, University of Utah, Utah State University, and Yonsei University (Seoul, South Korea).

RESEARCH FUNDING

In-kind, equipment, and other non-contract/grant funding [e.g., MOSIS support, money for travel for invited talks, etc.] not listed.

- Baker, R. J., (2023-2024) "Silicon Germanium (SiGe) Avalanche Photo Diode (APD) Chip," Department of Energy, Mission Support and Test Services (MSTS), LLC, $120,000
- Baker, R. Jacob, (2017-2023) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit," NASA, $29,999 (Phase I), $225,238 (Phase II), and $79,697 (Phase IIE)
- Goldman, J., Menezes, J., and Baker, R. J., (2021-2022) "Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling," UNLV Sports Research & Innovation Initiative. Proof of Concept Grant Program, $50,000
- Baker, R. Jacob, (2019-2021) "Dual-Mode, Extended Near-Infrared, Focal Plane Arrays Fabricated with CMOS Compatible GeSiSn Alloy Materials," DARPA, $149,998
- Baker, R. Jacob, (2018-2020) "Geiger Mode SiGe Receiver for Long-Range Optical Communications," NASA, $99,996

- Baker, R. Jacob, (2019) "Improved Quantum Efficiency Photo-Detector," Navy, $29,999
- Baker, R. Jacob, (2018-2019) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit – Phase I," NASA, $29,999
- Baker, R. Jacob, (2017-2019) "Quantum Cryptography Detector Chip," Defense MicroElectronics Activity (DMEA), $266,029
- Baker, R. Jacob, (2017-2019) "Advanced Printed Circuit Board Design Methods for Compact Optical Transceiver," U.S. Army/DOD, $299,605
- Baker, R. Jacob, (2016-2018) "High-Sensitivity Monolithic Silicon APD and ROIC," U.S. Air Force/DOD, $299,665

DOCTORAL STUDENT SUPERVSION

10. Sachin Namboodiri – A Multi-channel MCP-PMT based Readout Integrated Circuit for LiDAR Applications (2020)
9. Wenlan Wu – High-Speed Radhard Mega-Pixel CIS Camera for High-Energy Physics (2019)
8. Kostas Moutafis – A Highly-Sensitive Global-Shutter CMOS Image Sensor with On-Chip Memory for Hundreds of kilo-frames per second Scientific Experiments (2019)
7. Yiyan Li – Portable High Throughput Digital Microfluidics and On-Chip Bacteria Cultures (2016)
6. Yacouba Moumouni – Designing, Building, and Testing a Solar Thermoelectric Generation, STEG, for Energy Delivery to Remote Residential Areas in Developing Regions (2015)
5. Qawi IbnZayd Harvard – Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design (2011)
4. Vishal Saxena – K-Delta-1-Sigma Modulators for Wideband Analog-to-Digital Conversion (2010)
3. Robert Russell Hay – Digitally-Tunable Surface Acoustic Wave Resonator (2009)
2. Xiangli Li (the first Boise State University College of Engineering PhD graduate) – MOSFET Modulated Dual Conversion Gain CMOS Image Sensors (2008)
1. Feng Lin, Research and Design of Low Jitter, Wide Locking-Range Phase-Locked and Delay-Locked Loops (2000)

MASTERS STUDENT SUPERVISION

91. Jazmine Boloor – Survey of how Irregular Pathways in the Electrical System of the Human Heart Link to Different Heart Arrhythmias (2023)
90. Abraham Lopez – An Avalanche-Transistor-Based Pulse Generator Design For Infrared Laser Applications (2023)
89. David Santiago – Development of an Automated GPIB System for Characterization of SiGe Avalanche Photodiodes (2023)
88. Minsung Cho – Studies of Forward Projection Algorithms and Implementation on PC and FPGA (2023)
87. Armani Alvarez – A Control Integrated Circuit for a Hysteretic Flyback Power Converter (2022)
86. Francisco Mata-carlos – A Wearable Electronic Monitoring Device for Low Pressure Garment Applications and Temperature Analysis for Prevention of Ulceration and Infection (2022)
85. Daniel Senda – Designs and Outcomes of Transcranial Magnetic Stimulation (TMS) and Repetitive Transcranial Magnetic Stimulation (rTMS) Circuits (2021)
84. James Skelly – Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling (2021)
83. Gonzalo Arteaga – Current-mode photon-counting circuit with SiGe BiCMOS input stage (2020)
82. Jason Silic – Design and Fabrication of a 6-bit Current-Mode ADC for Lidar and High-Speed Applications (2020)
81. Brandon Wade (2020)
80. Mario Valles Montenegro – Front-End CMOS Transimpedance Amplifiers on a Silicon Photomultiplier Resistant to Fast Neutron Fluence (2020)
79. Jonathan DeBoy (2018)
78. Dane Gentry – Design, Layout, and Testing of SiGe APDs Fabricated in a BiCMOS Process (2018)
77. James Mellot – Variable Transition Time Inverters in a Digital Delay Line with Analog Storage for Processing Fast Signals and Pulses (2018)
76. Eric Monahan – High Speed Fast Transient Digitizer Design and Simulation (2018)
75. Shada Sharif – Design and Analysis of First and Second Order K-Delta-1-Sigma Modulators in Multiple Fabrication Processes (2018)
74. Vikas Vinayaka – Analysis and Design of Analog Front-End Circuitry for Avalanche Photodiodes (APD) and Silicon Photo-Multipliers (SiPM) in Time-of-Flight Applications (2018)

73. Claire Tsagkari – Design, Fabrication and Testing of a Capacitive Sensor Using Delta-Sigma Modulation (2017)
72. Kevin Buck – Fast Transient Digitizer and PCB Interface (2015)
71. Marzieh Sharbat Maleki (2015)
70. Angsuman Roy – Design, Fabrication and Testing of Monolithic Low-Power Passive Sigma-Delta Analog-to-Digital Converters (2015)
69. Daniel Anderson – Design and Implementation of an Instruction Set Architecture and Instruction Execution Unit for the RZ9 Coprocessor System (2014)
68. Jared Gordon – Design and Fabrication of an Infrared Optical Pyrometer ASIC (2013)
67. Justin Butterfield (2012)
66. Adam Johnson – Methods and Considerations for Testing Resistive Memories (2012)
65. Ben Millemon – CMOS Characterization, Modeling, and Circuit Design in the Presence of Random Local Variation (2012)
64. Justin Wood (2012)
63. Chamunda Ndinawe Chamunda (2011)
62. Gary VanAckern – Design Guide for CMOS Process On-Chip 3D Inductors using Thru-Wafer Vias (2011)
61. Lucien Jan Bissey – High-Voltage Programmable Delta-Sigma Modulation Voltage-Control Circuit (2010)
60. Kaijun Li (2010)
59. Yingting Li (co-supervised with Maria Mitkova) (2010)
58. Lael Matthews (co-supervised with Said Ahmed-Zaid) (2010)
57. Priyanka Mukeshbhai Parikh (2010)
56. Todd Plum (co-supervised with Jeff Jessing) – Design and Fabrication of a Chemicapacitive Sensor for the Detection of Volatile Organic Compounds (2010)
55. Rahul Srikonda (2010)
54. Avani Falgun Trivedi (2010)
53. Kuang Ming Yap – Gain and Offset Error Correction for CMOS Image Sensors using Delta-Sigma Modulation (2010)
52. Mahesh Balasubramanian – Phase Change Memory - Array Development and Sensing Circuits using Delta-Sigma Modulation (2009)
51. Lincoln Bollschweiler (2009)
50. Shantanu Gupta (2009)
49. Qawi Harvard – Wide I_O DRAM Architecture Utilizing Proximity Communication (2009)
48. Avinash Rajagiri (2009)
47. Ramya Ramarapu (2009)
46. Harikrishna Rapole (2009)
45. Aruna Vadla (2009)
44. Hemanth Ande (2008)
43. Curtis Cahoon – Low-Voltage CMOS Temperature Sensor Design using Schottky Diode-Based References (2008)
42. Prashanth Busa (2008)
41. John McCoy III (2008)
40. Dennis Montierth – Using Delta-Sigma-Modulation for Sensing in a CMOS Imager (2008)
39. Rudi Rashwand (2008)
38. Barsha Shrestha (co-supervised with Zhu Han) – Wireless Access in Vehicular Environments using Bit Torrent and Bargaining (2008)
37. Eric Becker – Design of an Integrated Half-Cycle Delay Line Duty Cycle Corrector Delay Locked Loop (2007)
36. Matthew Leslie – Noise-Shaping Sense Amplifier for Cross-Point Arrays (2007)
35. Jose Monje (2007)
34. Sanghyun Park (2007)
33. Vishal Saxena – Indirect Feedback Compensation Techniques for Multi-Stage Operational Amplifiers (2007)
32. Meshack Appikatla (2006)
31. Eric Booth – Wide Range, Low Jitter Delay-Locked Loop Using a Graduated Digital Delay Line and Phase Interpolator (2006)

30. Sucheta Das (2006)
29. Krishna Duvvada – High Speed Digital CMOS Input Buffer Design (2006)
28. Krishnamraju Kurra (2006)
27. Soumya Narasimhan (2006)
26. Roger Porter (2006)
25. David Butler – Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes (2005)
24. Dragos Dimitriu (2005)
23. Surendranath Eruvuru – Sensing Circuit Design for an Ion Mobility Spectrometer (2005)
22. Sandhya Sandireddy (2005)
21. Harish Singidi (2005)
20. Indira Vemula – Delta-Sigma Modulator Used in CMOS Imagers (2005)
19. Bhavana Kollimarla – A 1-Bit Analog-to-Digital Converter Using Delta Sigma Modulation for Sensing in CMOS Imagers (2004)
18. Sandeep Pemmaraju – High Voltage Charge Pump Circuit for an Ion Mobility Spectrometer (2004)
17. Ravindra Puthumbaka – Circuit Design for an Ion Mobility Spectrometer (2004)
16. Brandon Roth – Comparison of Asynchronous vs. Synchronous Design Technologies using a 16-bit Binary Adder (2004)
15. Jennifer Taylor – Reading and Writing Flash Memory Using Delta-Sigma Modulation (2004)
14. Jing Plaisted – Methods for Memory Testing (2003)
13. Murugesh Subramaniam – Flash Memory Sensing Using Averaging (2003)
12. Brian Johnson – Application of an Asynchronous FIFO in a DRAM Data Path (2002)
11. Scott Ward – Electrostatic Discharge (ESD) Protection in CMOS (2002)
10. Tyler Gomm – Design of a Delay-Locked Loop with a DAC-Controlled Analog Delay Line (2001)
9. Gexin Huang (2001)
8. Chris Atkins (2000)
7. Thaddeus Black (2000)
6. Zuxu Qin (2000)
5. Hao Chen (1999)
4. Doug Hackler (co-supervised with Steve Parke) – TMOS: A Novel Design for MOSFET Technology (1999)
3. Song Liu – Design of a CMOS 6-bit Folding and Interpolating Analog-to-Digital Converter (1999)
2. Ben Ba (1997)
1. Brent Keeth – A Novel Architecture for Advanced High Density Dynamic Random Access Memories (1996)

GRANTED US PATENTS

152. Baker, R. J., “Quantizing circuits having improved sensing,” **10,658,018**, May 19, 2020.
151. Baker, R. J., “Quantizing circuits having improved sensing,” **10,403,339**, September 3, 2019.
150. Baker, R. J., “Digital Filters with Memory,” **10,366,744**, July 30, 2019.
149. Baker, R. J., “Quantizing circuits having improved sensing,” **10,127,954**, November 13, 2018.
148. Baker, R. J. and Parkinson, W., “NMOS regulated voltage reference,” **9,753,481**, September 5, 2017.
147. Baker, R. J., “Digital Filters with Memory,” **9,734,894**, August 15, 2017.
146. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **9,697,883**, July 7, 2017
145. Baker, R. J., “Comparators for delta-sigma modulators,” **9,641,193**, May 2, 2017.
144. Baker, R. J., “Quantizing circuits having improved sensing,” **9,449,664**, September 20, 2016.
143. Baker, R. J., “Error detection for multi-bit memory,” **9,336,084**, May 10, 2016.
142. Baker, R. J. and Keeth, B., “Optical interconnect in high-speed memory systems,” **9,299,423**, March 29, 2016.
141. Baker, R. J., “Methods for sensing memory elements in semiconductor devices,” **9,299,405**, March 29, 2016.
140. Baker, R. J., “Comparators for delta-sigma modulators,” **9,135,962**, September 15, 2015.
139. Baker, R. J., “Resistive memory element sensing using averaging,” **9,081,042**, July 14, 2015.
138. Baker, R. J., “Digital Filters with Memory,” **9,070,469**, June 30, 2015.
137. Baker, R. J., "Reference current sources,” **8,879,327**, November 4, 2014.
136. Baker, R. J. and Beigel, K. D., “Multi-resistive integrated circuit memory,” **8,878,274**, November 4, 2014.
135. Baker, R. J., “Methods for sensing memory elements in semiconductor devices,” **8,854,899**, October 7, 2014.

134. Baker, R. J., "Quantizing circuits with variable parameters," **8,830,105**, September 9, 2014.
133. Baker, R. J., "Integrators for delta-sigma modulators," **8,754,795**, June 17, 2014.
132. Baker, R. J., "Methods of quantizing signals using variable reference signals," **8,717,220**, May 6, 2014.
131. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **8,712,249**, April 29, 2014.
130. Baker, R. J., "Resistive memory element sensing using averaging," **8,711,605**, April 29, 2014.
129. Baker, R. J., "Memory with correlated resistance," **8,681,557**, March 25, 2014.
128. Baker, R. J., "Reference current sources," **8,675,413**, March 18, 2014.
127. Baker, R. J., "Methods for sensing memory elements in semiconductor devices," **8,582,375**, November 12, 2013.
126. Linder, L. F., Renner, D., MacDougal, M., Geske, J., and Baker, R. J., "Dual well read-out integrated circuit (ROIC)," **8,581,168**, November 12, 2013.
125. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **8,516,292**, August 20, 2013.
124. Baker, R. Jacob, "Resistive memory element sensing using averaging," **8,441,834**, May 14, 2013.
123. Qawi, Q. I., Drost, R. J., and Baker, R. Jacob, "Increased DRAM-array throughput using inactive bitlines," **8,395,947**, March 12, 2013.
122. Baker, R. Jacob, "Memory with correlated resistance," **8,289,772**, October 16, 2012.
121. Lin, F. and Baker, R. Jacob, "Phase splitter using digital delay locked loops," **8,218,708**, July 10, 2012.
120. Baker, R. Jacob, "Subtraction circuits and digital-to-analog converters for semiconductor devices," **8,194,477**, June 5, 2012.
119. Baker, R. J., "Digital Filters for Semiconductor Devices," **8,149,646**, April 3, 2012.
118. Baker, R. J., "Error detection for multi-bit memory," **8,117,520**, February 14, 2012.
117. Baker, R. J., "Integrators for delta-sigma modulators," **8,102,295**, January 24, 2012.
116. Baker, R. J., "Devices including analog-to-digital converters for internal data storage locations," **8,098,180**, January 17, 2012.
115. Baker, R. J. and Beigel, K. D., "Multi-resistive integrated circuit memory," **8,093,643**, January 10, 2012.
114. Baker, R. J., "Quantizing circuits with variable parameters," **8,089,387**, January 3, 2012.
113. Baker, R. J., "Reference current sources," **8,068,367**, November 29, 2011.
112. Baker, R. J., "Methods of quantizing signals using variable reference signals," **8,068,046**, November 29, 2011.
111. Baker, R. J., "Systems and devices including memory with built-in self-test and methods of making using the same," **8,042,012**, October 18, 2011.
110. Baker, R. J., "Memory with correlated resistance," **7,969,783**, June 28, 2011.
109. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **7,941,056**, May 10, 2011.
108. Baker, R. J., "K-delta-1-sigma modulator," **7,916,054**, March 29, 2011.
107. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,877,623**, January 25, 2011.
106. Lin, F. and Baker, R. J., "Phase splitter using digital delay locked loops," **7,873,131**, January 18, 2011.
105. Hush, G. and Baker, R. J., "Complementary bit PCRAM sense amplifier and method of operation," **7,869,249**, January 11, 2011.
104. Baker, R. J., "Subtraction circuits and digital-to-analog converters for semiconductor devices," **7,839,703**, November 23, 2010.
103. Baker, R. J., "Digital Filters with Memory" **7,830,729**, November 9, 2010.
102. Baker, R. J., "Systems and devices including memory with built-in self test and methods of making using the same," **7,818,638**, October 19, 2010.
101. Baker, R. J., "Integrators for delta-sigma modulators," **7,817,073**, October 19, 2010.
100. Baker, R. J., "Digital filters for semiconductor devices," **7,768,868**, August 3, 2010.
99. Baker, R. J., "Quantizing circuits with variable reference signals," **7,733,262**, June 8, 2010.
98. Baker, R. J., "Quantizing circuits for semiconductor devices," **7,667,632**, February 23, 2010.
97. Baker, R. J., and Beigel, K. D., "Multi-resistive integrated circuit memory," **7,642,591**, January 5, 2010.
96. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,616,474**, November 10, 2009.
95. Baker, R. J., "Resistive memory element sensing using averaging," **7,577,044**, Aug. 18, 2009.

94. Baker, R. J., "Quantizing circuits with variable parameters," **7,538,702**, May 26, 2009.
93. Baker, R. J., "Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors," **7,528,877**, May 5, 2009.
92. Baker, R. J., "Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors," **7,515,188**, April 7, 2009.
91. Taylor, J. and Baker, R. J., "Method and apparatus for sensing flash memory using delta-sigma modulation," **7,495,964**, February 24, 2009.
90. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,489,575**, February 10, 2009.
89. Baker, R. J., "Per column one-bit ADC for image sensors," **7,456,885**, November 25, 2008.
88. Staples, T. and Baker, R. J., "Input buffer design using common-mode feedback," **7,449,953**, November 11, 2008.
87. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,421,607**, September 2, 2008.
86. Baker, R. J., "Methods for resistive memory element sensing using averaging," **7,372,717**, May 13, 2008.
85. Taylor, J. and Baker, R. J., "Method and apparatus for sensing flash memory using delta-sigma modulation," **7,366,021**, April 29, 2008.
84. Hush, G. and Baker, R. J., "Method of operating a complementary bit resistance memory sensor and method of operation," **7,366,003**, April 29, 2008.
83. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,330,390**, February 12, 2008.
82. Baker, R. J., "Input and output buffers having symmetrical operating characteristics and immunity from voltage variations," **7,319,620**, January 15, 2008.
81. Staples, T. and Baker, R. J., "Method and apparatus providing input buffer design using common-mode feedback," **7,310,018**, December 18, 2007.
80. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,286,428**, October 23, 2007.
79. Baker, R. J., and Cowles, T. B., "Method and apparatus for reducing duty cycle distortion of an output signal," **7,271,635**, September 18, 2007.
78. Baker, R. J., and Cowles, T. B., "Method and apparatus for reducing duty cycle distortion of an output signal," **7,268,603**, September 11, 2007.
77. Hush, G., Baker, R. J., and Moore, J., "Skewed sense AMP for variable resistance memory sensing," **7,251,177**, July 31, 2007.
76. Hush, G. and Baker, R. J., "Method of operating a complementary bit resistance memory sensor," **7,242,603**, July 10, 2007.
75. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,237,136**, June 26, 2007.
74. Moore, J. and Baker, R. J., "Rewrite prevention in a variable resistance memory," **7,224,632**, May 29, 2007.
73. Baker, R. J., "Integrated charge sensing scheme for resistive memories," **7,151,698**, December 19, 2006.
72. Baker, R. J., "Adjusting the frequency of an oscillator for use in a resistive sense amp," **7,151,689**, December 19, 2006.
71. Baker, R. J., "Resistive memory element sensing using averaging," **7,133,307**, Nov. 7, 2006.
70. Lin, F. and Baker, R. J., "Phase detector for all-digital phase locked and delay locked loops," **7,123,525**, October 17, 2006.
69. Baker, R. J., and Beigel, K. D., "Integrated circuit memory with offset capacitor," **7,109,545**, September 19, 2006.
68. Baker, R. J., "Input and output buffers having symmetrical operating characteristics and immunity from voltage variations," **7,102,932**, September 5, 2006.
67. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,095,667**, August 22, 2006.
66. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,082,045**, July 25, 2006.
65. Baker, R. J., "System and method for sensing data stored in a resistive memory element using one bit of a digital count," **7,009,901**, March 7, 2006.
64. Hush, G. and Baker, R. J., "Complementary bit resistance memory sensor and method of operation," **7,002,833**, February 21, 2006.
63. Lin, F. and Baker, R. J., "Phase detector for all-digital phase locked and delay locked loops," **6,987,701**, January 17, 2006.

62. Baker, R. J., "Adjusting the frequency of an oscillator for use in a resistive sense amp," **6,985,375**, January 10, 2006.
61. Baker, R. J., "Method for reducing power consumption when sensing a resistive memory," **6,954,392**, October 11, 2005.
60. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **6,954,391**, October 11, 2005.
59. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **6,954,390**, October 11, 2005.
58. Lin, F. and Baker, R. J., "Phase splitter using digital delay locked loops," **6,950,487**, September 27, 2005.
57. Baker, R. J., "Method and apparatus for measuring current as in sensing a memory cell," **6,930,942**, August 16, 2005.
56. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **6,917,534**, July 12, 2005.
55. Baker, R. J., "Dual loop sensing scheme for resistive memory elements," **6,914,838**, July 5, 2005.
54. Baker, R. J., "High speed low power input buffer," **6,914,454**, July 5, 2005.
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- Harvard, Q. I. and Baker, R. J., “Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design,” a presentation covering semiconductor packaging, DRAM architectures, and I/O circuits. The goal of this work is to investigate replacing the currently used dual in-line memory modules (DIMMs) with a smaller and a lower power memory module, a “Nano-Module.”
- Baker, R. J., and Campbell, K. A., “Reconfigurable Analog Electronics using the Memristor.”
- Baker, R. J., and Saxena, V., “A K-Delta 1-Sigma Modulator for Wideband Analog-to-Digital Conversion.”
- Li, K., Saxena, V., and Baker, R. J., "The Baker ADC: An Overview,"
- Saxena, V., and Baker, R. J., "High-Speed Op-Amp Design: Compensation and Topologies for Two and Three Stage Designs,"
- Baker, R. J., "Circuit Design for MLC Flash: Towards a Semiconductor Replacement for the Hard Disk Drive."
- Baker, R. J., Terman Award Acceptance Speech, given at the Frontiers in Education Conference (FIE 2007), Milwaukee, WI, October 11, 2007.
- Baker, R. J., "The One-Transistor, One-Capacitor (1T1C) Dynamic Random Access Memory (DRAM), and its Impact on Society," presented at the Franklin Institute, in the symposium honoring Dr. Robert H. Dennard and his receipt of the 2007 Benjamin Franklin Medal in Electrical Engineering, April 25, 2007.
- Baker, R. J. and Saxena, V., "Design of Bandpass Delta-Sigma Modulators: Avoiding Common Mistakes."
- Baker, R. J., "Sensing Circuits for Resistive Memory."
- Hadrick, M. and Baker, R. J., "Sensing in CMOS Imagers using Delta-Sigma Modulation."

- Baker, R. J., "Design of High-Speed CMOS Op-Amps for Signal Processing," IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED), April, 2005
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31. Loo, S. M., Cole, J., Youngberg, R., Baker, R. J., Gribb, M. M., "Field-programmable gate array in a miniature ion mobility spectrometer sensor system," *Proceedings of the 2006 International Conference on Embedded Systems & Applications*, June 26-29, 2006, Las Vegas, NV.
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29. Duvvada, K., Saxena, V., and Baker, R. J., High Speed Digital Input Buffer Circuits, *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 11-12, April, 2006.
28. Saxena, V., Plum, T. J., Jessing, J. R., and Baker, R. J., "Design and Fabrication of a MEMS Capacitive Chemical Sensor System," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 17-18, April, 2006.
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25. Gribb, M., Hill, H. H., Baker, R. J., Loo, S. M., and Moll, A. J., "Ion Mobility Spectrometer (IMS) Sensor Project," presented at the *Environmental & Subsurface Science Symposium*, Inland Research Alliance, Sept. 19-21, 2005, Big Sky, Montana.
24. Ogas, M. L., Price, P. M., Kiepert J., Baker R. J., Bersuker G., and Knowlton W.B., *Degradation of Rise Time in NAND Gates Using 2.0 nm Gate Dielectrics*, oral presentation and publication at the 2005 IEEE Integrated Reliability Workshop, October 2005.
23. Butler, D. L. and Baker, R. J., *Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes*, *Proceedings of the IEEE 48th International Midwest Symposium on Circuits and Systems*, Aug. 7-10, 2005.
22. Cheek, B. J., Southwick III, R. G., Ogas, M. L., Nagler, P. E., Whelchel, D., Kumar, S., Baker, R. J., and Knowlton, W. B., "Preliminary Soft Breakdown (SBD) Effects In CMOS Building Block Circuits," poster presentation at *2004 IEEE International Integrated Reliability Workshop*, Oct. 18-21, 2004.
21. Ogas, M., Southwick, R. G., Cheek, B. J., Lawrence, C. E., Kumar, S., Haggag, A., Baker, R. J., and Knowlton, W. B., "Multiple Waveform Pulse Voltage Stress Technique for Modeling Noise in Ultra-Thin Oxides," poster presentation at the *Workshop on Microelectronics and Electron Devices*, Boise, Idaho, April 16, 2004.
20. Ogas, M. L., Southwick III, R. G., Cheek, B. J., Baker, R. J., Bersuker, G., and Knowlton, W. B., "Survey of Oxide Degradation in Inverter Circuits Using 2.0nm MOS Devices," in *Proceedings of the 2004 IEEE International Integrated Reliability Workshop*, pp. 32-36.
19. Cheek, B. J., Stutzke, N., Santosh, K., Baker, R. J., Moll, A. J., and Knowlton, W. B., Investigation of Circuit-Level Oxide Degradation and its Effect on CMOS Inverter Operation Performance and MOSFET Characteristics, *2004 IEEE International Reliability Physics Symposium*, April, 25-29.
18. Stutzke, N., Cheek, B. J., Wiscombe, M., Lowman, T., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Effects of Circuit-Level Stress on Inverter Performance and MOSFET Characteristics*, 2003 IEEE International Integrated Reliability Workshop, Oct, 20-23.
17. Ogas, M. L., Southwick, R. G., Cheek, B. J., Lawrence, C. E., Kumar, S., Haggag, A., Baker, R. J., and Knowlton, W. B., *Investigation of Multiple Waveform Pulse Voltage Stress (MWPVS) Technique in Ultra-Thin Oxides*, poster presentation at the 2003 IEEE International Integrated Reliability Workshop Oct, 20-23.
16. Baker, R. J., *Mixed-Signal Design in the Microelectronics Curriculum,* IEEE University/Government/Industry Microelectronics (UGIM) Symposium, June 30 - July 2.

15. Hartman, J. A., Baker, R. J., Gribb, M., Hill, H. H., Jessing, J., Moll, A. J., Prouty, and Russell, D., *A Miniaturized Ion Mobility Spectrometer (IMS) Sensor for Wireless Operation*, FAME (Frontiers in Assessment Methods for the Environment) Symposium, Sponsored by NSF, Minneapolis, Minnesota, August 10-13, 2003.
14. Lawrence, C.E., Cheek, B. J., Lawrence, T. E., Kumar, S., Haggag, A., Baker, R. J., and Knowlton, W. B., *Gate Dielectric Degradation Effects on nMOS Devices Using a Noise Model Approach*, IEEE University/Government/Industry Microelectronics (UGIM) Symposium, June 30 - July 2, 2003.
13. Cheek, B., Lawrence, C., Lawrence, T., Gomez, J., Caldwell, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Gate Dielectric Degradation Effects on nMOS Devices and Simple IC Building Blocks (SICBBs),* IEEE Electron Devices Society Boise Meeting, Boise, ID Oct. 25, 2002.
12. Lawrence, C., Cheek, B., Caldwell, T., Lawrence, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Pulse voltage stressing of ultrathin gate oxides in NMOS devices, poster session at IEEE International Integrated Reliability Workshop,* October 21-24, 2002.
11. Cheek, B., Lawrence, C., Lawrence, T., Caldwell, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., Circuit level reliability of ultrathin gate oxides for SICBBs: Preliminary study concentrated on the effect of stress on the NMOSFET of an inverter, poster session at the IEEE International Integrated Reliability Workshop, October 21-24, 2002.
10. Baker, R. J., "Sensing Circuits for Resistive Memory," *IEEE Electron Devices Society* Meeting, Boise, Idaho October 25, 2002.
9. Rivera, B., Baker, R. J., Melngailis, J., "Design and Layout of Schottky Diodes in a Standard CMOS Process," 2001 International Semiconductor Device Research Symposium, Washington DC, Dec. 2001.
8. Hess, H. and Baker, R. J., "Easier Method to Simultaneously Trigger Series-Connected MOS Devices," *Power Systems World Conference* 2000, Boston, Massachusetts, September 2000.
7. Baker, R. J., and Hess, H., "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices." *International Electric Machines and Drives Conference,* Seattle, Washington, May 1999, pp. 673-676.
6. Baker, R. J., "A windows based integrated circuit design tool for distance education," *International Conference on Simulation and Multimedia in Engineering Education*."
5. Chen, H. and Baker, R. J., "A CMOS Standard-Cell Library for the PC-based LASI Layout System," *Proceedings of the 41st International Midwest Symposium on Circuits and Systems, August 9-12, 1998.*
4. Liu, S. and Baker, R. J., "Process and temperature performance of a CMOS beta-multiplier voltage reference," *Proceedings of the 41st International Midwest Symposium on Circuits and Systems, August 9-12, 1998.*
3. Boyce, D.E. and Baker, R. J., "A Complete Layout System for the PC," *IEEE 40th International Midwest Symposium on Circuits and Systems*, 1997.
2. Baker, R. J., and Blair, J. J., "Step response considerations and the design of a suitable step generator for high speed digitizer testing," *LLNL's Third Annual Workshop on High Speed Digitizers,* April 3-4, Las Vegas, Nevada, 1991.
1. Baker, R. J., "Step-recovery diodes sharpen pulses," *Engineering Design News Magazine*, pp. 154-156, May 10, 1990.

EXPERT WITNESS EXPERIENCE

The law firms and clients (underlined) whom I have provided expert witness services in electrical and computer engineering are listed below. I have been deposed 109 times, given expert testimony at 14 trials (7 USITC, 2 D. Del., 1 Arbitr., 1 S.D. Cal., 1 N.D. Ga., 1 D. Ore., and 1 E.D. Tex.), and participated in 1 mediation.

Pillsbury Winthrop Shaw Pittman LLP (San Francisco, CA)

Case – *MediaTek, Inc.* v. Redstone Logics LLC

Case Number – IPR2025-00085. Petition filed on October 22, 2024.

Case Subject Matter – multi-core processors with voltage and clock scaling functionality and related communications/control signaling.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declaration.

Baker Botts LLP (Houston, TX)

Case – *Innolux Corporation* v. Phenix Longhorn LLC

Case Numbers – IPR2025-00043 and IPR2025-00044. Petitions filed on October 15, 2024.

Case Subject Matter – Systems and methods for outputting "corrected" gamma reference voltages to drive a Liquid Crystal Display (LCD).

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Dority & Manning LLP (San Diego, CA and Greenville, SC)

Case – *LithiumHub, LLC* v. Bass Pro Outdoor et. al.

Case Numbers – ITC Investigation No. 337-TA-1421. Complaint filed September 12, 2024.

Case Subject Matter – starting a combustion engine using lithium-based battery cells and solid-state switches.

Work Performed – Provided expert consulting services. Wrote declaration for a claim construction brief.

Baker Botts LLP (Austin, TX and Houston, TX)

Case – *Silicon Motion Inc.* v. K.Mizra, LLC

Case Number – IPR2024-01236. Petition filed on September 10, 2024.

Case Number – IPR2024-01240. Petition filed on August 13, 2024.

Case Number – IPR2024-01241. Petition filed on August 9, 2024.

Case Subject Matter – Calibrating a memory controller for use with DDR (double-data rate) DRAM (dynamic random access memory). Calibrating a communication channel to receive a digital signal. A micro-threaded memory device.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Garlick & Markison, LLC (Phoenix, AZ and Austin, TX)

Case – Ex Parte Reexamination

Case Number – 90/019612. Request filed on August 6, 2024.

Case Subject Matter – Semiconductor manufacturing processes, fabrication and packaging of integrated circuits, layout and routing of signal lines.

Work Performed – Provided expert consulting services and wrote declaration**.**

Bookoff McAndrews, PLLC (Washington, DC)

Case – *Lenovo Inc.* v. Intellectual Ventures II LLC

Case – *Lenovo Inc.* v. University of Rochester

Case Numbers – IPR2024-01225 and IPR2024-01226. Petitions filed on August 2, 2024.

Case Subject Matter – Methods for calibrating intra-cycle timing in digital communications. Digital circuits with multiple clock domains.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Wolf, Greenfield & Sacks, P.C. (Washington, D.C., and Boston, MA)

Case – *Infineon Technologies* v. Innoscience Technology

Case Numbers – ITC Investigation No. 337-TA-1414. Complaint filed July 26, 2024.

Case Subject Matter – GaN-on-Si semiconductor devices, GaN field effect transistors (FETs), and packaging power transistors.

Work Performed – Provided expert consulting services.

DLA Piper LLP (Palo Alto, CA and Austin, TX)

Case – *BOE Technology Group Co., Ltd.* v. Optronic Sciences LLC

Case Numbers – IPR2024-01130, IPR2024-01133, and IPR2024-01134. Petitions filed on July 5, 2024

Case Subject Matter – Imaging pixels, layout, and fabrication. Light emitting devices, including packaging, covers, and structures.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Dentons US LLP (Washington, DC)

Case – *Reolink Digital Technology Co., Ltd.* v. KT Imaging US, LLC

Case Numbers – IPR2024-01154 and IPR2024-01155. Petitions filed on July 3, 2024

Case Subject Matter – Image sensor structure and package with integrated lens module for digital image products such as digital cameras, camera phones, video phones, fingerprint readers and so on.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Paul Hastings LLP (Washington, DC)

Case – Ex Parte Reexaminations

Case Numbers – 90/019,560, 90/019,962, and 90/019,964. Requests filed on July 1, 2024

Case Numbers – 90/019,556, 90/019,557, and 90/019,558. Requests filed on June 28, 2024.

Case Subject Matter – Wireless charging systems, power sources, and inductive receivers for charging mobile devices.

Work Performed – Provided expert consulting services and wrote declarations for ex parte reexaminations.

Banner Witcoff (Chicago, IL and Washington, DC)

Case – *ZF Friedrichshafen AG, ZF Active Safety and Electronics US LLC, and Nissan Motor Company, Ltd.* v. Foras Technologies, Ltd.

Case Number – IPR2024-00969. Petition filed on June 24, 2024.

Case Subject Matter – Detecting loss of lockstep between pairs of processors and loss of lockstep recovery

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Fish & Richardson P.C. (San Diego, CA and Boston, MA)

Case – *Vicor Corporation* v. Delta Electronics, Inc.

Case Numbers – IPR2024-00704, IPR2024-00705, IPR2024-00706, and IPR2024-00715. Petitions filed on March 25, 2024.

Case Subject Matter – Power converters including design, packaging, heatsinking and manufacturing. Resonant converters with overcurrent protection.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Pillsbury Winthrop Shaw Pittman LLP (San Francisco, CA)

Case – Redstone Logics LLC v. *MediaTek, Inc.*

Case Number – Texas, WD (Midland/Odessa) 7:24-cv-00029. Complaint filed January 26, 2024.

Case Subject Matter – multi-core processors with voltage and clock scaling functionality and related communications/control signaling.

Work Performed – Provided expert consulting services including writing declaration for claim construction.

Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C. (Boston, MA)

Case – RoadRunner Recycling, Inc. v. *Recycle Tract Systems*

Case Number – California, ND 3:23-cv-04804. Amended complaint filed on January 16, 2024.

Case Subject Matter – Waste and recycling metering technology.

Work Performed – Provided expert consulting services including writing expert report. Was deposed.

Winston & Strawn LLP (Los Angeles, CA and Redwood City, CA)

Case – *Silicon Motion, Inc.* v. Unification Technologies LLC

Case Number – IPR2024-00199. Petition filed on December 18, 2023.

Case Subject Matter – Memory controller, solid-state drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Garlick & Markison, LLC (Austin, TX)

Case – *NXP USA, Inc.* v. Bell Semiconductor, LLC

Case Numbers – IPR2024-00167 and IPR2024-00168. Petitions filed on November 9, 2023.

Case Subject Matter – Semiconductor manufacturing processes, fabrication and packaging of integrated circuits, layout and routing of signal lines.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Unified Patents, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/019288. Request filed on October 20, 2023.

Case Subject Matter – Power conversion device to drive an alternating-current motor for an electric vehicle.

Work Performed – Provided expert consulting services and wrote declaration.

Haynes and Boone, LLP (Dallas, TX)

Case – *Western Digital Technologies, Inc.* v. Longitude Licensing LTD.

Case Number – IPR2023-01200. Petition filed on July 14, 2023.

Case Subject Matter – Communications between a memory controller and memory.

Work Performed – Provided expert consulting services, wrote declaration for inter partes review, and was deposed.

Paul Hastings LLP (Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. Mojo Mobility, Inc.

Case Numbers – IPR2023-01094, IPR2023-01095, IPR2023-01096, IPR2023-01097, IPR2023-01098, IPR2023-01099, IPR2023-01100, and IPR2023-01124. Petitions filed on June 30, 2023.

Case Numbers – IPR2023-01101 and IPR2023-01102. Petitions filed on June 29, 2023.

Case Numbers – IPR2023-01091, IPR2023-01092, and IPR2023-01093. Petitions filed on June 28, 2023.

Case Numbers – IPR2023-01086, IPR2023-01087, IPR2023-01088, IPR2023-01089, and IPR2023-01090. Petitions filed on June 27, 2023.

Case Subject Matter – Wireless charging systems, power sources, and inductive receivers for charging mobile devices.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Winston & Strawn LLP (Los Angeles, CA, Redwood City, CA, Chicago, IL, and Houston, TX)

Case – Unification Technologies LLC v. *Silicon Motion, Inc.*

Case Number – Texas, ED (Marshall) 2:23-cv-00267. Complaint filed June 2, 2023.

Case Subject Matter – Memory controller, solid-state drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services.

Norton Rose Fulbright LLP (Austin, TX and Dallas, TX)

Case – *Current Lighting Solutions, LLC d/b/a GE Current* v. Jiaxing Super Lighting Electric Appliance Co., Ltd.

Case Numbers – IPR2023-00979 and IPR2023-00980. Petitions filed on May 31, 2023.

Case Number – IPR2023-00270. Petition filed on December 19, 2022.

Case Number – IPR2023-00271. Petition filed on December 14, 2022.

Case Subject Matter – LED lighting, lamps, tube lamps, assembly, and associated circuits and electronics.

Work Performed – Provided expert consulting services and wrote declarations for inter partes review.

Faegre Drinker Biddle & Reath LLP (San Francisco, CA, Washington, DC, and Minneapolis, MN)

Case – CogniPower LLC v. *Samsung Electronics*

Case Number – Texas, ED (Marshall) 2:23-cv-00160. Complaint filed April 10, 2023.

Case Subject Matter – Power conversion using switching power supplies.

Work Performed – Provided expert consulting services and wrote expert reports.

Baker Botts LLP (Dallas, TX)

Case – *Lennox Industries Inc.* v. Rosen Technologies LLC

Case Numbers – IPR2023-00715, IPR2023-00716, IPR2023-00717, IPR2023-00718, and IPR2023-00719. Petitions filed on March 29, 2023.

Case Subject Matter – Thermostat system communications, programming, and displays.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Cooley LLP (Palo Alto, CA)

Case – *Nintendo Co., Ltd. and Nintendo of America Inc.* v. Polaris PowerLED Technologies, LLC

Case Number – IPR2023-00778. Petition filed on March 28, 2023.

Case Subject Matter – Visual displays, circuit design, and related technologies.

Work Performed – Provided expert consulting services, wrote declaration for inter partes review, and was deposed.

Bracewell LLP (New York, NY and Seattle, WA)

Case – *Kioxia America, Inc. and Kioxia Corporation* v. BiTMICRO LLC

Case Numbers – IPR2023-00741, IPR2023-00742, and IPR2023-00743. Petitions filed on March 23, 2023.

Case Subject Matter – Solid-state storage devices utilizing multi-profile memory controllers. Optimizing memory operations in a memory system suitable for use in an electronic storage device. Supplying energy to a cache memory using a super capacitor.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Bookoff McAndrews, PLLC (Washington, DC)

Case – *Lenovo Inc. and Motorola Mobility LLC* v. Theta IP, LLC

Case Numbers – IPR2023-00694, IPR2023-00697, and IPR2023-00698. Petitions filed on March 7, 2023.

Case Subject Matter – Power in wireless communication circuits.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Sheppard, Mullin, Richter & Hampton LLP (Menlo Park, CA and San Diego, CA)

Case – Semiconductor Design Technologies LLC v. *Cadence Design Systems, Inc.*

Case Number – California, ND 3:23-cv-01001. Complaint filed March 6, 2023.

Case Subject Matter – Semiconductor design support device/method and manufacturing method for semiconductor integrated circuit.

Work Performed – Provided expert consulting services.

McDermott Will & Emery LLP (Chicago, IL and Austin, TX)

Case – *Xilinx, Inc.* v. Polaris Innovations Limited

Case Numbers – IPR2023-00513 and IPR2023-00514. Petitions filed on February 6, 2023.

Case Subject Matter – Methods for terminating a memory chip with various termination resistances and output drivers for integrated circuits.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed**.**

Willkie Farr & Gallagher LLP (San Franciso, CA)

Case –Bell Semiconductor, LLC. v. *Synopsys, Inc.*

Case Number – California, SD 3:22-cv-00594. Complaint filed on January 31, 2023.

Case Subject Matter – Integrated circuit design computer-aided design (CAD) tools for routing, design rule checking, layout versus schematic, electrical checking, dummy fill, reducing capacitance.

Work Performed – Provided expert consulting services and wrote expert reports.

Fish & Richardson P.C. (Washington, DC, Atlanta, GA, and Boston, MA)

Case – Element Capital Commercial Company PTE. LTD v. *BOE Technology Group Co. LTD and Motorola (Wuhan) Mobility*

Case Number – Texas, ED (Marshall) 2:22-cv-00118. Complaint filed January 11, 2023.

Case Subject Matter – Display technology, layout, circuit design, pixel design and fabrication.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Baker Botts LLP (San Franciso, CA and New York, NY) and O'Melveny & Myers LLP (Los Angeles, CA)

Case – Polaris PowerLED, LLC v. *Samsung Electronics and Samsung Display*

Case Number – Texas, ED (Marshall) 2:22-cv-00469. Complaint filed December 12, 2022.

Case Subject Matter – active matrix organic light-emitting diode (AMOLED) displays, controlling the intensity of light-emitting diodes in backlights of displays, control circuits for adjusting current delivery based upon temperature.

Work Performed – Provided expert consulting services including writing a declaration for claim construction.

Arnold & Porter (Los Angeles and Palo Alto, CA) and Willkie Farr & Gallagher LLP (San Franciso, CA)

Case – *Synopsys, Inc. and Cadence Design Systems, Inc.* v. Bell Semiconductor, LLC.

Case Number – Delaware, 1:22-cv-01512. Complaint filed on November 18, 2022.

Case Subject Matter – Integrated circuit design computer-aided design (CAD) tools for routing, design rule checking, layout versus schematic, electrical checking, dummy fill, reducing capacitance.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Paul Hastings LLP (Washington, DC)

Case – Ex Parte Reexaminations

Case Numbers – 90/015155 and 90/015156. Requests filed on November 7, 2022.

Case Number – 90/015134. Request filed on October 14, 2022.

Case Number – 90/015130. Request filed on September 30, 2022.

Case Subject Matter – Packaging and fabrication of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declaration.

Russ August & Kabat (Los Angeles, CA)

Case – *Resonant Systems, Inc.* v. Sony

Case Number – Texas, ED (Marshall) 2:22-cv-00424. Complaint filed on October 26, 2022.

Case Subject Matter – Linear vibration modules and linear-resonant vibration modules.

Work Performed – Provided expert consulting services, wrote claim construction disclosure, wrote expert reports, and was deposed.

Sheppard, Mullin, Richter & Hampton LLP (Menlo Park, CA and San Diego, CA) and Willkie Farr & Gallagher LLP (San Francisco, CA)

Case – Bell Semiconductor, LLC v. *NXP*, SMC, Micron, Nvidia, *Advanced Micro Devices (AMD)*, *Acer*, Infineon, Qualcomm, Motorola Mobility, and Western Digital

Case Number – ITC Investigation No. 337-TA-1340. Complaint filed October 6, 2022.

Case Subject Matter – Electronic devices, semiconductor devices, and components.

Work Performed – Provided expert consulting services.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Daedalus Prime LLC v. *Samsung Electronics* and Qualcomm Inc.

Case Number – ITC Investigation No. 337-TA-1335. Complaint filed September 12, 2022.

Case Subject Matter – Semiconductor devices, mobile devices, and components.

Work Performed – Provided expert consulting services.

Fish & Richardson P.C. (Boston, MA, Houston, TX, and Washington, DC)

Case – Sonrai Memory LTD. v. *Micron Technology, Inc.*

Case Numbers – Texas, WD (Waco) 6:22-cv-00855 and Texas, WD (Waco) 1:23-cv-01407. Complaint filed August 16, 2022.

Case Subject Matter – Portable RAM drive and variable charge pump circuit with dynamic load.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Russ August & Kabat (Los Angeles, CA and New York, NY)

Case – *NextGen Innovations, LLC* v. Infinera, Fujitsu, AT&T, and Nokia

Case Number – Texas, ED (Marshall) 2:22-cv-00306, Texas, ED (Marshall) 2:22-cv-00307, Texas, ED (Marshall) 2:22-cv-00308, and Texas, ED (Marshall) 2:22-cv-00309. Complaints filed on August 9, 2022.

Case Subject Matter – optical transmission systems including optical components for encoding, transmission (fiber optic transmitters and receivers), and decoding of data and related standards and concepts.

Work Performed – Provided expert consulting services, wrote claim construction disclosure, wrote expert reports, and was deposed twice.

DLA Piper (Chicago, IL and Washington, DC)

Case – Ampt, LLC v. *SolarEdge Technologies, Inc.*

Case Number – ITC Investigation No. 337-TA-1327. Complaint filed July 28, 2022.

Case Subject Matter – Solar power optimizers, inverters, and components.

Work Performed – Provided expert consulting services including writing declarations for claim construction, expert reports, and was deposed.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, and Irvine, CA)

Case – Signify North America Corporation v. *Shenzhen Intellirocks Tech Co.*

Case Number – Texas, WD (Waco) 6:22-cv-00760. Complaint filed on July 8, 2022.

Case Subject Matter – LED packaging, circuits, and systems.

Work Performed – Provided expert consulting services including writing declaration for claim construction. Was deposed.

Baker Botts LLP (Dallas, TX)

Case – Rosen Technologies LLC v. *Lennox Industries Inc.*

Case Number – Texas, ND (Dallas) 3:22-cv-00732. Complaint filed on June 7, 2022.

Case Subject Matter – Thermostat system communications, programming, and displays.

Work Performed – Provided expert consulting services.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. Scramoge Technology Ltd.

Case Numbers – IPR2022-01052, IPR2022-01053, and IPR2022-01058. Petitions filed on May 26, 2022.

Case Numbers – IPR2022-01054, IPR2022-01055, IPR2022-01056, and IPR2022-01057. Petitions filed on May 24, 2022.

Case Number – IPR2022-00939. Petition filed on April 29, 2022.

Case Subject Matter – An antenna that supports wireless charging using switching power supplies such as flyback converters.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Ex Parte Reexaminations
Case Number – 90/015020. Request filed on May 2, 2022.
Case Number – 90/014906. Request filed on November 12, 2021.
Case Number – 90/014899. Request filed on November 10, 2021.
Case Number – 90/014888. Request filed on October 21, 2021.
Case Numbers – 90/014886 and 90/014887. Requests filed on October 20, 2021.
Case Number – 90/014885. Request filed on October 19, 2021.
Case Subject Matter – Universal Serial Bus (USB) for charging.
Work Performed – Provided expert consulting services and wrote declarations**.**

DLA Piper (Chicago, IL, Austin, TX, and Washington, DC)

Case – *SolarEdge Technologies, Inc.* v. Fronius International GMBH
Case Number – IPR2022-00849. Petition filed on April 14, 2022.
Case Subject Matter – Mechanical assembly and enclosure whereby an upper housing part is detached from a lower housing part using a "rotate-and-lift" feature.
Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Kirkland & Ellis LLP (New York, NY)

Case – *Samsung Electronics Co.* v. Sonrai Memory Ltd.
Case Numbers – IPR2022-00305 and IPR2022-00306. Petitions filed on December 10, 2021.
Case Subject Matter – USB devices and circuits for saving power.
Work Performed – Provided expert consulting services including writing declarations for inter partes reviews.

Haynes and Boone, LLP (Washington, DC)

Case – *Unified Patents, LLC* v. Arigna Technology Limited
Case Number – IPR2022-00285. Petition filed on December 9, 2021.
Case Subject Matter – High voltage driver circuit for driving power devices such as insulated gate bipolar transistors (IGBTs).
Work Performed – Provided expert consulting services, wrote declaration for inter partes review and was deposed.

Paul Hastings LLP (Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. Lynk Labs, Inc.
Case Numbers – IPR2022-00149 and IPR2022-00150. Petitions filed on November 12, 2021
Case Numbers – IPR2022-00100 and IPR2022-00101. Petitions filed on October 28, 2021.
Case Numbers – IPR2022-00051, IPR2022-00052, and IPR2022-00098. Petitions filed on October 27, 2021.
Case Numbers – IPR2021-01575 and IPR2021-01576. Petitions filed on October 1, 2021.
Case Numbers – IPR2021-01299, IPR2021-01300, IPR2021-01345, IPR2021-01346, and IPR2021-01347. Petitions filed on September 7, 2021.
Case Subject Matter – Circuit design, including switching power supply design (e.g., flyback), rectifiers, power factor correction, etc. for lighting and displays using light emitting diodes (LEDs).
Work Performed – Provided expert consulting services, wrote declarations, and was deposed ten times.

Haynes and Boone, LLP (Plano, TX)

Case – *Pure Storage, Inc.* v. Digital Cache, LLC
Case Number – IPR2022-00121. Petition filed on October 29, 2021.
Case Subject Matter – Non-volatile memory (NVM) devices capable of retaining stored data in case of a power failure.
Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Banner Witcoff (Washington, DC)

Case – *SolarEdge Technologies Ltd.* v. Koolbridge Solar, Inc.

Case Numbers – IPR2022-00007, IPR2022-00008, IPR2022-00009, IPR2022-00010, IPR2022-00011, and IPR2022-00012. Petitions filed on October 11, 2021.

Case Numbers – IPR2022-00013, IPR2022-00014, and IPR2022-00015. Petitions filed on October 8, 2021.

Case Subject Matter – DC-to-AC converters using full-bridges, multi-level conversion for power systems, and other electronics for harvesting solar energy.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. LED Wafer Solutions LLC

Case Number – IPR2021-01554. Petition filed on September 20, 2021.

Case Number – IPR2021-01526. Petition filed on September 10, 2021.

Case Number – IPR2021-01506. Petition filed on September 7, 2021.

Case Number – IPR2021-01491. Petition filed on September 3, 2021.

Case Subject Matter – Packaging of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declarations.

Paul Hastings, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/014,846. Request filed on August 30, 2021.

Case Subject Matter – Wireless power transmission and ways to wirelessly charge and/or discharge a battery.

Work Performed – Provided expert consulting services and wrote declaration.

Jones Day (San Diego, CA and Pittsburgh, PA)

Case – *SOLiD, Inc.* v. CommScope Technologies LLC

Case Numbers – IPR2021-01390, IPR2021-01391, IPR2021-01392, IPR2021-01393, and IPR2021-01394. Petitions filed on August 12, 2021.

Case Subject Matter – Digital antenna system that enables extension of radio frequency (RF) analog signals from base stations to areas (e.g., inside of buildings) where access to such signals is inhibited.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declaration.

Unified Patents, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/019,015. Request filed on July 20, 2021.

Case Subject Matter – Voltage-controlled oscillator (VCO) temperature compensation.

Work Performed – Provided expert consulting services and wrote declaration.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – *Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC* v. Unification Technologies LLC

Case Numbers – IPR2021-00940, IPR2021-00941, and IPR2021-00942. Petitions filed on June 4, 2021.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declarations.

Hill, Kertscher & Wharton, LLP (Atlanta, GA)

Case – Kaijet Technology v. *Sanho Corporation*

Case Number – IPR2021-00886. Petition filed on April 30, 2021.

Case Subject Matter – Port extension apparatus for headphone jack, USB (Universal Serial Bus or Type-C ports), and video ports such as VGA (Video Graphics Array), DVI (Digital Visual Interface), HDMI (High-Definition Multimedia Interface), DP (Display Port), and mini-DP.

Work Performed – Provided expert consulting services for inter partes review, wrote declaration, was deposed.

O'Melveny & Myers LLP (Los Angeles, CA and New York, NY)

Case – Solas OLED LTD. v. *Samsung Electronics Co. LTD.*

Case Number – Texas, ED (Marshall) 2:21-cv-00105. Complaint filed March 22, 2021.

Case Subject Matter – Touch-sensors for gesture recognition and signal processing for capacitive touch displays.

Work Performed – Provided expert consulting services including writing declaration for claim construction.

O'Melveny & Myers LLP (San Francisco, CA)

Case – Super Interconnect Technologies LLC v. *Google LLC*

Case Number – Texas, ED (Marshall) 2:18-cv-00463 (complaint filed November 2, 2018) and Texas, WD (Waco) 6:21-cv-00259 (complaint filed March 15, 2021).

Case Subject Matter – Transmission of data and clock signals. Serial signals such as transition minimized differential signaling. Communications between processors and non-volatile storage such as Universal Flash Storage (UFS) and embedded MultiMedia Controller (eMMC).

Work Performed – Provided expert consulting services and wrote expert reports.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, and Irvine, CA)

Case – Fundamental Innovation Systems International LLC v. *Anker Innovations and Fantasia Trading LLC d/b/a Ankerdirect*

Case Number – Delaware, 1:21-cv-00339. Complaint filed on March 5, 2021.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – *TCT Mobile Inc. and TCL Communication, Inc.* v. Fundamental Innovation Systems International LLC

Case Numbers – IPR2021-00597, IPR2021-00598, and IPR2021-00599. Petitions filed on February 26, 2021.

Case Number – IPR2021-00428. Petition filed on January 13, 2021.

Case Number – IPR2021-00410. Petition filed on January 11, 2021.

Case Number – IPR2021-00395. Petition filed on December 31, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declarations for inter partes reviews. Was deposed twice.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – *Samsung, Inc.* v. Pictos Technologies, Inc.

Case Number – IPR2021-00557. Petition filed on February 18, 2021.

Case Number – IPR2021-00436. Petition filed on January 19, 2021.

Case Numbers – IPR2021-00437 and IPR2021-00438. Petitions filed on January 15, 2021.

Case Subject Matter – Solid-state imaging devices including red, green, and blue pixels, data conversion circuits, and interpolation circuits. CMOS imagers including fabrication and design, active pixels, and semiconductor physics.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

O'Melveny & Myers LLP (San Francisco, CA) and DLA Piper (New York, NY)

Case – Solas OLED Ltd. v. *BOE Technology Group Co. Ltd. and Samsung Electronics*

Case Number – ITC Investigation No. 337-TA-1243. Complaint filed January 5, 2021.

Case Subject Matter – Active matrix OLED display devices and components

Work Performed – Provided expert consulting services, wrote expert reports, was deposed, and testified at trial.

Paul Hastings LLP (Washington, DC)

Case – *Samsung, Inc.* v. Garrity Power Services LLC

Case Number – IPR2021-00389. Petition filed on December 31, 2020.

Case Subject Matter – Power electronics including full-bridge PWM modules for wireless power transmission using magnetic coupling via antennas and transformers. Design of inductors and coils.

Work Performed – Provided expert consulting services and wrote declaration for inter partes reviews.