UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE Technology Group Co., Ltd.
Petitioner

v.

Optronic Sciences LLC
Patent Owner

Inter Partes Review No.: IPR2025-00239

PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 8,502,757 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. §§ 42.1-100, ET SEQ

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CHART OF CLAIMS
[1pre] An organic light emitting display, comprising:
[1a] a data line for transmitting a data signal;
[1b] a first scan line for transmitting a first scan signal;
[1c] a second scan line for transmitting a second scan signal;
[1d] a transmission line for transmitting an emission signal;
[1e] an input unit, electrically connected to the data line and the first scan line, for outputting a preliminary control voltage according to the data signal and the first scan signal;
[1f] a voltage adjustment unit, electrically connected to the transmission line and the input unit, for adjusting the preliminary control voltage according to the emission signal and a second reference voltage;
[1g] a couple unit, electrically connected to the input unit and the voltage adjustment unit, for adjusting a control voltage through coupling a change of the preliminary control voltage;
[1h] a driving unit, electrically connected to the couple unit, for providing a driving current and a driving voltage according to the control voltage and a first power voltage;
[1i] a first reset unit, electrically connected to the driving unit and the second scan line, for resetting the driving voltage according to the second scan signal and a first reference voltage;
[1j] a second reset unit, electrically connected to the driving unit, the first reset unit and the first scan line, for resetting the control voltage according to the first scan signal and the driving voltage;
[1k] an organic light emitting diode for generating output light according to the driving current; and
[1l] an emission enable unit, electrically connected to the transmission line, the driving unit and the organic light emitting diode, for providing a control of furnishing the driving current to the organic light emitting diode according to the emission signal.
[2] The organic light emitting display of claim 1, wherein the input unit comprises a first transistor, the first transistor having a first end electrically connected to the data line, a gate end electrically connected to the first scan line, and a second end electrically connected to the voltage adjustment unit and the couple unit.
[3] The organic light emitting display of claim 2, wherein the first transistor comprises a thin film transistor or a field effect transistor.

CHART OF CLAIMS
[4] The organic light emitting display of claim 1, wherein the driving unit comprises a second transistor, the second transistor having a first end for receiving the first power voltage, a gate end for receiving the control voltage, and a second end for outputting the driving current and the driving voltage.
[5] The organic light emitting display of claim 4, wherein the second transistor comprises a thin film transistor or a field effect transistor.
[6] The organic light emitting display of claim 1, wherein the couple unit comprises a capacitor electrically connected between the input unit and the driving unit.
[7] The organic light emitting display of claim 1, wherein the first reset unit comprises a third transistor, the third transistor having a first end for receiving the first reference voltage, a gate end electrically connected to the second scan line, and a second end electrically connected to the driving unit, the second reset unit and the emission enable unit.
[8] The organic light emitting display of claim 7, wherein the third transistor comprises a thin film transistor or a field effect transistor.
[9] The organic light emitting display of claim 1, wherein the second reset unit comprises a fourth transistor, the fourth transistor having a first end electrically connected to the driving unit, the first reset unit and the emission enable unit, a gate end electrically connected to the first scan line, and a second end electrically connected to the couple unit and the driving unit.
[10] The organic light emitting display of claim 9, wherein the fourth transistor comprises a thin film transistor or a field effect transistor.
[11] The organic light emitting display of claim 1, wherein the voltage adjustment unit comprises a fifth transistor, the fifth transistor having a first end for receiving the second reference voltage, a gate end electrically connected to the transmission line, and a second end electrically connected to the input unit and the couple unit.
[12] The organic light emitting display of claim 11, wherein the fifth transistor comprises a thin film transistor or a field effect transistor.
[13] The organic light emitting display of claim 11, wherein the second reference voltage is the first power voltage.
[14] The organic light emitting display of claim 1, wherein the emission enable unit comprises a sixth transistor, the sixth transistor having a first end electrically connected to the driving unit, the first reset unit and the second reset unit, a gate end electrically connected to the transmission line, and a second end electrically connected to the organic light emitting diode.

CHART OF CLAIMS
[15] The organic light emitting display of claim 14, wherein the sixth transistor comprises a thin film transistor or a field effect transistor.
[16] The organic light emitting display of claim 1, wherein the organic light emitting diode comprises an anode electrically connected to the emission enable unit and a cathode for receiving a second power voltage.
[17pre] A driving method, comprising:
[17a] outputting a preliminary control voltage by an input unit according to a data signal and a first scan signal;
[17b] adjusting the preliminary control voltage by a voltage adjustment unit according to an emission signal and a second reference voltage;
[17c] adjusting a control voltage by a couple unit through coupling a change of the preliminary control voltage;
[17d] providing a driving current and a driving voltage by a driving unit according to the control voltage and a power voltage;
[17e] resetting the driving voltage by a first reset unit according to a second scan signal and a first reference voltage;
[17f] resetting the control voltage by a second reset unit according to the first scan signal and the driving voltage;
[17g] generating output light by an organic light emitting diode according to the driving current;
[17h] providing a control of furnishing the driving current to the organic light emitting diode by an emission enable unit according to the emission signal;
[17i] providing the first scan signal with a first level to the input unit and the second reset unit, providing the second scan signal with the first level to the first reset unit, providing the emission signal with a second level different from the first level for disabling a voltage adjusting operation of the voltage adjustment unit and disabling a current furnishing operation of the emission enable unit, and providing the data signal to the input unit during a first interval;
[17j] outputting the preliminary control voltage by the input unit according to the data signal and the first scan signal during the first interval;
[17k] resetting the driving voltage by the first reset unit according to the second scan signal and the first reference voltage during the first interval;
[17l] resetting the control voltage by the second reset unit according to the first scan signal and the driving voltage during the first interval;
[17m] switching the second scan signal from the first level to the second level for disabling a resetting operation of the first reset unit during a second interval following the first interval;

CHART OF CLAIMS
[17n] performing a threshold voltage compensation operation on the control voltage by the second reset unit and the driving unit according to the first scan signal and the power voltage during the second interval;
[17o] switching the first scan signal from the first level to the second level for disabling a resetting operation of the second reset unit and disabling an inputting operation of the input unit during a third interval following the second interval;
[17p] switching the emission signal from the second level to the first level during a fourth interval following the third interval;
[17q] adjusting the preliminary control voltage by the voltage adjustment unit according to the emission signal and the second reference voltage during the fourth interval;
[17r] adjusting the control voltage by the couple unit through coupling a change of the preliminary control voltage during the fourth interval;
[17s] providing the driving current by the driving unit according to the control voltage and the power voltage during the fourth interval;
[17t] furnishing the driving current to the organic light emitting diode by the emission enable unit according to the emission signal during the fourth interval; and
[17u] generating output light by the organic light emitting diode according to the driving current during the fourth interval.
[18] The driving method of claim 17, wherein the second level is greater than the first level.
[19] The driving method of claim 17, wherein the first level is greater than the second level.
[20] The driving method of claim 17, wherein the second reference voltage is the power voltage.
[21] The driving method of claim 17, wherein a length of the second interval is greater than a length of the first interval.

I. INTRODUCTION

BOE Technology Group Co. LTD. ("Petitioner") requests inter partes review of claims 1-21 ("Challenged Claims") of U.S. Patent No. 8,502,757 ("757 patent," EX1001), owned by Optronic Sciences LLC ("PO").

This petition relies upon the declaration of Dr. R. Jacob Baker (EX1002) and copies large portions of that declaration herein.

Petitioner certifies that the 757 patent is available for *inter partes* review.

II. STATEMENT OF PRECISE RELIEF REQUESTED

In accordance with 35 U.S.C. § 311, Petitioner requests cancelation of claims 1-21 of the 757 patent in view of the following grounds:

Ground	Claims	Stat. Basis	Prior Art
1	1-12, 14-19	35 U.S.C. § 102	Kim406
2	1-20	35 U.S.C. § 103	Kim406 in view of Kim730
3	1-21	35 U.S.C. § 102	Senda
4	1-21	35 U.S.C. § 103	Senda

III. THE 757 PATENT

A. Overview of the 757 Patent

The 757 patent was filed on November 15, 2011, and issued on August 6, 2013. EX1001; EX1002, ¶45.

The 757 patent purports to improve on a prior art pixel driving circuit (Figure 1) by adding reset and threshold voltage compensation mechanisms to

avoid image retention and pixel brightness distortion. EX1001, 7:4-9; EX1002, ¶46.

The 757 patent discloses a pixel driving circuit with two embodiments—Figures 2 and 4. In the embodiment in Figure 2, the voltage adjustment unit uses Vdd as the second reference voltage. *See* Fig. 2 (unit 220 is transistor 221 with electrode connected to Vdd). In the embodiment in Figure 4, the voltage adjustment unit uses Vref2. *See* Fig. 4 (unit 320 is transistor 321 with electrode connected to Vref2). The embodiments are otherwise identical and the timing of the circuit is provided in Figure 3 and accompanying text. EX1002, ¶47.

B. Overview of the 757 patent's File History

The claims of the 757 patent were allowed on the first office action (with amendments to claim 17 under *Ex Parte Quayle*). EX1003, 80-92 (April 25, 2013 Office Action). The Examiner found none of the prior art of record disclosed the voltage adjustment unit and first reset unit in combination with the other limitations of the claims. *Id.* The prior art asserted herein discloses those limitations as shown below. EX1002, ¶48.

C. Person of Ordinary Skill in the Art

A person of ordinary skill in the art ("POSITA") at the time of the alleged invention of the 757 patent (November 15, 2011), and for that matter, at all subsequent times through the present, would have had a Bachelors' degree in

electrical engineering or a comparable field of study, plus approximately one or more years of professional experience with electronic and optoelectronic system design. Additional graduate education could substitute for professional experience, and significant experience in the field could substitute for formal education. EX1002, ¶49.

D. Claim Construction Under 37 C.F.R. § 42.104(b)(3)

Any claim terms not listed below should be construed according to their plain and ordinary meaning to a POSITA at the time of the 757 patent. EX1002, ¶50.

1. Means-Plus-Function Limitations

Claim 1 recites several limitations as "… unit … for" performing a claimed function. The lack of the word "means" raises the presumption that these terms are not subject to Section 112f, but that presumption is rebutted because none of the terms recite sufficient structure for performing the claimed function. EX1002, ¶51.

Each term follows the same format: a functional qualifier, the nonce word "unit," an appositive reciting connections, and "for" followed by a function. The "voltage adjustment unit" in limitation [1f] is reproduced below as an example.

> a voltage adjustment unit, electrically connected to the transmission line and the input unit, for adjusting the preliminary control voltage according to the emission signal and a second reference voltage

EX1001, [1f]. EX1002, ¶52.

In each limitation, the initial functional qualifier is merely a shorthand paraphrasing of the function and does not impart structure to a POSITA. The word "unit" does not recite structure because it is merely a nonce word for any circuitry that would perform the function. The claimed connections add some limitations as to how the structure is connected but is not sufficient structure for performing the claimed function. The "for" clause then recites the function without any structure for performing the function. Thus, each limitation would not be recognized by one of ordinary skill in the art as reciting sufficiently definite structure for performing the claimed function. EX1002, ¶53.

This Petition applies the prior art under both the ordinary meaning of the claim and under the correct means-plus-function constructions. The prior art invalidates the claims under each construction. EX1002, ¶54.

Each limitation subject to 112f is presented below with its function underlined (the functions are entitled to their ordinary meaning and do not require further construction) followed by the corresponding structure disclosed and linked in the specification for performing the claimed function. EX1002, ¶55.

a. [1e] "an input unit…"

"An input unit, electrically connected to the data line and the first scan line, for outputting a preliminary control voltage according to the data signal and the

first scan signal" has the corresponding structure: transistor 216 connected as disclosed in Figures 2, 4 and 4:34-38.

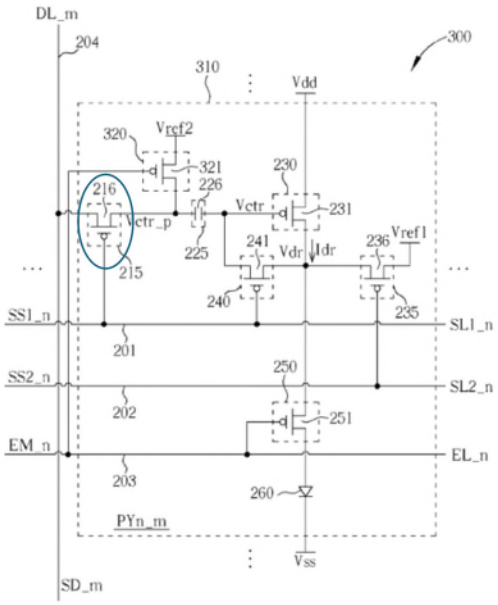


FIG. 4

This structure is linked to this function. EX1001, Fig. 3, 3:54-57, 5:13-15. EX1002, ¶¶56-57.

b. [1f] "a voltage adjustment unit…"

"A voltage adjustment unit, electrically connected to the transmission line and the input unit, for adjusting the preliminary control voltage according to the emission signal and a second reference voltage" has the corresponding structure:

a) transistor 221 connected as disclosed in Figure 2 and 4:34-38 (to Vdd), or

b) transistor 321 connected as disclosed in Figure 4 and 6:36-42 (to Vref2).

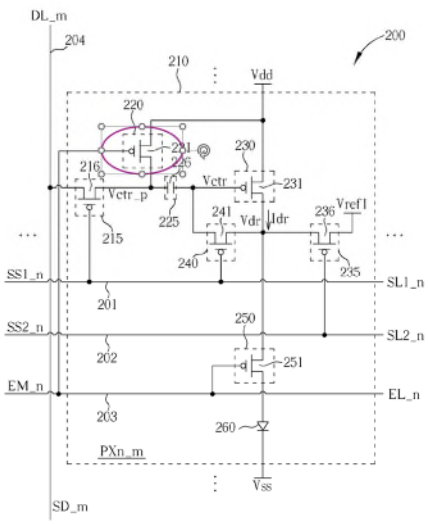


FIG. 2

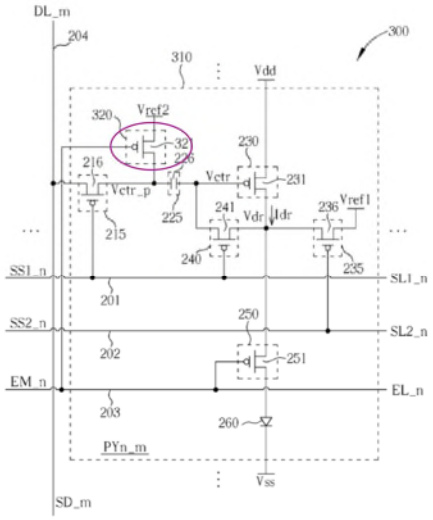


FIG. 4

Each of these structures is linked to this function. EX1001, Fig. 3, 3:58-61 (221), 5:45-55 (Vdd), 6:31-63 (321), 6:43-51 (Vref2). EX1002, ¶¶58-59.

c. [1g] "a couple unit…"

"A couple unit, electrically connected to the input unit and the voltage adjustment unit, for adjusting a control voltage through coupling a change of the preliminary control voltage" has the corresponding structure: capacitor 226 connected as disclosed in Figures 2 and 4 and 4:42-44.

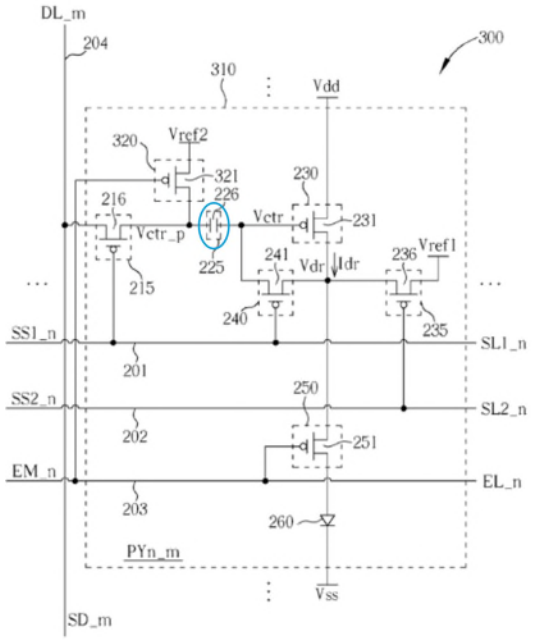


FIG. 4

This structure is linked to this function. EX1001, Fig. 3, 3:62-65, 5:50-55, 6:46-51. EX1002, ¶¶60-61.

d. [1h] "a driving unit…"

"A driving unit, electrically connected to the couple unit, for providing a driving current and a driving voltage according to the control voltage and a first power voltage" has the corresponding structure: transistor 231 connected as disclosed in Figures 2, 4 and 4:38-41.

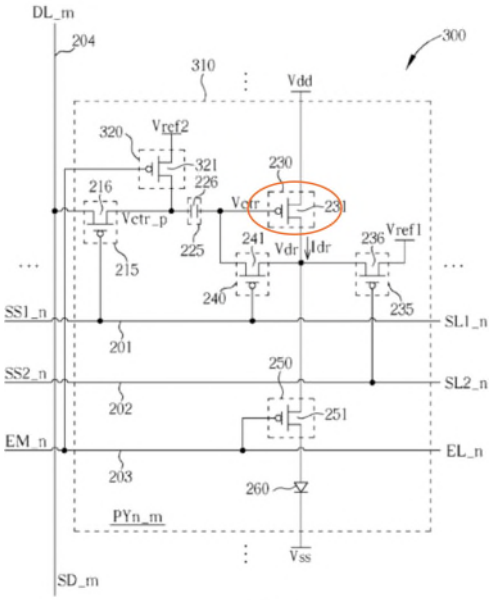


FIG. 4

This structure is linked to this function. EX1001, 3:65-4:2, 5:56-60, 6:53-64. EX1002, ¶¶62-63.

e. [1i] "a first reset unit…"

"A first reset unit, electrically connected to the driving unit and the second scan line, for resetting the driving voltage according to the second scan signal and a first reference voltage" has the corresponding structure: transistor 236 connected as disclosed in Figures 2, 4 and 4:44-48.

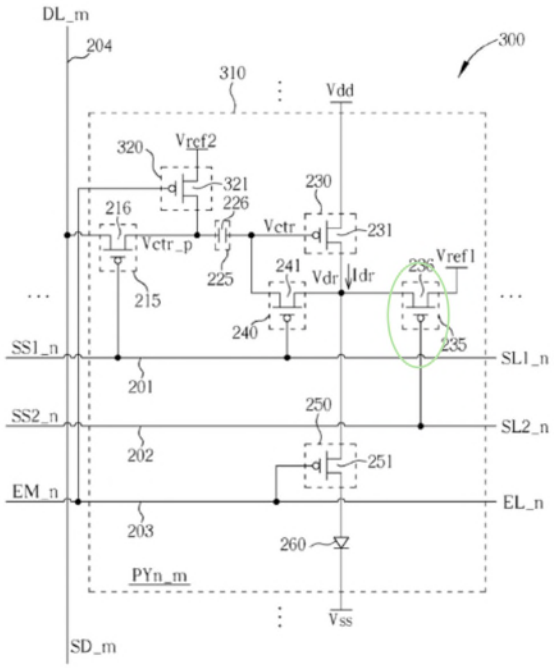


FIG. 4

This structure is linked to this function. EX1001, 4:2-5. EX1002, ¶¶64-65.

f. [1j] "a second reset unit…"

"A second reset unit, electrically connected to the driving unit, the first reset unit and the first scan line, for resetting the control voltage according to the first scan signal and the driving voltage" has the corresponding structure: transistor 241 connected as disclosed in Figures 2, 4 and 4:48-52.

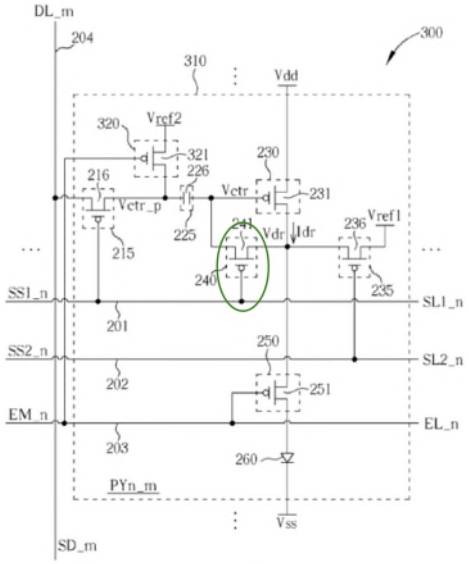


FIG. 4

This structure is linked to this function. EX1001, 4:5-9. EX1002, ¶¶66-67.

g. [1l] "an emission enable unit…"

"An emission enable unit, electrically connected to the transmission line, the driving unit and the organic light emitting diode, for providing a control of furnishing the driving current to the organic light emitting diode according to the emission signal" has the corresponding structure: transistor 221 connected as disclosed in Figures 2, 4 and 4:54-58.

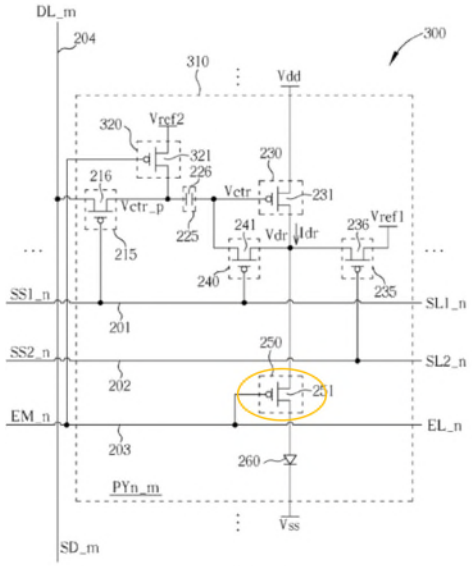


FIG. 4

This structure is linked to this function. EX1001, 4:9-14; EX1002, ¶¶68-69.

h. Abridged Claim Listing Summary

An abridged claim listing summarizing the 112f terms is reproduced below next to the corresponding structure as shown in Figure 4 (the alternative structure of 220/221 for the voltage adjustment unit in Figure 2 is not shown). EX1002, ¶70.

[1pre] An organic light emitting display, comprising:
[1a] a data line [DL_m];
[1b] a first scan line [SS1_n];
[1c] a second scan line [SS2_n];
[1d] a transmission line [EM_n];
[1e] an input unit [215/216]
[1f] a voltage adjustment unit [320/321]
[1g] a couple unit [225/226]
[1h] a driving unit [230/231]
[1i] a first reset unit [235/236]
[1j] a second reset unit [240/241]
[1k] an organic light emitting diode [260]
[1l] an emission enable unit [250/251]

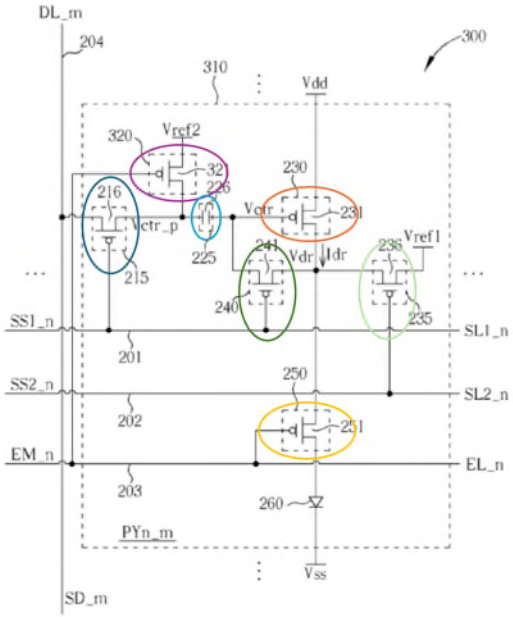


FIG. 4

2. "first/second reference voltage"

a. Primary Construction

The claims encompass first and second reference voltages that are the same or different from each other. The claims use "first" and "second" as labels to refer to two reference voltages in the independent claims. The claims themselves make clear that differently labelled voltages in the independent claims can be the same voltage. For example, claim 1 recites a "second reference voltage" and a "first power voltage" and then dependent claim 13 recites "wherein the second reference voltage is the first power voltage." EX1001, claims 1, 13. There is no definition or disclaimer in the specification or file history that would require limiting the "first" and "second" reference voltages to only the same voltage or to only different voltages. The disclosed embodiments do not explicitly state, or implicitly require, that the reference voltages be different from each other, so it is not possible to read such a limitation in from the specification (which would be legally improper, even if it were possible). Finally, the ordinary meaning of "first" and "second" reference voltages encompasses reference voltages that are the same or different. *See. e.g.*, EX1007 (Fig. 29.30); EX1008, [0039] (VREF1 and VREF2 may be the same or different voltage values). Thus, the claims encompass "first" and "second" reference voltages that are the same or different. EX1002, ¶71 (explaining specification further).

b. Alternative Construction

Under an alternative construction, the "first" and "second" voltages are limited to different voltages. EX1002, ¶72.

IV. OVERVIEW OF THE PRIOR ART REFERENCES

A. EX1004 – Kim406

U.S. Pat. App. Pub. 2007/0103406 to Kim406 was published on May 10, 2007 and is prior art under pre-AIA Section 102(b). EX1002, ¶73.

B. EX1005 – Kim730

U.S. Pat. App. Pub. 2005/0110730 to Kim730 was published on May 26, 2005 and is prior art under pre-AIA Section 102(b). EX1002, ¶74.

C. EX1006 – Senda

U.S. Pat. App. Pub. 2009/0040150 to Senda was published on February 12, 2000 and is prior art under pre-AIA Section 102(b). EX1002, ¶75.

D. Analogous Art

Each of the references is analogous art to the 757 patent because each relates to an OLED display with threshold voltage compensation and driving method. EX1002, ¶76.

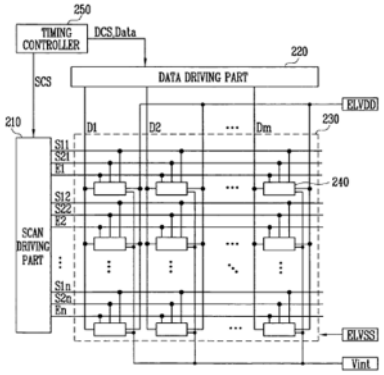
V. GROUND 1: CLAIMS 1-12 AND 14-19 ARE ANTICIPATED BY KIM406

A. Claim 1

1. [1pre]

Kim406 discloses "An organic light emitting display, comprising (see following limitations)." EX1002, ¶77.

FIG. 5



EX1004, Title, Figs. 5-7, [0003], [0045] ("organic light emitting display device"), [0046]-[0072], claims 1-20; EX1002, ¶78.

2. [1a]

Kim406 discloses "a data line (Dm) for transmitting a data signal (data signal)." EX1002, ¶79.

FIG. 5

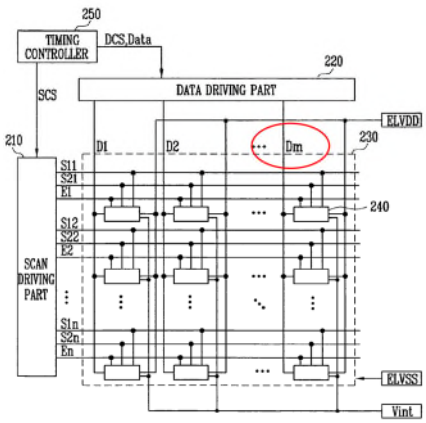
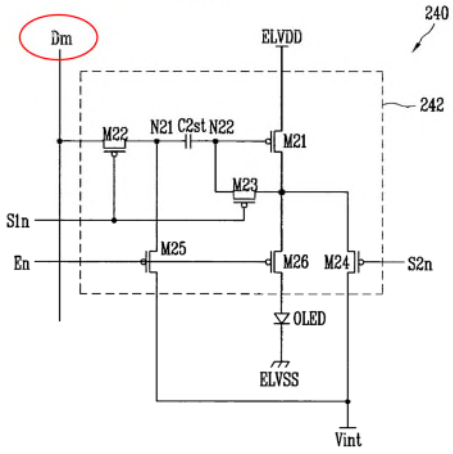


FIG. 6



EX1004, Figs. 5 (Data Driving Part 220 and lines D1 to Dm), Fig. 6 (line Dm), [0049] (Data Driving Part 220 sends data signals on data lines Dm), [0054] (pixel receives data signals from data lines Dm), [0064] (data signal supplied on Dm). EX1002, ¶80.

3. [1b]

Kim406 discloses "a first scan line (S1n) for transmitting a first scan signal (first scan signal)." EX1002, ¶81.

FIG. 5

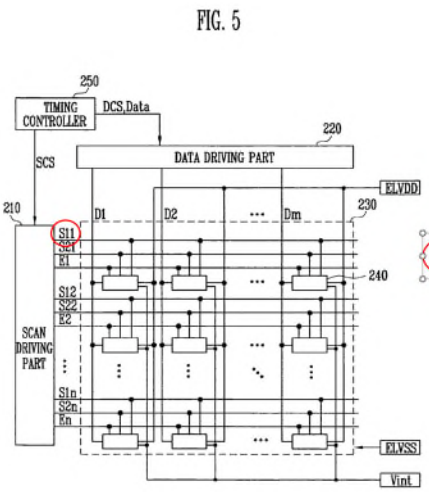
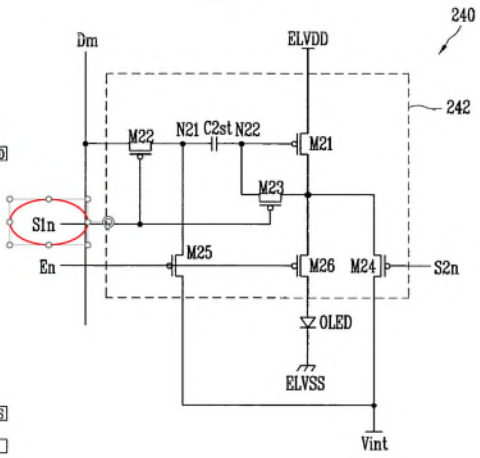


FIG. 6



EX1004, Figs. 5 (Scan Driving Part 210), Fig. 6 (S1n), Fig. 7 (S1n), [0048] (scan driving part 210 transmits first scan signal on S1n), [0054] (pixel receives first scan signal on S1n), [0062]-[0064] (first scan signal supplied on S1n). EX1002, ¶82.

4. [1c]

Kim406 discloses "a second scan line (S2n) for transmitting a second scan signal (second scan signal)." EX1002, ¶83.

FIG. 5

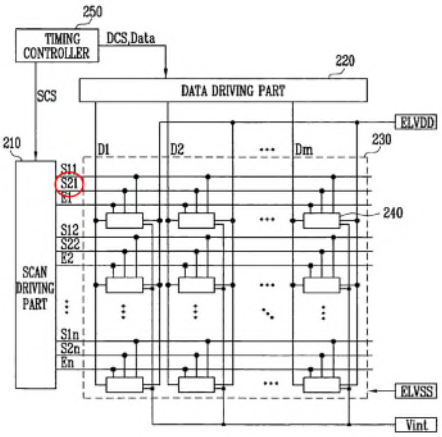
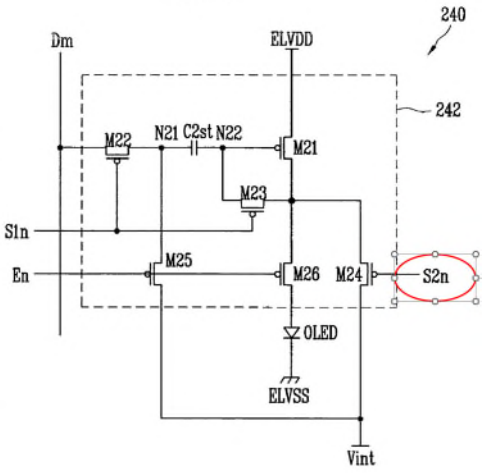


FIG. 6



EX1004, Fig. 5 (Scan Driving Part 210), Fig. 6 (S2n), Fig. 7 (S2n), [0048] (scan driving part 210 transmits second scan signal on S2n), [0054] (pixel receives second scan signal on S2n), [0062]-[0064] (second scan signal supplied on S2n). EX1002, ¶84.

5. [1d]

Kim406 discloses "a transmission line (En) for transmitting an emission signal (emission control signal)." EX1002, ¶85.

FIG. 5

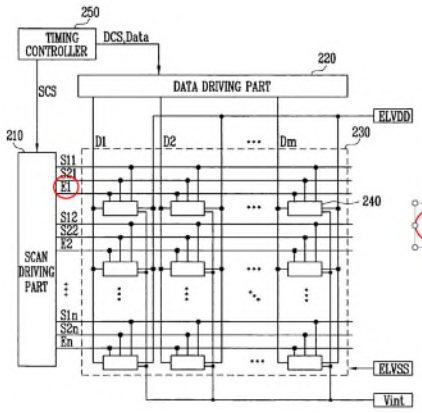
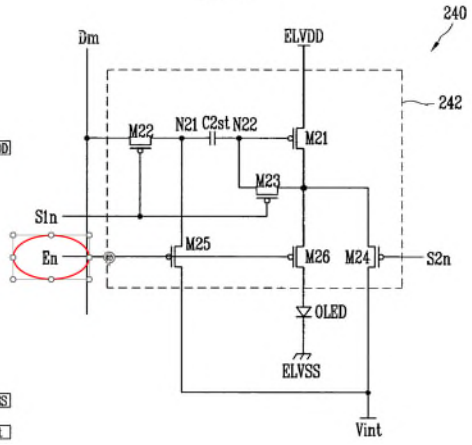


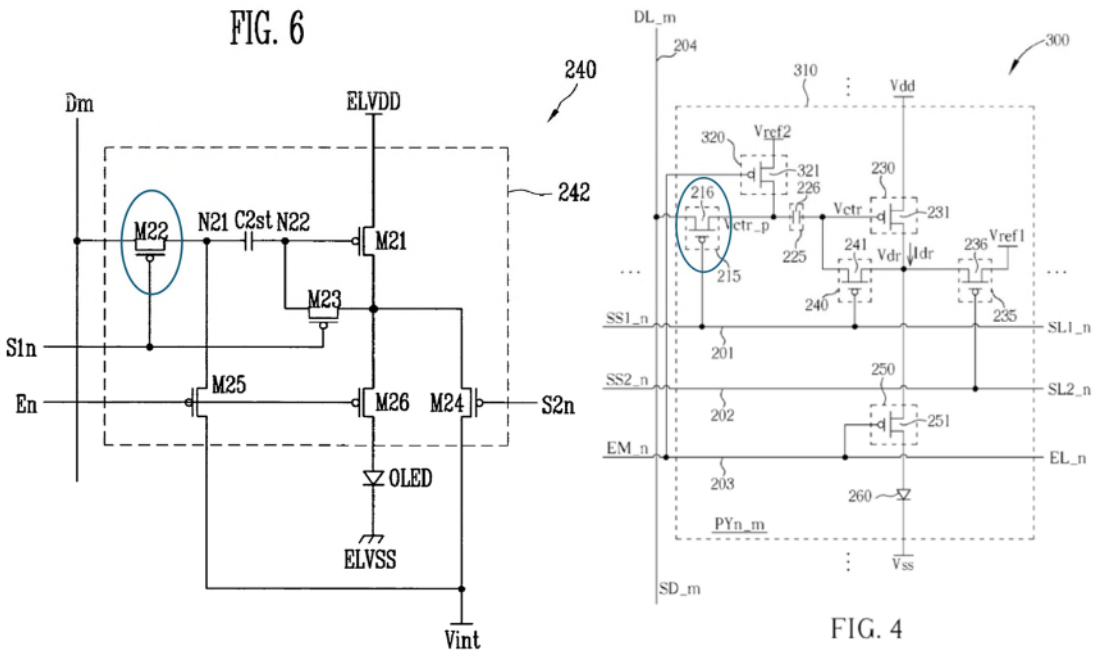
FIG. 6



EX1004, Fig. 5 (Scan Driving Part 210), Fig. 6 (En), Fig. 7 (En), [0048] (scan driving part 210 transmits emission control signal on En), [0062]-[0063], [0067] (emission control signal). EX1002, ¶86.

6. [1e]

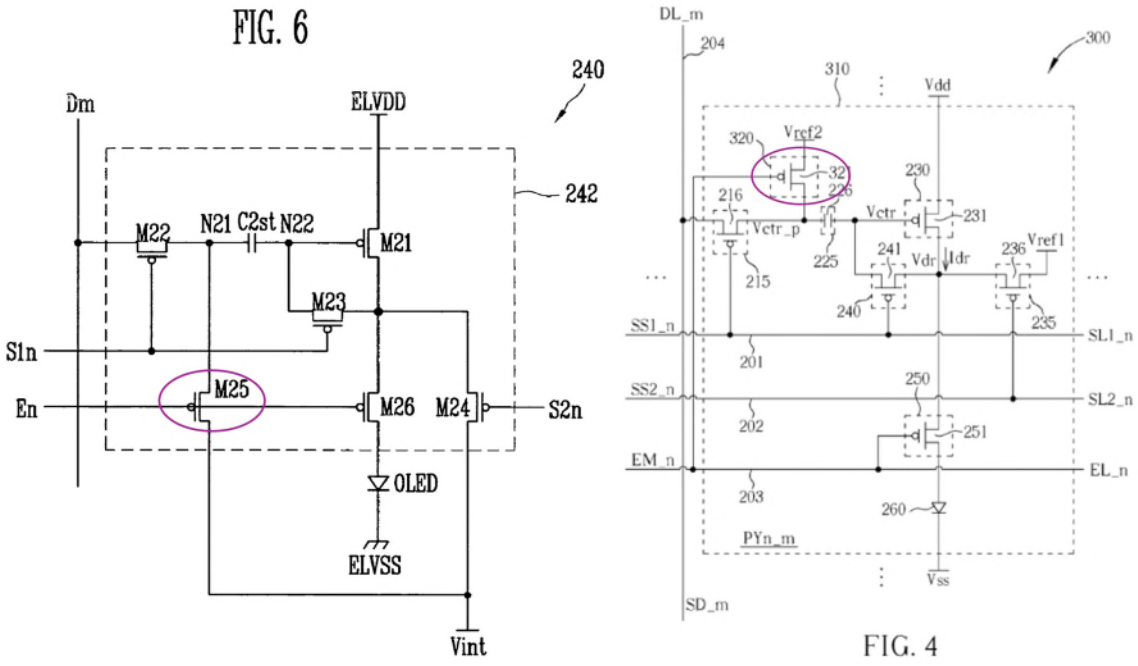
Kim406 discloses "an input unit (M22), electrically connected to the data line (Dm) and the first scan line (S1n), for outputting a preliminary control voltage (outputting preliminary control voltage to node N21) according to the data signal (data signal on Dm) and the first scan signal (first scan signal on S1n)." EX1002, ¶87.



Annotated Kim406 Figure 6 (left) and 757 patent Figure 4 (right) are shown above. Kim406 discloses M22 is a PMOS transistor with a gate coupled to S1n, a first electrode coupled to the data line Dm, and a second electrode coupled to first node N21, such that during T2 and T3, M22 outputs a preliminary control voltage to the first node N21 according to the data signal on Dm and the low first scan signal on S1n. EX1004, Figs. 6-7, [0055], [0063] (PMOS), [0064] (T2 and T3). The second electrode of M22 is electrically connected to the voltage adjustment unit (M25) and couple unit (C2st). *Id.*, Fig. 6, [0055], [0059], [0061]. Under 112f, Kim406's PMOS transistor M22 as connected performs the claimed function and is identical to the corresponding structure for the input unit 215 (PMOS transistor 216 as connected). EX1001, Fig. 4, 4:34-38; EX1002, ¶88.

7. [1f]

Kim406 discloses "a voltage adjustment unit (M25), electrically connected to the transmission line (En) and the input unit (M22), for adjusting the preliminary control voltage (voltage at N21) according to the emission signal (emission control signal on En) and a second reference voltage (Vint)." EX1002, ¶89.



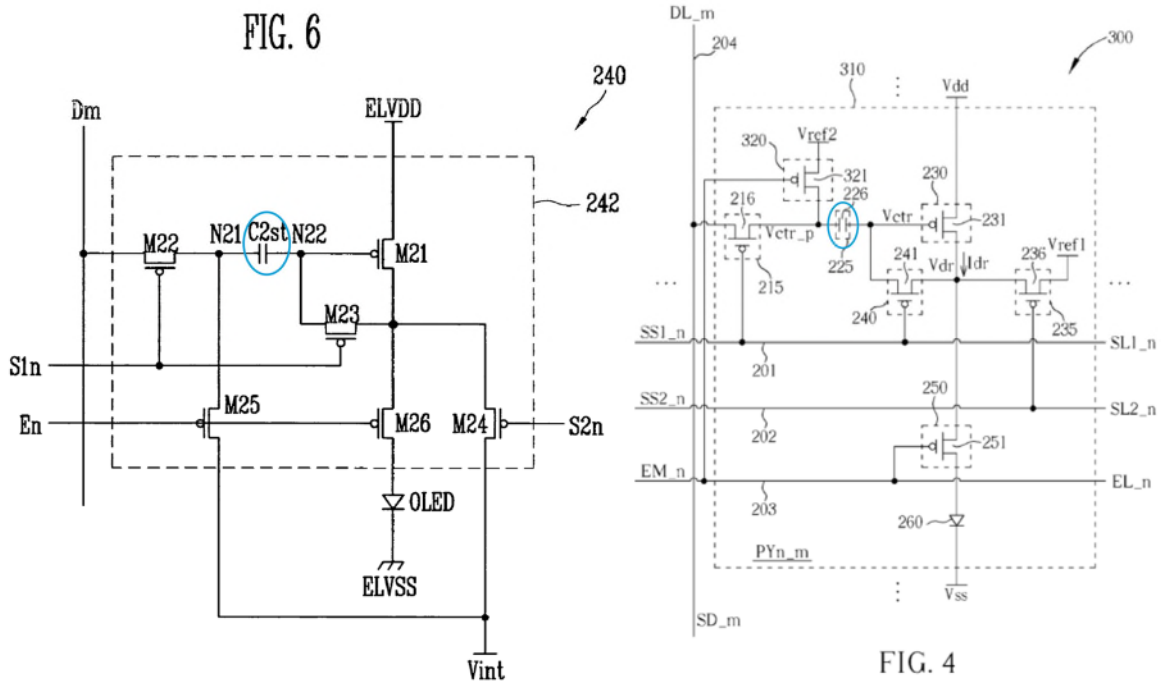
Annotated Kim406 Figure 6 (left) and 757 patent Figure 4 (right) are shown above. Kim406 discloses M25 is a PMOS transistor with a gate coupled to En, a first electrode connected to M22 and C2st (first node N21), and a second electrode coupled to initialization power source Vint, such that during T5, M25 adjusts the preliminary control voltage (voltage on first node N21) according to the low emission control signal on En and Vint. EX1004, Figs. 6-7, [0059], [0063] (PMOS), [0067] (when the fifth transistor M25 is turned on, the voltage value of

the first node N21 is reduced to the voltage value of the initialization power source Vint). *See* EX1001, 5:47-52, 6:43-48. Under 112f, Kim406's PMOS transistor M25 as connected performs the claimed function and is identical to the corresponding structure for the voltage adjustment unit 320 disclosed in the 757 patent (PMOS transistor 321 as connected). EX1001, Fig. 4, 6:36-42; EX1002, ¶90.

Kim406 discloses M25 is connected to "Vint" while the corresponding structure 321 is connected to "Vref2," but this difference in naming convention is not relevant. Vint in Kim406 is a reference voltage, which is all that is required under the primary construction. Under the alternative construction, see below for [1i]. EX1002, ¶91.

8. [1g]

Kim406 discloses "a couple unit (C2st), electrically connected to the input unit (M22) and the voltage adjustment unit (M25), for adjusting a control voltage (voltage on N22) through coupling a change of the preliminary control voltage (capacitor C2st couples the change of the preliminary control voltage at N21 to adjust the voltage at N22)." EX1002, ¶92.



Annotated Kim406 Figure 6 (left) and 757 patent Figure 4 (right) are shown above. Kim406 discloses storage capacitor C2st is between N21 and N22 and is charged during T3 to the voltage difference between N21 and N22. EX1004, Fig. 6, [0061], [0065]. N22 is floated in T4 and T5 by turning off M23, and in T5 when the preliminary control voltage at N21 is changed from the preliminary data signal voltage by application of Vint (*see* [1f]), capacitor C2st couples that change in voltage to N22, causing the voltage on N22 to change by the same amount. *Id.*, Fig. 7, [0066] (T4 turns off M22 and M23), [0067] (reducing voltage of N21 from data to Vint, and adjusting voltage of N22 with a reduction corresponding to the reduction of N21 to maintain a difference in C2st), [0069], claims 7 (second terminal (N22) floats), 8 (explaining how voltage at second terminal of capacitor

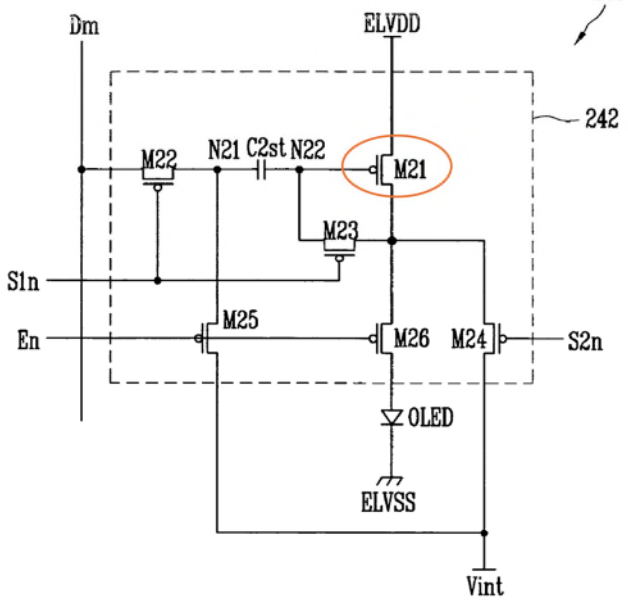
(N22) is reduced corresponding to the voltage drop at first terminal (N21)). EX1002, ¶93.

Under 112f, Kim406's capacitor C2st as connected performs the claimed function and is identical to the corresponding structure for the couple unit 225 in the 757 patent (capacitor 226 as connected). EX1001, Fig. 4, 4:42-44. EX1002, ¶94.

9. [1h]

Kim406 discloses "a driving unit (M21), electrically connected to the couple unit (C2st), for providing a driving current and a driving voltage (current and voltage at second electrode of M21), according to the control voltage (voltage at N22) and a first power voltage (ELVDD)." EX1002, ¶95.

FIG. 6



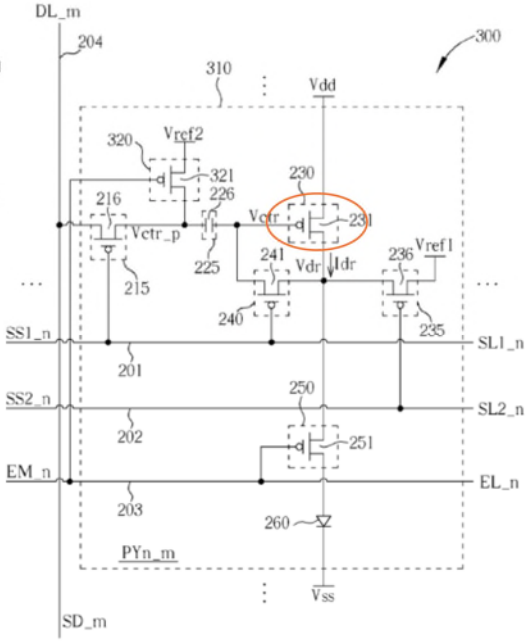


FIG. 4

Annotated Kim406 Figure 6 (left) and 757 patent Figure 4 (right) are shown above. Kim406 discloses M21 is a PMOS transistor with a gate coupled to C2st via node N22, a first electrode coupled to ELVDD, and a second electrode coupled to an unlabeled node with M23, M24, and M26, such that during T5 when M21 is turned on by the control voltage at N22 and EN turns on M26, M21 provides a driving current and driving voltage at its second electrode. EX1004, Figs. 6-7, [0056], [0063] (PMOS), [0067]-[0070] (describing M21 driving OLED through M26). Under 112f, Kim406's PMOS transistor M21 as connected performs the claimed function and is identical to the corresponding structure for the driving unit disclosed in the 757 patent (PMOS transistor 231 as connected). EX1001, Fig. 4, 4:38-41. EX1002, ¶96.

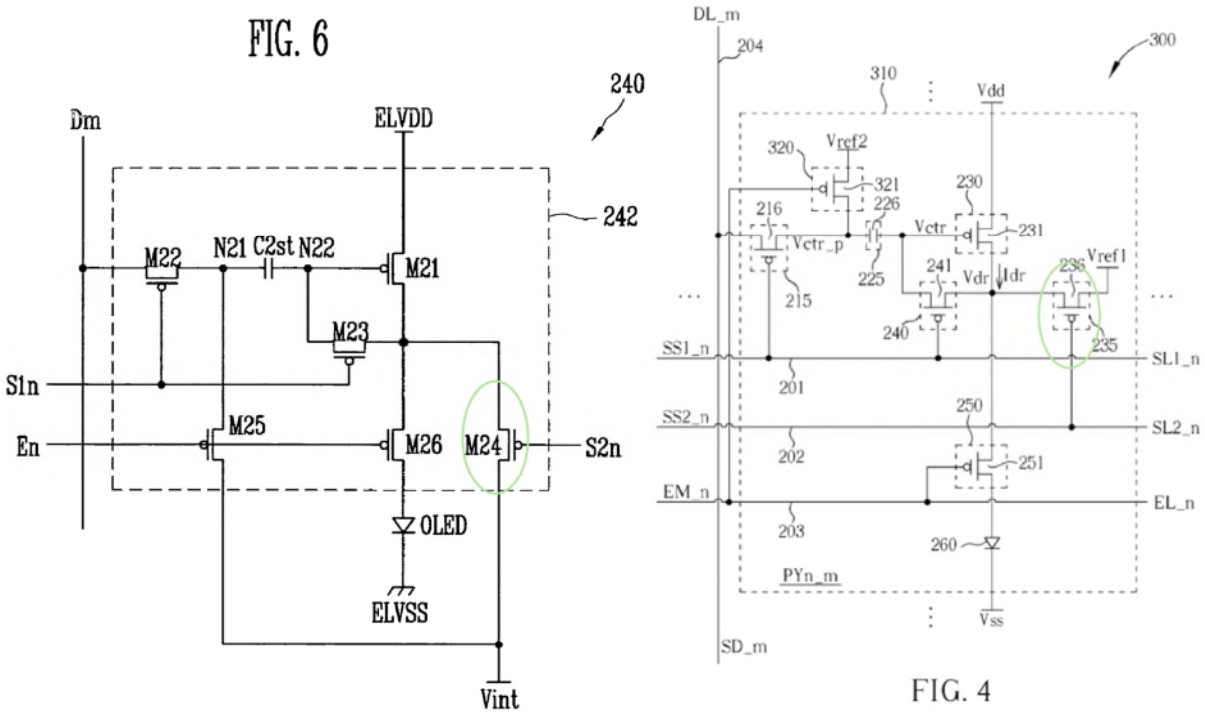
Kim406 explicitly discloses that M21 provides a driving current at its second electrode which, during T5 when M26 is on, will drive the OLED. EX1004, Fig. 7, [0056], [0067]-[0070]. And Kim406 discloses that driving current provided by M21 is provided according to ELVDD and the control voltage at N22 applied to the gate of M21. *Id.*; EX1002, ¶97.

Kim406 inherently discloses that M21 provides a "driving voltage." A POSITA would have known it was inherent from the electrical properties of Kim406's circuit that M21 is also providing a driving voltage with the driving current. To provide a driving current as disclosed in Kim406 a POSITA would

have known that there must also be a driving voltage, i.e., the difference in potential between the second electrode of M21 and ELVSS. A POSITA would have known that without that difference in potential, there would be no driving current as disclosed in Kim406 and the OLED would not emit light. A POSITA would have known that the precise magnitude of the driving voltage provided by M21 would be ELVDD minus the voltage drop across M21. EX1004, [0065], [0069]; EX1002, ¶98 (explaining diode equation).

10. [1i]

Kim406 discloses "a first reset unit (M24), electrically connected to the driving unit (M21) and the second scan line (S2n), for resetting the driving voltage (voltage at second electrode of M21) according to the second scan signal (S2n) and a first reference voltage (Vint)." EX1002, ¶99.



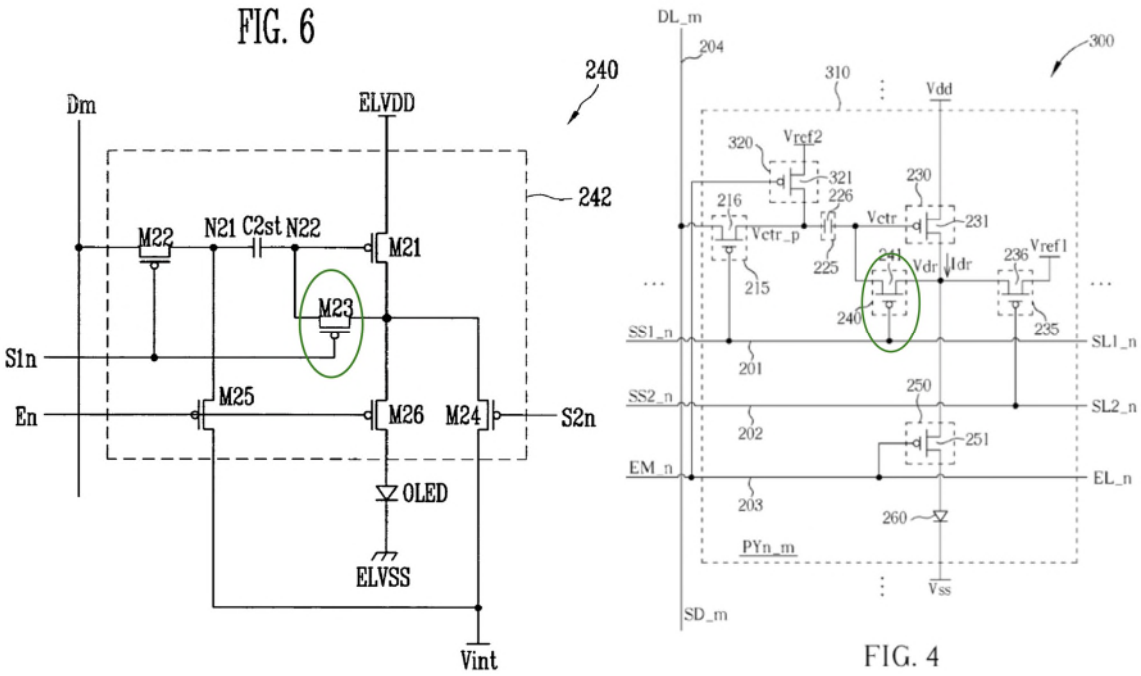
Annotated Kim406 Figure 6 (left) and 757 patent Figure 4 (right) are shown above. Kim406 discloses M24 is a PMOS transistor with a gate coupled to S2n, a first electrode coupled to the second electrode of M21 (and first electrode of M23 and first electrode of M26), and a second electrode coupled to the initialization power source Vint, such that during T2 when M24 is turned on by the second scan signal on S2n, it resets the driving voltage at the second electrode of M21 to Vint. EX1004, Figs. 6-7, [0058], [0063] (PMOS), [0064] (disclosing how during T2 M24 provides Vint to the node including the second electrode of M21, so that M23 can provide Vint to N22). *See* EX1001, 5:16-22. Vint provides a first reference voltage for M24 and a second reference voltage for M25 under the primary construction that encompasses the same voltage. Under 112f, Kim406's PMOS

transistor M24 as connected performs the claimed function and is identical to the corresponding structure for the first reset unit disclosed in the 757 patent (PMOS transistor 236 as connected). EX1001, Fig. 4, 4:44-48. EX1002, ¶100.

Kim406 discloses M24 is connected to "Vint" while the corresponding structure 326 is connected to "Vref1," but this difference in naming convention is not relevant. Vint in Kim406 is a reference voltage, which is all that is required under the primary construction. EX1002, ¶101.

11. [1j]

Kim406 discloses "a second reset unit (M23), electrically connected to the driving unit (M21), the first reset unit (M24), and the first scan line (S1n), for resetting the control voltage (voltage at N22) according to the first scan signal (S1n) and the driving voltage (voltage at second electrode of M21)." EX1002, ¶102.



Annotated Kim406 Figure 6 (left) and 757 patent Figure 4 (right) are shown above. Kim406 discloses M23 is a PMOS transistor with a gate coupled to S1n, a first electrode coupled to the second electrode of M21 (and M24 and M26), and a second electrode coupled to the gate of the M21 and C2st (N22), such that when M23 is turned on by the first scan signal on S1n, the driving voltage (voltage at second electrode of M21) is applied to reset the control voltage at N22. EX1004, Figs. 6-7, [0057], [0063]-[0065]. EX1002, ¶103.

During T2, the control voltage (N22) is reset according to low scan signal (S1n) and the driving voltage Vint (voltage at second electrode of M21). Specifically, S1n and S2n are supplied turning M23 and M24 on, such that the voltage on Node N22 is reset to Vint. EX1004, Figs. 6-7, [0064]; EX1002, ¶104.

During T3, the control voltage (N22) is reset according to low scan signal (S1n) and the driving voltage ELVDD-|Vth| (voltage at second electrode of M21). Specifically, S1n is still supplied keeping M23 on, but S2n is not supplied and M24 is turned off, such that the voltage on Node N22 is reset to ELVDD-|Vth|. EX1004, Figs. 6-7, [0065] (disclosing how current flows through M21 as a diode until "the voltage value of the second node N22 is obtained by subtracting the threshold voltage value of the first transistor M21 from the voltage value of the first power source ELVDD"). Kim406 discloses this reset is performed to compensate for the threshold voltage of M21. *Id.*, [0067]-[0069]; EX1002, ¶105.

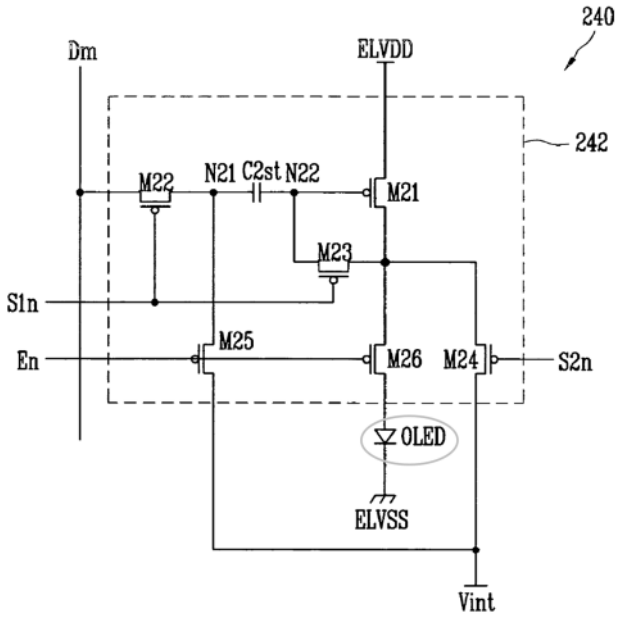
Kim406's disclosure in this regard is identical to the disclosure of the 757 patent wherein during T1, Vctrl is reset to Vref1 through 236 and 241 to ensure the driving transistor is in a conductive state, and during T2, Vctrl is reset to VDD-|Vth| through 241 to compensate for the threshold voltage of the driving transistor. EX1001, Fig. 3, 5:15-22 (T1), 5:23-38 (T2). EX1002, ¶106.

Under 112f, Kim406's PMOS transistor M23 as connected performs the claimed function and is identical to the corresponding structure for the second reset unit disclosed in the 757 patent (PMOS transistor 241 as connected). EX1001, Fig. 4, 4:48-52. EX1002, ¶107.

12. [1k]

Kim406 discloses "an organic light emitting diode (OLED) for generating output light according to the driving current." EX1002, ¶108.

FIG. 6

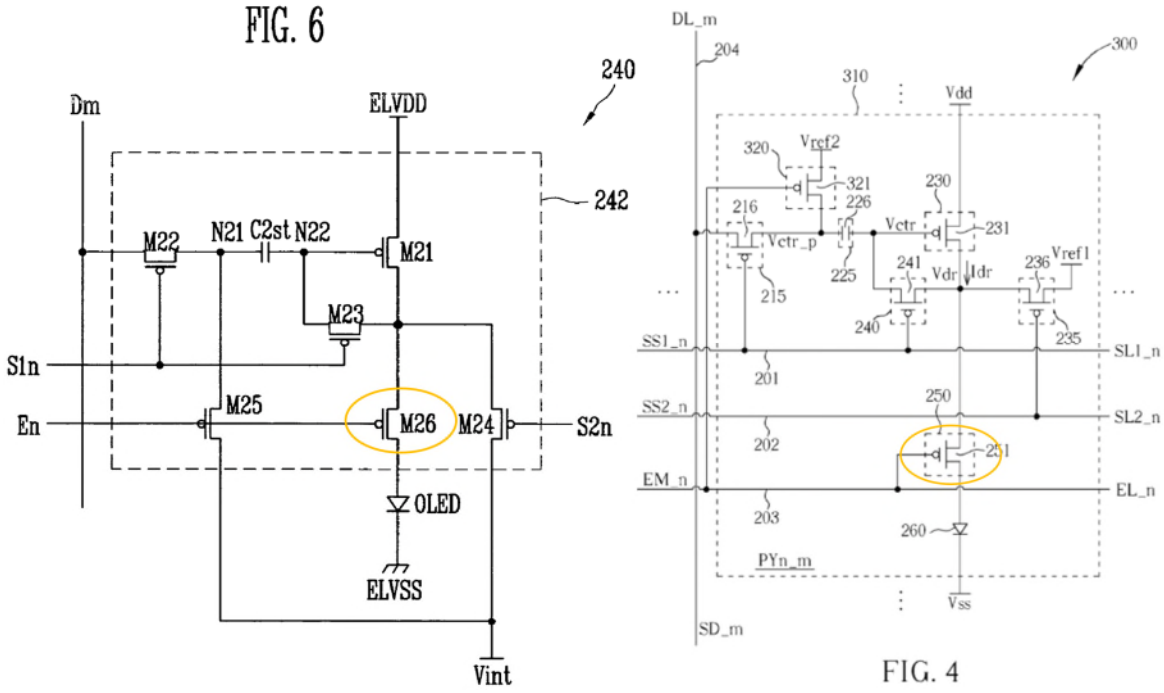


Kim406 discloses that the OLED is driven by the driving current provided by M21 to generate output light. EX1004, Fig. 6, [0052]-[0054], [0056], [0060], [0067]-[0070]. The amount of control voltage at N22 on the gate of M21 determines the amount of driving current M21 provides and, therefore, the brightness of the OLED. *Id.* EX1002, ¶109.

13. [1l]

Kim406 discloses "an emission enable unit (M26), electrically connected to the transmission line (En), the driving unit (M21), and the organic light emitting diode (OLED), for providing a control of furnishing the driving current to the

organic light emitting diode according to the emission signal (En)." EX1002, ¶110.



Annotated Kim406 Figure 6 (left) and 757 patent Figure 4 (right) are shown above. Kim406 discloses M26 is a PMOS transistor with a gate coupled to En, a first electrode coupled to the second electrode of M21 (and M23 and M24), and a second electrode coupled to the anode of the OLED, such that during T5 when M26 is turned on by the emission control signal on En, it furnishes the driving current from the second electrode of M21 to the OLED. EX1004, Figs. 6-7, [0060], [0063] (PMOS), [0067]-[0070] (disclosing how during T5 the low emission control signal causes M26 to turn on such that the driving current from the second electrode of M21 flows through M26 and drives the OLED). Under 112f, Kim406's PMOS transistor M26 as connected performs the claimed function and is

identical to the corresponding structure for the emission enable unit disclosed in the 757 patent (PMOS transistor 251 as connected). EX1001, Fig. 4, 4:54-58. EX1002, ¶111.

B. Claim 2:

Kim406 discloses claim 1 "wherein the input unit (M22) comprises a first transistor (M22), the first transistor having a first end (first electrode) electrically connected to the data line (Dm), a gate end electrically connected to the first scan line (S1n), and a second end (second electrode) electrically connected to the voltage adjustment unit (M25) and the couple unit (C2st)." *See* [1e]. EX1002, ¶112.

C. Claim 3:

Kim406 discloses claim 2, "wherein the first transistor (M22) comprises a thin film transistor or a field effect transistor (PMOS or NMOS)." EX1002, ¶113.

Kim406 discloses its transistors are PMOS or NMOS transistors. EX1004, [0026], [0063]. A POSITA would have known that PMOS and NMOS transistors are types of field effect transistors (FETs). Specifically, a POSITA would have known that PMOS and NMOS transistors are types of MOSFETs. EX1007, page 23; EX1002, ¶114.

D. Claim 4:

Kim406 discloses claim 1, "wherein the driving unit (M21) comprises a second transistor (M21), the second transistor (M21) having a first end (first

electrode) for receiving the first power voltage (ELVDD), a gate end for receive the control voltage (N22), and a second end (second electrode) for outputting the driving current and the driving voltage. *See* [1h]. EX1002, ¶115.

E. Claim 5:

See Claim 3, 4. EX1002, ¶116.

F. Claim 6:

Kim406 discloses claim 1 "wherein the couple unit (C2st) comprises a capacitor (C2st) electrically connected between the input unit (M22) and the driving unit (M21). *See* [1g]. EX1002, ¶117.

G. Claim 7:

Kim406 discloses claim 1 "wherein the first reset unit (M24) comprises a third transistor (M24), the third transistor having a first end (second electrode) for receiving the first reference voltage (Vint), a gate end electrically connected to the second scan line (S2n), and a second end (first electrode) electrically connected to the drive unit (M21), the second reset unit (M23) and the emission enable unit (M26). *See* [1i], [1j]-[1l]; EX1002, ¶118.

H. Claim 8:

See Claim 3, 7. EX1002, ¶119.

I. Claim 9:

Kim406 discloses claim 1 "wherein the second reset unit (M23) comprises a fourth transistor (M23), the fourth transistor having a first end (first electrode)

electrically connected to the driving unit (second electrode of M21), the first reset unit (M24) and the emission enable unit (M26), a gate end electrically connected to the first scan line (S1n), and a second end (second electrode) electrically connected to the couple unit (C2st) and the driving unit (gate of M21). *See* [1j], [1h]-[1l]. EX1002, ¶120.

J. Claim 10:

See Claim 3, 9. EX1002, ¶121.

K. Claim 11:

Kim406 discloses claim 1 "wherein the voltage adjustment unit (M25) comprises a fifth transistor (M25), the fifth transistor having a first end for receiving the second reference voltage (Vint), a gate end electrically connected to the transmission line (En), and a second end electrically connected to the input unit (M22) and the couple unit (C2st)." *See* [1f], [1e]-[1g]. EX1002, ¶122.

L. Claim 12:

See Claim 3, 11. EX1002, ¶123.

M. Claim 14:

Kim406 discloses claim 1 "wherein the emission enable unit (M26) comprises a sixth transistor (M26), the sixth transistor having a first end electrically connected to the driving unit (M21), the first reset unit (M24) and the second reset unit (M23), a gate end electrically connected to the transmission line

(En), and a second end electrically connected to the organic light emitting diode (OLED). *See* [1l], [1e], [1h], 7, 9. EX1002, ¶124.

N. Claim 15:

See Claim 3, 14. EX1002, ¶125.

O. Claim 16:

Kim406 discloses claim 1 "wherein the organic light emitting diode (OLED) comprises an anode electrically connected to the emission enable unit (M26) and a cathode for receiving a second power voltage (ELVSS)." *See* [1k]; EX1004, Fig. 6, [0053] ("The anode electrode of the OLED is coupled to the pixel circuit 242 and the cathode electrode of the OLED is coupled to the second power source ELVSS."); EX1002, ¶126.

P. Claim 17:

1. [17pre]

Kim406 discloses "a driving method, comprising." Kim406 discloses the pixel circuit in Figure 6 to drive an OLED as shown above. *See* Claim 1. Kim406 discloses in Figure 7 "a method of driving the pixel" of Figure 6. EX1004, Fig. 7, [0021]; EX1002, ¶`17.

2. [17a]

Kim406 discloses "outputting a preliminary control voltage (voltage at N21) by an input unit (M22) according to a data signal (data signal on Dm) and a first scan signal (first scan signal on S1n)." *See* [1e]; EX1002, ¶128.

3. [17b]

Kim406 discloses "adjusting the preliminary control voltage (voltage on N21) by a voltage adjustment unit (M25) according to an emission signal (emission control signal on En) and a second reference voltage (Vint)." *See* [1f]; EX1002, ¶129.

4. [17c]

Kim406 discloses "adjusting a control voltage (adjusting voltage on N22) by a couple unit (C2st) through coupling a change of the preliminary control voltage (capacitor C2st couples the change of the preliminary control voltage at N21 to the voltage at N22)." *See* [1g]; EX1002, ¶130.

5. [17d]

Kim406 discloses "providing a driving current and a driving voltage (current and voltage at second electrode of M21) by a driving unit (M21) according to the control voltage (voltage at N22) and a power voltage (ELVDD)." *See* [1h]; EX1002, ¶131.

6. [17e]

Kim406 discloses "resetting the driving voltage (voltage at second electrode of M21) by a first reset unit (M24) according to a second scan signal (S2n) and a first reference voltage (Vint)." *See* [1i]; EX1002, ¶132.

7. [17f]

Kim406 discloses "resetting the control voltage (voltage at N22) by a second reset unit (M23) according to the first scan signal (S1n) and the driving voltage (voltage at second electrode of M21)." *See* [1j]; EX1002, ¶133.

8. [17g]

Kim406 discloses "generating output light by an organic light emitting diode (OLED) according to the driving current (current at second electrode of M21)." *See* [1k]; EX1002, ¶134.

9. [17h]

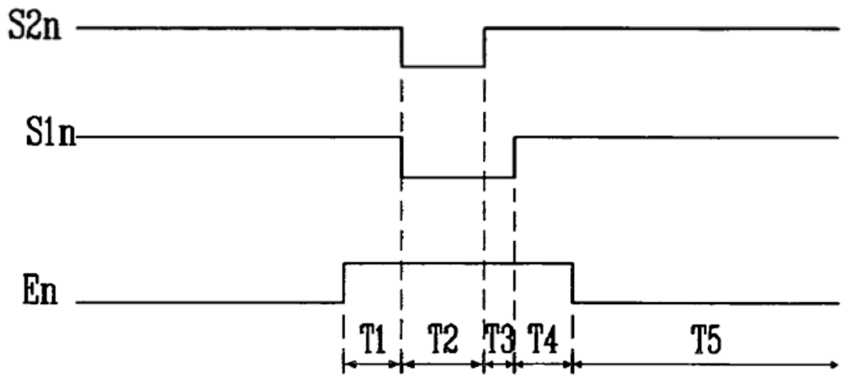
Kim406 discloses "providing a control of furnishing the driving current to the organic light emitting diode (OLED) by an emission enable unit (M26) according to the emission signal (En)." *See* [1l]; EX1002, ¶135.

10. [17i]

Kim406 discloses "providing the first scan signal (S1n) with a first level (low) to the input unit (M22) and the second reset unit (M23), providing the second scan signal (S2n) with the first level (low) to the first reset unit (M24), providing the emission signal (En) with a second level (high) different from the first level (low) for disabling a voltage adjusting operation of the voltage adjustment unit (M25) and disabling a current furnishing operation of the emission enable unit (M26), and providing the data signal (Dm) to the input unit (M22) during a first interval (T2)." *See* [1e]-[1f], [1i]-[1j], [1l]; EX1004, Fig. 7 (at T2 showing S1n

low, S2n low and En high), [0063]-[0064] (explaining that in T2 low signals on S1n and S2n turn on PMOS transistors M22, M23, M24 and high signal on En turns off PMOS transistors M25 and M26), [0026]; EX1002, ¶136 (explaining PMOS/NMOS).

FIG. 7



11. [17j]

Kim406 discloses "outputting the preliminary control voltage by the input unit (M22) according to the data signal (Dm) and the first scan signal (S1n) during the first interval (T2)." *See* [1e] (M22), [17a] (same), [17i] (T2); EX1002, ¶137.

12. [17k]

Kim406 discloses "resetting the driving voltage by the first reset unit (M24) according to the second scan signal (S2n) and the first reference voltage (Vint) during the first interval (T2)." *See* [1i] (M24), [17e] (same), [17i] (T2); EX1002, ¶138.

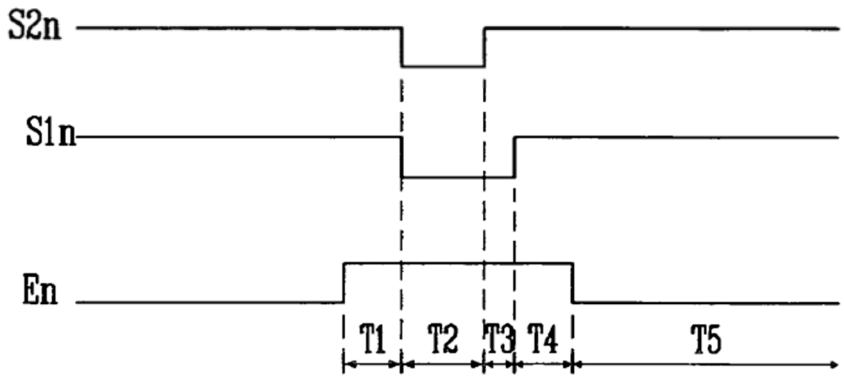
13. [17l]

Kim406 discloses "resetting the control voltage by the second reset unit (M23) according to the first scan signal (S1n) and the driving voltage (voltage at second electrode of M21) during the first interval (T2)." *See* [1j] (M23), [17f] (same), [17i] (T2); EX1002, ¶139.

14. [17m]

Kim406 discloses "switching the second scan signal (S2n) from the first level (low) to the second level (high) for disabling a resetting operation of the first reset unit (M24) during a second interval (T3) following the first interval (T2)." *See* EX1004, Fig. 7 (T3), [0063]-[0065] (explaining during T3 S2n goes high turning off PMOS transistor M24); EX1002, ¶140.

FIG. 7



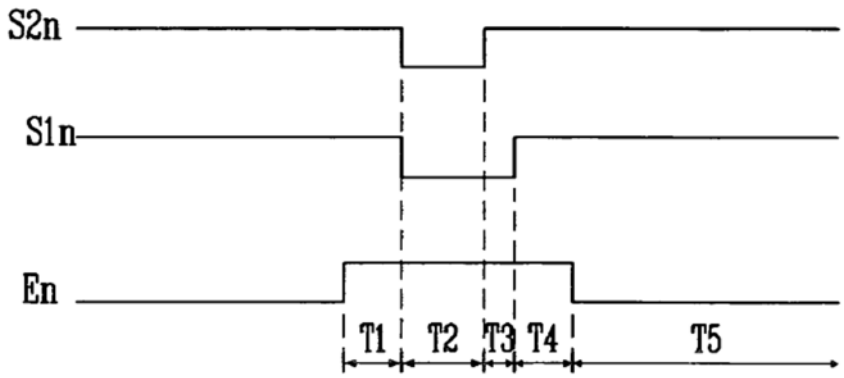
15. [17n]

Kim406 discloses "performing a threshold voltage compensation operation on the control voltage (voltage at N22) by the second reset unit (M23) and the driving unit (M21) according to the first scan signal (S1n) and the power voltage (ELVDD) during the second interval (T3)." *See* [1j] (explaining voltage compensation), [17f]; EX1004, [0065] (explaining that during T3, M21 serves as a diode such that a voltage according to ELVDD minus the threshold voltage of M21 is applied to N22), [0069] (explaining how this achieves voltage threshold compensation such that correct brightness is created "regardless of the threshold voltage" of M21); EX1002, ¶141.

16. [17o]

Kim406 discloses "switching the first scan signal (S1n) from the first level (low) to the second level (high) for disabling a resetting operation of the second reset unit (M23) and disabling an inputting operation of the input unit (M22) during a third interval (T4) following the second interval (T3)." EX1004, Fig. 7, [0066] (explaining that during T4, S1n goes high turning off PMOS transistors M22 and M23); EX1002, ¶142.

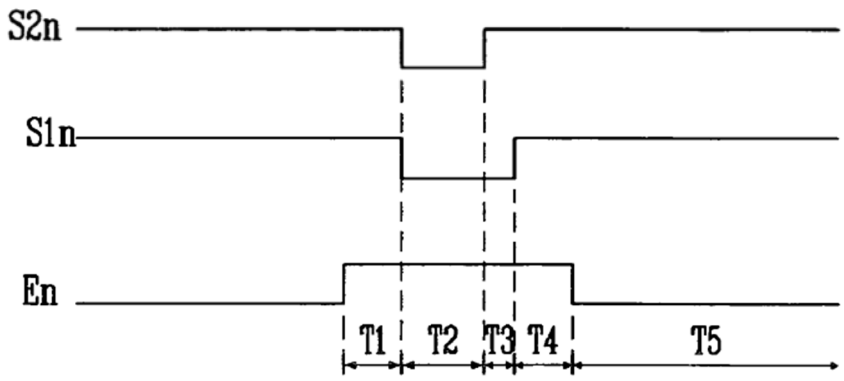
FIG. 7



17. [17p]

Kim406 discloses "switching the emission signal (En) from the second level (high) to the first level (low) during a fourth interval (T5) following the third interval (T4)." *See* [1l]; EX1004, Fig. 7, [0067]-[0069]; EX1002, ¶143.

FIG. 7



18. [17q]

Kim406 discloses "adjusting the preliminary control voltage (voltage at N21) by the voltage adjustment unit (M25) according to the emission signal (En) and the second reference voltage (Vint) during the fourth interval (T5)." *See* [1f] (M25), [17b] (same); EX1004, Fig. 7, [0067] (explaining En going low turns on PMOS transistor M25 such that N21 is changed by applying Vint); EX1002, ¶144.

19. [17r]

Kim406 discloses "adjusting the control voltage (adjusting the voltage at N22) by the couple unit (C2st) through coupling a change of the preliminary control voltage (coupling change in voltage at N21 to adjust the voltage at N22 by same amount) during the fourth interval (T5)." *See* [1g] (C2st), [17c] (same); EX1004, Fig. 7, [0067] (explaining C2st couples the change in N21 to N22 during T5); EX1002, ¶145.

20. [17s]

Kim406 discloses "providing the driving current (current provided on second electrode of M21) by the driving unit (M21) according to the control voltage (voltage at N22) and the power voltage (ELVDD) during the fourth interval (T5)." *See* [1h] (M21), [17d]; EX1004, [0067-[0069] (explaining during T5 M21 provides driving current to drive OLED according to the voltage at N22 and ELVDD); EX1002, ¶146.

21. [17t]

Kim406 discloses "furnishing the driving current to the organic light emitting diode (OLED) by the emission enable unit (M26) according to the emission signal (En) during the fourth interval (T5)." *See* [1l] (M26), [17e]; EX1004, Fig. 7, [0067]-[0069] (explaining that during T5 En goes low turning PMOS transistor M26 on to provide driving current to OLED); EX1002, ¶147.

22. [17u]

Kim406 discloses "generating output light by the organic light emitting diode (OLED) according to the driving current during the fourth interval (T5)." *See* [1k] (OLED), [17g] (same); EX1004, [0068]-[0069] (OLED generates light according to driving current during T5); EX1002, ¶148.

Q. Claim 18:

Kim406 discloses the method of claim 17, "wherein the second level (high) is greater than the first level (low)." *See* [17i]; EX1002, ¶149.

R. Claim 19:

Kim406 discloses the method of claim 17, "wherein the first level (high) is greater than the second level (low)." EX1002, ¶150.

As shown above, Kim406 discloses PMOS transistors with a second level (high-turn off) voltage which is greater than the first level (low-turn on) voltage. *See* [17i] (PMOS), 18; EX1002, ¶151.

Claim 19 reverses the levels, such that the first level (high-turn on) is greater than the second level (low-turn off). Kim406 discloses the PMOS transistors, which are turned on by low gate voltages and off by high gate voltages, can instead be NMOS transistors, which are turned on by high gate voltages and off by low gate voltages. EX1004, [0063] (NMOS uses the different signals). A POSITA would have been familiar with PMOS and NMOS transistors and known they were turned on and off by opposite gate voltages. Thus, Kim406 teaches that its PMOS embodiment can be implemented as an NMOS embodiment using the opposite gate voltages. EX1002, ¶152.

In Kim406's NMOS embodiment the voltage levels shown in Figure 7 would have been reversed to maintain the same functionality, i.e., the second level that turns the transistors off during the correct time periods would be low and the first level that turns the transistors on during the correct time periods would be high. Thus, in Kim406's NMOS embodiment, the first level (on, high) is greater than the second level (off, low). EX1002, ¶153.

VI. GROUND 2: CLAIMS 1-20 ARE OBVIOUS OVER THE COMBINATION OF KIM406 AND KIM730

Kim406 discloses the second reference voltage is Vint. *See* [1f]. It would have been obvious to a POSITA that Vint could have been ELVDD, the first power voltage. EX1002, ¶154.

A. Combination Rationale

Kim730 shares the common inventor with Kim406 and discloses similar OLED pixel driving circuits. EX1002, ¶155.

FIG.8

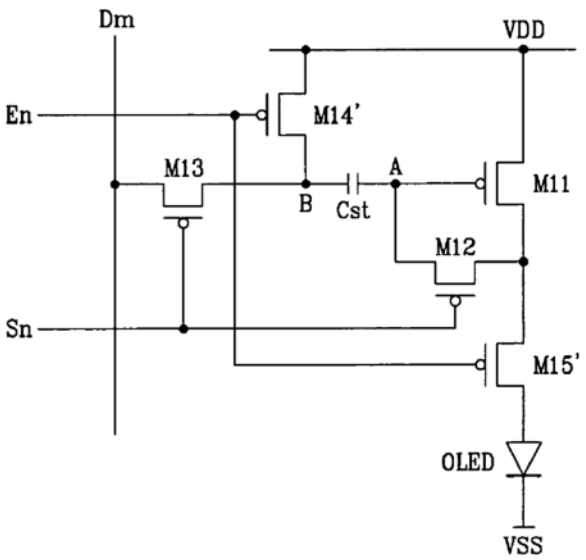
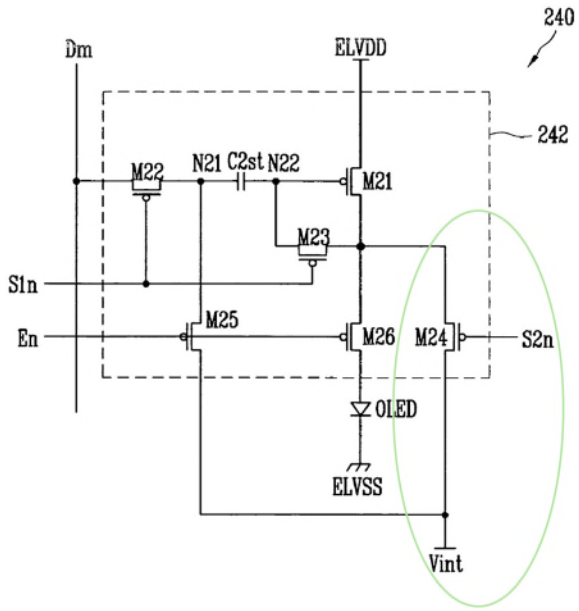


FIG. 6



Above are Figure 8 (left) of Kim730 and Figure 6 (right) of Kim406. The differences in the circuits are 1) Kim730's voltage adjustment unit (M14') is connected to VDD while Kim406's (M25) is connected to Vint and 2) Kim406 includes a first reset unit M24 for resetting the driving voltage using S2n, first reference voltage Vint and also as a second reference voltage Vint for M25. EX1002, ¶156.

It would have been obvious to a POSITA to modify the adjustment unit in Kim406 (M25) to use VDD as the reference voltage, instead of Vint, based on the teachings of Kim730. Kim730 explains how the voltage adjustment unit M14' can

be connected to VDD to make a voltage adjustment. EX1005, Figs. 7-8, [0052]-[0060], [0067]. Kim730 explains how M14' can be connected to a third voltage "V_{sus}" to make a voltage adjustment. *Id.*, Fig. 10 [0062]-[0068]. Thus, a POSITA would have understood each of these options was a known design choice. And because it was known to connect voltage adjustment units to VDD, VSS, or a third voltage source, none of those design choices is novel or non-obvious. In the combination a POSITA would have also understood to continue to use Vint (instead of VDD) at M24 to ensure M23 and M24 ensure M21 is put in a conductive state for reset as disclosed by Kim406 and because the voltage value of the "initialization power source Vint is set to be smaller than the voltage value of the data signal" which would not be true for VDD. EX1004, [0064]; EX1002, ¶157.

A POSITA would also have been motivated to use different reference voltage sources for each unit in order to use the optimum reference voltage for that unit to improve the efficiency and performance of the pixel circuit. Each of these voltage adjustments is different. Thus, using a reference voltage that is tailored to each particular desired voltage adjustment would improve the speed of the pixel circuit and reduce the overall power consumption of the pixel circuit. It was known that using different reference voltage sources would also reduce the voltage swing for driving the OLED display. A POSITA would have known of these

advantages and how significant they can become for large displays with thousands of pixels. EX1002, ¶158.

A POSITA would have had a reasonable expectation of success in making the modification. Kim730 teaches it was a known technique in the art to use VDD to perform a positive voltage adjustment and that each of the design choices could be used for a circuit. EX1004, Figs. 6-10 and accompanying text. EX1002, ¶159.

B. Claims 13, 20

The combination discloses "the organic light emitting display of claim 11, wherein the second reference voltage is the first power voltage" (claim 13) and "the driving method of claim 17, wherein the second reference voltage is the power voltage" (claim 20). *See* Ground 1, claims 11 and 17. In this combination, Kim406's voltage adjustment unit (M25) would have been connected to the first power voltage ELVDD in Kim406, based on the teachings in Kim730 as explained above. *See* [1f] (M25 connected to Vint), 11 (same); EX1005, Figs. 7-8, [0052]-[0061]; EX1002, ¶160.

C. Claims 1-20

Under the alternative construction that requires the first and second voltages in independent claims 1 and 17 to be different voltages, claims 1-20 are rendered obvious by the combination because, in the combination, the first reference voltage

is still Vint as taught by Kim406, while the second reference voltage has been changed to VDD as taught by Kim730 as explained above. EX1002, ¶161.

VII. GROUND 3: CLAIMS 1-21 ARE ANTICIAPTED BY SENDA

A. Senda's Modified Third Embodiment

Senda anticipates the claims because Senda expressly discloses a modified third embodiment that practices the claims, thereby disclosing to a POSITA within its four corners all elements of the claims as arranged in the claims. Specifically, Senda discloses its third embodiment (Fig. 6) should be modified as explained with respect to the seventh embodiment (Fig. 15) by connecting the PMOS transistor 314 shown in Figure 6 to Node C as illustrated by transistor 714 in Figure 15. EX1006, [0218]-[0219]. Senda discloses the modification initially with reference to the fifth embodiment (Fig. 11) by explaining that the first reset transistor connected to Node A (as showing in Fig. 11) should instead be connected to Node C (as shown in Fig. 15). *Id.* Senda explains this modification reduces leakage at Node A and thereby enhances display quality. *Id.* Senda then discloses this modification should also be made for embodiments 1-4 and 6. *Id.* Senda discloses no other modification should be made to the third embodiment, other than to move the connection of the relevant transistor (PMOS transistor 314 in the case of the third embodiment) from Node A to Node C. *Id.* Senda claims the modified third embodiment in dependent claim 5. *Id.*, claim 1 (claiming fourth switching element

in either position), claim 3 (claiming position of third embodiment), claim 5 (claiming position of modified third embodiment). Thus, Senda's "Modified 3rd Embodiment" can also be referred to as Senda's "claim 5 embodiment." EX1002, ¶162.

Figures 6 and 15 of Senda are shown below with annotations highlighting transistors 314 and 714. EX1002, ¶163.

Fig. 6

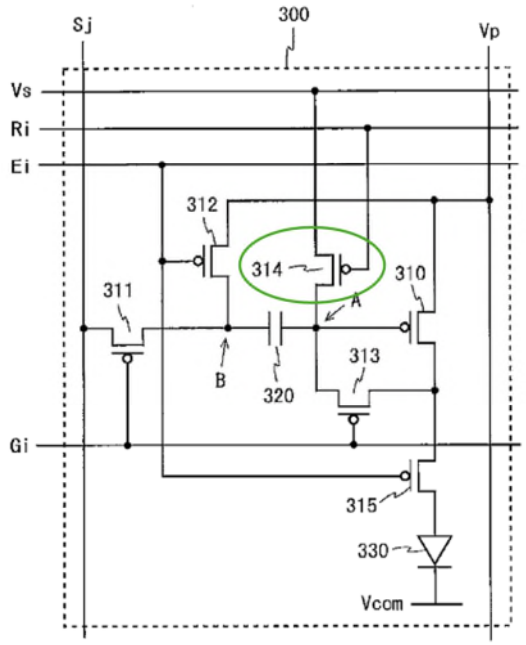
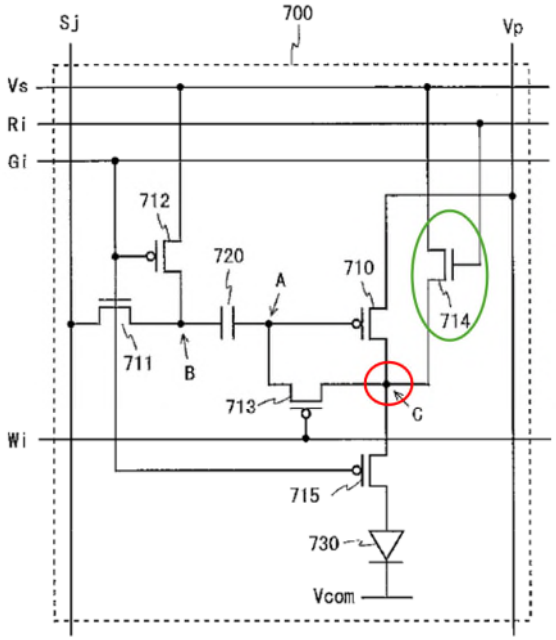
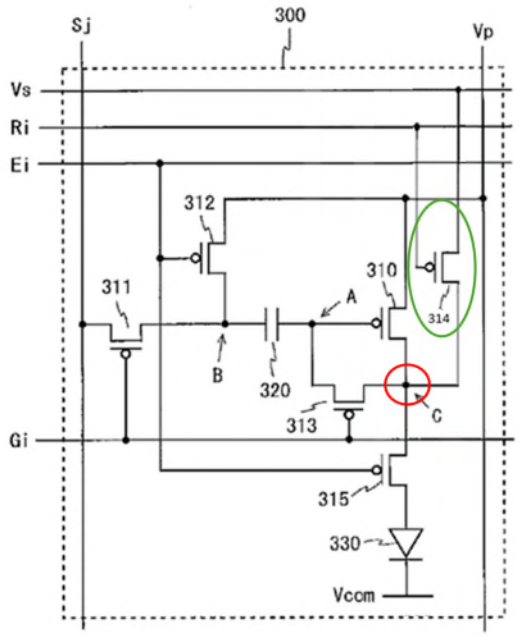


Fig. 15



A modified Figure 6 is shown below, which illustrates Senda's Modified 3rd Embodiment with PMOS transistor 314 connected to Node C, with no other changes to the third embodiment, as disclosed and claimed by Senda. EX1006, [0218]-[0219]; EX1002, ¶164.

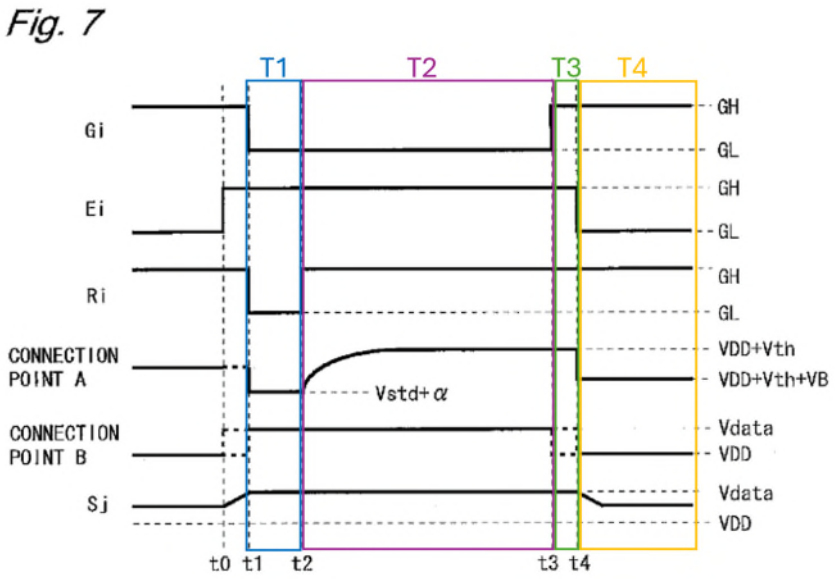
Senda's Modified 3rd Embodiment



This modification of Figure 6 illustrating Senda's Modified 3rd Embodiment will be used in the analysis of the claims below. Evidentiary citations will still be made to the original Figure 6 transistor 314, as well as Senda's disclosure to connect that transistor to Node C. EX1002, ¶165.

Based on Senda's disclosure that the only modification that should be made to the third embodiment is to connect the transistor to Node C, a POSITA would have understood the Modified 3rd Embodiment to still use the timing chart of Figure 7. Furthermore, a POSITA would have understood Figure 7 to still provide the relevant timing diagram for the Modified 3rd Embodiment because when reset transistor 314 is connected to Node C it would still perform its function during T1 of resetting the voltage at Node A to "a little higher" than Vstd to ensure

the driving transistor 310 is in a conductive state, prior to the voltage compensation period in T2. EX1006, [0169]-[0175], [0209]-[0217]. Because Ri turns off 314 in every period except T1, the operation of the circuit is not impacted in any other time period, other than to achieve a reduction of leakage current at Node A as disclosed by Senda. An annotated Figure 7 is shown below adding annotations for time period T1 (time after t1), T2 (time after t2), T3 (time after t3) and T4 (time after t4). This annotated timing diagram will be used in the analysis below. EX1002, ¶¶166-171 (explaining the application of the timing in annotated Figure 7 to the Modified 3rd Embodiment).

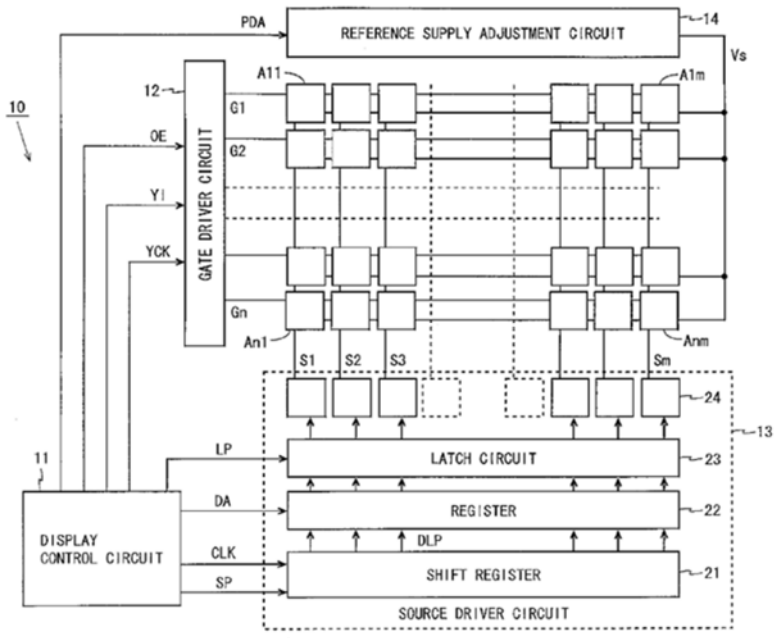


B. Claim 1

1. [1pre]

Senda discloses "An organic light emitting display, comprising (see following limitations)." EX1002, ¶172.

Fig. 1



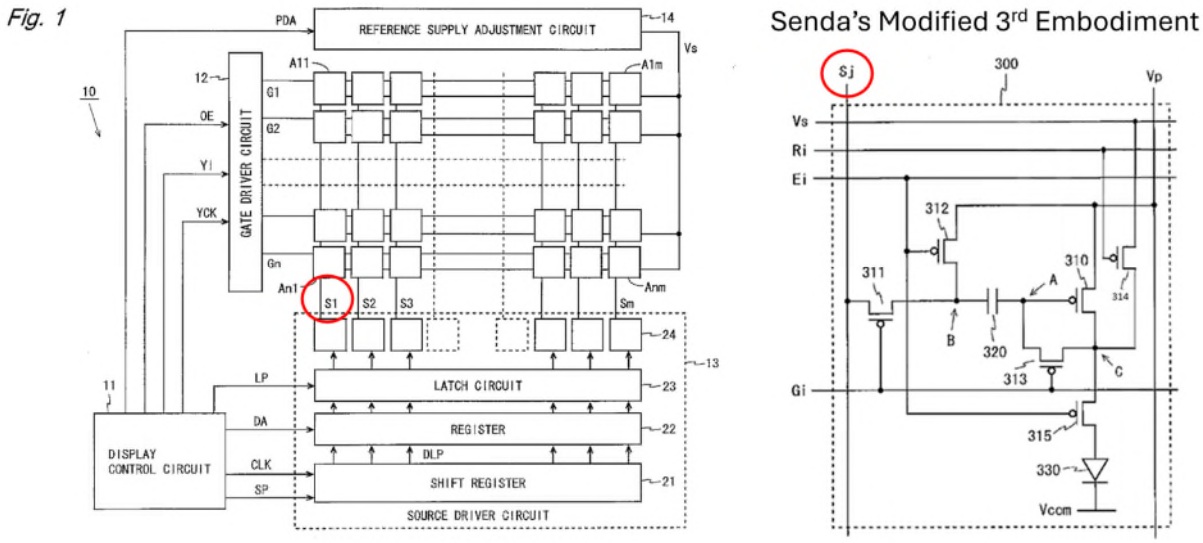
EX1006, Figs. 1-16, Abstract, [0001] (invention relates to a display device such as an organic EL display, [0117] ("130 … 330, and 730: organic EL element"), [0125] ("[a] display device according to each embodiment includes a pixel circuit … the pixel circuit includes an organic EL element"), [0135]-[0137], [0163], [0209]; EX1002, ¶173.

As discussed above, Senda discloses a Modified 3rd Embodiment, wherein Senda's third embodiment (Figs. 6-7, [0163]-[0174]) is modified as disclosed for the seventh embodiment (Fig. 15, [0209]-[0220]) to connect PMOS transistor 314 to Node C to reduce leakage at Node A. EX1006, [0218]-[0219], claims 1, 3, and 5. Senda discloses figure 1 and [0125]-[0134] apply to each of the first, third, and

seventh embodiments. *Id.*, [0125]-[0127]. Thus, Senda discloses all elements of the challenged claims, as arranged in the claims, as further explained for each limitation below. EX1002, ¶174.

2. [1a]

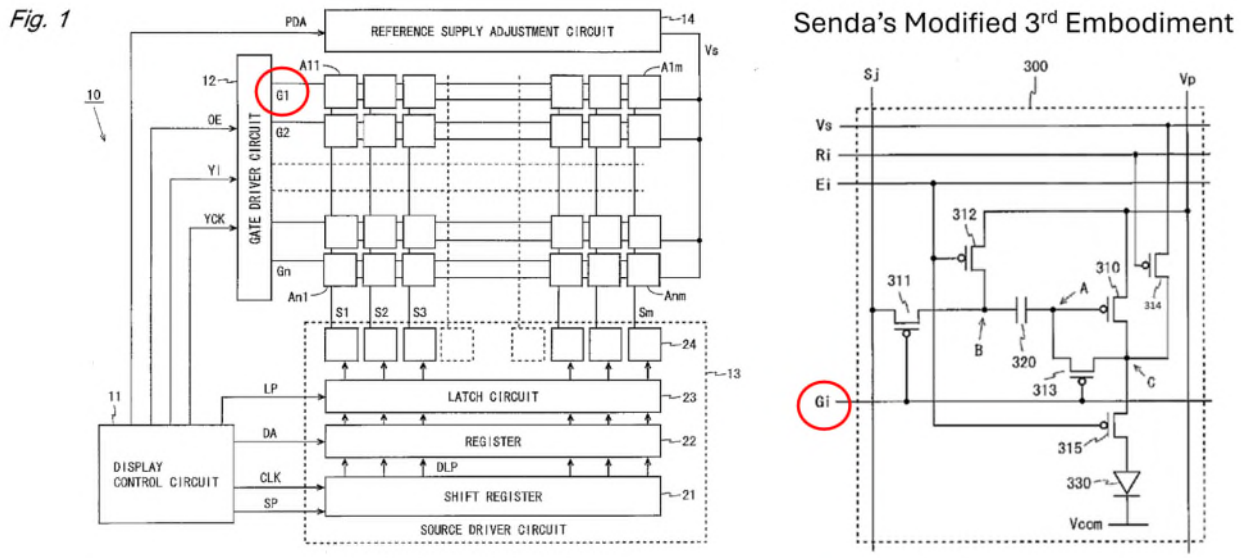
Senda discloses "a data line (Sj) for transmitting a data signal (Vdata)." EX1002, ¶175.



EX1006, Figs. 1 (annotated) (left), 6 (annotated and modified) (right) (data lines Sj are connected to the source driver circuit 13), 7 (data on Sj), [0128]-[0131] (circuit 13 functions as a display signal output circuit that provides potentials according to display data to the data lines Sj), [0124], [0163]-[0164], [0166] (data on Sj), [0169]-[0171] (Vdata on Sj); EX1002, ¶176.

3. [1b]

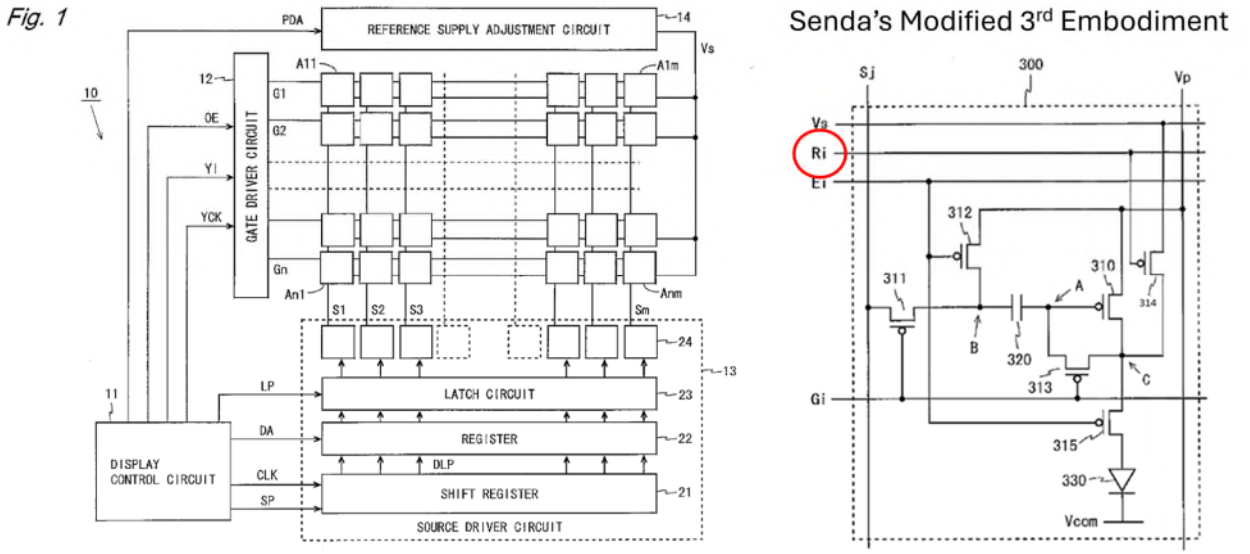
Senda discloses "a first scan line (Gi) for transmitting a first scan signal." EX1002, ¶177.



EX1006, Fig. 1 (annotated) (left) (a plurality of scanning lines Gi), 6 (annotated and modified) (right) (Gi), 7 (GL and GH on Gi), 15 (scanning line Gi), [0123] (Gi: scanning line), [0127]-[0128] (scanning lines Gi … are connected to the gate driver circuit 12), [0130] (gate driver circuit 12 functions as a scanning signal output circuit that selects a write-target pixel circuit using a corresponding scanning line Gi), [0136]-[0142], [0163]-[0172] (GL and GH on Gi), [0211]-[0212]; EX1002, ¶178.

4. [1c]

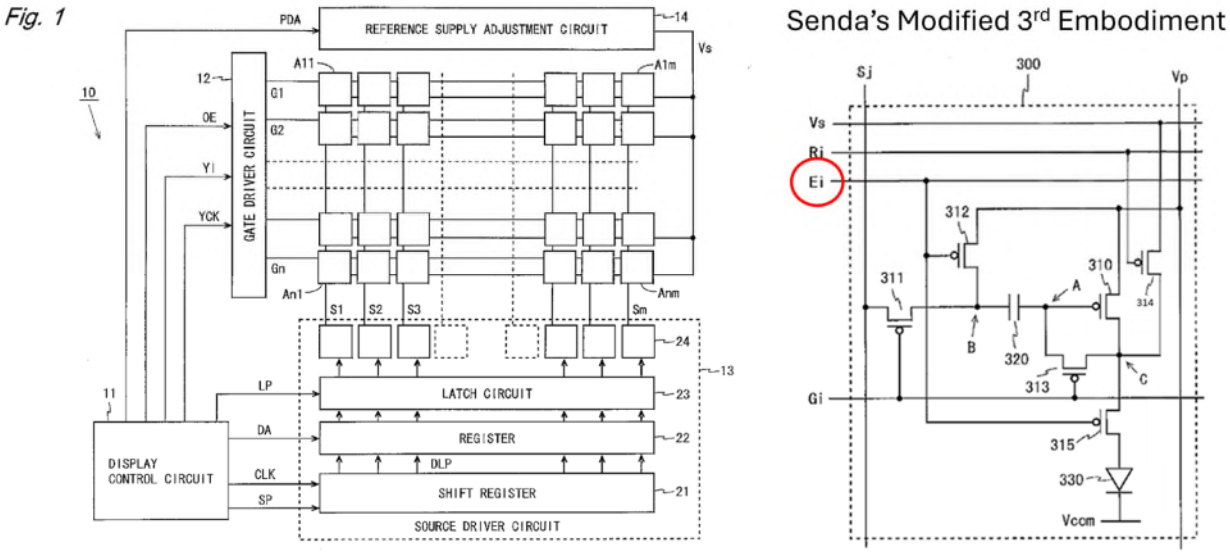
Senda discloses "a second scan line (Ri) for transmitting a second scan signal." EX1002, ¶179.



EX1006, Fig. 1, Fig. 6 (annotated and modified) (right) (Ri), 7 (GL and GH on Ri), 15 (Ri), [0122] (Wi, Ri, and Ei: control line), [0128] (scanning lines Gi and control lines Wi, Ri, etc. are connected to the gate driver circuit 12), [0130] (output from the logic operation corresponding control lines Wi, Ri, etc.), [0136], [0138]-[0140], [0143]-[0148], [0164]-[0174] (GL and GH on Ri control line), [0211]-[0218]; EX1002, ¶180.

5. [1d]

Senda discloses "a transmission line (Ei) for transmitting an emission signal." EX1002, ¶181.



EX1006, Figs. 1, 6 (annotated and modified) (right) (control line Ei), 7 (GL and GH on Ei), [0122] (Wi, Ri, and Ei: control line), [0164] ("[t]he potential of the control line Ei is controlled by the gate driver circuit 12"), [0165]-[0174] (GL and GH on Ei), [0211]-[0218]; EX1002, ¶182.

6. [1e]

Senda discloses "an input unit (311), electrically connected to the data line (Sj) and the first scan line (Gi), for outputting a preliminary control voltage (outputting preliminary control voltage to Node B) according to the data signal (data signal on Sj) and the first scan signal (first scan signal on Gi)." EX1002, ¶183.

Senda's Modified 3rd Embodiment

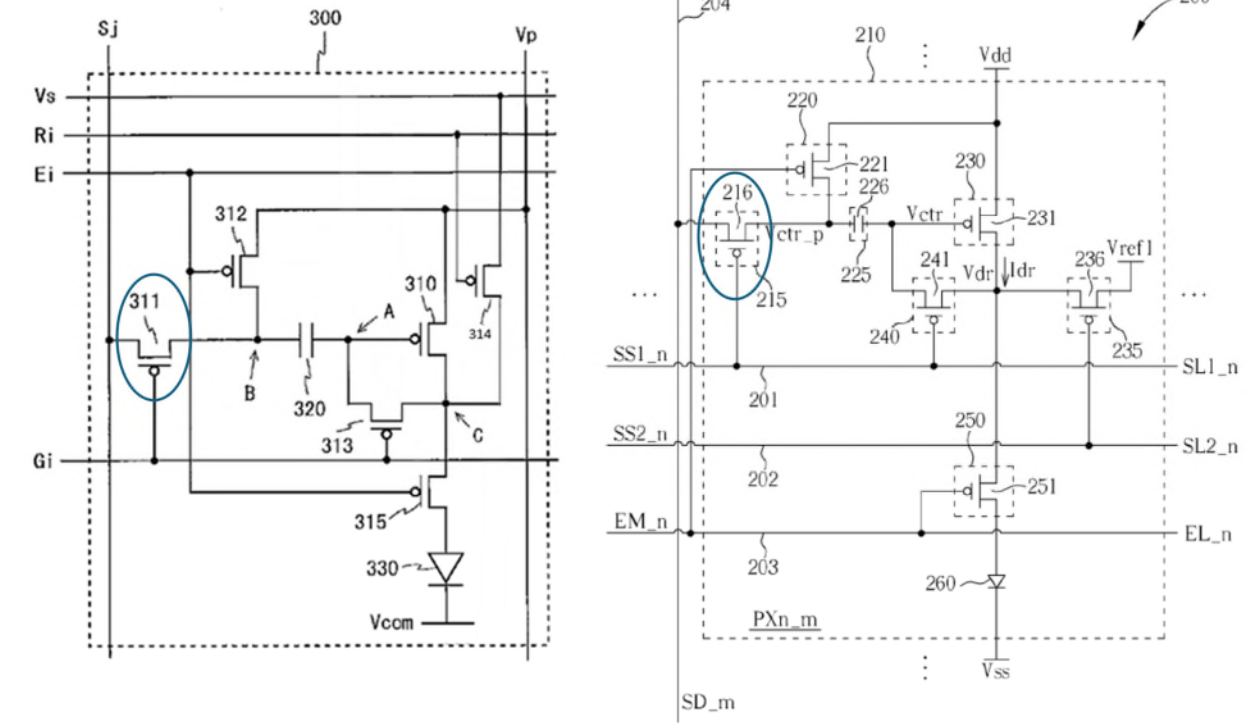


FIG. 2

Senda's Modified 3rd Embodiment (left) and 757 patent Figure 2 (right) are shown annotated above. Senda discloses 311 is a PMOS transistor with a gate coupled to Gi, a first electrode coupled to the data line Sj, and a second electrode coupled to Node B, such that during T1 and T2, 311 outputs a preliminary control voltage to the first Node B according to the data signal on Sj and the low level first scan signal on Gi. EX1006, Figs. 6-7 (showing Vdata on Sj and as output to Node B), [0135]-[0152], [0163]-[0164] (PMOS transistors, Gi, Sj), [0165]-[0175] (311 is turned on by GL on Gi such that it outputs Vdata to Node B from the data signal on Sj), [0169] ("B is connected to the data line Sj through the switching TFT 311, and thus, the potential at the connection point B is changed to Vdata"). The second

electrode of TFT 311 is electrically connected to the voltage adjustment unit (312) and couple unit (320) at Node B. *Id.* PMOS transistor 311 outputs Vdata to Node B after t1 and after t2 while GL is on Gi as shown in Figure 7. EX1002, ¶184.

Under 112f, Senda's PMOS transistor 311 as connected performs the claimed function and is identical to the corresponding structure for the input unit 215 (PMOS transistor 216 as connected). EX1001, Fig. 4, 4:34-38; EX1002, ¶185.

7. [1f]

Senda discloses "a voltage adjustment unit (312), electrically connected to the transmission line (Ei) and the input unit (311), for adjusting the preliminary control voltage (adjusting Vdata preliminarily stored at Node B) according to the emission signal (Ei) and a second reference voltage (VDD on Vp)." EX1002, ¶186.

Senda's Modified 3rd Embodiment

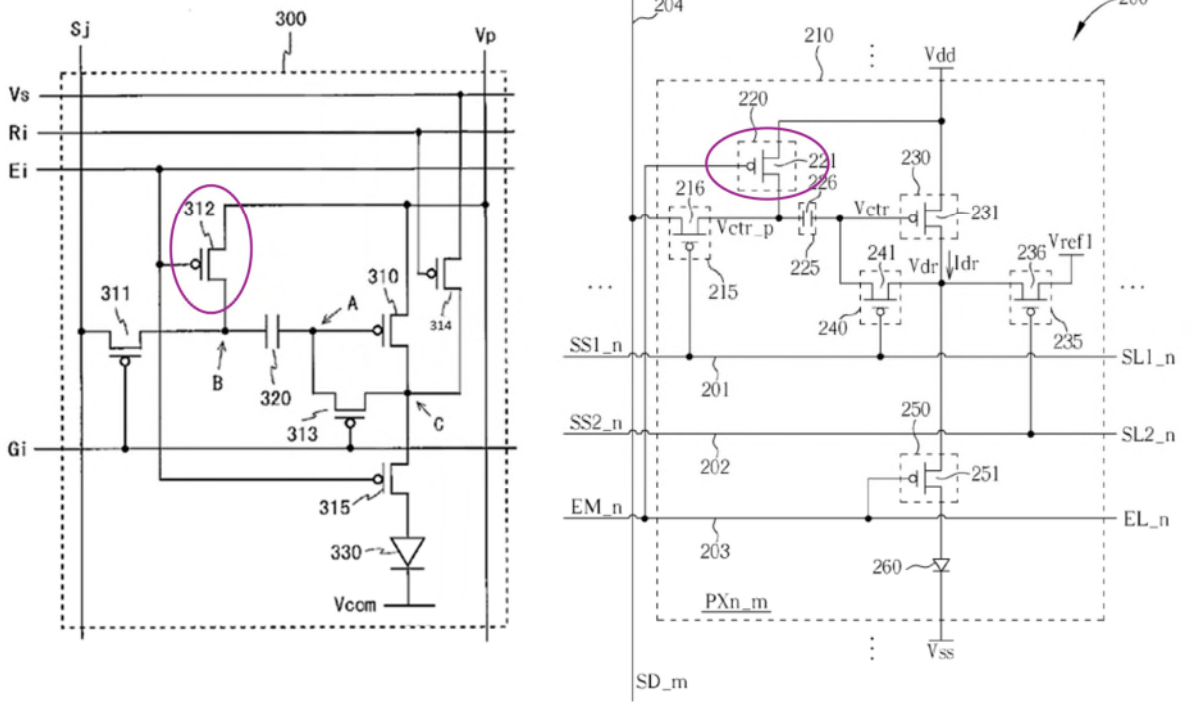


FIG. 2

Senda's Modified 3rd Embodiment (left) and 757 patent Figure 2 (right) are shown annotated above. Senda discloses 312 is a PMOS transistor with a gate coupled to Ei, a first electrode connected to 311 and 320 at Node B and a second electrode coupled to power supply wiring line Vp. EX1006, Figs. 6-7, [0163]-[0164] (connections for TFT 312). When 312 is turned on by a low emission control signal on Ei, 312 adjusts the preliminary control voltage Vdata at Node B to VDD. EX1006, Figs. 6-7 (after t4, showing adjustment of voltage at Node B from Vdata to Vdd), [0165]-[0174] (in T4, TFT 312 is switched on by low voltage on Ei, connecting Node B to power supply wiring line Vp to change voltage from

Vdata to VDD). TFT 312 is on during the light emitting period, after t4 in Figure 7. EX1002, ¶187.

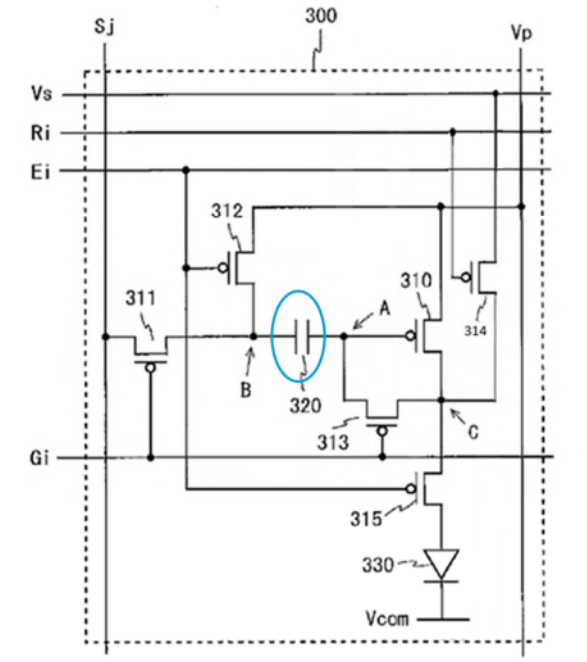
Under 112f, Senda's PMOS transistor 312 as connected performs the claimed function and is identical to the corresponding structure for the voltage adjustment unit 220 disclosed in the 757 patent (PMOS transistor 221 as connected). EX1001, Fig. 2 (connection to VDD), 6:36-42; EX1002, ¶188.

Note that the relevant corresponding structure in the 757 patent for this ground is the structure in Figure 2 (and dependent claim 13) where the voltage adjustment unit is connected to power supply voltage VDD as the second reference voltage. *See* Claim Construction [1f] above; EX1002, ¶189.

8. [1g]

Senda discloses "a couple unit (320), electrically connected to the input unit (311) and the voltage adjustment unit (312), for adjusting a control voltage (voltage at Node A) through coupling a change of the preliminary control voltage (capacitor 320 couples change in voltage at Node B to Node A)." EX1002, ¶190.

Senda's Modified 3rd Embodiment



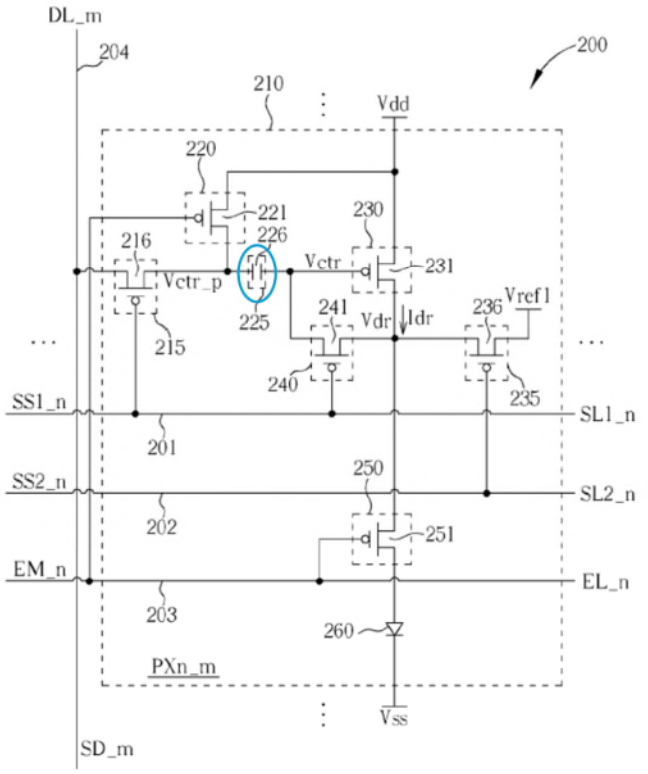


FIG. 2

Senda's Modified 3rd Embodiment (left) and 757 patent Figure 2 (right) are shown annotated above. Senda discloses storage capacitor 320 is coupled between Nodes A and B and, at time t3, is charged to the voltage difference between the preliminary control voltage Vdata on Node B and the voltage VDD+Vth on Node A. EX1006, Figs. 6-7, [0137], [0163]-[0164], [0169]-[0171] (charging of Nodes A and B), [0172] (at time t3 capacitor 320 holds the potential difference VDD+Vth-Vdata). After t4, when the preliminary control voltage on Node B is changed by 312 to VDD (potential of power supply line Vp), capacitor 320 couples that change in voltage to Node A. EX1006, Fig. 6-7 (showing after t4 the change in voltage at Node B and the corresponding change in voltage at Node A), [0163]-[0164]

(PMOS), [0173] ("the potential at the connection point B is changed from Vdata to VDD and accordingly the potential at the connection point A is changed by the same amount … and becomes (VDD+Vth+VB)."). The coupling of the change in voltage occurs after t4, during the light emission period in Figure 7. EX1002, ¶191.

Under 112f, Senda's capacitor 320 as connected performs the claimed function and is identical to the corresponding structure for the couple unit 225 in the 757 patent (capacitor 226 as connected). EX1001, Fig. 4, 4:42-44. EX1002, ¶192.

9. [1h]

Senda discloses "a driving unit (310), electrically connected to the couple unit (320), for providing a driving current and a driving voltage (current and voltage at second electrode of 310, Node C), according to the control voltage (voltage at Node A) and a first power voltage (VDD on Vp)." EX1002, ¶193.

Senda's Modified 3rd Embodiment

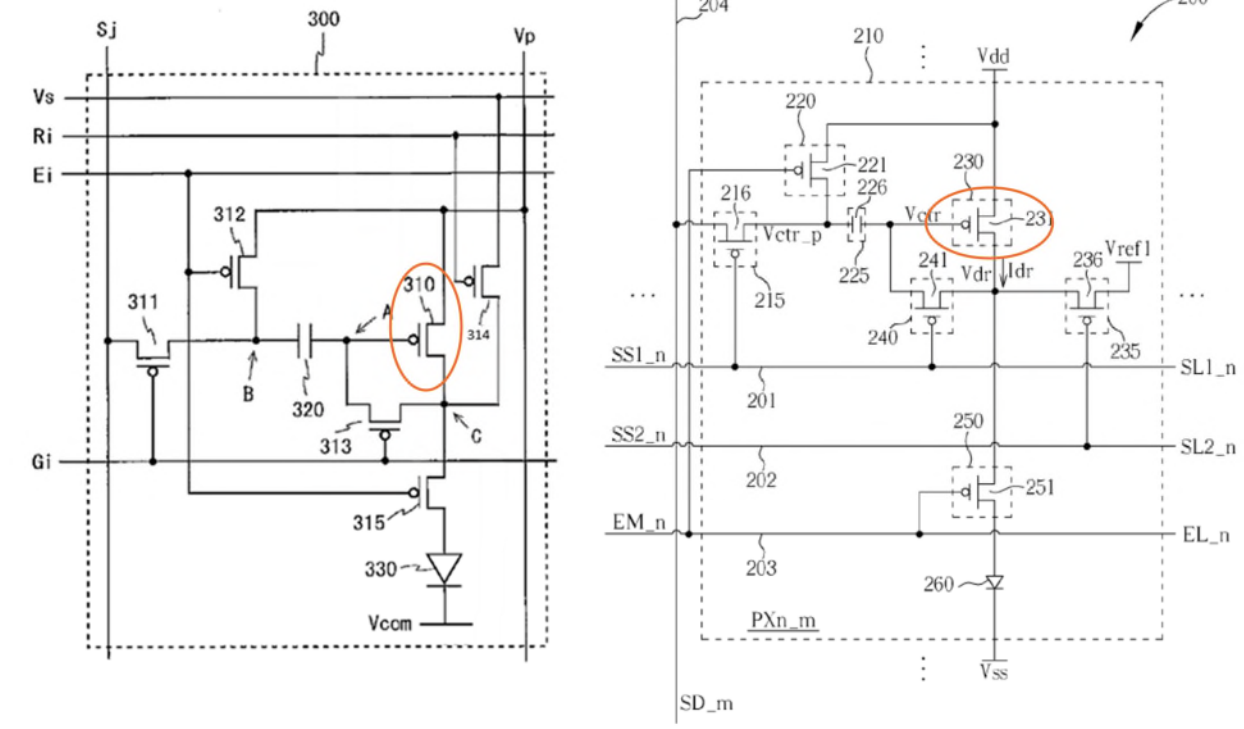


FIG. 2

Senda's Modified 3rd Embodiment (left) and 757 patent Figure 2 (right) are shown annotated above. Senda discloses 310 is a PMOS transistor with its gate terminal coupled to Node A (one electrode of capacitor 320), first electrode coupled to Vp providing VDD, and a second electrode coupled to Node C (313, 314, 315). After t4, when 310 is turned on by the control voltage at Node A and a low signal on Ei turns on 315, transistor 310 provides a driving current and driving voltage at its second electrode (Node C) to drive the organic EL element ("OLED") 330. EX1006, Figs. 6-7, [0163]-[0164] (PMOS), [0169]-[0174] (describing 310 driving after t4). Transistor 310 provides the driving current and driving voltage during the light emission period T4 in Figure 7. EX1002, ¶194.

Under 112f, Seanda's PMOS transistor 310 as connected performs the claimed function and is identical to the corresponding structure for the driving unit disclosed in the 757 patent (PMOS transistor 231 as connected). EX1001, Fig. 4, 4:38-41. EX1002, ¶195.

Senda explicitly discloses that 310 provides a current at its second electrode, Node C, to drive OLED 330. EX1006, Fig. 6-7, [0173]-[0174], [0210] (Node C). And Senda discloses that driving current provided by 310 is provided according to Vdd and the control voltage at Node A applied to the gate of 310. *Id.*; EX1002, ¶196.

Senda inherently discloses that 310 provides a "driving voltage." A POSITA would have known it was inherent from the electrical properties of Senda's pixel circuit 300 that TFT 310 is also providing a driving voltage with the driving current. To provide a driving current as disclosed in Senda, a POSITA would have known that there must be a driving voltage, i.e., a difference in potential between the second electrode of 310 at Node C and Vcom at the common cathode. EX1006, [0120], [0133]. A POSITA would have known that without that difference in potential, there would be no driving current as disclosed in Senda and the OLED 330 would not emit light. A POSITA would have known that the magnitude of the driving voltage provided by 310 at Node C would be Vdd minus the voltage drop across 310. EX1006, [0171]; EX1002, ¶197 (explaining diodes).

10. [1i]

Senda discloses "a first reset unit (314), electrically connected to the driving unit (310) at Node C and the second scan line (Ri), for resetting the driving voltage (voltage at Node C) according to the second scan signal (Ri) and a first reference voltage (Vstd on Vs)." EX1002, ¶198.

Senda's Modified 3rd Embodiment

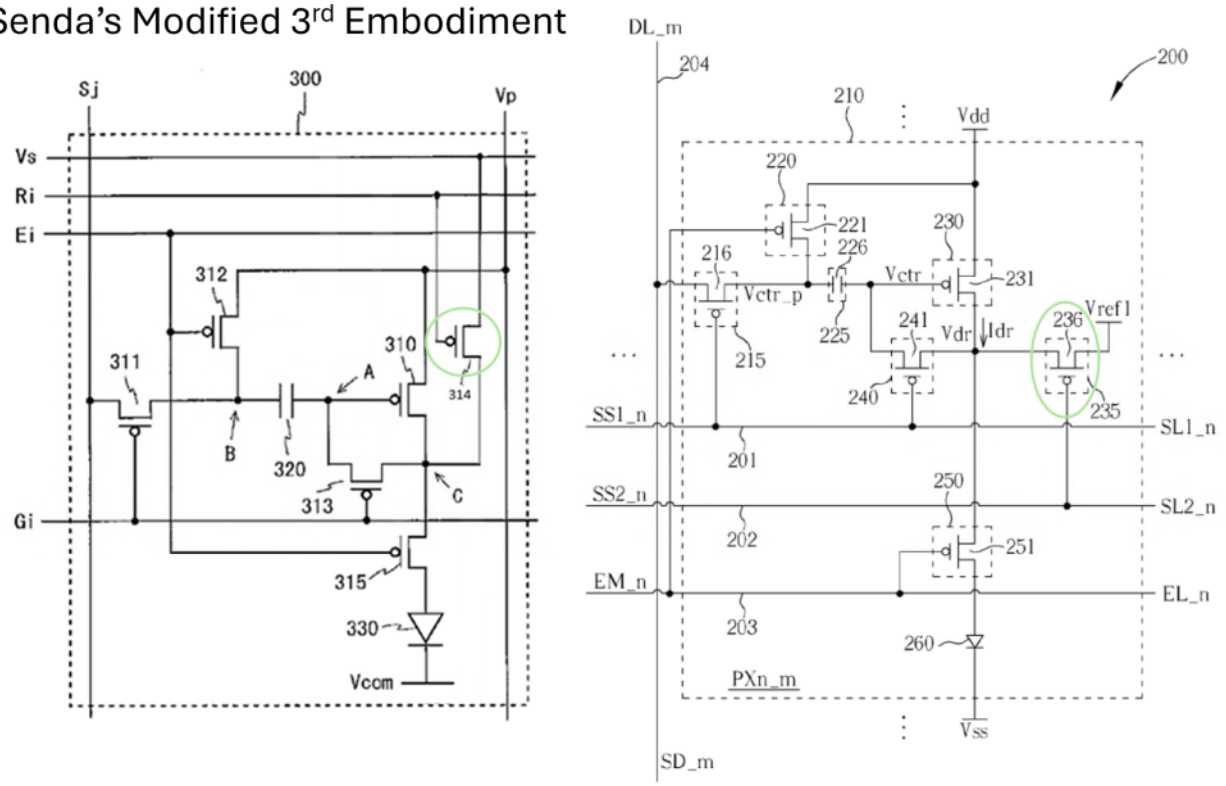


FIG. 2

Senda's Modified 3rd Embodiment (left) and 757 patent Figure 2 (right) are shown annotated above. Senda discloses transistor 314 is a PMOS transistor with a gate coupled to Ri, a first electrode coupled to transistor 310 at Node C, and a second electrode coupled to Vs, such that after t1 when 314 is turned on by the low second scan signal on Ri, the potential at Node C is reset

according to Vstd. EX1006, Figs. 6-7, [0163]-[0164] (PMOS), [0169]-[0170] (disclosing how during T1, TFT 314 is conductive), Fig. 15, [0210]-[0214], [0218]-[0219] (disclosing PMOS transistor 314 should be connected to Node C), claims 1 and 5 (claiming the modified third embodiment). As explained above, the Modified 3rd Embodiment discloses 314 will reset Node C according to the timing diagram in Figure 7 such as that when Ri is low, the driving voltage at Node C is rest according to Vstd. *See* Ground 3.A; EX1002, ¶199.

Under 112f, Senda's PMOS transistor 314 as connected performs the claimed function and is identical to the corresponding structure for the first reset unit disclosed in the 757 patent (PMOS transistor 236 as connected). EX1001, Fig. 4, 4:44-48; EX1002, ¶200.

Senda discloses transistor 314 is connected to Vstd on Vs while the corresponding structure 236 is connected to "Vref1," but this difference in naming convention is not relevant. Vstd on Vs in Senda is a reference voltage that is different from the second reference voltage VDD. EX1006, [0133] (Vstd is a "reference potential" that is adjustable and set by control signal PDA), [0155] (Vstd must be lower than VDD and is desirably close to VDD+Vth to ensure compensation for 310); EX1002, ¶201.

11. [1j]

Senda discloses "a second reset unit (313), electrically connected to the driving unit (310), the first reset unit (314), and the first scan line (Gi), for resetting the control voltage (voltage at Node A) according to the first scan signal (Gi) and the driving voltage (voltage at Node C)." EX1002, ¶202.

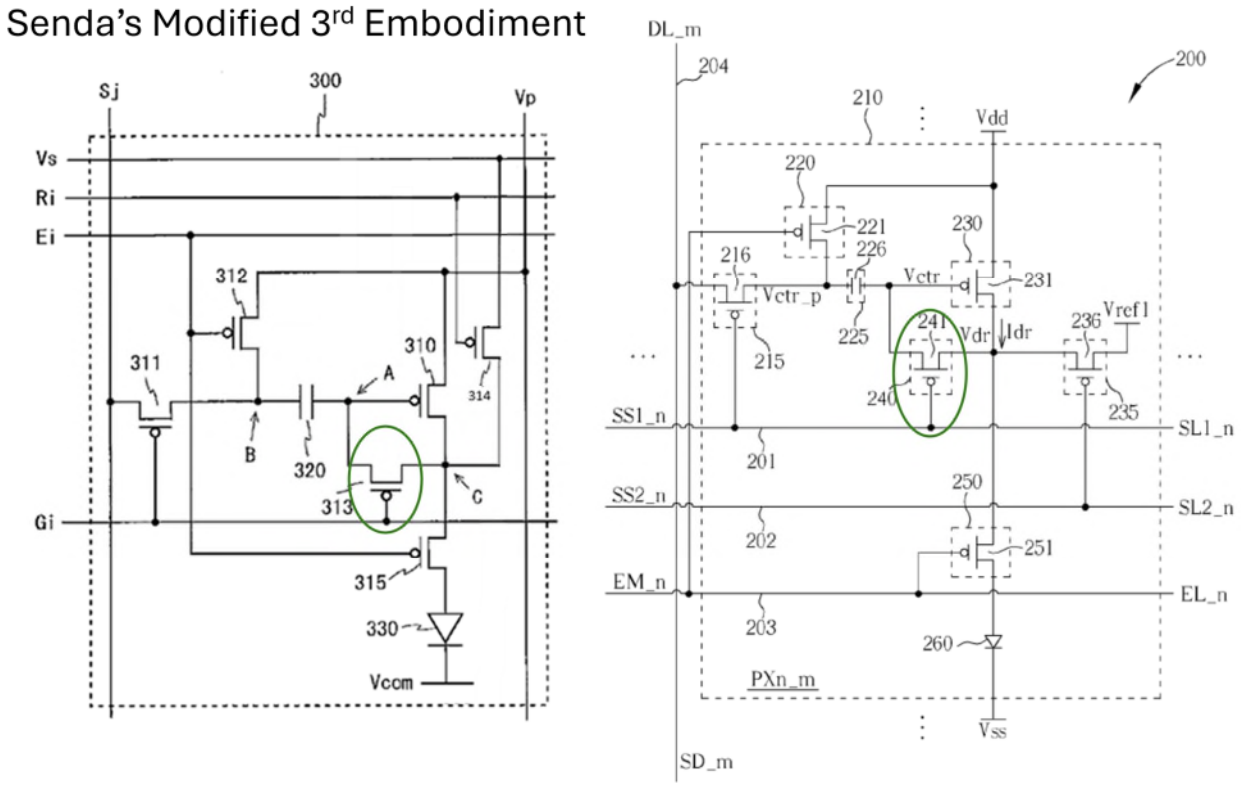


FIG. 2

Senda's Modified 3rd Embodiment (left) and 757 patent Figure 2 (right) are shown annotated above. Senda discloses 313 is a PMOS transistor with a gate coupled to Gi, a first electrode coupled to Node C (second electrode of 310, 314, and 315), and a second electrode coupled to Node A (the gate of 310 and an electrode of 320), such that when 313 is turned on by a low signal on Gi, the

driving voltage (voltage at Node C) is applied to reset the control voltage at Node A. EX1006, Figs. 6-7, [0163]-[0164], [0169]-[0172], [0211]-[0214]; EX1002, ¶203.

After t1 (during T1), the voltage at Node A is reset (to a little higher than Vstd) according to the low signal on Gi and the driving voltage at Node C. Specifically, low signals on Gi and Ri turn 313 and 314 on, such that the voltage on Node A is reset to Vstd plus alpha. EX1006, Figs. 6-7 (showing after t1, Node A at Vstd plus alpha), [0163]-[0164] (PMOS), [0169]-[0172], [0211]-[0214] (resetting voltage at Node A through 713 and 714); EX1002, ¶199 (explaining a little higher than Vstd); EX1002, ¶204.

After t2 (during T2), the voltage at Node A is reset (to VDD+Vth) according to the low signal on Gi and the driving voltage at Node C. Specifically, a low signal on Gi is still supplied keeping 313 on, but a high signal on Ri causes 314 to turn off, such that the voltage on Node A is reset to VDD+Vth. EX1006, Figs. 6-7 (showing after t2, Node A reaches VDD+Vth, and that Vth is a negative value), [0163]-[0164], [0169]-[0171]. Senda discloses that after t2, 310 operates in a conduction state until Node A reaches VDD+Vth, at which point 310 goes into a threshold state. *Id.*, [0171]. Senda discloses this reset is performed to compensate for the threshold voltage of 310. *Id.*, [0174]; EX1002, ¶205.

Senda's disclosure in this regard is identical to the disclosure of the 757 patent wherein during T1, Vctrl is reset to Vref1 through 236 and 241, and during T2, Vctrl is reset to VDD-|Vth| through 241. EX1001, Fig. 3, 5:15-22 (T1), 5:23-38 (T2). Senda discloses Vth is a negative value (EX1006, [0171]), so Senda's VDD+Vth is the same as the 757 patent's VDD-|Vth|. EX1002, ¶206.

Under 112f, Senda's PMOS transistor 313 as connected performs the claimed function and is identical to the corresponding structure for the second reset unit disclosed in the 757 patent (PMOS transistor 241 as connected). EX1001, Fig. 4, 4:48-52. EX1002, ¶207.

12. [1k]

Senda discloses "an organic light emitting diode (330) for generating output light according to the driving current." EX1002, ¶208.

Senda's Modified 3rd Embodiment

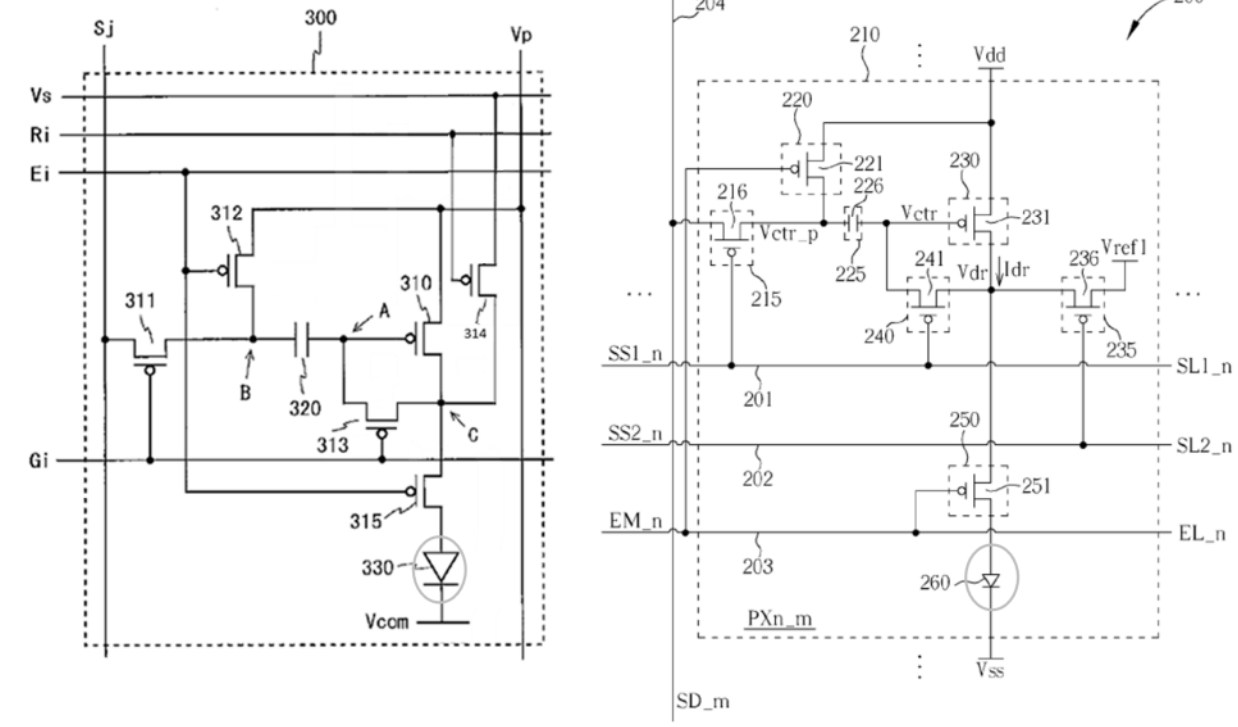


FIG. 2

Senda's Modified 3rd Embodiment (left) and 757 patent Figure 2 (right) are shown annotated above. Senda discloses that the OLED 330 is driven by the driving current provided by 310 to generate output light. EX1006, Fig. 6-7, [0117], [0163]-[0164], [0174] (disclosing the current through 310 drives the OLED to emit light). The amount of control voltage at Node A on the gate of 310 determines the amount of driving current 310 provides and, therefore, the brightness of the OLED. *Id*. EX1002, ¶209.

13. [1l]

Senda discloses "an emission enable unit (315), electrically connected to the transmission line (Ei), the driving unit (310), and the organic light emitting diode

(330), for providing a control of furnishing the driving current to the organic light emitting diode according to the emission signal (GL and GH on Ei)." EX1002, ¶210.

Senda's Modified 3rd Embodiment

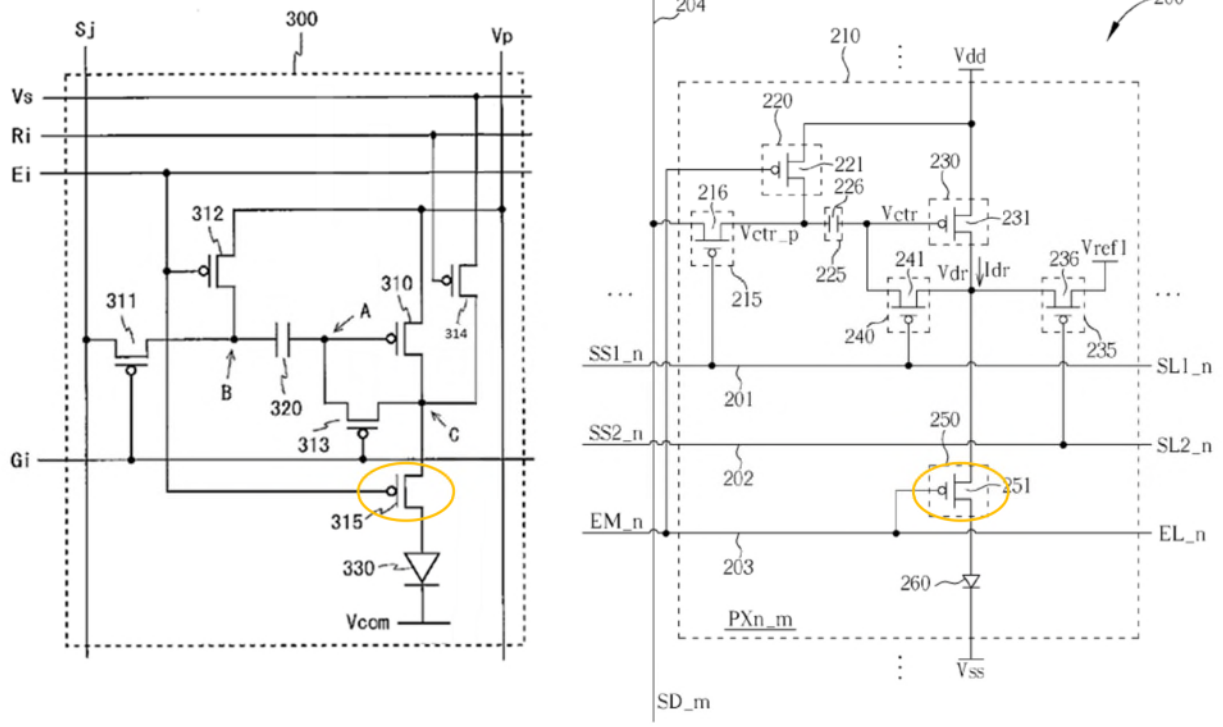


FIG. 2

Senda's Modified 3rd Embodiment (left) and 757 patent Figure 2 (right) are shown annotated above. Senda discloses 315 is a PMOS transistor with a gate coupled to Ei, a first electrode coupled to the second electrode of 310 at Node C and a second electrode coupled to OLED 330, such that when 315 is turned on by a low emission control signal on Ei, the driving current from the second electrode of 310 is applied to OLED 330. EX1006, Fig. 6-7, [0117], [0163]-[0164], [0174]; EX1002, ¶211.

Under 112f, Senda's PMOS transistor 315 as connected performs the claimed function and is identical to the corresponding structure for the second reset unit disclosed in the 757 patent (PMOS transistor 251 as connected). EX1001, Fig. 4, 4:54-58. EX1002, ¶212.

C. Claim 2:

Senda discloses claim 1 "wherein the input unit (311) comprises a first transistor (311), the first transistor having a first end (first electrode) electrically connected to the data line (Si), a gate end electrically connected to the first scan line (Gi), and a second end (second electrode connected to Node B) electrically connected to the voltage adjustment unit (312) and the couple unit (320)." *See* [1e]. EX1002, ¶213.

D. Claim 3:

Senda discloses claim 2, "wherein the first transistor (311) comprises a thin film transistor (TFT) or a field effect transistor (PMOS)." Senda discloses transistors 310-315, 714 are thin film transistors. EX1006, [0004] ("TFTs (Thin Film Transistors)"), [0163]-[0164] ("TFT"), [0135]-[0138], [0209] (TFT), claim 14 ("thin-film transistors"). EX1002, ¶214.

E. Claim 4:

Senda discloses claim 1, "wherein the driving unit (310) comprises a second transistor (310), the second transistor (310) having a first end (first electrode) for receiving the first power voltage (VDD on Vp), a gate end for receiving the control

voltage (voltage on Node A), and a second end (second electrode) for outputting the driving current and the driving voltage. *See* [1h]. EX1002, ¶215.

F. Claim 5:

See Claim 3, 4. EX1002, ¶216.

G. Claim 6:

Senda discloses claim 1 "wherein the couple unit (320) comprises a capacitor (320) electrically connected between the input unit (311) and the driving unit (310). *See* [1g]. EX1002, ¶217.

H. Claim 7:

Senda discloses claim 1 "wherein the first reset unit (314) comprises a third transistor (314), the third transistor having a first end (connected to Vs) for receiving the first reference voltage (Vstd on Vs), a gate end electrically connected to the second scan line (Ri), and a second end (connected to Node C) electrically connected to the drive unit (310), the second reset unit (313) and the emission enable unit (315)." *See* [1i], [1j]-[1l]; EX1002, ¶218.

I. Claim 8:

See Claim 3, 7. EX1002, ¶219.

J. Claim 9:

Senda discloses claim 1 "wherein the second reset unit (313) comprises a fourth transistor (313), the fourth transistor having a first end (connected at Node C) electrically connected to the driving unit (310), the first reset unit (314) and the

emission enable unit (315), a gate end electrically connected to the first scan line (Gi), and a second end (connected to Node A) electrically connected to the couple unit (320) and the driving unit (310). *See* [1j], [1h]-[1l], 7. EX1002, ¶220.

K. Claim 10:

See Claim 3, 9. EX1002, ¶221.

L. Claim 11:

Senda discloses claim 1 "wherein the voltage adjustment unit (312) comprises a fifth transistor (312), the fifth transistor having a first end for receiving the second reference voltage (VDD on Vp), a gate end electrically connected to the transmission line (Ei), and a second end electrically connected to the input unit (311) and the couple unit (320)." *See* [f], [1e]-[1g]. EX1002, ¶222.

M. Claim 12:

See Claim 3, 11. EX1002, ¶223.

N. Claim 13:

Senda discloses "the organic light emitting display of claim 11, wherein the second reference voltage (VDD on Vp) is the first power voltage (VDD on Vp)." *See* [1f], [1h], 4, 11; EX1002, ¶224.

O. Claim 14:

Senda discloses claim 1 "wherein the emission enable unit (315) comprises a sixth transistor (315), the sixth transistor having a first end (at Node C) electrically connected to the driving unit (310), the first reset unit (314) and the second reset

unit (313), a gate end electrically connected to the transmission line (Ei), and a second end electrically connected to the organic light emitting diode (330). *See* [1l], [1e], [1h], 7, 9. EX1002, ¶225.

P. Claim 15:

See Claim 3, 14. EX1002, ¶226.

Q. Claim 16:

Senda discloses claim 1 "wherein the organic light emitting diode (330) comprises an anode electrically connected to the emission enable unit (315) and a cathode for receiving a second power voltage (Vcom)." *See* [1k]; EX1006, Figs. 1, 6 (illustrating diode with anode (base of triangle) connected to 315 and cathode (line at tip of triangle) connected to Vcom), [0120] ("Vcom: COMMON CATHODE"), [0133] ("a common cathode Vcom (or a cathode wiring line CAi)"), [0135]-[0137] (disclosing one end of OLED connected to common cathode Vcom and other end (anode) connected to 315 and eventually to VDD), [0163]-[0164]; EX1002, ¶227 (explaining meaning of diode symbol to POSITA and how disclosure that one electrode is a cathode means the other electrode must be the anode).

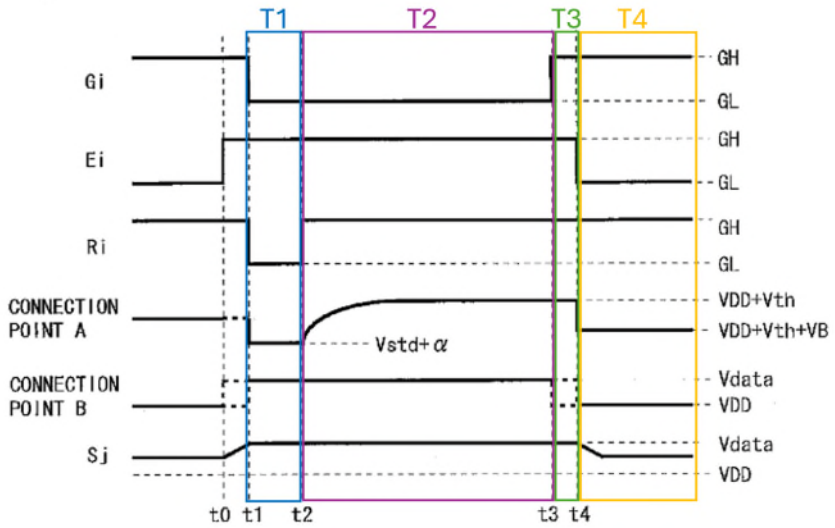
R. Claim 17:

1. [17pre]

Senda discloses "a driving method (Fig. 7), comprising." EX1006, Figs. 6-7, [0034], [0052]; [17pre]-[17u]. The timing diagram in combination with the pixel

structure discloses a driving scheme for an organic EL display. EX1006, [0003]-[0007]. Senda's Modified 3rd Embodiment uses the timing diagram in Figure. 7. *See supra* Ground 3.A (explaining Senda's Modified 3rd Embodiment and the timing of Figure 7). EX1002, ¶228.

Fig. 7



1. [17a]

Senda discloses "outputting a preliminary control voltage (outputting Vdata to Node B) by an input unit (311) according to a data signal (Vdata signal on Sj) and a first scan signal (GL/GH on Gi)." *See* [1e]; EX1002, ¶229.

2. [17b]

Senda discloses "adjusting the preliminary control voltage (changing voltage on Node B from Vdata to VDD) by a voltage adjustment unit (312) according to an emission signal (GL/GH on Ei) and a second reference voltage (VDD on Vp)." *See* [1f]; EX1002, ¶230.

3. [17c]

Senda discloses "adjusting a control voltage (voltage on Node A) by a couple unit (320) through coupling a change of the preliminary control voltage (capacitor 320 couples change in voltage at Node B to Node A)." *See* [1g]; EX1002, ¶231.

4. [17d]

Senda discloses "providing a driving current and a driving voltage (current and voltage at second electrode of 310, Node C) by a driving unit (310) according to the control voltage (voltage on Node A) and a power voltage (VDD on Vp)." *See* [1h]; EX1002, ¶232.

5. [17e]

Senda discloses "resetting the driving voltage (voltage on Node C) by a first reset unit (314) according to a second scan signal (GL/GH on Ri) and a first reference voltage (Vstd on Vs)." *See* [1i], 13; EX1002, ¶233.

6. [17f]

Senda discloses "resetting the control voltage (voltage on Node A) by a second reset unit (313) according to the first scan signal (GL/GH on Gi) and the driving voltage (voltage on Node C)." *See* [1j]; EX1002, ¶234.

7. [17g]

Senda discloses "generating output light by an organic light emitting diode (330) according to the driving current (current output from 310)." *See* [1k]; EX1002, ¶235.

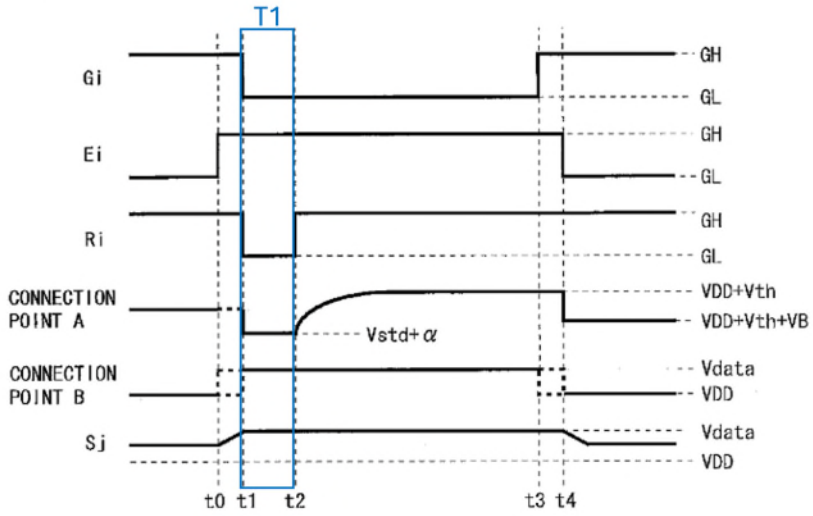
8. [17h]

Senda discloses "providing a control of furnishing the driving current to the organic light emitting diode (330) by an emission enable unit (315) according to the emission signal (GL/GH on Ei)." *See* [1l]; EX1002, ¶236.

9. [17i]

Senda discloses "providing the first scan signal (GL/GH on Gi) with a first level (GL) to the input unit (311) and the second reset unit (313), providing the second scan signal (GL/GH on Ri) with the first level (GL) to the first reset unit (314), providing the emission signal (GL/GH on Ei) with a second level (GH) different from the first level (GL) for disabling a voltage adjusting operation of the voltage adjustment unit (312) and disabling a current furnishing operation of the emission enable unit (315), and providing the data signal (Vdata on Sj) to the input unit (311) during a first interval (T1)." *See* [1e]-[1f], [1i]-[1j], [1l]; EX1006, Fig. 7 (at T1 showing Gi low, Ri low and Ei high), [0167]-[0170] (explaining that in T1 low signals on Gi and Ri turn on PMOS transistors 311, 313, 314 and high signal on Ei turns off PMOS transistors 312 and 315); EX1002, ¶237.

Fig. 7



10. [17j]

Senda discloses "outputting the preliminary control voltage (Vdata) by the input unit (311) according to the data signal (Vdata on Sj) and the first scan signal (GL/GH on Gi) during the first interval (T1)." *See* [1e] (311), [17a] (same), [17i] (T1); EX1002, ¶238.

11. [17k]

Senda discloses "resetting the driving voltage (voltage on Node C) by the first reset unit (314) according to the second scan signal (GL/GH on Ri) and the first reference voltage (Vstd on Vs) during the first interval (T1)." *See* [1i] (314), [17e] (same), [17i] (T1); EX1002, ¶239.

12. [17l]

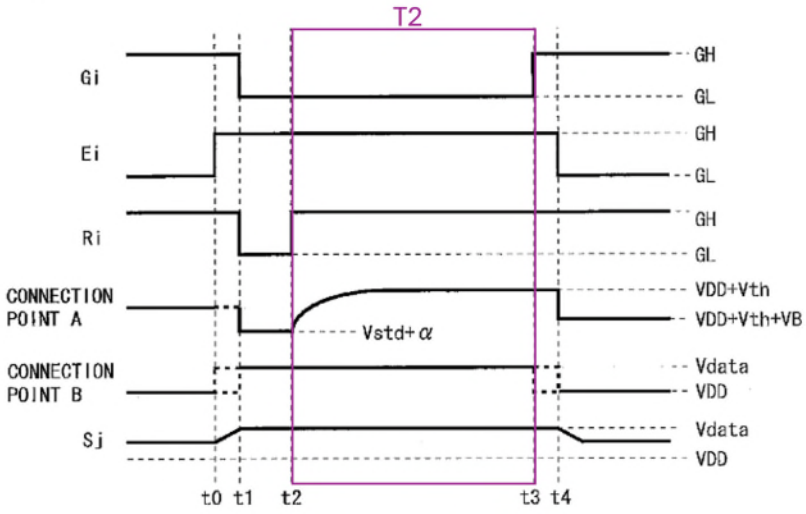
Senda discloses "resetting the control voltage (voltage on Node A) by the second reset unit (313) according to the first scan signal (GL/GH on Gi) and the

driving voltage (voltage on Node C) during the first interval (T1)." *See* [1j] (313), [17f] (same), [17i] (T1); EX1002, ¶240.

13. [17m]

Senda discloses "switching the second scan signal (GL/GH on Ri) from the first level (GL) to the second level (GH) for disabling a resetting operation of the first reset unit (314) during a second interval (T2) following the first interval (T1)." *See* [1i], EX1006, Fig. 7 (T2), [0171] (explaining after t2, Ri goes high turning off transistor 314); EX1002, ¶241.

Fig. 7



14. [17n]

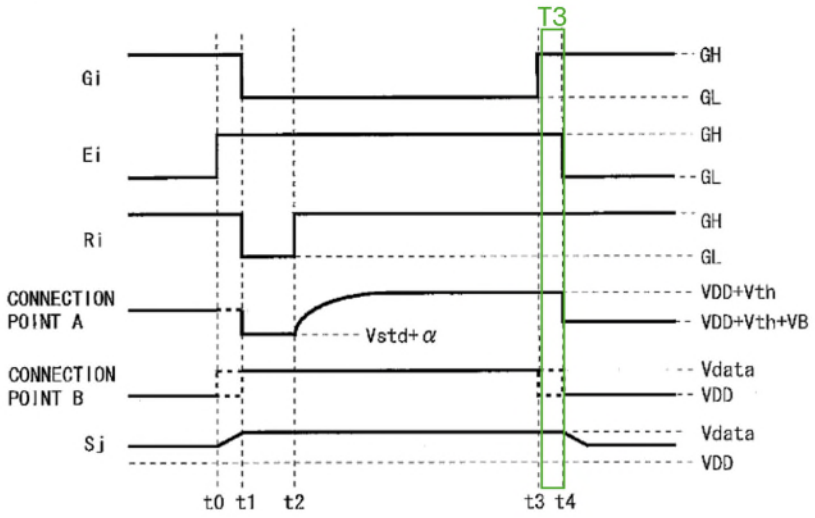
Senda discloses "performing a threshold voltage compensation operation on the control voltage (voltage on Node A) by the second reset unit (313) and the driving unit (310) according to the first scan signal (GL/GH on Gi) and the power

voltage (VDD on Vp) during the second interval (T2)." *See* [1j], (explaining threshold voltage compensation after t2), [17m]; EX1002, ¶242.

15. [17o]

Senda discloses "switching the first scan signal (GL/GH on Gi) from the first level (GL) to the second level (GH) for disabling a resetting operation of the second reset unit (313) and disabling an inputting operation of the input unit (311) during a third interval (T3) following the second interval (T2)." EX1006, Fig. 7, [0172] (explaining that after t3, Gi goes high turning off transistors 311 and 313); EX1002, ¶243.

Fig. 7

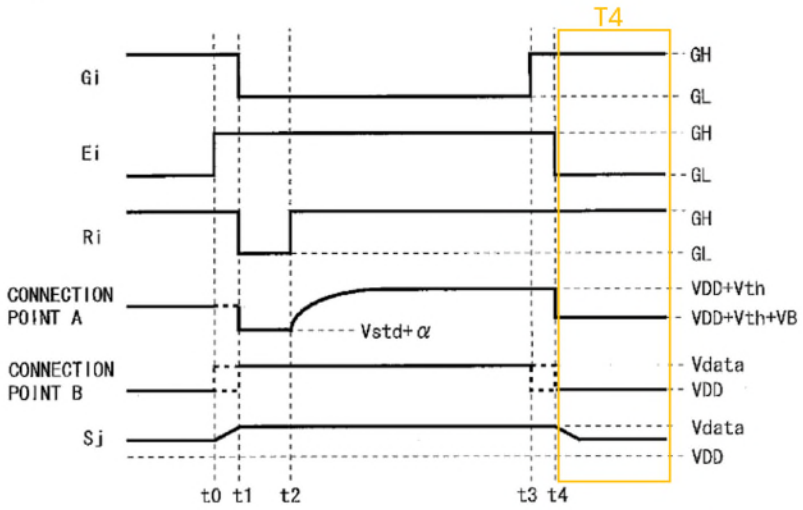


16. [17p]

Senda discloses "switching the emission signal (GL/GH on Ei) from the second level (GH) to the first level (GL) during a fourth interval (T4) following the

third interval (T3)." *See* [1l]; EX1006, Fig. 7, [0173]-[0174] (explaining after t4, Ei goes low); EX1002, ¶244.

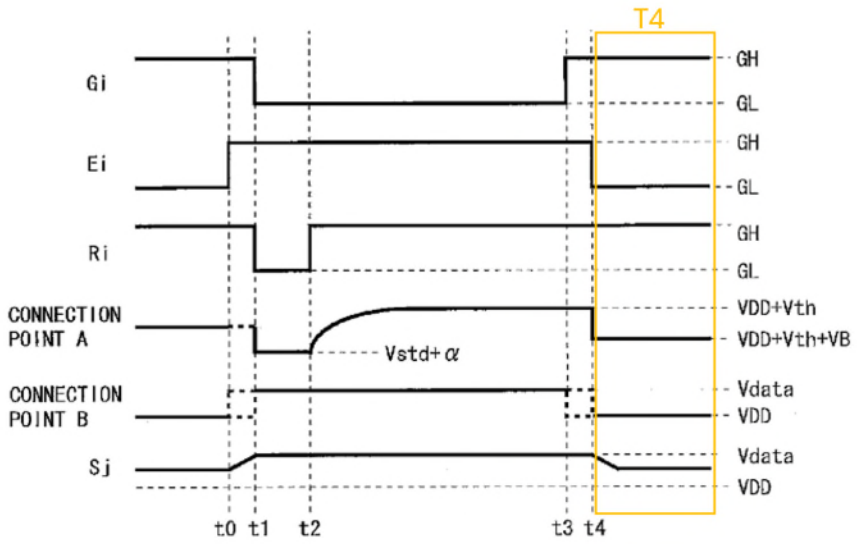
Fig. 7



17. [17q]

Senda discloses "adjusting the preliminary control voltage (voltage on Node B) by the voltage adjustment unit (312) according to the emission signal (GL/GH on Ei) and the second reference voltage (VDD on Vp) during the fourth interval (T4)." *See* [1f] (312), [17b] (same); EX1006, Fig. 7 (showing adjustment of voltage on Node B from Vdata to VDD after t4), [0173]-[0174] (explaining adjustment occurs after t4); EX1002, ¶245.

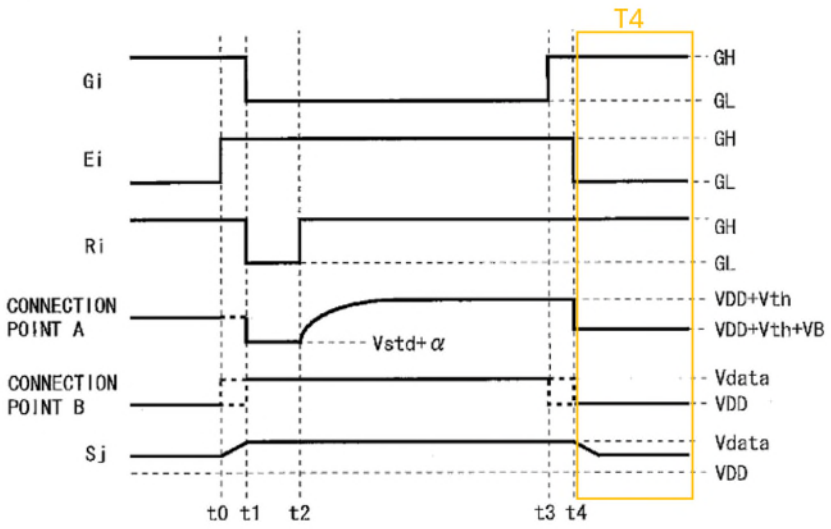
Fig. 7



18. [17r]

Senda discloses "adjusting the control voltage (voltage on Node A) by the couple unit (320) through coupling a change of the preliminary control voltage (voltage on Node B) during the fourth interval (T4)." *See* [1g] (320), [17c] (same); EX1006, Figs. 7 (showing coupled change in voltage on Node A after t4), [0019], [0172]-[0174] (after t4, adjusting the voltage on Node A from VDD+Vth to VDD+Vth+VB, by coupling the change of voltage at Node B from Vdata to VDD where VB=VDD-Vdata); EX1002, ¶246.

Fig. 7



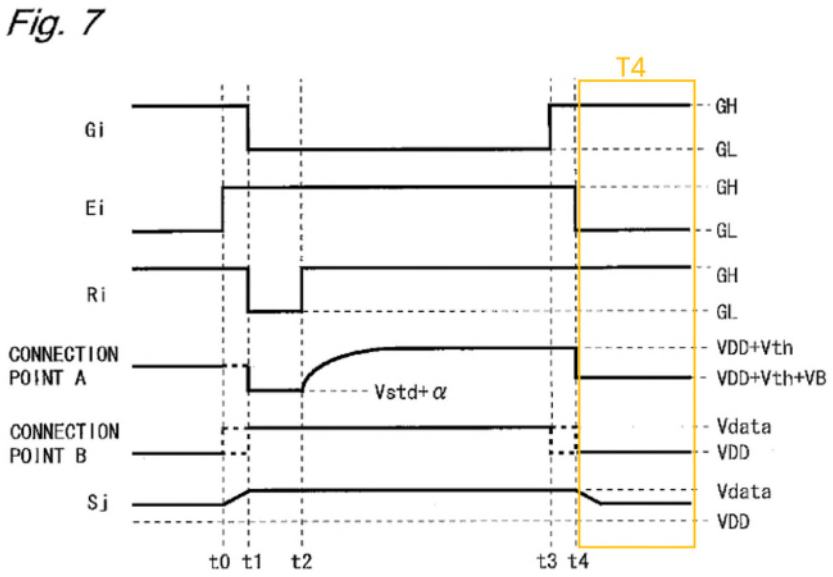
19. [17s]

Senda discloses "providing the driving current (current provided on second electrode of transistor 310 at Node C) by the driving unit (310) according to the control voltage (Node A) and the power voltage (VDD on Vp) during the fourth interval (T4)." *See* [1h] (310), [17d]; EX1006, Fig. 7, [0173]-[0175] (after t4 the current provided by TFT 310 corresponds to the voltage on Node A such that a current of an amount according to the data potential Vdata flows through to the OLED 330); EX1002, ¶247.

20. [17t]

Senda discloses "furnishing the driving current to the organic light emitting diode (330) by the emission enable unit (315) according to the emission signal (GL/GH on Ei) during the fourth interval (T4)." *See* [1l] (315), [17e]; EX1006,

Fig. 7, [0173]-[0175] (after t4, Ei goes low (GL) such that driving current from 310 flows through 315 to the OLED 330); EX1002, ¶248.



21. [17u]

Senda discloses "generating output light by the organic light emitting diode (330) according to the driving current during the fourth interval (T4)." *See* [1k] (330), [17g] (same); EX1006, Fig. 7, [0173]-[0175] (after t4, OLED 330 generates output light according to the drive current); EX1002, ¶249.

S. Claim 18:

Senda discloses the method of claim 17, "wherein the second level (GH) is greater than the first level (GL)." *See* [17i]; EX1002, ¶250.

T. Claim 19:

Senda discloses the method of claim 17, "wherein the first level is greater than the second level." EX1002, ¶¶ __. Claim 19 reverses the voltage levels of the

scan lines relative to claim 18. Senda discloses its modified third embodiment uses the levels as claimed for claim 18 as shown above. *See* [17i] (PMOS with second level (high-turn off (GH)) voltage which is greater than the first level (low-turn on (GL)) voltage)); EX1002, ¶251.

Senda discloses the voltage levels can be reversed as claimed by claim 19. Senda discloses its PMOS transistors, which are turned on by low gate voltages and off by high gate voltages, can instead be NMOS transistors, which are turned on by high gate voltages and off by low gate voltages. EX1006, Figs. 2-3, [0134] (p-channel or n-channel), [0135], [0163]-[0164] (first embodiment uses NMOS, which can be PMOS as shown for third embodiment as long as signals are adjusted), [0175] (third embodiment can use first embodiment transistors as long as signals are adjusted). A POSITA would have been familiar with PMOS and NMOS transistors and known they were turned on and off by opposite gate voltages. Thus, Senda discloses to a POSITA that its PMOS embodiment can be implemented as an NMOS embodiment using the opposite gate voltages. EX1002, ¶252.

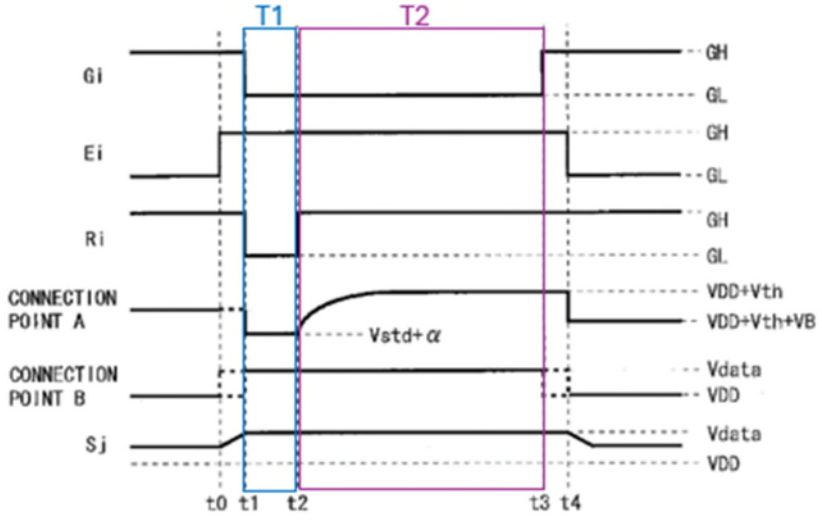
U. Claim 20

Senda discloses "the driving method of claim 17, wherein the second reference voltage (VDD on Vp) is the power voltage (VDD on Vp)." *See* [1f], 13, claim 17. EX1002, ¶253.

V. Claim 21

Senda discloses "the driving method of claim 17, wherein a length of the second interval (T2) is greater than a length of the first interval (T1)." *See* claim [17i]-[17l] (T1), [17m]-[17n] (T2); EX1002, ¶254.

Fig. 7



As shown in annotated Figure 7 of Senda above, Senda clearly discloses to a POSITA that T2 (the period after t2) is greater than the length of T1 (the period after t1); EX1002, ¶255.

VIII. GROUND 4: CLAIMS 1-21 ARE OBVIOUS OVER SENDA

A. Claims 1-21

As shown in Ground 3, Senda discloses that embodiment 3 should be modified as taught by embodiment 7 to connect transistor 314 to Node C as shown for transistor 714, such that the disclosures of Senda as a whole anticipate the claims. To the extent the Board disagrees and finds that Senda's disclosures do not

amount to anticipation, it would have been obvious to a POSITA to modify the third embodiment as taught by Senda in the seventh embodiment, rendering the claims obvious. EX1002, ¶256.

A POSITA would have been motivated by the express teachings of Senda to connect the first reset unit 314 of the third embodiment to Node C instead of Node A. Senda teaches that reducing the number of TFTs connected to Node A from two (as taught in embodiment five) to one (as taught in embodiment 7) is desirable to reduce leakage current at Node A and reduce fluctuations in the charge held by the capacitor. This will reduce fluctuations in the gate terminal potential of the driving TFT and enhance display quality. EX1006, [0218]-[0219]. Senda explicitly teaches this improvement is relevant to embodiment three which, like embodiment five, has two TFTs connected to Node A. *Id.*, Figs. 6, 13 [0219] ("the same change may be made to the pixel circuits according to the first to fourth and sixth embodiments"). For the third embodiment, Senda teaches changing the connection of the transistor to Node C without any other changes, and a POSITA would have understood the timing diagram in Figure 7 would still be used. *Id.*, [0210]. *Id.*, claims 1, 5; EX1002, ¶257.

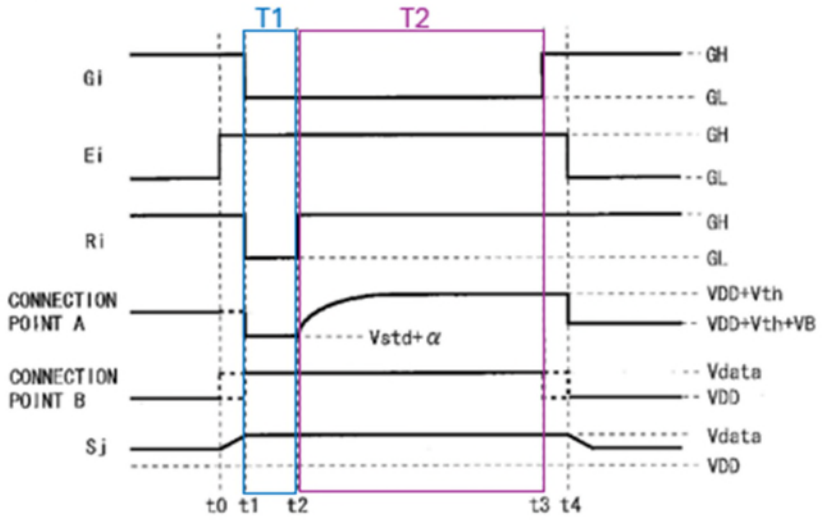
A POSITA would have understood it was known to connect the first reset unit to Node A or Node C, such that these were known design choices, and such that none of those design choices is novel or non-obvious. EX1002, ¶258.

A POSITA would have had a reasonable expectation of success in making the modification taught by Senda since it would have been a routine change that can easily be made. A POSITA knows how to connect transistors in a circuit. Senda teaches it was a known technique in the art to change the connection of the first reset unit from Node A to C and that each of the design choices could be used for a pixel circuit. EX1006, Figs. 2-3, 6-7, 11-12, 15-16, and accompanying text, [0217]-[0219]. Connecting transistors in the pixel circuit to make the modification taught by Senda would have been a routine matter involving known methods to a POSITA. EX1002, ¶259.

B. Claim 21

To the extent the additional limitation required by claim 21 is not disclosed as shown in Ground 3 by Figure 7, it would have been obvious over Senda. EX1002, ¶260.

Fig. 7



It would have been obvious to a POSITA to make T2 greater than T1, as illustrated in Figure 7, in order to make sure that the critical voltage difference is stored precisely in capacitor 320 as required during T2. EX1002, ¶261.

A POSITA would have been motivated to reduce the overall programming time relative to the display time and, therefore, would have been motivated to reduce the time of each programming step to the minimum time (with sufficient margin) required to complete the relevant operation for that step. EX1002, ¶262.

In minimizing the overall programming time, a POSITA would have understood that the precise voltage compensation operation would have taken longer than the simple operation in the preceding reset period, consistent with the illustrations in Senda's figures. Senda discloses that the only operation that must be completed in T1 is to reset the voltage on Node A to ensure that the driving transistor 310 is in a conductive state and that Node A will be Vstd plus a small but unknown value. EX1006, [0169]-[0170], [0212]-[0214]. In contrast, Senda discloses that during T2, the desired voltage must be precisely stored in capacitor 320 to accomplish Senda's purposes of compensating for the threshold voltage and emitting the desired amount of light. Senda stresses precision and full compensation is important. *Id.*, [0028]-[0029], [0151]-[0158], [0162]. A POSITA would have understood that precisely storing this voltage difference in capacitor 320 to ensure full compensation would take more time than simply putting 310 into

a conductive state. For example, a POSITA would have understood that the charging current through the driving transistor decreases as the gate voltage increases. A POSITA would have recognized this by Senda's disclosure that the period (either T2 or T3, depending on the embodiment) when voltage compensation is performed is always much greater than the preceding reset time period. *Id.*, Figs. 3, 5, 10, 12, 14 (T3 is much greater than prior reset period), Figs. 7, 16 (T2 is much greater than prior reset period). And with Senda's disclosure that the rate of increase in voltage at Node A slows during the voltage compensation period as compensation is performed, but that the change in voltage at Node A during the preceding reset time period is almost immediate. *Id.*; EX1002, ¶¶263-265 (explaining Senda's teaching that the compensation time would take longer and why a POSITA would have understood that to be the case with reference to EX1011, 806-808, EX1012, 505, and EX1013, 1-2, 6).

IX. DISCRETIONARY DENIAL IS NOT WARRANTED

A. 35 U.S.C. § 314(a) Analysis

The factors in *Apple Inc. v. Fintiv, Inc.*, IPR2020-0019, Paper 11 weigh against discretionary denial.

1. Stay

This factor is neutral because no stay motion has been filed and the Board will not attempt to predict how the district court will rule. *Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7.

2. Trial Date

The deadline for a Final Written Decision will likely be in August 2026. A trial date has been set for May 4, 2026. EX1009. However, there are eleven trials set for the same date (EX1014), and therefore it is likely that trial will occur sometime after that date. Thus, this factor is neutral.

3. Parallel Proceeding

This factor weighs against discretionary denial. Petitioner is seeking review promptly after service of infringement contentions. EX1010. At the time of the institution decision (August 2025), the parties will have only exchanged contentions, and the district court will not have issued any substantive orders. EX1009 (scheduling *Markman* hearing for November 2025); *Fintiv*, Paper 11 at 9-11.

4. Issue Overlap

This factor weighs strongly against discretionary denial. This Petition challenges claims 1-21 (all claims), including independent claim 17. The litigation involves only claims 1 and 16. EX1010.

5. Same Party

Because this Board is likely to reach the merits around the same time as the district court, this factor weighs slightly against discretionary denial. *See NVIDIA Corp. v. Invensas Corp.*, IPR2020-00603, Paper 11, at 23.

6. Other Considerations

Other considerations weigh strongly against discretionary denial. Petitioner has not previously challenged any related patents, and the 757 patent has never been challenged.

The merits of the grounds herein are "particularly strong," as shown by the fact that the references disclose the identical structures as the 757 patent, thereby invalidating the claims under narrow mean-plus-function constructions. *Fintiv*, Paper 11, 14-15 (a ground with "particularly strong" merits favors institution).

B. 35 U.S.C. § 325(b) Analysis

The asserted prior art was not of record during prosecution, is not cumulative of any art of record, and discloses the limitations the examiner found were missing during prosecution. *See* Section III.B. To the extent the art is cumulative, the examiner made a clear error in allowing the claims for the same reason.

X. COMPLIANCE WITH FORMAL REQUIREMENTS

A. Mandatory Notices Under 37 C.F.R. §§ 42.8(b)(1)-(4)

1. Real Party-In-Interest

BOE Technology Group Co., Ltd. is the real party-in-interest.

2. Related Matters

The 757 patent is subject to the following actions: Optronic Sciences LLC v. BOE Technology Group Co., LTD, 2:23-cv-00549 (EDTX).

3. Lead and Backup Counsel

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4. Service Information

Please address correspondence to counsel at the addresses above. Petitioner consents to electronic service to: dla-boe-optronicsciences-IPR@us.dlapiper.com and the email addresses listed above.

XI. CONCLUSION

All Challenged Claims of the 757 patent should be found unpatentable.

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Petitioner certifies that this petition includes 13,839 words, as measured by Microsoft Word, exclusive of the table of contents, mandatory notices under § 42.8, certificates of service, word count, claim listing, and exhibits.

Date: March 7, 2025

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CERTIFICATE OF SERVICE

The undersigned certifies pursuant to 37 C.F.R. §§ 42.6(e) and 42.105 that on March 7, 2025, a true and correct copy of the Petition for *Inter Partes* Review of U.S. Patent No. 8,502,757 was served by emailing a copy of same (by agreement) to the following attorneys for the Patent Owner:

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