UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MEDIATEK, INC. and
MEDIATEK USA, INC.,
Petitioners,

v.

REDSTONE LOGICS LLC,
Patent Owners.

IPR2025-00085
U.S. Patent No. 8,549,339

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,549,339

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I. MANDATORY NOTICES

A. Real Party-In-Interest (37 C.F.R. §42.8(b)(1))

Petitioners MediaTek Inc. and MediaTek USA, Inc. ("Petitioners" or "MediaTek") are real parties-in-interest.

B. Identification of Related Matters (37 C.F.R. §42.8(b)(2))

Patent Owner has asserted U.S. Patent No. 8,549,339 (the "'339 Patent") against Petitioners in co-pending civil litigation, *Redstone Logics LLC v. MediaTek, Inc. and MediaTek USA, Inc.*, No. 7:24-cv-00029-DC-DTG (W.D. Tex.) ("Texas Action"). Petitioner MediaTek USA, Inc. was served with the original complaint in the Texas Action on January 30, 2024. Ex[1012]. Petitioner MediaTek Inc. waived service of process on February 14, 2024. Ex[1013]. Patent Owner has asserted Claims 1, 5, 8-10, 14, and 21 of the '339 Patent against Petitioners. Ex[1014]. A schedule was entered in the Texas Action on August 27, 2024, which set trial for May 4, 2026. Ex[1015].

Patent Owner has also asserted the '339 Patent in *Redstone Logics LLC v. NXP Semiconductors N.V. et al*, No. 7:24-cv-00028-DC-DTG (W.D. Tex.), *Redstone Logics LLC v. Qualcomm Inc. et al*, No. 7:24-cv-00231-ADA (W.D. Tex.), and *Redstone Logics LLC v. Samsung Electronics Co., Ltd. et al*, No. 2:23-cv-00485-JRG (E.D. Tex.).

C. Counsel and Service Information (37 C.F.R. §§42.8(b)(3) & (b)(4))

Petitioners designate the following Lead and Backup Counsel. Concurrently filed with this Petition is a Power of Attorney for appointing the following Lead and Backup Counsel, per 37 C.F.R. § 42.10(b). Service via hand-delivery may be made at the postal mailing addresses below. Petitioners consent to electronic service by email at the following address: Case-MediaTekIPRMembers@pillsburylaw.com.

Lead Counsel	Back-Up Counsel
Robert C.F. Pérez (Reg. No. 39,328) PILLSBURY WINTHROP SHAW PITTMAN LLP 7900 Tysons One Place, Suite 500 Tysons, VA 22102 Telephone: 703.770.7759 Facsimile: 703.770.7901 Email: robert.perez@pillsburylaw.com	**Christopher Kao** (*Pro Hac Vice* to be requested) **Brock S. Weber** (*Pro Hac Vice* to be requested) **Surui Qu** (*Pro Hac Vice* to be requested) PILLSBURY WINTHROP SHAW PITTMAN LLP Four Embarcadero Center, 22nd Floor San Francisco, CA 94111 Telephone: 415.983.1000 Facsimile: 415.983.1200 christopher.kao@pillsburylaw.com brock.weber@pillsburylaw.com surui.qu@pillsburylaw.com **Michael Liu** (Reg No. 77,133) PILLSBURY WINTHROP SHAW PITTMAN LLP 2550 Hanover Street Palo Alto, CA 94304 Telephone: 650.233.4500 Facsimile: 650.233.4545 michael.liu@pillsburylaw.com

D. Payment of Fees (37 C.F.R. §42.103)

Petitioners authorize the Patent and Trademark Office to charge Deposit Account No. 033975 for the petition fee and for any other required fees.

II. INTRODUCTION

Petitioners hereby petition to institute *inter partes* review ("IPR") of Claims 1-6, 8-11, 14 and 21 ("Challenged Claims") of U.S. Patent No. 8,549,339 (the "'339 Patent," Ex[1001]), and cancel those claims as unpatentable under 35 U.S.C. § 103.

The prior art references presented in this Petition—Knoth (Ex[1005]), Allarey (Ex[1006]), Flautner (Ex[1007]), Wolfe (Ex[1008]), Kumar (Ex[1009]), and Naffziger (Ex[1010])—disclose multi-core processors with voltage and clock scaling functionality and related communications/control signaling that render the Challenged Claims obvious. None of the prior art presented in this Petition was cited or discussed during original prosecution.

III. STATEMENT OF PRECISE RELIEF REQUESTED FOR EACH CHALLENGED CLAIM/REQUIREMENTS FOR INTER PARTES REVIEW

This Petition complies with all statutory and regulatory requirements 37 C.F.R. §§ 42.103-105 and 42.15 and should be accorded the filing date of this Petition pursuant to 37 C.F.R. §42.106.

A. Grounds for Standing (37 C.F.R. § 42.104(a))

Petitioners certify that the '339 Patent is available for IPR and Petitioners are

not barred or estopped from requesting IPR of the Challenged Claims on the grounds identified in this Petition.

B. Claims for Which Review Is Requested (37 C.F.R. § 42.104(b))

Petitioners respectfully request review of the Challenged Claims of the '339 Patent pursuant to 37 C.F.R. § 42.300 and cancellation of those claims as unpatentable.

C. Statutory Grounds of Challenge

The Challenged Claims of the '339 Patent are unpatentable under 35 U.S.C. § 103 because they are obvious, as shown in the grounds below.

Ground	Invalidity	Exhibit(s)
1	Claims 1, 5, 8-10, 14 and 21 would have been obvious over Knoth (Ex[1005]) in view of Allarey (Ex[1006]) under 35 U.S.C. § 103.	**1005, 1006**
2	Claims 2-4 would have been obvious over Knoth (Ex[1005]) and Allarey (Ex[1006]) in view of Flautner (Ex[1007]) under 35 U.S.C. § 103.	**1005, 1006, 1007**
3	Claim 6 would have been obvious over Knoth (Ex[1005]) and Allarey (Ex[1006]) in view of	**1005, 1006, 1008, 1009**

Ground	Invalidity	Exhibit(s)
	Wolfe (Ex[1008]) and further in view of Kumar (Ex[1009] under 35 U.S.C. § 103.	
4	Claim 11 would have been obvious over Knoth (Ex[1005]) and Allarey (Ex[1006]) in view of Wolfe (Ex[1008]) under 35 U.S.C. § 103.	**1005, 1006, 1008**
5	Claims 1-3, 5, 8-10, 14 and 21 would have been obvious over Naffziger (Ex[1010]) and Allarey (Ex[1006]) under 35 U.S.C. § 103.	**1006, 1010**
6	Claim 4 would have been obvious over Naffziger (Ex[1010]) and Allarey (Ex[1006]) in view of Flautner (Ex[1007]) under 35 U.S.C. § 103.	**1006, 1007, 1010**
7	Claim 6 would have been obvious over Naffziger (Ex[1010]) and Allarey (Ex[1006]) in view of Wolfe (Ex[1008]) and further in view of Kumar (Ex[1009] under 35 U.S.C. § 103.	**1006, 1008, 1009, 1010**

Ground	Invalidity	Exhibit(s)
8	Claim 11 would have been obvious over Naffziger (Ex[1010]) and Allarey (Ex[1006]) in view of Wolfe (Ex[1008]) under 35 U.S.C. § 103.	**1006, 1008, 1010**

IV. CLAIM CONSTRUCTION

For the purposes of this Petition, Petitioners contend that, unless otherwise specifically noted herein, the claim terms in the '339 Patent are accorded their ordinary and customary meaning that they would have to a person having ordinary skill in the art at the time of the alleged invention ("PHOSITA"). Petitioners' interpretation of the claim terms is further explained for each limitation in relation to the prior art discussed in Grounds 1-8, below.[1]

V. A PERSON HAVING ORDINARY SKILL IN THE ART

A PHOSITA with respect to the '339 Patent would have had at least a bachelor's degree in electrical engineering, computer engineering, computer

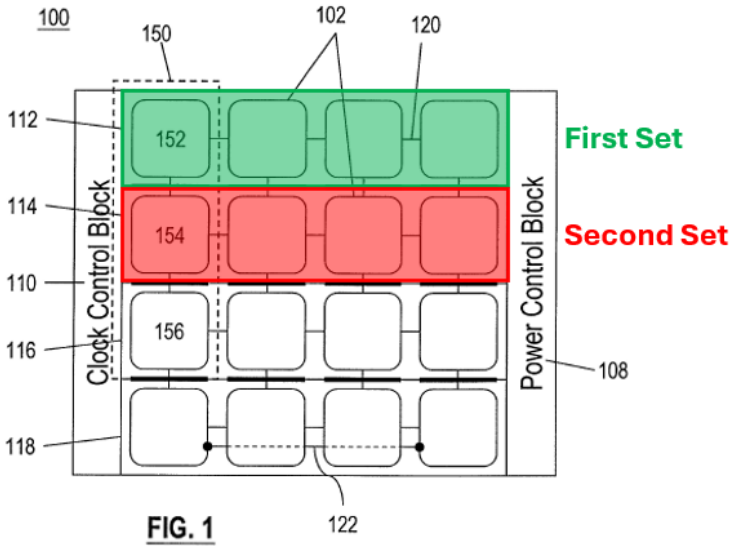
[1] Petitioners reserve the right to address any claim construction positions taken by the Patent Owner in its Preliminary Response, including under 37 C.F.R. § 42.108(c).

science, or a similar field, and at least two years of industry or academic experience designing or analyzing electronic circuits, semiconductors, processors, or power management, and related firmware and software, or the equivalent. Ex[1003] (Declaration of Dr. R. Jacob Baker), ¶ 29.

VI. OVERVIEW OF THE '339 PATENT

A. Purported Invention Of The '339 Patent

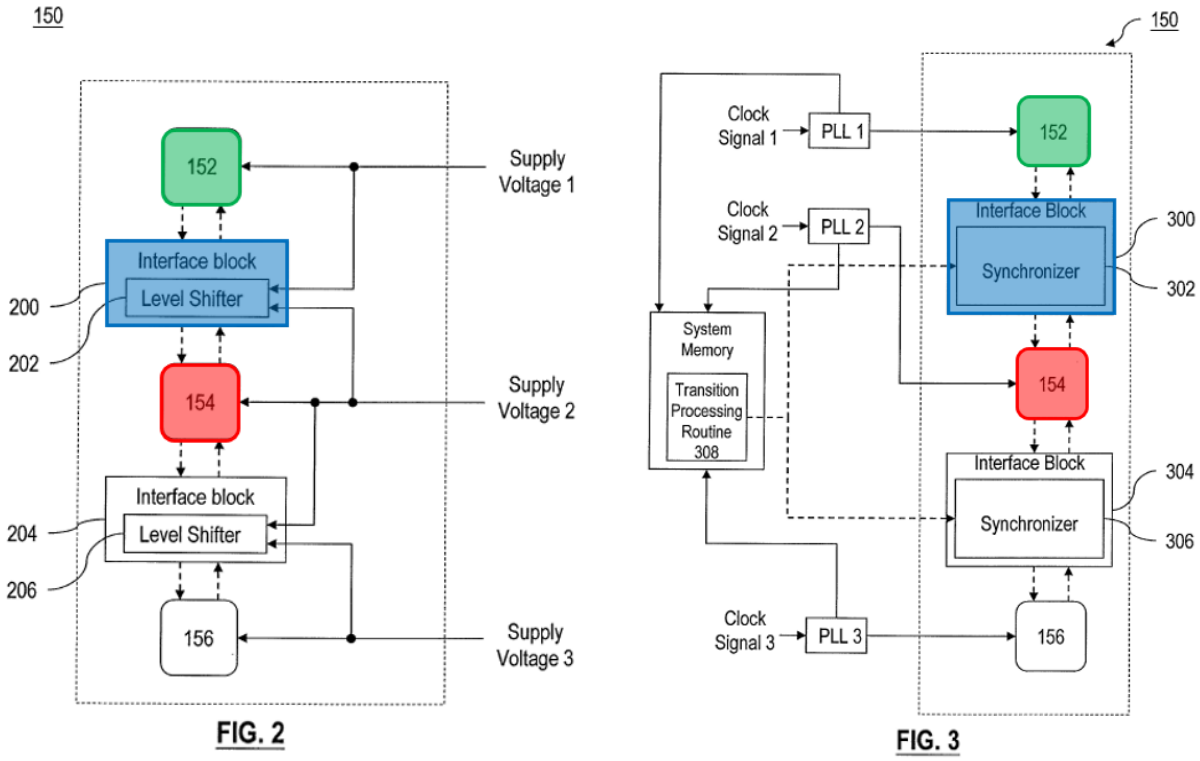
The '339 Patent concerns techniques for handling communication between processor cores of a multi-core processor. Ex[1001], Abstract. Figure 1 shows four sets of processor cores, with the first set and the second set of processor cores highlighted:



'339 Patent, Fig. 1 (annotated)

Figures 2 and 3 show an interface block coupled to the first and second sets

of processor cores:



'339 Patent. Figs. 2 and 3 (annotated)

The '339 Patent discloses dynamic voltage supply and clock speed control for the processor cores so that the multi-core processor may operate at high power and high clock frequency when needed and at low power when the computing requirements are reduced. *Id.*, 1:10-14. The power supplies for the first and second sets of processor cores are independent. Similarly, the clock signals of the first second sets of processor cores are independent. *Id.* at 2:25-31. As such, facilitating communication between two sets of processor cores is necessary and is performed by interface blocks. *Id.*, 3:21-23, 3:30-34, 4:4-8.

B. Priority Date

The earliest possible priority for the '339 Patent is February 26, 2010, the date it was filed, which is what Patent Owner has contended in the Texas Action. Ex[1016]. Petitioners take no position on the proper priority date for each claim of the '339 Patent, but assume this earliest date as the priority date.

VII. OVERVIEW OF THE STATE OF THE ART

Petitioners present the references below, none of which were cited or discussed during prosecution of the '339 Patent. Ex[1002]. The Board should not deny institution under Section 325(d). *See Amber.IO, Inc. D/B/A Two Tap v. 72Lux, Inc. D/B/A Shoppable*, IPR2020-00015, Paper 8 at 18-20 (PTAB April 1, 2020).

A. U.S. Patent Application Publication No. 2009/0158078 A1 to Knoth ("Knoth") (Ex[1005])

Knoth is a publication of a U.S. patent application filed on December 12, 2007 and published on June 18, 2009. Ex[1005] at 1. Knoth is prior art to the '339 Patent under at least 35 U.S.C. §§ 102(a) and 102(e)(1).

Knoth teaches a multiprocessor system that includes an arbitrary number of processor cores a-n. *Id.* at [0023]. Knoth's multi-core processor 100 includes a power management unit 102 that provides individual frequency management (FM) signals 111a-n to clock ratio controllers 106a-n to initiate frequency adjustments to independently control/scale the clock frequency of each processor core 110a-n;

power management unit 102 also provides individual management (VM) signals 113a-n to voltage controllers 107a-n to independently control the voltage of each processor core 110a-n. *Id.* at [0025], [0041]-[0042]. Coherency manager 108 is coupled to processor cores 110a-n to facilitate communications between the processor cores. *Id.* at [0006] and [0033].

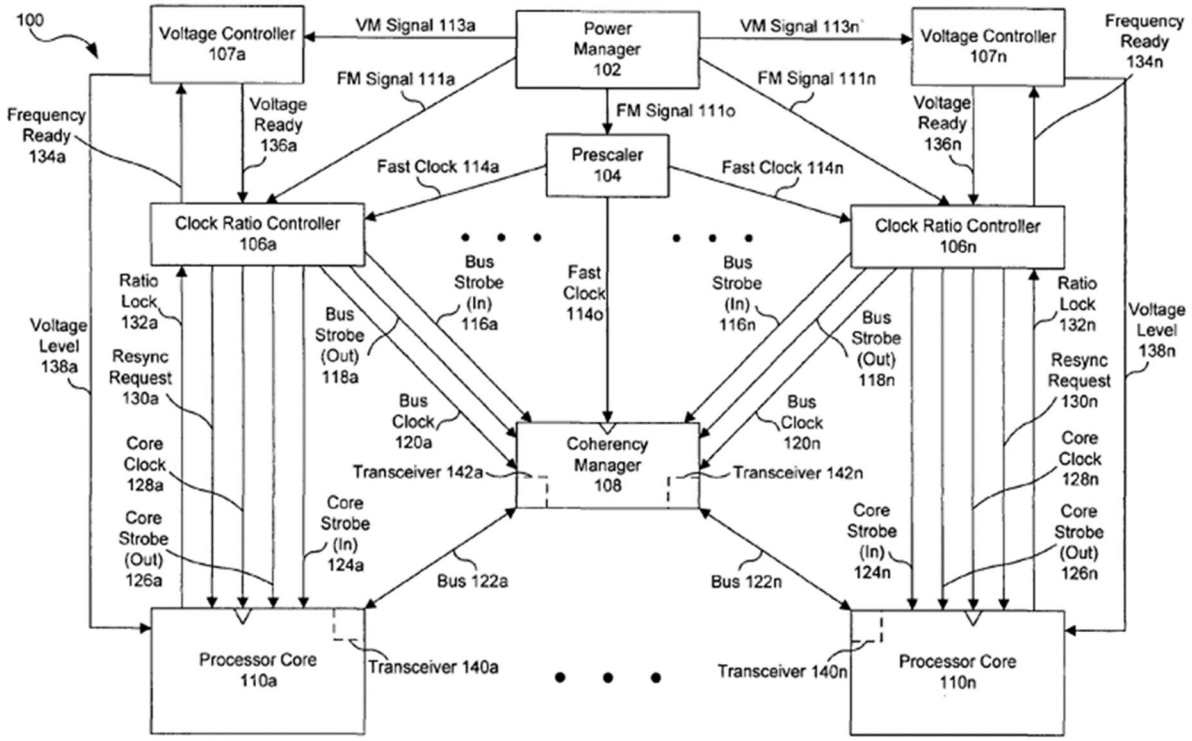


FIG. 1A

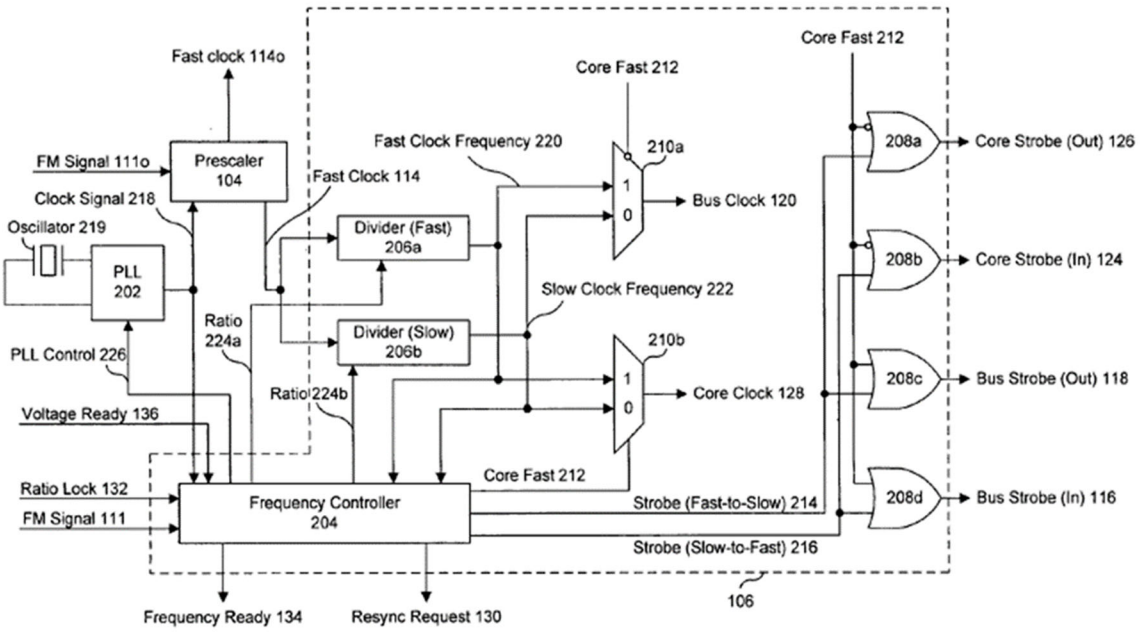


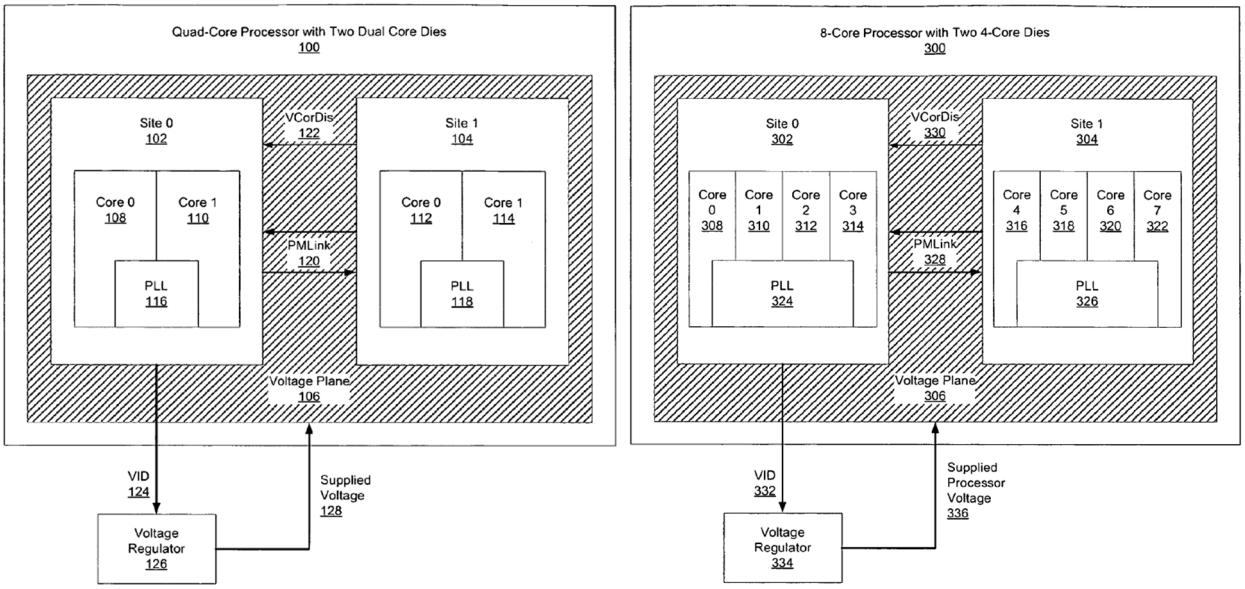
FIG. 2A

FIGS. 1A and 2A of Knoth

B. U.S. Patent No. 8,122,270 to Allarey et al. ("Allarey") (Ex[1006])

Allarey is a U.S. patent filed on September 29, 2008 and issued on February 21, 2012. Ex[1006] at 1. Allarey is prior art to the '339 Patent under at least 35 U.S.C. § 102(e)(2).

Allarey teaches a multi-core processor system comprising processor cores in two sites. The voltage supplied to the processor and the frequency of the cores in each site may be independently and dynamically modified. *Id.* at 1:15-24. Allarey discloses a power management link (PMLink) to couple the cores in the two sites. *Id.* at 2:59-3:3, 5:34-43.



FIGS. 1 and 3 of Allarey

C. U.S. Patent Application Publication No. 2005/0034002 A1 to Flautner ("Flautner") (Ex[1007])

Flautner a publication of a U.S. patent application filed on August 4, 2003 and published on February 10, 2005. Ex[1007] at 1. Flautner is prior art to the '339 Patent under at least 35 U.S.C. § 102(b).

Flautner discloses a multi-core processor that includes a synchronisation module 50 and a voltage level shifter 52 to deal with clock synchronization issues and the different supply voltage levels between cores in two independent domains. *Id.* at [0047]-[0048].

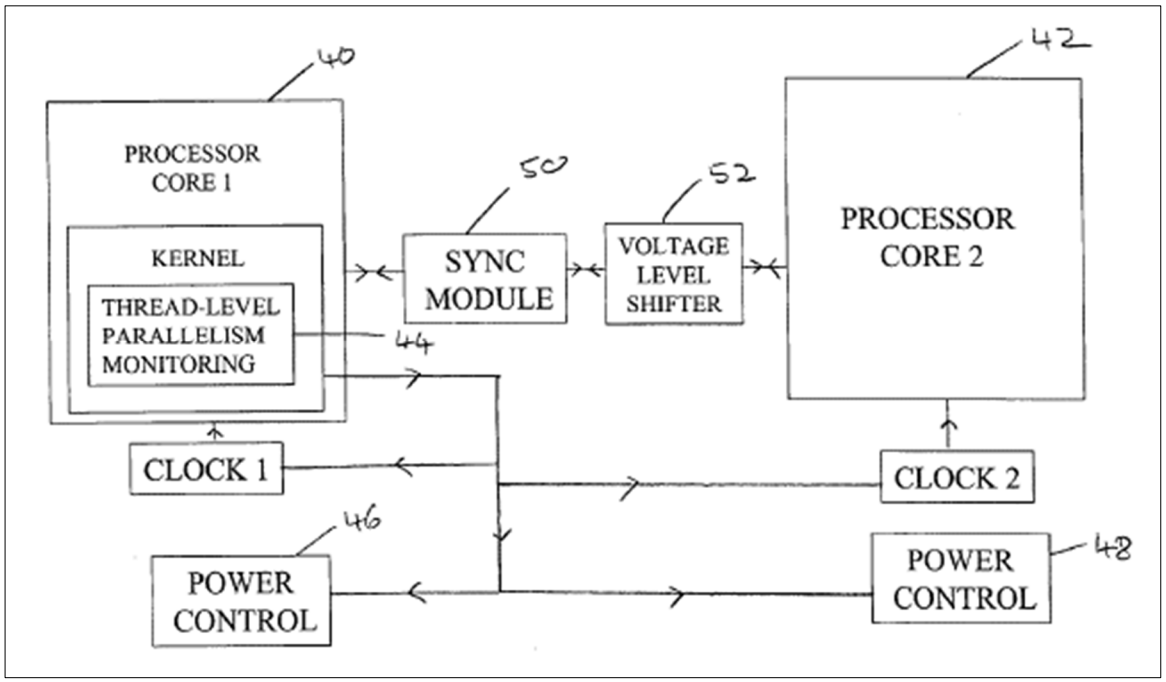


FIG. 4 of Flautner

D. U.S. Patent Application Publication No. 2011/0153984 A1 to Wolfe et al. ("Wolfe") (Ex[1008])

Wolfe is a publication of a U.S. patent application filed on December 21, 2009 and published on June 23, 2011. Ex[1008] at 1. Wolfe is prior art to the '339 Patent under at least 35 U.S.C. § 102(e)(1).

Wolfe teaches that processor cores may be "arranged in rows and columns in a 2-dimensional array." *Id.* at [0014]. Wolfe also discloses grouping cores based on geometric mapping. *Id.* at [0016], [0022].

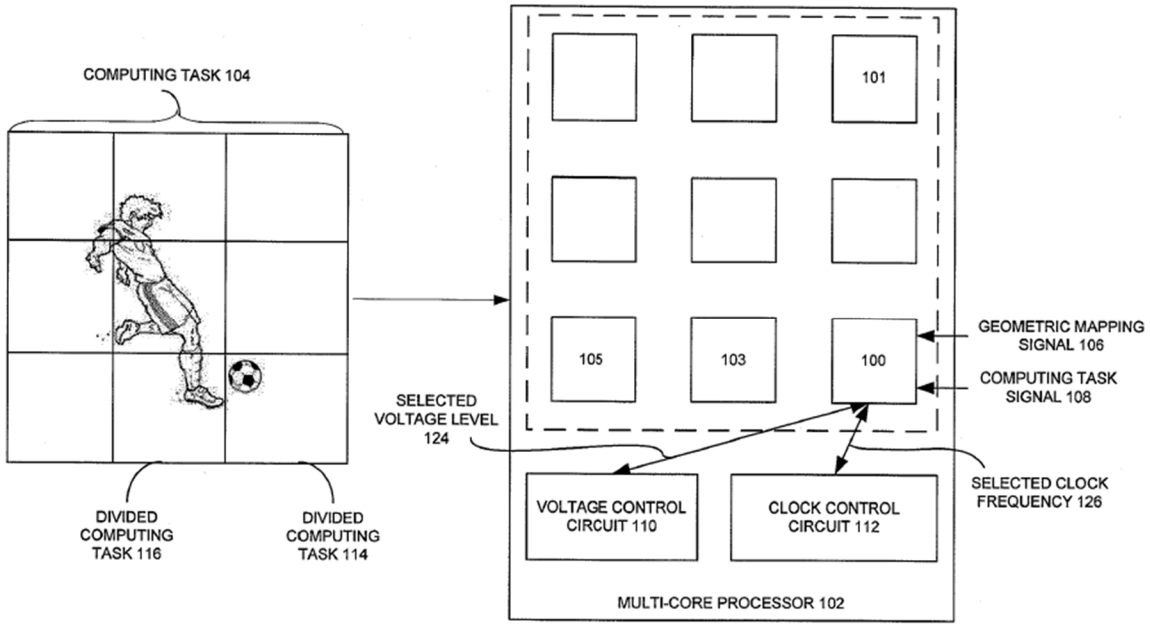


FIGURE 1A of Wolfe

A. U.S. Patent Application Publication No. 2007/0080696 A1 to Kumar et al. ("Kumar") (Ex[1009])

Kumar is a publication of a U.S. patent application filed on October 11, 2005 and published on April 12, 2007. Ex[1009] at 1. Kumar is prior art to the '339 Patent under at least 35 U.S.C. § 102(b).

Kumar discloses monitoring and adjusting a voltage V_1 across one or more components 130 and a voltage V_2 across one or more components 530 based on one or more predetermined relationships, including whether the absolute value of the difference between voltage V_1 and the voltage V_2 is less than, or equal to, a predetermined amount or a predetermined percentage of either V_1 or V_2. *See, e.g.*, *id.* at [0058]-[0059].

B. U.S. Patent Application Publication No. 2010/0122101 A1 to Naffziger et al. ("Naffziger") (Ex[1010])

Naffziger is a publication of a U.S. patent application filed on November 11, 2008 and published on May 13, 2010. Ex[1010] at 1. Naffziger is therefore prior art to the '339 Patent under at least 35 U.S.C. § 102(e)(1).

Naffziger teaches a multi-core processor, wherein the cores have separate, independent core supply voltage planes and are configured to receive separate, independently controlled core clock signals from PLL circuits. *Id.* at [0054].

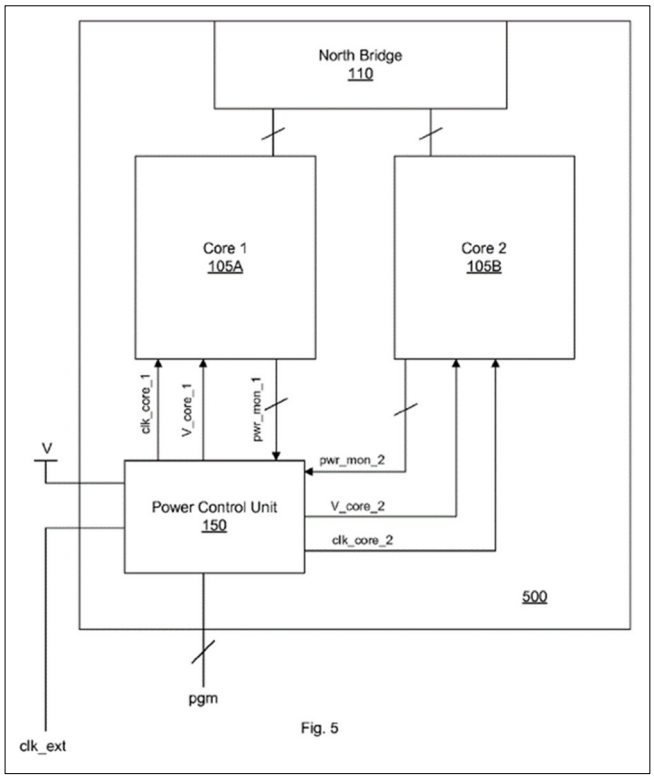


FIG. 5 of Naffziger

VIII. GROUND 1: CLAIMS 1, 5, 8-10, 14 AND 21 ARE OBVIOUS UNDER §103 OVER KNOTH IN VIEW OF ALLAREY

Knoth and Allarey, alone or in combination, disclose each and every limitation of Claims 1, 5, 8-10, 14 and 21.

A. Motivation to Combine Knoth and Allarey

A PHOSITA would have been motivated to combine Knoth and Allarey and would have had a reasonable expectation of success in doing so, because they relate to the same well-known technologies. Ex[1003], ¶¶ 80-95.

Knoth and Allarey are directed to the same field of multi-core processors, address similar problems and propose similar solutions for managing voltage and frequency scaling of multi-core processors. Ex[1003], ¶¶ 80-86. For example, Knoth discloses solutions for multi-core processor systems to control power consumption that include changing operational states with different power consumptions by adjusting the voltage and clock frequency. *See* Ex[1005] at [0001]-[0003]. Allarey describes solutions to optimize the ability of multi-core processor systems to conserve power by dynamically modifying the voltage supplied to and the frequency of the processor. *See* Ex[1006] at 1:6-24.

Knoth is authored by MIPS engineers, and Allarey is authored by Intel engineers. Ex[1003], ¶¶ 87-89. A PHOSITA would have looked to publications by such leading companies in semiconductor design, such as MIPS and Intel, and considered the similar techniques disclosed in these references for optimizing the

power and/or performance of cores. *Id*.

A PHOSITA also would have found the combination obvious to try because it combines well-known techniques that are related—e.g., Knoth provides a system that dynamically adjusts clock signals without losing synchronization, focusing on coordination between different clock domains; Allarey provides a method to ensure stable voltage during these adjustments, crucial for the proper functioning of Knoth's clock ratio controller. *Id.*, ¶ 90. Knoth's method relies on stable voltage conditions during frequency adjustments, which Allarey's invention directly addresses. *See, e.g.*, Ex[1005] at [0032]; Ex[1006] at 3:25-49; Ex[1003], ¶¶ 91-93. A PHOSITA would have found synergy in combining dynamic power adjustments from Knoth with voltage stabilization from Allarey to improve overall processor performance and stability. *Id*. Therefore, a PHOSITA would have found that Knoth and Allarey provide complimentary solutions and would have been motivated to combine them to benefit from their respective teachings. *Id*.

Finally, a PHOSITA would have considerable expectation of success when combining these teachings because the combination would amount to a mere substitution of one known element (e.g., Knoth's core-level control) for another (Allarey's site-level control), applying a known technique to a known system ready for improvement, and/or use of known techniques to improve in a similar multi-core

environment. *Id*., ¶¶ 94-95. Therefore, the teachings and considerations of Allarey would allow a PHOSITA to improve on Knoth's systems effortlessly (and vice versa). *Id*.

B. Claim 1

1. 1[pre]

To the extent that the preamble is limiting, Knoth teaches a multi-core processor. Ex[1003], ¶¶ 96-98. For example, Knoth discloses that "digital system 100 is a multiprocessor digital system that includes at least two processor cores 110." Ex[1005] at [0023]. *See, e.g.*, *id.* at FIG. 1A.

Allarey also discloses a "multi-core processor." Ex[1003], ¶¶ 99-102; Ex[1006] at 1:6-8. For example, Allarey discloses a quad-core processor 100 that includes two dual-core dies. *Id.* at 2:38-58; FIG. 1. As another example, Allarey discloses an 8-core processor with two 4-core dies 100. *Id.* at 5:13-23; FIG. 3.

2. 1[a1]

Knoth and Allarey, alone or in combination, disclose this limitation. Ex[1003], ¶¶ 103-109.

Knoth discloses that "digital system 100 is a multiprocessor digital system that includes at least two processor cores 110." Ex[1005] at [0023], FIG. 1A.

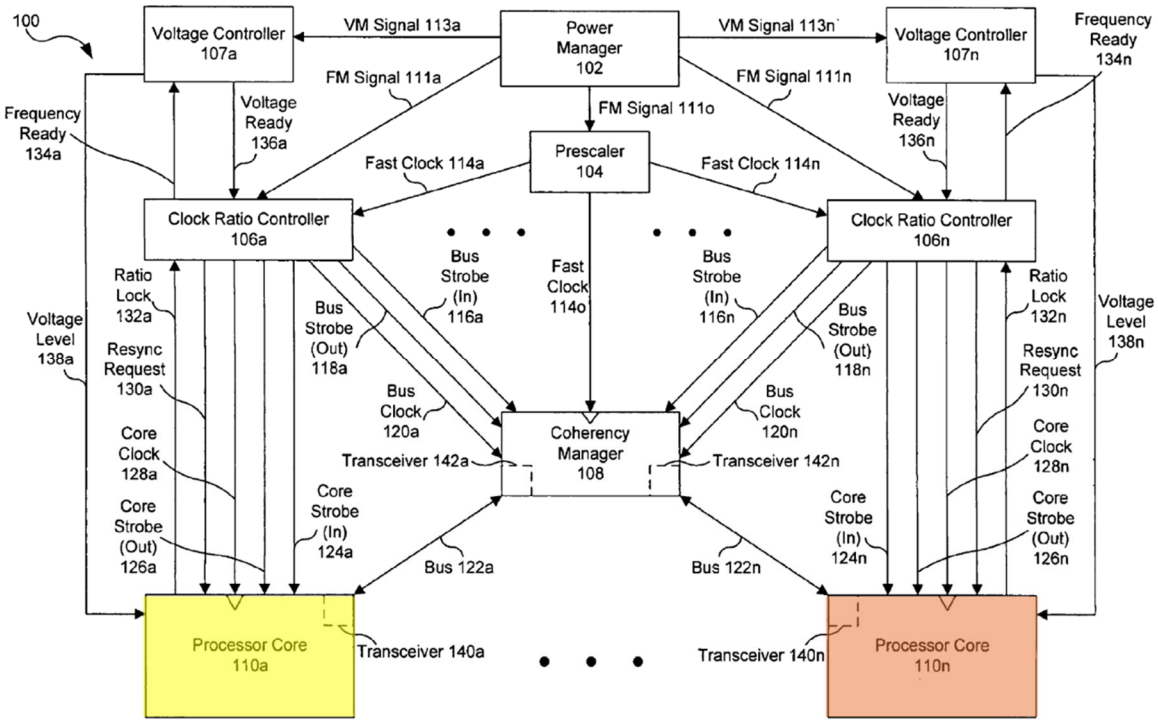


FIG. 1A of Knoth, annotated

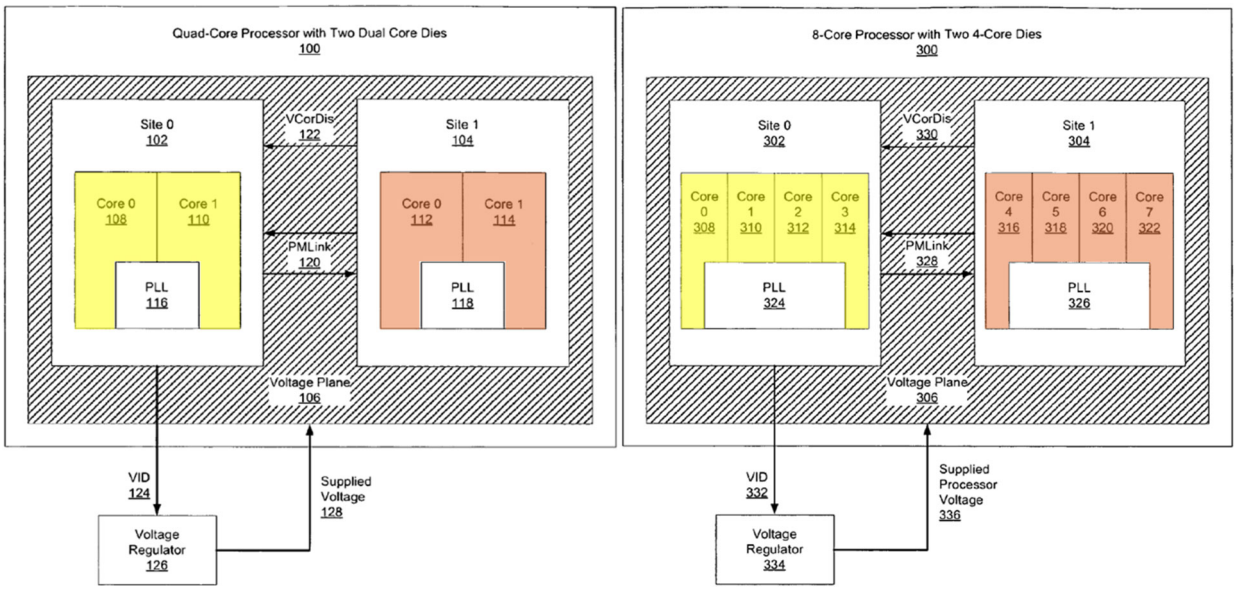
The multiprocessor digital system 100 includes a series of processor cores a-n, with an explicit depiction of at least two processor cores 110a (highlighted in yellow) and 110n (highlighted in orange). Knoth discloses that the processor cores 110a-n operate independently through dedicated power and frequency management. Ex[1005] at [0025]-[0027], [0031]. The processor cores 110a and 110n disclose the recited first set of processor cores and the second set of processor cores of the multi-core processor, to the extent that a "set" can include one or more. Ex[1003], ¶¶ 104-106.

To the extent it is argued that the processor cores 110a-n are individual cores,

or that a "set" means "two or more," it would have been obvious to a PHOSITA to extend the disclosed architecture of Knoth to include two distinct sets of cores, where each set of cores is managed separately. *Id.*, ¶ 107. After all, Knoth discloses an arbitrary number of processor cores a-n and, therefore, more than two cores could be included in two distinct sets. *Id.* Extending Knoth's architecture to treat two cores or more in at least two distinct sets would have been a routine and desired modification for a PHOSITA, requiring only minor adjustments to the existing power and frequency management mechanisms, such as sending the power control signals to an individual core to a shared power domain or voltage plane for a set of cores that operates under the same conditions, which was common and well-understood adjustments a PHOSITA would have easily implemented. *Id.* A PHOSITA would have also understood that extending from individual cores to sets of cores would improve the system by enabling more efficient management of power and resources through grouped control, reducing complexity and enhancing scalability for handling diverse workloads. *Id.*

Furthermore, a PHOSITA would have been motivated to modify Knoth to have two sets of cores, rather than two individual cores, based on the teachings of Allarey. *Id.*, ¶ 108.

Allarey discloses a first set of processor cores in the form of a multi-core die in site 0 (highlighted in yellow) and a second set of processor cores in the form of a multi-core die in site 1 (highlighted in orange), as depicted below. Ex[1006] at 2:41-58, 5:17-33.



FIGs. 1 and 3 of Allarey, annotated

A PHOSITA would have understood that modifying Knoth based on Allarey to have sets of cores would achieve the benefits of reducing the complexity of individually managing each core, leading to improved scalability, reduced overhead, and more efficient resource allocation of the semiconductor system. Ex[1003], ¶ 107. Accordingly, Knoth and Allarey, alone or in combination, disclose this limitation. *Id.*, ¶¶ 103-109.

3. 1[a2]

Knoth discloses this limitation. Ex[1003], ¶¶ 110-116. As depicted in FIG. 1A below, Knoth discloses that each of the processor cores 110a-n receives its respective voltage supply "voltage level signal 138a-n" (shown by blue lines) from its respective voltage controller 107a-n and its respective clock signal core clock signal 128a-n (shown by purple lines) output from respective clock ratio controller 106a-n (shown by purple boxes). Ex[1005] at [0027], [0031]. As explained below, each of clock ratio controllers 106a-n includes a phase locked loop (PLL) (for ease of discussion, referred to as PLL 202a-n corresponding to clock ratio controller 106a-n) (highlighted in purple).

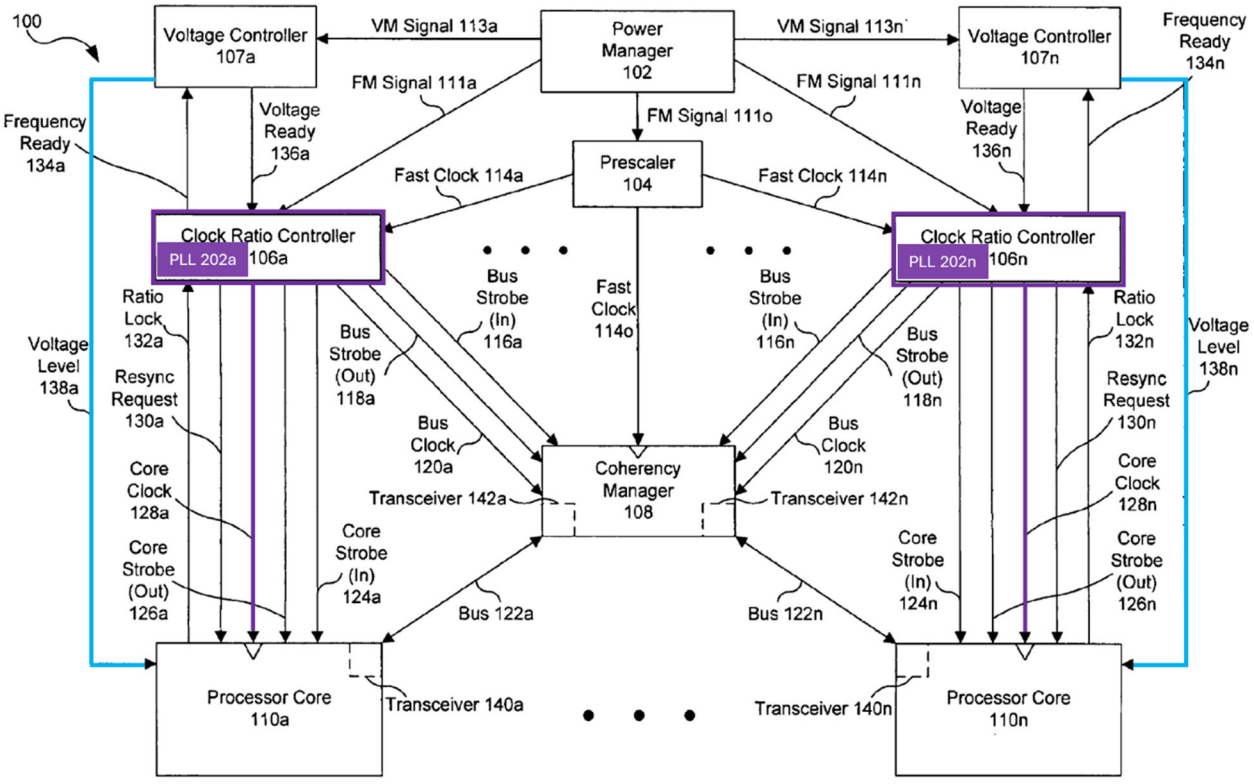


FIG. 1A of Knoth, modified to show PLL 202a and PLL 202n

As illustrated in FIG. 2A below, Knoth discloses clock ratio controllers 106a-n that each includes a phase locked loop (PLL) 202 (highlighted in purple) having as input "timing pulses generated by an oscillator 219" within the corresponding clock ratio controller 106 (for ease of discussion, referred to as oscillator 219a-n corresponding to clock ratio controller 106a-n). Ex[1005] at [0041]-[0042]. Alternatively, each PLL within clock ratio controller 106 receives as input a "PLL control signal 226" (for ease of discussion, referred to as PLL control signal 226a-n corresponding to clock ratio controller 106a-n).

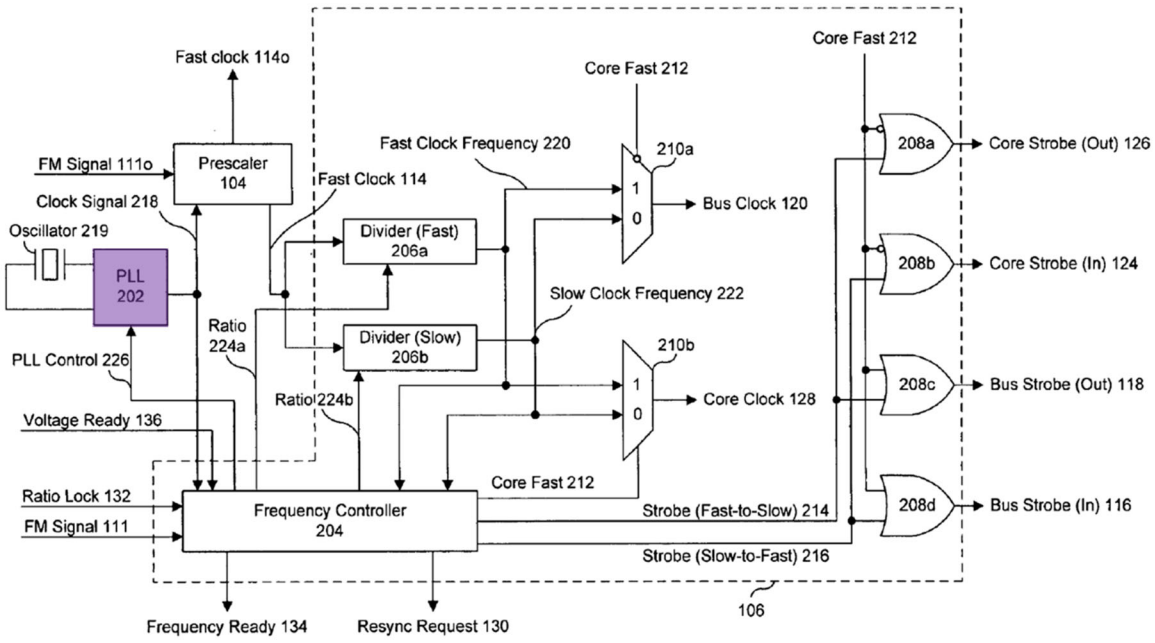


FIG. 2A of Knoth, annotated

Processor cores 110a-n receive respective voltage supply "voltage level signal

138a-n" from voltage controller 107a-n and respective output clock signal "core clock signal 128a-n" from clock ratio controller 106a-n for "dynamic voltage and frequency scaled digital systems." *Id.* at [0001]. Specifically, Knoth discloses that each of voltage controllers 107a-n receives "individual voltage management (VM) signals 113a-n" that "individually control/scale the voltage of each processor core 110a-n" so that the voltage supply may increase or decrease. *Id.* at [0025], [0031]-[0032]. Processor cores 110a-n thus dynamically receive voltage level 138a-n.

Knoth also discloses that each of clock ratio controllers 106a-n receives "individual frequency management (FM) signals 111a-n" that "initiate frequency adjustments" to "individually control/scale the frequency of each processor core 110a-n" so that core clock signals 128a-n are dynamically modified. *Id.* at [0025], [0027], [0032]. Processor core 110a-n thus dynamically receives core clock 128a-n.

Thus, Knoth discloses that the first set of cores (processor core 110a extendable to include associated cores, or processor core 110a of Knoth modified in view of Allarey to include a set of multiple cores) dynamically receives a first supply voltage (voltage level 138a) and a first output clock signal (core clock 128a) of a first phase lock loop (PLL) (PLL 202a) having a first clock signal as input (the timing pulses from oscillator 219a, or alternatively, PLL control signal 226a); the second set of cores (processor core 110n extendable to include associated cores, or processor

core 110n of Knoth modified in view of Allarey to include a set of multiple cores) dynamically receives a second supply voltage (voltage level 138n) and a second output clock signal (core clock 128n) of a second phase lock loop (PLL) (PLL 202n) having a second clock signal as input (the timing pulses from oscillator 219n, or alternatively, PLL control signal 226n). Ex[1003], ¶ 116.

Allarey also discloses this limitation. *Id.*, ¶¶ 117-121. Allarey discloses that the processor cores in site 0 and the processor cores in site 1 are supplied with voltage from voltage plane 106. Ex[1006] at 2:41-44, 2:59-3:24. "Site 1(104) may have different voltage requirements than site 0 (102) at any given time" and requests a different voltage. *Id.* at 3:20-24.

Further, Allarey discloses that the processor cores in site 0 (e.g., cores 108 and 110 in site 0 (102)) receive the clock signal generated by the PLL for site 0 (PLL 116) (highlighted in purple). *Id.* at 2:38-3:3. The processor cores in site 1 (e.g., cores 112 and 114 in site 1 (104)) receive the clock signal generated by the PLL for site 1 (PLL 118) (highlighted in purple). *Id.*

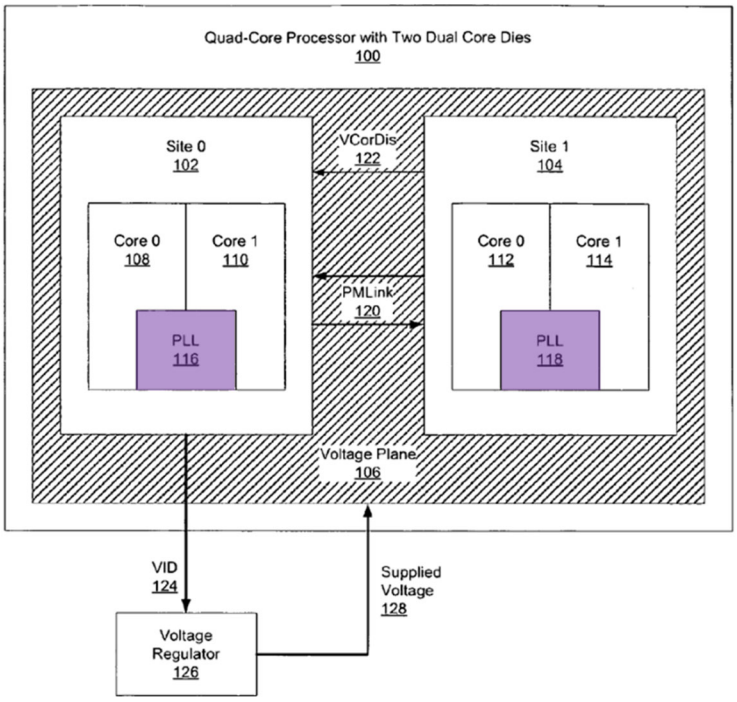


FIG. 1 of Allarey, annotated

"The voltage supplied to the processor and the frequency of the processor may be dynamically modified." *Id.* at 1:15-17. Allarey discloses "dynamically modify[ing]" "[t]he voltage supplied to the processor and the frequency of the processor." *Id.* at 1:12-24. Specifically, Allarey discloses "dynamically modify[ing] a voltage supplied to the first site" and "voltage regulator 126 … regulates the supplied voltage 128 … to supply to the voltage plane 106." *Id.* at Abstract and 3:4-19, FIG. 1. Accordingly, Allarey discloses that the cores in site 0 and site 1 dynamically receive respective supply voltages.

For the clock signaling, "[e]ach PLL can change the frequency of the clock signal." *Id.* at 2:41-58. Further, Allarey discloses that "[e]ach site includes a phase

locked loop (PLL) clock signal generation circuit" and "[e]ach PLL is capable of generating a clock signal." *Id.* at 2:41-58. Accordingly, Allarey discloses that the cores in site 0 and site 1 dynamically receive respective output clock signals of a PLL.

4. 1[b1]

As explained for Claim 1[a1] in Ground 1, Knoth and Allarey, alone or in combination, disclose this limitation.

5. 1[b2]

As explained for Claim 1[a2] in Ground 1, Knoth and Allarey, alone or in combination, disclose this limitation.

6. 1[b3]

Knoth discloses this limitation. Ex[1003], ¶¶ 124-126. Knoth discloses that the first and second sets of cores receive independent supply voltages. Knoth discloses that "VM signals 113a-n can be used to individually control/scale the voltage of each processor core 110a-n" and "[e]ach voltage controller 107a-n also sends a voltage or voltage level signal 138a-n to each processor core 110a-n to power each processor core 110a-n." Ex[1005] at [0025] and [0031]. Accordingly, Knoth teaches individually controlling each voltage level signal 138a-n such that the first supply voltage is independent from the second supply voltage.

Allarey also this limitation. Ex[1003], ¶¶ 127-128. The first and second sets of cores of Allarey receive independent supply voltages. Ex[1006] at 3:20-24 ("[s]ite 1 (104) may have different voltage requirements than site 0 (102) at any given time."). Accordingly, Allarey teaches different supply voltage requirements for the sets of processor cores such that the first supply voltage is independent from the second supply voltage.

7. 1[b4]

Knoth discloses this limitation. Ex[1003], ¶¶ 129-134. Knoth discloses that clock ratio controllers 106a-n receive, respectively, "individual frequency management (FM) signals 111a-n" that are "used to individually control/scale the frequency of each processor core 110a-n." Ex[1005] at [0025]. Thus, clock ratio controllers 106a-n operate independently from each other. Ex[1003], ¶ 130. As such, the first clock signal of the first PLL within clock ratio controller 106a is independent from the second clock signal of the second PLL within clock ratio controller 106n. *Id*.

Furthermore, as explained for Claim 1[a2] in Ground 1, Knoth discloses that clock ratio controller 106a-n each includes a phase locked loop (PLL) 202 having as input "timing pulses generated by an oscillator 219" within the corresponding clock ratio controller 106. Ex[1006] at [0041]-[0042]. A PHOSITA would read Knoth to

include independent first and second PLLs within clock ratio controllers 106a and 106n, respectively, receiving the first and second clock signals (the timing pulses generated by oscillators 219a and 219n) that are independent from each other. Ex[1003], ¶¶ 131-132.

Alternatively, PLL control signals 226a and 226n of Knoth disclose that the first and second clock signals are independent of each other, as claimed. *Id.*, ¶ 133. Each PLL control signal 226 is generated based on its respective, independent "voltage ready signal 136" (136a-n) and "FM signal 111" (111a-n). Ex[1005] at [0055]. Specifically, each voltage ready signal 136a-n is provided by a separate voltage controller 107a-n operating independently from each other. *Id.* at [0025], [0031]. Knoth also discloses that "power management unit 102 provides individual frequency management (FM) signals 111a-n" that separate from each other. *Id.* at [0025].

Allarey also discloses this limitation. Ex[1003], ¶¶ 135-136. In Allarey, each site includes a PLL clock signal generation circuit. Ex[1006] at 2:41-58. The PLL clock signal generation circuits are independent of each other. Ex[1003], ¶ 136. Therefore, the first PLL clock signal generation circuit is independent from the second PLL clock signal generation circuit. *Id*.

8. 1[c1]

Knoth discloses this limitation. Ex[1003], ¶¶ 137-140. As depicted in FIG. 1A, Knoth discloses a coherency manager 108 (highlighted in green) coupled to the processor cores 110a and 110n (highlighted in yellow). Ex[1005] at [0033], FIG. 1A.

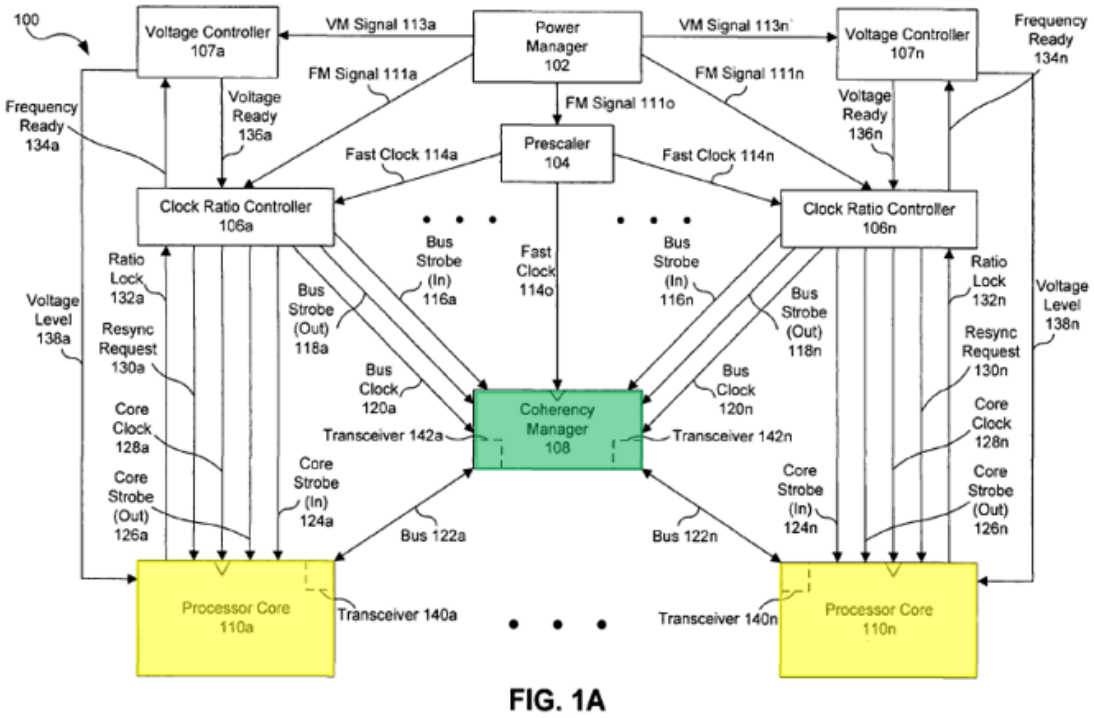


FIG. 1A

FIG. 1A of Knoth, annotated

Coherency manager 108 and processor cores 110a-n are coupled together by busses 122a-n. *Id.* at [0033]. Therefore, Knoth discloses an interface block (coherency manager 108) coupled to the first set of processor cores (110a) and the second set of processor cores (110n).

Allarey also discloses this limitation. Ex[1003], ¶¶ 141-143. As depicted in FIG. 1, Allarey discloses a power management link (PMLink) 120 (highlighted in green) that couples the cores in site 0 and site 1 (highlighted in yellow). Ex[1006] at 2:59-3:3, FIG. 1A. "[P]ower management link (PMLink) 120 communicatively couples site 0 and site 1." *Id.* at 2:59-3:3.

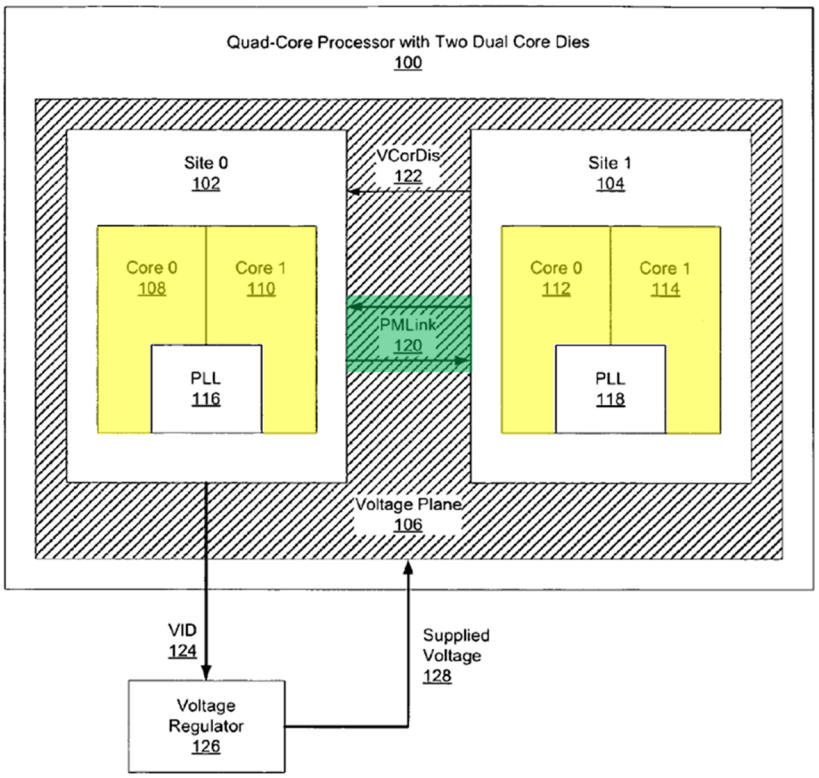


FIG. 1A of Allarey, annotated

9. 1[c2]

Knoth discloses this limitation. Ex[1003], ¶ 144. Knoth discloses that coherency manager 108 "facilitate[s] communications between the first digital circuit and the second digital circuit." Ex[1005] at [0006]. Accordingly, Knoth

teaches that the interface block (coherency manager 108) is configured to facilitate communications between the first set of processor cores 110a and the second set of processor cores 110n.

Allarey also discloses this limitation. Ex[1003], ¶¶ 145-146. Allarey teaches "power management link (PMLink) 120 communicatively couples site 0 and site 1," which is further described as "transmitting data back and forth between site 0 (102) and site 1 (104)." Ex[1006] at 2:59-3:3.

C. Claim 5

1. 5[pre]

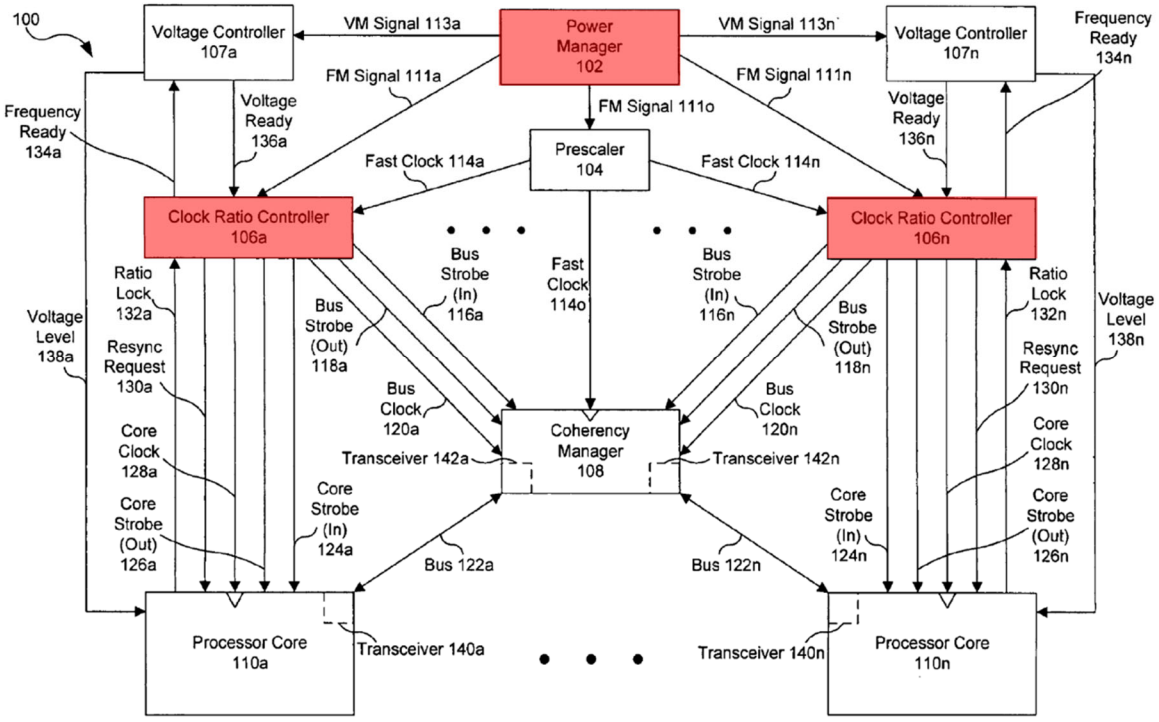
As explained above for Claim 1, Knoth and Allarey, alone or in combination, disclose each and every limitation of Claim 1.

2. 5[a]

The '339 Patent provides no definition or explanation of the claimed "control signals."

Knoth discloses that "power management unit 102 provides individual frequency management (FM) signals 111a-n" and "individual voltage management (VM) signals 113a-n." Ex[1005] at [0025]. FM signals 111a-n "are used … to initiate frequency adjustments" and "to individually control/scale the frequency of each processor core 110a-n." *Id.* VM signals 113a-n "are used … to initiate voltage adjustments" and "to individually control/scale the Voltage of each processor core

110a-n." *Id.* As depicted below, power management unit 102 (highlighted in red) is located in the periphery of Knoth's multi-core processor. *Id.* at FIG. 1A (annotated).



Knoth also discloses that "clock ratio controllers 106a-n … generate resynchronization (resync) requests 130a-n" that coordinates synchronization between the processor cores and controls timing of synchronization and frequency adjustments. *Id.* at [0029]. "[R]esynchronization requests 130a-n are an indication from clock ratio controllers 106a-n to processor cores 110a-n that a clock ratio adjustment is about to occur." *Id.* As depicted above, clock ratio controllers 106a-n (highlighted in red) are located in the periphery of Knoth's multi-core processor.

The ’339 Patent provides no indication that the location of the control blocks would in any way alter their function. *See* Ex[1003], ¶¶ 153-154. A PHOSITA would have understood that to place a control block in the periphery, centrally, or in other locations serves the same function of providing control signals for managing/coordinating the operations of processor cores. *Id.* A PHOSITA would have also understood that this function depends on the logical connections and signal routing, rather than the physical location of the control block relative to the processor. *Id.* Thus, a control block could be relocated from a substantially central location to the periphery (or vice versa) without affecting its ability to perform this function. *Id.* A PHOSITA would have understood that the physical location of a control block would have been driven by routine design preferences, such as minimizing of the length of critical paths to other components of the processor. *Id.* Therefore, a PHOSITA reading Knoth would have found it obvious that the control blocks of Knoth could be placed at a periphery of the multi-core processor. *Id.*, ¶¶ 149-154.

Allarey also discloses this limitation. *Id.*, ¶¶ 155-159. Allarey discloses that “there is a master site and a slave site with respect to controlling the voltage level supplied to the voltage plane 106” that supplies supply voltages to the first and second sets of cores of Allarey. Ex[1006] at 2:65-3:3. Specifically, “logic within site

0 (102) dictates the supplied voltage to both site 0 (102) and site 1 (104)" by "send[ing] a voltage identification (VID) value 124 to a voltage regulator 126 external to the processor." *Id.* at 3:4-19. "The voltage regulator 126 interprets the VID value and based on that information, regulates the supplied voltage 128 to the processor 100." *Id.* Voltage identification (VID) value 124 "informs … the new voltage to supply" "for supplied voltage modifications." *Id.* A PHOSITA reading Allarey would have understood that voltage regulator 126 is responsible for adjusting the voltage supplied to the processor cores and to carry out that function, voltage regulator 126 must internally generate one or more control signals that adjust the output voltage level. Ex[1003], ¶ 157. Such internal control signals are inherently part of how a voltage regulator operates. *Id.*

Therefore, Allarey teaches that the processor cores of Allarey receive one or more control signals including VID value 124 from logic within site 0 (102) (highlighted in red) and the control signals from voltage regulator 126 (highlighted in red). Ex[1006], FIG. 1 (annotated). As depicted below, voltage regulator 126 is located at a periphery of the multi-core processor of Allarey. *Id.*; *see also id.* at 3:5-6 (voltage regulator 126 is located "external to" the processor dies).

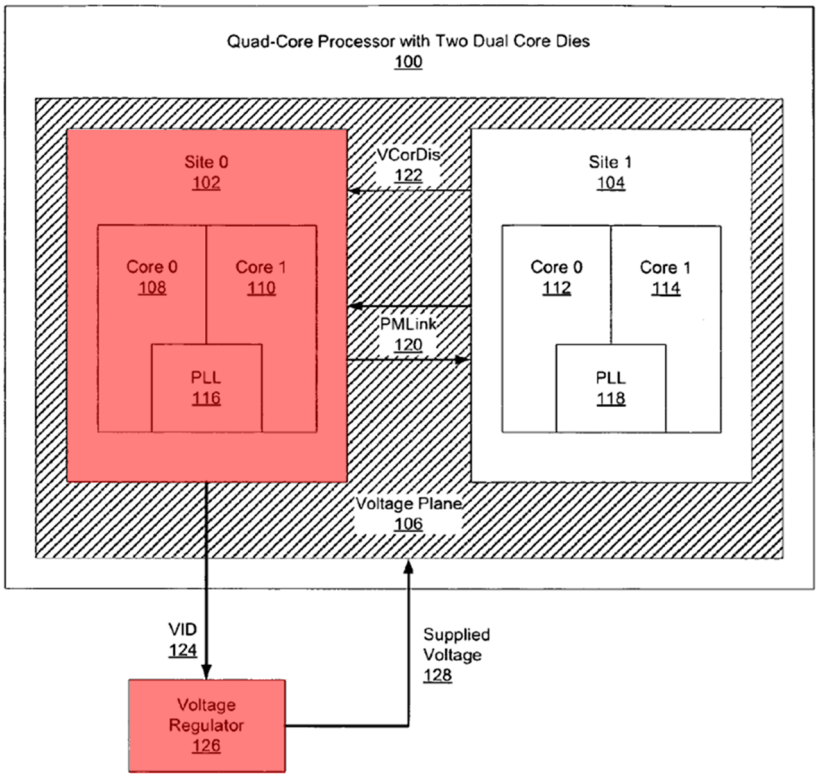


FIG. 1 of Allarey, annotated

Furthermore, as explained above, a PHOSITA reading Allarey would have found it obvious that the control blocks including voltage regulator 126 would be placed at a periphery of the multi-core processor without affecting its function of providing control signals to the processor cores. Ex[1003], ¶¶ 154, 159.

D. Dependent Claim 8

1. 8[pre]

As explained above for Claim 1, Knoth and Allarey, alone or in combination, disclose each and every limitation of Claim 1.

2. 8[a]

The '339 Patent discloses that a "region" is simply a spatial grouping of cores. *See, e.g.*, Ex[1001] at 2:20-23 ("the regions of multi-core processor 100 may correspond to rows of the two-dimensional array, and the regions may or may not be overlapping"), FIG. 5 ("the second region is adjacent to the first region"); Ex[1003], ¶ 162.

Knoth discloses this limitation. *Id.*, ¶¶ 163-166. Knoth discloses that the multi-core processor system comprises an arbitrary number of cores a through n, including at least two sets of processor cores, for example, 110a and the associated cores (e.g., cores b-i) (highlighted in yellow) and 110n and the associated cores (e.g., cores j-n) (highlighted in orange).

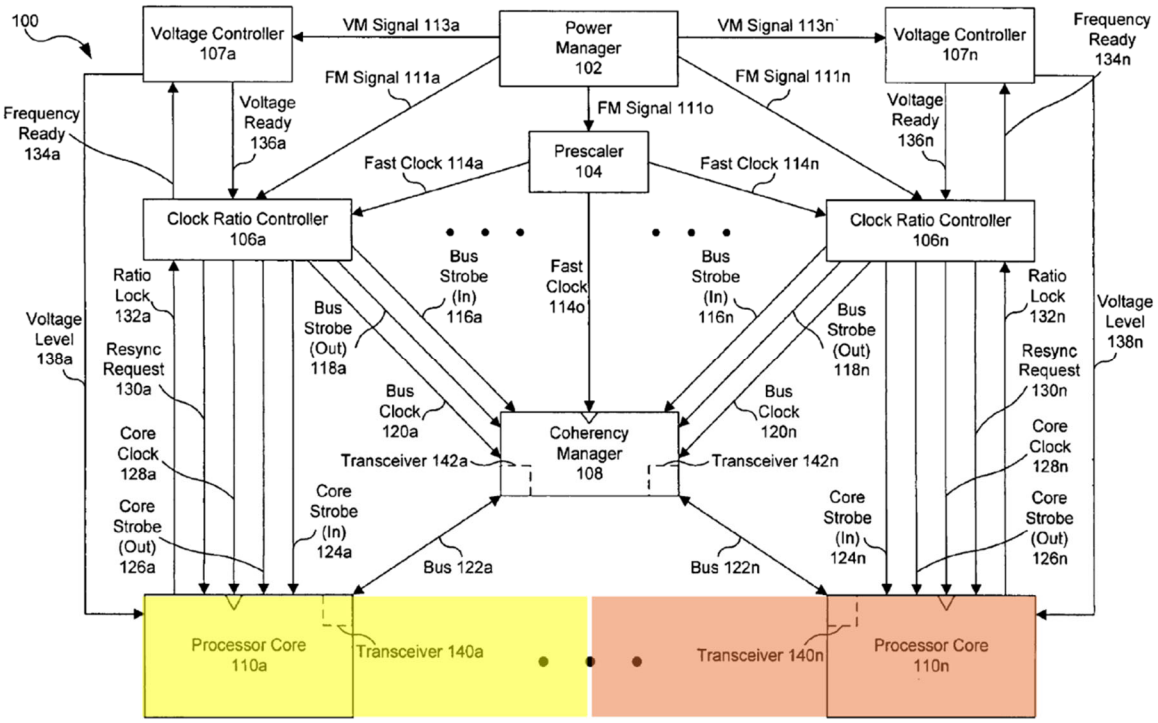


FIG. 1A of Knoth, annotated

The first set of cores (core 110a and associated cores 110b-i) are located, for instance, in the physical space depicted below in red dotted box; the second set of cores (core 110n and associated cores 110j-n) are located in the physical space depicted below in green dotted box. As such, Knoth includes a first region corresponding to the physical location reflected by the red dotted box, and a second region corresponding to the physical location reflected by the green dotted box.

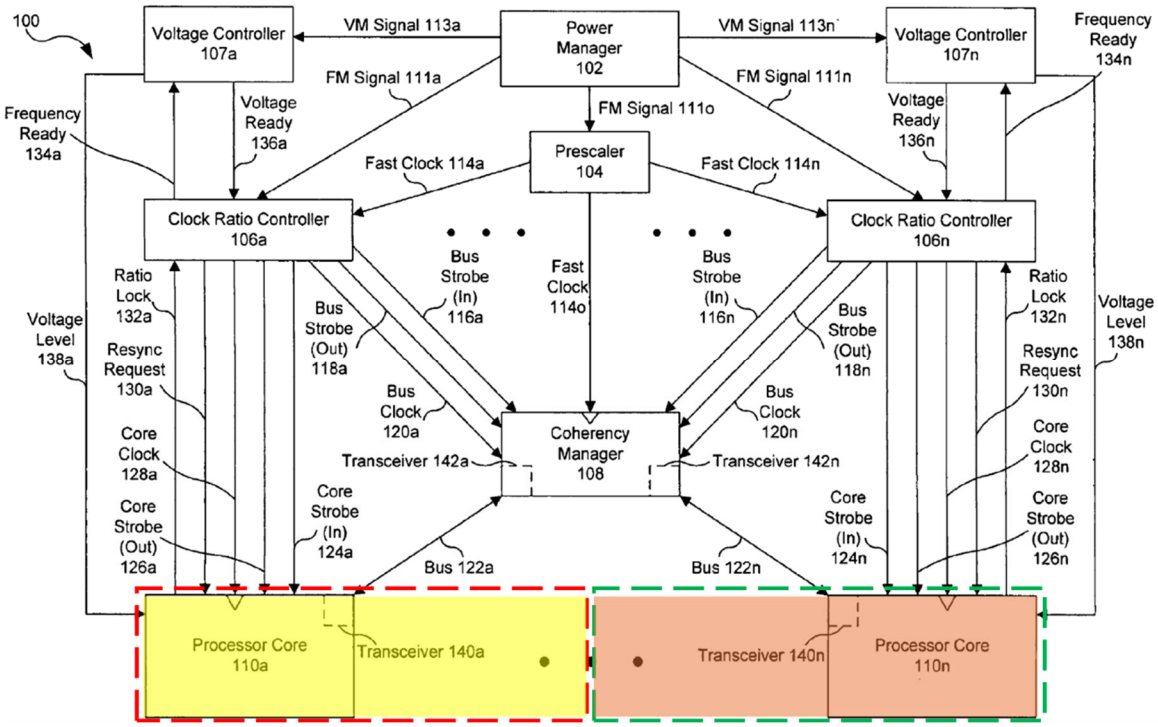


FIG. 1A of Knoth, annotated

Alternatively, for instance, the first set of cores (core 110a and associated cores 110b-i) are located in the physical space depicted below in purple dotted box; the second set of cores (core 110n and associated cores 110j-n) of Knoth are located in the physical space depicted below in blue dotted box. As such, Knoth includes a first region corresponding to the physical location reflected by the purple dotted box, and a second region corresponding to the physical location reflected by the blue dotted box.

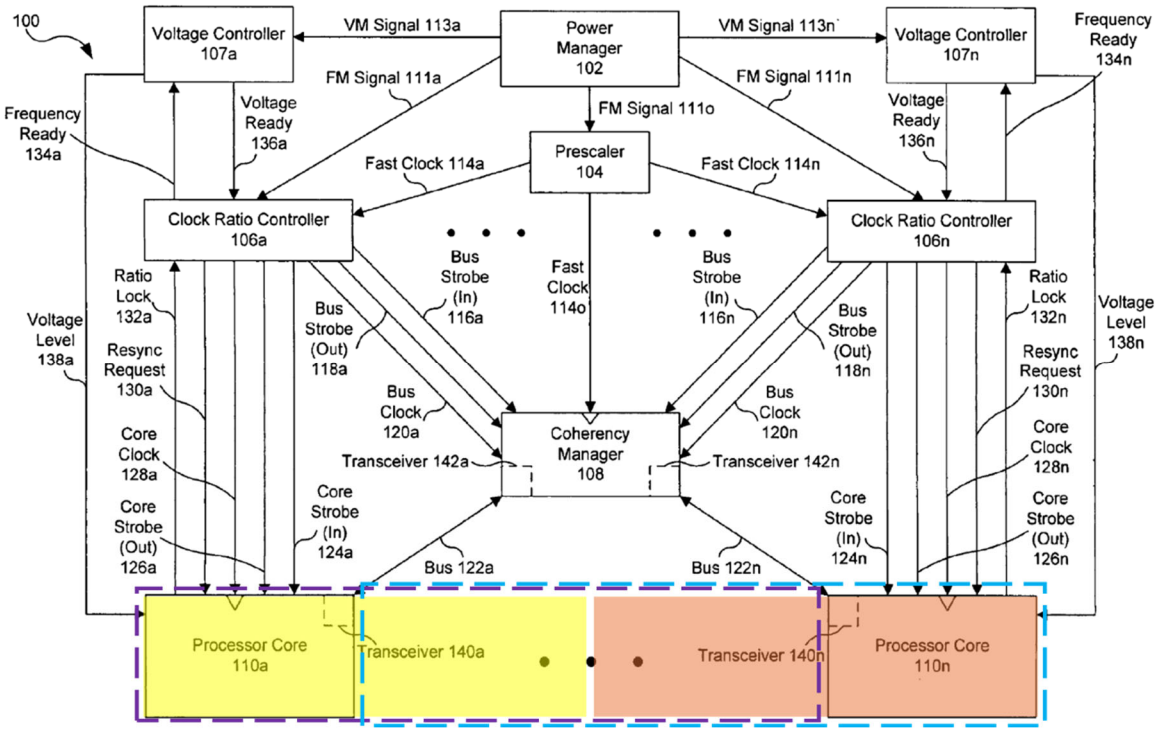


FIG. 1A of Knoth, annotated

Allarey also discloses this limitation. Ex[1003], ¶¶ 167-170. The multi-core processor system of Allarey comprises multiple cores physically located on two sites. *See, e.g.*, Ex[1006] at 1:52-53, 5:13-33. As discussed above, the multi-core processor of Allarey includes the first set of processor cores (e.g., core 0 (308), core 1 (310), core 2 (312), and core 3 (314)) and the second set of processor cores (e.g., core 4 (316), core 5 (318), core 6 (320), and core 7 (322)).

The first set of cores (core 0 (308), core 1 (310), core 2 (312), and core 3 (314)) of Allarey are located in the physical space depicted below in red dotted box; the second set of cores (core 4 (316), core 5 (318), core 6 (320), and core 7 (322)) of

Allarey are located in the physical space depicted below in green dotted box. As such, Allarey includes a first region corresponding to the physical location where cores 0-3 are located (in red dotted box), and a second region corresponding to the physical location where cores 4-7 are located (in green dotted box).

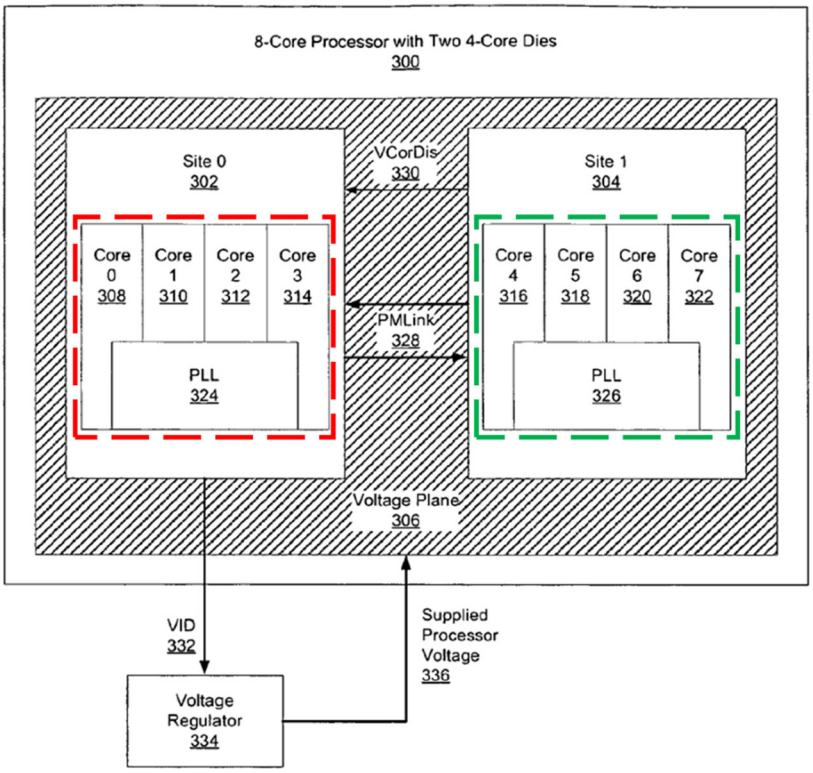


FIG. 3 of Allarey, annotated

Alternatively, the first set of cores (core 0 (308), core 1 (310), core 2 (312), and core 3 (314)) are located in the physical space depicted below in purple dotted box; the second set of cores (core 4 (316), core 5 (318), core 6 (320), and core 7 (322)) of Allarey are located in the physical space depicted below in blue dotted box.

As such, Allarey includes a first region where cores 0-6 are located, and a second region where cores 1-7 are located.

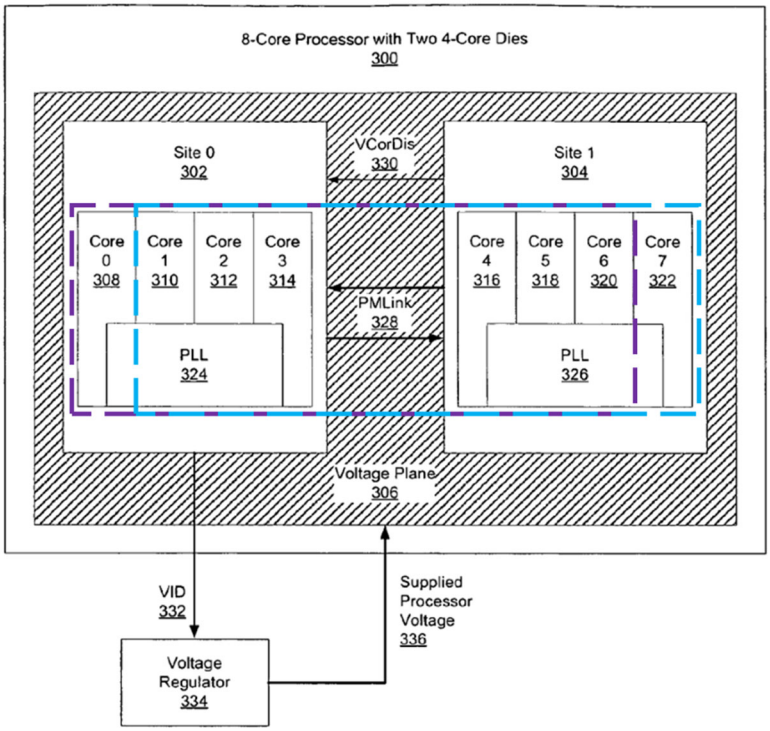


FIG. 3 of Allarey, annotated

E. Dependent Claim 9

1. 9[pre]

As explained above for Claim 8, Knoth and Allarey, alone or in combination, disclose each and every limitation of Claim 8.

2. 9[a]

As explained for Claim 8[a] in Ground 1, Knoth and Allarey, alone or in combination, disclose this limitation. Ex[1003], ¶¶ 162-171, 173-175.

Again, in Knoth, as depicted below the first set of cores (highlighted in yellow) are located in the physical space in purple dotted box; the second set of cores (highlighted in orange) are located in the physical space in blue dotted box. The first and second regions share some physical space and thus are overlapping.

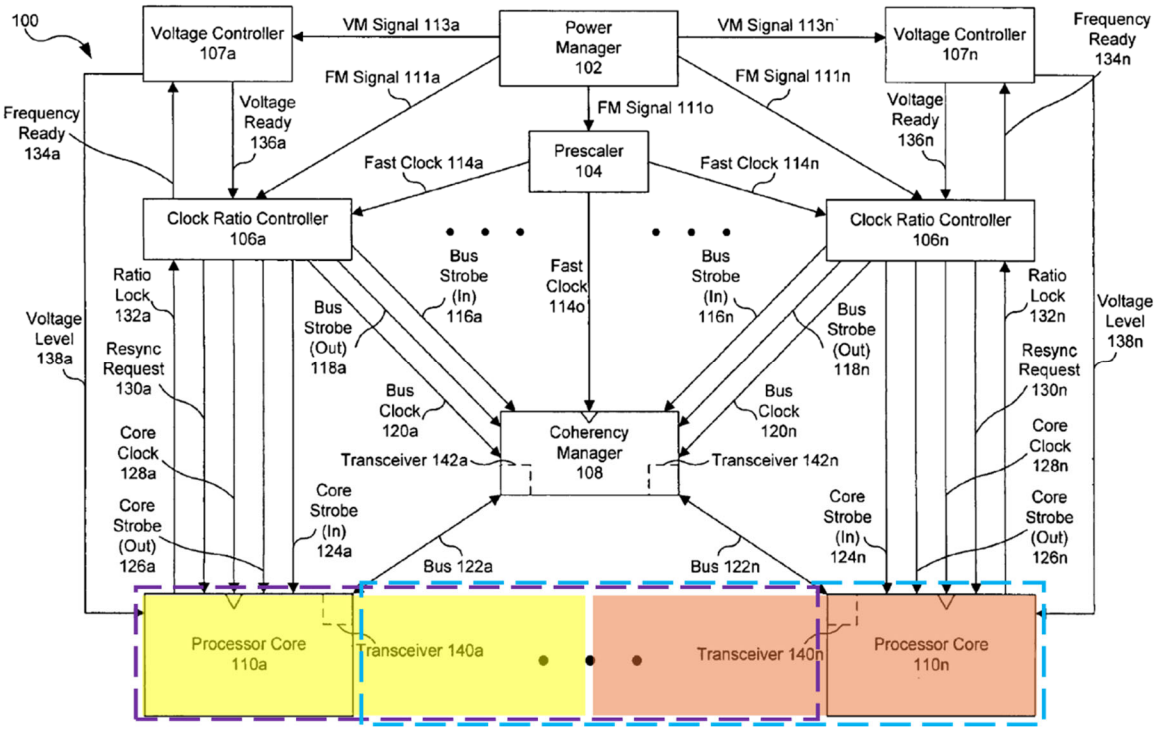


FIG. 1A of Knoth, annotated

In Allarey, as depicted below, the first set of cores (e.g., core 0 (308), core 1 (310), core 2 (312), and core 3 (314)) are located in the first region in purple dotted box; the second set of cores (core 4 (316), core 5 (318), core 6 (320), and core 7 (322)) of Allarey are located in the second region in blue dotted box. The first and second regions share some physical space and thus are overlapping.

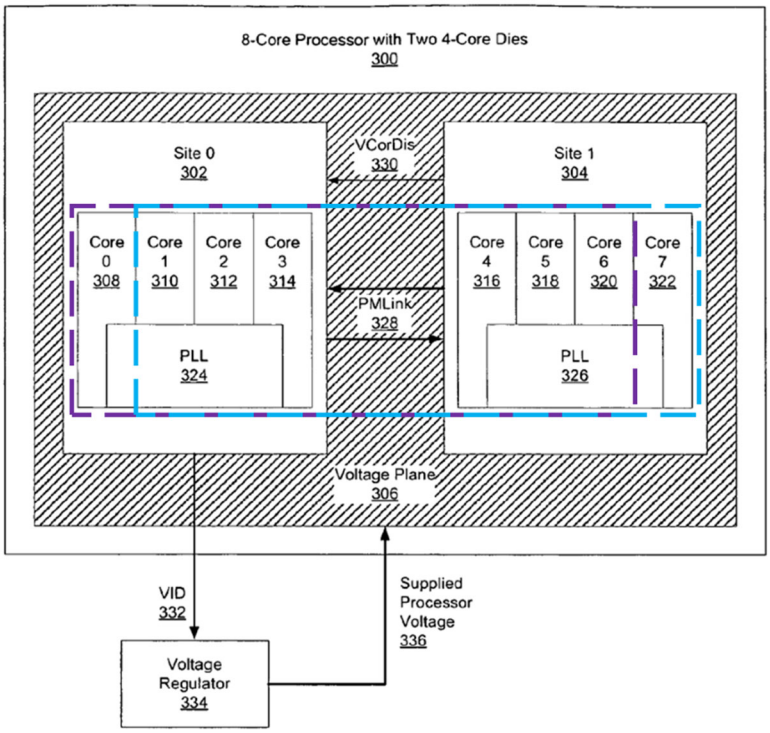


FIG. 3 of Allarey, annotated

F. Dependent Claim 10

1. 10[pre]

As explained above for Claim 8, Knoth and Allarey, alone or in combination, disclose each and every limitation of Claim 8.

2. 10[a]

As explained for Claim 8[a] in Ground 1, Knoth and Allarey, alone or in combination, disclose this limitation. Ex[1003], ¶¶ 162-171, 177-179.

Again, in Knoth, as depicted below, the first set of cores (highlighted in yellow) are located in the physical space in red dotted box; the second set of cores (highlighted in orange) of Knoth are located in the physical space in green dotted

box. The first and second regions are separate in physical layout and thus are non-overlapping.

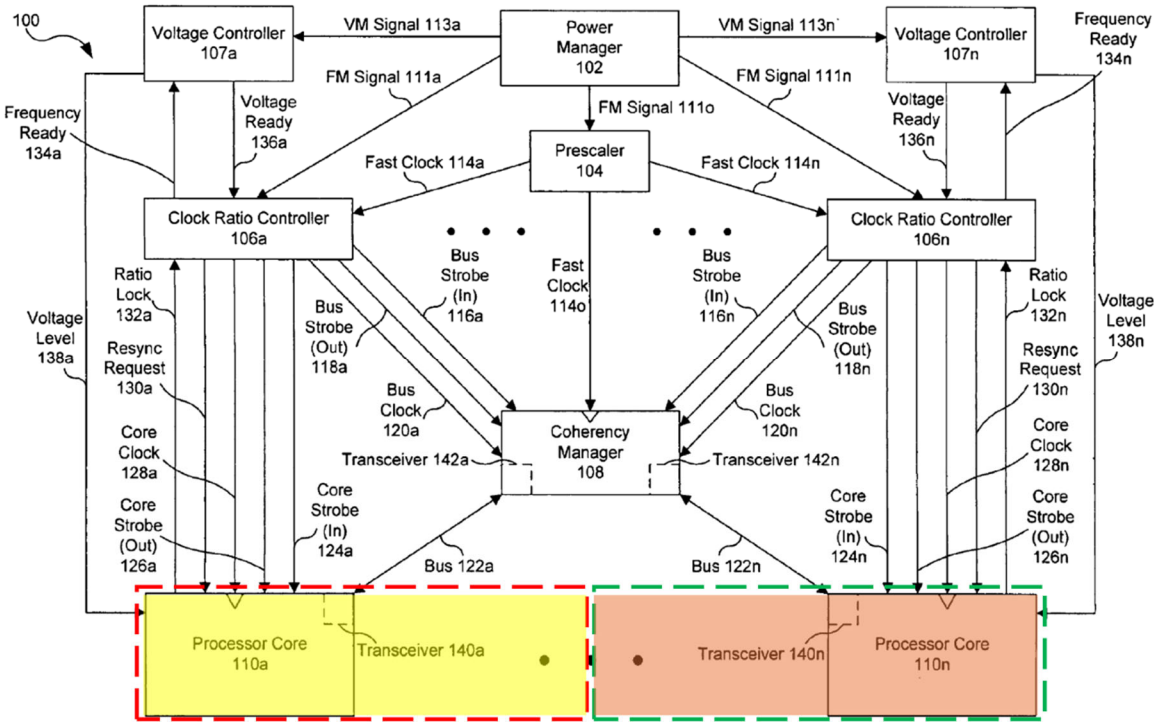


FIG. 1A of Knoth, annotated

In Allarey, as depicted below, the first set of cores (core 0 (308), core 1 (310), core 2 (312), and core 3 (314)) are located in the first region in red dotted box; the second set of cores (core 4 (316), core 5 (318), core 6 (320), and core 7 (322)) of Allarey are located in the second region in green dotted box. The first and second regions are separate in physical layout and thus are non-overlapping.

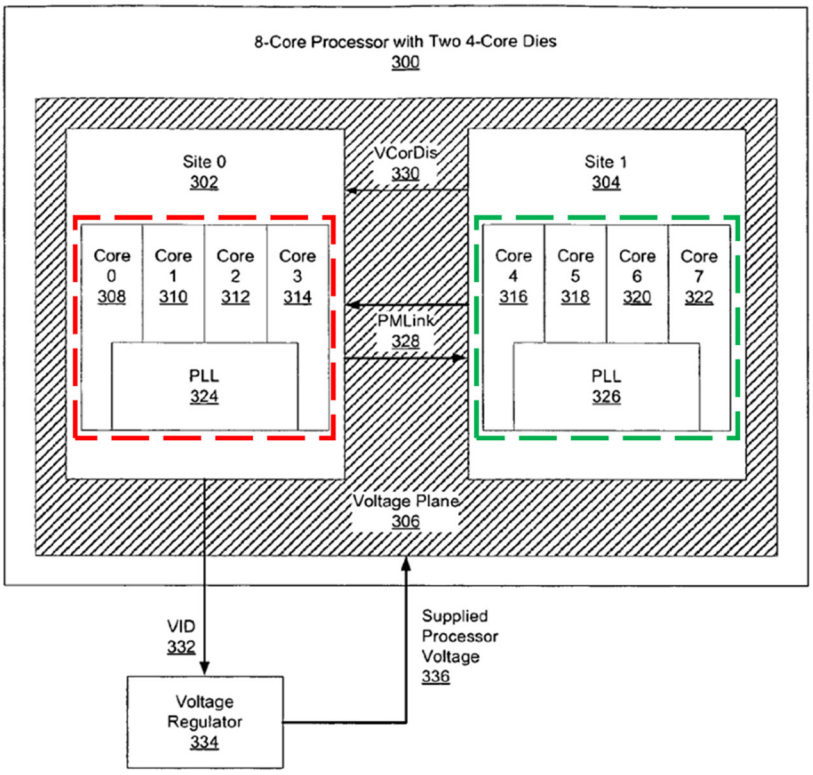


FIG. 3 of Allarey, annotated

G. Dependent Claim 14

1. 14[pre]

As explained above for Claim 1, Knoth and Allarey, alone or in combination, disclose each and every limitation of Claim 1.

2. 14[a]

As explained for Claim 5[a] in Ground 1, Knoth discloses this limitation. Ex[1003], ¶¶ 150-152, 181-183. Knoth discloses the control blocks in the form of power management unit 102 (highlighted in red) and clock ratio controllers 106a-n, as depicted below. *Id.*

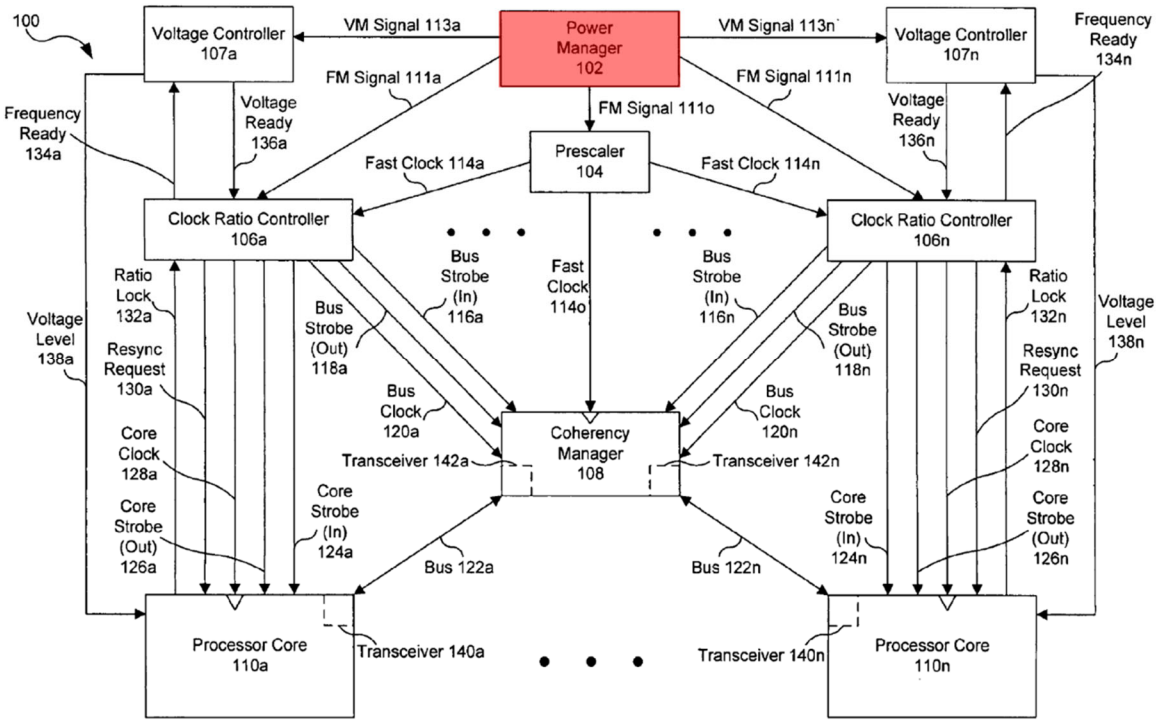


FIG. 1A of Knoth, annotated

As reviewed for Claim 8 in Ground 1, the '339 Patent provides that a "region" is simply a spatial grouping of cores. Power management unit 102 is positioned centrally relative to the first and second sets of cores Knoth (illustrated by processor core 110a and processor core 110n). *Id.*, ¶ 182.

Furthermore, as explained for Claim 5 in Ground 1, it was a known and obvious design option for a PHOSITA to place the control blocks of Knoth in a common region central to the first and second sets of processor cores. *Id.*, ¶ 183.

Allarey also discloses this limitation. *Id.*, ¶¶ 184-185. Allarey discloses the control blocks in the form of the logic within site 0 (102) and voltage regulator 126.

The logic within site 0 must be part of the circuitry within site 0. A PHOSITA would have understood that the logic within site 0 could be, for example, positioned towards the boundary of site 0 on the side of core 1, thus located substantially central to the first set of cores (illustrated by core 0 (108) and core 1 (110)) and the second set of cores (illustrated by core 0 (112) and core 1 (114)), as illustrated below by the red arrow. Ex[1003], ¶ 184.

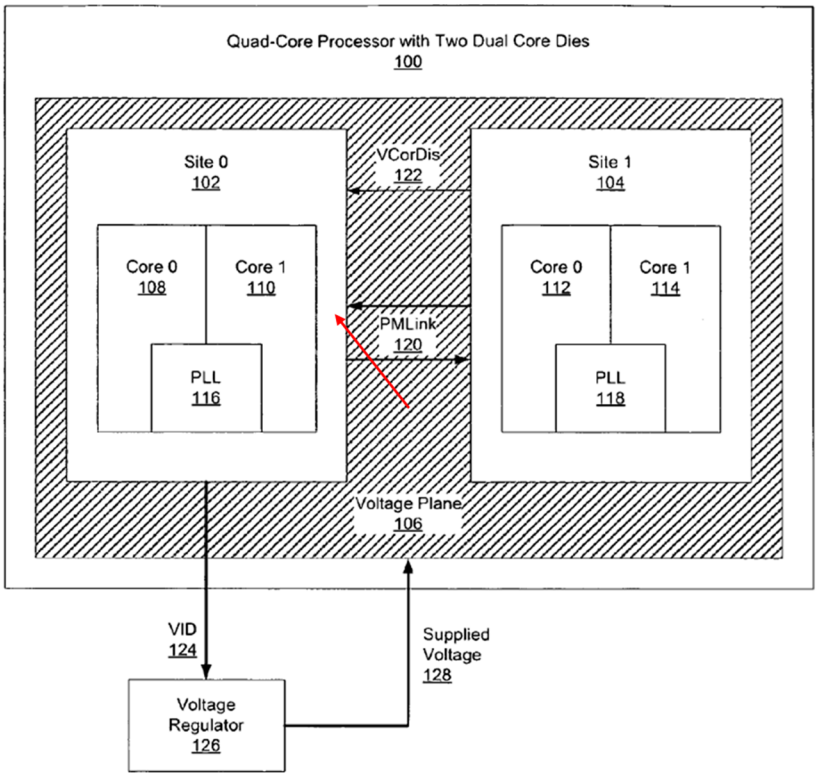


FIG. 1 of Allarey, annotated

Furthermore, as explained for Claim 5 in Ground 1, it was a known and obvious design option for a PHOSITA to place the control blocks of Allarey in a common region central to the first and second sets of processor cores. *Id.*, ¶ 185.

H. Independent Claim 21

1. 21[pre]

To the extent the preamble is limiting, for the same reasons described for Claim 1[Preamble] in Ground 1, Knoth and Allarey, alone or in combination, disclose a multi-core processor. Ex[1003], ¶ 186.

2. 21[a1]

For the same reasons described for Claim 1[a1] in Ground 1, Knoth and Allarey, alone or in combination, disclose this limitation. Ex[1003], ¶ 187.

3. 21[a2]

For the same reasons described for Claim 1[a2] in Ground 1, Knoth and Allarey, alone or in combination, disclose "wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage" and "a first output clock signal from a first phase lock loop (PLL) having a first clock signal as input."

Knoth further discloses a power control block in the form of voltage controllers 107a-n (shown in dashed blue block) and a clock control block in the form of clock ratio controllers 106a-n (shown in dashed purple block). Ex[1005] at [0027], [0031]; Ex[1003], ¶ 189. Again, Knoth discloses that each processor core 110(a-n) receives its respective supply from voltage controller 107(a-n) and its respective output clock signals core clock signal 128(a-n) output from PLL 202 in

clock ratio controller 106(a-n). Ex[1005] at [0027], [0031]; Ex[1003], ¶ 189.

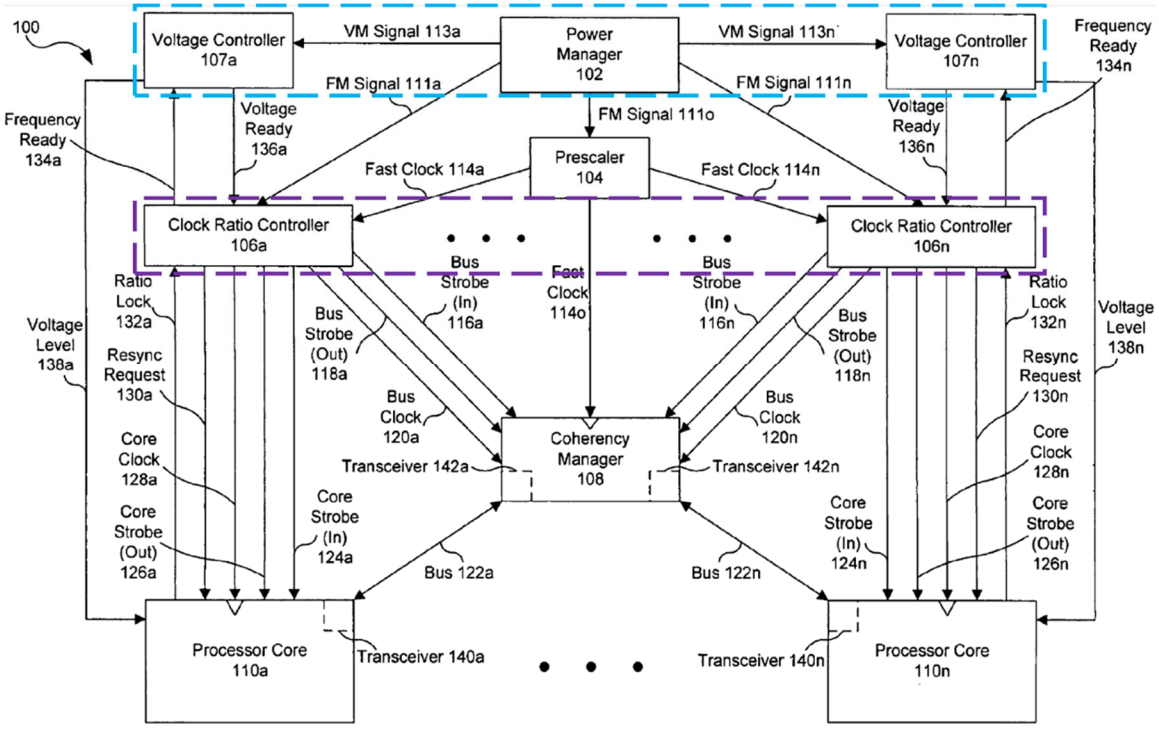


FIG. 1A of Knoth, annotated

Allarey further discloses a power control block in the form of voltage plane 106/306 (highlighted in red) and a clock control block in the form of PLL circuits 116 and 118 (or 324 and 326) (shown in dashed purple block). *Id.*, ¶ 190. Again, Allarey discloses that the first set of processor cores (e.g., core 0 (108) and core 1 (110) in site 0 (102)) receives the first supply voltage from voltage plane 106, and the first output clock signal from PLL 116 in the PLL circuits that includes PLL 116 and 118. Ex[1006] at 2:41-44, 3:59-3:24. The second set of processor cores (for example, core 0 (112) and core 1 (114) in site 1 (104)) receives the second supply

voltage from voltage plane 106, and the second output clock signal from PLL 118 in the PLL circuits that includes PLL 116 and 118. *Id.*

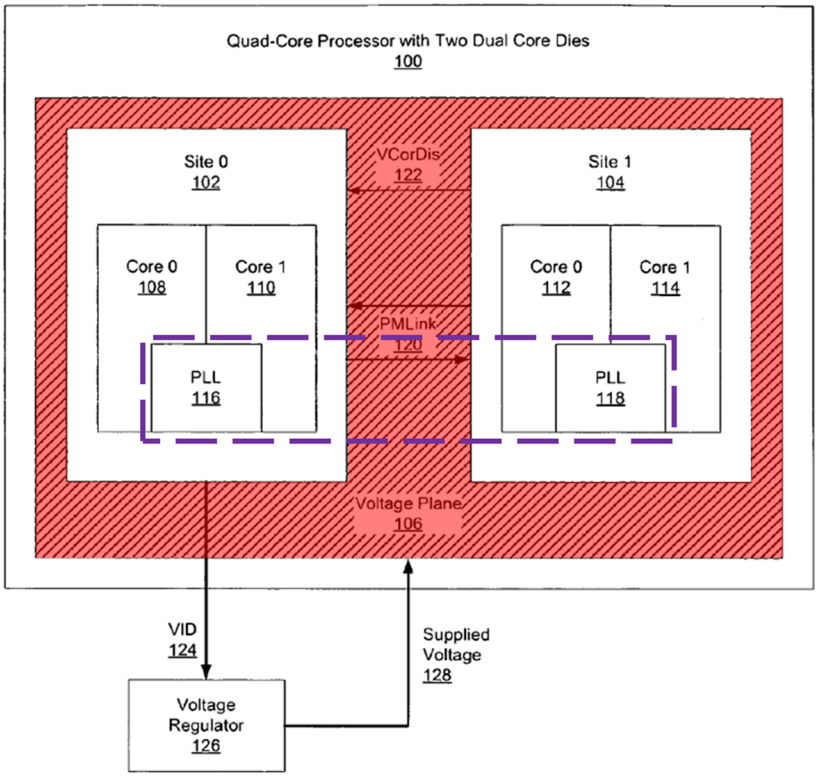


FIG. 1 of Allarey, annotated

4. 21[b1]

For the same reasons described for Claim 1[b1] in Ground 1 and as explained for Claim 21[a1] in Ground 1, Knoth and Allarey, alone or in combination, disclose this limitation.

5. 21[b2]

For the same reasons described for Claim 1[a2], [b2] and Claim 21[a2] in Ground 1, Knoth and Allarey, alone or in combination, disclose this limitation.

6. 21[b3]

For the same reasons described for Claim 1[b3] in Ground 1, Knoth and Allarey, alone or in combination, disclose this limitation.

7. 21[b4]

For the same reasons described for Claim 1[b4] in Ground 1, Knoth and Allarey, alone or in combination, disclose this limitation.

8. 21[c1]

For the same reasons described for Claim 1[c1] in Ground 1, Knoth and Allarey, alone or in combination, disclose this limitation.

9. 21[c2]

For the same reasons described for Claim 1[c2] in Ground 1, Knoth and Allarey, alone or in combination, disclose this limitation.

IX. GROUND 2: CLAIMS 2-4 ARE OBVIOUS UNDER §103 OVER KNOTH AND ALLAREY IN VIEW OF FLAUTNER

Knoth and Allarey, alone or in combination, further in view of Flautner disclose each and every limitation of Claims 2-4.

A. Motivation To Combine Knoth, Allarey, And Flautner

A PHOSITA would have been motivated to combine Knoth and Allarey with Flautner. Ex[1003], ¶¶ 198-204.

To improve the coordination and communication efficiency between the processor cores managed by Knoth's and Allarey's interface block, a PHOSITA

would have been inclined to look beyond the teachings of these references to identify improved configurations as part of the normal course of his/her own research. *Id.*, ¶ 199. For example, a PHOSITA would have been inclined to seek references that cover specific components dedicated to the functions of clock synchronization and level shifting because the processor cores in Knoth and Allarey operate in different voltage domains with different voltage levels and at different frequencies. *Id* . Knoth and Allarey expressly indicate the need for the interface block to perform these functions. *See, e.g.*, Ex[1005] at [0002] ("communications and the exchange of data between various components are disrupted until a resynchronization occurs"), [0029]; Ex[1006] at 1:23-24 ("Asynchronous voltage changes during this time may disrupt a PLL lock process.").

Flautner, like Knoth and Allarey, discloses technology in the field of multi-core processor systems, specifically addressing the challenges of managing different operational states and power domains within such systems. *See, e.g.*, Ex[1007] at [0047]-[0048] & Fig. 4. Flautner discloses the specific details of the components to handle clock synchronization and voltage level shifting between cores operating at different supply voltages and frequencies. *Id.*; Ex[1003], ¶¶ 200-202.

Applying these teachings to Knoth and Allarey does not require substantial changes and would yield predictable results because such changes amount to a

simple combination of known parts. Ex[1003], ¶ 203. In Knoth's architecture, the addition of Flautner's synchronization module and voltage level shifter would seamlessly integrate into the existing system of independent clock and voltage controllers, enhancing the system's capability to handle cores operating under diverse conditions. *Id.* Similarly, in Allarey's structure, incorporating Flautner's components would address the potential voltage mismatches between sites and improve overall communication efficiency, ensuring that signals are properly synchronized and translated between cores, regardless of their voltage and frequency differences. *Id.*

B. Claim 2

1. 2[pre]

As explained above for Claim 1, Knoth and Allarey, alone or in combination, disclose each and every limitation of Claim 1.

2. 2[a]

Flautner teaches the use of a level shifter. Ex[1003], ¶¶ 206-210. Flautner discloses that the first processor core 40 and the second processor core 42 within separate voltage domains receiving different supply voltage levels. Ex[1007] at [0047]-[0048]. A voltage level shifter 52 is provided between the first processor core 40 and the second processor core 42 to "deal with … the different supply voltage levels (voltage signaling levels) between the two domains." *Id.* Voltage level shifter

52 thus translates the voltage of a signal from the cores in one voltage domain to the expected level associated with the cores in the other domain.

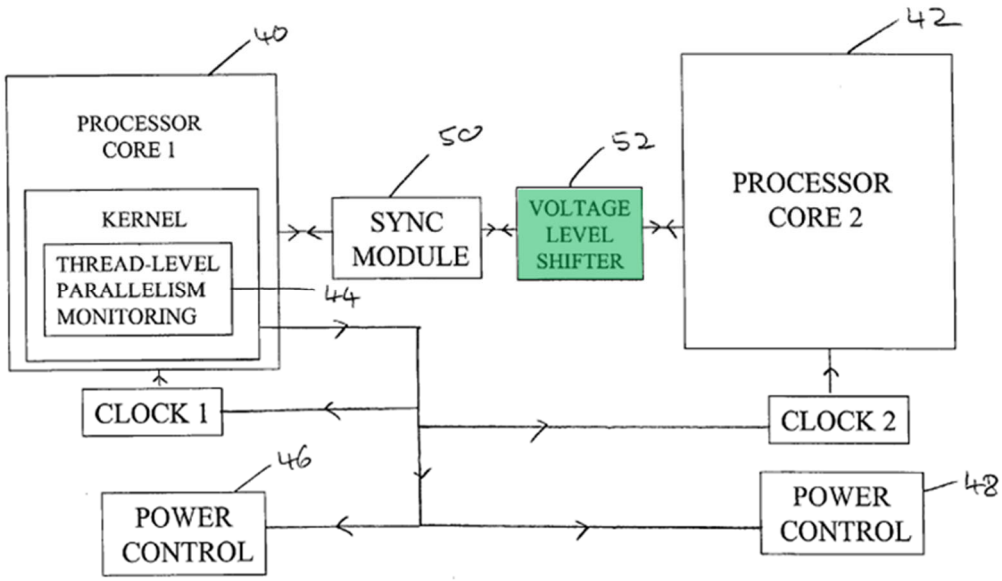


Fig. 4 of Flautner, annotated

A PHOSITA reading Flautner would have understood that translating voltage levels inherently involves translating the corresponding logic levels associated with the cores. Ex[1003], ¶¶ 207-209. When a signal is transmitted between cores operating with different voltage levels, the signal's logic levels may not match the expected input levels of the receiving domain. *Id*. If a signal crosses from one domain to another without adjusting its voltage, it could be misinterpreted by the receiving core. *Id*. Therefore, a voltage level shifter must adjust the signal's voltage so that a logic '1' or '0' in one core remains a logic '1' or '0' in the other core, preserving the intended logic state despite different voltage requirements. *Id.*

To the extent it is argued or found that voltage level shifter 52 has the shared functions between the processor cores in two voltage domains, it would have been obvious to a PHOSITA that voltage level shifter 52 could have separate level shifter modules for the core(s) in each voltage domain because level shifters are standard, routine components and Flautner already has it in the multi-core processor system, and because adding a known level shifter in the processor layout of Knoth or Allarey would require this simple modification. *Id.*, ¶ 210. A PHOSITA would also be motivated to provide dedicated level shifters for each domain to further improve precision of voltage translation across voltage domains. *Id*.

C. Dependent Claim 3

1. 3[pre]

As explained above for Claim 1, Knoth and Allarey, alone or in combination, disclose each and every limitation of Claim 1.

2. 3[a]

For the same reasons described for Claim 2[a] in Ground 2, Flautner discloses this limitation. Accordingly, Knoth and Allarey, further in view of Flautner, disclose each and every limitation of Claim 3. Ex[1003], ¶¶ 211-212.

D. Claim 4

1. 4[pre]

As explained for Claim 1 in Ground 1, Knoth and Allarey, alone or in

combination, disclose each and every limitation of Claim 1.

2. 4[a]

Flautner teaches the use of a synchronizer. *Id.*, ¶¶ 214-215. Specifically, Flautner discloses that a "synchronisation module 50" is provided between the first processor core 40 and the second processor core 42. Ex[1007] at [0048]. The first processor core 40 and the second processor core 42 are "asymmetrically controlled by the clock speed controller 44" that supplies "clocks of different speeds … to respective ones of the first processor core 40 and the second processor core 42." *Id.* at [0047]. The synchronisation module "deal[s] with clock synchronisation issues" between the first processor core 40 and the second processor core 42 running at different clock speeds. *Id.* at [0048].

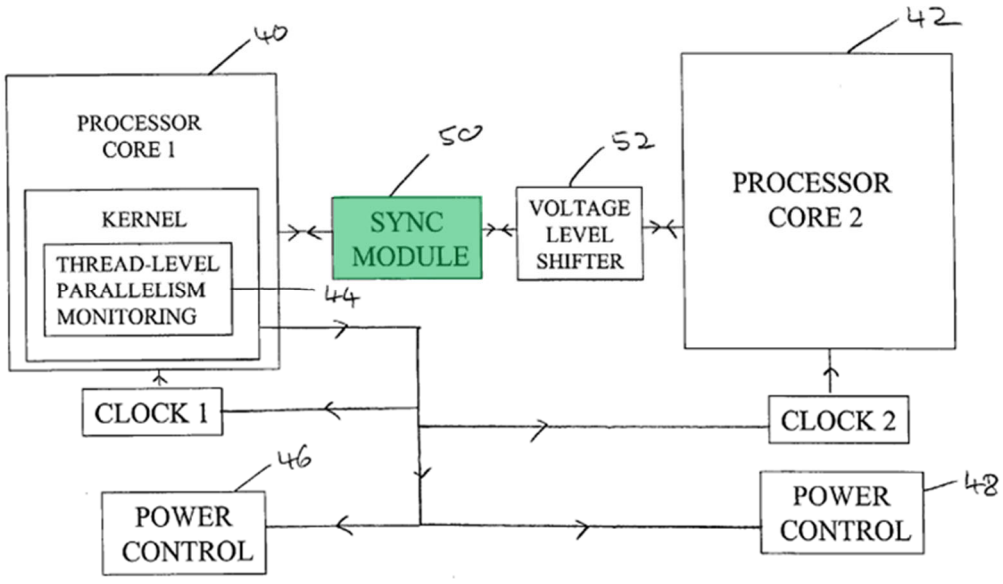


Fig. 4 of Flautner, annotated

A PHOSITA would have understood that, to facilitate communication between the first and second cores of Knoth and Allarey, the clock signals of the two cores would necessarily be required to be synchronized. Ex[1003], ¶ 215. When two cores operate at different clock speeds, the timing of signal transfers between the cores will not align. *Id.* Synchronizing clock signals is necessary to make sure the communication from one core is recognized and correctly interpreted by the other core. *Id.* Synchronisation module 50 of Flautner thus synchronizes the clock signals of the first and second cores for communication between the first and second cores, as would be required in the systems of Knoth and Allarey. *Id*.

X. GROUND 3: CLAIM 6 IS OBVIOUS UNDER §103 OVER KNOTH AND ALLAREY IN VIEW OF WOLFE, AND FURTHER IN VIEW OF KUMAR

Knoth and Allarey, alone or in combination, in view of Wolfe, and further in view of Kumar, disclose each and every limitation of Claim 6.

A. Motivation to Combine Knoth, Allarey, and Wolfe

A PHOSITA would have been motivated to combine Knoth and Allarey with Wolfe. Ex[1003], ¶¶ 217-218.

A PHOSITA would have recognized that Knoth and Allarey focus more on functional mechanisms for dynamic voltage and frequency regulation in a multi-core processor system. *Id*. It would have been in the best interest of a PHOSITA to

explore complementary configurations that optimize the physical layout of the multi-core processor system to support these mechanisms. *Id*. Wolfe discloses a grid organization and relevant physical layout considerations for a multi-core processor having independent control mechanisms for dynamic management of voltage and frequency levels. *See, e.g.*, Ex[1008] at [0014]. This structured layout would prompt a PHOSITA to consider combining the functional mechanisms disclosed by Knoth and Allarey with the physical layout strategy of Wolfe to achieve a multi-core processor system that maximizes both operational efficiency and performance. Ex[1003], ¶ 218.

B. Motivation to Combine Knoth, Allarey, and Kumar

A PHOSITA would have been motivated to combine Knoth and Allarey with Kumar. To improve the power management and inter-core voltage regulation of Knoth's and Allarey's multi-core processor systems, a PHOSITA would have been inclined to look beyond the teachings of these references to identify improved configurations as part of the normal course of his/her own research. Ex[1003], ¶ 219. A PHOSITA would have been inclined to seek references that cover specific mechanisms for inter-core voltage regulation in a multi-core processor. *Id*.

As discussed for Claim 5 in Ground 1, Knoth and Allarey disclose control blocks for managing voltage and frequency independently for processor cores. *See,*

e.g., Ex[1005] at [0025], Ex[1006] at 2:65-3:19. Kumar, like Knoth and Allarey, discloses a power management system in the context of integrated circuits. Kumar discloses additional details for dynamically managing the respective voltage supplies within predetermined voltage relationships to optimize the overall power distribution and performance. Ex[1009] at [0054]-[0060]. A POSITA would have been motivated to combine Knoth and Allarey further with Kumar because Kumar's teaching could improve Knoth's and/or Allarey's system by providing a more granular control of voltage levels across different sets of cores to improve voltage stability and power efficiency. Ex[1003] at ¶ 220.

Applying these teachings from Kumar to Knoth and Allarey does not require substantial changes and would yield predictable results because such changes amount to a simple combination of known parts. *Id.*, ¶ 221.

C. Claim 6

1. 6[pre]

As explained above for Claim 5, Knoth and Allarey, alone or in combination, disclose each and every limitation of Claim 5.

2. 6[a]

Knoth and Allarey, alone or in combination, disclose "wherein the first set of processor cores is adjacent to the second set of processor cores." Ex[1003], ¶¶ 223-225.

Knoth discloses that processor cores 110a-n are placed adjacent to each other, as depicted below.

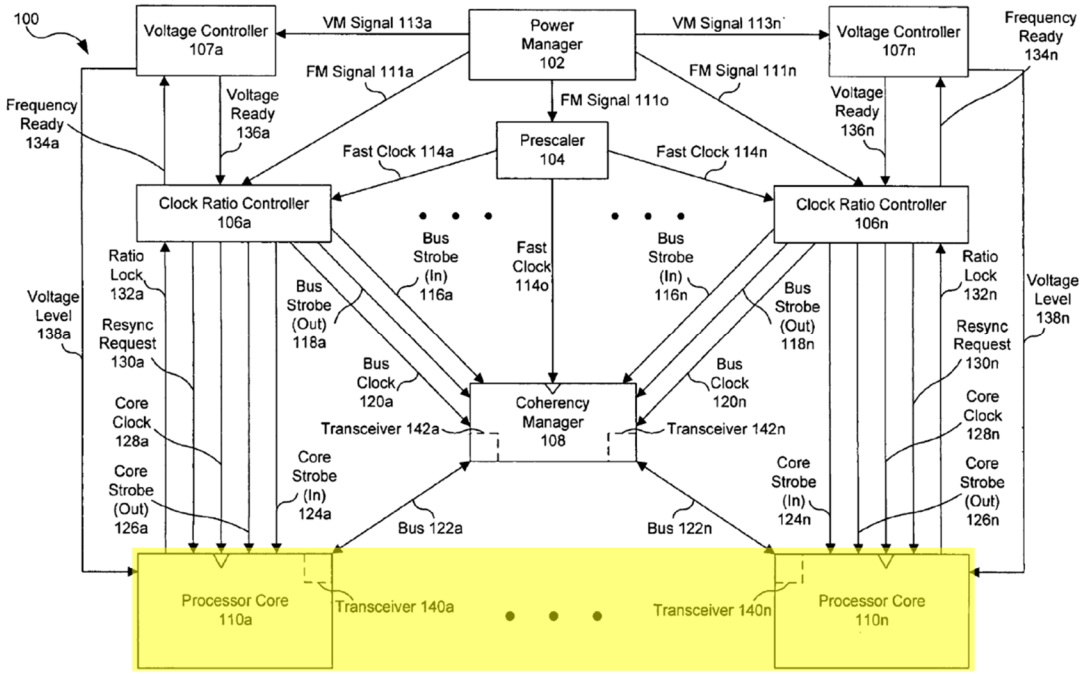


Fig. 1A of Knoth, annotated

Allarey likewise discloses that the cores in sites 0 and 1 are adjacent as depicted below.

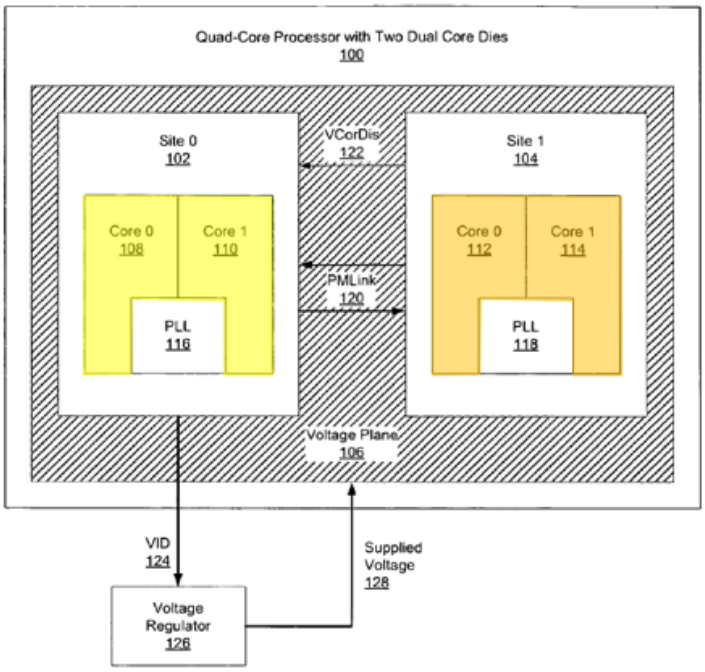


FIG. 1 of Allarey, annotated

Wolfe also discloses this limitation. Ex[1003], ¶¶ 226-227. Wolfe discloses a grid organization of processor cores—the processor cores of a multi-core processor may be "arranged in rows and columns in a 2-dimensional array." Ex[1008] at [0014], Figure 1. Wolfe also discloses grouping cores based on geometric mapping. *Id.* at [0016], [0022]; Ex[1003], ¶ 226. The first set of cores of the multi-core processor could be, for example, located in a first region corresponding to a row of the two-dimensional array (highlighted in yellow), and the second set of cores in a second region corresponding to an adjacent row of the array (highlighted in orange). *Id.*, ¶ 227.

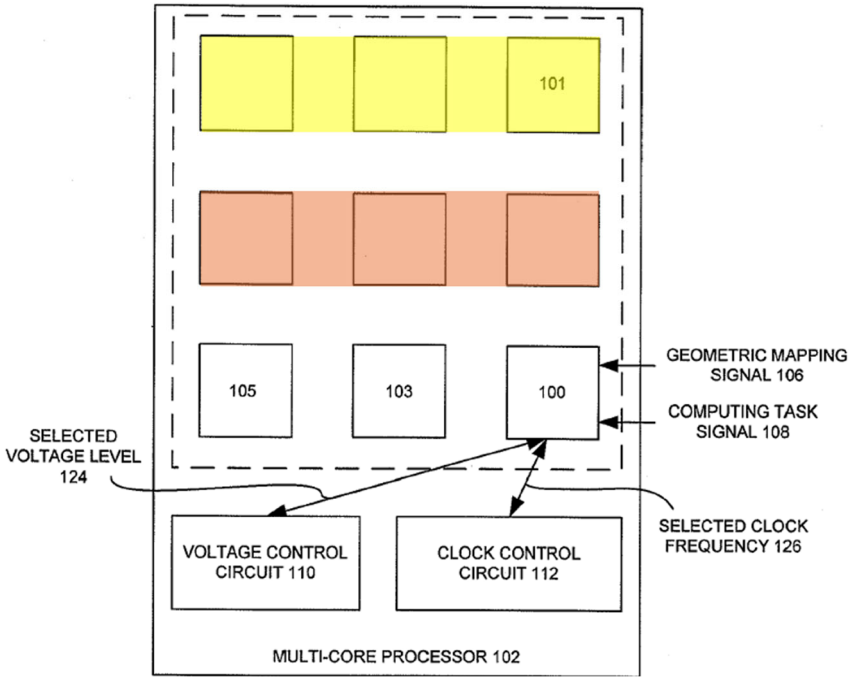


Figure 1 of Wolfe, annotated

3. 6[b]

Kumar discloses this limitation. Ex[1003], ¶¶ 228-229. Kumar discloses managing and maintaining a differential relationship between the voltages of two sets of components using a controller. Kumar discloses a controller 540 that controls "generat[ing] a voltage V1 across one or more components 130 and … a voltage V2 across one or more components 530, wherein voltage V1 is to satisfy one or more predetermined relationships with voltage V2." Ex[1009] at [0054]. "If voltage V1 and voltage V2 do not satisfy one or more predetermined relationships," including "whether the absolute value of the difference between voltage V1 and voltage V2 is less than, or less than or equal to, a predetermined amount or a predetermined

percentage of either voltage V1 or voltage V2," controller 540 makes adjustments to "help voltage V1 and voltage V2 satisfy one or more predetermined relationships." *Id.* at [0058]-[0060]. The architecture disclosed by Kumar is applicable to a multi-core processor system. *See, e.g.*, *id.* at [0073].

XI. GROUND 4: CLAIM 11 IS OBVIOUS UNDER 35 U.S.C. § 103 OVER KNOTH AND ALLAREY IN VIEW OF WOLFE

Knoth and Allarey, in view of Wolfe, disclose each and every limitation of Claim 11.

1. 11[pre]

As explained for Claim 8 in Ground 1, Knoth and Allarey, alone or in combination, disclose each and every limitation of Claim 8.

2. 11[a]

For the same reasons described for Claim 6[a] in Ground 3, a PHOSITA reading Wolfe would have understood that the first set of cores of the multi-core processor thus could be located in a first region corresponding to a first row of the two-dimensional array (highlighted in yellow), and the second set of cores in a second region corresponding to a second row of the array (highlighted in orange). Ex[1003], ¶ 232.

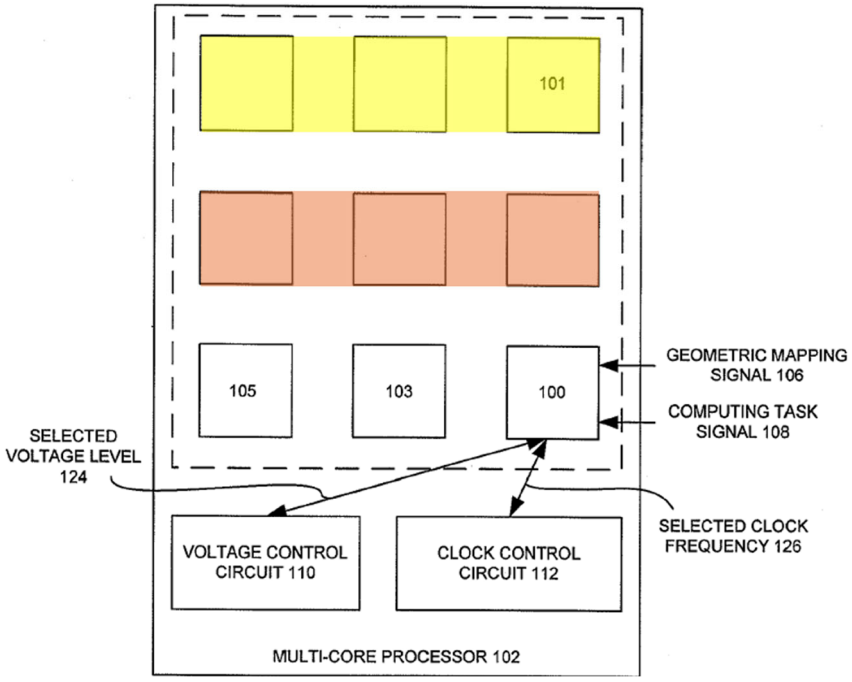


Figure 1 of Wolfe, annotated

XII. GROUND 5: CLAIMS 1-3, 5, 8-10, 14 AND 21 ARE OBVIOUS UNDER 35 U.S.C. § 103 OVER NAFFZIGER IN VIEW OF ALLAREY

Naffziger and Allarey, alone or in combination, disclose each and every limitation of Claims 1-3, 5, 8-10, 14 and 21.

A. Motivation to Combine Naffziger and Allarey

A PHOSITA would have been motivated to combine Naffziger and Allarey and would have had a reasonable expectation of success in doing so, because they relate to the same well-known technologies. Ex[1003], ¶¶ 235-239.

Naffziger and Allarey are directed to the same field of multi-core processors, and address similar problems and propose similar solutions for managing voltage and frequency scaling of multi-core processors, similar to those disclosed in the '339

Patent. *Id.*, ¶ 236. For example, Naffziger seeks to propose solutions for multi-core processor systems' control over power consumption that include changing operational states with different power consumptions by adjusting the supply voltage, clock frequency and other parameters. *See* Ex[1005] at [0001]-[0012]. Allarey seeks to propose solutions for optimize multi-core processor systems' power conservation by dynamically modifying the voltage supplied to and the frequency of the processor. *See* Ex[1006] at 1:6-24.

Naffziger is authored by Advanced Micro Devices engineers, and Allarey by Intel engineers. Ex[1010], Ex[1006]. A PHOSITA would have looked to publications by such leading companies in designing multi-core processing systems, such as AMD and Intel, and considered the different techniques disclosed in these references for optimizing the power and/or performance of cores. Ex[1003], ¶ 237.

A PHOSITA would, at a minimum, have found the combination obvious to try because it combines well-known techniques that are inter-related—Naffziger deals with dynamic power and performance adjustments, and Allarey studies stabilizing a supplied voltage during a clock signal frequency locking process. *Id.*, ¶ 238. A PHOSITA would have found synergy in combining dynamic power adjustments from Naffziger with voltage stabilization from Allarey to improve overall processor performance and stability. *Id.*, ¶¶ 235-239.

Therefore, the teachings and considerations of Allarey would allow a PHOSITA to improve on Naffziger's systems effortlessly (and vice versa). For at least these reasons, a PHOSITA would have been motivated to seek and combine Naffziger and Allarey. *Id*.

B. Claim 1

1. 1[pre]

To the extent that the preamble is limiting, Naffziger teaches this subject matter. Ex[1003], ¶ 240. Naffziger discloses a processor that "includes one or more processor cores." Ex[1010] at [0008], [0055].

As explained for Claim 1[Preamble] in Ground 1, Allarey likewise teaches a multi-core processor.

2. 1[a1]

Naffziger and Allarey, alone or in combination, disclose this limitation. Ex[1003], ¶¶ 242-247.

Naffziger discloses that the multi-core processor has a first core 105A and a second core 105B "the operational states [of which are] controlled independently of one another." Ex[1010] at [0053]-[0054]. For the first and second cores 105A and 105B, Naffziger discloses a power control unit 150 with separate, independent supply voltage and clock signal control planes, or alternatively, multiple power control units each associated with a corresponding process core, that regulates their

core supply voltage and core clock frequency. *Id.* at [0022]-[0023], [0030], [0054]-[0055].

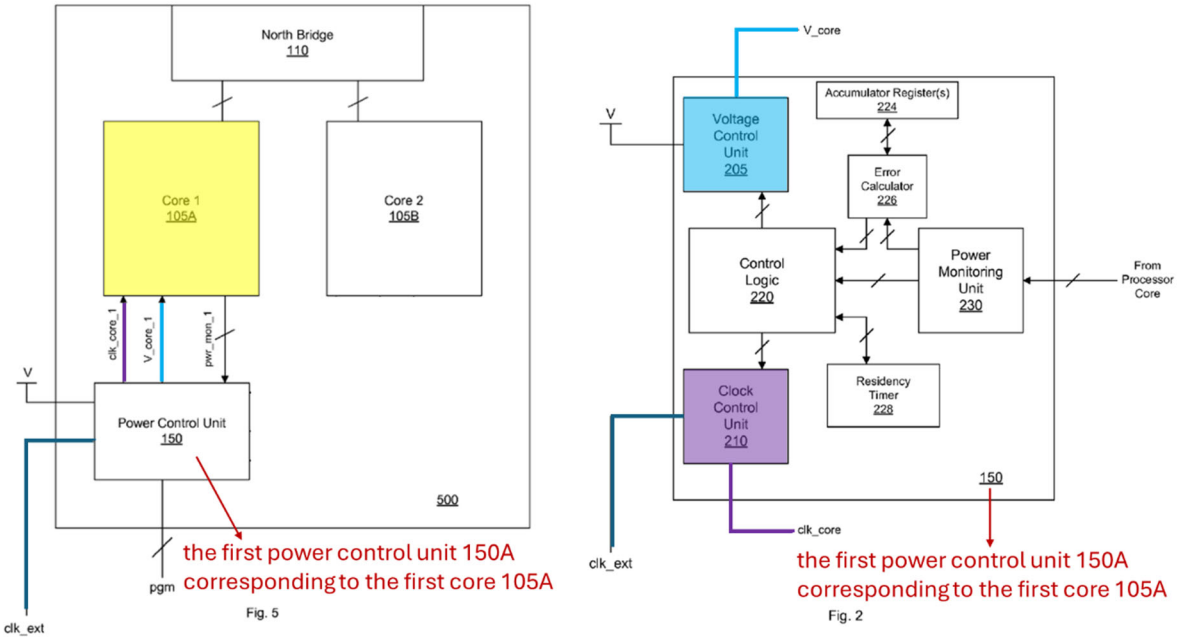
To the extent it is argued or found that the first and second cores 105A and 105B are individual cores, it would have been obvious to a PHOSITA to extend the disclosed architecture of Naffziger to include two distinct sets of cores, where each set of cores is monitored and controlled separately. Ex[1003], ¶ 244. For example, instead of managing individual cores, the system could treat core 105A and additional cores associated with it as a first set, while core 105B and its associated cores could form a second set. Each set would be monitored and controlled independently, allowing the system to fine-tune power consumption based on the specific demands of each set. *Id.*

Furthermore, a PHOSITA would have been motivated to modify Naffziger to have two sets of cores, rather two individual cores, based on the teachings as disclosed in Allarey. As explained for Claim 1[a1] in Ground 1, Allarey discloses a first set of processor cores in the form of a multi-core die in site 0. Ex[1006] at 2:41-58, 5:17-33.

3. 1[a2]

Naffziger discloses this claim limitation. Ex[1003], ¶¶ 248-253. Naffziger discloses that the first core 105A receives a first voltage supply "V_core_1" (shown

by blue lines) and a first output clock signal "clk_core_1" (shown by purple lines) of a phase locked loop (PLL) of the power control unit 150 (highlighted in purple) having a first clock signal "clk_ext" (shown by dark blue lines) as input. Further, Naffziger discloses that the multi-core processor system "includes multiple power control units, each of which is associated with a corresponding one of a plurality cores[, wherein] each power control unit may separately control the states of operation of its corresponding core." Ex[1010] at [0055]. A PHOSITA reading Naffziger would have understood that the multi-core processor 500 includes more than one power control unit 150 each associated with a corresponding core—a first power control unit 150 corresponding to the first core 105A (for ease of discussion, referred to as the "first power control unit 150A") and a second power control unit 150 corresponding to the second core 105B (for ease of discussion, referred to as the "second power control unit 150B"), as illustrated below in annotated Figs 2 and 5. Ex[1003], ¶ 250.



Figs. 2 and 5 of Naffziger, annotated

Naffziger discloses dynamically "adjust[ing] the core supply voltage or the frequency of the core clock signal." Ex[1010] at [0023]. Specifically, Naffziger discloses that the first power control unit 150A includes the voltage control unit 205 that "us[es] adjustable voltage regulator circuitry, level shifter circuity, or any other suitable circuitry configured to vary a supply voltage," including "V_core_1." *Id.* at [0032], Fig. 2 (above, annotated). Accordingly, Naffziger discloses that its first set of cores dynamically receives a first supply voltage ("V_core_1") that varies as adjusted by circuitry of the voltage control unit 205 of the first power control unit 150A.

Each power control unit 150 including the first power control unit 150A

further includes the clock control unit 210 that "us[es] a phase locked loop (PLL) … for adjusting the frequency of a clock signal" and "is configured to vary the frequency of the core clock signal" to dynamically provide a "core clock signal, clk_core, … to processor core 105," including "clk_core_1." *Id.* at [0033], Figs. 2 and 5 (above, annotated). Accordingly, Naffziger discloses that its first set of cores dynamically receives a first output clock signal ("clk_core_1") of a first PLL (the PLL used by the clock control unit 210 of the first power control unit 150A, shaded in purple).

The PLL of clock control unit 210 of the first power control unit 150A receives as an input "an external clock signal, clk_ext." *Id.* at [0033], Figs. 2 and 5 (above, annotated); *see also id.* at [0022] (each power control unit 150 "is coupled to receive an external clock signal, clk_ext.").

As explained for Claim 1[a2] in Ground 1, Allarey also discloses this limitation.

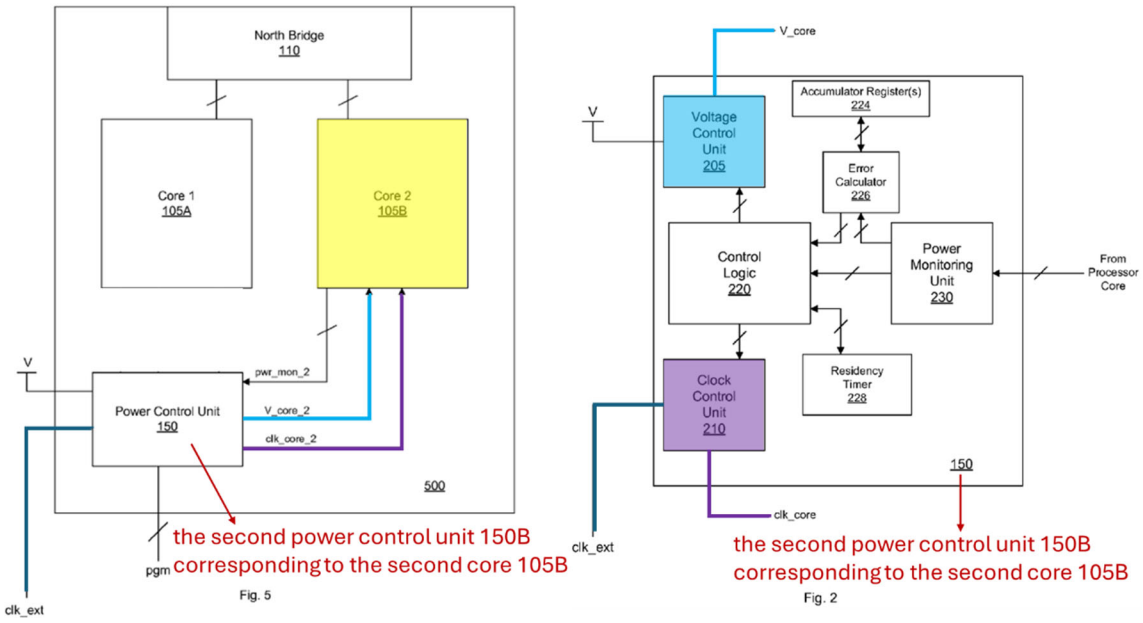
4. 1[b1]

As explained for Claim 1[a1] in Ground 5, Naffziger discloses "a second set of processor cores of the multi-core processor." Furthermore, to the extent it is argued or found that Naffziger does not disclose this limitation, a PHOSITA would have been motivated to modify the architecture of Naffziger to include a first and

second sets of cores in view of Allarey. Therefore, Naffziger and Allarey, alone or in combination, disclose this limitation. *See also* Ex[1003], ¶ 255.

5. 1[b2]

Naffziger discloses this limitation. Ex[1003], ¶¶ 256-260. As depicted in Figs. 2 and 5, Naffziger discloses that the second core 105B receives a second voltage supply "V_core_2" (shown by blue lines) and a second output clock signal "clk_core_2" (shown by purple lines) of a phase locked loop (PLL) of the second power control unit 150B (highlighted in purple) having a second clock signal "clk_ext" (shown by dark blue lines) as input.



Figs. 2 and 5 of Naffziger, annotated

The second core 105B of Naffziger receives the second voltage supply "V_core_2" and the second output clock signal "clk_core_2" from the power control

unit 150 (including the second power control unit 150B). As explained for Claim 1[a2] in Ground 5, Naffizger discloses the power control unit includes circuitry to "vary a supply voltage"—including "V_core_2." Ex[1010] at 0032], Fig. 2 (above, annotated). Accordingly, Naffziger discloses that its second set of cores dynamically receives a second supply voltage ("V_core_2").

The power control unit 150 (including the second power control unit 150B further includes the clock control unit 210 that "us[es] a phase locked loop (PLL) … for adjusting the frequency of a clock signal" and "is configured to vary the frequency of the core clock signal"—including "clk_core_2." *Id.* at [0033], Fig. 2 (above, annotated). Accordingly, Naffziger discloses that its second set of cores dynamically receives a second output clock signal ("clk_core_2") of a second PLL (*i.e.*, the PLL used by the clock control unit 210 of the second power control unit 150B).

The PLL of clock control unit 210 of the second power control unit 150A receives as an input "an external clock signal, clk_ext." *Id.* at [0033], Figs. 2 and 5 (above, annotated); *see also id.* at [0022] (each power control unit 150 "is coupled to receive an external clock signal, clk_ext.").

As explained for Claim 1[b2] in Ground 1, Allarey also discloses this limitation.

6. 1[b3]

Naffziger discloses this limitation. Ex[1003], ¶ 262. Naffziger discloses that the first and second sets of cores receive independent voltage supplies and clock signals. Naffziger discloses that "the operational states of processor cores 105A and 105B may be controlled independently of one another." Ex[1010] at [0054]. "Such a configuration may require that cores 105A and 105B have separate, independent core supply voltage planes and/or are configured to receive separate, independently controlled core clock signals." *Id.*

As explained for Claim 1[b3] in Ground 1, Allarey also discloses this limitation.

7. 1[b4]

Naffziger discloses this limitation. Ex[1003], ¶ 264. As discussed for Claim 1[a2] and [b2]-[b3] in Ground 5, Naffziger discloses that the multi-core processor system includes separate, independent power control units associated with the cores—for example, the first power control unit 150A corresponding to the first core 105A and the second power control unit 150B corresponding to the second core 105B—and each power control unit receives as an input an external clock signal. A PHOSITA would read Naffziger to include independent first and second power control units receiving the first and second clock signals that are independent from

each other. *Id*.

As explained for Claim 1[b4] in Ground 1, Allarey likewise discloses this limitation.

8. 1[c1]

Naffziger discloses this limitation. Ex[1003], ¶¶ 266-270. Naffziger discloses that the power control units are associated with their respective corresponding cores, and further discloses that "[t]he power control unit for each core … also monitor power consumption of the processor as a whole … as a basis for determining the operational state of its corresponding core." Ex[1010] at [0055]. A PHOSITA would have understood that the power control units 150A and 150B would be coupled to both the first and second sets of cores to monitor the multi-core processor as a whole. Ex[1003], ¶ 267.

Alternatively, Naffziger discloses a "power control unit 150 [that] is configured to monitor the processing workloads of each processor core 105A and 105B" such that "processor cores 105A and 105B may be controlled independently of one another" with "separate, independent core supply voltage planes" for the voltage supply and clock signals, as depicted in Fig. 5 (below). *See, e.g.*, Ex[1010] at [0054]. Naffziger thus also discloses a power control unit (highlighted in green) coupled to both sets of processor cores (highlighted in yellow) with separate,

independent planes dedicated to each set. Ex[1003], ¶ 268.

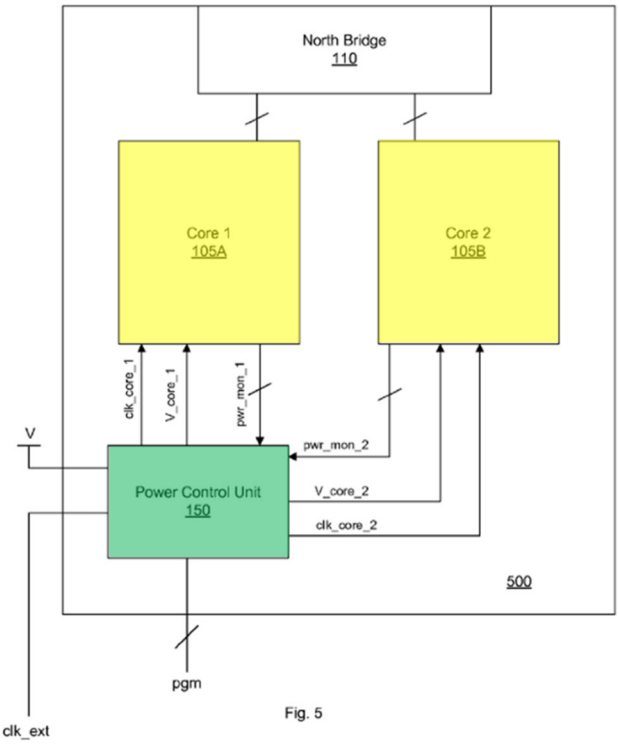


Fig. 5 of Naffziger, annotated

Naffziger teaches that the planes of the power control unit each controls a core separately and independently with independent operational state with independent voltage supply and clock signals. Ex[1010] at [0054]. A PHOSITA reading Naffziger would have understood that for each core, the corresponding plane controls its voltage and frequency independently of the other core. Ex[1003], ¶ 269. A PHOSITA thus would have understood that for each core, its corresponding plane contains the entire architecture of at least an independent voltage control unit 205 to

regulate its power supply and an independent clock control unit 210 to control clock signals. *Id*.

The dual-plane power control unit 150 (shown in green box) would have appeared as depicted below, with separate planes for controlling the first core 105A and second core 105B independently. *Id.*, ¶ 270.

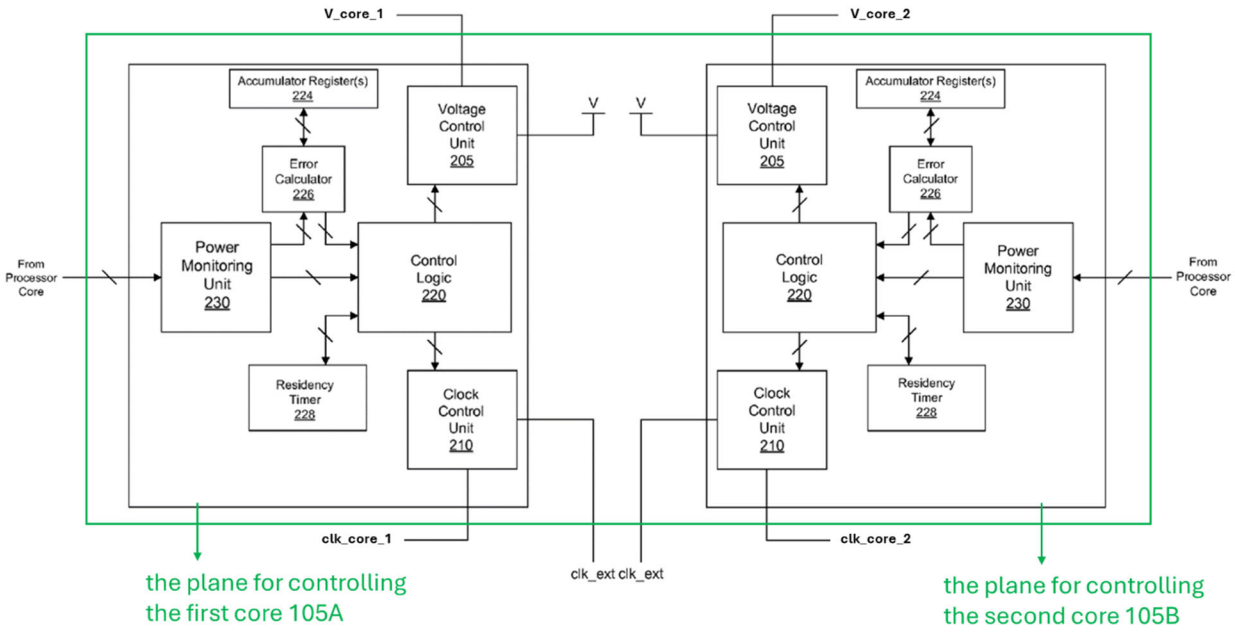


Fig. 2 of Naffziger, modified to show separate planes

As explained for Claim 1[b4] in Ground 1, Allarey likewise discloses this limitation.

9. 1[c2]

The interface block of Naffziger (the power control units or the dual-plane power control unit 150) is "configured to facilitate communication between the first

set of processor cores and the second set of processor cores." Ex[1003], ¶¶ 272-273.

Naffziger discloses that the "[p]ower control unit 150 is configured to monitor the power of both processor cores 105A and 105B, and configured to alternate operation of these cores." Ex[1010] at [0053]-[0054]. Furthermore, the power control unit(s) "monitor power consumption of the processor as a whole … as a basis for determining the operational state of [each] processor core." Ex[1010] at [0055]. A PHOSITA would have understood that the power information of the processor as a whole including that of the second core would be communicated to the first core for determining the operational state of the first core, and vice versa. Ex[1003], ¶ 273.

To the extent it is argued or found that Naffziger does not expressly disclose the interface block facilitates communications between the cores, as explained for Claim 1[b4] in Ground 1, Allarey discloses an interface block in the form of the power management link (PMLink) 120/328 that "communicatively couples" the first set of cores (the cores within site 0) and the second set of cores (the cores within site 1) and "transmit[s] data back and forth between" the first and second sets of cores. Ex[1006] at 2:59-3:3.

C. Dependent Claim 2

1. 2[pre]

As explained for Claim 1 in Ground 5, Naffziger and Allarey, alone or in combination, disclose each and every limitation of Claim 1.

2. 2[a]

Naffziger teaches the use of a level shifter in the power control unit corresponding to the first core of Naffziger. Ex[1003], ¶¶ 277-281. Naffziger discloses that the power control unit 150 includes the voltage control unit 205 that "us[es] … level shifter circuity … configured to vary a supply voltage." Ex[1010] at [0032], Fig. 2.

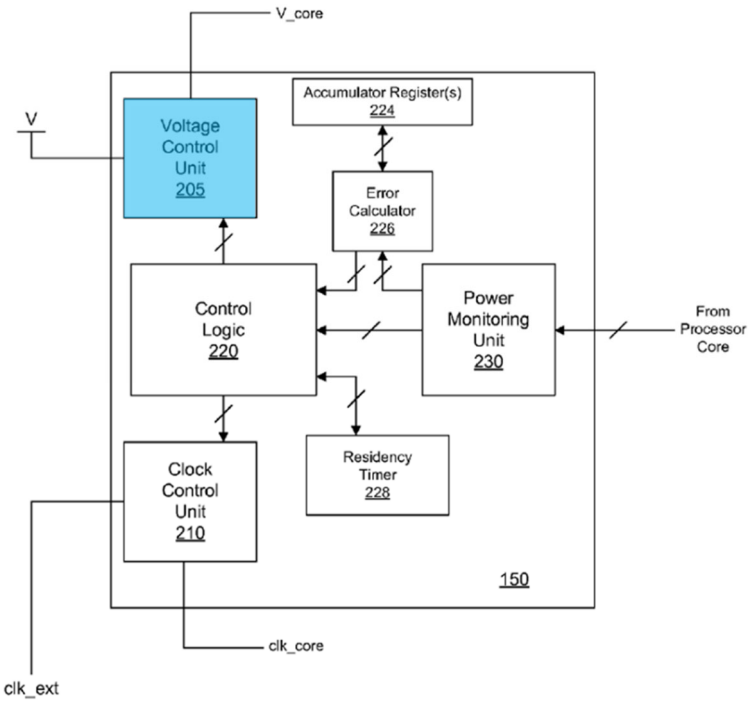


Fig. 2

Fig. 2 of Naffziger, annotated

As such, the power control unit corresponding to the first core 105A has a first level shifter and the power control unit corresponding to the second core 105B has a second level shifter.

Alternatively, the power control unit has "separate, independent core voltage supply planes" to separately control the first and second cores 105A and 105B. *Id.* at [0054]. As discussed for Claim 1[c1] in Ground 5, a PHOSITA reading Naffziger would have understood that each plane has a voltage control unit 205 comprising separate level shifter circuitry for independent control of voltage supply to each core. Ex[1003], ¶¶ 268-270, 279. Accordingly, Naffziger discloses that the interface block comprises a first level shifter (highlighted in dashed blue block) and a second level shifter (highlighted in solid blue block).

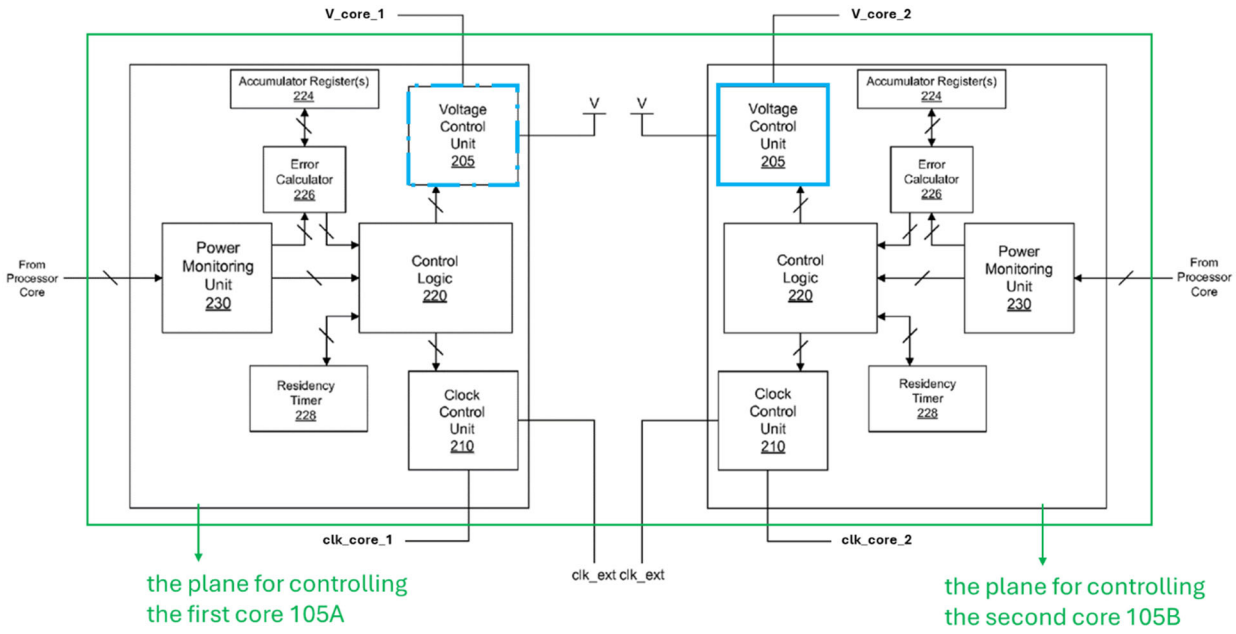


Fig. 2 of Naffziger, modified to show two planes with a first level shifter (dashed blue block) and a second level shifter (solid blue block)

Naffziger discloses that the first and second cores 105A and 105B operate in different states under different supply voltages. Ex[1010] at [0025], [0053]-[0054]. When a signal is transmitted between cores operating with different voltage levels, the signal's logic levels may not match the expected input levels of the receiving domain. Ex[1003], ¶ 281. A PHOSITA would have understood that, to ensure proper interpretation and to prevent signal integrity issues or physical damage, it is necessary to translate the voltage level of the signal from the first set of cores to the second set of cores. *Id*. Level shifters were well-understood as a standard design choice to translate signals transmitted between circuits with different voltage levels.

Id. The routine application of a level shifter to handle inter-core signals is to translate the logic levels of one core to compatible logic levels of the other. *Id*. A PHOSITA would know that level shifters are a simple and routine design choice, with applicability in this context, based on the teaching in Naffziger and/or Allarey of the first and second level shifters in the interface block that facilitates communication between the first and second cores operating with different voltage levels. *Id*.

D. Dependent Claim 3

1. 3[pre]

As explained for Claim 1 in Ground 5, Naffziger and Allarey, alone or in combination, disclose each and every limitation of Claim 1.

2. 3[a]

As discussed for Claim 2[a] in Ground 5, Naffziger discloses this limitation.

E. Dependent Claim 5

1. 5[pre]

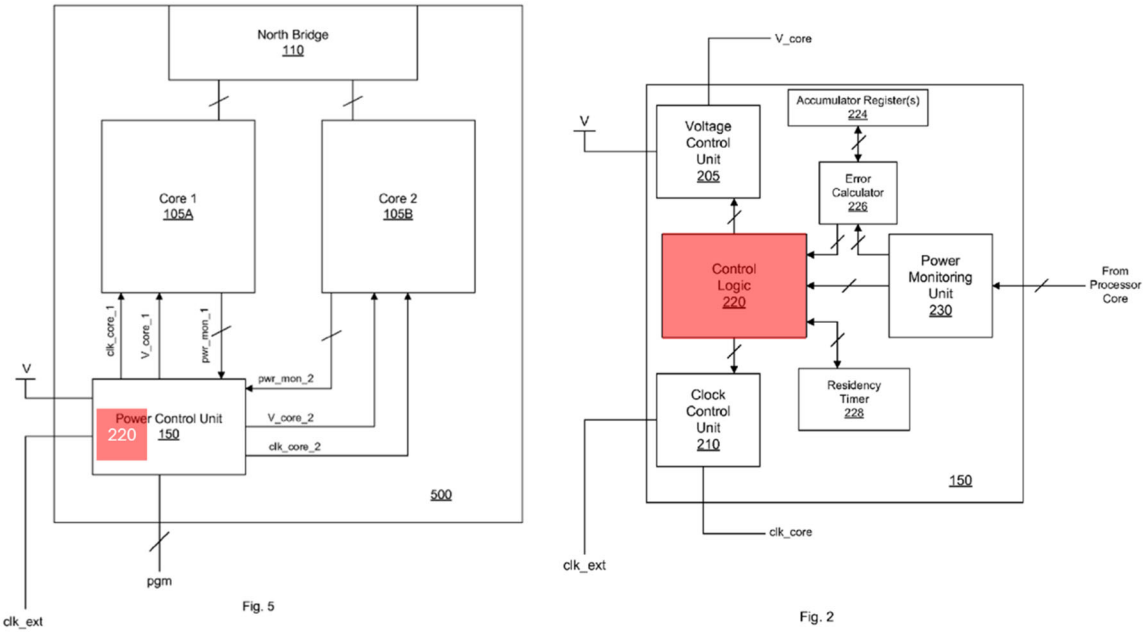
As explained for Claim 1 in Ground 5, Naffziger and Allarey, alone or in combination, disclose each and every limitation of Claim 1.

2. 5[a]

As explained for Claim 5[a] in Ground 1, Allarey teaches this limitation.

Naffziger discloses that "control logic 220" within power control unit 150 controls the operating states of the processor cores "through manipulating one or

both of a core supply voltage (V_core) or the frequency of a core clock signal (clk_core)." Ex[1010] at [0032]. Control logic 220 is coupled to both voltage control unit 205 and clock control unit 210. *Id.* Control logic 220 "provide[s] signals to voltage control unit 205" and "direct[s] voltage control unit 205 to change the core supply voltage provided to processor core 105." *Id.* Control logic 220 also provides signals to clock control unit 210 to "vary the frequency of the core clock signal." *Id.* at [0033]. As depicted below, control logic 220 (highlighted in red) is located in the periphery of Naffziger's multi-core processor.



Figs. 2 and 5 of Naffziger, annotated

Furthermore, as explained for Claim 5[a] in Ground 1, it was a known design option for a PHOSITA to place the control blocks in a periphery of the multi-core

processor without affecting its function of providing control signals to the processor cores. Ex[1003], ¶¶ 154, 288. A PHOSITA reading Naffziger would have found it obvious that control logic 220 would be placed at a periphery of the multi-core processor. *Id.*

F. Dependent Claim 8

1. 8[pre]

As explained for Claim 1 in Ground 5, Naffziger and Allarey, alone or in combination, disclose each and every limitation of Claim 1.

2. 8[a]

As discussed for Claim 8[a] in Ground 1, the '339 Patent discloses that a "region" is simply a spatial grouping of cores based on their physical location in the multi-core processor system. In Naffziger, the first set of processor cores (processor core 105A and its associated cores) are located in the physical space depicted below in red dotted box; the second set of processor cores (processor core 105B and its associated cores) are located in the physical space depicted below in green dotted box.

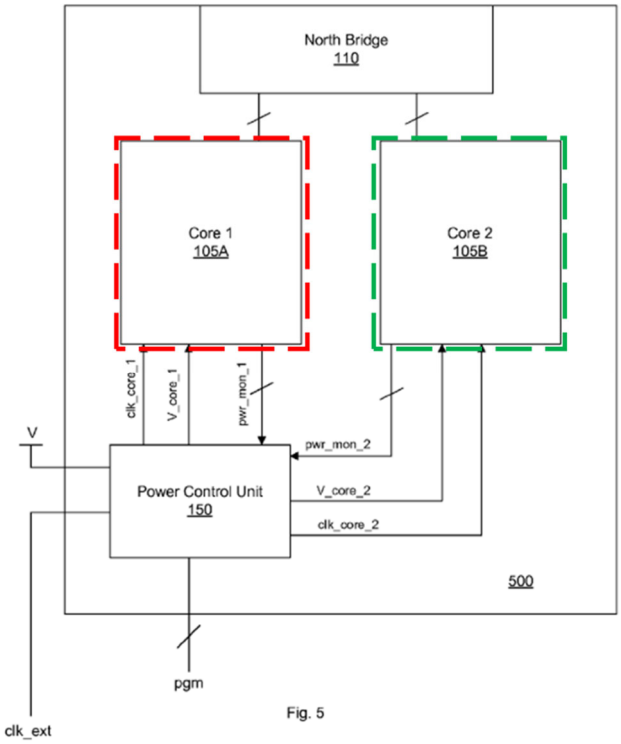


Fig. 5 of Naffziger, annotated

As such, Naffziger includes a first region corresponding to the physical location reflected by the red dotted box, and a second region corresponding to the physical location reflected by the green dotted box. The first and second regions depicted below are completely separate in physical layout and thus are non-overlapping. Ex[1003], ¶¶ 291-292.

For the same reasons described for Claim 8[a] in Ground 1, Allarey discloses this limitation.

G. Dependent Claim 9

1. 9[pre]

As explained for Claim 8 in Ground 5, Naffziger and Allarey, alone or in combination, disclose each and every limitation of Claim 8.

2. 9[a]

For the same reasons described for Claim 9[a] in Ground 1, Allarey discloses this limitation. Accordingly, Naffziger alone or Naffziger in view of Allarey renders Claim 9 obvious.

H. Dependent Claim 10

1. 10[pre]

As explained for Claim 8 in Ground 5, Naffziger and Allarey, alone or in combination, disclose each and every limitation of Claim 8.

2. 10[a]

For the same reasons described for Claim 8[a] in Ground 5, Naffziger discloses this limitation. For the same reasons described for Claim 10[a] in Ground 1, Allarey discloses this limitation. Accordingly, Naffziger alone or Naffziger in view of Allarey renders Claim 9 obvious.

I. Claim 14

1. 14[pre]

As explained above for Claim 1, Naffziger and Allarey, alone or in combination, disclose limitation of Claim 1.

2. 14[a]

For the same reasons described for Claim 14[a] in Ground 1, Allarey discloses this limitation. Accordingly, Naffziger alone or Naffziger in view of Allarey renders Claim 14 obvious.

J. Independent Claim 21

1. 21[pre]

To the extent the preamble is limiting, for the same reasons described for Claim 1[Preamble] in Ground 5, Naffziger and Allarey, alone or in combination, disclose a multi-core processor.

2. 21[a1]

For the same reasons described for Claim 1[a1] in Ground 5, Naffziger and Allarey, alone or in combination, disclose a first set of processor cores of the multi-core processor.

3. 21[a2]

Naffziger and Allarey, alone or in combination, disclose this limitation. Ex[1003], ¶¶ 306-312.

As described for Claim 1[a2] in Ground 5, the first and second sets of cores of Naffziger respectively receive "V_core_1" and "V_core_2" from the voltage control units 205 of the first and second power control units, and "clk_core_1" and "clk_core_2" from the clock control units 210 of the first and second power control unit. Ex[1010] at [0033]. Naffziger thus discloses a power control block comprising the voltage control units 205 of the first and second power control units, and a clock control block comprising the clock control units 210 of the first and second power control units.

As previously described for Claim 1[c1] in Ground 5 and depicted below, Naffziger also teaches a single structure power control unit 150 that includes separate planes for controlling the first and second processor cores 105A and 105B independently. As depicted below, power control unit 150 includes the power control block comprising the voltage control units 205 of both planes (shown in dashed blue block) and the clock control block comprising the clock control units 210 of both planes (shown in dashed purple block).

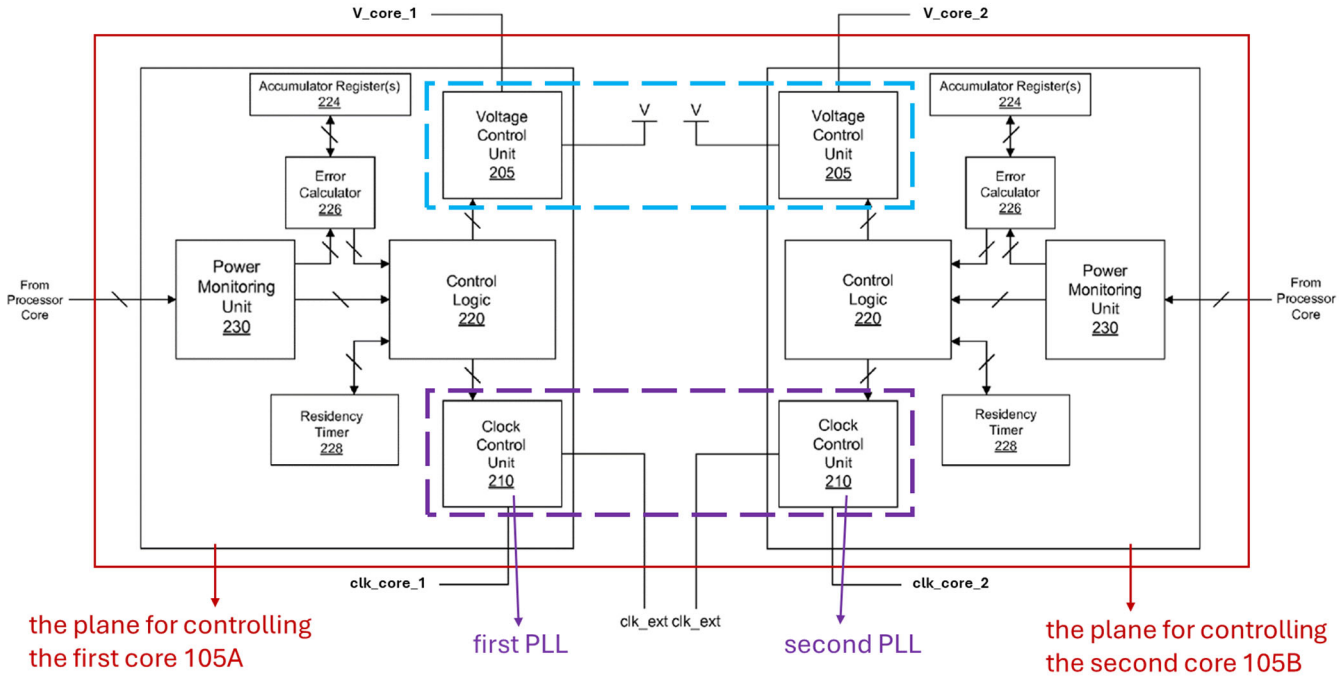


Fig. 2 of Naffziger, modified to show separate planes

Accordingly, Naffziger discloses this limitation. Ex[1003], ¶¶ 306-311.

For the same reasons described for Claim 21[a2] in Ground 1, Allarey also discloses this limitation.

4. 21[b1]

For the same reasons described for Claim 1[b1] in Ground 5 and as explained for Claim 21[a1] in Ground 5, Naffziger and Allarey, alone or in combination, disclose a second set of processor cores of the multi-core processor. Ex[1003], ¶ 313.

5. 21[b2]

For the same reasons described for Claims 1[b2] and 21[a2] in Ground 5, Naffziger discloses this limitation. Ex[1003], ¶¶ 314-315.

For the same reasons described for Claim 21[a2] and [b2] in Ground 1, Allarey also discloses this limitation.

6. 21[b3]

For the same reasons described for Claim 1[b3] in Ground 5, Naffziger discloses this limitation.

For the same reasons described for Claim 1[b3] in Ground 1, Allarey also discloses this limitation.

7. 21[b4]

For the same reasons described for Claim 1[b4] in Ground 5, Naffziger discloses this limitation.

For the same reasons described for Claim 1[b4] in Ground 1, Allarey discloses this limitation.

8. 21[c1]

For the same reasons described for Claim 1[c1] in Ground 5, Naffziger discloses this limitation.

For the same reasons described for Claim 1[c1] in Ground 1, Allarey discloses this limitation.

9. 21[c2]

For the same reasons described for Claim 1[c2] in Ground 5, Naffziger alone or Naffziger in view of Allarey discloses this limitation.

XIII. GROUND 6: CLAIM 4 IS OBVIOUS UNDER §103 OVER NAFFZIGER AND ALLAREY IN VIEW OF FLAUTNER

Naffziger and Allarey, alone or in combination, further in view of Flautner disclose each and every limitation of Claim 4.

A. Motivation to Combine Naffziger, Allarey and Flautner

Naffziger and Allarey disclose complex multi-core processors that operate in different power states and require careful management of timing and synchronization to ensure efficient communication and operation. Ex[1003], ¶¶ 327-328. Flautner's synchronizer is specifically designed to handle the timing and voltage differences between processor cores, making it highly compatible with the needs of a multi-core system that operates under varying conditions. Ex[1007] at [0047]-[0048].

Further, a PHOSITA would have understood that to facilitate communication between the first and second sets of cores of Naffziger and Allarey, the clock signals of the two cores would necessarily be required to be synchronized. Ex[1003], ¶ 328. When two cores operate at different clock speeds, the timing of signal transfers between the cores will not align. *Id.* Synchronization of the timing of the clock signals is necessary to make sure the communication from one core is recognized and correctly interpreted by the other core. *Id.* The synchronization module 50 of Flautner thus synchronizes the clock signals of the first and second cores for

communication between the first and second cores, as would be required in the systems of Naffziger and Allarey. *Id*.

B. Dependent Claim 4

Naffziger and Allarey, further in view of Flautner, disclose each and every limitation of Claim 4. *See also* Ex[1003], ¶¶ 324-329.

1. 4[pre]

As explained for Claim 1 in Ground 5, Naffziger and Allarey, alone or in combination, disclose each and every limitation of Claim 1.

2. 4[a]

As explained for Claim 4 in Ground 2, Flautner discloses this claim element.

XIV. GROUND 7: CLAIM 6 IS OBVIOUS UNDER §103 OVER NAFFZIGER AND ALLAREY IN VIEW OF WOLFE AND/OR KUMAR

Naffziger and Allarey, alone or in combination, in view of Wolfe, and further in view of Kumar disclose each and every limitation of Claim 6.

A. Motivation to Combine Naffziger, Allarey and Wolfe

A PHOSITA would have been motivated to combine Naffziger and Allarey with Wolfe. Ex[1003], ¶ 332. A PHOSITA would have recognized that Naffziger and Allarey focus more on functional mechanisms for dynamic voltage and frequency regulation in a multi-core processor system. *Id*. It would have been in the best interest of a PHOSITA to explore complementary configurations that optimize

the physical layout of the multi-core processor system to support these mechanisms. *Id*. For similar reasons as described in Section X.A, Wolfe discloses a physical layout for a multi-core processor having independent control mechanisms for dynamic management of voltage and frequency levels that would prompt a PHOSITA to consider combining with Naffziger and Allarey. *Id*.

B. Motivation to Combine Naffziger, Allarey and Kumar

To improve the power management and inter-core voltage regulation of Naffziger's and Allarey's multi-core processor systems, a PHOSITA would have been inclined to look beyond the teachings of these references to identify improved configurations as part of the normal course of his/her own research. *Id.*, ¶ 333. A PHOSITA would have been inclined to seek references which cover specific mechanisms for inter-core voltage regulation in a multi-core processor. *Id*.

For similar reasons as described in Section X.B, a PHOSITA would have been motivated to combine Naffziger and Allarey with Kumar because Kumar is directed to the same field of endeavor, *i.e.*, a power management system in the context of integrated circuits, and Kumar additionally discloses details for dynamically managing the respective voltage supplies within predetermined voltage relationships to optimize the overall power distribution and performance that can be easily implemented by a simple combination of known parts. *Id.*, ¶ 334.

C. Dependent Claim 6

1. 6[pre]

As explained for Claim 5 in Ground 5, Naffziger and Allarey, alone or in combination, disclose each and every limitation of Claim 5.

2. 6[a]

Naffziger and Allarey, alone or in combination, in view of Wolfe disclose this limitation. Ex[1003], ¶¶ 336-338.

Naffziger discloses that processor cores 105A and 105B are placed adjacent to each other, as depicted below.

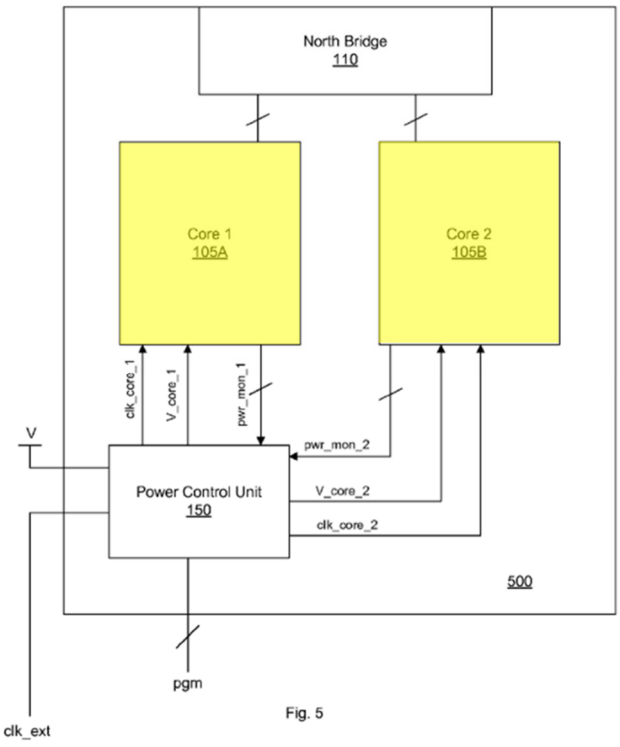


Fig. 5 of Naffziger, annotated

For the same reasons as discussed for Claim 6[a] in Ground 4, Allarey and Wolfe also disclose this limitation.

3. 6[b]

For the same reasons as discussed for Claim 6[b] in Ground 4, Kumar discloses this limitation.

XV. GROUND 8: CLAIM 11 IS OBVIOUS UNDER 35 U.S.C. § 103 OVER NAFFZIGER AND ALLAREY IN VIEW OF WOLFE

Naffziger and Allarey, in view of Wolfe disclose each and every limitation of Claim 11.

1. 11[pre]

As explained for Claim 8 in Ground 5, Naffziger and Allarey, alone or in combination, disclose each and every limitation of Claim 8.

2. 11[a]

For the same reasons as stated for Claim 11[a] in Ground 3, Wolfe discloses this limitation. Accordingly, Naffziger and/or Allarey in view of Wolfe renders Claim 11 obvious.

XVI. DISCRETIONARY DENIAL IS NOT APPROPRIATE

The Board should decline to exercise its discretion to deny institution based on the co-pending Texas Action. The factors set forth in *Apple Inc. v. Fintiv, Inc*., IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) ("*Fintiv* factors")

favor institution.

The first *Fintiv* factor favors institution, or is at a minimum neutral, because the potential of a stay exists in the Texas Action if this proceeding is instituted, especially as this Petition challenges all asserted claims.

The second *Fintiv* factor favors institution. Trial is not currently set to begin in the Texas Action for another 19 months on May 4, 2026. Ex[1015]. Accordingly, the statutory deadline for a Final Written Decision in this IPR would occur before trial in the Texas Action.

The third *Fintiv* factor weighs in favor of institution. The Texas Action is in its early stages. Petitioners have not served invalidity contentions, and the parties have not yet briefed claim construction, or begun discovery, and trial is 19 months away. Patent Owner served infringement contentions less than two months ago on August 15, 2024. Ex[1016]. Petitioners have diligently prepared the petition challenging the claims identified in Patent Owner's infringement contentions. *See Dish Network L.L.C. v. Broadband iTV, Inc*., IPR2020-01359, Paper 15 (PTAB Feb. 12, 2021).

The fourth *Fintiv* factor weighs in favor of institution or is, at a minimum, neutral. As discussed above, the Texas Action is in its early stages, and Patent Owner just served infringement contentions. Petitioners will file in the parallel district court

litigation a stipulation that, if IPR is instituted, they will not pursue in the parallel litigation any ground that is raised or that could have reasonably been raised in an IPR. This favors institution. *Sotera, Wireless, Inc. v. Masimo Corp*., IPR2020-01019, Paper 12 at 19 (PTAB Dec. 1, 2020) (precedential).

Also, despite Petitioners being the defendants in the Texas Action (*Fintiv* factor five)—something out of Petitioners' control—other circumstances weigh against discretionary denial (*Fintiv* factor six). For one, the strength of the merits in the proposed invalidity grounds favors institution. *Fintiv*, 14-15. Furthermore, this IPR is the sole IPR challenging the '339 Patent before the Board, which favors institution. *Google LLC v. Uniloc 2017 LLC*, IPR2020-00115, Paper 10 at 6 (PTAB May 12, 2020).

XVII. CONCLUSION

For the foregoing reasons, Petitioners respectfully request that a trial for *inter partes* review of the '339 Patent be instituted and that Claims 1-6, 8-11, 14 and 21 be canceled.

Dated: October 22, 2024

Respectfully submitted,

/Robert C.F. Pérez/

Robert C.F. Pérez (Reg. No. 39,328)
PILLSBURY WINTHROP SHAW
PITTMAN LLP
7900 Tysons One Place, Suite 500
Tysons, VA 22102
Telephone: 703.770.7759
Facsimile: 703.770.7901
Email: robert.perez@pillsburylaw.com

Counsel for Petitioners
MEDIATEK, INC. and
MEDIATEK USA, INC.

CERTIFICATE OF COMPLIANCE

1. The undersigned certifies that this brief complies with the type volume limitations of 37 CFR § 42.24(a)(1)(i). This brief contains 13,963 words (excluding the table of contents, the table of authorities, mandatory notices under 37 CFR § 42.8, the certificate of service, certificate of compliance, and appendix of exhibits), as calculated by the "Word Count" feature of Microsoft Word 360, the word processing program used to create it.

2. The undersigned further certifies that this brief complies with the typeface requirements of 37 CFR § 42.6(a)(2)(ii) and typestyle requirements of 37 CFR § 42.6(a)(2)(iii). This brief has been prepared in a proportionally spaced typeface using Microsoft Word in Times New Roman 14-point font.

Dated: October 22, 2024

Respectfully submitted,

/Robert C.F. Pérez/
Robert C.F. Pérez (Reg. No. 39,328)

Counsel for Petitioners
MEDIATEK, INC. and
MEDIATEK USA, INC.

CERTIFICATE OF SERVICE

The undersigned hereby certifies that a true copy of the foregoing **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,549,339 B1** and supporting materials have been served in its entirety by electronic mail this 22nd day of October, 2024, and sent by FedEx on October 23, 2024 on Patent Owner at the correspondence address for the attorney of record for U.S. Patent No. 8,549,339 shown in USPTO Patent Center, as well as on counsel for Patent Owner in the co-pending litigation:

Patent Owner in Patent Center:

Gene Su
Ren-Sheng International Ip Management Ltd.
7F, No. 57, Sec. 2, Dun Hua S. Road
Taipei, - 106 Taiwan
Telephone: (408) 729-9496

Counsel for Patent Owner in co-pending litigation:

Reza Mirzaie
Email: rmirzaie@raklaw.com
Marc A. Fenster
Email: mfenster@raklaw.com
Neil A. Rubin
Email: nrubin@raklaw.com
Christian W. Conkle
Email: cconkle@raklaw.com
Jonathan Ma
Email: jma@raklaw.com
RUSS AUGUST & KABAT
12424 Wilshire Boulevard, 12th Floor
Los Angeles, California 90025
Telephone: (310) 826-7474
Facsimile: (310) 826-6991

Qi (Peter) Tong
Email: ptong@raklaw.com
RUSS AUGUST & KABAT
4925 Greenville Avenue, Suite 200
Dallas, TX 75206
Telephone: (310) 826-7474
Facsimile: (310) 826-6991

/Robert C.F. Pérez
Robert C.F. Pérez