IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Innolux Corporation

Petitioner,

v.

Phenix Longhorn LLC

Patent Owner.

Case No. IPR2025-00043
U.S. Patent No. 7,233,305

PETITION FOR *INTER PARTES* REVIEW OF CLAIMS 1-5, 8-14 OF U.S. PATENT NO. 7,233,305

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CLAIM INDEX

Limitation #	Claim Language
1[0]	An integrated circuit for producing voltage signals on a plurality of outputs comprising:
1[1]	a plurality of non-volatile storage cells;
1[2]	circuits for programming coupled to a multiplexer for addressing and programming said storage cells, wherein the addressing is based on a plurality of inputs;
1[3]	drivers connected to said storage cells and to the plurality of outputs; and
1[4]	the plurality of inputs connected to said multiplexer for addressing said storage cells, wherein said voltage signals are gamma reference voltage signals for determining actual driving voltages of columns of a display,
1[5]	wherein said non-volatile storage cells are organized into two or more banks of cells wherein each bank contains a predetermined gamma reference voltage signal display condition; and
1[6]	means to switch between the banks based on one or more external signals is provided on said integrated circuit.
2	The integrated circuit of claim 1 wherein said non-volatile storage cells are reprogrammable
3	The integrated circuit of claim 2 wherein said means to switch between banks can have a switching time from about 10 msec to about one second.

4	The integrated circuit of claim 1 wherein said non-volatile storage cells hold analog voltage values which are a constant fraction of said gamma reference voltage signals.
5	The integrated circuit of claim 1 wherein said circuits for programming require an external source for the high voltage programming means.
8[0]	An integrated circuit for producing voltage signals on a plurality of outputs comprising:
8[1]	a plurality of non-volatile storage cells;
8[2]	circuits for programming coupled to a multiplexer for addressing and programming said storage cells, wherein the addressing is based on a plurality of inputs;
8[3]	drivers connected to said storage cells and to the plurality of outputs; and
8[4]	the plurality of inputs connected to said multiplexer for addressing said storage cells,
8[5]	an output pin connected to an output through a second multiplexer connected to said plurality of outputs wherein said output pin is at an output buffer voltage level of said output when said integrated circuit is in a programming mode to program said storage for said output.
9	The integrated circuit of claim 8 wherein said non-volatile storage cells are reprogrammable.
10	The integrated circuit of claim 9 wherein said reprogrammable, non-volatile storage cells are organized into two or more banks of cells wherein each bank contains a predetermined gamma reference

	voltage signal display condition; and means to switch between the banks based on one or more external signals is provided on said integrated circuit.
11	The integrated circuit of claim 10 wherein said means to switch between banks can have a switching time from about 10 msec to about one second.
12	The integrated circuit of claim 8 wherein said voltage signals are gamma reference voltage signals for driving columns of a display.
13	The integrated circuit of claim 8 wherein said non-volatile storage cells hold analog voltage values which are a constant fraction of said gamma reference voltage signals.
14	The integrated circuit of claim 8 wherein said circuits for programming require an external source for supplying high voltage.

I. Introduction

U.S. Patent 7,233,305 (the "'305 Patent") is invalid. The '305 Patent purports to claim systems and methods for outputting "corrected" gamma reference voltages to drive a Liquid Crystal Display (LCD). The '305 Patent claims that there was a need to "automate the gamma adjustment" that will "provide reprogrammable capability" at an "acceptable cost." (EX1001, at 2:4-12). But integrated circuits for producing gamma correction voltages to drive an LCD display were already well-known in the art as of the '305 patent's priority date, June 11, 2003, as is discussed herein. Indeed, numerous references described herein illustrate these techniques. Thus, the Board should hold each challenged claim invalid.

II. Mandatory Notices (37 C.F.R. § 42.8)

A. Real Parties-in-Interest

Innolux Corporation ("Innolux" or "Petitioner"), located at No. 160, Kexue Road, Zhunan Science Park, Miaoli County 35053, Taiwan, is the real party in interest.

B. Related Matters

Below is a listing of related matters involving U.S. Patent 7,233,305 (the '305 Patent):

- *Phenix Longhorn, LLC v. AU Optronics Corp.*, No. 2:23-cv-00477 (E.D. Tex. Filed Oct. 10, 2023)

- *Phenix Longhorn, LLC v. Innolux Corporation*, No. 2:23-cv-00478 (E.D. Tex. Filed Oct. 10, 2023)
- *Wistron Corporation v. Phenix Longhorn, LLC*, IPR No. 2018-01255 (P.T.A.B. filed June 19, 2018, Terminated Jan. 28, 2019)
- *Phenix Longhorn, LLC v. Texas Instruments*, No. 2:18-cv-00020 (E.D. Tex. Filed Jan. 22, 2018, Terminated Aug. 27, 2019)
- *Phenix Longhorn LLC v. Wistron Corporation*, No. 2:17-cv-00711 (E.D. Tex. Filed Oct 25, 2017, Terminated Sept. 9, 2019)
- *Phenix Longhorn LLC v. VIZIO, Inc.*, No. 6:17-cv-00010 (E.D. Tex. Filed Jan. 5, 2017, Terminated Jan. 4, 2018)
- *Phenix Longhorn LLC v. Integrated Memory Logic, Ltd.*, No. 6:15-cv-00436 (E.D. Tex. Filed Apr. 17, 2015, Terminated Mar. 28, 2016).

C. Designation of Lead and Back-Up Counsel

LEAD COUNSEL	BACK-UP COUNSEL
Jeffrey Johnson **BAKER BOTTS L.L.P.** 910 Louisiana Street Houston, TX 77002 Phone: (713) 229-1222 Fax: (713) 229-7922 Jeffrey.Johnson@bakerbotts.com USPTO Reg. No. 53,078	Parker Hancock **BAKER BOTTS L.L.P.** 910 Louisiana Street Houston, TX 77002 Phone: (713) 229-11196 Fax: (713) 229-2896 Parker.Hancock@bakerbotts.com USPTO Reg. No. 73,667 Robert Benson (Pro hac vice forthcoming) **BAKER BOTTS L.L.P.**

	101 California Street, Suite 3200 San Francisco, CA 94111 Phone: (415) 291-6285 Fax: (415) 291-6385 Robert.Benson@bakerbotts.com

D. Service Information

Petitioners consent to electronic service at DLInnoluxIPR305@bakerbotts.com. A Power of Attorney is filed concurrently herewith under 37 C.F.R. § 42.10(b).

E. Payment of Fees – 37 C.F.R. § 42.103

Innolux authorizes the USPTO to charge Deposit Account No. 02-0384 for the fee set forth in 37 C.F.R. § 42.15(a) for this Petition and further authorizes payment for any additional fees to be charged to this deposit account.

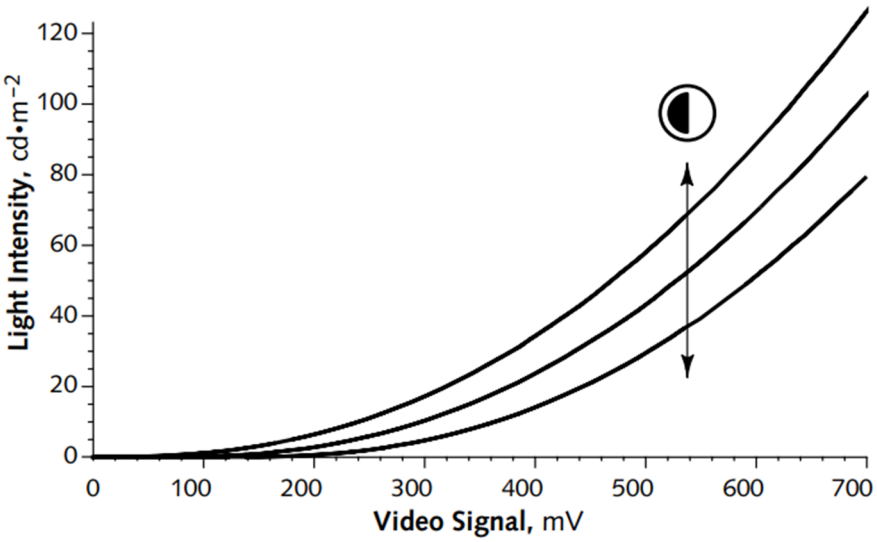
III. Petitioner Meets Standing and Eligibility Requirements for *Inter Partes* Review.

Petitioner certifies under 37 C.F.R. § 42.104(a) that the '305 Patent "is available for *inter partes* review and that the Petitioner is not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in the petition." Patent Owner served a complaint on Petitioner less than one year ago, on October 17, 2023.

IV. Background

A. Gamma Correction

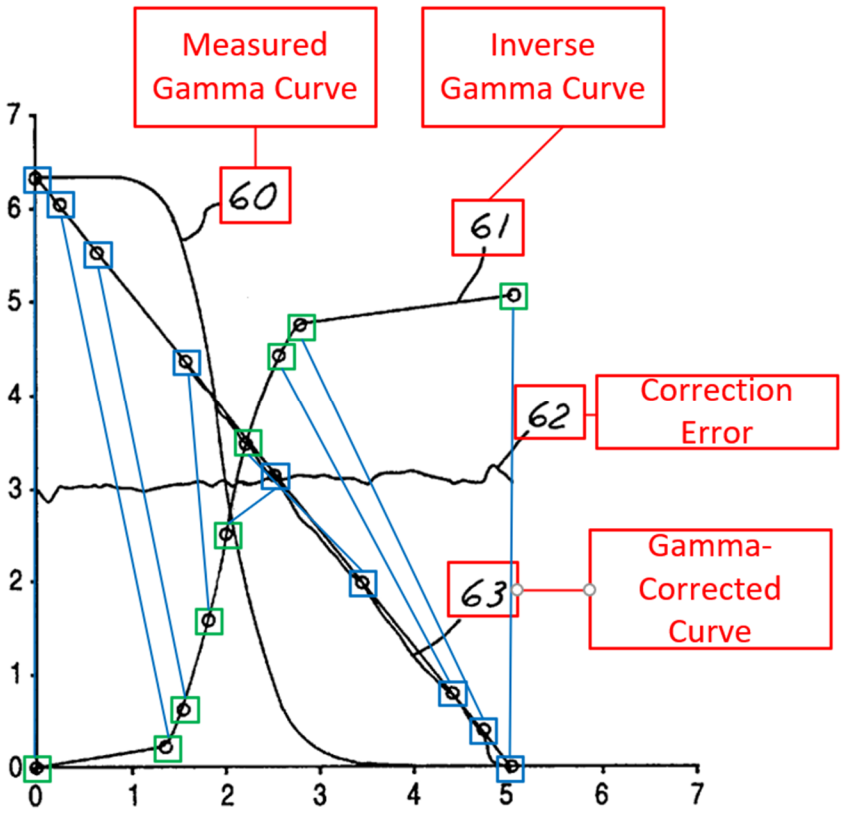
Gamma correction is an important concept in display technology that ensures that images are faithfully rendered on display devices. (EX1009, at 92-93; EX1003, at ¶43). Gamma correction addresses a mismatch between how electronic devices create images and how our eyes perceive them (EX1009, at 91; EX1003, at ¶43). Traditional cathode ray tube (CRT) displays are known to have a nonlinear relationship between the input signal and display brightness - when you increase the input signal linearly, the brightness does not increase linearly. (EX1009, at 91; EX1003, at ¶43). Instead, it follows a curved path (EX1009, at 913; EX1003, at ¶43). This curve is described by a parameter called "gamma" (EX1009, at 92-93; EX1003, at ¶43).



(EX1009, at 93; EX1003, at ¶43). Human eyes have a similar but opposite curve when perceiving brightness (EX1009, at 93; EX1003, at ¶43). By applying a gamma correction to adjust the signal before it reaches the display, the final image matches what our eyes expect to see (EX1009, at 101; EX1003, at ¶43).

Liquid Crystal Display ("LCD") screens have a similar nonlinear relationship between input voltage and transmittance – how well the LCD panel allows light to pass through it. (EX1010, at 1:10-35; EX1003, at ¶44). In order to correct this nonlinearity, the voltage-to-transmittance curve for a specific display must be determined, and an inverse transformation applied to accommodate for this nonlinearity (EX1010, at 1:36-60; EX1003, at ¶44).

This is typically done by selecting a number of points (sometimes referred to as channels) on the measured gamma curve, and providing corrections for each of those points to produce an inverse gamma curve. (EX1010, at 3:63-4:16; EX1003, at ¶45). When that inverse gamma curve is applied to inputs to the display, a linear relationship between input voltage and transmittance can be obtained. (EX1010, at 3:63-4:16; EX1003, at ¶45). This is illustrated in the figure below, which shows a measured gamma curve 60 for a display, an inverse gamma curve 61 defined by nine points (highlighted in green), and the gamma-corrected curve 63. The annotations further illustrate how the nine points (in green) in the inverse gamma curve 61 map to nine points on the gamma corrected curve 63 (in blue).



(EX1010, at 4:17-23, Fig. 6; EX1003, at ¶45). A common approach to gamma correction in LCD displays in 1997 was to store these nine points in high-speed digital memory, and to use a set of digital to analog converters (DAC's) to apply these gamma correction values to a display. (EX1011, at 4:43-65; EX1003, at ¶45).

B. Gamma Correction Circuits

Many years later, in 2003 – the time of the alleged invention - the state of the art in display technology included sophisticated systems for gamma correction to optimize image quality. (EX1003, at ¶46). Display devices commonly incorporated integrated circuits with dedicated gamma correction functionality, including nonvolatile memory for storing correction data, control circuitry for applying

corrections, and driver circuits for outputting adjusted signals to display pixels. (EX1008, Fig. 1, 3:30-37, 6:10-28; EX1003, at ¶46). These integrated designs, with components formed on a single substrate, enabled high-speed operations and efficient switching between different gamma correction data sets. (EX1008, 19:56-65; EX1003, at ¶46)

The art recognized the importance of providing independent gamma correction for different color channels to improve overall image quality. Advanced data drivers could generate separate gamma reference voltages for red, green, and blue colors, allowing for optimized color reproduction. (EX1005, 1:61-2:3, Fig. 1; EX1003, at ¶47). These systems typically employed digital-to-analog converters to transform stored digital gamma data into analog reference voltages, which were then used to convert image data into appropriate driving voltages for the display. (EX1005, 3:15-32, Fig. 1; EX1003, at ¶47)

Flexibility in gamma correction was a key focus, with systems designed to store and apply multiple sets of correction data to accommodate varying display conditions. (EX1005, 2:25-28; EX1006, 2:29-35, 8:58-67; EX1003, at ¶48). This adaptability was achieved through the use of reprogrammable nonvolatile memory arrays organized in rows and columns, allowing for efficient storage and retrieval of correction values. (EX1006, 4:11-25, 5:19-28, Fig. 3; EX1003, at ¶48)

The art also taught sophisticated memory architectures to enable on-chip programming and flexible data management. (EX1003, at ¶49). Microcomputers with embedded flash memory could partition storage into separate blocks for loader programs and application data, with shared I/O circuitry and bus multiplexing to efficiently switch between execution and programming modes. (EX1007, 3:5-13, 7:49-67, Fig. 3; EX1003, at ¶49).

Overall, the state of the art demonstrated a clear trend towards integrated, flexible, and dynamically adjustable gamma correction systems in display devices, leveraging advances in memory technology and circuit design to optimize image quality across various operating conditions. (EX1003, at ¶50).

C. Addressing Memory Cells

By 2003, it was well known to those of ordinary skill in the art that memory arrays required multiplexers to perform read and write operations on each memory cell within an array of memory cells. (EX1003, at ¶51). For example, U.S. Patent No. 5,602,987 to Harari et al., titled "Flash EEPROM System" ("Harari", EX1011), discusses conventional techniques as of 1993 – a decade before the priority date of the '305 Patent, for addressing digital memory in semiconductor devices. Below is Figure 7, which illustrates the data path for programming memory cells:

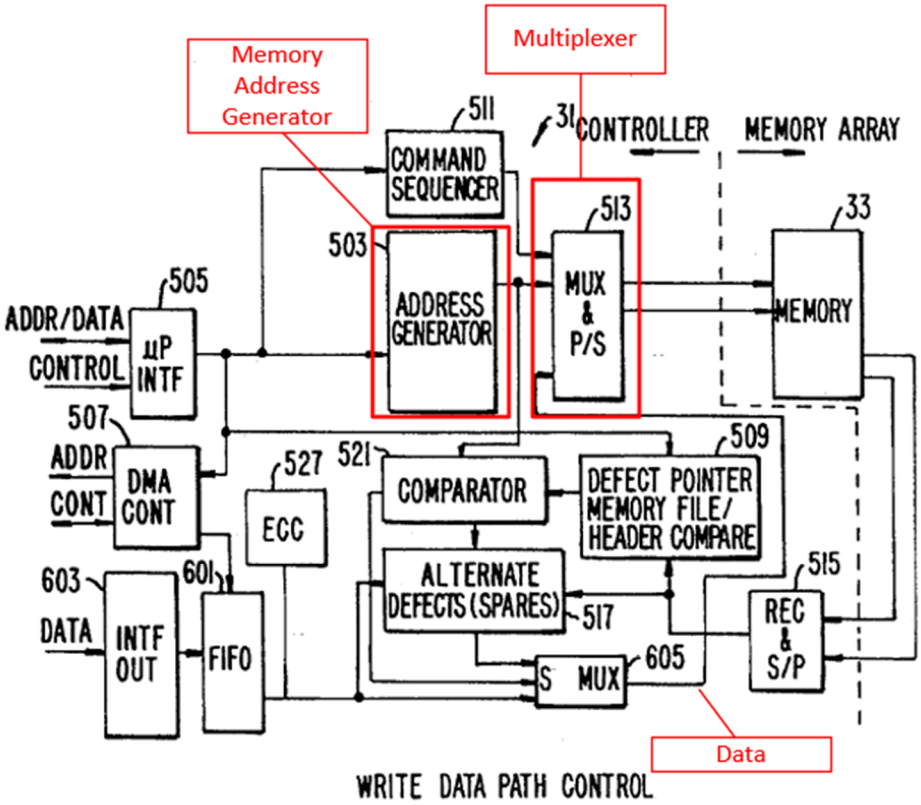


FIG._7.

As Harari describes, "data is [] sent to the memory device through multiplexers 605 and 513" (EX1011, at 11:3-14).

As another example, some non-volatile storage systems use row and column select circuits in order to choose what memory cell to send data to. (EX1003, ¶53). U.S. Patent 5,667,869 to Fazio ("Fazio") illustrates this means of performing memory addressing:

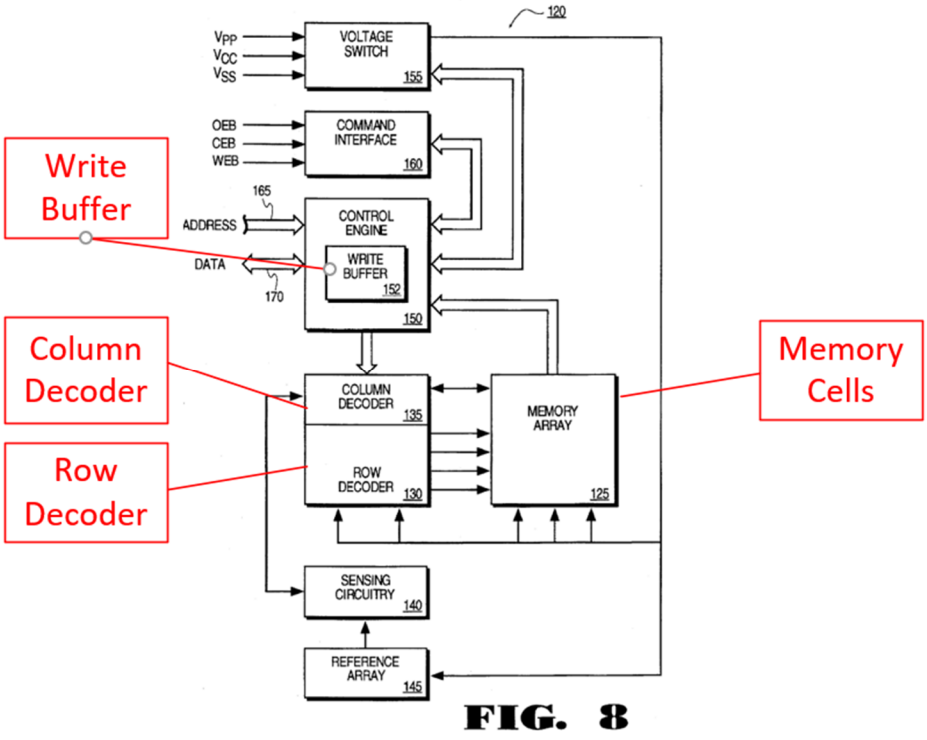


FIG. 8

(EX1012, Fig. 8; EX1003, ¶42). Fazio describes this means of addressing as follows:

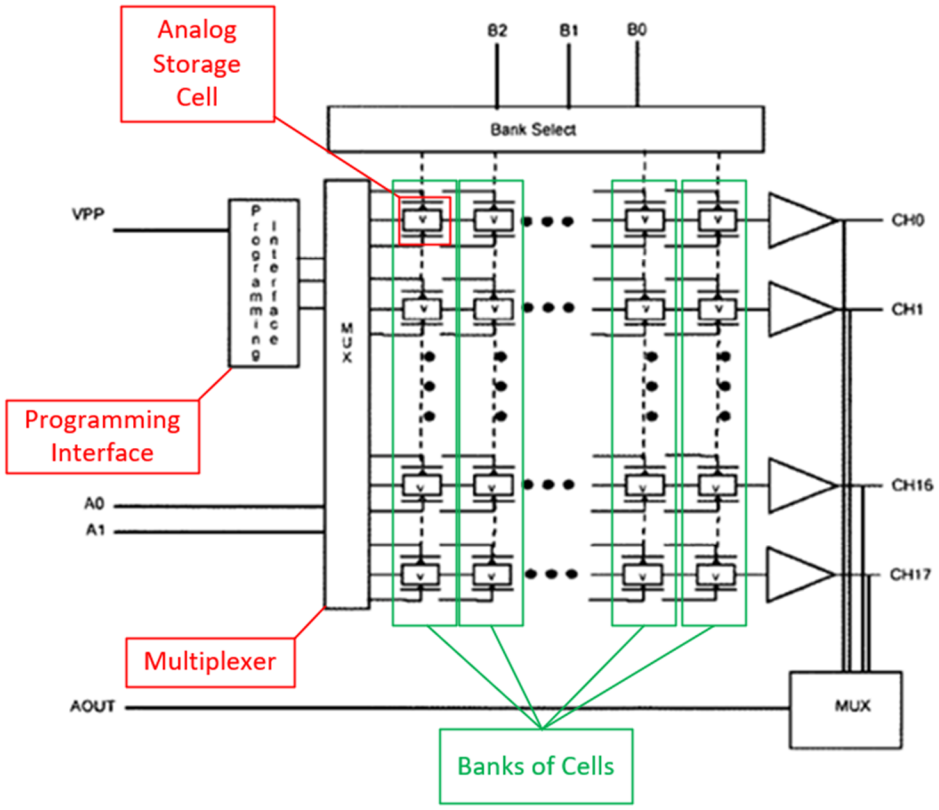
> To read data stored in the memory array 125, row decoder 130 and column decoder 135 select a number of memory cells of the memory array 125 in response to a user-provided address received via address lines 165. Row decoder 130 selects the appropriate row of memory array 125, and column decoder 135 selects the appropriate column (or columns) of memory array 12

(EX 102, at 7:17-23; EX1003, ¶54). As the figure depicts, the row decoder 130 and column decoder 135 also select rows and columns during write operations, as depicted by the arrow showing data flowing from the write buffer 152 to the column decoder 135 and row decoder 130, and on to the memory array 125. (EX1003, ¶55).

V. Summary of the '305 Patent

U.S. Patent 7,233,305 ("the '305 patent") describes an integrated circuit for generating gamma reference voltages used in LCD displays. (EX1001, 1:10-15; EX1003, ¶56). The '305 patent acknowledges that gamma correction has long been a problem for TFT flat panel display manufacturers, and that existing approaches like select-on-test resistors were already known in the art. (EX1001, 1:19-27; EX1003, ¶56). The patent proposes using non-volatile storage cells to store gamma correction data, which can be programmed to output a set of gamma correction reference voltages. (EX1001, 2:16-28; EX1003, ¶56)

The '305 patent describes organizing the non-volatile storage cells into multiple banks, where each bank contains predetermined gamma reference voltage data for different display conditions. (EX1001, 5:49-58, Fig. 6; EX1003, ¶57).



(EX1001, Fig. 6; EX1003, ¶56). The integrated circuit includes means to switch between these banks based on external signals, such as using the Bank Select shown above. (EX1001, 5:59-6:6; EX1003, ¶58). The patent describes using a programming interface to allow programming of the buffer outputs during manufacturing and testing of the display panel. (EX1001, 2:22-28; EX1003, ¶58).

The ’305 patent mentions that the non-volatile storage cells can be reprogrammable, allowing for updates to the stored gamma correction data. (EX1001, 2:29-35; EX1003, ¶59). The patent also notes that the storage cells can hold analog voltage values which are a constant fraction of the gamma reference voltage signals. (EX1001, 4:34-44; EX1003, ¶59). Additionally, the ’305 patent

describes using an external source for supplying high voltage to the programming circuits. (EX1001, 6:22-36; EX1003, ¶59). The patent claims these features allow for automated assembly, automated test and gamma adjustment, and reprogrammable settings in a stand-alone solution. (EX1001, 2:29-38; EX1003, ¶59).

A. Effective Filing Date and Date of Invention

The '305 Patent was filed on December 23, 2003, and claims priority through Provisional Application No. 60/477,680, (the '680 Application) filed on June 11, 2003. (EX1001, cover; EX1016). The effective filing date of the claims challenged herein, however, are December 23, 2003, because none of them are supported by the '680 Application.

The '680 Application entirely omits any specification description of the claimed invention at all. While the Application Data Sheet lists an invention titled "Gamma Trimster and Method for Gamma reference Voltage Generation for Displays", the actual filing contains a specification for a "Haptic Targeting Device." (EX10##, at 4, 8). That specification describes an "Invention [that] relates [to] haptic devices, and in particular to a targeting device providing haptic feedback to a user." (*Id.*). The specification contains no description of displays, gamma correction, or any other feature claimed in the '305 Patent. There appears to have been an error in the filing of the '680 Application, such that the specification of an entirely different

application was filed completely unrelated to gamma correction. This does not appear to be a USPTO record-keeping error, as both Patent Center and the new Open Data Portal show the same incorrect specification being filed under the '680 Applications' application number, and all bear the same client-matter code from the filing law firm (60477680.061103).

The '680 Patent does have three figures that apparently were intended to be part of the filing, but these figures do not include any that show numerous claimed features in the challenged claims. That one figure – Figure 3 – illustrates an embodiment with a single row of non-volatile memory cells, and omits a second output multiplexer:

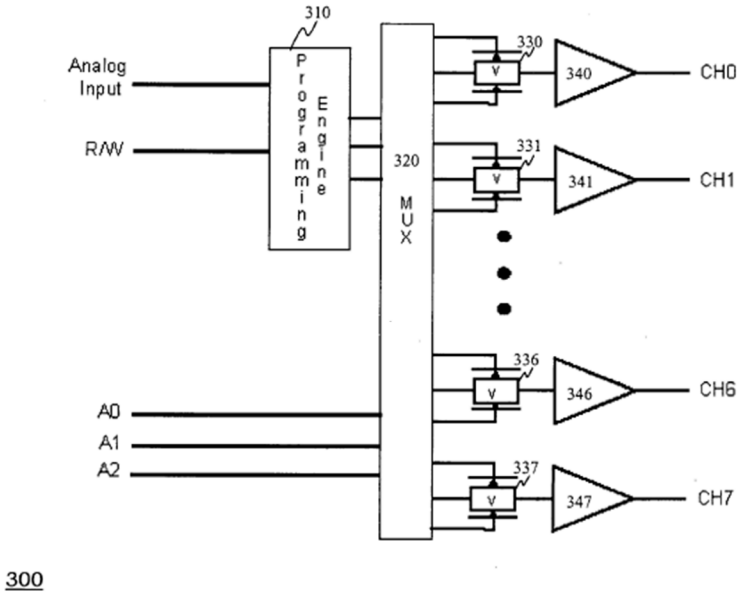


FIG. 3

(EX1016, at 3). As a result, it fails to provide *any* support for the limitation "said non-volatile storage cells are organized into two or more banks of cells" in Claim 1,

or "an output pin connected to an output through a second multiplexer connected to said plurality of outputs" in Claim 8.

Accordingly, the effective filing date of the claims challenged herein is December 23, 2003.

B. Prosecution History of the '305 Patent

The application which issued as the '305 Patent was filed on December 23, 2003 with 22 original claims. (EX1002, at 245). A non-final office action was issued on September 6, 2006 rejecting all claims. Claims 1-7, 12, 14-22 were rejected under 35 U.S.C. § 112. (EX1002, at 218-27). Claims 1, 2 and 5 were rejected as anticipated by Steffensmeier (US Pat. No. 6,373,478). (EX1002, at 218-27). Claim 8 was rejected as obvious over Liaw et al (US Pat. No. 5,593,934). (EX1002, at 218-27). Claims 9-13 were rejected as obvious over Liaw in view of Stessen (US Pat. No. 7,038,721). (EX1002, at 218-27). In response, Applicant amended claims 1, 15, 16, and 20, and withdrew claims 3, and 8-13. (EX1002, at 203-214). In a subsequent phone interview, Applicant also cancelled claims 3, 6, and 8-13 and agreed to additional amendments in the pending claims. (EX1002, at 191-196). Based on the amendments, the examiner allowed claims 1, 2, 4, 5, 7, and 14-22 on February 21, 2007, without any further examination. (EX1002, at 191-196).

C. Level or Ordinary Skill in the Art

A POSA is a hypothetical person who is presumed to know the relevant art. *See Gnosis S.P.A. et al. v. S. Ala. Med. Sci. Foundation,* Case IPR2013-00116, Paper 68 at 9, 37 (PTAB June 20, 2014). A POSA has ordinary creativity, is not an automaton, and is capable of combining teachings of the prior art. *Id.* (citing *KSR Intl'l Co. v. Teleflex Inc.,* 550 U.S. 398, 420–21 (2007)).

With respect to the '305 Patent, a POSA as of June 11, 2003, would have had at least a bachelor of science degree in physics, electrical engineering, or the equivalent thereof and three (3) years of experience in circuit design or display technologies. (EX1003 at ¶24). Such a POSA would have had knowledge of integrated circuits, gamma correction, and storage of gamma correction voltage values within memory, and would have understood how to search available literature for relevant publications. (EX1003 at ¶24).

VI. Claim Construction

The Board construes claims under the same construction standard as civil actions in federal district court. 37 C.F.R. § 42.100(b), *See Phillips v. AWS Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc).

A. "circuits for programming"

In the Wistron Litigation, the court ruled that the term "circuits for programming" was not a means-plus-function limitation, and carries its plain and ordinary meaning. (EX1013, at 34). Petitioner agrees with this construction.

B. "means to switch between the banks based on one or more external signals"

The term "means to switch between the banks based on one or more external signals" is a means-plus-function limitation under 35 U.S.C. § 112 ¶6. When construing a means-plus-function claim under 35 U.S.C. § 112 ¶6, courts must first identify the claimed function. The Federal Circuit has emphasized that "the function of a means-plus-function limitation must be determined from the claim language" itself. *JVW Enters., Inc. v. Interact Accessories, Inc.*, 424 F.3d 1324, 1331 (Fed. Cir. 2005). While the specification may provide context for understanding the claims, courts must be cautious not to improperly import functional limitations from the specification that are not recited in the claim. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005) (en banc). Once the function is properly identified, the court then looks to the specification to determine the corresponding structure that performs that function. *Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc.*, 248 F.3d 1303, 1311 (Fed. Cir. 2001).

In the Wistron Litigation[1], the court ruled that this term was a means-plus-function limitation under § 112 ¶6. (EX1013, at 46). The court further ruled that this term recites the function of "switching between the banks based on one or more external signals," and referred to the Bank Select components in the '305 Patent,

[1] *Phenix Longhorn LLC v. Wistron Corp.*, No. 2:17-cv-00711 (E.D. Tex. Filed Oct. 25, 2017).

shown in Fig. 4A (B0-B2); Fig. 4B (pins 20, 22, 23), Fig. 5 (Tdamp); Fig. 6 (Bank Select, B0, B1, B2). (EX1012, at 46).

This construction is mostly correct, but is incorrect in that it includes the damping functionality (EX1003, at ¶63). Patent Owner has repeatedly argued that this claim limitation includes not only means to switch between the banks, but specific circuitry that "damps" or "slows" the transition between banks by damping when switching banks. (EX1013, at 45-46). The court looked to a portion of the '305 Patent that explains that "[w]hen deemed appropriate an internal damping circuit creates a slow transition, about 10 msec., between banks to prevent disruptive display artifacts." (EX1001, at 5:62-6:21). However, this damping function is not described in the claim limitation, nor is this "damping" circuit a required feature of embodiments of the '305 Patent, which only suggests that such circuits be used "when deemed appropriate." (EX1003, ¶63).

Further, the inclusion of this "damping" feature would vitiate the scope of Claim 3, which further requires that the "means to switch between banks can have a switching time from about 10msec to about one second." (EX1003, ¶64). This Claim 3 additionally requires features which could be embodied by the damping circuit, but their express inclusion in Claim 3 suggests that they are *not* included in the function of Claim 1. (EX1003, ¶64). Courts must interpret claims to give meaning to all terms and avoid rendering dependent claims superfluous. *Ortho-McNeil*

Pharm., Inc. v. Mylan Labs., Inc., 520 F.3d 1358, 1362 (Fed. Cir. 2008). As the Federal Circuit has emphasized, "a claim construction that renders asserted claims facially nonsensical cannot be correct," and thus, a court should not construe an independent claim in a way that would incorporate limitations recited in its dependent claims. *Aspex Eyewear, Inc. v. Marchon Eyewear, Inc.*, 672 F.3d 1335, 1348 (Fed. Cir. 2012).

Accordingly, Petitioner respectfully submits that the proper construction of this term is that it recites the function of "switching between the banks based on one or more external signals" as shown in Fig. 4A (B0-B2); Fig. 4B (pins 20, 22, 23), and Fig. 6 (Bank Select, B0, B1, B2) (EX1003, ¶65). Nonetheless, as a POSITA would recognize, the "damping circuit" described is merely a low-pass filter, a common component well within the knowledge of a POSITA that, as argued below, could easily have been added to any of the prior art described below. (EX1003, ¶65)

A. "non-volatile storage cell"

The court in the Wistron Litigation ruled that a "non-volatile storage cell" refers to "memory cells which retain stored data even when power is removed," which can encompass both digital and analog storage cells. (EX1013, at 18-25). Petitioner agrees with this construction. (EX1003, ¶66). The term "non-volatile storage cell," would have been understood by a POSITA to refer to digital or analog storage. (EX1003, ¶66).

B. "multiplexer"

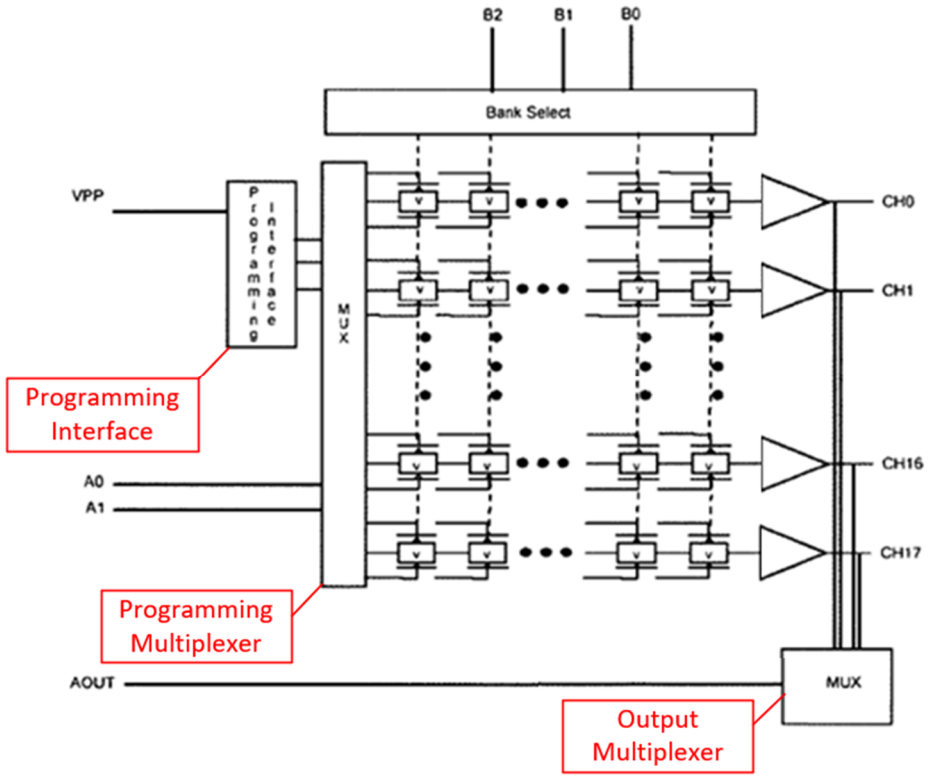
The term "multiplexer" means "one or more circuits that couple (1) one input (or one set of inputs) to one of many outputs (or one of many sets of outputs) [a de-multiplexer] or (2) one of many inputs (or one set of many sets of inputs) to one output (or one set of outputs) [a multiplexer]." (EX1013, at 13; EX1003, ¶67).

In the Board's decision denying institution in the previous petition, the Board construed the term "multiplexer" *sua sponte*, without any briefing or argument from the parties. (EX1014, at 13-14). In doing so, it inadvertently adopted a construction that does not make sense in the context of the '305 Patent, nor is it what Patent Owner agrees that the term means.

1. The Board's Prior *Sua Sponte* Construction is Incorrect.

The Board's initial construction of "multiplexer" was "a device that interleaves signals to a single line, or selects one input and switches its information to the output." (EX1014, at 14). The Board based this construction on a definition of the term in the Authoritative Dictionary of IEEE Standard Terms. (EX1014, at 13). However, this construction is incorrect and inconsistent with the use of the term as it is used in the '305 Patent, which makes clear that the term "multiplexer" can refer either to a device that can switch one of many inputs to a single output, *or* switch one input to one of many outputs. (EX1003, ¶68).

Claim 1 explains that the multiplexer is "for addressing and programming said storage cells." (EX1001, at Claim 1; EX1003, ¶68). The multiplexer referred to in the claims is shown below as "Programming Multiplexer":



(EX1001, Fig. 6).

When the multiplexer is used as part of the programming interface to write to the storage cells, the multiplexer is used to allow the programming interface to write to the various storage cells. (EX1003, ¶70). That is, it takes in a from the programming interface, and can switch that signal to one of many outputs to the storage cells (i.e. a one-to-many multiplexer). (EX1003, ¶70). Fig. 6 also shows another multiplexer, which is used to switch the gamma correction channels (CH0-

17) to the analog output (AOUT), which is therefore switching many input signals to one output (i.e. a many-to-one multiplexer.). (EX1003, ¶70). This feature is expressly claimed in Claim 8, which recites "an output pin connected to an output through a second multiplexer connected to said plurality of outputs." (EX1001, Claim 8). This is also consistent with how the term "multiplexer" is used by POSITAs, where the term "multiplexer" can be a generic term to refer to multiplexers, demultiplexers, or bidirectional multiplexers (that operate as either multiplexers or demultiplexers depending on the operating mode.) (EX1003, ¶70).

2. Patent Owner Has Agreed to the Proper Construction of the Term "Multiplexer."

In the Wistron Litigation, Patent Owner agreed that the term "multiplexer" should be defined as" one or more circuits that couple (1) one input (or one set of inputs) to one of many outputs (or one of many sets of outputs) [a de-multiplexer] or (2) one of many inputs (or one set of many sets of inputs) to one output (or one set of outputs) [a multiplexer]." (EX1012, at 13). This is the correct construction that is consistent with how the term is used by POSITAs, and how the term is used in the '305 Patent. (EX1001, at 3:18-31, 3:48-4:3, Claim 8; EX1003, ¶71).

C. "two or more banks of cells"

For the purposes of this Petition, the term "two or more banks of cells" should be construed as "two or more separate devices of addressable computer memory." (EX1003, ¶72). In the prior proceeding, the Board adopted a similar construction of

the term "banks of cells," which it construed as "contiguous sections of addressable memory" (EX1014, at 15). The Board relied upon the Authoritative Dictionary of IEEE Standards Terms, which in part defined a "bank" as "a contiguous section of addressable memory." (EX1014, at 15).

This construction is incorrect. (EX1003, ¶73). Petitioner takes no issue with this understanding of the term "bank" as it is used to refer to a single collection of devices. (EX1003, ¶73). However, the claim term refers to a plurality of banks of cells, not a single bank. (EX1003, ¶73). As a result, the term as it is used in the '305 Patent must refer to separate "banks," and not a single bank. (EX1003, ¶73). And if a bank is a "contiguous section of addressable memory," then the term "two or more banks of cells" must refer to more than one such contiguous sections. (EX1003, ¶73).

Petitioner does not believe that any other terms are necessary to be construed to resolve this Petition in favor of Petitioner.

VII. Specific Relief Requested

A. Proposed Grounds

1. Ground 1

Claims 1-5, and 8-14 are invalid under 35 U.S.C. § 103 over Nakata (EX1005).

2. Ground 2

Claims 1-5, and 8-14 are invalid under 35 U.S.C. § 103 over Nakata (EX1005), in view of Tsai (EX1007).

3. Ground 3

Claims 1-5, and 8-14 are invalid under 35 U.S.C. § 103 over Petropoulous (EX1006).

4. Ground 4

Claims 1-5, and 8-14 are invalid under 35 U.S.C. § 103 over Petropoulous (EX1006), in view of Tsai (EX1007).

5. Ground 5

Claims 1-5, and 8-14 are invalid under 35 U.S.C. § 103 over Nakata (EX1005) in view of Tsai, in further view of Yamazaki (EX1008).

6. Ground 6

Claims 1-5, and 8-14 are invalid under 35 U.S.C. § 103 over Petropoulous (EX1006) in view of Yamazaki (EX1008).

7. Ground 7

Claims 1-5, and 8-14 are invalid under 35 U.S.C. § 103 over Petropoulous (EX1006), in view of Tsai (EX1007), in further view of Yamazaki (EX1008).

B. Qualifying Prior Art

The references relied upon in the grounds above qualify as prior art for the following reasons:

Prior Art Reference	Priority Date	Publication / Issue Date	Applicable Section of 35 U.S.C. § 102
U.S. Publication 2004/0090409 A1 to Nakata et al. ("Nakata")	Nov. 7, 2003	May 13, 2004	§ 102(e)
U.S. Patent 6,760,068 to Petropoulos et al. ("Petropoulous")	Dec. 31, 1998	Jul. 6, 2004	§ 102(e)
U.S. Patent 5,974,528 to Tsai et al. ("Tsai")	July 7, 1998	Oct. 26, 1999	§ 102(a), (e)
U.S. Patent 6,271,825 to Yamazaki, et al. ("Yamazaki")	Aug. 31, 1998	Jan. 1, 2002	§ 102(a), (e)

VIII. The Board Should Not Deny Institution Under 35 U.S.C. § 325(d)

The Board should not deny institution under 35 U.S.C. § 325(d), because the arguments presented here have not been previously presented to the USPTO. In particular, the arguments presented here address newly found prior art, and address additional rulings and statements by Patent Owner in district court litigation that occurred after the Board denied institution in IPR2018-01255, involving the '305 Patent.

A. The Board Should Not Deny Institution Because This Petition Cures The Deficiencies in the Prior Petition in IPR2018-01255

This patent was previously challenged by a Petition for Inter Partes Review that was denied. *Wistron Corp. v. Phenix Longhorn LLC*, IPR2018-01255, Paper No. 14 (June 18, 2018). In that Petition, the Board denied institution for the following reasons:

- Petitioner failed to present a claim construction for the term "means to switch between the banks based on one or more external signals", which was a means-plus-function limitation. (*Id.* at 9-10).
- The Prior Art failed to show the presence of "circuits for programming coupled to a multiplexer for addressing and programming said storage cells." (*Id.* at 17-21).
- The Prior Art failed to show that the "non-volatile storage cells are organized into two or more banks of cells." (*Id.* at 22-23)
- The Prior Art failed to show "means to switch between the banks based on one or more external signals." (*Id.* at 23-25).

The present Petition cures each of these deficiencies.

1. Petitioner Presents a Construction of "means to switch between banks . . ."

First, Petitioner herein has presented a construction of the term "means to switch between banks . . ." relying on the constructions issued by the Board in the prior proceeding (EX1013, at 9-13), and the court's Claim Construction in the Wistron Litigation (EX1014, at 41-46). Petitioner disputes that the proper construction of that term includes the "damping circuit," because such function is not described by the claim language and violates the principle of claim differentiation. Nonetheless, the described "damping circuit" as described herein is

merely a low-pass filter that would have been well within the skill of a POSITA to incorporate into any of the grounds of challenge as described below. (EX1003, ¶63).

B. Patent Owner Has Taken Conflicting Positions on The Presence of "Multiplexers" In Digital Memory.

PO has obtained two constructions of the term "multiplexer," and has taken a third position on the meaning of the term in its litigation against Innolux. Institution of this petition is necessary to resolve this conflict and invalidate the '305 Patent. As described above, PO has received two conflicting constructions – one *sua sponte* from the Board in the Prior Proceeding, and one by agreement with a defendant in the Wistron Litigation. PO has taken *yet a third* position with respect to the term "multiplexer" in its litigation with Innolux that conflicts with this Board's prior construction. (EX1015, at

In the Innolux Litigation, Patent Owner has accused Petitioner's products of infringing the claims of the '305 Patent. In the Infringement Contentions served on Petitioner, Patent Owner argues that the accused products contain "circuits for programming coupled to a multiplexer for addressing and programming said storage cells" because the digital memory used in those devices uses an I^2C serial interface:

> Upon information and belief, the Accused Innolux Chips meet the "circuits for programming coupled to a multiplexer for addressing and programming said storage cells, wherein the addressing is based on a plurality of inputs" element of claim limitation 1[b].
>
> Interface to the memory locations is accomplished through the I^2C serial interface, which consists of a serial data line (SDA or GSDA) and

> a serial clock line (SCL). Address information is sent to the device in a bit serial fashion, and the data is either read or written in the same bit serial manner. In order to program the storage cells, upon information and belief, a write command is sent to the device by changing the value in the location on the screen.

(EX1015, at 21-22). However, in opposing the prior Petition, PO argued extensively that I^2C interfaces *could not* satisfy this limitation. Specifically, it argued that "a multiplexer and an I^2C serial interface do not perform the same function within an integrated circuit and are therefore not interchangeable." (EX1014, at 25).

Given the multiple conflicting constructions and positions taken by PO, the Board should not deny institution in part to resolve this construction issue, which would inevitably lead to the conclusion that the Challenged Claims are invalid.

C. The Board Should Not Deny Institution Because This Petition Presents New Prior Art Satisfying the Allegedly Missing Claim Limitations.

Both Nakata (EX1005) and Yamazaki (EX1007) have not previously been presented to the USPTO to challenge the validity of the '305 Patent, nor are they cumulative with any references previously presented. Petropoulos (EX1006) and Tsai (EX1007) were previously relied upon in IPR2018-01255. However, Petitioner respectfully submits that institution should not be denied on that basis in view of the subsequent litigation and conflicts over the meaning of the term "multiplexer."

Further, Tsai (EX1007) was used in the prior IPR to show express disclosure of a "multiplexer," but was not relied upon as a primary reference. (EX1014, at 47). The Board found no fault with the application of Tsai to disclose a "multiplexer,"

and instead denied institution of the Tsai grounds because of other deficiencies in the base references. (EX1014, at 47).

IX. The Board Should Not Deny Institution Under 35 U.S.C. § 314(a)

The factors described in *Apple, Inc. v. Fintiv, Inc*, IPR2020-00019, Paper 11 (PTAB March 20, 2020) (Precedential) ("*Fintiv-I*") favor institution.

As of this Petition, discovery has only recently opened in the District Court Litigation and, although a stay motion has not yet been filed, Petitioner intends to promptly file a stay motion in the event of IPR institution. The Board has treated related factors as neutral after declining to speculate on the outcome of a stay motion. *See, e.g., HP Inc. v. Slingshot Printing LLC*, IPR2020-01084, Paper 13 at 9 (PTAB Jan. 14, 2021) ("HP") (instituting IPR after declining to speculate on likelihood of a stay).

Institution is strongly favored where, as here, Petitioner has been "exceptionally diligent" in filing. *Micron Tech., Inc. v. Godo Kaisha IPR Bridge 1*, IPR2020-01007, Paper 15 at 15-16 (PTAB Dec. 7, 2020). The Board has made clear that "it is often reasonable for a Petitioner to wait to file its petition until it learns which claims are being asserted against it in the parallel proceeding," and here, Petitioner filed its Petition less than eight weeks after receiving infringement contentions. *Fintiv-I* at 11. In light of Petitioner's diligence, any argument

comparing the timing of respective milestones between this proceeding and the District Court Litigation would be premature.

If Patent Owner raises §314(a) arguments in a Preliminary Response, Petitioner respectfully requests the opportunity to reply prior to institution, in order to address expected schedules at that time and whether a stipulation limiting arguments to be made in the District Court Litigation would be appropriate.

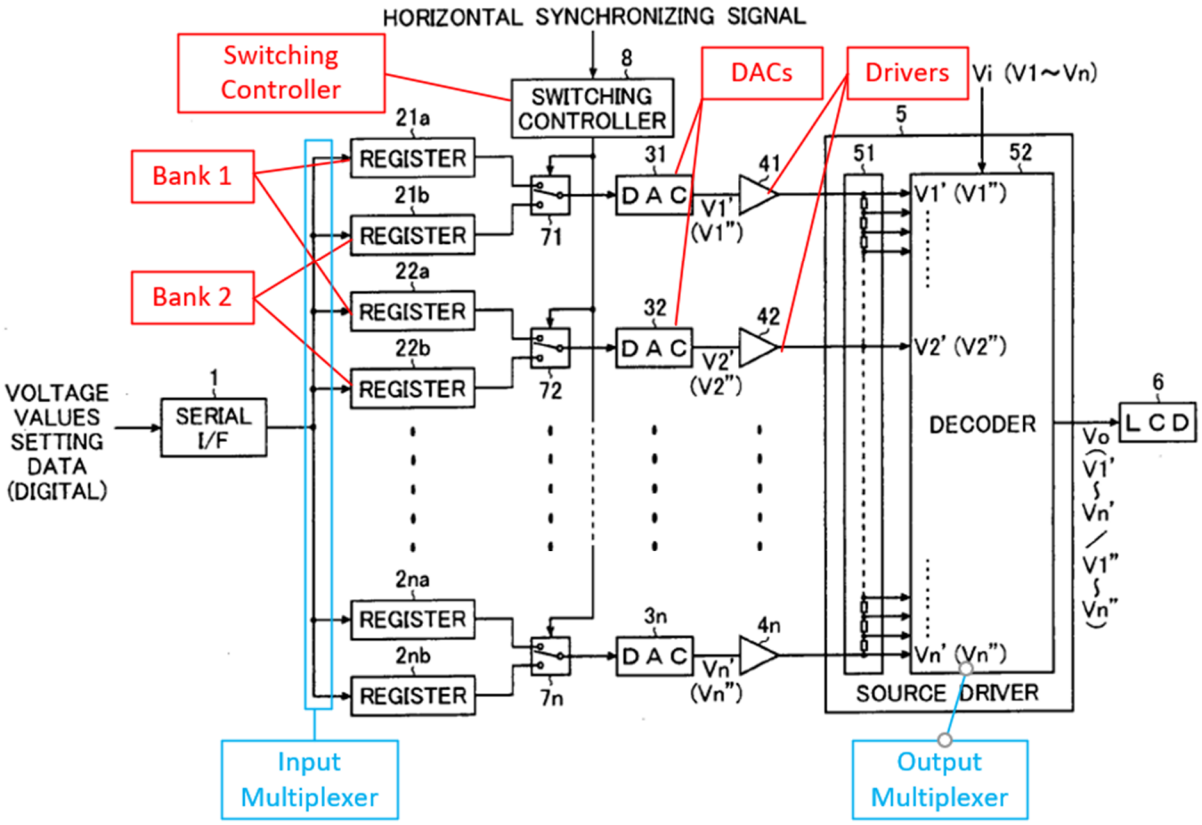
X. The Prior Art

A. Nakata (EX1005)

The Nakata reference discloses a gamma correction voltage generation device for producing gamma reference voltages to drive a liquid crystal display. (EX1005, [0017], Fig. 1; EX1003, ¶82). The device comprises multiple sets of registers for holding digital data, digital-to-analog converters (DACs) for converting the digital data to analog voltages, and buffers for amplifying and outputting the analog voltages as gamma correction voltages. (EX1005, [0017]-[0019], Fig. 1; EX1003, ¶82). Nakata teaches that the registers can be implemented as non-volatile, reprogrammable memories to easily store and update corrected gamma values. (EX1005, [0019], [0028]).

In some embodiments, Nakata discloses organizing the registers into multiple banks, each containing a different pattern of gamma correction data. (EX1005, [0021]-[0024], Fig. 2; EX1003, ¶83). A switching controller allows switching between these banks based on external signals like scanline information. (EX1005,

[0024], Fig. 2; EX1003, ¶83). This reference was selected because it demonstrates that using reprogrammable non-volatile storage to generate customizable gamma correction voltages was known in the art. (EX1003, ¶83). The multi-bank organization and switching capabilities further show that dynamically adjustable gamma correction based on display conditions was a known technique for enhancing image quality in LCD devices. (EX1003, ¶83)



(EX1005, at Fig. 3 (annotated)).

B. Petropoulos (EX1006)

The Petropoulos reference discloses an integrated circuit for modifying sensor array outputs using programmable analog/multi-level non-volatile memory.

(EX1006, 3:38-47, Fig. 2; EX1003, ¶84). The system stores modification voltages, including gamma correction values, in reprogrammable memory cells organized in rows and columns. (EX1006, 4:11-25, 5:19-28, Fig. 3; EX1003, ¶84). These stored values are used to adjust sensor outputs through various modification circuits, such as summing, subtraction, and multiplication. (EX1006, 4:52-64, 7:7-24, Figs. 4-5; EX1003, ¶84). The reference also describes using high programming voltages supplied externally to program the non-volatile memory cells. (EX1006, 5:58-64; EX1003, ¶84). Petropoulos was selected for this IPR because it demonstrates that storing and applying gamma correction values using reprogrammable non-volatile memory in display driver circuits was known in the art. (EX1003, ¶84). The reference contributes significantly to the invalidity analysis by showing how gamma correction values could be flexibly stored and updated to optimize display output for various conditions. (EX1003, ¶84).

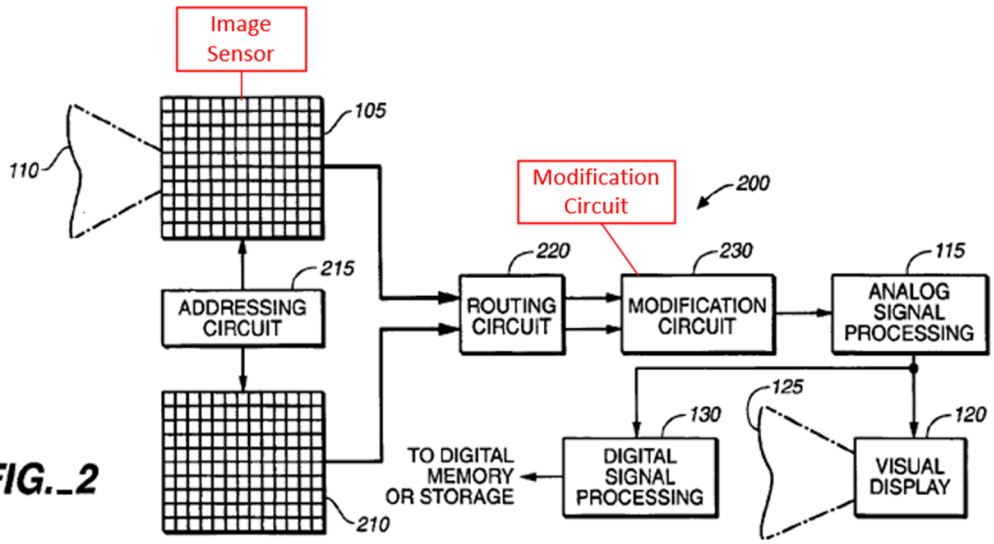


FIG._2

(EX1006, at Fig. 2)

C. Tsai (EX1007)

The Tsai reference discloses a microcomputer with an embedded flash memory unit that enables on-chip programming without external tools. (EX1007, Abstract, 2:38-43; EX1003, ¶85). The flash memory is partitioned into a loader block for storing a loader program and a user block for storing application programs, both sharing the same I/O circuit. (EX1007, 3:5-13, Fig. 2; EX1003, ¶85). A bus multiplexer selectively connects either block to the microprocessor unit or register set based on memory selection (MSEL) and bus selection (BSEL) signals. (EX1007, 3:23-42, 7:49-67, Fig. 3; EX1003, ¶85). The microprocessor includes a timer to control the programming process, ensuring sufficient time for data transfer while maintaining system responsiveness. (EX1007, 4:41-5:21, Fig. 4; EX1003, ¶85). Tsai's reprogrammable memory structure and flexible switching mechanism make

it particularly relevant for implementing updateable voltage generation systems, such as those used for gamma correction in displays. (EX1003, ¶85). The ability to store and switch between multiple sets of programmed data aligns well with the needs of adaptive display systems. (EX1003, ¶85).

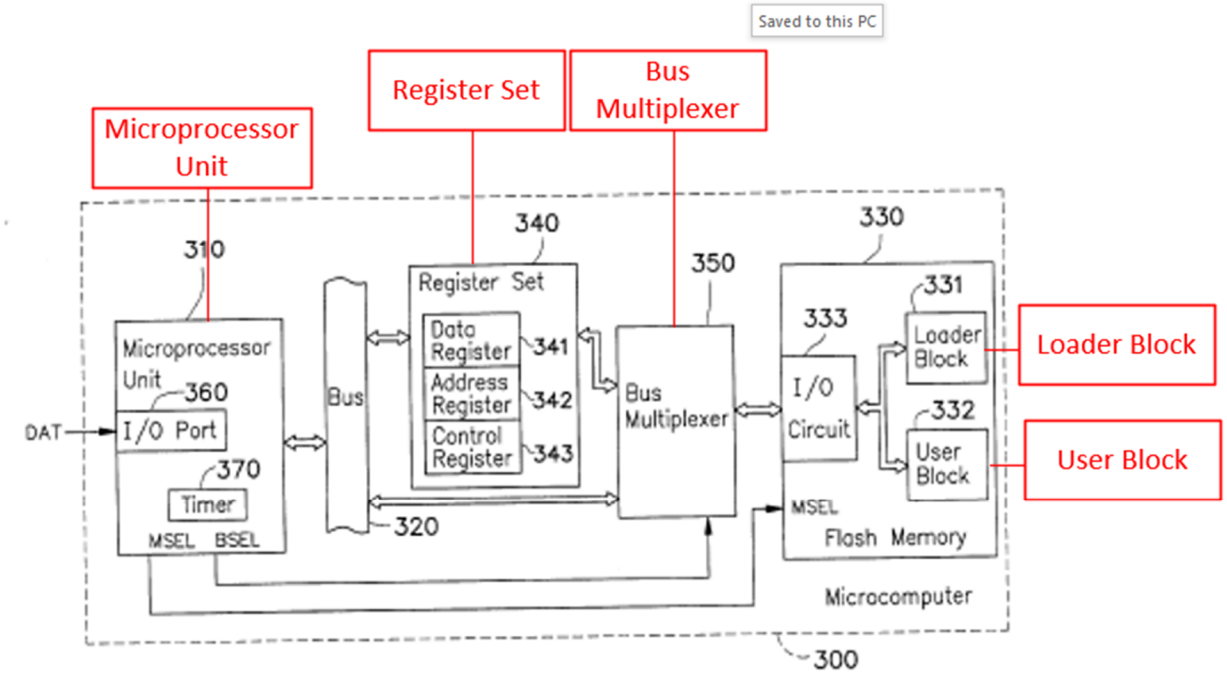


FIG. 3

(EX1007, Fig. 3 (annotated)).

D. Yamazaki (EX1008)

Yamazaki discloses an integrated circuit for gamma correction in a display device (EX1003, ¶86). The circuit includes a nonvolatile memory for storing gamma correction data, a control circuit for performing gamma correction, and driver circuits for outputting corrected signals to display pixels. (EX1008, Fig. 1, 3:30-37, 6:10-28; EX1003, ¶86). The nonvolatile memory comprises FAMOS-type TFTs

with floating gates arranged in a matrix, allowing storage of multiple gamma correction data sets. (EX1008, Fig. 3, 8:16-34; EX1003, ¶86). Yamazaki's system enables customized gamma correction for individual displays by storing device-specific correction data. (EX1008, 5:60-6:9; EX1003, ¶86)

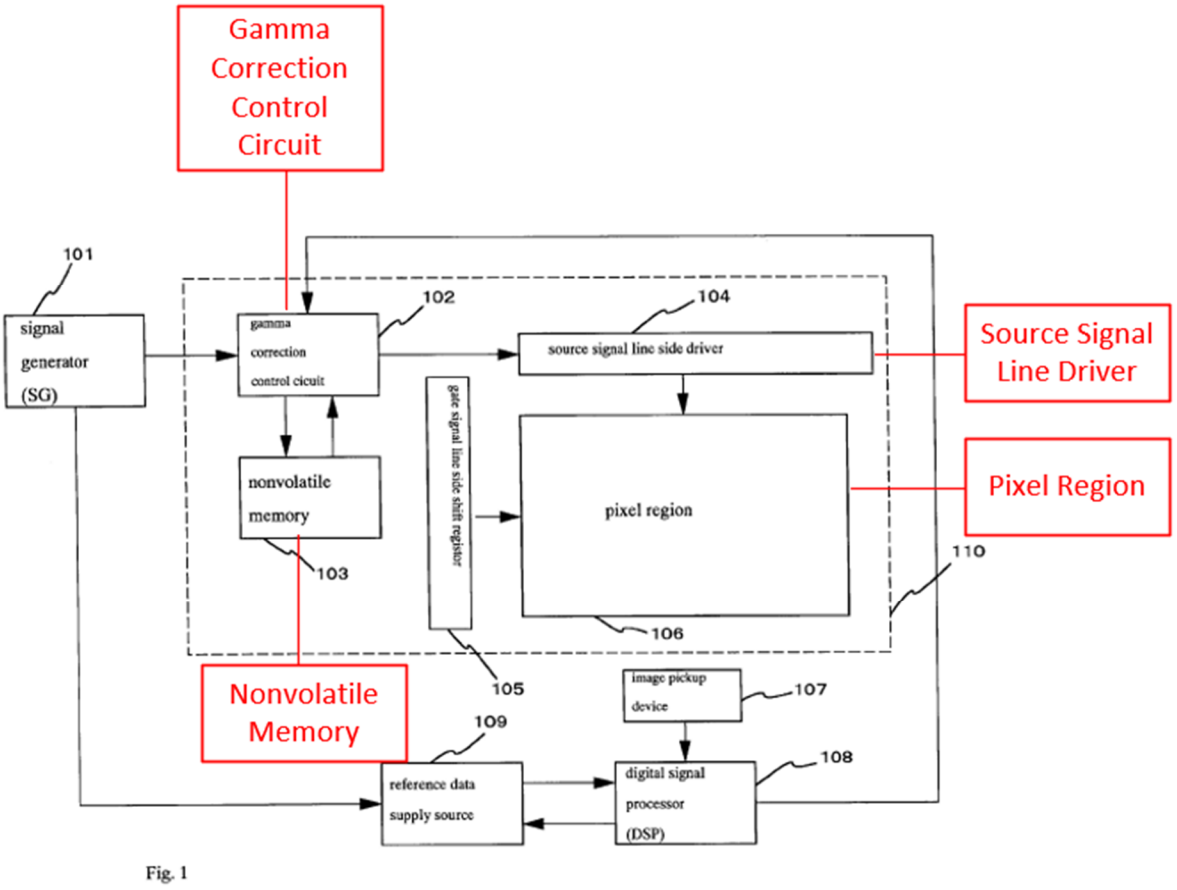


Fig. 1

(EX1008, Fig. 1)

The gamma correction control circuit receives input signals and addresses the appropriate memory cells to retrieve correction data. (EX1008, 6:39-46; EX1003, ¶87). This data is then used to adjust voltage levels applied to the display columns

via the source signal line side driver. (EX1008, 6:14-28; EX1003, ¶87). Yamazaki's integrated design, with all components formed on a single substrate, enables high-speed operations and efficient switching between different gamma correction data sets. (EX1008, 19:56-65; EX1003, ¶87)

XI. Motivations to Combine

A POSITA would have been motivated to combine each of the asserted combinations here to arrive at the challenged claims. (EX1003, ¶88). Each of Nakata, Petropoulous, and Yamazaki relate to the field of integrated circuits for producing gamma reference voltages to drive a display. (EX1003, ¶88). Each also includes programmable non-volatile storage cells for storing the voltage values. (EX1003, ¶88). Thus, all the references asserted here are analogous art, because they are in the same field of endeavor. (EX1003, ¶88). Tsai is in the field of memory devices, and thus would also be analogous to the '703 Patent because it is also in the same field of endeavor – related to the storage and use of information – but does not disclose gamma reference voltage correction. (EX1003, ¶88). Even if Tsai is not in the same field of endeavor, it is reasonably pertinent to the problems to be solved by the '305 Patent, because it discloses a memory device useful for storage and retrieval of information. (EX1003, ¶88). The specific rationales to combine these references, along with more specific similarities of each, are further provided below.

XII. Ground 1: Claims 1-5, and 8-14 are Invalid as Obvious over Nakata

Claims 1-5, and 8-14 are invalid as obvious over Nakata. Below is a limitation-by-limitation analysis of Nakata, showing where each limitation is found in the prior art. (EX1003, ¶89)

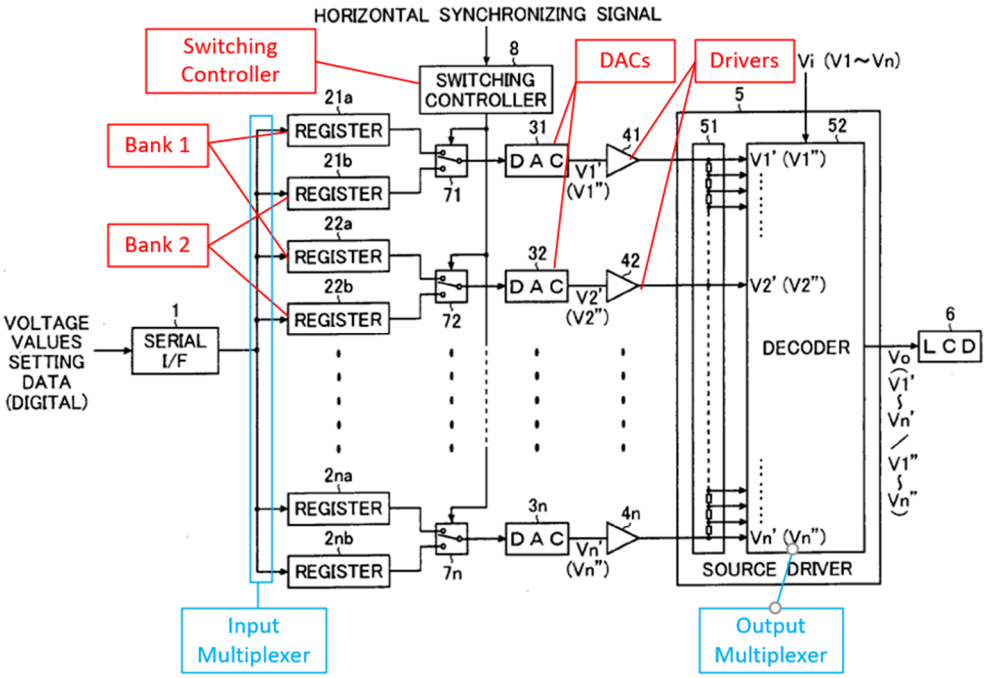
A. Claim 1

1. Limitation 1[0]: An integrated circuit for producing voltage signals on a plurality of outputs comprising:

Nakata discloses this limitation. (EX1003, ¶90). Nakata describes a gamma correction voltage generation device that outputs analog voltages V1' to Vn' as gamma correction voltages on multiple outputs from buffers 41 to 4n. (EX1005, [0017]-[0019], Fig. 1; EX1003, ¶90). While not explicitly labeled an "integrated circuit," a POSITA would understand the gamma correction voltage generation device to be implemented as an integrated circuit, as this was the standard implementation for display driver circuits at the time. (EX1005, [0029]-[0031]; EX1003, ¶90).

2. Limitation 1[1]: a plurality of non-volatile storage cells;

Nakata discloses this limitation. (EX1003, ¶91). Specifically, Nakata describes registers 21 to 2n for holding digital data used to generate gamma correction voltages, shown below as Bank 1 and Bank 2. (EX1005, [0017]-[0019], Fig. 1; EX1003, ¶91).



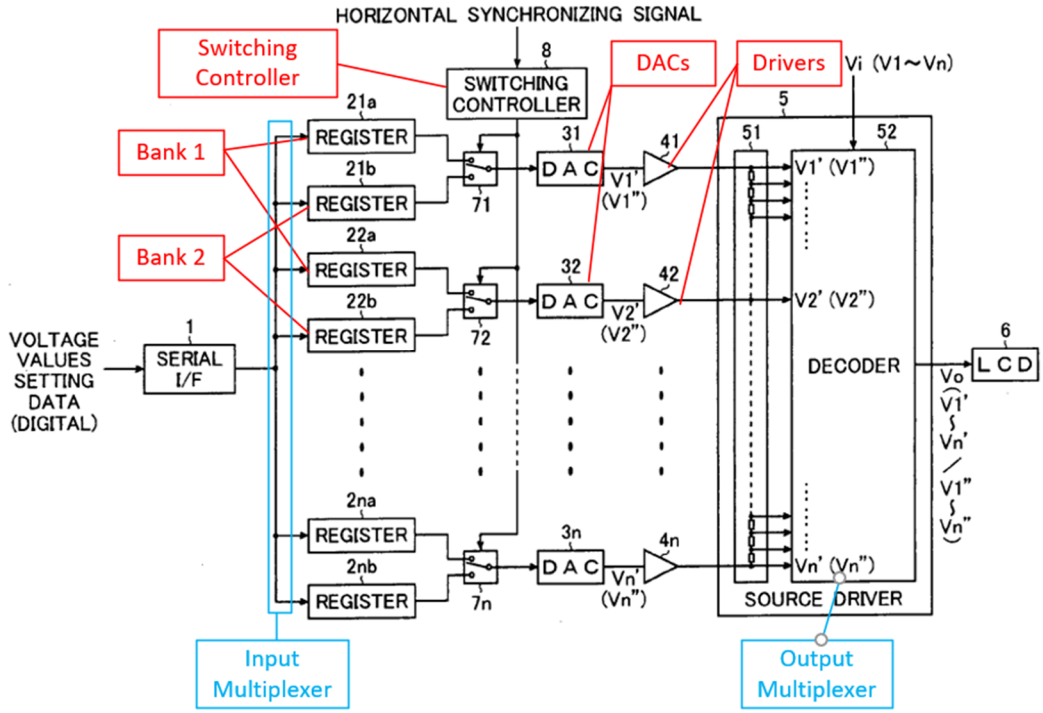
(EX1005, Fig. 3 (annotated)).

Nakata teaches that these registers can be implemented as non-volatile memories to easily store corrected values without a separate memory device. (EX1005, [0028]; EX1003, ¶92). While not explicitly called "storage cells," a POSITA would understand the non-volatile registers to be comprised of storage cells for holding individual digital data bits. (EX1003, ¶92). Therefore, Nakata's non-volatile registers correspond to the claimed plurality of non-volatile storage cells. (EX1003, ¶92).

3. Limitation 1[2]: circuits for programming coupled to a multiplexer for addressing and programming said storage cells, wherein the addressing is based on a plurality of inputs;

Nakata discloses this limitation. (EX1003, ¶93). Specifically, Nakata describes a serial interface 1 for distributing digital data to registers 21 to 2n.

(EX1005, [0017], [0020], Fig. 1; EX1003, ¶93). While not explicitly called a multiplexer, a POSITA would understand the serial interface 1 includes multiplexing functionality to route serial data to multiple registers based on addressing. (EX1003, ¶93). This can be seen in the figure below, labeled ("Input Multiplexer"), where the output from the Serial I/F component branches out to the various registers for programming, and is thus a "multiplexer" (EX1003, ¶93).



(EX1005, Fig. 3 (annotated)).

The addressing is based on the serial input data, which comprises a plurality of inputs. (EX1005, [0017], Fig. 1; EX1003, ¶94). Therefore, Nakata discloses programming circuits (serial interface 1) coupled to multiplexing functionality for

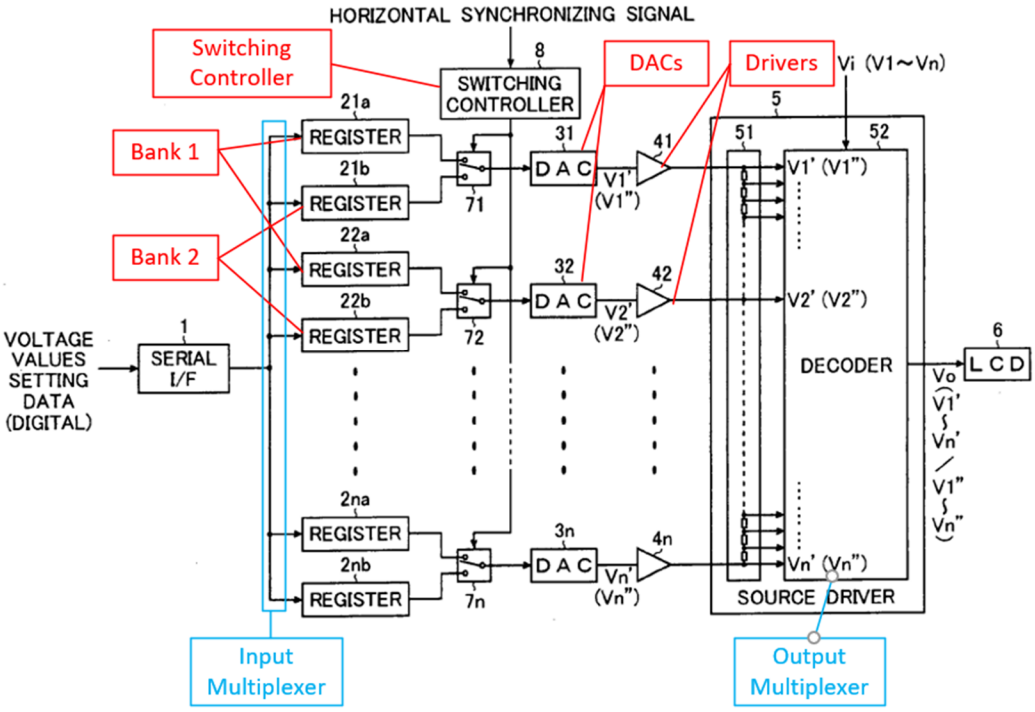
addressing and programming the registers (storage cells) based on plural inputs (serial data). (EX1003, ¶94).

4. Limitation 1[3]: drivers connected to said storage cells and to the plurality of outputs; and

Nakata discloses this limitation. (EX1003, ¶95). Specifically, Nakata discloses DACs 31 to 3n connected to the registers 21 to 2n (storage cells), and buffers 41 to 4n connected to the outputs of the DACs. (EX1005, [0017]-[0019], Fig. 1; EX1003, ¶95). The DACs and buffers together form drivers that convert the digital data in the registers to analog voltages and amplify them to drive the plurality of outputs. (EX1005, [0017]-[0019]; EX1003, ¶95). Therefore, Nakata clearly discloses the claimed drivers connected to both the storage cells and outputs. (EX1003, ¶95).

5. Limitation 1[4]: the plurality of inputs connected to said multiplexer for addressing said storage cells, wherein said voltage signals are gamma reference voltage signals for determining actual driving voltages of columns of a display,

Nakata discloses this limitation. (EX1003, ¶96). The serial input data (plurality of inputs) is used by the serial interface 1 (which includes multiplexing functionality) to address and program the registers. (EX1005, [0017], [0020], Fig. 1; EX1003, ¶96).



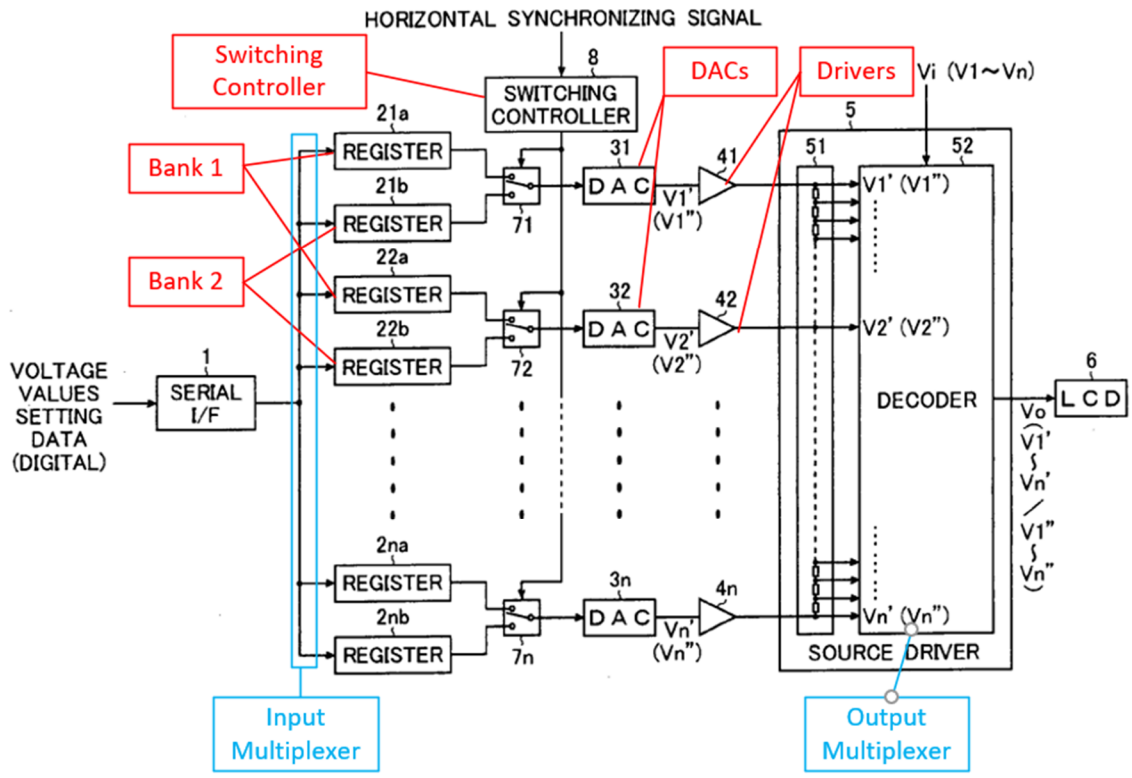
(EX1005, Fig. 3 (annotated)).

Nakata explicitly states that the output voltages V1' to Vn' are gamma correction voltages used for driving a liquid crystal display. (EX1005, [0017]-[0019], Fig. 1; EX1003, ¶97). These gamma correction voltages determine the actual driving voltages applied to the LCD columns via the source driver 5. (EX1005, [0018]-[0019], Fig. 1; EX1003, ¶97).

6. Limitation 1[5]: wherein said non-volatile storage cells are organized into two or more banks of cells wherein each bank contains a predetermined gamma reference voltage signal display condition; and

Nakata discloses this limitation. (EX1003, ¶98). Specifically, Nakata describes embodiments with multiple sets of registers (e.g. 21a/21b to 2na/2nb), where each set holds a different pattern of digital data for generating gamma

correction voltages. (EX1005, [0021]-[0027], Figs. 2-3; EX1003, ¶98). These are labeled below as Bank 1 and Bank 2 (EX1003, ¶98):

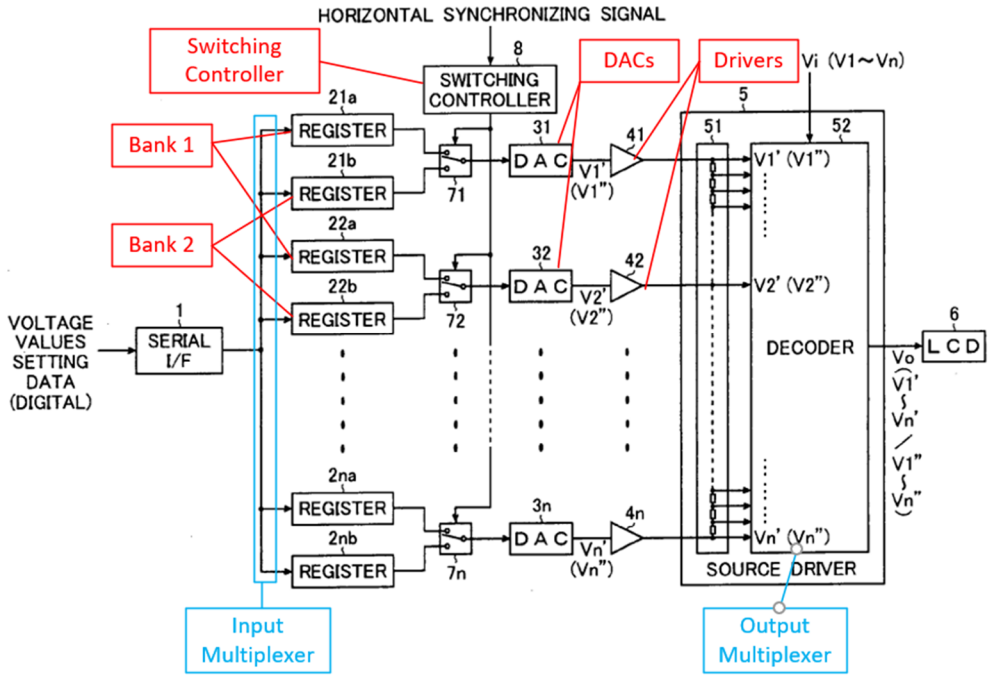


(EX1005, Fig. 3 (annotated)).

Each register set corresponds to a bank of storage cells containing data for a predetermined gamma voltage pattern (display condition). (EX1003, ¶99). Nakata teaches using these different patterns for various display conditions, such as odd vs. even scanlines. (EX1005, [0024]; EX1003, ¶99). A POSITA would understand the register sets to be organized banks of non-volatile storage cells as claimed. (EX1003, ¶99).

7. Limitation 1[6]: means to switch between the banks based on one or more external signals is provided on said integrated circuit.

Nakata discloses this limitation. (EX1003, ¶100). Specifically, Nakata describes a switching controller 8 that controls selectors 71 to 7n to switch between different sets (banks) of registers. (EX1005, [0022]-[0024], Fig. 2; EX1003, ¶100). The switching controller 8 switches banks based on scanline information, which is an external signal indicating which scanline is being driven. (EX1005, [0024]; EX1003, ¶100). This can be seen below in Fig. 3, labeled "Switching Controller":



(EX1005, Fig. 3 (Annotated)).

While not explicitly stated, a POSITA would understand the switching controller to be part of the same integrated gamma correction voltage generation

device, as integrating all components on a single chip was standard practice for display driver circuits at the time. (EX1005, [0029]-[0031]; EX1003, ¶101).

B. Claim 2: The integrated circuit of claim 1 wherein said non-volatile storage cells are reprogrammable.

Nakata discloses this limitation. (EX1003, ¶102). Specifically, Nakata teaches that the digital data held in registers 21 to 2n can be rewritten while checking the LCD image in real time. (EX1005, [0019]; EX1003, ¶102). Nakata further states that the registers can be implemented as non-volatile memories to easily store corrected values without a separate memory device. (EX1005, [0028]; EX1003, ¶102). A POSITA would understand from these disclosures that Nakata's registers are non-volatile reprogrammable storage cells for holding gamma correction data that can be repeatedly updated as needed to optimize display performance. (EX1003, ¶102).

C. Claim 3: The integrated circuit of claim 2 wherein said means to switch between banks can have a switching time from about 10 msec to about one second.

A POSITA would understand that Nakata discloses this limitation. (EX1003, ¶103). Nakata describes switching between register banks on a per-scanline basis using switching controller 8 and selectors 71-7n. (EX1005, [0022]-[0024], Fig. 2; EX1003, ¶103). While not explicitly stating a time, switching every few scanlines at typical display refresh rates (e.g. 60 Hz) would fall within the claimed 10 ms to 1 second range. (EX1003, ¶103). Additionally, Nakata's goal of enhancing image quality (EX1005, [0024]) implies switching fast enough to be imperceptible, which

a POSITA would understand to be within the claimed range given standard display timing parameters. (EX1003, ¶103)

D. Claim 4: The integrated circuit of claim 1 wherein said non-volatile storage cells hold analog voltage values which are a constant fraction of said gamma reference voltage signals.

A POSITA would understand that Nakata discloses this limitation. (EX1003, ¶104). While Nakata describes the registers storing digital data (EX1005, [0017-0019]; EX1003, ¶104), a POSITA would recognize this digital data directly represents specific analog voltage levels to be output by the DACs. (EX1005, Fig. 1; EX1003, ¶104). Since the DAC outputs are amplified by the buffers to produce the final gamma correction voltages (EX1005, [0017]; EX1003, ¶104), the analog values represented by the register data are necessarily a constant fraction (scaled-down version) of the output gamma voltages. (EX1003, ¶104). Therefore, Nakata's registers hold analog voltage values that are a constant fraction of the gamma reference signals. (EX1003, ¶104).

E. Claim 5: The integrated circuit of claim 1 wherein said circuits for programming require an external source for the high voltage programming means.

A POSITA would understand that Nakata discloses this limitation. (EX1003, ¶105). While Nakata does not explicitly state this, programming non-volatile memory typically requires higher voltages than normal operating voltages. (EX1003, ¶105). Nakata teaches storing the register data in non-volatile memory

after adjustments are completed. (EX1005, [0019]; EX1003, ¶105). A POSITA would recognize that programming this non-volatile memory would require an external high voltage source, as this is standard practice for integrated circuits with on-chip non-volatile memory. (EX1003, ¶105). The serial interface for programming the registers would necessarily include circuitry to interface with this external high voltage source for programming the non-volatile memory. (EX1005, Fig. 1, [0017-0019]; EX1003, ¶105).

F. Claim 8

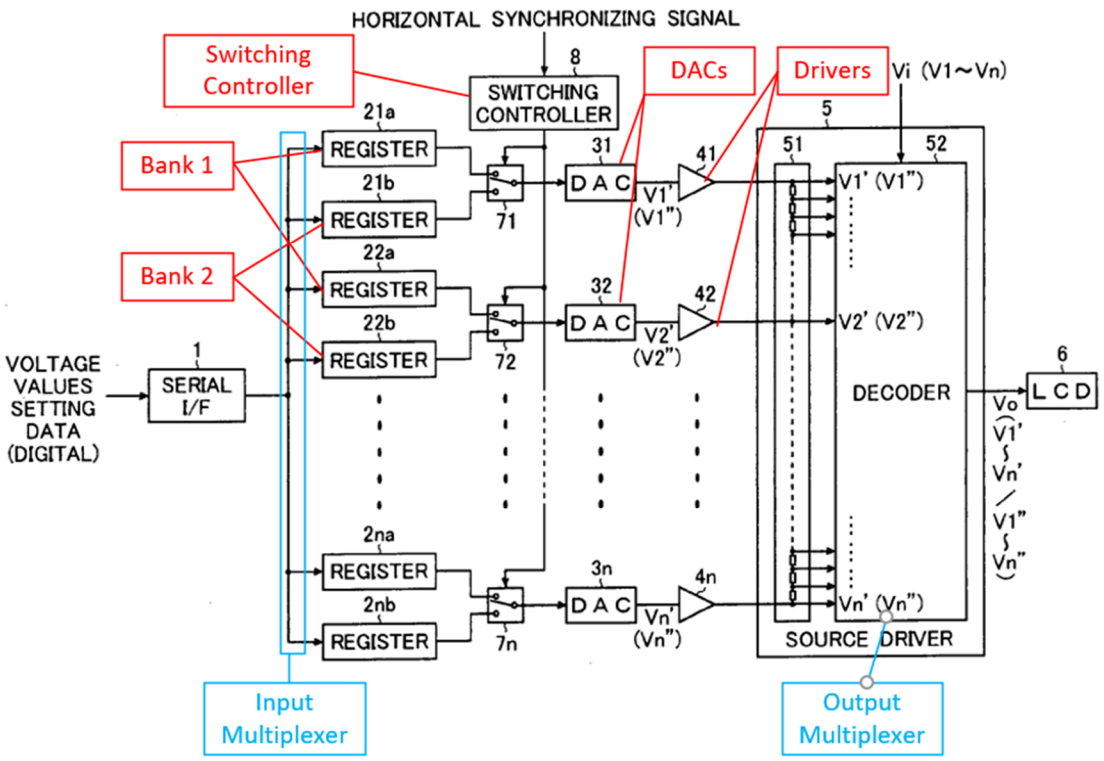
1. Limitations 8[0]-8[4]

Limitations 8[0]-8[4] are substantially identical to limitations 8[0]-8[4], and are disclosed in Nakata, as described *supra*, at § XII.A.1-5.

2. Limitation 8[5]: an output pin connected to an output through a second multiplexer connected to said plurality of outputs wherein said output pin is at an output buffer voltage level of said output when said integrated circuit is in a programming mode to program said storage for said output.

Nakata this limitation. (EX1005, [0018]; EX1003, ¶107). Specifically, Nakata describes a source driver 5 comprising a decoder 52 that selects and outputs a voltage Vo from among the gamma correction voltages V1' to Vn' or intermediate voltages generated by the resistance ladder 51. (EX1005, Fig. 1, [0018]; EX1003, ¶107). The decoder 52 corresponds to the claimed "second multiplexer." (EX1005, [0018]; EX1003, ¶107). This is because the decoder 52 couples one of many input voltages (V1' to Vn' or intermediate voltages) to one output voltage Vo. (EX1005, [0018];

EX1003, ¶107). The output voltage Vo is provided to the LCD 6, which requires an output pin, and this output pin would be at the voltage level of the selected gamma correction voltage or intermediate voltage when the device is in a mode for programming the gamma correction values stored in the registers. (EX1005, [0019]; EX1003, ¶107). This is labeled as "Output Multiplexer" in the figure below:



(EX1005, Fig. 3 (annotated)).

Therefore, Nakata discloses all elements of the claimed limitation. (EX1005, Fig. 1, [0018]-[0019]; EX1003, ¶108).

Claim 9

Claim 9 is substantially identical to Claim 2. Nakata discloses the features of Claim 9, as described *supra*, at § XII.B.

Claim 10

Claim 10 is substantially identical to limitations 1[5]-1[6]. Nakata, in view of Tsai, discloses these features, as described *supra*, at § XII.A.6-7.

Claim 11

Claim 11 is substantially identical to Claim 3. Nakata, in view of Tsai discloses these features, as described *supra*, at § XII.A.6-7.

Claim 12

Claim 12 is substantially identical to limitation 1[4]. Nakata, in view of Tsai, discloses these features, as described *supra*, at § XII.A.5.

Claim 13

Claim 13 is substantially identical to Claim 4. Nakata, in view of Tsai, discloses these features as described supra, at § XII.D.

Claim 14

Claim 14 is substantially identical to Claim 5. Nakata discloses these features as described *supra*, at § XII.E.

XIII. Ground 2: Claims 1-5 and 8-14 are Invalid as Obvious over Nakata, in view of Tsai

In the event that the Board does not find that Nakata discloses two "banks" of memory cells, Tsai does. A POSITA would have been motivated to combine Nakata

with Tsai to arrive at the claimed features. (EX1003, ¶115). Specifically, a POSITA would have been motivated to modify Nakata's gamma correction voltage generation device to incorporate Tsai's partitioned memory architecture with a loader block and user block. (EX1003, ¶115). This modification would have been obvious to try, as it would provide a known solution to the problem of efficiently reprogramming gamma correction data. (EX1007, 2:38-43; EX1003, ¶115)

Nakata discloses the need to rewrite gamma correction data while checking display output in real-time. (EX1005, [0019]; EX1003, ¶116). Tsai's partitioned memory architecture, with a loader block for storing a loader program and a user block for application data, offers a predictable solution to this problem. (EX1007, 3:5-13; EX1003, ¶116). A POSITA would recognize that incorporating Tsai's memory architecture into Nakata's device would allow for efficient reprogramming of gamma correction data without external tools, while maintaining normal display operation. (EX1007, 2:38-3:4; EX1003, ¶116)

Furthermore, a POSITA would be motivated to implement Tsai's switching mechanism between memory blocks in Nakata's device. (EX1003, ¶117). This modification would be a use of a known technique to improve a similar device, yielding the predictable result of more flexible gamma correction control. (EX1003, ¶117).

The combination would also benefit from Tsai's teaching of using a timer and interrupt system for managing the reprogramming process. (EX1007, 4:41-5:21; EX1003, ¶118). This modification would be applying a known technique to a known device ready for improvement to yield predictable results. (EX1003, ¶118).

A limitation-by-limitation analysis of Nakata is provided *supra*, at § XII. A limitation-by-limitation analysis of Tsai is provided below.

A. Claim 1

1. Limitation 1[0]

To the extent that the preamble is limiting, Tsai also discloses an integrated circuit for producing voltage signals on a plurality of outputs. (EX1003, ¶120). Tsai describes a microcomputer implemented as an integrated circuit that includes a microprocessor unit and embedded flash memory for generating and outputting voltage signals. (EX1007, 2:14-28, Fig. 3; EX1003, ¶120). The microcomputer produces gamma reference voltages, which are voltage signals, on multiple outputs to drive source drivers for a display. (EX1007, 1:19-27, 3:1-6, Fig. 3; EX1003, ¶120). Figure 3 shows the integrated circuit architecture with multiple output channels (CH0-CH7) for outputting the voltage signals. (EX1007, Fig. 3; EX1003, ¶120)

2. Limitation 1[1]

Even if Nakata does not disclose this limitation, Tsai discloses a plurality of non-volatile storage cells. Tsai describes an embedded flash memory unit within the

microcomputer. (EX1007, 1:24-33, 3:5-22, Fig. 2; EX1003, ¶121). Flash memory is a type of non-volatile memory that retains data without power. A POSITA would recognize that an embedded flash memory unit necessarily comprises multiple non-volatile storage cells to store data and programs, as individual storage cells are the fundamental building blocks of flash memory. (EX1003, ¶121). The loader block and user block described by Tsai (EX1007, Fig. 2) would each require numerous storage cells to store their respective programs. (EX1003, ¶121).

3. Limitation 1[2]

Even if Nakata does not disclose this feature, Tsai does. (EX1003, ¶89). Tsai discloses circuits for programming coupled to a multiplexer for addressing and programming storage cells, with addressing based on a plurality of inputs. (EX1003, ¶89). Tsai describes a microprocessor unit 310 coupled to a bus multiplexer 350 that addresses and programs the loader block 331 and user block 332 of the flash memory 330 during data reprogramming. (EX1007, 3:2-9, Fig. 3; EX1003, ¶89). The addressing is controlled by signals from the microprocessor unit, including a memory selection signal MSEL and bus selection signal BSEL, which determine which block is active and connected to the register set 340 for programming. (EX1007, 3:14-19, 7:49-67, Fig. 3; EX1003, ¶89). The MSEL and BSEL signals, along with address values stored in the address register 342, constitute the plurality of inputs for addressing. (EX1007, 3:14-19, 7:41-48, Fig. 3; EX1003, ¶89).

4. Limitation 1[3]

Even if Nakata does not disclose this limitation, a POSITA would understand that Tsai discloses drivers connected to the storage cells and outputs. (EX1003, ¶91). Tsai describes a microprocessor unit that manages data flow between a register set and flash memory blocks during programming and execution modes. (EX1007, 7:49-67, 8:37-47, Fig. 3; EX1003, ¶91). A POSITA would recognize that drivers are necessary components to interface between the microprocessor and flash memory for reading and writing operations. (EX1003, ¶91). The drivers are present to buffer and amplify signals between the storage cells in the flash memory and the outputs to the microprocessor and register set, enabling the described data transfer functionality. (EX1007, Fig. 3; EX1003, ¶91).

5. Limitation 1[4]

Tsai does not expressly disclose gamma reference voltage signals for determining driving voltages of display columns. (EX1003, ¶93). However, a POSITA would have found it obvious to adapt Tsai's programmable voltage generation system for this purpose. (EX1003, ¶93). Tsai discloses an integrated circuit that produces programmable voltage signals on multiple outputs using non-volatile storage cells and drivers. (EX1007, Fig. 3, 3:2-9, 7:10-19; EX1003, ¶93). A POSITA would recognize this architecture could be readily applied to generate gamma reference voltages, which are simply a set of programmable voltages used to drive display columns. The ability to program and store multiple voltage values

in Tsai's system (EX1007, 3:23-29) aligns well with the needs of gamma correction, where different voltage levels are required for optimal display performance. (EX1003, ¶93)

6. Limitation 1[5]

Tsai discloses that the non-volatile storage cells are organized into two or more banks. (EX1003, ¶95). Specifically, Tsai describes partitioning the embedded flash memory into a loader block and a user block. (EX1007, 3:5-13, Fig. 2; EX1003, ¶95). The loader block stores a loader program, while the user block stores application programs. (EX1007, 3:14-16, Fig. 2; EX1003, ¶95). A POSITA would understand these blocks to be analogous to banks containing predetermined display conditions, as the loader and application programs define different operational states of the display system. The blocks can be separately addressed and accessed to retrieve their respective programs for execution. (EX1007, 3:35-47, Fig. 3; EX1003, ¶95).

7. Limitation 1[6]

Tsai discloses a means to switch between banks based on external signals provided on the integrated circuit. (EX1003, ¶96). Specifically, Tsai describes a bus multiplexer that selectively connects either the loader block or user block to the microprocessor or register set based on external signals MSEL and BSEL from the microprocessor unit. (EX1007, 3:23-42, 7:49-67, Fig. 3; EX1003, ¶96). The MSEL

signal selects which memory block is active, while BSEL controls the bus multiplexer connections. (EX1007, Fig. 3; EX1003, ¶96). This switching mechanism allows the microcomputer to alternate between executing the loader program and writing new data to the user block during on-chip programming. (EX1007, 7:49-67; EX1003, ¶96).

B. Claim 2

Tsai discloses that the non-volatile storage cells are reprogrammable. (EX1003, ¶97). Tsai describes a microcomputer with embedded flash memory that has "on-chip programming capability that allows new data to be reprogrammed by the microcomputer itself into the embedded flash memory" (EX1007, Abstract; EX1003, ¶97). The flash memory is partitioned into a loader block and a user block, where the user block stores application programs that can be updated through reprogramming (EX1007, 2:62-3:6, Fig. 2; EX1003, ¶97). Tsai details a method for reprogramming data into the flash memory, including receiving new data, temporarily storing it, and writing it into the memory blocks (EX1007, 4:41-57, Fig. 5; EX1003, ¶97). This on-chip reprogramming capability is a key feature that allows updating the stored programs without external tools, clearly indicating the reprogrammable nature of the non-volatile storage cells.

C. Claim 3

A POSITA would have found it obvious to configure Tsai's switching time between banks to be from about 10 msec to about one second. (EX1003, ¶98). While Tsai does not expressly disclose this specific time range, Tsai teaches using a timer to control switching between memory blocks during programming. (EX1007, 4:41-5:21, Fig. 4; EX1003, ¶98). Tsai explains that the timer is set based on the time required to program one block of data. (EX1007, 8:30-37; EX1003, ¶98). A POSITA would have understood that flash memory programming typically takes on the order of milliseconds to seconds per block, and would have found it obvious to set Tsai's timer within the claimed range to allow sufficient time for programming while maintaining responsive operation. (EX1003, ¶98). The claimed range represents a straightforward optimization of Tsai's disclosed timing mechanism based on typical flash memory characteristics known to POSITAs. (EX1003, ¶98).

D. Claim 4

A POSITA would understand that Tsai, in combination with Nakata, discloses non-volatile storage cells holding analog voltage values which are a constant fraction of gamma reference voltage signals. (EX1003, ¶100). Tsai teaches an embedded flash memory unit partitioned into blocks for storing program data (EX1007, 6:15-26, Fig. 3; EX1003, ¶100). When incorporated into Nakata, the flash memory unit of Tsai would hold values that are analog voltage values which are a constant fraction of a gamma correction value. (EX1003, ¶100). Specifically, the digital

values would be constant, and would correlate to a fraction of a gamma correction value, such that when the digital values are converted to analog values (i.e. by a DAC), it would be a fraction of the gamma reference voltage applied to the DAC. (EX1003, ¶100). While Tsai does not explicitly describe storing analog voltages, a POSITA would recognize that flash memory cells store analog charge levels that correspond to discrete digital values. (EX1003, ¶100). In the context of gamma reference generation for displays, these stored analog levels would necessarily represent fractions of the full gamma reference voltage range. (EX1003, ¶100). Therefore, the non-volatile cells in Tsai hold analog voltages that are constant fractions of gamma reference signals when used for this purpose. (EX1003, ¶100).

E. Claim 5

Nakata discloses this feature. *See supra*, § XII.E.

F. Claim 8

1. Limitation 8[0]-8[4]

Limitations 8[0] to 8[4] are identical to Limitations 1[0] to 1[4]. Nakata discloses these features. *See supra*, § XII.A.1-5.

2. Limitation 8[5]

Nakata discloses this feature. *See supra*, § XII.F.2.

G. Claim 9

Claim 9 is substantially identical to Claim 2. Nakata, in view of Tsai discloses the features of Claim 9, as described *supra*, at § XII.B; XIII.B.

H. Claim 10

Claim 10 is substantially identical to limitations 1[5]-1[6]. Nakata, in view of Tsai, discloses these features, as described *supra*, at § XII.A.6-7, XIII.A.6-7.

I. Claim 11

Claim 11 is substantially identical to Claim 3. Nakata, in view of Tsai, discloses these features, as described *supra*, at § XII.A.6-7, XIII.A.6-7.

J. Claim 12

Claim 12 is substantially identical to limitation 1[4]. Nakata, in view of Tsai, discloses these features, as described *supra*, at § XII.A.5, XIII.A.5.

K. Claim 13

Claim 13 is substantially identical to Claim 4. Nakata, in view of Tsai, discloses these features as described *supra*, at § XII.D, XIII.D.

L. Claim 14

Claim 14 is substantially identical to Claim 5. Nakata discloses these features as described *supra*, at § XII.E, XIII.E.

XIV. Ground 3: Claims 1-5 and 8-14 are Invalid as Obvious over Petropoulos

Claims 1-5, and 8-14 are invalid as obvious over Petropoulos. Below is a limitation-by-limitation analysis of Petropoulous, showing where each limitation is found in the prior art. (EX1003, ¶137)

A. Claim 1

1. Limitation 1[0]

Petropoulos discloses a circuit for processing analog signals received from a sensor before outputting the signals to a display or other device. (EX1006 at Abstract; EX1003, ¶138). Petropoulos teaches that "[t]he memory array can be programmed with data corresponding to desired modifications, such as low and high offset voltage correction, low gain correction, and gamma correction." (EX1006 at Abstract; EX1003, ¶138). Given Petropoulos' teaching that "the quality of the reproduced image is particularly important especially in high-end imaging applications," a POSITA would have been motivated to implement the system of Petropoulos on a single integrated circuit. (EX1003, ¶138).

2. Limitation 1[1]

Petropoulos discloses "a plurality of non-volatile storage cells." (EX1003, ¶139). Specifically, Petropoulos describes an "analog/multi-level memory array" containing multiple "memory cells" that retain stored data even when power is removed. (EX1006, 3:9-19, 5:19-28, Fig. 3; EX1003, ¶139). These non-volatile memory cells are used to store modification voltages for adjusting sensor array outputs. (EX1006, 4:11-25; EX1003, ¶139). Figure 3 shows a memory array 210 with MxN memory cells C11 to CMN, each implemented as a non-volatile floating gate transistor. (EX1006, 5:19-28, Fig. 3; EX1003, ¶139). A POSITA would have understood these cells retain their stored analog values when powered off, meeting the non-volatile storage cell limitation. (EX1003, ¶139).

3. Limitation 1[2]

Petropoulos discloses an address signal generator which "provides address signals indicating a row address and a column address for a selected one of memory cells C11 to CMN to which the data value will be written." (EX1006 at [0031]; EX1003, ¶140). A POSITA would have understood that this circuit for programming and addressing storage cells is necessarily based on multiple inputs. (See EX1006 at Fig. 3; EX1003, ¶140). Petropoulos teaches that the address signal generator "can be a buffer circuit that generates the address signals from address [sic] provided by circuitry external to memory 300, or . . . can generate sequential addresses for recording analog or multi-level samples of a continuous analog signal." (EX1006 at [0031]; EX1003, ¶140). A POSITA would have understood that the addressing is based on a plurality of inputs to select any memory cell, and that the decoder tree and other elements within the memory are circuits for programming. (EX1003, ¶140).

4. Limitation 1[3]

Petropoulos discloses a multiplier circuit that applies gamma voltages to the sensor data connected to the memory array, which stores gamma correction values. (EX1006 at Fig. 7, [0050]; EX1003, ¶141). The multiplier circuit includes an op amp, which a POSITA would understand is a driver because it "multiplies the input voltage Vs from individual sensor elements in the image sensor by a corresponding

gamma correction factor Vgc stored in the gamma correction memory array." (EX1006 at [0050]; EX1003, ¶141).

5. Limitation 1[4]

As discussed above, Petropoulos discloses an address signal generator that selects where data is written into the storage cells. (EX1006 at [0031]; EX1003, ¶142). Petropoulos describes a plurality of inputs connected to a decoder tree which accepts multiple inputs from the address signal generator to address the storage cells. (EX1006 at Fig. 4; EX1003, ¶142). Petropoulos teaches that "[w]hen writing a data value, an address signal generator 320 provides address signals indicating a row address and a column address for a selected one of memory cells C11 to CMN to which the data value will be written. (EX1006 at [0031]; EX1003, ¶142). A POSITA would understand that the use of the plural (i.e., signals), indicates the use of a plurality of inputs. (EX1003, ¶142).

Petropoulos also teaches that the correction signals can be gamma correction values for gamma correction of visual displays. (EX1006 at [0026]; EX1003, ¶143). These gamma correction factors are voltages Vgc which are combined with the signal voltage Vs by the op amp, (*See* EX1006 at Fig. 7, [0050]; EX1003, ¶143). Because the resultant voltages are output to a visual display device, a POSITA would have understood that these gamma correction factors are used to determine actual driving voltages for columns of the display. (EX1003, ¶143)

6. Limitation 1[5]

Petropoulos discloses "a plurality of memory arrays 210, each being programmed and stored with voltages for a different modification function, [so that] a variety of modifications to the sensor element voltages can be performed." (EX1006 at [0051]; EX1003, ¶144). Petropoulos further describes other embodiments in which "a single analog/multi-level memory array can be used in conjunction with a decoder for multiple types of modifications." (EX1006 at [0053]; EX1003, ¶144). Petropoulos teaches that in these embodiments, the decoder "determines the type of modification for a particular voltage from an image sensor element and accesses the desired voltage from the memory array," then supplies the voltages to the appropriate modification circuit. (*Id.).* A POSITA would have understood that multiple memories, or multiple types of modifications within a single memory, correspond to multiple banks of storage cells because different levels correspond to different groups, *i.e.,* banks. (EX1003, ¶144). Moreover, a POSITA would have understood that these types of memory could be used for display gamma correction. (EX1003, ¶144)

7. Limitation 1[6]

Petropoulos discloses the use of a decoder to access the desired voltage from a memory array. (EX1006 at [0053]; EX1003, ¶145). Petropoulos teaches that "a desired one of the memory arrays 210 is selected for a particular modification." (EX1006 at [0051]; EX1003, ¶145). A routing circuit 220 selects the desired

modification. (EX1006 at [0027]; EX1003, ¶145). A POSITA would have understood that a decoder, which selects a location in the memory array, is a means to switch between the banks based on external signals, *i.e.,* the routing circuit. (EX1003, ¶145).

B. Claim 2

Petropoulos discloses that the non-volatile storage cells, *i.e.,* the memory arrays, "can be reprogrammed." (EX1006 at [0054]; EX1003, ¶145).

C. Claim 3

A POSITA would have found it obvious to implement the switching time between banks in Petropoulos to be from about 10 msec to about one second based upon the POSITA's knowledge that such a switching would be unnoticeable by the viewer of the display. (EX1003, ¶146). While Petropoulos does not explicitly specify a switching time, it discloses reprogrammable memory arrays that can be updated to correct sensor outputs over time. (EX1006, 2:64-3:8, 9:44-51; EX1003, ¶146). A POSITA would have understood that switching between banks too quickly could cause display artifacts, while switching too slowly would be inefficient and may impact display quality. (EX1003, ¶146). Therefore, a POSITA would have been motivated to implement a switching time in the claimed range to balance smooth transitions with responsiveness, which represents a routine optimization within the prior art. (EX1003, ¶146). Specifically, a POSITA could have used a low-pass filter

– a common and well-understood component in electronic systems – to effectively filter out the harsh transition between banks. (EX1003, ¶146)

D. Claim 4

A POSITA would have understood that Petropoulos discloses non-volatile storage cells holding analog voltage values which are a constant fraction of gamma reference voltage signals. (EX1003, ¶147). Petropoulos teaches using an analog/multi-level memory array to store voltages for gamma correction of display signals. (EX1006, 2:64-3:8, 4:11-25, Fig. 7; EX1003, ¶147). A POSITA would have recognized that gamma correction typically involves multiplying input voltages by constant fractional values to achieve the desired non-linear response. (EX1003, ¶147). Thus, the analog voltages stored in Petropoulos' memory for gamma correction would necessarily be constant fractions of the gamma reference voltages in order to properly perform the gamma correction function when multiplied with the input signals. (EX1003, ¶147)

E. Claim 5

Petropoulos discloses a programming voltage Vpp that is used to program voltages into the memory. (EX1006 at [0032]; EX1003, ¶148). Petropoulos also teaches that "[i]f memory array 210 is a Flash memory array, typical programming voltages Vpp and Vdp are respectively about 12 volts and about 6 volts above voltage Vss. (Id.). A POSITA would have understood that these voltage levels are

high voltages. (EX1003, ¶148). Moreover, it would have been obvious to a POSITA to supply the voltage using an external source. (See EX1006 at Fig. 3; EX1003, ¶148).

F. Claim 8

1. Limitations 8[1]-8[4]

Limitations 8[0] to 8[4] are identical to Limitations 1[0] to 1[4]. Petropoulous discloses these features. *See supra*, § XIV.B.1-5.

2. Limitation 8[5]

While Petropoulos does not expressly disclose an output pin connected through a second multiplexer to the plurality of outputs, a POSITA would have found this limitation obvious. (EX1003, ¶149). Petropoulos teaches using a decoder to selectively route sensor outputs and stored modification values to a modification circuit. (EX1006, 9:38-47, Fig. 8; EX1003, ¶149). A POSITA would have understood that implementing this selective routing functionality with a multiplexer connected to an output pin would have been an obvious and straightforward design choice to enable reading out the modified sensor values during programming. (EX1003, ¶149). Using a multiplexer to selectively output signals was a well-known technique that a POSITA would have readily applied to achieve the predictable result of selectively outputting the modified sensor values in Petropoulos' system. (EX1003, ¶149).

G. Claim 9

Claim 9 is substantially identical to Claim 2, but differs only in that it depends from Claim 8, rather than Claim 1. Petropoulous discloses the features of Claim 9, as described *supra*, at § XIV.B.

H. Claim 10

Claim 10 is substantially identical to limitations 1[5]-1[6]. Petropoulous discloses these features, as described *supra*, at § XIV.A.6-7.

I. Claim 11

Claim 11 is substantially identical to Claim 3. Petropoulous discloses these features, as described *supra*, at § XIV.A.6-7.

J. Claim 12

Claim 12 is substantially identical to limitation 1[4]. Petropoulous discloses these features, as described *supra*, at § XIV.A.5.

K. Claim 13

Claim 13 is substantially identical to Claim 4. Petropoulous discloses these features as described *supra*, at § XIV.D.

L. Claim 14

Claim 14 is substantially identical to Claim 5. Petropoulous discloses these features as described *supra*, at § XIV.E.

XV. Ground 3: Claims 1-5 and 8-14 are Invalid as Obvious over Petropoulos in view of Tsai

In the event that the Board finds that Ground 2 is insufficient to show the claimed multiplexer, Petitioner submits that Tsai, in combination with Petropoulos, renders obvious the claimed multiplexer. (EX1003, ¶155). Specifically, a POSITA would have been motivated to incorporate Tsai's bank switching mechanism into Petropoulos' system to enable dynamic selection between multiple sets of gamma correction values. (EX1003, ¶155). This modification would have been obvious to try, as it would provide the predictable benefit of allowing Petropoulos' system to efficiently switch between different gamma correction curves for various display conditions or user preferences. (EX1006, 2:29-35; EX1007, 3:23-42, 7:49-67; EX1003, ¶155).

Each of the limitations of the challenged claims are present in Petropoulos, as described *supra*, at § XIV, or in Tsai, as described *supra*, at XIII.

XVI. Ground 4: Claims 1-5 and 8-14 are Invalid as Obvious over Nakata, in view of Tsai, in further view of Yamazaki

In the event that the Board finds that Ground 1 is insufficient because the combination of Nakata and Tsai does not adequately disclose nonvolatile storage cells, Yamazaki, which expressly discloses such storage cells, does. (EX1003, ¶154).

A POSITA would have been motivated to combine Nakata with Tsai and Yamazaki to arrive at the claimed features. (EX1003, ¶155). Specifically, a POSITA would have been motivated to modify Nakata's gamma correction voltage generation device to incorporate the multiple banks of non-volatile storage cells and switching means disclosed in Tsai and Yamazaki. (EX1003, ¶155).

Nakata teaches storing gamma correction data in registers that can be implemented as non-volatile memory. (EX1005, [0028]; EX1003, ¶156). A POSITA would have been motivated to incorporate Tsai's teaching of partitioning memory into multiple blocks, each containing different display conditions, as this would allow for storing multiple gamma correction profiles. (EX1007, 3:5-13; EX1003, ¶156). This modification would have been a simple substitution of Tsai's partitioned memory structure for Nakata's single set of registers, yielding the predictable result of increased flexibility in gamma correction. (EX1003, ¶156)

Furthermore, a POSITA would have been motivated to incorporate Yamazaki's teaching of storing multiple sets of gamma correction data and switching between them based on external signals. (EX1008, 7:21-26, 19:35-55; EX1003, ¶157). The combination would have been obvious to try, as there are a finite number of ways to implement multiple gamma correction profiles, and Yamazaki's approach provides clear benefits. (EX1003, ¶157).

Regarding the switching time, while not explicitly disclosed, a POSITA would have found it obvious to implement a switching time between 10 msec and 1 second. (EX1003, ¶158). Tsai teaches using a timer and interrupt system for memory operations (EX1007, 4:41-5:21), and Yamazaki discloses a high-speed integrated design (EX1008, 19:56-65). (EX1003, ¶158). A POSITA would have recognized that implementing switching within the claimed range would balance system responsiveness and power efficiency, applying known techniques to yield predictable results. (EX1003, ¶161).

These modifications to Nakata would have been straightforward applications of known techniques in display driver circuits, motivated by the desire to improve display quality and flexibility in gamma correction. (EX1003, ¶159).

A limitation-by-limitation analysis of Nakata and Tsai is provided *supra*, at § XII, XIII, and is not repeated here. Below is an analysis of where in Yamazaki each limitation is found.

A. Claim 1

1. Limitation 1[0]

Yamazaki discloses an integrated circuit for producing voltage signals on a plurality of outputs. (EX1003, ¶164). Yamazaki describes a semiconductor display device correcting system that includes a control circuit, memory elements, and other components for gamma correction integrally formed on an insulating substrate. (EX1008, 8:6-24, Fig. 7B; EX1003, ¶164). This integrated system produces voltage

signals on multiple outputs to drive the display pixels. (EX1008, 5:60-6:9; EX1003, ¶164). Specifically, Yamazaki discloses that the gamma correction control circuit outputs corrected voltage signals to a source signal line side driver, which then selects corresponding pixel TFTs to write picture information. (EX1008, 6:3-9, Fig. 1; EX1003, ¶164). This demonstrates an integrated circuit producing voltage signals on multiple outputs to drive the display. (EX1003, ¶164)

2. Limitation 1[1]

Yamazaki discloses a plurality of non-volatile storage cells. (EX1003, ¶165). Specifically, Yamazaki describes a nonvolatile memory composed of FAMOS type TFTs with floating gates for storing gamma correction data. (EX1008, 8:16-34, 9:16-17; EX1003, ¶165). The memory includes multiple storage elements arranged in a matrix, with each element comprising a P-channel FAMOS TFT and an N-channel switching TFT. (EX1008, 8:16-34, Fig. 3; EX1003, ¶165). This matrix arrangement of multiple non-volatile memory elements clearly constitutes a plurality of non-volatile storage cells as claimed.

3. Limitation 1[2]

Yamazaki discloses circuits for programming coupled to a multiplexer for addressing and programming storage cells based on multiple inputs. (EX1003, ¶166). The gamma correction control circuit 102 interacts with nonvolatile memory 103 to adjust voltage levels based on input signals. (EX1008, 5:60-6:9, Fig. 1;

EX1003, ¶166). This process involves addressing and programming memory cells. The system uses multiple inputs, including digital picture signals from signal generator 101 and feedback signals from digital signal processor 108, to control the addressing and programming. (EX1008, 6:39-46, Fig. 1; EX1003, ¶166). The X-address decoder 301 and Y-address decoder 302 act as multiplexers to select specific memory elements for programming based on these inputs. (EX1008, 8:43-49, Fig. 3; EX1003, ¶166).

4. Limitation 1[3]

Yamazaki discloses drivers connected to storage cells and to the plurality of outputs. (EX1003, ¶167). Specifically, Yamazaki describes a source signal line side driver 104 and gate signal line side driver 105 that are connected to the nonvolatile memory 103 (storage cells). and to the pixel region 106 (plurality of outputs). (EX1008, Fig. 1, 6:10-28; EX1003, ¶167). The source and gate drivers receive gamma-corrected signals from the gamma correction control circuit 102, which retrieves data from the nonvolatile memory 103, and provide those signals to drive the pixels in the pixel region 106. (EX1008, 6:14-28; EX1003, ¶167). This configuration directly connects the drivers to both the storage cells and outputs as claimed. (EX1003, ¶167).

5. Limitation 1[4]

Yamazaki discloses the plurality of inputs connected to said multiplexer for addressing said storage cells, wherein said voltage signals are gamma reference voltage signals for determining actual driving voltages of columns of a display. (EX1003, ¶168). Yamazaki describes a gamma correction control circuit 102 connected to a nonvolatile memory 103 via a multiplexer, where the memory stores gamma correction data used to adjust voltage levels for driving display columns. (EX1008, Fig. 1, 5:60-6:9; EX1003, ¶168). The gamma correction control circuit 102 uses inputs to address the storage cells in memory 103 to retrieve the appropriate gamma correction data. (EX1008, 6:10-28; EX1003, ¶168). This gamma correction data is then used to generate gamma reference voltages that determine the actual driving voltages applied to the display columns via the source signal line side driver 104. (EX1008, Fig. 1, 6:29-46; EX1003, ¶168).

6. Limitation 1[5]

Yamazaki discloses non-volatile storage cells organized into two or more banks, each containing a predetermined gamma reference voltage signal display condition. (EX1003, ¶169). Yamazaki teaches storing "multiple sets of gamma values" to "provide optimized gamma correction curves for different user or application requirements." (EX1008, 2:24-28; EX1003, ¶169). These multiple sets correspond to banks of cells, each set providing gamma correction for a different display condition. (EX1003, ¶169). Yamazaki further discloses that "when all

gamma correction data of gradation signals are stored in the memory 103, the signal generator 101 and the digital signal processor 108 are detached from the liquid crystal panel." (EX1008, 5:60-63, Fig. 1; EX1003, ¶169). This indicates the gamma correction data is organized into multiple sets (banks) in the non-volatile memory 103, allowing different gamma corrections to be applied for various display conditions without external components. (EX1003, ¶169).

7. Limitation 1[6]

Yamazaki does not expressly disclose means to switch between banks based on external signals. (EX1003, ¶170). However, a POSITA would have found this limitation obvious in view of Yamazaki's teachings. (EX1003, ¶170). Yamazaki discloses storing multiple sets of gamma correction data in nonvolatile memory to provide different gamma correction curves for different requirements. (EX1008, 2:24-28, Fig. 3; EX1003, ¶170). A POSITA would have understood that to utilize these different stored gamma curves, some means of switching between them based on external signals (e.g. user input or sensor data) would be necessary and obvious to implement on the integrated circuit. (EX1003, ¶170). This would allow dynamically selecting the appropriate gamma correction for different display conditions or user preferences, as suggested by Yamazaki. (EX1008, 7:20-32; EX1003, ¶170).

B. Claim 2

Yamazaki discloses that the non-volatile storage cells are reprogrammable. Yamazaki describes a nonvolatile memory comprised of FAMOS (Floating gate Avalanche injection MOS) type TFTs for storing gamma correction data. (EX1008, 8:16-34, Fig. 3; EX1003, ¶171). A POSITA would understand that FAMOS cells are reprogrammable due to their floating gate structure, which allows electrical erasure and reprogramming. (EX1003, ¶171). Yamazaki further confirms the reprogrammable nature by stating that the storage content of the memory elements "can be erased by irradiation of X-rays, ultraviolet rays, or electron beams, or by application of heat." (EX1008, 9:9-12; EX1003, ¶171). This disclosure of erasure methods indicates the ability to reprogram the non-volatile storage cells. (EX1003, ¶171).

C. Claim 3

A POSITA would understand that Yamazaki discloses a means to switch between banks with a switching time from about 10 msec to about one second. (EX1003, ¶172). Yamazaki describes integrating a control circuit, nonvolatile memory, and volatile memory on the same substrate to enable "high speed operations" when switching between stored gamma correction data banks. (EX1008, 19:21-34, 19:35-55, 19:56-65; EX1003, ¶172). While a specific switching time is not explicitly stated, a POSITA would recognize that integrating these components on a single substrate to achieve "high speed operations" necessarily results in

switching times within the claimed 10 msec to 1 second range, which was typical for such integrated memory systems at the time of the invention. (EX1003, ¶172).

D. Claim 4

A POSITA would understand that Yamazaki discloses that the non-volatile storage cells hold analog voltage values which are a constant fraction of the gamma reference voltage signals. (EX1003, ¶173). Yamazaki discloses that the nonvolatile memory stores gamma correction data used to adjust voltage levels corresponding to image gradations. (EX1008, 3:30-37, 3:52-4:5; EX1003, ¶173). The stored gamma correction data represents analog voltage values that are constant fractions of the gamma reference voltages, as this is necessary to achieve the desired gradation adjustments across the full range of reference voltages. (EX1003, ¶173). A POSITA would recognize that storing fractional values, rather than absolute voltages, allows the system to flexibly apply gamma correction across different voltage ranges. (EX1003, ¶173).

E. Claim 5

Yamazaki discloses that the circuits for programming require an external source for the high voltage programming means. (EX1003, ¶174). Specifically, Yamazaki describes that during the writing operation of the memory element, "a high voltage of 50 V is applied to the signal line C1." (EX1008, 8:54-61; EX1003, ¶174). This disclosure of applying a high 50V signal implies the necessity of an

external high voltage source, as such a high voltage would not be internally generated within the integrated circuit itself. (EX1003, ¶174). A POSITA would understand that this externally-supplied high voltage is crucial for programming the nonvolatile memory cells described by Yamazaki. (EX1008, 9:6-9; EX1003, ¶174).

F. Claim 8

1. Limitation 8[0]-8[4]

Limitations 8[0] to 8[4] are identical to Limitations 1[0] to 1[4]. The combination of Nakata and Tsai disclose these features. *See supra*, § XII.A.1-5, XIII.A.1-5.

2. Limitation 8[5]

Yamazaki does not expressly disclose an output pin connected to an output through a second multiplexer, wherein this output pin is at an output buffer voltage level of said output when the integrated circuit is in a programming mode. (EX1003, ¶175). While Yamazaki discusses output interactions for driving display pixels and signal processing (EX1008, 6:47-57; EX1003, ¶175), it does not specifically describe the claimed output pin configuration with a second multiplexer. However, a POSITA would have found it obvious to implement such an output configuration to enable programming and verification of the nonvolatile memory cells while maintaining normal display output functionality. (EX1003, ¶175). Adding a multiplexed output pin connected to the memory cell outputs would allow for

efficient programming and readback without disrupting the display operation. (EX1008, Fig. 3, 6:22-36, 12:26-35; EX1003, ¶175)

G. Claim 9

Claim 9 is substantially identical to Claim 2. The combination of Nakata and Tsai disclose the features of Claim 9, as described *supra*, at § XII.B, XIII.B.

H. Claim 10

Claim 10 is substantially identical to limitations 1[5]-1[6]. The combination of Nakata and Tsai disclose these features, as described *supra*, at § XII.A.6-7; XIII.A.6-7.

I. Claim 11

Claim 11 is substantially identical to Claim 3. The combination of Nakata and Tsai discloses these features, as described *supra*, at § XII.A.6-7, XIII.A.6-7.

J. Claim 12

Claim 12 is substantially identical to limitation 1[4]. The combination of Nakata and Tsai disclose these features, as described *supra*, at § XI.A.5, XIII.A.5.

K. Claim 13

Claim 13 is substantially identical to Claim 4. The combination of Nakata and Tsai disclose these features as described *supra*, at § XI.D, XII.D.

L. Claim 14

Claim 14 is substantially identical to Claim 5. Nakata discloses these features as described *supra*, at § XII.E.

XVII. Ground 5: Petropoulos in view of Yamazaki

In the event that the Board finds that Ground 2 is insufficient because Petropoulos does not adequately disclose memory cells stored in banks, Petitioner submits that Yamazaki, which expressly discloses such storage cells, does. (EX1003, ¶181). A POSITA would have been motivated to combine Petropoulos with Yamazaki to arrive at the claimed features. (EX1003, ¶181). Specifically, a POSITA would have been motivated to modify Petropoulos to include means to switch between banks of gamma reference voltage signals based on external signals, as taught by Yamazaki. (EX1003, ¶181). This modification would have been obvious to try, as it would allow dynamically selecting appropriate gamma correction for different display conditions or user preferences, providing optimized image quality. (EX1008, 2:24-28, 7:20-32; EX1003, ¶181). The combination would have yielded predictable results, as both references relate to gamma correction for displays using stored reference values. (EX1006, 2:29-35; EX1008, 5:60-6:9; EX1003, ¶181)

A limitation-by-limitation analysis of Petropoulos is provided *supra*, at § XIV, and a limitation-by-limitation analysis of Yamazaki is provided supra, at § XVI, and they are not repeated here.

XVIII. Ground 6: Petropoulos in view of Tsai in further view of Yamazaki

In the event that the Board finds that Grounds 2 and/or 4 are insufficient on their own, Petitioner submits that Petropoulous, in view of Tsai, in further view of

Yamazaki overcomes these challenges. A motivation to combine Petropoulous with Tsai is provided above *supra*, at § XV. A further motivation to combine Petropoulous with Yamazaki is provided above, *supra*, at § XVII.

A limitation-by-limitation analysis of Petropoulous is provided *supra*, at § XIV, a limitation-by-limitation analysis of Tsai is provided supra, at § XIII, and a limitation-by-limitation analysis of Yamazaki is provided supra, at § XV.

XIX. Conclusion

For the foregoing reasons, Petitioner respectfully requests that the Board institute an *Inter Partes* Review, and find that each of Claims 1-5 and 8-14 are invalid.

Dated: October 15, 2024

Respectfully submitted,

/Jeffrey Johnson/
Jeffrey Johnson
Reg. No. 53,078
Attorney for Petitioner

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,233,305 contains, as measured by the word-processing system used to prepare this paper, 13,983 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Dated: October 15, 2024

Respectfully submitted,

/Jeffrey Johnson/
Jeffrey Johnson
Reg. No. 53,078
Attorney for Petitioner

CERTIFICATE OF SERVICE UNDER 37 C.F.R. § 42.105

I hereby certify that on October 15, 2024, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,233,305 and supporting exhibits to be served via FedEx Express® or Express Mail on the Patent Owner at the following correspondence address of record as listed on the USPTO Patent Center:

WOMBLE BOND DICKINSON (US) LLP
ATTN: IP DOCKETING
P.O. Box 570489
ATLANTA, GA 30357-0037
UNITED STATES

A courtesy copy was also served via electronic mail on Patent Owner's litigation counsel:

Fabio Elia Marino (Fabio.marino@wbd-us.com)
Katherine Lange Johnson (kate.johnson@wbd-us.com)
Nicolas S Gikkas (nsg@gikkaslaw.com)
Rodney RaShard Miller (Rodney.miller@wbd-us.com)
Steven Mark Levitan (steve.levitan@wbd-us.com)
Eric Hugh Findlay (efindlay@findlaycraft.com)

Dated: October 15, 2024

Respectfully submitted,

/Jeffrey Johnson/
Jeffrey Johnson (Reg. No. 53,078)
Attorney for Petitioner