IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

***In re* Patent of:**	Hampel, et al.	§	**Docket No.:**	M80673235-466
		§		
U.S. Patent No.:	9,160,466	§	**Customer No.:**	196553
		§		
Issue Date:	October 13, 2015	§	**Group Art Unit:**	N/A
		§		
Filing Date:	November 6, 2014	§	**Examiner:**	N/A
		§		
Patent Title:	Periodic Calibration for Communication Channels By Drift Tracking			

REQUEST FOR *EX PARTE* REEXAMINATION OF
U.S. PATENT 9,160,466

Patent Center Filed
Mail Stop *Ex Parte* Reexam
Commissioner for Patents
United States Patent and Trademark Office
P. O. Box 1450
Alexandria, VA 22313-1450

TABLE OF CONTENTS

LIST OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 9,160,466 (The ’466 Patent)
1002	Declaration of R. Jacob Baker, Ph.D., P.E.in Support of Request for *Ex Parte* Reexamination of U.S. Patent No. 9,160,466 (“Baker Declaration”)
1003	Curriculum Vitae of R. Jacob Baker, Ph.D., P.E.
1004	U.S. Patent Publication No. 2003/0070123 A1 (“Meaney”)
1005	U.S. Patent Publication No, 2003/0151450 A1 (“Nguyen”)
1006	U.S. Patent No. 6,356,106 (“Greef”)
1007	U.S. Patent No. 6,255,979 (“Allee”)
1008	File History of U.S. Patent No. 9,160,466
1009	Patent Trial and Appeal Board (PTAB) Decision Regarding Granting Institution of Petition for *Inter Partes* Review
1010	Patent Trial and Appeal Board (PTAB) Decision Regarding Termination Due to Settlement After Institution of Trial 35 U.S.C. § 317, 37 C.F.R. § 42.74
1011	Disclaimer in a Patent Under 35 USC §1.321(a) regarding Patent Number 8,929,424, filed 11/6/2014

I. INTRODUCTION

Pursuant to 35 U.S.C. §§ 302-307 and 37 C.F.R. § 1.510, the undersigned, on behalf of NXP USA, Inc. (hereinafter "NXP"), hereby requests *ex parte* reexamination of claims 1-19 of U.S. Patent No. 9,160,466 ("the ’466 Patent"), entitled "Periodic Calibration for Communication Channels by Drift Tracking" a copy of which is attached as Exhibit 1001. The ’466 Patent was issued on October 13, 2015, to Rambus Inc. and was originally assigned to Rambus Inc.; the ’466 Patent is now assigned to K.MIZRA LLC. The ’466 Patent issued from Application No. 14/535,006 filed on 11/06/2014, and is a continuation of Application No. 14/145,966, filed on 01/01/2014, issued as U.S. Patent 8,929,424, which is a continuation of Application No. 13/452,543, filed on 04/20/2012, issued as U.S. Patent 8,644,419, which is a continuation of Application No. 12/173,530, filed on 07/15/2008, issued as U.S. Patent 8,165,187, which is a continuation of Application No. 11/754,107, filed on 05/25/2007, issued as U.S. Patent 7,400,671, which is a continuation of Application No. 10/766,761, filed on 01/28/2004, U.S. Patent 7,400,670.

The ’466 Patent is at issue in the United States District Court for the Western District of Texas. *See K.MIZRA LLC v. NXP USA, INC.*, Civil Action No. 7:25-cv-00304-DC-DTG (W.D. Tex.). Because this patent is involved in concurrent litigation, the USPTO should accord it priority. *See* MPEP § 2261 (“Any cases involved in litigation, whether they are reexamination proceedings or reissue applications, will have priority over all other cases.”).

The ’466 Patent was the subject of a Petition for *Inter Partes* Review (IPR), which was granted institution on March 5, 2025 and was terminated on March 14, 2025 due to Settlement After Institution of Trial 35 U.S.C. § 317; 37 C.F.R. § 42.74. Copies of each are attached hereto as Exhibits 1009 and 1010.

This *ex parte* reexamination request (“Request”) presents substantially new questions (“SNQ”) of patentability for claims 1-19 (“challenged claims”) in comparison to the patentability questions raised during prosecution. This Request includes new 35 U.S.C. § 103 grounds for unpatentability in view of 4 new prior art references (Meaney, Nguyen, Greeff, and Allee).

Because this Request presents new prior art references that have not been previously considered and they raise substantial new questions (“SNQ”) of patentability, *ex parte* reexamination should be granted and each of the challenged claims should be canceled as unpatentable.

II. REQUIREMENTS FOR EX PARTE REEXAMINATION UNDER 37 C.F.R. § 1.510

II.A 37 C.F.R. § l.510(b)(l): Statement pointing out each substantial new question of patentability

A statement pointing out each substantial new question of patentability ("SNQ") based on the cited references in accordance with 37 C.F.R. § l.510(b)(l), is presented below in Section V.

The following SNQs are detailed herein:

SNQ #1: Claims 1, 2, 6-12, 15, 16 of the ’466 Patent are obvious in view of Meaney in view of the knowledge of a POSITA.

SNQ #2: Claims 1, 2, 6-12, 15, 16 of the ’466 Patent are obvious in view of Meaney and Nguyen in view of the knowledge of a POSITA.

SNQ #3: Claims 4, 5, 13, 14, 17-19 of the ’466 Patent are obvious in view of Meaney and Greef in view of the knowledge of a POSITA.

SNQ #4: Claims 4, 5, 13, 14, 17-19 of the ’466 Patent are obvious in view of Meaney, Nguyen, and Greef in view of the knowledge of a POSITA.

SNQ #5A: Claim 3 of the ’466 Patent is obvious in view of Meaney and Allee in view of the knowledge of a POSITA.

SNQ #5B: Claim 3 of the ‘466 Patent is obvious in view of Meaney, Nguyen, and Allee in view of the knowledge of a POSITA.

II.B 37 C.F.R. § l.510(b)(2): Identification of every claim for which reexamination is requested

In accordance with 37 C.F.R. § l.510(b)(2), reexamination is requested for claims 1-19 of the ’466 Patent.

II.C 37 C.F.R. § l.510(b)(2): Detailed explanation of the pertinency and manner of applying the prior art

A detailed explanation of the pertinency and manner of applying the cited prior art to each claim for which reexamination is requested, is provided below in Section V.

II.D 37 C.F.R. § l.510(b)(3): Copy of every patent or printed publication relied upon or referred to

A copy of every patent or printed publication relied upon herein is submitted as Exhibits 1004 through 1007. Each of these cited prior art references constitutes effective prior art as to the claims of the ’466 Patent under pre-AIA 35 U.S.C. § 102.

II.E 37 C.F.R. § l.510(b)(4): Copy of the entire patent for which reexamination is requested

A full copy of the ’466 Patent is submitted herein as Exhibit 1001 and its corresponding file history is submitted as Exhibit 1008.

II.F 37 C.F.R. § l.510(b)(5): Certification that a copy of the request has been served in its entirety on the patent owner

A copy of this request has been served in its entirety on the Patent Owner at the following Patent Center correspondence address of record:

Counsel:

Marc P. Schuyler / Rambus
P.O. Box 2535
Saratoga, CA 95070

Patent Owner:

K.MIZRA LLC
777 Brickell Avenue #500-96031
Miami, FL 33131

II.G 37 C.F.R. § 1.510(b)(6): Certification by the third party requester

NXP certifies that the statutory estoppel provisions of 35 U.S.C. § 315(e)(l) or 35 U.S.C. § 325(e)(l) do not prohibit NXP from filing this ex *parte* reexamination request.

II.H 37 C.F.R. § l.510(a): Fee for requesting reexamination

The fee for this Request, including the fee specified by 37 C.F.R. § l.510(a), is being paid by credit card. The Office is authorized to charge any additional fees associated with this Request to Deposit Account No. 50-2126.

II.I Identification of Related Matters

Requester NXP is a party to a concurrent proceeding brought by K.MIZRA. The '466 Patent has been asserted by K.MIZRA against NXP in an action before the United States District Court in the Western District of Texas entitled K.MIZRA LLC v. NXP USA, Inc., *See K.MIZRA LLC v. NXP USA, INC.*, Civil Action No. 7:25-cv-00304-DC-DTG (W.D. Tex.).

III. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art ("POSITA") at the time of the alleged invention of the '466 Patent would have had a bachelor's degree in electrical engineering, computer engineering, or an equivalent field as well as at least two years of academic or industry experience in design and implementation of high-speed digital communication systems. An individual with an advanced degree in a relevant field, such as computer or electrical engineering, would require less experience in the design and implementation of high-speed digital communication systems, and vice versa. (Ex. 1002, ¶24.)[1]

IV. OVERVIEW OF THE '466 PATENT

The '466 Patent is entitled, "Periodic Calibration for Communication Channels by Drift Tracking" (Ex. 1001, Title) and was filed on November 6, 2014. The '466 Patent relates generally to methods and systems for calibration of a communication channel in a system that includes a receive component with circuitry to receive a digital signal. Ex. 1001, Abstract, Fig. 1, Fig. 3. Figure 3, reproduced below, depicts a transmit component 100 including a transmitter circuit 103 driving a data signal over link 102 to a receive component 101 including a receiver circuit 104. *Id.*, 7:31-42.

[1] Petitioner submits the Declaration of R. Jacob Baker, Ph.D., P.E. (Ex. 1002), an expert in the field of the '466 Patent. (Ex. 1002, ¶¶ 24.)

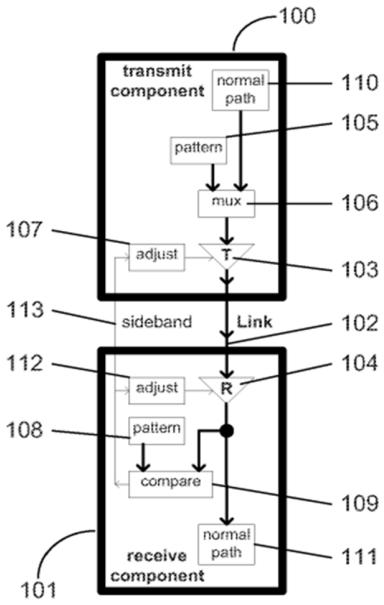


Fig. 3

The calibration methods of the ’466 Patent include a first calibration (e.g., during initialization) and a second calibration (e.g., during operation). Id., Abstract. The ’466 Patent purports to have invented the use of a simplified second calibration to account for drift in timing, voltage or other parameters of a communication channel caused by changes in operation conditions, without repeating a more exhaustive initial calibration. Id., 2:58-3:5.

The ’466 Patent explains that the first calibration identifies an initial value for a parameter of the communication channel, and that the first calibration may be exhaustive so that a suitable operation value can be determined for most conditions in which the system is designed to operate. *Id.*, 3:12-16, 3:33-38, 6:25-38. The ’466 Patent provides examples of the calibrated parameter as “timing parameters specifying the drive times and sample times, voltage levels for drivers and comparators, resistance values such as link termination resistances, driver strength, adaptive equalization coefficients, noise cancellation coefficients, parameters that cause overshoot and undershoot of signals such as driver switching power or speed, and so on.” *Id.*, 6:28-35.

The second calibration of the ’466 Patent updates an existing value of the calibrated parameter to account for drift attributable to changes in operating conditions such as voltage or temperature. Id., 2:31-3:11, 3:38-41. The second calibration of the ’466 Patent is described as being performed periodically and as using less resources of the communication channel than the first calibration. Id., 10:20-33.

The ’466 Patent explains that these calibrations may be performed on the receive component of the communication system, which includes circuitry to receive data communicated across a channel by a transmit component. Id., 7:31-42, 10:59-64. The ’466 Patent explains that performing the second calibration may involve suspending operations of the receive component. Id., 14:3-5.

The ’466 Patent provides an example calibration technique of sending first and second data patterns from a transmit component to the receive component and comparing those data patterns to expected patterns. *Id.*, 9:22-43.

V. THE PRIOR ART

V.A Meaney – U.S. Publication No. 2003/0070123 A1 (Ex. 1004)

Filed on September 21, 2001,
No priority claim,
Issued as U.S. Patent No. 6,922,789 B2 on July 26, 2005

Meaney is entitled, “**Apparatus and Method for Recalibrating a Source-Synchronous Pipelined Self-Time Interface**” (Ex. 1004.) and relates to an apparatus and method for recalibrating a source- synchronous pipelined interface with minimal impact on a running system which allows a computer system to remain operational despite environmental drift or degradation. Ex. 1004, ¶ [0001].

Meaney explains that in symmetric multiprocessing (SMP) systems, managing latencies on cards, wires, or boards that exceed data cycle times is crucial, including source-synchronous pipelined interfaces that capture data within a precise timing window, which requires initial calibration with a known data pattern. Ex. 1004, ¶¶ [0003]-[0004]. Meaney further explains that over time, these interfaces can drift due to environmental changes (e.g., temperature), which can lead to system failures. Ex. 1004, ¶¶ [0005]-[0006].

Meaney states that it solves this problem by providing periodic recalibration with minimal disruption by putting the system into a wait state, performing fast initialization, and resuming operation. Ex. 1004, ¶¶ [0009]-[0012]. The recalibration is a simplified form of the initial calibration, using one less clock centering step and sipping a data deskew step. Ex. 1004, ¶ [0013]. The system assist processor (“SAP”) controls the sequence, first ensuring the interface is idle before calibration by interacting directly with hardware registers and loading calibration patterns. Ex. 1004, ¶¶ [0036]-[0038]. The recalibration logic re-centers the clock efficiently, optimizing the

timing window to adapt to environmental changes. Ex. 1004, ¶ [0040]. Upon completion, the system resumes normal operation, maintaining precise timing and continuous functionality. Ex. 1004, ¶ [0041]

V.B Nguyen – U.S. Publication No. 2003/0151450 A1 (Ex. 1005)

Filed on May 28, 2002,
Is a Continuation-in-part of application 10/076,666, filed on February 14, 2002,
Issued as U.S. Patent No. 6,876,248 B2 on April 5, 2005

Nguyen is entitled, "Signaling Accommodation" (Ex. 1005, title.) and relates to methods for applying offsets to existing values to determine a calibrated value. Ex. 1005, ¶ [0065]. This technique ensures that the reference voltage is accurately set to match the common mode voltage of received signals, thus maintaining signal integrity. *Id.*, [0004], ¶¶ [0059]-[0064].

Nguyen also discloses circuitry including components for receiving a digital signal and calibrating computer system parameters. *Id.*, ¶¶ [0083]-[0086]. A digital calibration component determines high and low compensated voltage failure points and calculates a midpoint value to set the reference voltage, ensuring it matches the common mode voltage of the received signal. *Id.*, ¶¶ [0083]-[0086].

Additionally, Nguyen details a parameters table for storing calibration data for different transmitting units. *Id.*, ¶¶ [0075]-[0078], [0098]-[0100]. This allows the system to dynamically adjust the reference voltage based on the specific characteristics of each unit and environmental conditions. *Id.*, [0100], ¶ [0147]

V.C Greeff –U.S. Patent No. 6,356,106 (Ex. 1006)

Filed on September 12, 2000,
No priority claim or listed priority claim,
Issued on March 12, 2002

Greeff is entitled, "Active Termination in a Multidrop Memory System" (Ex. 1006.) and relates to a system that addresses the issues of signal reflections and integrity in digital systems through an active termination scheme that integrates termination circuits within the devices connected to a multidrop bus rather than on the system's printed circuit board ("PCB"). Ex. 1006, Abstract, 1:5-20. Greeff states that this integration allows for selective enabling or disabling of termination based on the device location and communication traffic, thereby reducing cost and conserving PCB space. Ex. 1006, Abstract, 2:13-34.

A key aspect of Greeff is the calibration of termination resistance and driver strength to optimize signal integrity. Ex. 1006, 4:11-14, 6:3-6, 7:52-8:62. Greeff discloses adjusting the termination resistance during a calibration process that can be either static (performed after system configuration) or dynamic (adjusted during system operation) to account for variations in process, voltage, or temperature. Ex. 1006, 7:52-8:3.

V.D Allee –U.S. Patent No. 6,255,979 (Ex. 1007)

Filed on February 24, 1999,
No priority claim or list priority claim,
Issued on July 3, 2001

Allee is entitled, "CMOS Flash Analog to Digital Converter Compensation" (Ex. 1007,.) and relates to a system including a plurality of comparators, each receiving differential input and reference signals to generate output signals. Ex. 1007, Abstract. A self-calibration circuit within the system adjusts these differential reference signals to mitigate noise from digital switching, ensuring accurate signal processing by compensating for component mismatches and non-linearities. *Id.*, Abstract, 2:13-34. This design enhances the performance of the system in environments with significant digital switching noise. *Id.*

Each comparator in the system undergoes self-calibration to minimize input offset errors, where the reference voltage is adjusted until the comparator switches states accurately. Ex. 1007, 6:17-40. The calibration involves sequentially fine- tuning each comparator, starting from the lowest quantized level, to achieve accurate threshold points for reliable system performance. Ex. 1007, 6:17-40, 7:24-40.

VI. DETAILED EXPLANATION OF UNPATENTABILITY

The arguments presented below are based on 35 U.S.C. § 103 under which a claim is unpatentable if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time of the invention to a person having ordinary skill in the art. *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness, if present. See *Graham*, 383 U.S. at 17–18. When evaluating a claim for obviousness, we also must "determine whether there was an apparent reason to combine the known

elements in the fashion claimed by the patent at issue." *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

The following is a non-exhaustive list of rationales to support a conclusion of obviousness.

(A) Combining prior art elements according to known methods to yield predictable results;

(B) Simple substitution of one known element for another to obtain predictable results;

(C) Use of known technique to improve similar devices (methods, or products) in the same way;

(D) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(E) "Obvious to try" – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(F) Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art; and

(G) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

The cited references (Meaney, Nguyen, Greeff, and Allee) of this Request are in an analogous art to that of the '466 Patent. In particular, the '466 Patent and the cited references are each addressing calibration, and/or recalibration of communication interfaces and/or communication channels accounting for changing conditions that may be attributable to changes in operating conditions and/or drift due environmental changes (e.g., temperature and/or voltage).

Based on the forgoing, it is more than reasonable for a POSITA to look to the above references and combine the known elements of them in the fashion claimed by the patent at issue.

VI.A SNQ #1: Claims 1, 2, 6-12, 15, 16 of the '466 Patent are obvious in view of Meaney in view of the knowledge of a POSITA.

VI.A.1 Claim 1

1. A method of operation in a system that includes a receive component having circuitry to receive a digital signal, the method comprising:

subjecting the receive component to a first calibration during initialization to identify an initial value for a parameter affecting proper reception by the circuitry of the receive component of data communicated across a channel as part of the digital signal;

periodically subjecting the receive component to a second calibration to update an existing value of the parameter for drift attributable to change in at least one of operating voltage or temperature; and

wherein the existing value is dependent on the initial value and wherein the second calibration is constrained to occur during a time period that is shorter than a time period of the first calibration.

Claim 1 is also provided with identifiers for respective claim elements below:

1[pre] A method of operation in a system that includes a receive component having circuitry to receive a digital signal, the method comprising:

1[a] subjecting the receive component to a first calibration during initialization to identify an initial value for a parameter affecting proper reception by the circuitry of the receive component of data communicated across a channel as part of the digital signal;

1[b] periodically subjecting the receive component to a second calibration to update an existing value of the parameter for drift attributable to change in at least one of operating voltage or temperature; and

1[c] wherein the existing value is dependent on the initial value and wherein the second calibration is constrained to occur during a time period that is shorter than a time period of the first calibration.

VI.A.1(A) 1[pre] A method of operation in a system that includes a receive component having circuitry to receive a digital signal, the method comprising:

To the extent the preamble is limiting, *Meaney* discloses a "method of operation in a system that includes a receive component having circuitry to receive a digital signal." *Meaney* discloses "symmetrical computer systems, and particularly to an apparatus and method for recalibrating [a] source-synchronous pipelined interface with minimal impact to a running system." Ex. 1004, Abstract, ¶ [0001]

The computer systems and methods of *Meaney* include a "receiver" and "i logic 14" for capturing (i.e., receiving) transferred data from driver logic 11 through the interface bus 12. *Id.*,

¶¶ [0003]-[0004], [0023], Fig. 1 (annotated below). The receiver and/or receiver calibration logic of *Meaney* are "receive components."

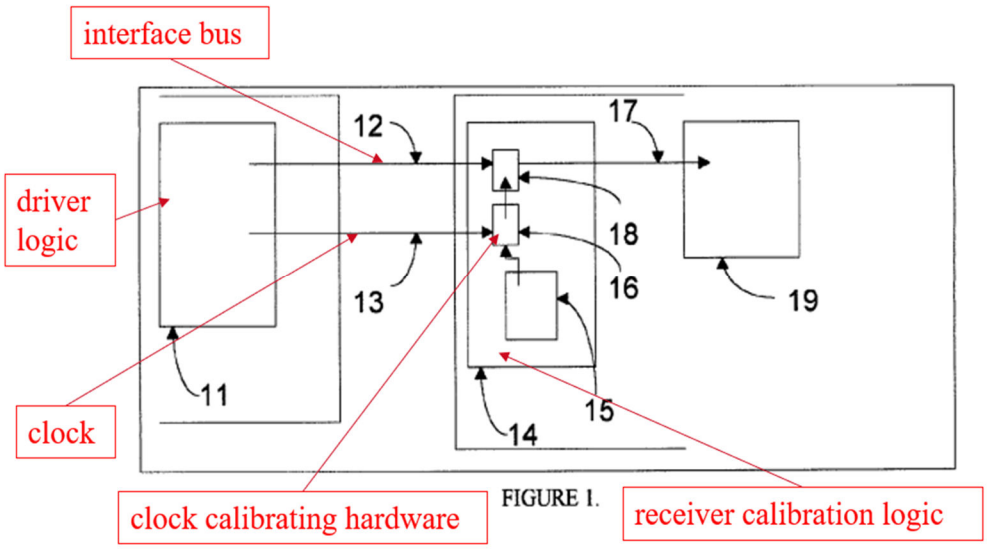


FIGURE 1.

Meaney further discusses the hardware and circuitry of its computer systems and the need to calibrate the receiver to compensate changes to the "circuit." *Id.*, ¶¶ [0007], [0015]-[0016], [0020]-[0021], claim 12. A POSITA would have understood that the receiver of *Meaney* would have circuitry to receive a digital signal. Ex. 1002, Appx, 1-5. Accordingly, a POSITA would have understood that *Meaney*, in view of the knowledge of a POSITA, renders obvious "[a] method of operation in a system that includes a receive component having circuitry to receive a digital signal." *Id.*

VI.A.1(B) 1[a] subjecting the receive component to a first calibration during initialization to identify an initial value

Meaney discloses an initial calibration of the receive component from a stopped position before the interface is in operation. Ex. 1004, ¶¶ [0006], [0021], [0024]1, Fig. 3; Ex. 1002, Appx, 6-8. One of the parameters calibrated to an initial value is clock delay. Ex. 1004, ¶ [0040]; Ex. 1002, Appx, 6-8. Meaney describes the receiver and the "receiver calibration logic" as performing calibration. Ex. 1004, ¶¶ [0004], [0038], Fig. 3. Specifically, Meaney describes the receive calibration logic of the receiver as including "clock calibrating hardware." Id. at ¶ [0023]. Meaney also discloses determining an initial value for clock delay during initialization by disclosing that future re-calibrations will be determined based on the original clock delay. See, e.g., Ex. 1004, ¶¶ [0040] ("clock delays are reset as part of the final clock calibration sequence."); [0051] ("[f]or

instance, if it is known that only the frequency changes, the change in frequency can be calculated by additional hardware and half the difference can be applied as a delay shift"); claim 12 ("recalibration []includes . . . re-ap***plying the clock frequency calculation to the clock delay*** to re-center the clock") (emphasis added).

VI.A.1(C) 1[b] for a parameter affecting proper reception by the circuitry of the receive component of data communicated across a channel as part of the digital signal

Meaney discloses that the calibrated parameter (clock delay) affects proper reception by the circuitry of the receive component of data communicated across a channel as part of the digital signal. Ex. 1004, ¶¶ [0003], [0004], [0040]; Ex. 1002, Appx, 8-9. *Meaney* explains that in transferring data in its computer system, the data must be captured by the receiver within a small temporal window, or "eye." *Id.*; Ex. 1004, ¶ [0003]. *Meaney* further explains that the calibration of the clock delay calibration "is able to ***find the optimum data capture time for the interface***. Since the calibration is done periodically, ***this window gets reoptimized every time*** recalibration occurs." Ex. 1004, [0040] (emphasis added). *Meaney* states that this allows the receiver to recalibrate to new conditions such as changes to cycle time, voltage, or the computing environment. *Id.*

VI.A.1(D) 1[c] periodically subjecting the receive component to a second calibration to update an existing value of the parameter for drift attributable to change in at least one of operating voltage or temperature; and

Meaney discloses periodically subjecting the receive component to a second calibration in the form of a "recalibration." Ex. 1004, ¶¶ [0008] ("The invention allows for the re-calibration of the interface at periodic intervals."); [0009], [0038]. As discussed above, Meaney discloses identifying an initial value for clock delay, which discloses the "existing value of the parameter." Supra Section VI.A.1 (B), SNQ #1. Alternatively, because Meaney discloses several periodic recalibrations, the output value from previous recalibrations would be the existing value for the next recalibration. Ex. 1004, ¶¶ [0008], [0016], [0040].

Meaney discloses that the recalibrations of the clock delay allow the receiver to compensate for "drift over time on the interface to compensate for temperature, voltage, cycle time, and end-of-life degradation." Id., Abstract, ¶¶ [0015], [0016], [0040]; Ex. 1002, Appx, 9-10. Specifically,

Meaney refers to recalibrating the receiver to update the clock delay to account for "cycle time, voltage, or other changes [] made to the environment for testing," and states that the recalibration allows the receiver to recalibrate to the new conditions. Ex. 1004, ¶ [0040]. A POSITA would have understood this as rendering obvious "subjecting the receive component to a second calibration to update an existing value of the parameter for drift attributable to change in at least one of operating voltage or temperature." Ex. 1002, Appx, 9-10.

VI.A.1(E) 1[d] wherein the existing value is dependent on the initial value

Meaney discloses that the existing value of clock delay is dependent on the initial value identified by the first calibration. Ex. 1002, Appx, 10-13. As discussed above, Meaney discloses two alternative values that can be the claimed existing value: the initial value for clock delay or a clock delay value that was determined from previous recalibrations. See Section VI.A.1 (D). (citing Ex. 1004, ¶¶ [0008], [0016], [0040]).

A POSITA would have understood that either alternative of the "existing values" of Meaney are dependent on the initial value. Ex. 1002, Appx, 10-13. In the first instance, the initial value is copied or adopted as the existing value to be used as the starting point for the next calibration. Id.

In the second instance, the output of a previous recalibration depends on the initial value for clock delay because it is necessarily determined, directly, or indirectly, based on one or more recalibrations of the initial value for clock delay. Id. Meaney explains that recalibration reoptimizes the window for data capture by recalibrating the existing clock delay to account for changes in conditions, and discloses that this recalibration occurs without resetting the hardware. Ex. 1004, ¶¶ [0033], [0040], [0051]. A POSITA would have understood that these recalibrations would be performed based on the existing clock delay value. Ex. 1002, Appx, 11. For the first recalibration performed after the initial calibration, the initial value would be used as a starting point in the recalibration to generate a new clock delay, which was generated based on the initial clock delay value. Id. For the next recalibration, the starting point (the claimed "existing value") would be the new clock delay, which was generated from, and thus dependent on, the initial value. Id. For example, Meaney discloses that the clock can be recalibrated by "adding delay" to the clock path or applying a delay shift to the existing clock delay. Ex. 1004, ¶¶ [0040], [0051]; Ex. 1002, Appx, 11.

To the extent Patent Owner argues that Meaney does not disclose the existing value being dependent on the initial value, in light of the disclosure of "adding delay" and "delay shifts" in Meaney, a POSITA would have found it obvious to modify Meaney to use the initial value as the starting point and apply the results of the calibration to that value to determine a calibrated value. Ex. 1002, Appx, 11. Moreover, *Meaney's* disclosure of "adding delay" necessarily requires an initial value to be present—otherwise there would nothing to which to add delay. *Id.*

VI.A.1(F) 1[e] and wherein the second calibration is constrained to occur during a time period that is shorter than a time period of the first calibration.

Meaney discloses that the recalibration is faster and has fewer steps than the initial calibration performed during the original initialization process. Ex. 1004, [0008], [0013], [0038]-[0039]. Specifically, *Meaney* discloses that recalibration is performed using a "fast initialization" process that can occur with minor disruption to the computer system by skipping certain steps (e.g., a data deskew and a clock centering step) that are performed during the original initialization process. Ex. 1004, ¶¶ [0008], [0013], [0038], Fig. 3. Moreover, the initial calibration of *Meaney* is performed from a stopped position, whereas the recalibration merely requires putting the system in a "wait" state for the duration of the recalibration. Ex. 1004, ¶¶ [0024], [0035], [0039], [0041]. Accordingly, a POSITA would have understood that the recalibration of *Meaney* would occur during a time period that is shorter than the time period of *Meaney's* initial calibration. Ex. 1002, Appx, 13-14. Thus, a POSITA would have understood that *Meaney* discloses "the second calibration is constrained to occur during a time period that is shorter than a time period of the first calibration."

VI.A.2 Claim 2

2. The method of claim 1, wherein periodically subjecting includes calculating an interval and repeatedly (a) performing the second calibration at each expiration of the interval and (b) resetting the interval.

Prior art discloses *Meaney* discloses performing recalibration in "periodic intervals" and states that the recalibration method can be "triggered periodically." Ex. 1004, ¶¶ [0008], [0015], claim 5. Accordingly, a POSITA would have understood the disclosure of *Meaney* to disclose "calculating an interval and repeatedly (a) performing the second calibration at each expiration of the interval and (b) resetting the interval." Ex. 1002, Appx, 14-15. To be triggered in periodic

intervals, *Meaney* necessarily must involve calculating the interval, repeating the recalibration when the interval is expired, and resetting the interval between recalibrations. *Id.*

To the extent Patent Owner argues this limitation is not taught by *Meaney*, it would have been obvious to a POSITA to modify *Meaney* to have the interval be calculated and repeatedly reset between recalibrations. Ex. 1002, Appx, 15. *Meaney* discloses that periodic recalibration allows the system to ensure that changes to the circuitry or environmental characteristics do not adversely affect performance over time. Ex. 1004, ¶ [0016]. To achieve this objective, it would have been obvious to a POSITA to calculate an interval based on, for example, an expected time it would take an environmental characteristic (e.g., change in temperature) to affect performance, and then repeatedly recalibrate the system based on that calculated interval. Ex. 1002, Appx, 15. Periodic recalibration based on intervals using timers were well known at the time of the '466 Patent. Ex. 1002, Appx, 15; Ex. 1010, ¶ [0042].

VI.A.3 Claim 6

6. The method of claim 1, wherein the second calibration uses less resources of the channel than the first calibration.

As discussed above in Section VI.A.3, SNQ #1, *Meaney* discloses that a second calibration (*Meaney's* recalibration) is faster and has fewer steps than a first calibration, i.e., the initial calibration performed during the original initialization process. Ex. 1004, ¶¶ [0008], [0013], [0038]-[0039]. Specifically, *Meaney* discloses that recalibration is performed using a "fast initialization" process that can occur with minor disruption to the computer system by skipping certain steps (e.g., a data deskew and a clock centering step) that are performed during the original initialization process. Ex. 1004, ¶¶ [0008], [0013], [0038], Fig. 3.

Because the recalibration of *Meaney* is faster than the initial calibration, it occupies the data channel for less time. Ex. 1002, Appx, 16. Thus, a POSITA would have understood that *Meaney* discloses "second calibration uses less resources of the channel than the first calibration." *Id*.

VI.A.4 Claim 7

7. The method of claim 1, wherein subjecting the receive component to the first calibration comprises receiving a first set of operations at the circuitry to exhaustively determine the initial value of the parameter, and wherein periodically subjecting the receive

component to the second calibration comprises receiving a second set of operations at the circuitry to update the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value.

Claim 7 is also provided with identifiers for respective claim elements below:

7[a] The method of claim 1, wherein subjecting the receive component to the first calibration comprises receiving a first set of operations at the circuitry to exhaustively determine the initial value of the parameter, and

7[b] wherein periodically subjecting the receive component to the second calibration comprises receiving a second set of operations at the circuitry to update the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value.

VI.A.4(A) 7[a] The method of claim 1, wherein subjecting the receive component to the first calibration comprises receiving a first set of operations at the circuitry to exhaustively determine the initial value of the parameter, and

As discussed above in Section VI.A.1 (B), *Meaney* discloses subjecting the circuitry of the receive component to the first calibration by calibrating clock delay during initialization of the computer system. *Meaney* explains that the initial calibration is an exhaustive calibration, which involves sending a known data pattern across a data transfer interface to receive circuitry. Ex. 1004, ¶¶ [0004], [0024]-[0033], Fig. 3. This triggers the receiver circuitry to use exhaustive calibration techniques to determine an initial clock delay value that "compensates for the various package tolerances." *Id.* *Meaney* explains that a system assist processor (SAP) controls the calibration sequence and signals the receiver calibration logic to perform calibration. *Id.* at [0038]. Thus, the receiver of *Meaney* receiving the known data pattern and/or receiving signals from the SAP discloses "receiving a first set of operations at the circuitry." *Meaney* explains that this calibration technique requires stopping the system and involves two separate clock calibrations and deskewing the data. *Id.* Accordingly, a POSITA would have understood that *Meaney* discloses "subjecting the receive component to the first calibration comprises receiving a first set of operations at the circuitry to exhaustively determine the initial value of the parameter." Ex. 1002, Appx, 17-19.

VI.A.4(B) 7[b] wherein periodically subjecting the receive component to the second calibration comprises receiving a second set of operations at the circuitry to

update the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value.

As discussed above with respect to 1[d], *Meaney* discloses subjecting the receive component to a second calibration (*Meaney's* recalibration) to update an existing value of the parameter (clock delay) for drift. *Meaney* further discloses the receive component circuitry receiving a set of operations to perform the recalibration if a desired clock delay value has drifted from the existing value by more than a delta value. Ex. 1004, Abstract, ¶¶ [0001], [0005]. As explained above in 7[a], *Meaney* discloses a system assist processor (SAP) controlling the recalibration sequence and signaling the receiver calibration logic to perform recalibration. *Id.* at ¶ [0038]. Thus, the receiver receiving the known data pattern and/or receiving signals from the SAP discloses " receiving a second set of operations at the circuitry to update the existing value."

Meaney discloses that recalibration may be performed in response to a trigger event that suggests that the clock delay has drifted and the data capture time window has changed and is no longer accurate. Ex. 1004, ¶ [0017]. *Meaney* explains that this trigger event can be indicated when, for example, error correction (ECC) is performed on the data and a correctable error is found. *Id.* Errors in data caused by clock delay drift would indicate that the clock delay has drifted by more than a delta value, i.e., by more than the amount that the system could tolerate without introducing errors into the data. Ex. 1002, Appx, 20-21. Accordingly, a POSITA would have understood that *Meaney*, in view of the knowledge of a POSITA, renders obvious "wherein periodically subjecting the receive component to the second calibration comprises receiving a second set of operations at the circuitry to update the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value." *Id.*

To the extent Patent Owner argues that *Meaney* does not disclose recalibrating "a desired value of the parameter has drifted from the existing value by more than a delta value," it would have been obvious to a POSITA to modify *Meaney* to include this feature. *Id. Meaney* emphasizes the need to recalibrate clock delay to maintain accurate data capture despite drift to circuitry changes or changes in environmental conditions, and discloses recalibrating in response to a trigger event. Ex. 1004, Abstract, ¶¶ [0004]-[0005]. It would have been obvious to a POSITA to trigger recalibration in response to clock delay, or other parameters indicative of clock delay, drifting from an existing value by an amount beyond the tolerance of the computer system (the claimed "delta value"). Ex. 1002, Appx, 20-21.

VI.A.5 Claim 8

8. The method of claim 1, wherein periodically subjecting the receive component to the second calibration comprises suspending transmit and receive operations of the circuitry of the receive component.

As discussed above with respect to 1[c], *Meaney* discloses periodically recalibrating the receiver. *Meaney* further discloses that the first step of the recalibration process is putting the computer system or data transfer interface into a "wait state" to keep it from being used for anything other than recalibration. Ex. 1004, ¶¶ [0009]-[0015], [0041]-[0042], Fig. 3, claim 7. Additionally, *Meaney* discloses setting interface fences to block the interface from being used by any system operations other than recalibration. *Id.*, Abstract, ¶¶ [0037], [0044]. In this way, the system of *Meaney* suspends transit and receive operations of the receiver circuitry as part of the recalibration process. Ex. 1002, Appx, 22-24. Accordingly, *Meaney* discloses "wherein periodically subjecting the receive component to the second calibration comprises suspending transmit and receive operations of the circuitry of the receive component." *Id.*

VI.A.6 Claim 9

9. The method of claim 8, wherein subjecting the receive component to the first calibration comprises receiving at the circuitry a first pattern transmitted by a transmit component and comparing, in the receive component, the first pattern with a first expected pattern, and wherein periodically subjecting the receive component to the second calibration comprises receiving at the circuitry a second pattern transmitted by the transmit component and comparing in the receive component the second pattern with a second expected pattern.

Claim 9 is also provided with identifiers for respective claim elements below:

9[a] The method of claim 8, wherein subjecting the receive component to the first calibration comprises receiving at the circuitry a first pattern transmitted by a transmit component and comparing, in the receive component, the first pattern with a first expected pattern, and

9[b] wherein periodically subjecting the receive component to the second calibration comprises receiving at the circuitry a second pattern transmitted by the transmit component and comparing in the receive component the second pattern with a second expected pattern.

VI.A.6(A) 9[a] The method of claim 8, wherein subjecting the receive component to the first calibration comprises receiving at the circuitry a first pattern

transmitted by a transmit component and comparing, in the receive component, the first pattern with a first expected pattern, and

As discussed above with respect to 1[c], *Meaney* discloses a first calibration of the system clock during initialization to determine a clock delay. *Meaney* further discloses performing the initial calibration by sending a "known data pattern" across the interface to the receiver circuitry, which is used to calibrate the clock using calibration techniques. Ex. 1004, ¶¶ [0004], [0027]-[0031], Fig. 2. A POSITA would have understood that this discloses performing calibration by comparing, in the receive component, the received data pattern with the known data pattern to determine if they match, and if not, adjusting the clock delay. Ex. 1002, Appx, 25- 26.

VI.A.6(B) 9[b] wherein periodically subjecting the receive component to the second calibration comprises receiving at the circuitry a second pattern transmitted by the transmit component and comparing in the receive component the second pattern with a second expected pattern.

As discussed above with respect to 1[c], *Meaney* discloses periodically recalibrating the receiver. As discussed above with respect to 9[a], *Meaney* discloses initially calibrating a clock by transmitting a known data pattern and comparing the data pattern received by the receiver component with the known data pattern. Ex. 1004, ¶¶ [0004], [0027]-[0031], Fig. 3; Ex. 1002, Appx, 27-28. *Meaney* further discloses that the same "known data pattern" techniques are used for recalibration (the claimed "second calibration"). Ex. 1004, ¶¶ [0037]-[0038], [0042]-[0048]. *Meaney* explains that recalibration includes turning on a known "driver calibration pattern" (e.g., a repeating bit pattern), which is used to re-calibrate the clock. *Id.*; Ex. 1002, Appx, 27-28. A POSITA would have understood that the re- calibration would be performed by comparing, in the receiver and receiver calibration logic, the received data pattern with the known data pattern to determine if they match, and if not, to re-calibrate the clock. Ex. 1002, Appx, 27-28.

VI.A.7 Claim 10

10. A system, comprising:

a receive component, the receive component having circuitry to receive data communicated across a channel by a transmit component;

the receive component to

perform at system initialization a first calibration, the first calibration to identify an initial value for a parameter affecting proper reception by the circuitry of the data communicated across the channel, and

perform on a periodic basis a second calibration, the second calibration to update an existing value of the parameter for drift attributable to change in at least one of voltage or temperature, wherein a time duration of the second calibration is constrained to be shorter than a time duration of the first calibration; and

circuitry to store the existing value of the parameter, the existing value of the parameter dependent on the initial value and any updates from the second calibration.

Claim 10 is also provided with identifiers for respective claim elements below:

10[pre] A system, comprising:

10[a] a receive component, the receive component having circuitry to receive data communicated across a channel by a transmit component;

10[b] the receive component to

10[c] perform at system initialization a first calibration, the first calibration to identify an initial value for a parameter affecting proper reception by the circuitry of the data communicated across the channel, and

10[d] perform on a periodic basis a second calibration, the second calibration to update an existing value of the parameter for drift attributable to change in at least one of voltage or temperature, wherein a time duration of the second calibration is constrained to be shorter than a time duration of the first calibration; and

10[e] circuitry to store the existing value of the parameter,

10[f] the existing value of the parameter dependent on the initial value and any updates from the second calibration.

VI.A.7(A) 10 [pre] A system, comprising:

To the extent the preamble is limiting, *Meaney* discloses "[a]n SMP computer system has an apparatus and method for recalibrating a self-timed, source- synchronous, pipelined interface while the computer system is running." Ex. 1004, Abstract, ¶ [0001]; Ex. 1002, Appx, 28.

VI.A.7(B) 10[a] a receive component, the receive component having circuitry to receive data communicated across a channel by a transmit component;

As discussed above regarding claim 1[pre], *Meaney* discloses computer systems that include a receive component having circuitry to receive data. Ex. 1004, ¶¶ [0003]-[0004], [0007], [0015]-[0016], [0020]-[0021], [0023]. *Meaney* further discloses data communicated across a channel by a transmit component. Ex. 1002, Appx, 29-33. Specifically, the computer systems of *Meaney* include the transfer of data across a source-synchronous pipelined interface, which a POSITA would have understood is a data channel. Ex. 1004, ¶ [0003]; Ex. 1002, Appx, 29-33. *Meaney* explains that data is communicated "across the interface." Ex. 1004, ¶ [0004]. Accordingly, a POSITA would have understood *Meaney* to disclose "a transmit component." Ex. 1002, Appx, 29-33.

VI.A.7 C) 10[b] the receive component to perform at system initialization a first calibration, the first calibration to identify an initial value for a parameter affecting proper reception by the circuitry of the data communicated across the channel, and

As discussed above regarding 1[a] and 1[b], *Meaney* discloses subjecting the receive component to a first calibration during initialization to identify an initial value for a parameter affecting proper reception by the circuitry of the receive component of data communicated across a channel as part of the digital signal. *Supra* Sections VI.A.1 (B) and (C), SNQ #1. For the same reasons, *Meaney* discloses "the receive component to perform at system initialization a first calibration, the first calibration to identify an initial value for a parameter affecting proper reception by the circuitry of the data communicated across the channel." Ex. 1002, Appx, 34-35.

VI.A.7(D) 10[c] perform on a periodic basis a second calibration, the second calibration to update an existing value of the parameter for drift attributable to change in at least one of voltage or temperature,

As discussed above regarding 1[c], *Meaney* discloses periodically subjecting the receive component to a second calibration to update an existing value of the parameter for drift attributable to change in at least one of operating voltage or temperature. *Supra* Section VI.A.1 (D). For the same reasons, *Meaney*, in view of the knowledge of a POSITA, renders obvious "perform on a periodic basis a second calibration, the second calibration to update an existing

value of the parameter for drift attributable to change in at least one of voltage or temperature." Ex. 1002, Appx, 36.

VI.A.7(E) 10[d] wherein a time duration of the second calibration is constrained to be shorter than a time duration of the first calibration; and

As discussed above regarding 1[e], *Meaney* discloses wherein the second calibration is constrained to occur during a time period that is shorter than a time period of the first calibration. *Supra* Section VI.A.1 (F), SNQ #1. For the same reasons, *Meaney*, in view of the knowledge of a POSITA, renders obvious "wherein a time duration of the second calibration is constrained to be shorter than a time duration of the first calibration." Ex. 1002, Appx, 37.

VI.A.7(F) 10[e] circuitry to store the existing value of the parameter,

Meaney discloses that the computer system includes clock calibrating hardware. Ex. 1004, ¶¶ [0015]-[0016], [0020]-[0021], [0023]. *Meaney* further discloses a system assist processor (SAP) that uses a hardware interface protocol to read and write registers in the logic of the interface. Ex. 1004, ¶ [0037]. A POSITA would have understood that the clock calibrating hardware would include circuitry and would at least temporarily store the existing value of the clock delay in order to perform the recalibration. Ex. 1002, Appx, 38. Additionally, a POSITA would have understood that the SAP would write the clock delay into a register in the interface logic. *Id.* Accordingly, *Meaney*, in view of the knowledge of a POSITA, renders obvious "circuitry to store the existing value of the parameter." *Id.*

Additionally, to the extent Patent Owner argues that *Meaney* does not disclose circuity to store the existing clock delay parameter, it would have been obvious to a POSITA to modify *Meaney* to do so. Ex. 1002, Appx, 38. *Meaney* has clock calibration hardware and discloses performing periodic recalibration of clock delay in a manner that depends on the existing clock delay. *Id.*; Ex. 1004, ¶¶ [0033], [0040], [0051]. A POSITA would have been motivated to store the existing clock delay locally in the computer system so that the existing clock delay would be readily accessible in performing the next clock recalibration. Ex. 1002, Appx, 38.

VI.A.7(G) 10[f] the existing value of the parameter dependent on the initial value and any updates from the second calibration.

As discussed above regarding 1[d], *Meaney* discloses the existing value of clock delay is dependent on the initial clock delay value. *Supra* Section VI.A.1 (E). For the same reasons,

Meaney, in view of the knowledge of a POSITA, renders obvious "the existing value of the parameter dependent on the initial value." Ex. 1002, Appx, 39. And, as discussed above in 1[c], *Meaney* discloses updating the clock delay based on the recalibration.

VI.A.8 Claim 11

11. The system of claim 10, wherein the second calibration is to be performed at expiration of an interval of time, at which time the circuitry is to suspend receive operations.

For the same reasons discussed above for claim 2, *Meaney*, in view of the knowledge of a POSITA, renders obvious "the second calibration is to be performed at expiration of an interval of time." *Supra* Section VI.A.2; Ex. 1002, Appx, 41- 43.

And for the same reasons discussed above for claim 8, *Meaney*, in view of the knowledge of a POSITA, renders obvious performing the second calibration at expiration of an interval of time, "at which time the circuitry is to suspend receive operations." *Supra* Section VI.A.5.

VI.A.9 Claim 12

12. The system of claim 11, wherein passage of the interval of time is to be tracked by the transmit component and the second calibration is to be initiated by the transmit component.

As discussed above for 10[a], *Meaney* discloses a transmit component. *Supra* Section VI.A.7 (B). *Meaney* discloses performing recalibration in "periodic intervals" and states that the recalibration method can be "triggered periodically." Ex. 1004, ¶ [0008], *Meaney* further discloses that the passage of the interval of time is tracked by the transmit component and the recalibration is initiated by the transmit component periodically. Specifically, the recalibration of *Meaney* is initiated by a driver side calibration flag signaling hardware to drive a repeating pattern across the interface to the receiver. Ex. 1004, ¶ [0037]. Accordingly, a POSITA would have understood that *Meaney* discloses the hardware of the transmit component tracking the periodic intervals and the second calibration being initiated by the transmit component. Ex. 1002, Appx, 44.

Additionally, to the extent Patent Owner argues that *Meaney* does not disclose the transmit component tracking the passage of the interval of time, it would have been obvious to a POSITA to modify *Meaney* to do so. *Id*. *Meaney* discloses that periodic recalibration allows the system to ensure that changes to the circuitry or environmental characteristics do not adversely affect performance over time, and discloses that the transmit component (the driver side hardware)

initiates the recalibration. Ex. 1004, ¶¶ [0016], [0037]. A POSITA would have been motivated to have the transmit component track the periodic time intervals so it could initiate the recalibration directly without needing further instructions or signals (e.g., from the receiving component or other hardware). Ex. 1002, Appx, 44.

VI.A.10 Claim 15

15. The system of claim 10, wherein the receive component is to perform, responsive to the second calibration, one of an increment operation or a decrement operation upon the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value.

As discussed above with respect to 1[d], *Meaney* discloses subjecting the receive component to a second calibration (*Meaney's* recalibration) to update an existing value of the parameter (clock delay) for drift. *Meaney* further discloses that the receive component performs, responsive to the second calibration, one of an increment operation or a decrement operation upon the existing clock delay if a desired value of the clock delay has drifted from the existing clock delay by more than a delta value. Ex. 1002, Appx, 46-47. *Meaney* discloses that recalibration may be performed, by the receiver and receiver calibration logic, in response to a trigger event that suggests that the clock delay has drifted and the data capture time window has changed and is no longer accurate. Ex. 1004, ¶ [0017]. *Meaney* explains that this trigger event can be indicated when, for example, error correction (ECC) is performed on the data and a correctable error is found. *Id.* Errors in data caused by clock delay drift would indicate that the clock delay has drifted by more than a delta value, i.e., by more than the amount that the system could tolerate without introducing errors into the data. Ex. 1002, Appx, 46-47. In response, *Meaney* discloses that the clock delay may be adjusted by a "delay shift" (i.e., an increment or decrement operation) calculated based on a recalibration and then applied to the existing clock delay value. Ex. 1004, ¶ [0051]; Ex. 1002, Appx, 46-47. Accordingly, a POSITA would have understood that *Meaney*, in view of the knowledge of a POSITA, renders obvious "the receive component is to perform, responsive to the second calibration, one of an increment operation or a decrement operation upon the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value." Ex. 1002, Appx, 46-49.

To the extent Patent Owner argues that *Meaney* does not disclose "perform[ing], responsive to the second calibration, one of an increment operation or a decrement operation upon the existing

value if a desired value of the parameter has drifted from the existing value by more than a delta value," this would have been obvious to a POSITA. Ex. 1002, Appx, 47. *Meaney* emphasizes the need to recalibrate clock delay to maintain accurate data capture despite drift to circuitry changes or changes in environmental conditions, and discloses recalibrating in response to a trigger event. Ex. 1004, Abstract, ¶¶ [0004]-[0005]. *Meaney* also discloses changing the clock delay by performing a recalibration and then applying a "delay shift" to the existing clock delay based on the results of the recalibration. *Id.* at ¶ [0051]. It would have been obvious to a POSITA, in response to a recalibration, to perform an increment operation or a decrement operation on the existing clock delay value, to shift the value of the clock delay based on the results of the recalibration (e.g., based on the amount the received data pattern differs from the known data pattern). Ex. 1002, Appx, 46-49; Ex. 1004, ¶¶ [0004], [0037]-[0038], [0042]-[0048].

For example, a POSITA would be motivated to do so at least in view of *Meaney* disclosure of recalibrating clock delay to account for drift due to changes in circuitry or environmental conditions, as well as *Meaney's* use of a "delay shift" to change the clock delay. Ex. 1002, Appx, 46-49.

VI.A.11 Claim 16

16. The system of claim 10, further comprising circuitry to store a first expected pattern and a second expected pattern, and circuitry to compare the first expected pattern with a pattern received from the transmit component in association with the first calibration, and to compare the second expected pattern with a pattern received from the transmit component in association with the second calibration.

Claim 16 is also provided with identifiers for respective claim elements below:

16[a] The system of claim 10, further comprising circuitry to store a first expected pattern and a second expected pattern, and

16[b] circuitry to compare the first expected pattern with a pattern received from the transmit component in association with the first calibration, and to compare the second expected pattern with a pattern received from the transmit component in association with the second calibration.

VI.A.11(A) 16[a] The system of claim 10, further comprising circuitry to store a first expected pattern and a second expected pattern, and

As discussed above with respect to claim elements 9[a] and 9[b], *Meaney* discloses that both the initial calibration and the recalibration may be performed by comparing, in the receive circuitry, the received data pattern with the known data pattern to determine if they match, and if not, adjusting the clock delay. *Supra* Section VI.A.6. In order to carry out that comparison, the receiver circuity must, at least temporarily, store the respective known data patterns needed for each calibration or recalibration, and thus those data patterns must be stored in circuitry of the computer system. Ex. 1002, Appx, 49-51. Additionally, because claim 16[a] does not specify where the circuitry must be, storage of those known data patterns anywhere in the circuitry of *Meaney's* computer system is sufficient to meet this element. *Id.*

VI.A.11(B) 16[b] circuitry to compare the first expected pattern with a pattern received from the transmit component in association with the first calibration, and to compare the second expected pattern with a pattern received from the transmit component in association with the second calibration.

As discussed above with respect to claim elements 9[a] and 9[b], *Meaney* discloses that both the initial calibration and the recalibration may be performed by comparing, in the receive circuitry, the received data pattern with the known data pattern to determine if they match, and if not, adjusting the clock delay. *Supra* Section VI.A.6. For the same reasons, *Meaney*, in view of the knowledge of a POSITA, renders obvious "circuitry to compare the first expected pattern with a pattern received from the transmit component in association with the first calibration, and to compare the second expected pattern with a pattern received from the transmit component in association with the second calibration." Ex. 1002, Appx, 52-53.

VI.B SNQ #2: Claims 1, 2, 6-12, 15, 16 of the '466 Patent are obvious in view of Meaney and Nguyen in view of the knowledge of a POSITA.

The combination of *Meaney* and *Nguyen*, either alone or in combination, discloses and/or suggests all limitations of claims 1, 2, 6-12, 15, and 16, and thus renders those claims obvious. Ex. 1002, Appx, 54-81. Specifically, *Meaney* in combination with *Nguyen* discloses applying offsets to existing values to determine a calibrated value, and circuitry for receiving a digital signal, calibrating computer system parameters, and storing calibration data. *See, e.g.,* Ex. 1002, Appx,

54, 61- 63, 75-77. All other elements of claims 1, 2, 6-12, 15, and 16 are disclosed or rendered obvious by *Meaney* as explained in SNQ #1.

VI.B.1 One of skill in the art would have been motivated to combine *Meaney* with *Nguyen.*

Meaney discloses a system for calibrating communication system parameters. Ex. 1004, Abstract, ¶¶ [0008]-[0017], [0039]-[0040]. Similarly, *Nguyen* discloses techniques for applying offsets to existing values to determine calibrated values for a digital system, as well as specific circuitry for signal reception and parameter calibration. Ex. 1005, ¶¶ [0065], [0083-0085], [0099]. Accordingly, *Meaney* and *Nguyen* both relate to electronic systems and methods for calibration and adjustment of communication system parameters. Ex. 1002, Appx, 54.

Nguyen discloses applying offsets to existing values to derive calibrated values to ensure precise adjustments in system parameters. Ex. 1005, ¶ [0099]; Ex. 1002, Appx, 54. Combining this method with the system of *Meaney* would enhance the accuracy of *Meaney's* calibration process, improving overall system performance. Ex. 1002, Appx, 54. Thus, a POSITA would have been motivated to make this combination to enhance calibration accuracy. *Id.*

Due to similarities between the calibration techniques of *Meaney* and *Nguyen*, a POSITA would have had a reasonable expectation of success in making this modification. *Id*. For example, *Meaney* describes a concept similar to *Nguyen's* offsets: "adding delay" to the parameters or applying a shift to the existing parameters. Ex. 1004, ¶¶ [0040], [0051]; Ex. 1002, Appx, 54. Alternatively, a POSITA would have understood that the calibration systems of *Meaney* would be enhanced with the offsets of *Nguyen* because this improvement represents the use of a known technique to predictably improve a similar system in the same way. Ex. 1002, Appx, 54; *see KSR Int'l Co. v. Teleflex, Inc.,* 127 S.Ct. 1727, 1740 (2007).

A POSITA would have also been motivated to integrate the circuitry of *Nguyen* into the system of *Meaney* to improve efficiency of the calibration. Ex. 1002, Appx, 54. *Nguyen* discloses a streamlined approach to system calibration with particular circuitry. Ex. 1005, ¶¶ [0065], [0083-0085], [0099]; Ex. 1002, Appx, 54. Because *Meaney* does not specify the particular circuitry that is employed, incorporating the circuitry of *Nguyen* into the system of *Meaney* would have been choosing from a finite number of identified, predictable solutions, and a simple substitution of one known element for another to yield predictable results. *Id.*, Appx, 54; *see KSR Int'l,* 127 S.Ct. at 1740 (2007).

A POSITA would have had a reasonable expectation of success in combining *Meaney* and *Nguyen*. Ex. 1002, Appx, 54. Both address common challenges in the field of electronic system calibration and optimization. Ex. 1004, Abstract, ¶¶ [0008]-[0017], [0039]-[0040]; Ex. 1005, ¶¶ [0065], [0083-0085], [0099]; Ex. 1002, Appx, 54.

The integration of *Nguyen's* calibration techniques and circuitry into *Meaney's* system would have been straightforward and cost-effective. Ex. 1002, Appx, 54. The required modifications would have been minimal, and the results of the combination would have been predictable, given the complementary nature of the technologies. Ex. 1005, 7:10-25; Ex. 1002, Appx, 54.

VI.B.2 Claim 1

1. A method of operation in a system that includes a receive component having circuitry to receive a digital signal, the method comprising:

subjecting the receive component to a first calibration during initialization to identify an initial value for a parameter affecting proper reception by the circuitry of the receive component of data communicated across a channel as part of the digital signal;

periodically subjecting the receive component to a second calibration to update an existing value of the parameter for drift attributable to change in at least one of operating voltage or temperature; and

wherein the existing value is dependent on the initial value and wherein the second calibration is constrained to occur during a time period that is shorter than a time period of the first calibration.

VI.B.2(A) 1[pre] A method of operation in a system that includes a receive component having circuitry to receive a digital signal, the method comprising:

As discussed in SNQ #1, *Meaney* discloses a method of operation in a system that includes a receive component having a receiver and a receiver calibration logic for capturing a digital signal. Ex. 1004, ¶¶ [0003]-[0004], [0023]; *supra* Section VI.A.1 (A). *Nguyen* also discloses a receive component having circuitry to receive a digital signal. Ex. 1002, Appx, 55-60. For example, *Nguyen* discloses a receiving unit 115 that receives a signal 110 from the transmitting unit 110. Ex. 1005, ¶ [0030] Fig. 1 (annotated below).

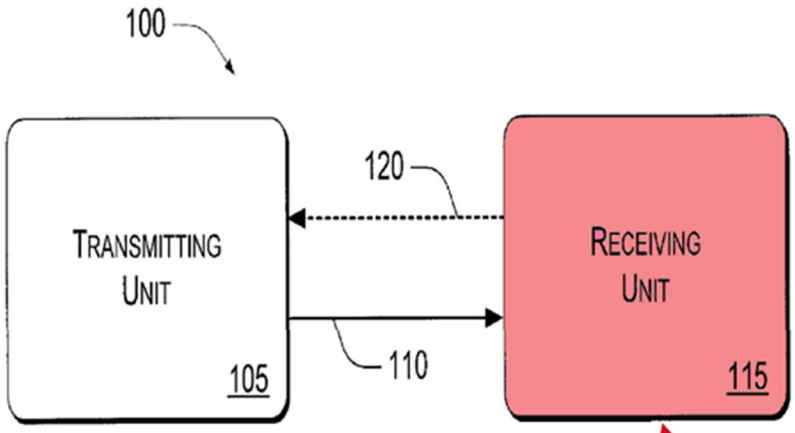


FIG. 1

receive component

Nguyen discloses, for example, that the receiving unit may be part of an integrated circuit or printed circuit board, and discloses that the transmitted signal 110 may be a digital signal. Ex. 1005, ¶¶ [0031], [0032], [0047]; Ex. 1002, Appx, 56. *Nguyen* also gives examples of specific circuitry that could be implemented in the receiving unit. Ex. 1005, Fig. 4A (annotated):

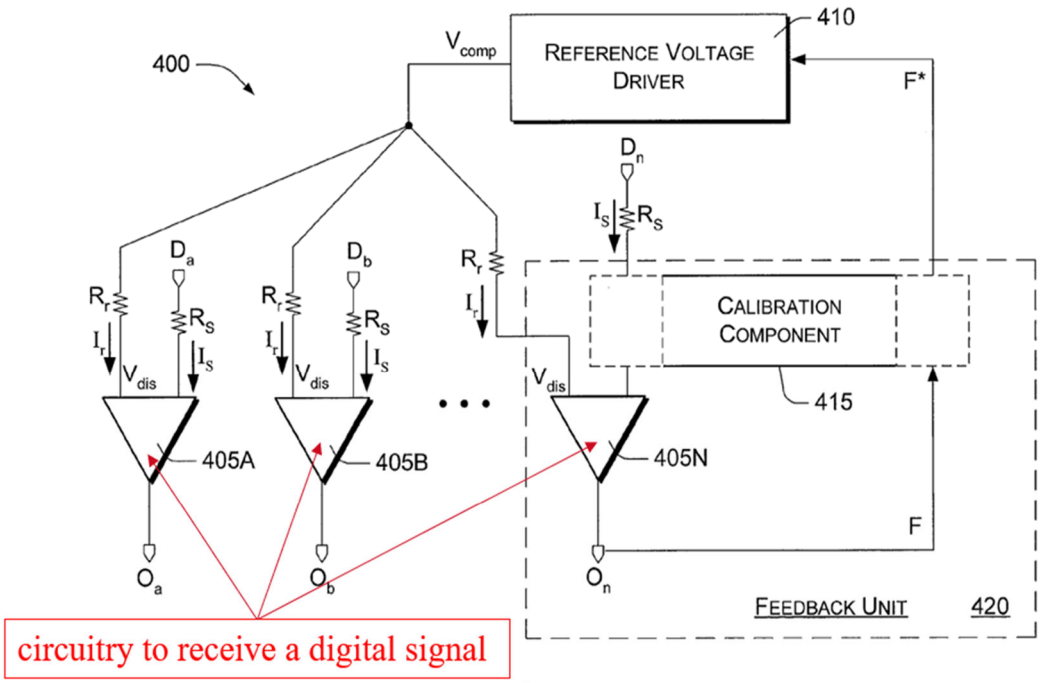


FIG. 4A

As discussed in Section VI.B.1, it would have been obvious to a POSITA to enhance the computer system interface of *Meaney* with the receiver circuitry and digital signals of *Nguyen*. Ex. 1002, Appx, 56. Because *Meaney* does not specify the particular receiver circuitry that is employed in receiving the transmitted data, it would have been obvious to a POSITA to modify *Meaney* to include the digital signal receiving unit of *Nguyen* to receive the digital signal of *Meaney*. Ex. 1002, Appx, 56-57.

VI.B.2(B) 1[d] wherein the existing value is dependent on the initial value

As discussed in SNQ #1, *Meaney* discloses that an existing value for clock delay is dependent on an initial clock delay determined during initialization, either directly or indirectly. Ex. 1004, ¶¶ [0008], [0016], [0040]; *supra* Section VI.A.1 (E). *Nguyen* discloses adjusting a parameter of a digital signal receiver (compensated voltage) by applying an offset to a previously calibrated value. Ex. 1002, Appx, 61-63; Ex. 1005, ¶ [0099] ("This calibrated value may be read from the register 710 and an offset value may be added. The resultant summed value may then be programmed back into the register 710 and used during normal operation of the device"). Specifically, *Nguyen* discloses determining a calibrated value, then adding or subtracting an offset value. Ex. 1002, Appx, 61-63; Ex. 1005, ¶ [0099]. The offset value may be determined at design time or determined dynamically as part of an initialization or calibration procedure. Ex. 1002, Appx, 61-63; Ex. 1005, ¶ [0099].

As discussed in Section VI.B.1, it would have been obvious to a POSITA to enhance the calibration techniques of *Meaney* with the offset values of *Nguyen*. Ex. 1002, Appx, 54. *Meaney* discloses recalibration techniques that include applying a delay shift to the existing clock delay. Ex. 1004, ¶¶ [0040], [0051]. A POSITA would have understood this as a similar concept to the offsets of *Nguyen*. Ex. 1002, Appx, 61-62. In light of these similar disclosures, it would have been obvious to a POSITA to apply the offset values of *Nguyen* to the clock delay calibration of *Meaney.* Ex. 1002, Appx, 62. For example, a POSITA could implement a predetermined offset to the clock delay of *Meaney* to compensate for an environmental difference (e.g., temperature) between the calibration environment and operational environment of the computer system interface. *Id*.

VI.B.3 Claims 2, 6, 8, 9, 11, and 12

As discussed above in SNQ #1, each and every element of claims 2, 6, 8, 9, 11, and 12 are taught by *Meaney*. *Supra* Sections VI.A.2-3, 5-6, & 8-9. The combination of *Meaney* and *Nguyen*,

as described above, does not affect the disclosure of *Meaney* that render those claims obvious. Accordingly, the combination of *Meaney* and *Nguyen* render claims 2, 6, 8, 9, 11, and 12 obvious for the same reasons as discussed in SNQ #1.

VI.B.4 Claim 7

7. The method of claim 1, wherein subjecting the receive component to the first calibration comprises receiving a first set of operations at the circuitry to exhaustively determine the initial value of the parameter, and wherein periodically subjecting the receive component to the second calibration comprises receiving a second set of operations at the circuitry to update the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value.

VI.B.4(A) 7[a] The method of claim 1, wherein subjecting the receive component to the first calibration comprises receiving a first set of operations at the circuitry to exhaustively determine the initial value of the parameter, and

As discussed in SNQ #1, *Meaney* discloses subjecting the circuitry of the receive component to a first calibration by calibrating clock delay during initialization of the computer system, which is triggered by sending a known data pattern across a data transfer interface, to exhaustively determine the initial value of clock delay. *Supra* Section VI.A.4 (A). To the extent Patent Owner argues that *Meaney* does not disclose this element, *Nguyen* discloses the first calibration comprises receiving a first set of operations at the circuitry to exhaustively determine the initial value of the parameter. Ex. 1002, Appx, 65-70; Ex. 1005, ¶¶ [0071]-[0074], [0110], Fig. 4B.

As shown in Fig. 4B, reproduced below, *Nguyen* discloses steps taken during an initialization or calibration phase, including repeating many of the steps of the initialization or calibration process until the voltage parameter reaches a satisfactory level. Ex. 1005, ¶¶ [0071]-[0074], Fig. 4B (annotated):

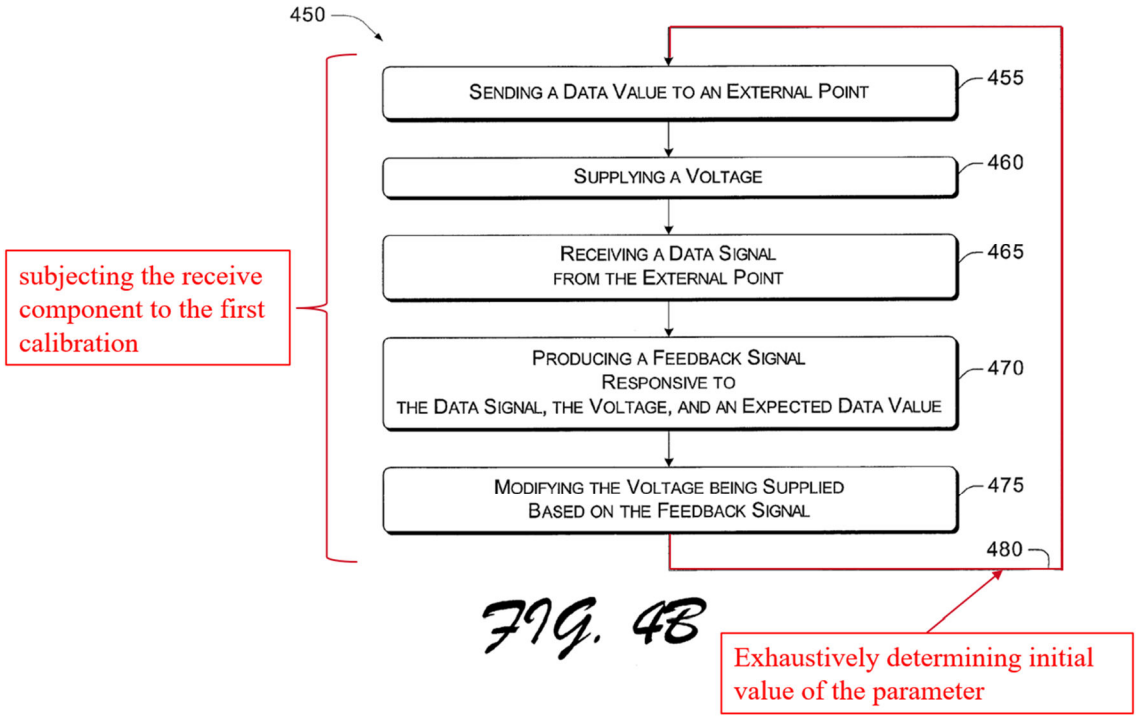


FIG. 4B

Similarly, as shown in Fig. 9B, reproduced below, *Nguyen* discloses steps taken during an initialization or calibration phase, including repeating many of the steps of the initialization or calibration process until the compensated voltage reaches a satisfactory level. Ex. 1005, ¶¶ [0107-0110], Fig. 9B (annotated):

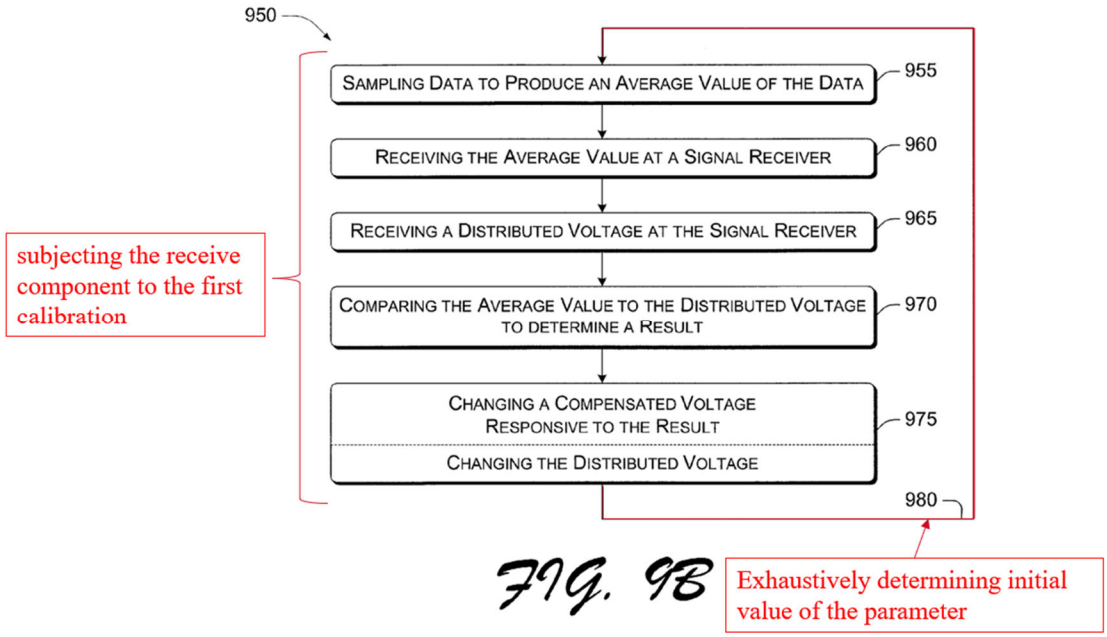


FIG. 9B

A POSITA would have understood this disclosure of *Nguyen* to disclose "exhaustively determining the initial value" of the calibrated parameter. Ex. 1002, Appx, 65-70.

As discussed in Section VI.B.1, it would have been obvious to a POSITA to enhance the calibration techniques of *Meaney* with the exhaustive calibration techniques of *Nguyen*. Ex. 1002, Appx, 54. *Meaney* discloses initialization calibration techniques that involve repeating the clock calibration step twice. Ex. 1004, ¶¶ [0004], [0024]-[0033], Fig. 3. In combination with *Nguyen*, a POSITA would have been motivated to repeat the clock calibration step of *Meaney*, as well as other initialization steps, until the clock delay recaches a satisfactory value. Ex. 1002, Appx, 65-70. For example, a POSITA would have been motivated to perform these steps periodically not just during initialization but periodically to account for shifts in temperature or power supply voltage. *Id.* at Appx, 67.

VI.B.4 (B) 7[b] wherein periodically subjecting the receive component to the second calibration comprises receiving a second set of operations at the circuitry to update the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value.

As discussed in SNQ #1, *Meaney* discloses receiving a second set of operations at the circuitry to update the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value. *Supra* Section VI.A.4 (B). To the extent Patent Owner argues that *Meaney* does not disclose this limitation, *Nguyen* also discloses that calibration may be repeated to correct for drifts in the calibrated parameter, or in response to "a predetermined number of detected (e.g., bit or byte) errors." Ex. 1002, Appx, 71-72; Ex. 1005, ¶¶ [0094], [0147]. A POSITA would have understood a predetermined number of detected errors to represent a delta value (e.g., the delta between no errors and a certain number of errors) that represents a parameter drift. Ex. 1002, Appx, 71-72. Accordingly, a POSITA would have understood that *Nguyen* discloses recalibration "if a desired value of the parameter has drifted from the existing value by more than a delta value." *Id*.

As discussed in Section VI.B.1, it would have been obvious to a POSITA to enhance the recalibration triggers of *Meaney* with the predetermined number of errors of *Nguyen*. Ex. 1002, Appx, 54. *Meaney* also discloses triggering recalibration when correctable errors are found in the data. Ex. 1004, ¶ [0017]. Accordingly, it would have been obvious for a POSITA to modify *Meaney*'s error- triggered recalibrations to include the "predetermined number of detected errors"

of *Nguyen* to allow the system of *Meaney* to react to a desired level of error tolerance for example, account for errors due to changes in voltage and temperature. Ex. 1002, Appx, 71-72.

VI.B.5 Claim 10

10. A system, comprising:

a receive component, the receive component having circuitry to receive data communicated across a channel by a transmit component;

the receive component to

perform at system initialization a first calibration, the first calibration to identify an initial value for a parameter affecting proper reception by the circuitry of the data communicated across the channel, and

perform on a periodic basis a second calibration, the second calibration to update an existing value of the parameter for drift attributable to change in at least one of voltage or temperature, wherein a time duration of the second calibration is constrained to be shorter than a time duration of the first calibration; and

circuitry to store the existing value of the parameter, the existing value of the parameter dependent on the initial value and any updates from the second calibration.

As discussed in SNQ #1, elements 10[pre], 10[b], 10[c], and 10[d] are taught by *Meaney*. *Supra* Sections VI.A.7 (A), (C), (D), and (E).

VI.B.5(A) 10[a] a receive component, the receive component having circuitry to receive data communicated across a channel by a transmit component;

As discussed in SNQ #1, *Meaney* discloses a receive component having circuitry to receive data communicated across a channel by a transmit component. *Supra* Section VI.A.7 (B). As discussed above in 1[pre], the combination of *Meaney* and *Nguyen*, in view of the knowledge of a POSITA, renders obvious "the receive component having circuitry to receive data." *Supra* Section VI.B.2 (A); Ex. 1002, Appx, 73-74.

VI.B.5(B) 10[e] circuitry to store the existing value of the parameter,

As discussed in SNQ #1, *Meaney* discloses that the computer system includes clock calibrating hardware including an SAP that uses a hardware interface protocol to read and write registers in the logic of the interface. Ex. 1004, ¶¶ [0015]-[0016], [0020]-[0021], [0023]. To the extent Patent Owner argues that *Meaney* does not disclose this limitation, *Nguyen* also discloses

"circuitry to store the existing value of the parameter." Ex. 1002, Appx, 75-76. For example, *Nguyen* discloses the use of a "parameters table" and a parameters table bus during initialization/calibration to store calibrated parameter values. Ex. 1005, ¶¶ [0130]-[0133]. As discussed in Section VI.B.1, it would have been obvious to a POSITA to enhance the computer system interface of *Meaney* with the calibration techniques and receiver circuitry of *Nguyen*. Ex. 1002, Appx, 54. Moreover, it would have been obvious for a POSITA to modify *Meaney*'s system to include the parameter table and parameter table bus of *Nguyen* to allow the system of *Meaney* to more easily and reliably store and retrieve clock delay values from calibrations and recalibrations. Ex. 1002, Appx, 75.

VI.B.5(C) 10[f] the existing value of the parameter dependent on the initial value and any updates from the second calibration.

As discussed in SNQ #1, *Meaney* discloses "the existing value of the parameter dependent on . . . any updates from the second calibration" by updating clock delay based on a recalibration. *Supra* VI.A.7 (G). As discussed above in this SNQ #2, *Meaney* and *Nguyen*, in view of the knowledge of a POSITA, renders obvious "the existing value of the parameter dependent on the initial value." *Supra* Section VI.B.2 (B); Ex. 1002, Appx, 77.

VI.B.8 Claim 15

15. The system of claim 10, wherein the receive component is to perform, responsive to the second calibration, one of an increment operation or a decrement operation upon the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value.

As discussed in SNQ #1, *Meaney* teaches recalibration may be performed in response to a trigger event that suggests that the clock delay has drifted and the data capture time window is no longer accurate. *Supra* VIII.A.10. As discussed in this SNQ #2 regarding 1[d] and 7[b], the combination of *Meaney* and *Nguyen* teaches applying an increment or decrement operation by adjusting the clock delay through by a predetermined offset in response to drift by more than a delta value (e.g., a predetermined number of detected errors). *Supra* Section VI.B.2 (B), VIII.B.4 (B); Ex. 1002, Appx, 78.

VI.B.9 Claim 16

VI.B.9(A) 16[a] The system of claim 10, further comprising circuitry to store a first expected pattern and a second expected pattern, and

VI.B.9(B) 16[b] circuitry to compare the first expected pattern with a pattern received from the transmit component in association with the first calibration, and to compare the second expected pattern with a pattern received from the transmit component in association with the second calibration.

As discussed in SNQ #1, *Meaney* teaches circuitry to store a first expected pattern and a second expected pattern, as well as comparing first expected patterns and second expected patterns to data patterns received from a transmit component in association with first and second calibrations. *Supra* Section VI.A.11.

To the extent Patent Owner argues that *Meaney* does not teach these limitations, *Nguyen* discloses first and second expected patterns and circuitry for receiving, storing, and providing the expected data, and circuitry for comparing the same. Ex. 1005, ¶¶ [0112], [0114], Fig. 10A. Specifically, as shown in annotated Fig. 10A below, *Nguyen* discloses a "digital calibration component 510" that has interfaces for "receiving and/or providing calibration data" including a "calibration data register 1005." Ex. 1005, ¶¶ [0112], [0114]. *Nguyen* explains that the calibration data includes "expected value[s] to be received from a transmitting unit" (i.e., "expected pattern[s]") which is compared against received data to determine if they are equal in the comparison unit 1010. *Id.*, ¶ [0114].

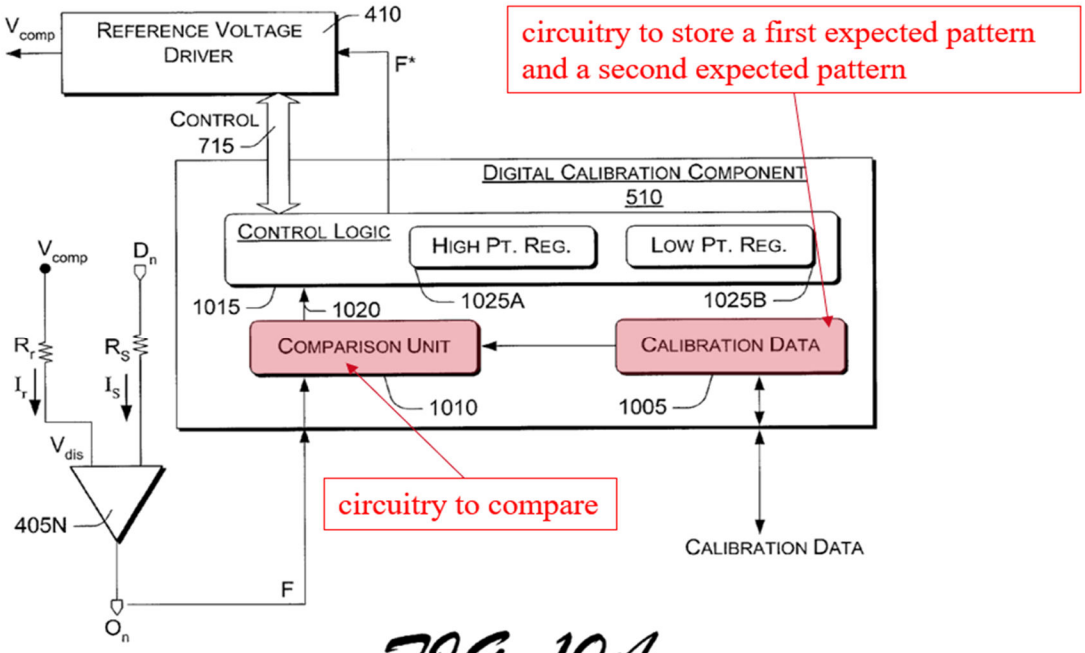


FIG. 10A

As discussed in Section VI.B.1, it would have been obvious to a POSITA to enhance the computer system interface of *Meaney* with the calibration techniques and the storage and receiver circuitry of *Nguyen*. Ex. 1002, Appx, 79-81. For example, because *Meaney* does not specify the particular receiver circuitry that is employed in comparing the known data pattern with the received data pattern, it would have been obvious to look to *Nguyen* for the type of circuitry suitable for storage of the data pattern. *Id.* A POSITA would have been motivated to do because of the benefit of having local storage of the expected patterns for use during calibrations without needing to request the expected pattern from another location. Ex. 1002, Appx, 80. For example, a POSITA would find it obvious to include the digital calibration component 510 of *Nguyen* to operate the receiver calibration logic 14 of *Meaney*, as shown below. *Id.*

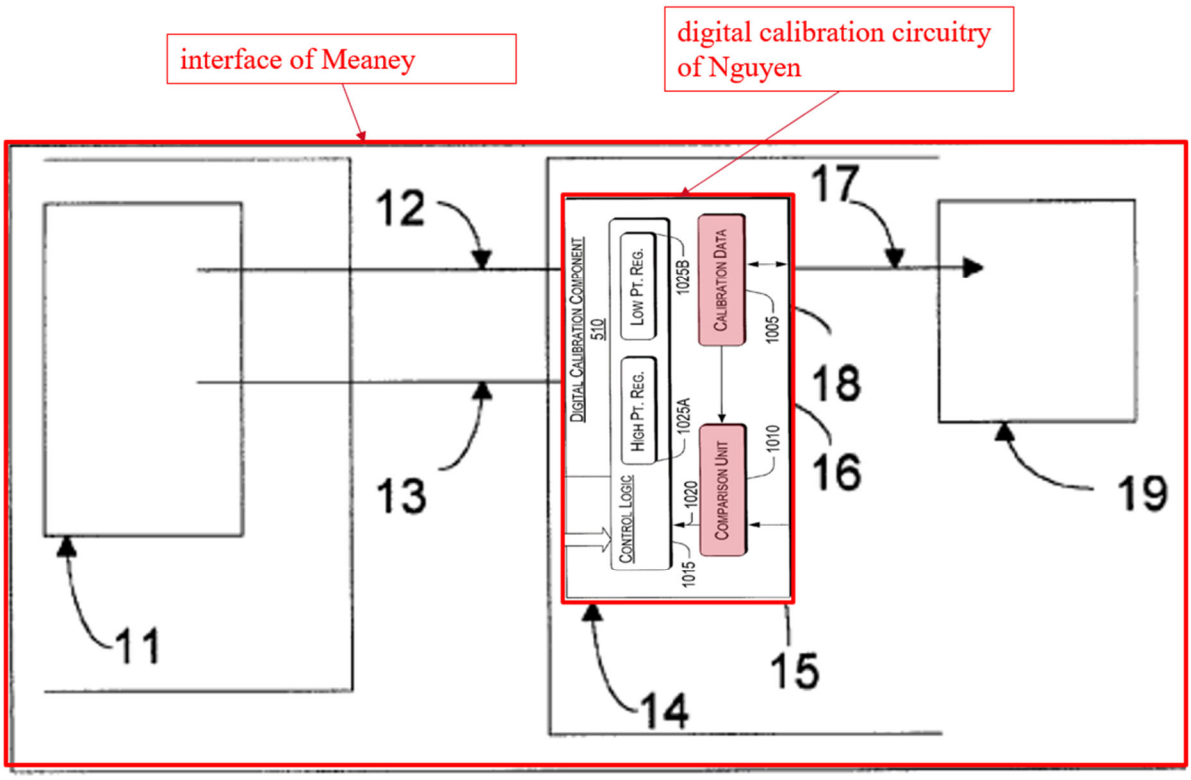


FIGURE 1.

VI.C SNQ #3: Claims 4, 5, 13, 14, 17-19 of the '466 Patent are obvious in view of Meaney and Greef in view of the knowledge of a POSITA.

The combination of *Meaney* and *Greeff* teaches and/or suggests all limitations of claims 4, 5, 13, 14, and 17-19, and thus renders those claims obvious. Ex. 1002, Appx, 82-123. Specifically, *Meaney* in combination with *Greeff* discloses or renders obvious "an existing value representative of at least one of a termination resistance and a driver strength" as required by independent claim 17. Ex. 1002, Appx, 82. All other elements of claims 4, 5, 13, 14, and 17-19 are disclosed or at least rendered obvious by *Meaney* as described above in SNQ #1.

VI.C.1 One of skill in the art would have been motivated to combine *Meaney* and *Greeff*

Meaney and *Greeff* both pertain to electronic systems and methods for calibration and adjustment of system parameters. *Meaney* discloses a system for calibrating a parameter of an electronic system, while *Greeff* discloses termination circuitry that are integral to electronic system performance. Ex. 1004, Abstract, ¶¶ [0008]-[0017], [0039]-[0040]; Ex. 1006, 3:65-4:20, 4:11-20,

5:59-6:6, 7:52-8:56; Ex. 1002, Appx, 82. Both references emphasize the importance of calibrating variables both initially, prior to operation, and during operation. Ex. 1004, ¶¶ [0006], [0008], [0013], [0021], [0024], [0038]; Ex. 1006, 4:11-20, 7:52-8:56; Ex. 1002, Appx, 82.

A POSITA would have been motivated to incorporate the termination circuitry disclosed in *Greeff* with the system of *Meaney* to achieve enhanced system performance and reliability. Ex. 1002, Appx, 82. *Greeff's* termination circuitry ensures proper signal integrity and reduces reflections in high-speed data transmission systems. Ex. 1006, 1:28-31, 4:10-12, 8:3-5; Ex. 1002, Appx, 82. *Meaney's* calibration techniques, when applied to the termination resistance and transistor drive strength of *Greeff*, would ensure that these parameters remain optimal throughout system operation. Ex. 1002, Appx, 82.

Moreover, both *Meaney* and *Greeff* disclose methods for calibrating variables initially and during operation for recalibration. Ex. 1004, ¶¶ [0006], [0008], [0013], [0021], [0024], [0038]; Ex. 1006, 4:11-20, 7:52-8:56; Ex. 1002, Appx, 82. A POSITA would have found it obvious to apply *Meaney's* calibration process to *Greeff's* termination circuitry in order to optimize the termination resistance and drive strength of the termination circuitry. Ex. 1002, Appx, 82. This represents the use of a known technique to predictably improve a similar system in the same way. *KSR Int'l Co. v. Teleflex, Inc*., 127 S.Ct. 1727, 1740 (2007).

A POSITA would have had a reasonable expectation of success in combining *Meaney* and *Greeff*. Ex. 1002, Appx, 82. The integration of *Greeff's* termination circuitry into *Meaney's* system would have been straightforward and cost-effective. *Id.* The required modifications are minimal, and the results of the combination are predictable, given the complementary nature of the technologies. *Id*.

VI.C.2 Claim 4

4. The method of claim 1, wherein the parameter is a link termination resistance.

As shown below in annotated Fig. 1, *Greeff* discloses a multidrop bus including circuitry capable of receiving a digital signal that includes termination circuitry 120 including a switch 122 connected between a "trimmable" termination resistor 124, having a trimmable termination resistance RTERM, and a reference voltage VTERM. Ex. 1006, 3:65-4:20, 5:59-6:6, 7:52-8:56, Fig. 1; Ex. 1002, Appx, 83. A POSITA would have understood *Greeff*'s termination resistance to be the claimed "link termination resistance." *Id. Greeff* explains that the termination resistance is

modified during initial calibration and recalibration processes to provide a substantially optimal termination of the bus 102. Ex. 1006, 4:11-20, 7:52-8:56; Ex. 1002, Appx, 83.

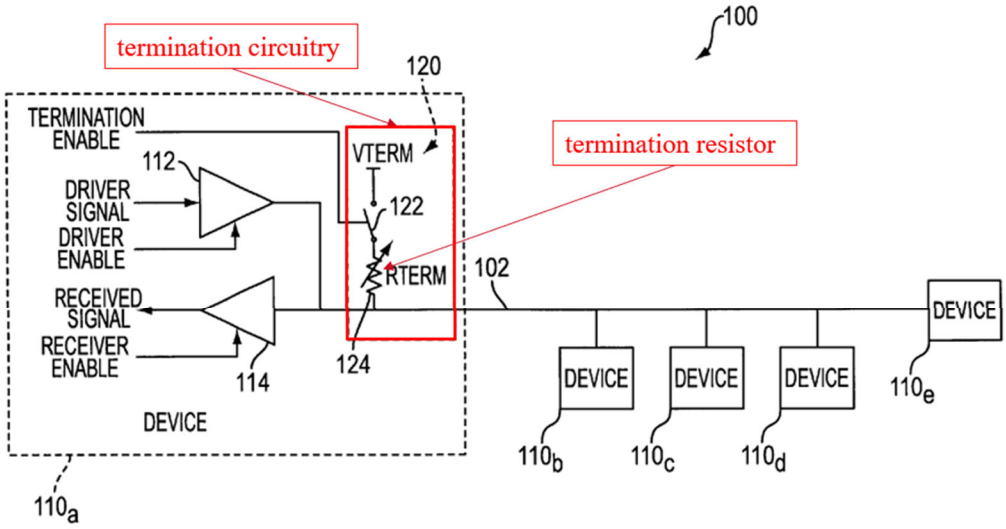


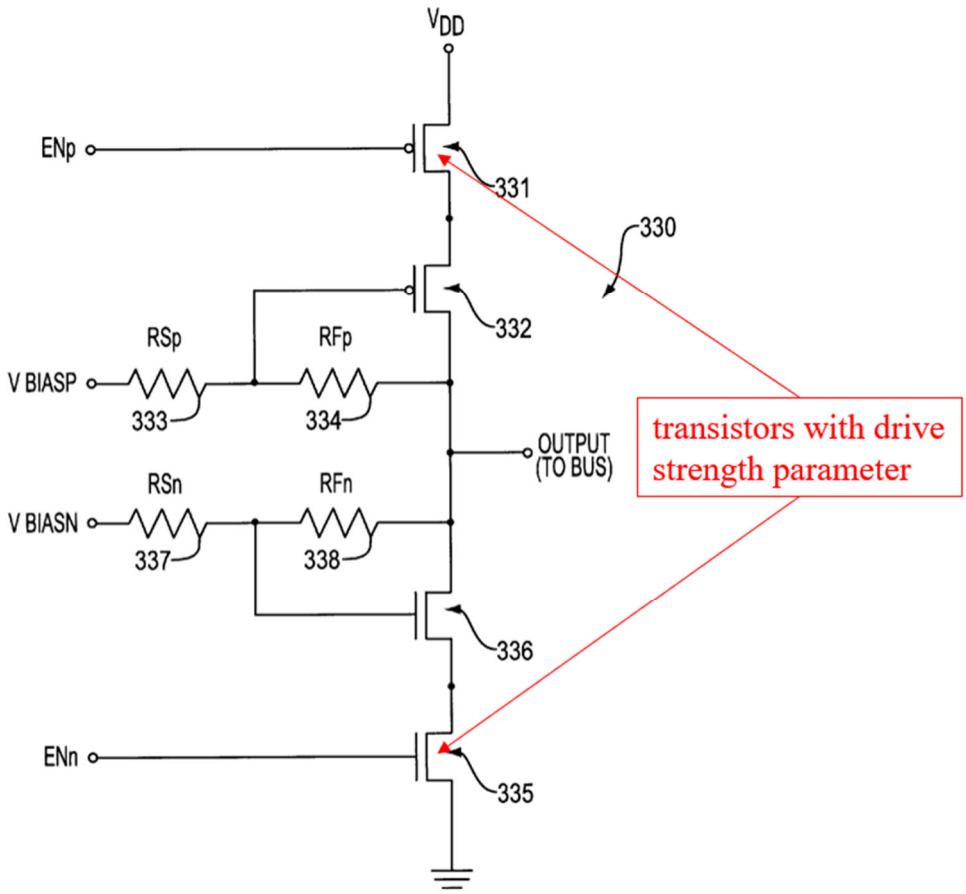
FIG. 1

Thus, *Greeff* in combination with *Meaney* discloses claim 4. Ex. 1002, Appx, 83.

VI.C.3 Claim 5

5. The method of claim 1, wherein the parameter is a driver strength.

As shown below in annotated Fig. 3, *Greeff* discloses an active termination circuit 330 including circuitry capable of receiving a digital signal that uses transistors 331 and 335 as switches that enable or disable the active termination. Ex. 1006, 6:40-55, Fig. 3; Ex. 1002, Appx, 84-85. *Greeff* explains that the drive strength of the transistors can be calibrated. Ex. 1006, 8:3-5, claim 42; Ex. 1002, Appx, 84-85. A POSITA would have understood *Greeff*'s drive strength to be the claimed "driver strength." Ex. 1002, Appx, 84-85.



Thus, *Greeff* in combination with *Meaney* discloses claim 5. Ex. 1002, Appx, 84-85.

VI.C.4 Claim 13

13. The system of claim 10, wherein the parameter is a link termination resistance.

Supra Section VI.C.2.

VI.C.5 Claim 14

14. The system of claim 10, wherein the parameter is a driver strength for a driver of the receive component.

See Section VI.C.3.

VI.C.6 Claim 17

VI.C.6(A) 17[pre] A system comprising:

To the extent the preamble is limiting, *Meaney* discloses a system. *Supra* Section VI.A.7 (A).

VI.C.6(B) 17[a] circuitry to store an existing value representative of at least one of a termination resistance and a driver strength to be applied in association with data communicated across a channel;

As discussed in SNQ #1, *Meaney* discloses circuitry to store an existing value of a parameter. *Supra* Section VI.A.7 (F). *Greeff* discloses that the existing value is representative of at least one of a termination resistance and a driver strength to be applied in association with data communicated across a channel. Ex. 1002, Appx, 86-89. As discussed above regarding claims 4 and 5, *Greeff* discloses calibration of both a termination resistance and a drive strength of transistors for active termination. *Supra* Sections VI.C.2-3.

VI.C.6(C) 17[b] circuitry to perform a first calibration at system initialization, to identify a first value to be initially applied as the existing value

As discussed in SNQ #1, *Meaney* discloses circuitry to perform a first calibration at system initialization, to identify a first value to be initially applied as the existing value. *Supra* Section VI.A.7 (A)-(C). *Greeff* discloses calibrating parameters such as termination resistance prior to the first use of the system, which it refers to as "static calibration." Ex. 1006, 4:10- 13, 7:52-61. As shown in Fig. 2 (annotated below), *Greeff* discloses active termination circuitry that would be used to calibrate the termination resistance ("RTERM"). Ex. 1006, 4:10-13, 7:52-61, Fig. 2; Ex. 1002, Appx, 89-90.

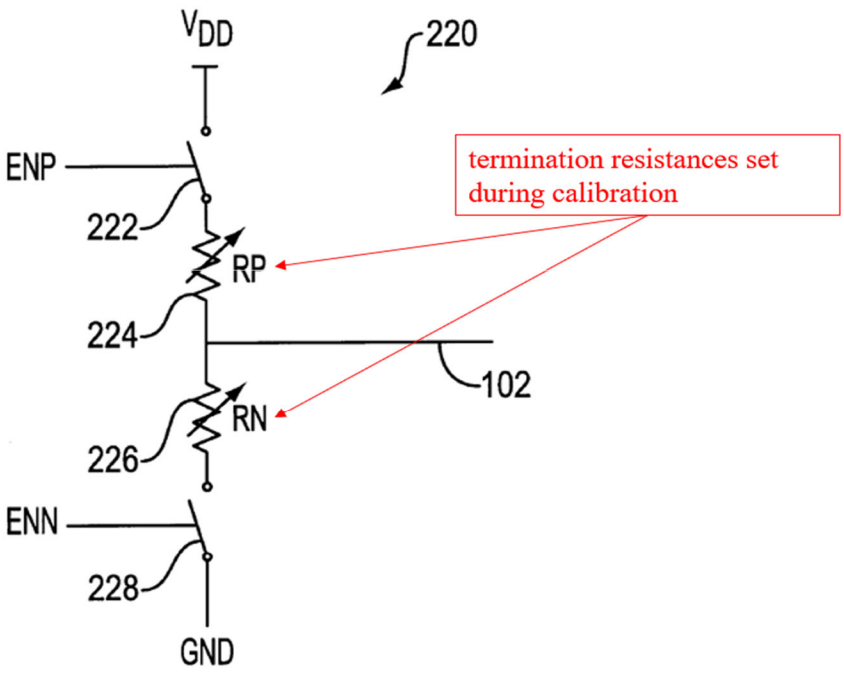


FIG. 2

For example, *Greeff* explains that the "two termination resistances RP, RN would be set during the calibration process to provide substantially optimal termination," and that the termination enable signals ENP and ENN would be generated during calibration as well. Ex. 1006, 6:3-5; Ex. 1002, Appx, 89-95.

VI.C.6(D) 17[c] the first calibration to be performed during a first calibration interval prior to normal system operation; and

As discussed in SNQ #1, *Meaney* discloses the first calibration to be performed during initialization, prior to normal system operation. *Supra* Section VI.A.7 (B). *Greeff* discloses calibrating parameters such as termination resistance prior to the first use of the system, which it refers to as "static calibration." Ex. 1006, 7:52-61; Ex. 1002, Appx, 96-99. A POSITA would have understood calibration performed prior to first use to be calibration performed "during a first calibration interval prior to normal system operation." Ex. 1002, Appx, 96-99.

VI.C.6(E) 17[d] circuitry to periodically perform a second calibration, to update the existing value;

As discussed in SNQ #1, *Meaney* discloses periodically subjecting receiver circuitry to a second calibration in the form of a "recalibration" that updates an existing parameter value. *Supra* Sections VI.A.7 (B)(D). As discussed above in 17[b], *Greeff* discloses circuitry for performing calibration of termination resistance. *Greeff* further discloses recalibrating termination resistance during operation of the system, for example when the value changes due to temperature or supply voltage changes, which *Greeff* refers to as "dynamic calibration." Ex. 1006, 7:52-65; Ex. 1002, Appx, 100-105. Thus, the combination of *Meaney* and *Greeff* discloses circuitry to periodically recalibrate an existing value of termination resistance. Ex. 1002, Appx, 100-105.

VI.C.6(F) 17[e] wherein the existing value is initially set and periodically updated responsive to the first calibration and the second calibration, respectively, and

As discussed in SNQ #1, *Meaney* discloses determining an initial value for a parameter through an initial calibration and periodically performing a recalibration to update the parameter value. *Supra* Section VI.A.1 (B), (C).

Greeff discloses calibration techniques including initially setting a termination resistance at a known value and then performing the calibration process to update the value. Ex. 1006, 8:27-33 ("Another calibration process may [ ] first set[] the resistance of the pull-up (or pull-down) resistor . . . against a known passive resistor, and then balance[e] the pull-down (or pull-up) resistor."); Ex. 1002, Appx, 106-111. *Greeff* also discloses an initial calibration to set a value (static calibration) and a second calibration (dynamic calibration) to adapt to changes in operating conditions. Ex. 1006, 4:10-13, 7:52-617:52-65; Ex. 1002, Appx, 106-111.

Thus, *Meaney* and *Greeff*, in view of the knowledge of a POSITA, render obvious "wherein the existing value is initially set and periodically updated responsive to the first calibration and the second calibration, respectively." Ex. 1002, Appx, 106-111.

VI.C.6(G) 17[f] wherein the second calibration is constrained to be performed during a time period that is shorter than a time period of the first calibration; and

As discussed in SNQ #1, *Meaney* discloses "wherein the second calibration is constrained to be performed during a time period that is shorter than a time period of the first calibration." *Supra* VIII.A.1.vi; Ex. 1002, Appx, 112-113.

VI.C.6(H) 17[g] wherein the system further comprises a receive component, the at least one to be applied to permit proper reception of a digital signal to be communicated across a communications channel.

As discussed in SNQ #1, *Meaney* discloses "a system further comprises a receive component" and at least one parameter "to be applied to permit proper reception of a digital signal to be communicated across a communications channel." *Supra* VIII.A.1.i & iii.

Greeff further discloses that the termination resistance and a driver strength are applied to permit proper reception of a digital signal to be communicated across a communications channel. Ex. 1002, Appx, 113-117. *Greeff* explains that termination resistance is calibrated to provide substantially optimal termination of the bus, and that drive strength is calibrated to improve achieve the desired active termination. Ex. 1006, 1:28-31, 4:10-12. Both of these calibrations are performed to improve the termination of the system, which improves digital signal integrity by minimizing transmission line reflections. Ex. 1006, 1:28-31, 4:10-12, 8:3-5; Ex. 1002, Appx, 113-17.

VI.C.7 Claim 18

18. The system of claim 17, wherein the circuitry to perform the second calibration is, responsive to the second calibration, to perform one of an increment operation or a decrement operation upon the existing value if the desired value has drifted from the existing value by more than a delta value relative to an existing value.

As discussed in SNQ #1, *Meaney* discloses this limitation either alone or in combination with the knowledge of a POSITA. *Supra* Section VI.A.10. Specifically, *Meaney* discloses that the receive component performs, responsive to the second calibration, one of an increment operation or a decrement operation upon the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value. *Id. Meaney* further discloses that

recalibration may be performed in response to a trigger event that suggests that the parameter has drifted and the data capture time window has changed and is no longer accurate, which may be indicated, for example, by the detection of correctable errors. *Id.* Moreover, as explained in SNQ #1, it would have been obvious to a POSITA, in response to a recalibration, to perform an increment operation or a decrement operation on the existing value, to shift the value of the based on the results of the recalibration. *Id.*

Greeff similarly discloses increasing and decreasing parameters used in the active termination circuit to account for variations in process, voltage, or temperature. *Greeff*, Ex. 1006, 7:66-8:5; Ex. 1002, Appx, 118-20. It would have been obvious to a POSITA to, in response to a recalibration, implement the increment or decrement operations of *Meaney* (and that were known in the art) when calibrating the termination resistance of *Greeff*. Ex. 1002, Appx, 118-20.

VI.C.8 Claim 19

19. The system of claim 18, further comprising circuitry to store a first expected pattern and a second expected pattern, and circuitry to compare the first expected pattern with a pattern received from an external component in association with the first calibration, and to compare the second expected pattern with a pattern received from the external component in association with the second calibration.

As discussed in SNQ #1, *Meaney* discloses circuitry to store a first expected pattern and a second expected pattern, and circuitry to compare the first expected pattern with a pattern received from an external component in association with the first calibration, and to compare the second expected pattern with a pattern received from the external component in association with the second calibration. *Supra* Sections VIII.A.6, 11; Ex. 1002, Appx, 121.

VI.D SNQ #4: Claims 4, 5, 13, 14, 17-19 of the '466 Patent are obvious in view of Meaney, Nguyen, and Greef in view of the knowledge of a POSITA.

The combination of *Meaney*, *Nguyen* and *Greeff* discloses and/or suggests all limitations of claims 4, 5, 13, 14, and 17-19, and thus renders those claims obvious. Ex. 1002, Appx, 124-48. Specifically, as discussed above in SNQ #2, *Meaney* in combination with *Nguyen* discloses applying offsets to existing values to determine a calibrated value, and circuitry for receiving a digital signal, calibrating computer system parameters, and storing calibration data. Ex. 1002, Appx, 54. Additionally, as discussed above in SNQ #3, *Meaney* and *Greeff*, in view of the

knowledge of a POSITA, render obvious "an existing value representative of at least one of a termination resistance and a driver strength." *Id.*, Appx, 86-87. As discussed below, for the same reasons, the combination of *Meaney*, *Nguyen*, and *Greeff* discloses those same limitations. All other elements of claims 4, 5, 13, 14, and 17-19 are disclosed or rendered obvious by *Meaney* as explained in SNQ #1.

VI.D.1 One of skill in the art would have been motivated to combine *Meaney, Nguyen,* and *Greeff*

In addition to being motivated to combine *Meaney* and *Nguyen* as described in Section VI.B.1 of SNQ #2, a POSITA would have been motivated to further combine *Meaney* and *Nguyen* with *Greeff* with a reasonable expectation of success for the same reasons discussed above in Section VI.C.1; Ex. 1002, Appx, 124.

VI.D.2 Claims 4, 5, 13, and 14

As discussed above in SNQ #3, each and every element of claims 4, 5, 13, and 14 are taught by *Greeff*. *Supra* Sections VI.C.2-5. The combination of *Meaney*, *Nguyen*, and *Greeff* as described above, does not affect the disclosure of *Greeff* that render those claims obvious. Accordingly, the combination of *Meaney*, *Nguyen*, and *Greeff* render claims 4, 5, 13, and 14 obvious for the same reasons as discussed in SNQ #3.

VI.D.3 Claim 17

As discussed in SNQ #3, elements 17[pre], 17[c], 17[e], 17[f], and 17[g] are taught by *Meaney* and *Greeff*. *Supra* Sections VI.C.6 (A), (D)-(H).

VI.D.3(A) 17[a] circuitry to store an existing value representative of at least one of a termination resistance and a driver strength to be applied in association with data communicated across a channel;

As discussed in SNQ #2, *Meaney* and *Nguyen* disclose circuitry to store an existing value of a parameter. *Supra* Section VI.B.5 (B). As discussed in SNQ #3, *Meaney* and *Greeff* disclose termination resistance to be applied in association with data communicated across a channel. *Supra* Section VI.C.6 (B); Ex. 1002, Appx, 125.

VI.D.3(B) 17[b] circuitry to perform a first calibration at system initialization, to identify a first value to be initially applied as the existing value,

As discussed in SNQ #3, *Meaney* and *Greeff* disclose circuitry to perform a first calibration at system initialization, to identify a first value to be initially applied as the existing value. *Supra* Section VI.C.6 (B). To the extent Patent Owner argues that *Meaney* and *Greeff* do not disclose circuitry to perform a first calibration, *Nguyen* discloses calibration circuitry. *Supra* Sections VI.B.2 (A), VI.B.7; Ex. 1002, Appx, 125-33.

VI.D.3(C) 17[d] circuitry to periodically perform a second calibration, to update the existing value;

As discussed in SNQ #3, *Meaney* and *Greeff* disclose circuitry to perform a second to update the existing value. *Supra* Section VI.C.6 (E); Ex. 1002, Appx, 134-41. To the extent Patent Owner argues that *Meaney* and *Greeff* do not disclose circuitry to perform a second calibration, *Nguyen* discloses such calibration circuitry. *Supra* Sections VI.B.2 (B), VI.B.7; Ex. 1002, Appx, 134-41.

VI.D.4 Claims 18 and 19

As discussed above in SNQ #3, claim 18 is taught by the combination of *Meaney* and *Greeff*, and claim 19 is taught by *Meaney*. *See supra* Sections VIII.C.7- 8; Ex. 1002, Appx, 143-48.

VI.E SNQ #5A: Claim 3 of the '466 Patent is obvious in view of Meaney and Allee in view of the knowledge of a POSITA.

VI.E.1 One of skill in the art would have been motivated to combine *Meaney* and *Allee*

As described above, *Meaney* discloses calibration by comparing a known data pattern with a received data pattern. *Supra* Section VI.A.6. *Allee* provides details of a comparator that is self-calibrating and allows expansion of the functionality of digital integrated circuits. Ex. 1007, 2:35-36, 3:9-19; Ex. 1002, Appx, 149. A POSITA would have been motivated to combine *Meaney* and *Allee* with a reasonable expectation of success to use the comparator of *Allee* to compare the data patterns of *Meaney* to achieve the stated benefits of self-calibration and expanded functionality of digital circuitry. Ex. 1002, Appx, 149. Accordingly, a POSITA would have been motivated to combine *Meaney* and *Allee* with a reasonable expectation of success, because the teaching,

suggestion, and motivation in *Meaney* and in *Allee* would have led a POSITA to arrive at the claimed invention. *Id.*

VI.E.1(A) Claim 3

3. The method of claim 1, wherein the parameter is a voltage level for a comparator.

Allee discloses computer systems including comparators that may be calibrated by a self-calibration circuit 116 to adjust the input voltage ("voltage level for a comparator"). Ex. 1007, 3:9-19,4:1-9, 6:17-39, Fig. 1; Ex. 1002, Appx, 149-151. As depicted in Fig. 1 below, *Allee* discloses comparators 102 that may be self- calibrated to compensate for an input offset by adjusting an input signal equal to a desired reference voltage. Ex. 1007, 3:9-19, Fig. 1 (annotated).

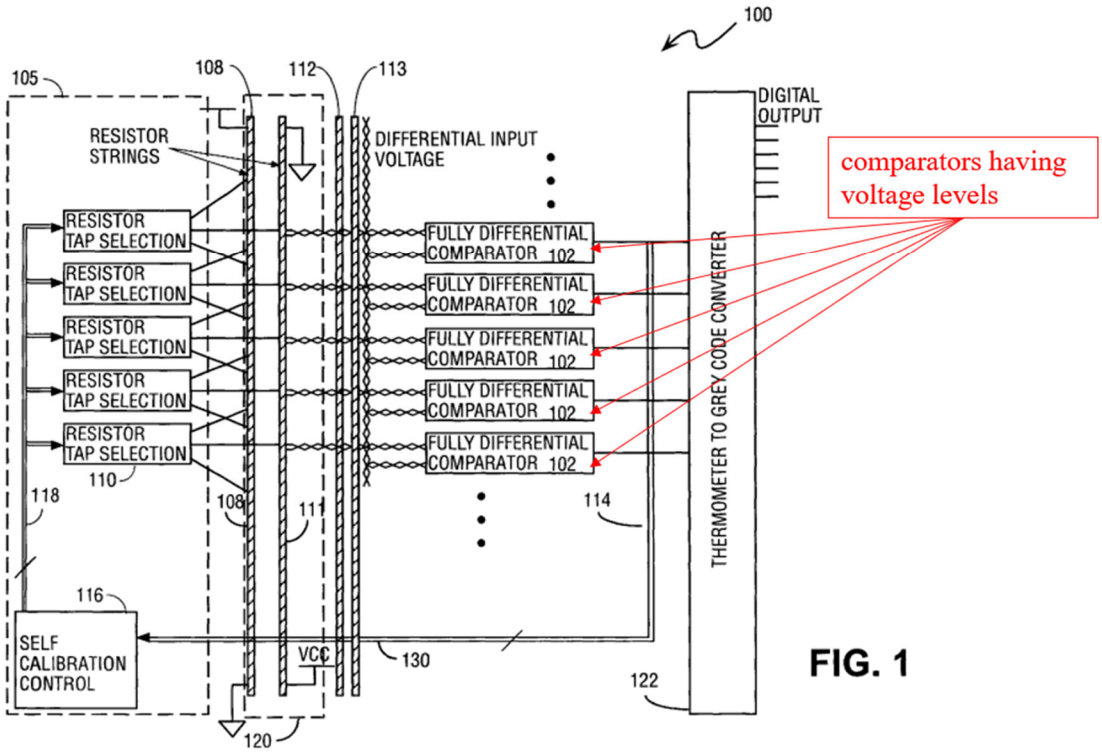


FIG. 1

Allee further discloses a self-calibration circuit 116 that calibrates the comparators 102 to adjust the voltage by adjusting the tap position of the reference voltage. Ex. 1007, 4:1-9; Ex. 1002, Appx, 149-150. *Allee* discloses both an initial calibration process (before operation), and self-calibration of the comparator during operation. Ex. 1007, 6:17-39; Ex. 1002, Appx, 149-151.

VI.F SNQ #5B: Claim 3 of the '466 Patent is obvious in view of Meaney, Nguyen, and Allee in view of the knowledge of a POSITA.

VI.F.1 One of skill in the art would have been motivated to combine *Meaney, Nguyen,* and *Allee*

In addition to being motivated to combine *Meaney* with *Nguyen* as explained in Section VI.B.1, a POSITA would have been motivated to further combine *Meaney* and *Nguyen* with *Allee* with a reasonable expectation of success for the same reasons stated above in Section VI.E.1. Ex. 1002, Appx, 152.

VI.F.1(A) Claim 3

3. The method of claim 1, wherein the parameter is a voltage level for a comparator.

Supra Section VI.E.1.

VII. CONCLUSION

For the above reasons, the references discussed herein raise substantial new questions of patentability with respect to claims 1-19 of the '466 Patent and render these claims unpatentable.

RESPECTFULLY SUBMITTED,

By: /SXShort/ Reg. No. 45,105

Shayne S. Short, Ph.D.
Attorney for Third Party Requester NXP USA, Inc.

Garlick & Markison
2025 Guadalupe Street, Suite 260
Austin, TX 78705
Phone: 512-825-1145
E-mail: sxshort@garlickmarkison.com

CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. § 1.510(b)(5), that on December 31, 2025 I caused a true and correct copy of the foregoing Request for *Ex Parte* Reexamination Under 35 U.S.C. §322 and 37 C.F.R. §1.913 to be served via First Class Mail on the Patent Owner of U.S. Patent No. 9,160,466 at its correspondence address of record at the U.S. Patent and Trademark Office.

Counsel:

Marc P. Schuyler / Rambus
P.O. Box 2535
Saratoga, CA 95070

Patent Owner:

K.MIZRA LLC
777 Brickell Avenue
#500-96031
Miami, FL 33131

Date: 12/31/2025

By: /Melanie Murdock/
Melanie Murdock, Paralegal

Garlick & Markison
2025 Guadalupe Street, Suite 260
Austin, TX 78705