Mail Stop *Ex Parte* Reexam

In re *Ex Parte* Reexamination of:	)	
U.S. Patent No. 9,147,747 B2	)	
Issued: September 29, 2015	)	Group Art Unit: To Be Assigned
Named Inventor: Ching-Wen Hung, *et al.*	)	Examiner: To Be Assigned
Control Number: To Be Assigned	)	
Filed: May 2, 2013	)	
Title: SEMICONDUCTOR STRUCTURE WITH HARD MASK DISPOSED ON THE GATE STRUCTURE	)	**VIA Patent Center**

Attn: Central Reexamination Unit
Commissioner for Patents

P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

Taiwan Semiconductor Manufacturing Company Limited ("Requestor") respectfully requests *ex parte* reexamination of U.S. Patent No. 9,147,747 ("'747 Patent").

Prior art references, including at least Pethe, Chang, Pham, Sell, Huang, Chi, and Hong, raise substantial new questions of patentability with respect to claims 1-9 of the '747 Patent. This prior art undercuts the Applicant's arguments during prosecution of the '747 Patent, rendering claims 1-9 anticipated and/or obvious

under 35 U.S.C. §§ 102, 103. Requestor respectfully asks that the Office grant this Request for *ex parte* reexamination and cancel claims 1-9.

In accordance with 37 C.F.R. § 1.510(b), this Request includes:

> (1) A statement pointing out each substantial new question of patentability based on prior patents and printed publications.
>
> (2) An identification of every claim for which reexamination is requested, and a detailed explanation of the pertinency and manner of applying the cited prior art to every claim for which reexamination is requested. For each statement of the patent owner and accompanying information submitted pursuant to [37 C.F.R.] § 1.501(a)(2) which is relied upon in the detailed explanation, the request must explain how that statement is being used to determine the proper meaning of a patent claim in connection with the prior art applied to that claim and how each relevant claim is being interpreted. If appropriate, the party requesting reexamination may also point out how claims distinguish over cited prior art.
>
> (3) A copy of every patent or printed publication relied upon or referred to in paragraph (b) (1) and (2) of this section accompanied by an English language translation of all the necessary and pertinent parts of any non-English language patent or printed publication.
>
> (4) A copy of the entire patent including the front face, drawings, and specification/claims (in double column format) for which reexamination is requested, and a copy of any disclaimer, certificate of correction, or reexamination certificate issued in the patent. All copies must have each page plainly written on only one side of a sheet of paper.
>
> (5) A certification that a copy of the request filed by a person other than the patent owner has been served in its entirety on the patent owner at the address as provided for in [37 C.F.R.] § 1.33(c). The name and address of the party served must be indicated. If service was not possible, a duplicate copy must be supplied to the Office.
>
> (6) A certification by the third party requester that the statutory estoppel provisions of 35 U.S.C. [§] 315(e)(1) or 35 U.S.C. [§] 325(e)(1) do not prohibit the requester from filing the *ex parte* reexamination request.

TABLE OF CONTENTS

LISTING OF CLAIMS

Claim 1	
[1.a]	A semiconductor structure, comprising:
[1.b]	a substrate;
[1.c]	a first dielectric layer disposed on the substrate;
[1.d]	at least two metal gates disposed in the first dielectric layer;
[1.e]	a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface;
[1.f]	a source/drain region (S/D region) disposed between two metal gates;
[1.g]	a plurality of first contacts disposed in the first dielectric layer that are electrically connected to parts of the S/D region;
[1.h]	a plurality of second contacts disposed in the first dielectric layer that are electrically connected to one of the metal gates, wherein at least one of the first contacts directly connects at least one of the second contacts; and
[1.i]	a hard mask disposed on one of the metal gates, wherein the top surface of the hard mask and the top surface of the first dielectric layer are on the same level.

Claim 2
The semiconductor device of claim 1, further comprising a second dielectric layer disposed on the first dielectric layer.
Claim 3
The semiconductor device of claim 2, further comprising an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface.
Claim 4
The semiconductor device of claim 2, wherein the first contacts disposed in the first dielectric layer and in the second dielectric layer and each first contact is a monolithically formed structure.
Claim 5
The semiconductor device of claim 2, wherein the second contacts disposed in the first dielectric layer and in the second dielectric layer and each second contact is a monolithically formed structure.
Claim 6
The semiconductor device of claim 1, further comprising at least one fin structure disposed on the substrate.
Claim 7
The semiconductor device of claim 1, further comprising a salicide layer disposed between each S/D region and each first contact.

Claim 8
The semiconductor device of claim 3, further comprising a plurality of third contacts disposed on parts of the first contacts and on parts of the second contacts, wherein each third contact is a monolithically formed structure.
Claim 9
The semiconductor device of claim 8, wherein each third contact comprises a via hole structure and a trace structure, wherein the via hole structure and the trace structure comprise the same material and contact each other directly.

TABLE OF EXHIBITS

Exhibit	Description
Challenged Patent & Prosecution History	
Ex-01	U.S. Patent No. 9,147,747 B2 to Hung et al. ("'747 Patent").
Ex-02	Prosecution History of the '747 Patent ("Prosecution History").
Declarations	
Ex-03	Declaration of Dr. Jacob Baker
Ex-04	Curriculum Vitae of Dr. Jacob Baker
Prior Art in Proposed Rejections	
PA-01	U.S. Patent No. 9,461,143 ("Pethe")
PA-02	U.S. Patent No. 8,906,754 ("Pham")
PA-03	U.S. Patent App. Pub. No. 2013/0161707 ("Huang")
PA-04	U.S. Patent App. Pub. No. 2006/0223302 ("Chang")
PA-05	U.S. Patent No. 8,741,723 ("Chi")
PA-06	U.S. Patent No. 8,803,245 ("Sell")
PA-07	U.S. Patent No. 8,895,389 ("Hong")

Exhibit	Description
Additional Evidence	
Ex-05	International Patent Application PCT/US2011/066989 ("Golonzka")
Ex-06	CN 2013 1 0006390 ("HongCN") and Certified Translation of Hong with Certification of Translation
Ex-07	D. Neamen, *Semiconductor Physics and Devices – Basic Principles*, 4th Ed. (2011)
Ex-08	U.S. Patent No. 8,258,057 ("Kuhn")
Ex-09	Wolf, Stanley. *Silicon Processing for the VLSI Era: Deep-Submicron Process Technology*. Lattice Press, 2002 ("Wolf")
Ex-10	May, Gary S., and Simon M. Sze. *Fundamentals of Semiconductor Fabrication*. John Wiley & Sons, 2004 ("May")
Ex-11	U.S. Patent App. Pub. No. 2012/0252180 ("Tomimatsu")
Ex-12	U.S. Patent App. Pub. 2008/0142975 ("Ning")
Ex-13	U.S. Patent App. Pub. 2013/0154022 ("Chung")
Ex-14	U.S. Patent App. Pub. 2014/0048888 ("Chen'888")
Ex-15	Xiao, H. (2012). *Introduction to Semiconductor Manufacturing Technology* (2nd ed.). Prentice Hall ("Xiao")
Ex-16	U.S. Patent No. 8,835,245 ("Baars")
Ex-17	*RESERVED*

Exhibit	Description
Ex-18	Sze, S.M. *Physics of Semiconductor Devices*. 2nd ed., John Wiley & Sons, 1981 ("Sze")
Ex-19	U.S. Patent App. Pub. No. 2009/0155991 ("Lee")
Ex-20	U.S. Patent App. Pub. No. 2009/0014796 ("Liaw")
Ex-21	Banerjee, G. and R. Rhoades, Chemical Mechanical Planarization, ECS Trans., 13 (4) 1-19 (2008)
Ex-22	U.S. Patent No. 5,536,962 ("Pfiester")
Ex-23	U.S. Patent No. 8,928,048 ("Xie")
Ex-24	U.S. Patent App. Pub. 2009/0236669 ("Chen'669")
Ex-25	*Taiwan Semiconductor Manufacturing Company Limited et al v. Marlin Semiconductor Limited*, Inter Partes Review IPR2025-00865, Paper 1 (Petition), April 17, 2025
Ex-26	*Taiwan Semiconductor Manufacturing Company Limited et al v. Marlin Semiconductor Limited*, Inter Partes Review IPR2025-00865, Paper 8 (Patent Owner's Preliminary Response), August 15, 2025
Ex-27	U.S. Patent No. 8,617,986 ("Liang")
Ex-28	U.S. Patent No. 8,247,285 ("Lin")
Ex-29	U.S. Patent App. Pub. No. 2008/0121932 ("Ranade")
Ex-30	U.S. Patent No. 6,413,802 ("Hu")

Exhibit	Description
Ex-31	B. Doyle et al., *Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout*, Digest of the 2003 Symposium on VLSI Technology (2003) ("Doyle")
Ex-32	U.S. Patent App. Pub. No. 2010/0148217 ("Simonelli")
Ex-33	U.S. Patent No. 7,518,196 ("Chau")
Ex-34	U.S. Patent No. 8,623,728 ("Chang")
Ex-35	M.-H. Chi, *Challenges in Manufacturing FinFET at 20nm Node and Beyond*, Technology Development (2012)
Ex-36	U.S. Patent No. 8,455,314 ("Griebenow")
Ex-37	*Foreign-Fabricated Semiconductor Devices, Products Containing the Same, and Components Thereof*, Inv. No. 337-TA-1443, International Trade Commission, Complainants' Initial *Markman* Brief, August 21, 2025

I. BACKGROUND OF THE TECHNOLOGY

The '747 patent relates to a semiconductor manufacturing process and resulting semiconductor structure. Ex-01, Abstract, 1:7-11.

A. Field-Effect-Transistors (FETs)

The field-effect transistor (FET) has been the foundational device for very-large-scale integrated circuits (ICs) for decades. Ex-18, 431. FETs (e.g., MOSFETs), function essentially as a switch controlled by voltage applied to a "gate" (G) between "source" (S) and "drain" (D) regions.

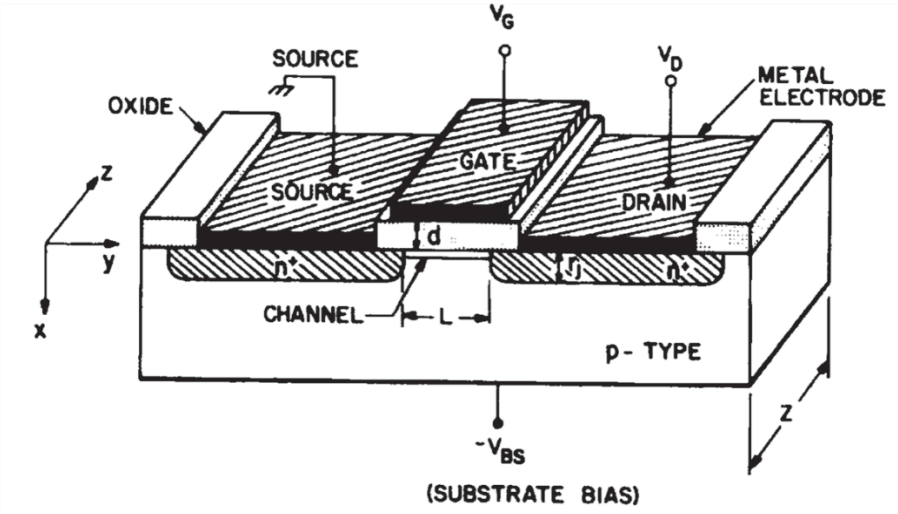


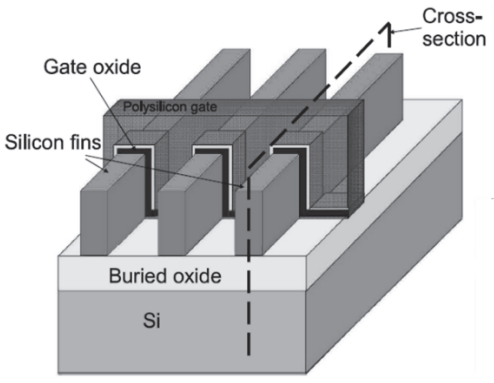
Fig. 3 Schematic diagram of a MOSFET. (After Kahng and Atalla, Ref. 4.)

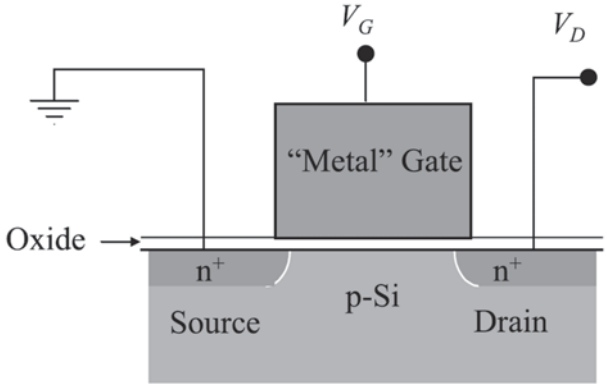
Ex-18, 433-34, FIGs. 3, 6; Ex-03, ¶¶27-29.

As shown above, the channel is disposed below the gate, and the source and drain semiconductor regions are disposed on each side of the gate. When the FET is turned on, current flows between the source and drain regions through the "channel" formed under the gate of the FET. Ex-18 (Sze), 433-34, 438, FIGs. 3, 6.

The element that provides the source of electrical carriers that will flow along the channel during operation is generally termed the "source," and the element that acts as a sink or drain for the electrical carriers to flow to during operation is generally termed the "drain." A source or drain element is commonly referred to as a "source/drain" because whether the element operates as a "source" of electrical carriers or a "drain" for electrical carriers in a FET is interchangeable depending on the voltage applied to the element. A POSITA would have understood that source/drain regions are conventionally formed by diffusion of dopants, and in such instances, were commonly referred to as diffusion regions. Ex-07 (Neamen), xxiii, FIG. 0.5; Ex-09 (Wolf), 3, 6.)

Two types of FETs were conventionally known at the time of the '747 patent's filing: (1) planar FETs (e.g., planar MOSFET); and (2) non-planar three-dimensional (3D) FETs (e.g., tri-gate transistor, FinFET, both examples of non-planar MOSFETs).





Ex-15, Figure 9.41(a) (FinFET) | **Ex-15, Figure 3.20 (part) (planar MOSFET)**

Ex-15, 351, 72-74; Ex-03, ¶30.

Inter-layer dielectric layers (ILDs) were known IC structure features typically disposed on the wafer/substrate between features (e.g., metal gates) in the structure. Ex-03, ¶¶31-32; *e.g.*, Ex-15 (Xiao), 370-71.

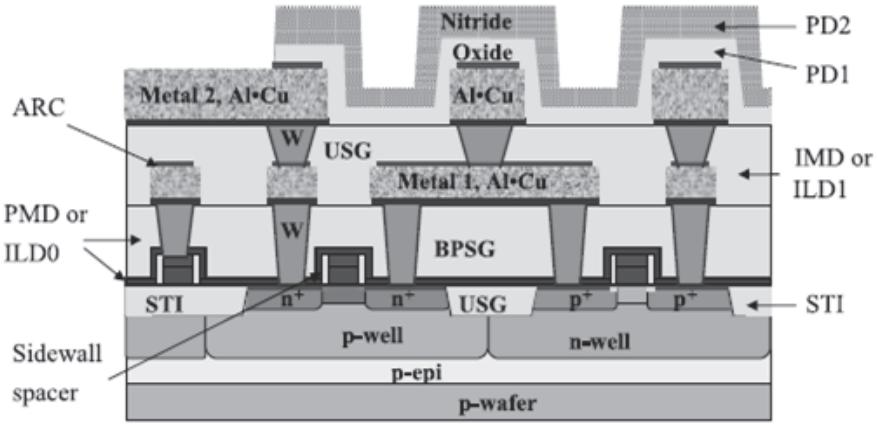


Figure 10.2 Applications of dielectric thin film in a CMOS circuit with Al–Cu interconnection.

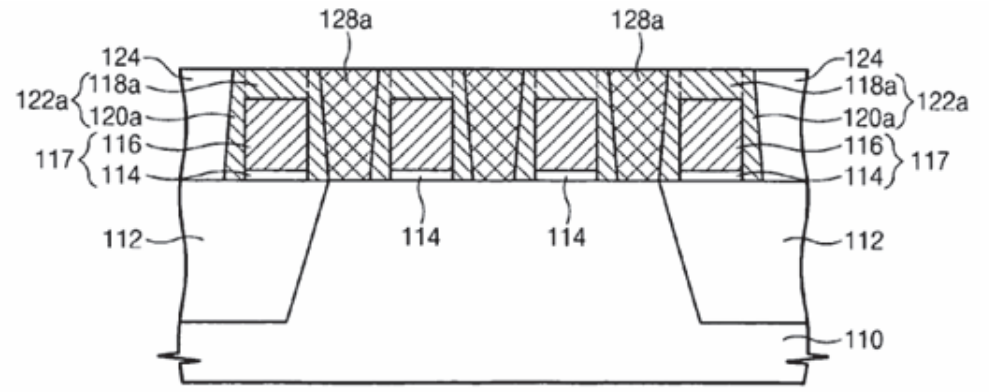
Ex-15 (Xiao), 371, FIG. 10.2 (ILD filling space between features); PA-01 (Pethe), FIG. 2C, 5:7-10 (ILDs 270).

B. Self-Aligned/Shared Contacts

In ICs, transistors are interconnected in various arrangements through contact plugs and interconnection structures. Ex-01 ('747 Patent), 1:17-21. With "the continuous miniaturization of…IC[s], the line width of interconnections and the feature sizes of semiconductor devices…continuously shrunk." *Id.*, 1:14-17. Making electrical contacts to such miniaturized devices was a known challenge. Ex-

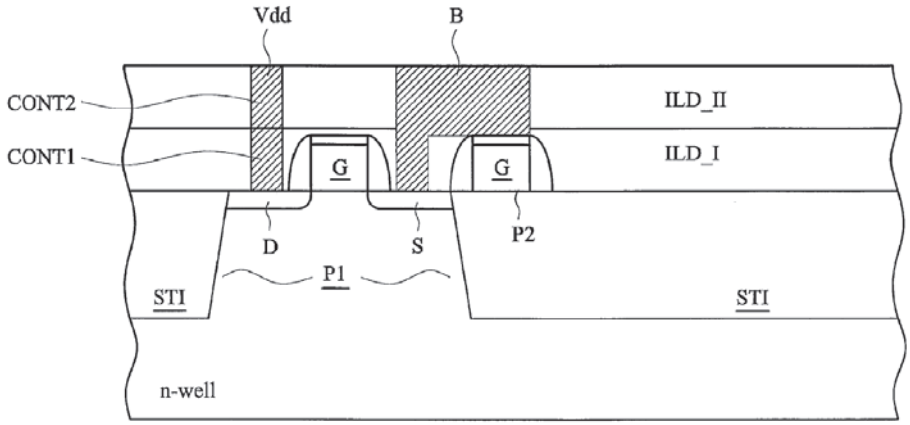
13, 1:36-65. A known technique to form such contacts was self-aligned contacts (SAC). *Id.*, 1:66-2:13, 2:55-56; Ex-19 (Lee), ¶¶5, 64-68, FIGs. 3D-3F (SAC 128a); Ex-03, ¶¶33-34. In SACs, "after forming an opening that simultaneously exposes gates of a region requiring a contact plug and a semiconductor substrate between the gates, a conductive layer is deposited to fill the opening," and the conductive layer (e.g., metal) is then planarized. Ex-19, ¶6; Ex-03, ¶¶33-34.

Implementation of SACs was known to include the use of cap layers, (hard masks) to cover and thus protect the gate during contact opening formation to features such as the source/drain. Ex-19, ¶7; Ex-03, ¶¶35-37.



Ex-19 (Lee), FIG. 3F.

For some IC structures, *e.g.*, static random-access memory (SRAM), it was known to implement shared contacts, which are single contacts connecting together two transistor features, such as a source/drain and a gate. Ex-20 (Liaw), ¶¶3, 42-43, FIG. 1 (contact 10), FIG. 8C (below, contact B); Ex-03, ¶38.



Ex-20 (Liaw), FIG. 8C.

Such shared contacts (*e.g.*, Ex-20, FIGs. 1, 8C) were a known way to "mak[e] electrical connection…where high device density is desired…, thus, reducing the [IC] die area and enhancing device reliability." Ex-20 (Liaw), ¶3; Ex-22 (Pfiester), 5:59-6:18, FIG. 4 (shared contact 82). Ex-03, ¶37.

C. Planarization

Semiconductor device contacting was known to include a planarization step, which was known to include etching and/or chemical mechanical planarization (CMP) for planarizing the surface of semiconductor structures. Ex-15 (Xiao), 511-514; Ex-21 (Banerjee), 1-2 ("CMP became a mainstream process at and below the 0.35um technology node" in "1995"). CMP is a removal process employing chemical and mechanical means to planarize the surface of a semiconductor structure/wafer. Planarizing etchback processes for recessing transistor

gates/spacers in ILD was also known. Ex-23 (Xie), 4:37-60, 7:4-53, FIGs. 1A, 2A-2C; Ex-24 (Chen'669), 4:37-5:6, 7:48-8:37, FIGs. 1B, 2A-2C. Ex-03, ¶¶38-41.

D. Metal Interconnect (BEOL)

After individual transistors are fabricated and contacted, e.g., through a SAC, for example, BEOL (Back-End-of-Line) processes are used to interconnect the transistors to form an IC. Such interconnection has conventionally included "dual-damascene" processing where metal lines and vias are formed simultaneously to connect to a lower contact level. Ex-15 (Xiao), 19, 345-49, 453, 464, 517-18; Ex-09 (Wolf), 696-98; Ex-10 (May), 55-56. This process involves depositing metal in an etched geometry representing the shape of the metal lines and vias, and then removing the excess metal using CMP. *Id.*

In order to interconnect the up to billions of transistors on modern integrated circuits (ICs), it became necessary to provide multiple metal layers. Ex-15 (Xiao), 570; Ex-09 (Wolf), 559. To do so, "this dual damascene process is repeated multiple times, depending on how many metal layers there are" (i.e., M2/V1, M3/V2, etc.). Ex-15 (Xiao), 19, 345-49, 570; Ex-09 (Wolf), 696-98; Ex-12 (Ning), ¶¶37-40, FIG. 3A; Ex-03, ¶¶42-44.

II. OVERVIEW OF THE '747 PATENT

A. '747 Patent Specification

The '747 patent purports to address drawbacks of prior semiconductor manufacturing process/structures where a barrier layer is formed between upper and lower contact structures formed in different steps. Ex-01, Abstract, 1:7-41; *id.*, 1:45-5:66-6:37, FIG. 9.

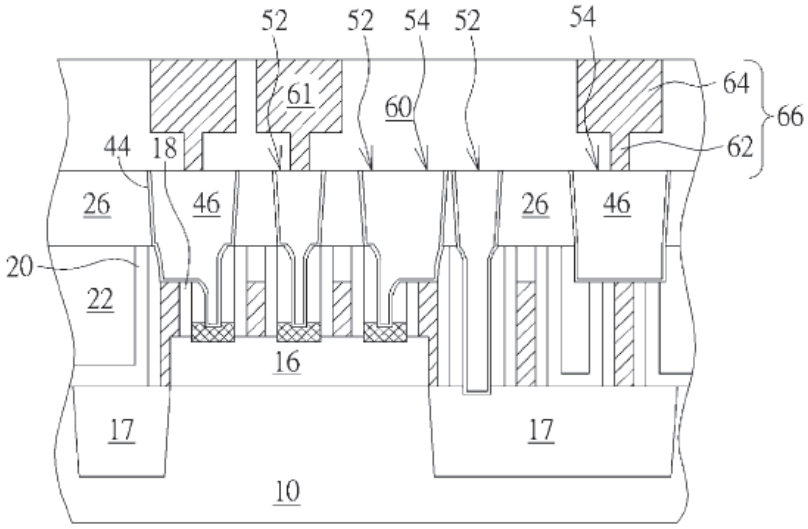


FIG. 9

Ex-03, ¶¶45-50.

B. Prosecution History

The '747 patent issued following a series of rejections/amendments, which added the now claimed truncated spacer, contacts, metal gate, and S/D features. Ex-02, 93-110, 134-159; Ex-03, ¶¶51-61. None of the references that form the basis for the SNQs here were considered during prosecution.

C. Prior *Inter Partes* Review for the '747 Patent

Requester filed a petition requesting *inter partes* review of the '747 patent on April 17, 2025, on the basis of similar prior art and arguments contained in this request. On September 3, 2025, the Acting Director issued a decision exercising discretion to deny institution in view of the co-pending ITC matter. A request for Director Review was denied on November 5, 2025. As a result, the Office did not consider the merits of any of the prior art at issue in the IPR.

D. Claim Construction

Because the present Request relates to an unexpired patent, the claims of the '747 Patent should be construed under their broadest reasonable interpretation ("BRI") in view of the claim language and specification. *In re Suitco Surface, Inc.*, 603 F.3d 1255, 1259 (Fed. Cir. 2010). Additionally, "[d]uring patent examination, the pending claims must be 'given their broadest reasonable interpretation consistent with the specification.'" MPEP § 2111; *see also* MPEP § 2258. The standard of claim interpretation in reexamination is different than that used by the courts in patent litigation. MPEP § 2258; *In re Rambus, Inc.*, 753 F.3d 1253, 1255 (Fed. Cir. 2014) ("Claims are generally given their 'broadest reasonable interpretation' consistent with the specification during reexamination."); *SkyHawke Techs., LLC v. Deca Int'l Corp.*, 828 F.3d 1373, 1376 (Fed. Cir. 2016) (noting that district courts apply the "standard of claim construction as explored in *Phillips v. AWH Corp.*"

rather than the "broadest reasonable construction"). Therefore, any claim interpretations submitted or implied herein for the purpose of this reexamination do not necessarily correspond to the appropriate construction under the legal standards mandated in litigation.[1] MPEP § 2686.04; *see also In re Zletz*, 893 F.2d 319, 322 (Fed. Cir. 1989). Given how closely the prior art maps to the claims, Requester submits that no construction is required any claim terms because the claims would be unpatentable under any reasonable construction of the terms. Accordingly, the analysis discussed below applies the BRI.

[1] Requester reserves all rights and defenses available including, without limitation, defenses as to invalidity, unenforceability, and non-infringement regarding the '747 patent. Further, because the claim interpretation standard used by courts in patent litigation is different from the appropriate standard for this reexamination, any claim constructions submitted or implied herein for the purposes of this reexamination are not binding upon Requester in any litigation related to the '747 patent. Specifically, any interpretation or construction of the claims presented herein or in Dr. Baker's declaration for reexamination, either implicitly or explicitly, should not be viewed as constituting, in whole or in part, the Requester's own interpretation or construction of such claims.

1. "A Truncated Top Surface"

Before being dropped from the pending ITC proceeding (*see infra* Section VIII.C), three interpretations of the term "truncated top surface" were advanced under the *Phillips* standard. While the broadest reasonable interpretation (BRI) standard applies in these proceedings, Requester demonstrates below how, under any of the three interpretations, the prior art invalidates the challenged claims.

Interpretation 1	"Truncated" is planar. "A truncated top surface" is a planar top surface, where the words "a truncated top surface" must be construed together.
Interpretation 2	"Truncated" is to have made shorter by removing a part. "A truncated top surface" is a top surface of a feature (e.g. spacer) that has been "truncated."
Interpretation 3	"A truncated top surface" is a top surface that has been made shorter by removing a part during a planarization process.

2. "Directly Connects"

The term "at least one of the first contacts directly connects at least one of the second contacts" in Claim 1 was also considered in the ITC proceeding (*see infra* Section VIII.C). An interpretation of the term has been advanced under the *Phillips* standard. While the broadest reasonable interpretation (BRI) standard applies in these proceedings, Requester demonstrates below how, under this interpretation, the prior art invalidates the challenged claims.

Interpretation 4	At least one of the first contacts connects with at least one of the second contacts with no intervening layer or material therebetween.

E. Level of Ordinary Skill

A person of ordinary skill in the art ("POSITA") would have had a master's degree in electrical engineering, physics, chemistry, materials science, or a related field and three years of work experience in semiconductor manufacturing, such as for example, integrated circuit device (or transistor) design and/or manufacturing. Ex-03, ¶23.[2] Additional relevant education could substitute for professional experience, and significant work experience or training could substitute for less formal education. *Id.*

III. IDENTIFICATION OF PRIOR ART

Requester respectfully requests reexamination of claims 1-9 of the '747 patent in view of the following prior art references:

PA-1	U.S. Patent No. 9,461,143 ("Pethe")
PA-2	U.S. Patent No. 8,906,754 ("Pham")
PA-3	U.S. Patent App. Pub. No. 2013/0161707 ("Huang")
PA-4	U.S. Patent App. Pub. No. 2006/0223302 ("Chang")
PA-5	U.S. Patent No. 8,741,723 ("Chi")
PA-06	U.S. Patent No. 8,803,245 ("Sell")
PA-07	U.S. Patent No. 8,895,389 ("Hong")

[2] Requester submits the declaration of Dr. Jacob Baker (Ex-03), an expert in the field of the '747 patent. (Ex-03, ¶¶5-20; Ex-04.)

A copy of each of the above-listed references is attached to this request pursuant to 37 C.F.R. § 1.510(b)(3). A copy of the '747 patent is also attached to this request as Exhibit Ex-01, pursuant to 37 C.F.R. § 1.510(b)(4).

Each of the cited references qualifies as prior art.

Reference	**Filed**	**Published**	**AIA Prior Art Qualification**
Pethe	September 19, 2012	October 4, 2016	§102(a)(2)
Pham	March 15, 2013	December 9, 2014	§102(a)(2)
Huang	December 22, 2011	June 27, 2013	§102(a)(2)
Chang	March 31, 2005	October 5, 2006	§§102(a)(1), (a)(2)
Chi	April 25, 2012	June 3, 2014	§102(a)(2)
Sell	June 30, 2008	August 12, 2014	§102(a)(2)
Hong	January 8, 2013 (CN)	July 10, 2014	§102(a)(2)[3]

[3] Hong (PA-07) claims priority to Chinese Application No. CN201310006390, which was filed January 8, 2013. Accordingly, Hong was effectively filed on January 8, 2013, prior to the earliest effective filing date of the '747 patent (May 2, 2013), and is thus prior art under 35 U.S.C. § 102(a)(2). Exhibit PA-07 (Hong) includes a copy of US8,895,389, while Exhibit Ex-06 (HongCN) includes a copy of CN20131006390, a certified English translation, and a certification of translation.

A. Pethe (U.S. Patent No. 9,461,143) (PA-01)

Pethe is prior art under AIA §102(a)(2). Because Pethe is in the same field (MOSFETs) and reasonably pertinent to a problem the '747 patent purports to address (e.g., MOSFET fabrication), Pethe is analogous art. PA-01 (Pethe), 2:50-3:10, 7:9-11:42, 12:22-13:12, 14:4-11; Ex-01 ('747 Patent), 1:9-2:9, 2:39-42, 5:31-6:37; Ex-03, ¶¶78-86.

Pethe discloses semiconductor devices, including MOS transistors (MOSFETs) having gate contact structures disposed over active portions of gates and methods of forming such structures. PA-01, 2:50-52, 2:50-3:10, 7:9-11:42, 12:22-13:12, 14:4-11. Pethe discloses a semiconductor structure as shown in FIG. 5B, the fabrication of which is shown collectively in FIGs. 5A-5B. PA-01, 2:32-36, 12:32-33.

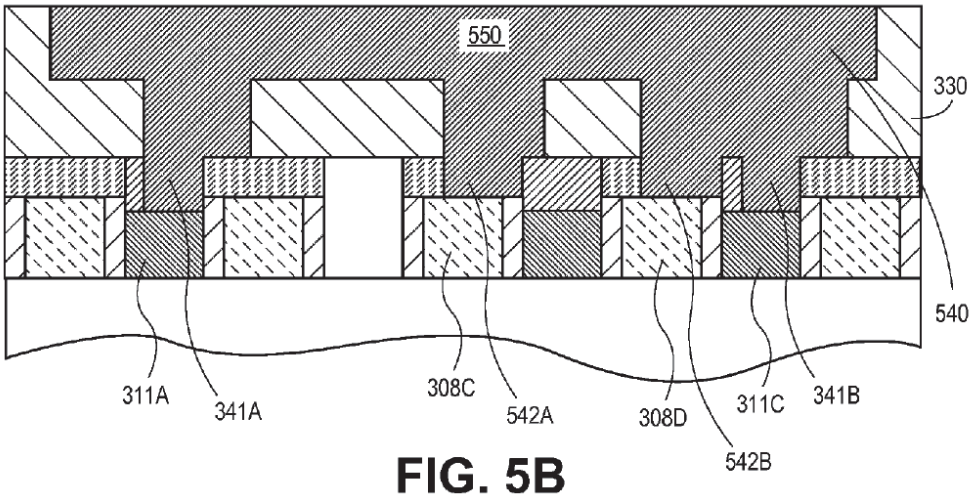


FIG. 5B

PA-01, FIG. 5B.

Pethe explains that in the FIG. 5 Embodiment "the spacer may be **recessed** to be essentially **planar** with the gate structures." PA-01, 12:22-26, 12:48-53 ("**in contrast to the structure 300** described in associated with FIG. 3A, **the spacers 520 have been recessed** to approximately the same height as the gate stack structures 308A-308E").

Pethe's Figure 5B structure also includes a cap layer 522 (the same as the cap layer 322 but wider because of the recessed spacers 520). Pethe's Figure 5B structure also includes gate contact vias 542 and metal portion 550 (the same as the gate contact vias 342 and the metal portion 350 but extending deeper because of the recessed spacers 520).

The Figure 5 embodiment starting structure 500 is "provided following trench contact (TCN) formation." PA-01, 7:15-16, 12:32-33. Pethe's-Figure-5-Embodiment also relies on earlier disclosures from within Pethe (e.g. disclosures relating to FIG. 3). *Id.*, 12:37-48 (referring to gate stack structures 308A-308E, substrate 302, gate dielectric layer and gate electrode (in connection with Figure 2), and trench contacts 310A-310C, coupled with similar features associated with Figure 5A (structure 500, spacers 520, cap layer 522); *see also* Ex-03, ¶¶78-86.

B. Pham (U.S. Patent No. 8,906,754) (PA-02)

Pham is prior art under AIA §102(a)(2). Because Pham is in the same field (MOS transistors), as with Pethe and Chang, and is reasonably pertinent to a problem

the ’747 patent purports to address (e.g., MOSFET fabrication), Pham is analogous art. PA-02 (Pham), Abstract, 1:54-2:20, 4:37-5:41; Ex-01 (’747 Patent), 1:9-13, 5:66-6:37; PA-01 (Pethe), 12:32-13:12, 13:63-14:11, 9:29-10:36, 11:23-31; PA-04 (Chang), ¶¶27-35, 46-49, 52, 89-92, 107, 111-114; Ex-03, ¶¶87-92.

Pham discloses methods for forming a semiconductor device that includes a gate structure position above a substrate with a spacer structure positioned adjacent the gate structure. PA-02 (Pham), Abstract. *See also id.*, 1:54-2:20, 4:37-54 (“[g]enerally, the present disclosure is directed to various methods of forming a semiconductor device with a protected gate cap layer, and the resulting semiconductor device”), 4:55-5:41. Pham discloses that sidewall spacers (e.g., 118) are formed adjacent dummy gate structures, as shown in FIG. 2A and gate structures 111 are formed between the spacers using a replacement gate manufacturing technique, such that final gate structures 111 are formed following a CMP, which exposes the upper surface of the gate structures (and results in spacers with a planar top surface). *Id.*, 7:48-8:8; *see also id.*, 6:51-7:5, 7:20-8:37, FIGs. 2A-2C. Accordingly, Pham discloses spacers 118 (118A) that are made shorter by removing a part (including during a planarization process) that also results in a planar top surface.

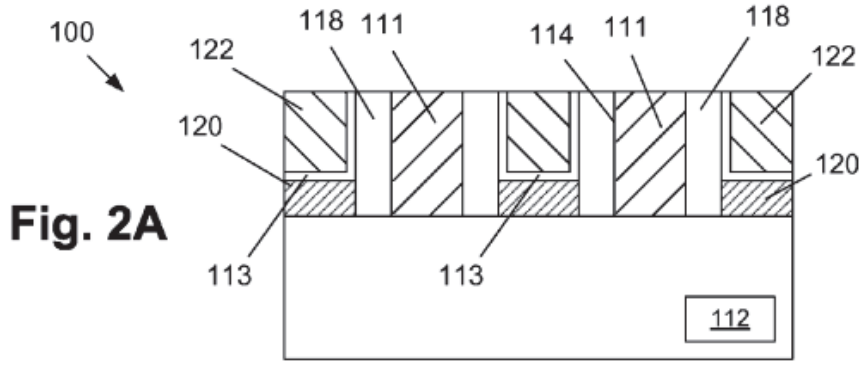


Fig. 2A

Id., FIG. 2A. For example, Pham discloses that time recess etching processes are performed that "remove portions of the sidewall spacer 118…to define recessed sidewall spacers 118A" as shown in FIG. 2C (below). *Id.*, 8:9-37.

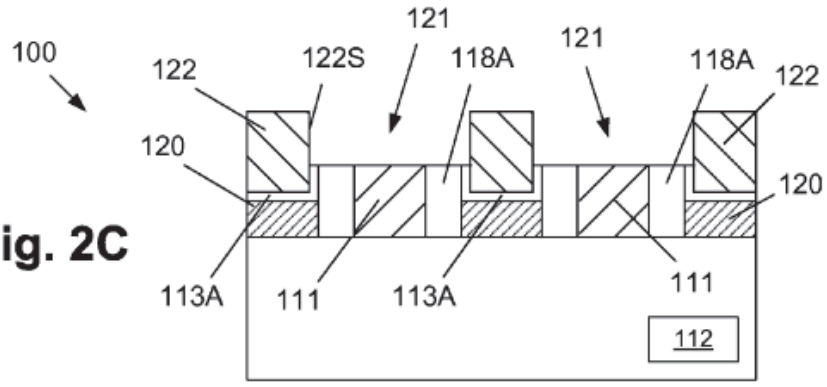


Fig. 2C

PA-02 (Pham), FIG. 2C.

C. Huang (U.S. Patent Pub. 2013/0161707) (PA-03)

Huang is prior art under AIA §102(a)(1). Because Huang is in the same field (planar or Field-Effect MOS transistors with metal layers to contacts), as with Pethe and Chang, and is reasonably pertinent to a problem the '747 patent purports to address (e.g., MOSFET fabrication), Huang is analogous art. PA-03 (Huang), ¶¶2-

10, 14, 17; Ex-01 ('747 Patent), 1:9-13, 5:66-6:37; PA-01 (Pethe), 8:24-51, 9:29-43, 11:23-42; PA-04 (Chang), ¶¶1, 17-44; Ex-03, ¶¶93.

Huang discloses methods for forming a semiconductor memory device comprising FETs. PA-03, ¶¶3-5, 7-8. Huang teaches the use of dual-damascene processing to provide M1 lines and M0 vias in forming the device. PA-03, ¶17, FIG. 8A. Huang describes M1 layer's metal lines 74 and M0 vias 72 "for connecting to contact plugs 60 and 62," shown below.

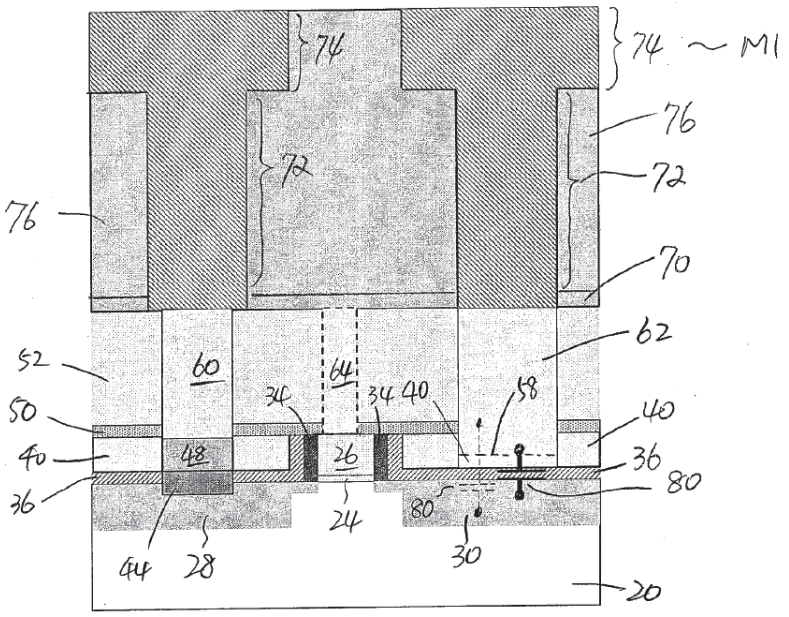


Fig. 8A

Ex-03, ¶93; PA-03, ¶17. "M0 vias 72 and metal lines 74 may be formed using a dual-damascene process, and hence no noticeable interfaces being formed between M0 vias 72 and respective overlying metal lines 74." *Id*.

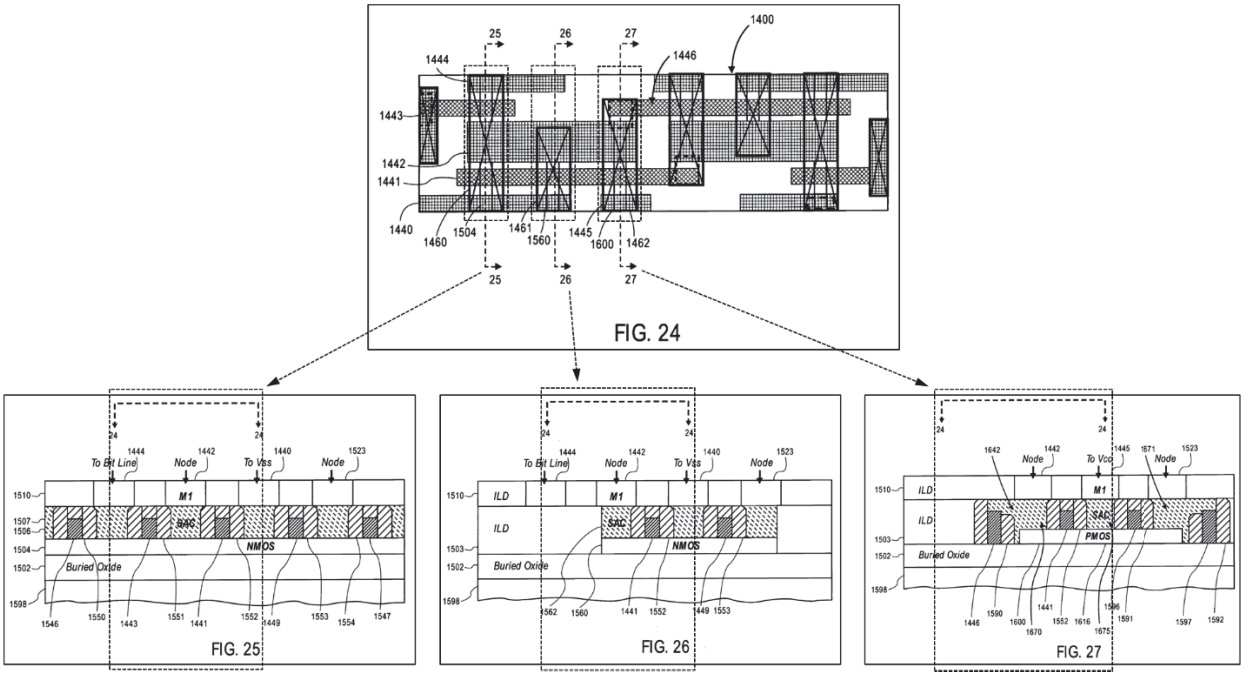
D. Chang (U.S. Patent Pub. 2006/0223302) (PA-04)

Chang is prior art under AIA §102(a)(1). Because Chang is in the same field (MOSFETs) and reasonably pertinent to a problem the '747 patent purports to address (e.g., MOSFET fabrication), Chang is analogous art. PA-04 (Chang), ¶¶27-35, 46-49, 52, 89-92, 107, 111-114; Ex-01 ('747 Patent), 1:9-2:9, 2:39-42, 5:31-6:37; Ex-03, ¶¶94-100.

Chang teaches an "SRAM containing transistor structures with gate-protected self-aligned contacts" in Figures 24-27. PA-04, ¶107. The transistor structures in Chang's SRAM include MOSFETs. PA-04, ¶1, 27-35, 46-49, 52, 89-92, 107-114. The SRAM of Figures 24-27 is disclosed in the context of Chang's "self-aligned contacts" with a "gate-protection option," which Chang explains "is described with respect to FIGS. 17-27." PA-04, ¶52; Ex-03, ¶¶94-100.[4] Specifically, "FIGS. 17 through 23 show wafer cross sections that illustrate operations in connection with the gate-protect option with respect to forming self-aligned contacts" (PA-04, ¶89) and "FIG. 24 is a top view of a layout 1400 of an SRAM containing transistor structures with gate-protected self-aligned contacts…cross sections of the SRAM layout 1400 are shown in FIGS. 25, 26, and 27" (*id*., ¶107).

[4] Chang discloses an alternative "no gate-protect option … in reference to FIGS. 6 through 16." (PA-04, ¶51.)

A POSITA would have thus understood that the teachings of Figures 17-23 are methods and operations for the SRAM of Figures 24-27. Ex-03, ¶96. Specifically, Figures 17-23 illustrate forming the self-aligned contacts, and Figures 24-27 show an SRAM with those contacts. More specifically, Figures 25-27 show three cross-sections of the SRAM structure in Figure 24, as depicted below:



PA-04, FIGs. 24-27.

E. Chi (U.S. Patent 8,741,723) (PA-05)

Chi is prior art under AIA §102(a)(2). Because Chi is in the same field (semiconductor MOS devices), as with Chang, and is reasonably pertinent to a problem the '747 patent purports to address (e.g., MOSFET fabrication), Chi is analogous art. PA-05 (Chi), Abstract, 3:48-57, 5:42-56; Ex-01, 5:31-6:37; PA-04 (Chang), ¶¶93-94, 97, 108-13; Ex-03, ¶101.

Chi discloses a method for forming gate structures for transistors above a semiconductor substrate and contacts on a semiconductor device. PA-05 (Chi), Abstract, 3:48-57. Chi's processes are applicable to planar and non-planar devices, such as FinFETs. *Id.*, 5:42-52; *see also id.*, 5:53-56, FIGs. 1A-1D. Among other features, Chi describes the formation of conductive contact structures and metal silicide regions in the source/drain regions between transistors of a device. *Id.*, 6:26-35, FIG. 2A. The transistors each comprise a gate structure made of one or more conductive gate electrode layers 30B and a gate cap layer 31, and sidewall spacers 32. PA-05, 6:35-40, 11:7-14. Chi also discloses methods concerning gate-last techniques in connection with FIGs. 3A-3J. PA-05, 13:63-14:9, FIGs. 3A-3B. Chi explains "as shown in FIG. 3C one or more CMP processes are performed to remove portions of the layer of insulating material 70, the etch stop layer 34 and the gate cap layer. PA-05, 14:20-24. FIG. 3C below shows the results of such CMP process resulting in sidewall spacers 32 and etch stop layer 34 with a planar top surface. Thus, Chi discloses spacers and an etch stop layer that have been made shorter by removing a part (including during a planarization process). *See also* PA-05, 14:25-15:9, FIGs. 3C-3E, 15:41-16:60, FIG. 3J (below).

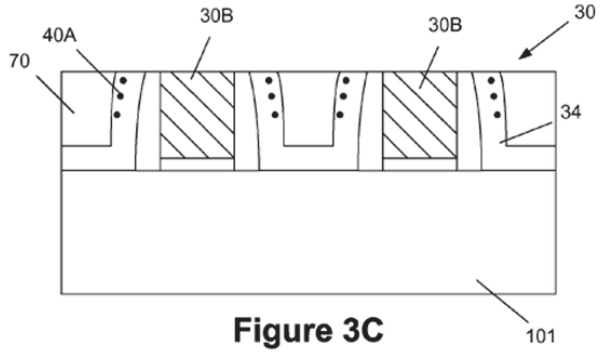


Figure 3C

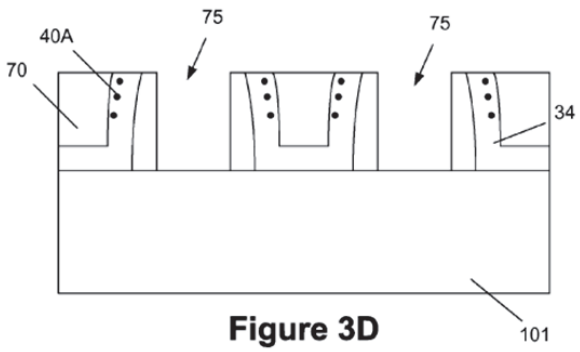


Figure 3D

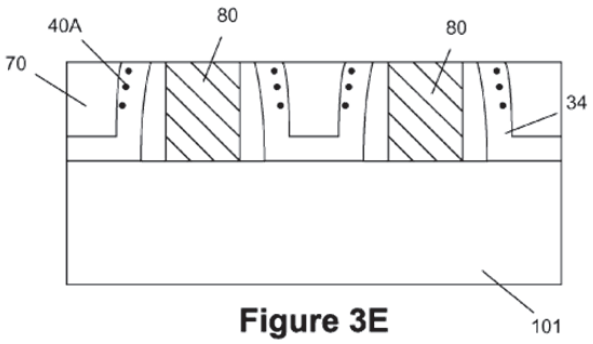


Figure 3E

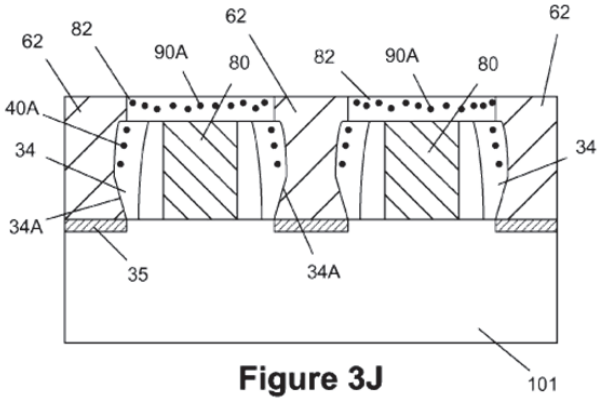


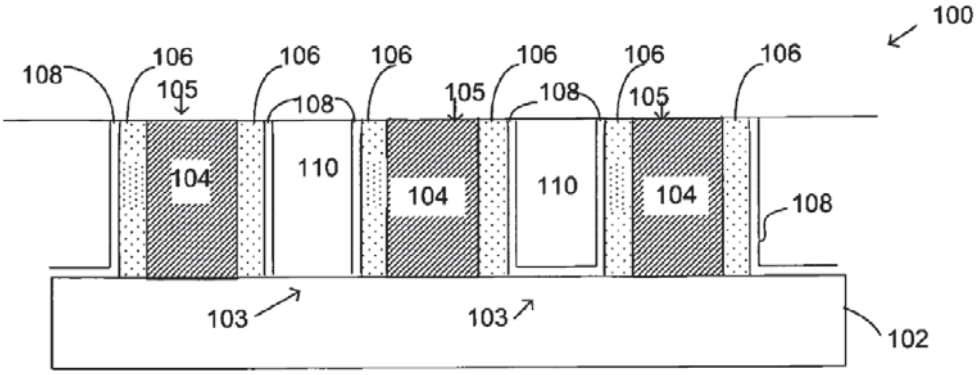
Figure 3J

Id., FIGs. 3C-3E, 3J.

F. Sell (U.S. Patent 8,803,245) (PA-06)

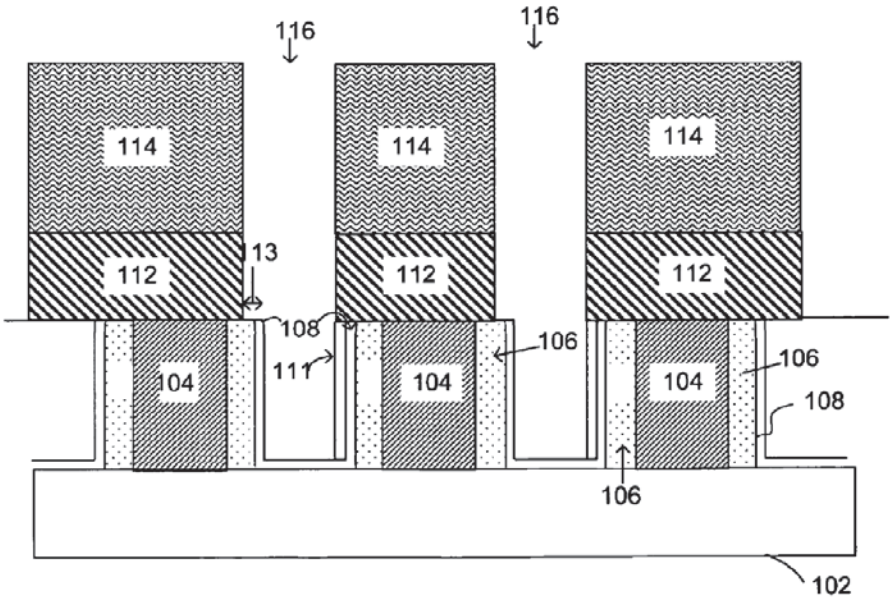
Sell is prior art under AIA §102(a)(2). Because Sell is in the same field (integrated circuit (IC) CMOS semiconductor devices), as with Pethe and Chang, and is reasonably pertinent to a problem the '747 patent purports to address (e.g., CMOS fabrication), Sell is analogous art. PA-06 (Sell), Abstract, 1:50-2:9, 2:10-22, 2:35-61, 3:31-43; Ex-01 ('747 Patent), 5:31-6:37; PA-01 (Pethe), 12:32-13:12, 13:63-14:11, 9:29-10:36, 11:23-31; PA-04 (Chang), ¶¶93-94, 97, 108-13; Ex-03, ¶¶102-103.

Sell discloses methods and associated structures of forming a microelectronic device, including "forming a structure comprising a first contact metal disposed on a source/drain contact of a substrate, and a second contact metal disposed on a top surface of the first contact metal, wherein the second contact metal is disposed within an IID disposed on a top surface of a metal gate disposed on the substrate." PA-06 (Sell), Abstract, 1:50-2:9, FIGs. 1a-1g.



PA-06, FIG. 1a.

Sell discloses that the "transistor structure 100 may further comprise a spacer material 106, that may be adjacent and in direct contact with the gate 104." *Id.*, 2:10-22. The spacer 106 has a planar top. *Id.*, FIG. 1a (above), FIG. 1b (below).



PA-06, FIG. 1b, 2:35-49. *See also*, *id.*, 2:50-61, 3:31-43 ("the first contact metal 120 may be planarized with a planarized top surface 121 of the gate 104, i.e., it may be polished by the polishing process 123 so that a top surface 122 of the first contact metal 120 may be planar with the planarized top surface 121 of the gate 104" and that "[t]he polishing process 123 additionally removes the depth 117 of the exposed portion 113 of the spacer material 106 that was due to the misregistration of the resist layer 114 (referring back to FIG. 1c)"). Ex-03, ¶¶102-103.

G. Hong (U.S. Patent 8,895,389) (PA-07)

Hong is prior art under AIA §102(a)(2). Because Hong is in the same field (semiconductor MOS devices), as with Chang, and is reasonably pertinent to a problem the '747 patent purports to address (e.g., MOSFET fabrication), Hong is analogous art. PA-07 (Hong), 2:4-10, 2:13-58, 8:53-9:27, 9:55-64, 10:46-67, 11:1-

9; Ex-06 (HongCN), Abstract, ¶¶8-17, 27; Ex-01, 5:31-6:37; PA-04 (Chang), ¶¶93-94, 97, 108-13; Ex-03, ¶104.

Hong discloses improved structures for electrically contacting semiconductor device features. PA-07 (Hong), Abstract, 2:13-58, 3:46-53 8:53-9:27, 10:46-67; *see also*, 2:4-10, 9:55-64, 11:1-9, FIGs. 3-7, 10; Ex-06 (HongCN), Abstract, ¶¶8-17, 27. Hong discloses a shared contact for FETs that includes contact 442 formed simultaneously between a metal gate 411 and source/drain region 402, and within a plurality of dielectric layers (e.g., layer 406 on layer 401). PA-07 (Hong), 8:53-9:27, 10:46-67, FIGs. 6-9; Ex-06 (HongCN), ¶¶14, 23. Hong discloses forming a first metal gate 411 and a second metal gate 421 and doped regions 402 (e.g., S/D regions of a transistor) on both sides of the first gate structures. PA-07, FIGs. 3, 7-9, 3:54-4:3, 4:26-45, 5:16-26. *See also* Ex-06 (HongCN), Abstract, FIGs. 5-9, claims 1-39, ¶¶8-17, 28-29, 36, 40, 44, 46-48, 51, 54-56, 58-69, 71-87.

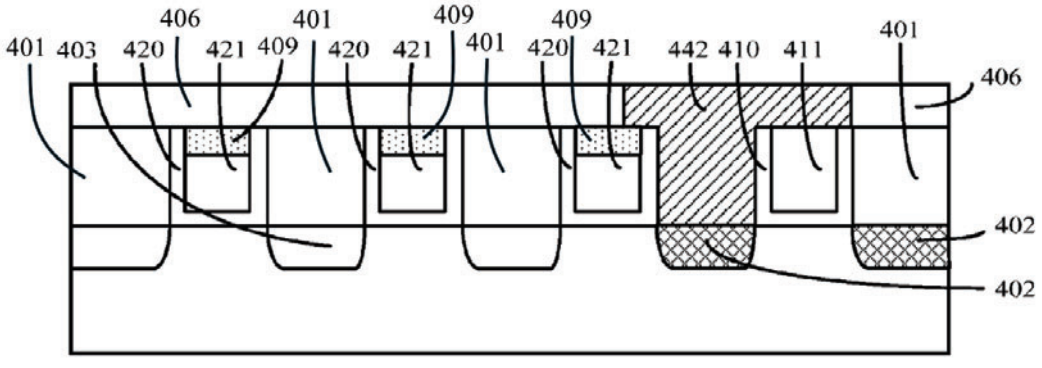


FIG. 7

PA-07 (Hong), FIG. 7 (additional annotations added); Ex-03, ¶104.

IV. IDENTIFICATION OF CLAIMS FOR REEXAMINATION AND PROPOSED REJECTIONS

Requestor respectfully requests reexamination and cancellation of claims 1-9 the '747 Patent.[5] A listing of claims, with limitations identified by reference number, appears after the Table of Contents and Table of Authorities.

As set forth in more detail below, Requestor proposes the following rejections of claims 1-9 of the '747 Patent:

Proposed Rejection	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A	1-8	102	Pethe
1B	1-8	103	Pethe
1C	1-8	103	Pethe, Pham
1D	7	103	Pethe, Sell
1E	8-9	103	Pethe, Huang
2A	1-2 and 6	102	Chang
2B	1-2 and 4-6	103	Chang
2C	1-7	103	Chang, Sell
2D	8-9	103	Chang, Sell, Huang
2E	1-7	103	Chang, Chi
2F	1-9	103	Chang, Huang
2G	4-5	103	Chang, Hong

[5] U.S. Patent No. 9,147,747 (Ex-01).

V. IDENTIFICATION OF SUBSTANTIAL NEW QUESTIONS OF PATENTABILITY (SNQS)

The '747 patent issued following a series of rejections/amendments, which added the now claimed truncated spacer, contacts, metal gate, and S/D features. Ex-02, 93-110, 134-44, 146-59, 169-71. None of the references that form the basis for the SNQs here were considered during prosecution.

More specifically, the '747 patent was filed on May 2, 2013. The Examiner issued an office action on September 23, 2014, rejecting all pending claims based on Chen'888 (Ex-14) alone or in combination with a Chung (Ex-13) (neither of which is at issue in this request). Ex-02, 75-78. The Applicant amended the independent claim to include "the spacer has a truncated top surface" limitation. *Id.*, 95, 104-09. The Examiner, however, again rejected all pending claims based on a combination of Chen'888 and Chen'669 (Ex-24) (teaching the truncated top surface), or further in view of Chung. *Id.*, 114-17.

The Applicant then amended independent claim 1 with the limitations "a plurality of first contacts. . .that are electrically connected to parts of the S/D region," "a plurality of second contacts disposed. . .that are electrically connected to one of the metal gate[s], wherein at least one of the first contacts *directly connects* at least one of the second contacts" (the "directly connects" limitation). Ex-02, 134-38, 141-44. The Examiner subsequently allowed the claims "since the prior art made of

record and considered pertinent to the applications' disclosure do not teach or suggest the claimed limitations." [6] *Id.*, 170. In short, the amendment adding a first contact that "directly connects" with a second contact was the limitation that led the Examiner to allow the '747 Patent.

The two primary references in this request disclose the sole "directly connects" limitation missing from the prior art before the Examiner, thereby raising substantial new questions of patentability (SNQs).

A. Pethe, Pham, Sell, and Huang Raise SNQs

Proposed rejections 1A, 1B, 1C, 1D, and 1E rely on Pethe. In ***Proposed Rejection 1A***, Pethe is used as an anticipation reference. Pethe teaches trench contact vias 341A, 341B (**plurality of first contacts**) are **disposed in a first dielectric layer** (inter-layer dielectric material of which region 323 is a part) and contacting source/drain regions of the device via trench contacts, e.g. 311C. PA-01, 12:54-67, FIG. 5B; Ex-03, ¶105. Pethe also teaches gate contact vias 542A, 542B that are **a plurality of second contacts**, the gate contact vias 542A, 542B disposed in Pethe's first dielectric layer (of which region 323 is a part) and are "to [connect]

[6] The examiner observed that the "spacer . . . [that] has a truncated top surface" limitation should not have been removed from claim 1. Ex-02, 149. The Applicant did not dispute the examiner's position and reinserted the limitation into the claims before allowance. *Id.*, 157, 162.

gate structures 308C and 308D, respectively." PA-01, 12:54-67, FIG. 5B. Given gate contact via 542A is electrically connected to 308C (one of the metal gates) and gate contact via 542B is electrically connected to 308D (one of the metal gates), the **plurality of second contacts are electrically connected to one of the metal gates**.

Pethe discloses a single metal deposition in which metal (0) trench 334 is filled with metal (0) portion 550, gate contact vias 542A, 542B fill via openings 338, and trench contact vias 341A, 341B fill via openings 336. PA-01, 11:23-42. Pethe thus teaches trench contact vias, e.g. 341B (**at least one of the first contacts**), that **directly connects** gate contact vias, e.g. 542B (**at least one of the second contacts**), with no intervening layers or other barriers in the Figure 5B structure. *Id.*, 12:54-67; Ex-03, ¶105.[7]

[7] Pethe's teachings are consistent with the '747 patent's descriptions of first and second contacts formed next to each other. Ex-01, FIG. 9 (elements 52/54); Ex-02, 135.

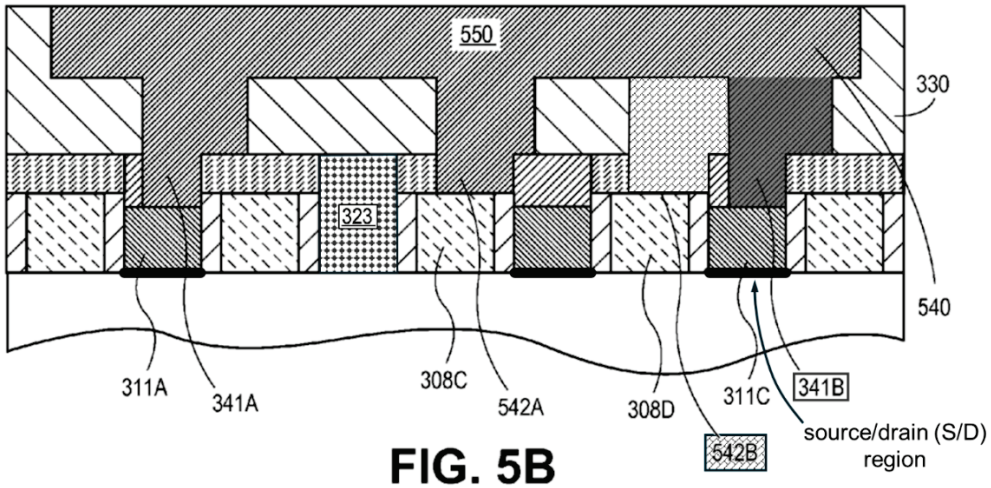


FIG. 5B

PA-01, 12:54-67, FIG. 5B (annotated to show gate contact via 542B in diagonal-brick pattern, trench contact via 341B in grey diagonal pattern, region 323 of inter-layer dielectric material, and source/drain regions under the trench contact 311C); PA-01, 10:35-36, 9:29-10:36; 12:54-59; Ex-03, ¶¶105-229.

Thus, Pethe discloses the limitation a first contact that "directly connects" with a second contact which lead to allowance. For at least the above reasons, Pethe raises SNQs for Claims 1-8.

In ***Proposed Rejection 1B***, embodiments relating to FIGs. 5A-5B of Pethe as the primary reference are combined with Pethe's embodiment relating to a multi-gate transistor structure. PA-01, 12:39-42. In particular, proposed rejection 1B combines Pathe's MOSFET structure having a first contact that "directly connects" with a second contact with Pethe's "tri-gate transistor" having a fin structure where a gate structure is for use with and "disposed over the non-planar diffusion or active

region 204C," which is identified as a "fin structure." *Id.*, 4:62-5:5, FIG. 2C; Ex-03, ¶¶105, 230-260.

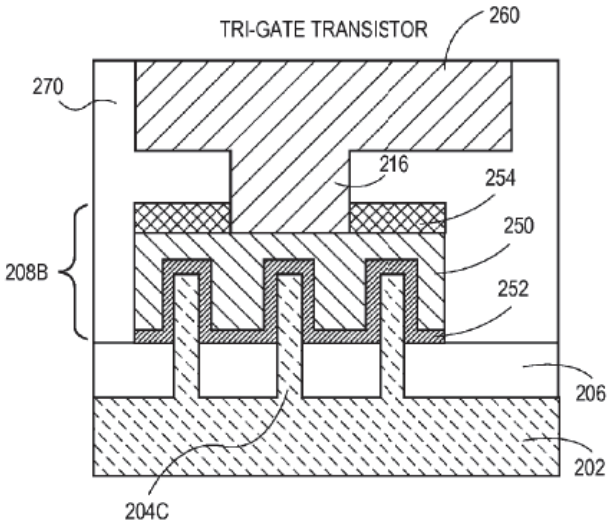


FIG. 2C

PA-01, 4:62-5:5; FIG. 2C. Pethe also teaches that "all of [trench] contacts 210A and 210B" in FIG. 2A may be composed of "a silicide material." PA-01, 6:53-59, 4:33-36, 11:26-31, 7:39-41.

Thus, as the proposed rejections below explain, a POSITA would have been motivated to combine the various embodiments in Pethe, and would have had a reasonable expectation of success in realizing their combination. For at least these reasons, Pethe raises SNQs for Claims 1-8.

In ***Proposed Rejection 1C***, Pethe is a primary reference combined with well-known features that are taught by Pham. In particular, proposed rejection 1C combines Pethe's MOSFET having trench contact vias (first contacts) that "directly

connects" gate contact vias (second contacts) and Pham's use of recessed gate structures with recessed spacers. Pham's processes form a metal gate and sidewall spacer configuration where the structures have planar top surfaces and are on the same level. PA-02 (Pham), 4:37-5:18, 8:9-58, FIGs. 2C-2D; Ex-03, ¶¶105, 261-354. As the proposed rejections below explain, a POSITA would have been motivated to combine Pethe and Pham, and would have had a reasonable expectation of success in realizing their combination. For at least these reasons, Pethe and Pham raise SNQs for Claims 1-8.

In ***Proposed Rejection 1D***, Pethe is a primary reference combined with well-known features that are taught by Sell. In particular, proposed rejection 1D combines Pethe's MOSFET having trench contact vias (first contacts) "that are electrically connected to parts of the S/D region" and Sell's use of a salicide between source/drain contact and the source/drain in a transistor structure such that "a salicide layer disposed between each S/D region and each first contact." PA-06 (Sell), 1:7-13, 3:6-16, 3:17-30, 4:5-18; FIGs. 1d, 1e, 1f, 11. As the proposed rejections below explain, a POSITA would have been motivated to combine Pethe and Sell, and would have had a reasonable expectation of success in realizing their combination. For at least these reasons, Pethe and Sell raise SNQs for Claim 7. Ex-03, ¶¶105, 355-375.

In ***Proposed Rejection 1E***, Pethe is a primary reference combined with well-known features that are taught by Huang. In particular, proposed rejection 1E combines Pethe's MOSFET having trench contact vias (first contacts) that "directly connects" gate contact vias (second contacts) and Huang's use of dual-damascene processing to provide M1 lines and M0 vias in forming its device. Huang describes M1 layer's metal lines 74 (a plurality of third contacts) and M0 vias 72 (hole structures) "for connecting to contact plugs 60 and 62." PA-03, ¶17, FIG. 8A; Ex-03, ¶¶105, 376-406. As the proposed rejections below explain, a POSITA would have been motivated to combine Pethe and Huang, and would have had a reasonable expectation of success in realizing their combination. For at least these reasons, Pethe and Huang raise SNQs for Claims 8 and 9.

B. Chang, Sell, Huang, Chi, and Hong Raise SNQs

Proposed rejections 2A, 2B, 2C, 2D, 2E, 2F, and 2G rely on Chang. In ***Proposed Rejection 2A***, Chang is used as an anticipation reference. Chang teaches self-aligned contacts 1670, 1671, 1675 (first parts of which correspond to **plurality of first contacts**) that are electrically connected to the source/drain regions of PMOS transistor structure 1616, the self-aligned contacts 1670, 1671, 1675 **disposed in** interlayer dielectric layer 1503 (**first dielectric layer**). PA-04, ¶¶112-13, FIG. 27; Ex-03, ¶¶105, 407-503. The second parts of Chang's self-aligned contacts 1670 (identified as 1642) and 1671 (which correspond to **plurality of second contacts**)

are electrically connected to gates 1446, 1597 that are also **disposed in** interlayer dielectric layer 1503 (**first dielectric layer**). PA-04, ¶¶112-13. Chang teaches that self-aligned contacts 1670, 1671 are "merged" contacts "that contacts the respective gate as well as the adjacent PMOS diffusion region 1600," whereby, for contact 1670 for example, the right portion (**at least one of the first contacts**) **directly connects** the "merged" left portion (**at least one of the second contacts**) without any intervening layers or other barriers. PA-04, ¶¶112. Chang also explains that its transistor structure 116 (diffusion region 1600) includes a fin 104. PA-04, ¶¶48, 110-112; Ex-03, ¶¶105, 407-503.

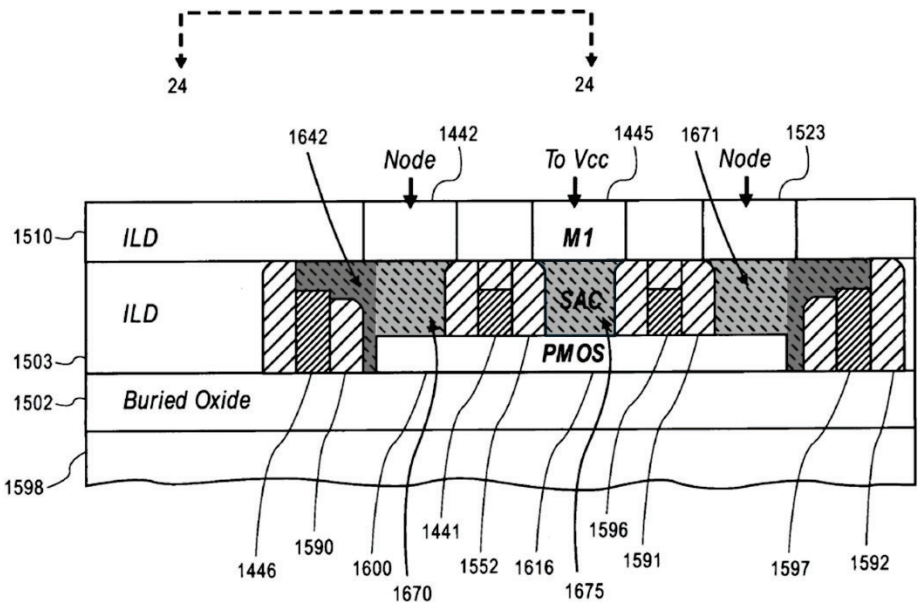


FIG. 27

PA-04, FIG. 27 (annotated to show first contacts in light grey dash-diagonals, and second contacts in dark grey dash-diagonals), ¶¶110-13.

Thus, Chang discloses the limitation a first contact that "directly connects" with a second contact which lead to allowance. For at least the above reasons, Chang raises SNQs for Claims 1-2 and 6.

In ***Proposed Rejection 2B***, Chang's structure is modified by well-known techniques related to Chang's single deposition of self-aligned contacts 1670, 1671. Chang recognizes the single deposition approach advantageously "result[s] in a higher aspect ratio for etch and metal deposition." PA-04 (Chang), ¶105; Ex-03, ¶¶105, 504-556. As was known, a higher aspect ratio contact means the contact is achieved with a narrower width, and thus less chip area is required, and resultingly, more structures/devices may be provided on a given area. PA-04 (Chang), ¶¶97, 105. A POSITA would have been motivated to implement such features in Chang's structure such that each first and/or second contact is a monolithically formed structure. The POSITA would have had a reasonable expectation of success in realizing such a modification. Additionally, Chang teaches that "transistor structure 116 includes diffusion layer 104 (also called diffusion body 104 or fin 104)." PA-04, ¶48. A POSITA would have understood diffusion area 704 would have been "also called" a fin, which compris[es] at least one fin structure. For at least these reasons, Chang raises SNQs for Claims 1-2 and 4-6.

In ***Proposed Rejection 2C***, Chang is a primary reference combined with well-known features that are taught by Sell. In particular, proposed rejection 2C combines

Chang's self-aligned contacts 1670, 1671 (parts of which correspond to the claimed plurality of first contacts and plurality of second contacts that are "directly" connected) and Sell's use of a salicide between source/drain contact and the source/drain in a transistor structure such that "a salicide layer disposed between each S/D region and each first contact." PA-06 (Sell), 1:7-13, 3:6-16, 3:17-30, 4:5-18; FIGs. 1d, 1e, 1f, 11; Ex-03, ¶¶105, 557-638. As the proposed rejections below explain, a POSITA would have been motivated to combine Chang and Sell, and would have had a reasonable expectation of success in realizing their combination. For at least these reasons, Chang and Sell raise SNQs for Claims 1-7.

In ***Proposed Rejection 2D***, Chang is a primary reference combined with well-known features that are taught by Sell and Huang. In particular, proposed rejection 2D combines Chang's self-aligned contacts 1670, 1671, 1675 (parts of which correspond to the claimed plurality of first contacts and plurality of second contacts that are "directly" connected) and inter-layer dielectric layers 1503, 1510, with Sell's etching stop layer (108) disposed on two sides of a metal gate 104 where the etching stop layer has a truncated top surface, and Huang's overlay metal lines 74 and vias 72. PA-06 (Sell), 2:10-49, 50-61, FIG. 1d; PA-03 (Huang), ¶17, FIG. 8A; Ex-03, ¶¶105, 639-672. As the proposed rejections below explain, a POSITA would have been motivated to combine Chang, Sell and Huang, and would have had a

reasonable expectation of success in realizing their combination. For at least these reasons, Chang, Sell, and Huang raise SNQs for Claims 8 and 9.

In ***Proposed Rejection 2E***, Chang is a primary reference combined with well-known features that are taught by Chi. In particular, proposed rejection 2E combines Chang's self-aligned contacts 1670, 1671 (parts of which correspond to the claimed plurality of first contacts and plurality of second contacts that are "directly" connected) and Chi's sidewall spacers 32 that are subject to one or more CMP processes are performed to remove portions of material from its structure. PA-04 (Chang), ¶105; PA-05 (Chi) 14:25-15:9, FIGs. 3C-3E, 15:41-16:60, FIG. 3I-3J; Ex-03, ¶¶105, 673-762. As the proposed rejections below explain, a POSITA would have been motivated to combine Chang and Chi, and would have had a reasonable expectation of success in realizing their combination. For at least these reasons, Chang and Sell raise SNQs for Claims 1-7.

In ***Proposed Rejection 2F***, Chang is a primary reference combined with well-known features that are taught by Huang. In particular, proposed rejection 2F combines Chang's gates 1441, 1443, 1446, 1596, 1597 and Huang's gate spacers 34, Contact Etch Stop Layer (CESL) 36 disposed on both sides of gate dielectric 24 and gate electrode 26, and overlay metal lines 74 and vias 72. PA-04 (Chang), FIG. 27; ¶¶112, 108, 114, 47, 111, FIG. 24; PA-03 (Huang), FIG. 1, 8A, ¶¶ 8-10, 14, 17; Ex-03, ¶¶105, 763-847. As the proposed rejections below explain, a POSITA would

have been motivated to combine Chang and Huang, and would have had a reasonable expectation of success in realizing their combination. For at least these reasons, Chang and Huang raise SNQs for Claims 1-9.

In ***Proposed Rejection 2G***, Chang is a primary reference combined with well-known features that are taught by Hong. In particular, proposed rejection 2G combines Chang's self-aligned contacts 1670, 1671 (parts of which correspond to the claimed plurality of first contacts and plurality of second contacts that are "directly" connected) and Hong's formation of a first contact layer 442 in a first dielectric layer 401 and a second dielectric layer 406. PA-04 (Chang), ¶105; PA-07 (Hong), 8:54-9:27, FIG. 7; Ex-03, ¶¶105, 848-868. As the proposed rejections below explain, a POSITA would have been motivated to combine Chang and Hong, and would have had a reasonable expectation of success in realizing their combination. For at least these reasons, Chang and Hong raise SNQs for Claims 4 and 5.

VI. DETAILED EXPLANATION OF THE PROPOSED REJECTIONS

A. Proposed Rejections 1A-1E: Pethe

1. Proposed Rejection 1A: Claims 1-8 Are Anticipated by *Pethe*

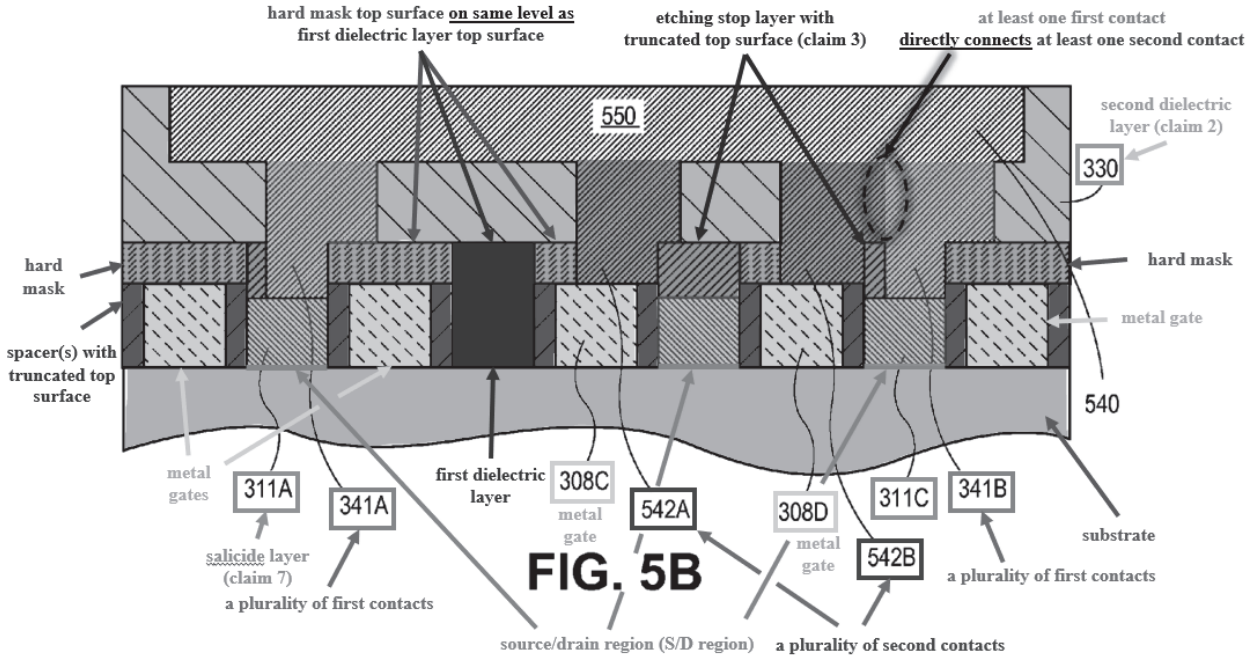
Pethe discloses gate contact structures disposed over active portions of gates and methods of forming such structures. PA-01, 2:50-52, 2:50-3:10. Pethe explains "well-known features, such as integrated circuit design layouts, are not described in

detail in order to not unnecessarily obscure embodiments of the present invention." *Id.*, 2:55-62; Ex-03, ¶¶106-107.

Pethe discloses a semiconductor structure in FIG. 5B, including substrate 302, gate electrodes 308, trench contacts 311A-C, ILD region 323, dielectric layer 330, and trench contact vias 341, which are common features (same labels) with FIG. 3 and discussed therein (PA-01, 12:22-13:12, FIGs. 5A-5B; *id.*, 2:3-26, 7:9-11:42) (Pethe does not repeat the details/discussions in FIG. 5B).[8] Additionally, FIG. 5B's structure includes common features (similar labels) with slight difference from FIG. 3 due to recess of spacers 520 (same as spacers 320). *Id.*, 12:22-26, 12:48-53. The features include a cap layer 522 (same as cap layer 322 but wider because of the recessed spacers 520) and includes gate contact vias 542 and metal portion 550 (same as gate contact vias 342 and metal portion 350 but extending deeper because of recessed spacers 520). *Id.*, 12:62-64 ("In comparison to the structure described in association with FIG. 3F, the resulting structure of FIG. 5B is slightly different since the spacers 522 are not exposed, yet coverage of the insulating cap layers 522 is extended, during etch formation of the via openings leading to gate contact vias

[8] To be clear, Pethe's FIG. 5B structure (alone or as modified/combined) discloses/suggests the claim structure in the challenged claims addressed in Proposed Rejections 1A-1E for reasons explained.

542A and 542B."); Ex-03, ¶¶106-107. Pethe discloses each of the limitations of the Claims, as summarily exemplified below.



PA-01 (Pethe), FIG. 5B.

A POSITA would have understood Pethe to disclose features relating to MOS transistors (MOSFETs) and thus describes features in the same technical field as the '747 Patent and reasonably relevant to a problem that the '747 Patent alleges to address. *See e.g.*, PA-01, 1:7-3:10, 7:9-11:42, 12:22-13:12; PA-01, 1:5-2:9, 2:39-3:25, 5:1-6:37. For example, Pethe discloses the formation of gate and source/drain contacts that are in direct contact with no barrier layer or other intervening layer or material between them similar to the shared contact features highlighted by the '747 Patent. *See, e.g.*, limitations 1(f)-1(h) below; Ex-01 ('747 Patent), 1:22-39, 2:1-9, 5:1-30, FIG. 9.

a. Claim 1

(1) [1.pre] A semiconductor structure, comprising:

To the extent limiting, Pethe discloses claim 1's preamble. Ex-03, ¶¶108-109; *infra* §§VI.A.1.a(2)-(9). Pethe discloses a "semiconductor structure" as claimed. For example, the structure described in connection with FIG. 5B (below) of the Figure 5 embodiment of Pethe (FIGs. 5A-5B) is **a semiconductor structure**, the fabrication of which is shown collectively in FIGs. 5A-5B. PA-01, 2:32-36, 12:32-33.

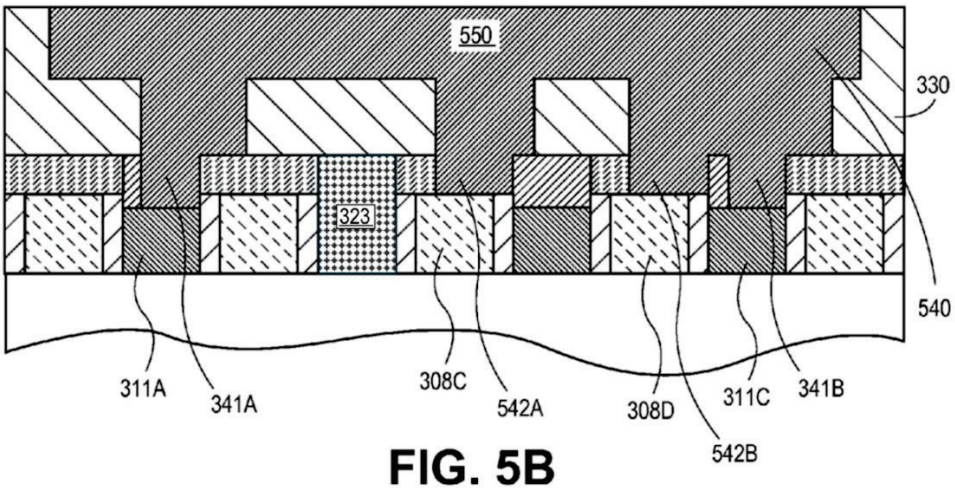


FIG. 5B

PA-01, FIG. 5B (annotated).

(2) [1.a] a substrate;

Pethe discloses this limitation. Pethe's device 500 in FIG. 5A includes **a substrate** 302. Pethe labels substrate 302 in FIG. 5A, which is the same substrate shown (but unlabeled) in FIG. 5B. PA-01, 12:32-39, FIGs. 5A-5B (annotated to show **substrate 302**); Ex-03, ¶¶110-112.

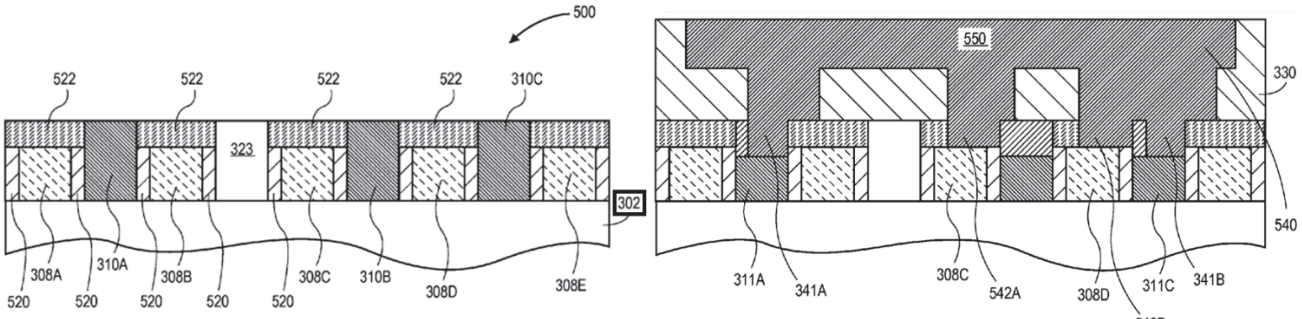


FIG. 5A FIG. 5B

PA-01, 12:37-45, FIGs. 5A-5B (annotated).

(3) [1.b] a first dielectric layer disposed on the substrate;

Pethe discloses this limitation. Ex-03, ¶¶113-120. Pethe discloses an inter-layer dielectric layer that includes **region 323 disposed on the substrate 302** as shown in FIG. 5B's structure. The inter-layer dielectric layer is the first dielectric layer. *See* PA-01, 2:32-36, 12:32-53, FIG. 5A.

Region 323, while not labeled, is likewise included in the FIG. 5B structure. A POSITA would have understood that while not labeled, the same region 323 is included in the FIG. 5B structure and **disposed on substrate 302**, which is also annotated in red below. *See* PA-01, 2:32-36, 12:54-13:12, FIG. 5B; Ex-03, ¶114.

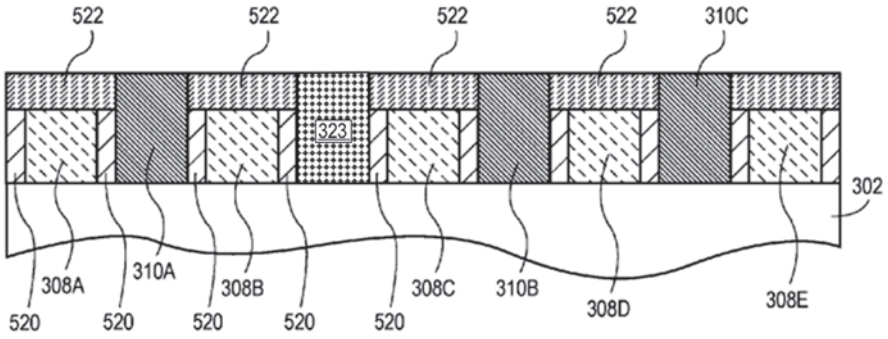


FIG. 5A

PA-01, FIG. 5A (annotated).

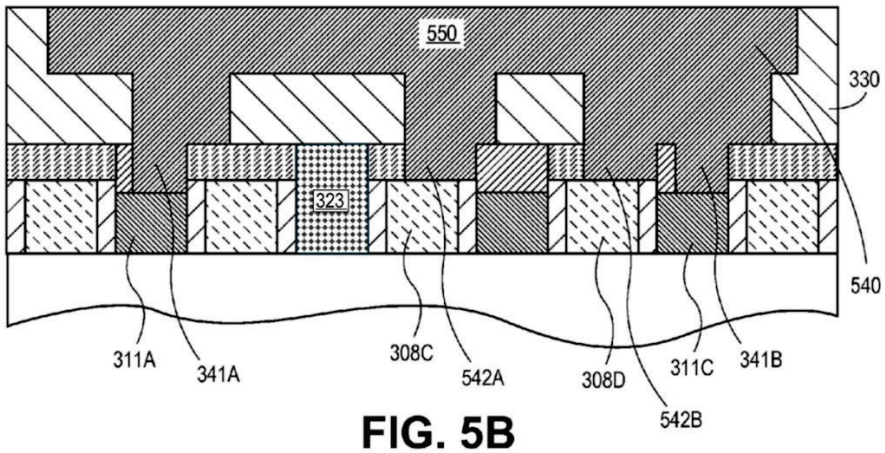


FIG. 5B

Id., FIG. 5B (annotated).

Pethe describes region 323 in similar fashion in connection with FIGs. 3A-3F. Namely, Pethe explains with reference to FIG. 3A that region 323 is "contact blocking regions or 'contact plugs' [that is] fabricated from an inter-layer dielectric material." *See* PA-01, 2:32-36, 7:15-34, FIGs. 3A, 3F (annotated below); *see also* FIGs. 3B-3F (showing same region (unlabeled) in the subsequent fabrication processes leading to the structure of FIG. 3F), 7:9-14; Ex-03, ¶115.

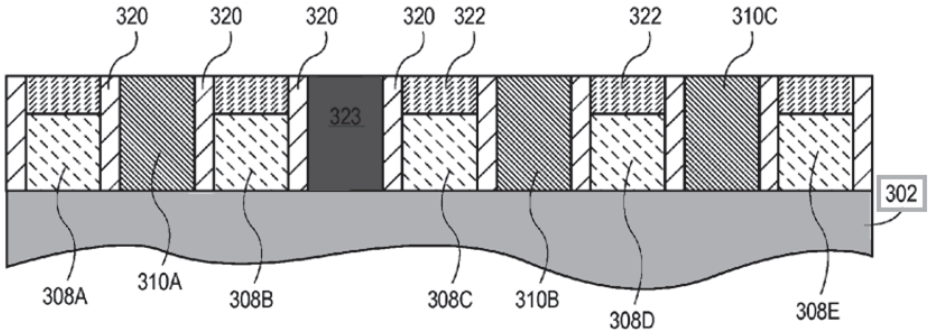


FIG. 3A

PA-01, FIG. 3A (annotated).

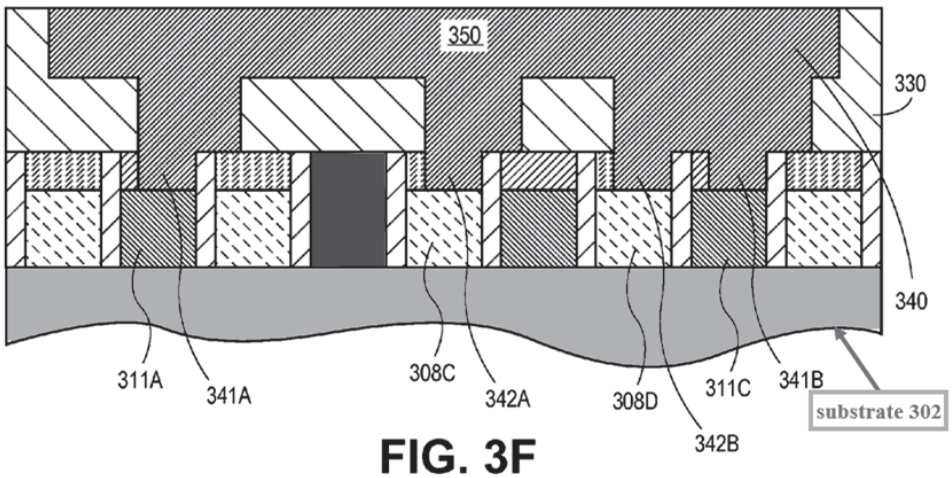


FIG. 3F

PA-01, FIG. 3F (annotated).

A POSITA would have understood that Pethe's consistent use of "region 323" in the Figure 3 and Figure 5 embodiments, and the description of region 323 in connection with Figure 3A, apply to Pethe's discussion of region 323 in those embodiments, including region 323 in the structure of FIG. 5B. *See e.g.*, PA-01, FIGs. 3A-3F, 5A-5B, 7:11-11:42, 12:15-13:12; Ex-03, ¶116.

A POSITA would have thus understood from Pethe's disclosure that region 323 is a layer in the Figure 5B structure (and in the FIG. 5A structures) that is fabricated from, and a part of, the "inter-layer dielectric material." The inter-layer dielectric ("ILD") with the inter-layer dielectric material of region 323 that is disposed on **substrate 302** is the claimed "first inter-layer dielectric layer." For example, as identified above, Pethe explains that "region 323 fabricated from an inter-layer dielectric material, may be included in regions where contact formation is to be blocked" (PA-01, 7:31-34). Therefore, a POSITA would have understood

the inter-layer dielectric (from which the inter-layer dielectric material of region 323 is a part) is formed in regions of the semiconductor structure as a layer where contact formation is blocked, such as shown in FIGs. 5A-5B, and thus fills space between structural elements in a semiconductor structure consistent with known ILDs used at the time. Ex-03, ¶117.

Further, the teachings in Golonzka (Ex-05), which Pethe incorporates by reference, describes a process that may be used to provide structure 300, and explains that Pethe's dielectric layer, which inter-layer dielectric material of region 323 is a part, is a "first inter-layer dielectric layer" as claimed. *See* PA-01, 7:35-41 ("[a] process used to provide structure 300 may be one described in International Patent Application No. PCT/US 11/66989, entitled "Gate Aligned Contact and Method to Fabricate Same," filed Dec. 22, 2011 by Intel Corp., incorporated by reference herein" and "[f]or example, a trench contact etch engineered selective to the insulating cap layer 322 may be used to form self-aligned contacts 310A-310C"). Ex-03, ¶118.

Golonzka discloses deposition and planarization processes for forming a first permanent interlayer dielectric portion" 128 and a "second permanent interlayer dielectric portion" 132 that like the inter-layer dielectric including the inter-layer dielectric material of region 323 in Pethe's FIG. 5B structure is a layer in a semiconductor structure. *See* Ex-05 (Golonzka), ¶41 ("Referring to Figure 1G, an

interlayer dielectric layer 126 is formed above the patterned dielectric layer 124 and above and between the exposed dummy gates 108 of the gate line grating 106"), ¶42 ("Referring to Figure 1H, the interlayer dielectric layer 126 and the patterned dielectric layer 124 are planarized to expose the top portions of all dummy gates 108 of the gate line grating 106. In accordance with an embodiment of the present invention, the planarizing provides a first permanent interlayer dielectric portion 128"), ¶43, ¶44 ("Figure 1I may be of a cross-section in a location different (e.g., into or out of the page) than the cross-section illustrated in FIG. 1H. Thus, at this point, a permanent interlayer dielectric layer may be defined by the combination of the first permanent interlayer dielectric portion 128 formed in first regions (not shown in Figure II) and the second permanent interlayer dielectric portion 132 formed in second regions"), ¶¶45, 47, 50, FIGs. 1A-1K, 2; Ex-03, ¶119.

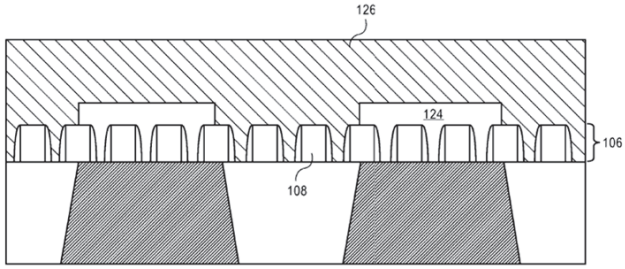


FIG. 1G

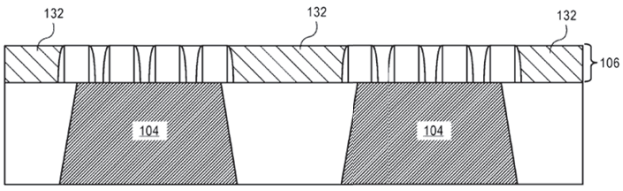


FIG. 1I

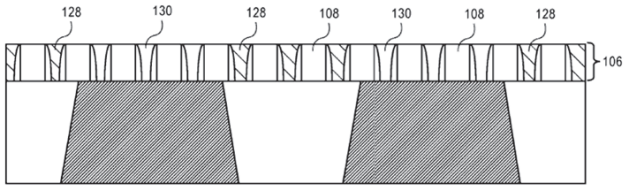


FIG. 1H

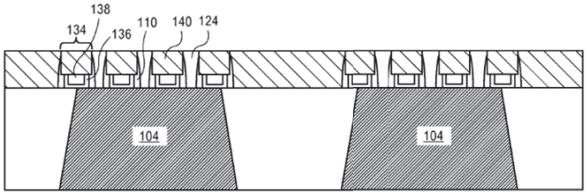


FIG. 1J

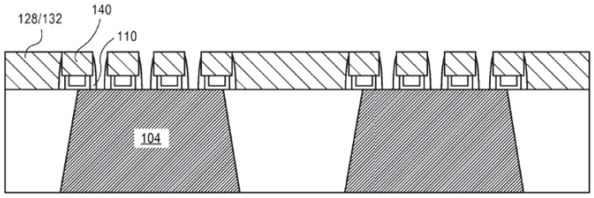


FIG. 1K

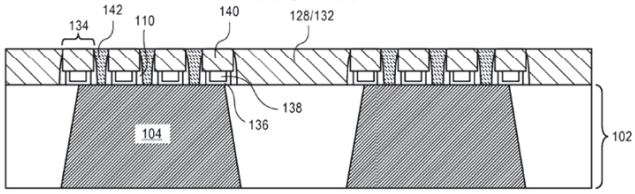


FIG. 2

Ex-05 (Golonzka), FIGs. 1G-1K, 2.

Thus, Pethe's FIG. 5B structure includes contact blocking regions (of which region 323 is a part and fabricated with inter-layer dielectric material (*supra*)) that is a **dielectric layer** (hereinafter "Pethe's first dielectric layer") that is **disposed on the substrate** (302). PA-01, 12:32-53, 7:20-34, 12:39-13:12; Ex-03, ¶120.

(4) [1.c] at least two metal gates disposed in the first dielectric layer;

Pethe discloses this limitation. Ex-03, ¶¶121-127. Pethe's structure in FIG. 5A includes "one or more gate stack structures, such as gate stack structures 308A-308E disposed above substrate 302" (PA-01, 12:32-39) and are disposed in the inter-layer dielectric that region 323 is a part) (i.e., the "first dielectric layer"), as shown below.

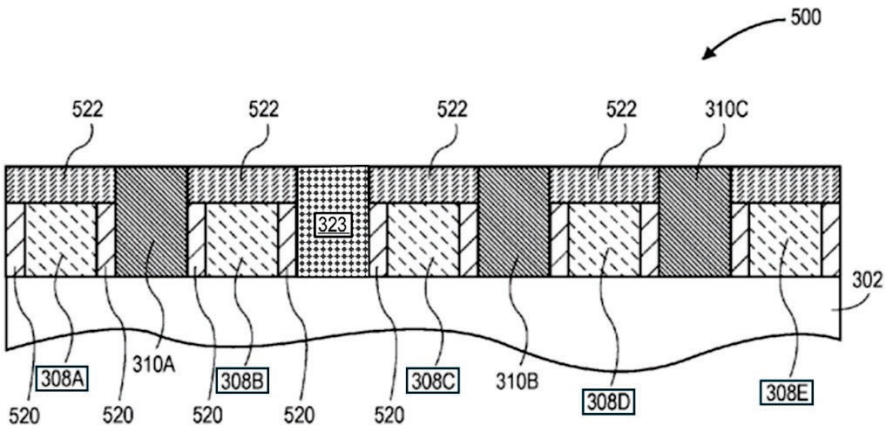


FIG. 5A

Pethe's semiconductor structure of FIG. 5B likewise includes the same five gate stack structures 308A-308E disposed above substrate 302 and disposed in the inter-layer dielectric that region 323 is a part (i.e., the "first dielectric layer"), as shown below.

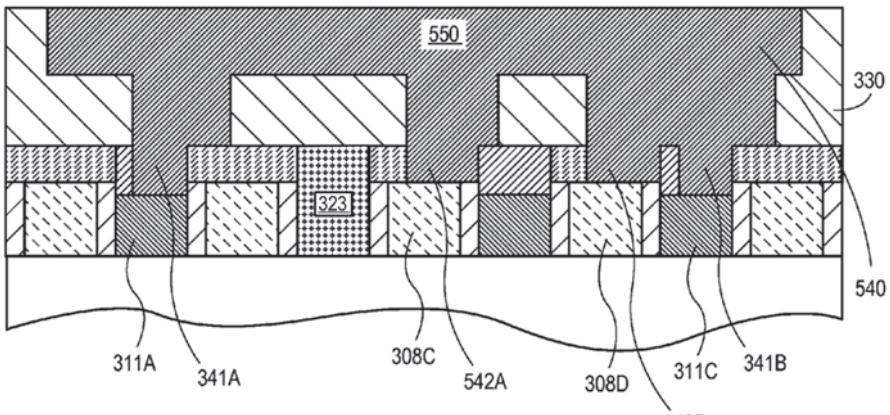


FIG. 5B

PA-01, 12:32-53; Ex-03, ¶122.

Pethe explains that "[t]he gate stack structures may include a gate dielectric layer and a gate electrode, as described above in association with FIG. 2." *Id.*, 12:39-42.

With reference to FIGs. 2A-2C, Pethe describes "the gate electrode of gate electrode stack is composed of a metal gate" (*id.*, 6:16-21) and that "[i]n one embodiment, the gate electrode is composed of a metal layer such as, but not limited to, metal nitrides, metal carbides, metal silicides, metal aluminides, hafnium, zirconium, titanium, tantalum, aluminum, ruthenium, palladium, platinum, cobalt, nickel or conductive metal oxides" (*id.*, 6:37-41.)

Further, the FIG. 5A structure is "provided following trench contact (TCN) formation." *Id.*, 12:32-53. Pethe also incorporates the teachings of Golonzka to describe a process used to provide structure 300. *Id.*, 7:35-41. Golonzka discloses forming permanent gate electrode layer or stack 138 (Ex-05 (Golonzka), ¶47) that

"is composed of a metal gate" (*id.*, ¶49). *See also e.g., id.*, FIGs. 1J, 1K, 2 (below, showing metal gate 138 disposed in dielectric layer 128/132).

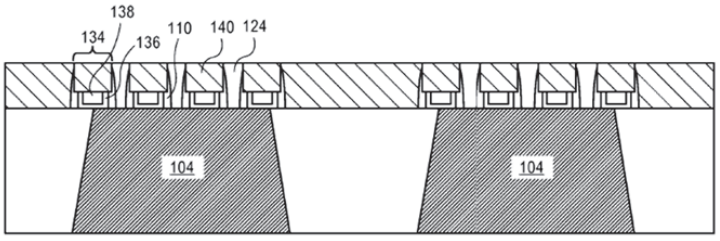


FIG. 1J

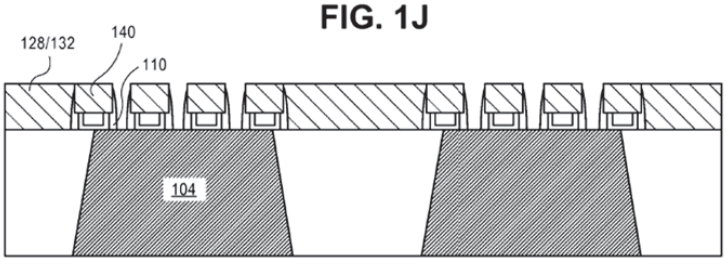


FIG. 1K

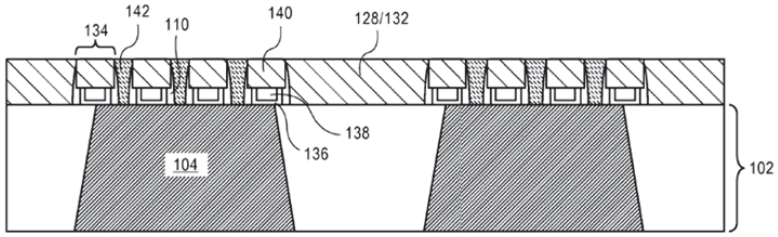


FIG. 2

Ex-05, FIGs. 1J-1K, 2. A POSITA would have understood such teachings likewise disclose that each of the five similarly labeled gate stack structures 308A-308E in the FIG. 5B structure of Pethe includes a metal gate. Accordingly, the resulting Figure 5B structure includes at least two metal gates disposed in the first dielectric layer as claimed.

The relationship of the metal gates and the first dielectric layer in Pethe's Figure 5B structure is consistent with the '747 patent disclosure of similar features:

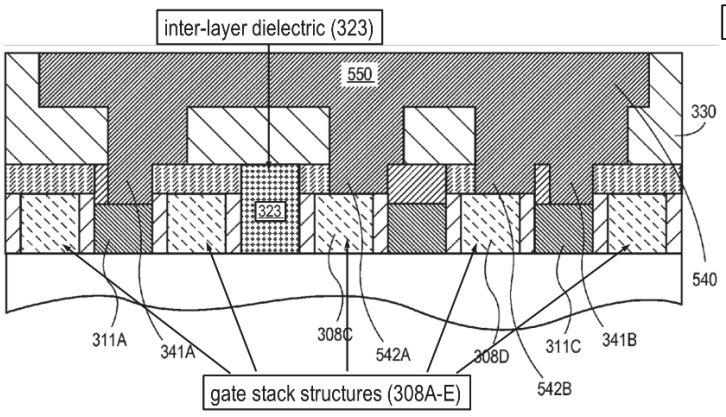


FIG. 5B

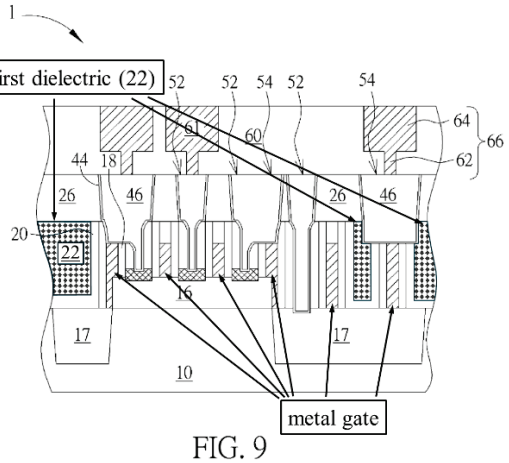


FIG. 9

PA-01 (Pethe), 95-99; Ex-01 ('747 Patent), 5:66-6:5.

Thus Pethe discloses that the semiconductor structure of FIG. 5B includes **at least two metal gates** (e.g., any two of 308A-308E) that are **disposed in the inter-layer dielectric** that region 323 is a part, as claimed. Ex-03, ¶¶123-127.

(5) [1.d] a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface;

Pethe discloses this limitation. Ex-03, ¶¶128-146. Pethe discloses that the semiconductor structure of FIG. 5B includes a spacer disposed on two sides of the metal gate[9], wherein the spacer has a truncated top surface. For example, Pethe

[9] For purposes of analysis concerning the prior art (here and in the other proposed rejections discussed below), Requester assumes the term "disposed on two sides of **the metal gate**" refers to any of the metal gates that are included in the claimed semiconductor structure. Ex-03, ¶¶128-146. As explained below, Pethe discloses

explains "trench contacts 310A-310C…**are spaced apart from gate stack structures 308A-308E by dielectric spacers 520**." PA-01 (Pethe), 12:37-45, FIG. 5A (annotated below).

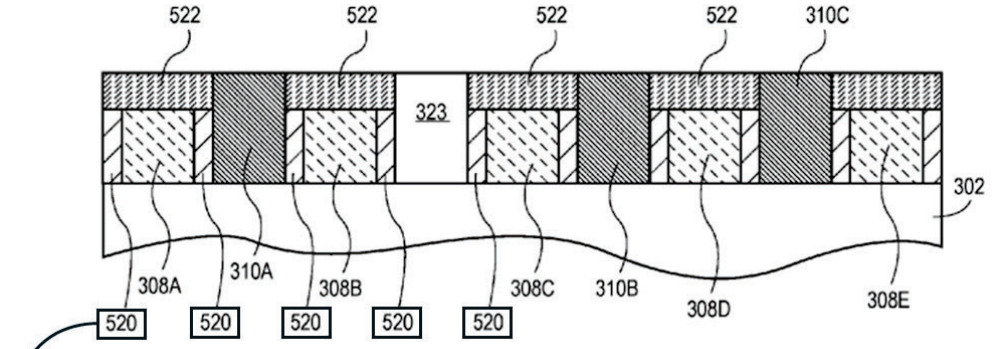


FIG. 5A

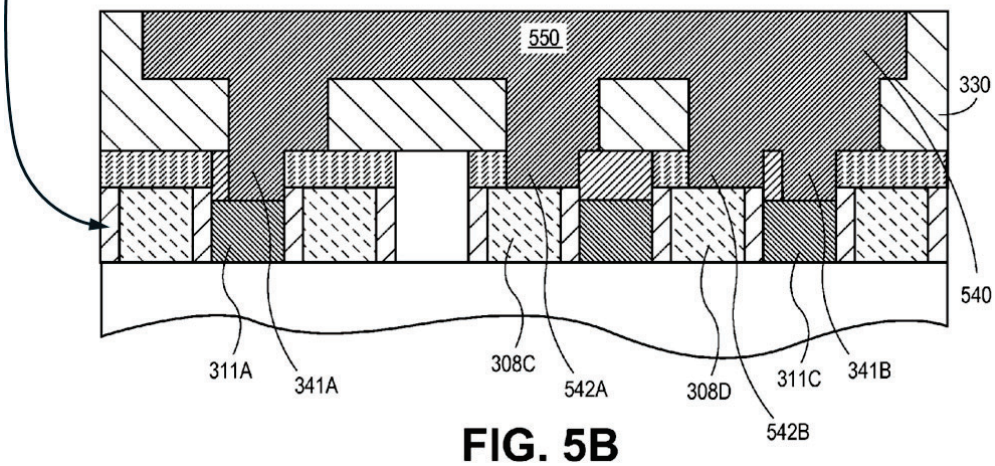


FIG. 5B

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that spacers 520 are disposed on two sides of gate stack structures 308A-308D, and as one example on two sides of gate stack structures 308C and 308D, which collectively is a non-limiting example of the claimed "at least two metal gates" recited in limitations 1(c). *Id.*

PA-01, 12:42-53, 12:22-31, FIGs. 5A-5B; Ex-03, ¶¶129-130. While the spacers are unlabeled in FIG. 5B, a POSITA would have understood from Pethe's disclosure that the same structural elements in the FIG. 5B structure where spacers 520 are identified in FIG. 5A are spacers in the FIG. 5B structure, as annotated below. *See id.*, 12:15-67.

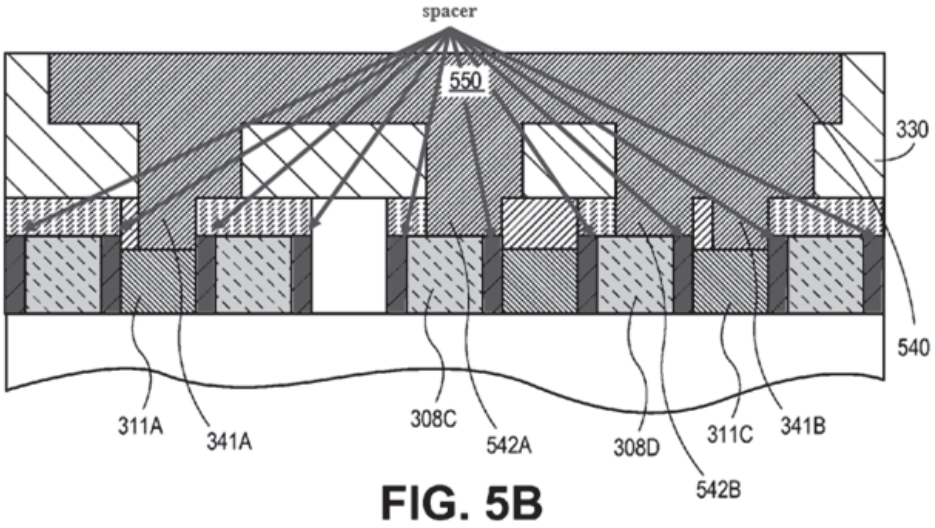


FIG. 5B

PA-01, FIG. 5B (annotated).

Notably, Pethe misidentifies "spacers 522." *Id.*, 12:62-67. A POSITA would have understood that element "522" is, as Pethe correctly identifies in the same sentence, the "insulating cap layers 522" that are identified in FIG. 5A. A POSITA would have understood that "spacers 522" to be a typographical error or the like, since the same spacers in FIG. 5A are identified as "spacers 520." Thus, a POSITA would have understood the spacers in the FIG. 5B structure are the recessed spacers 520 described in connection with FIG. 5A. Ex-03, ¶131.

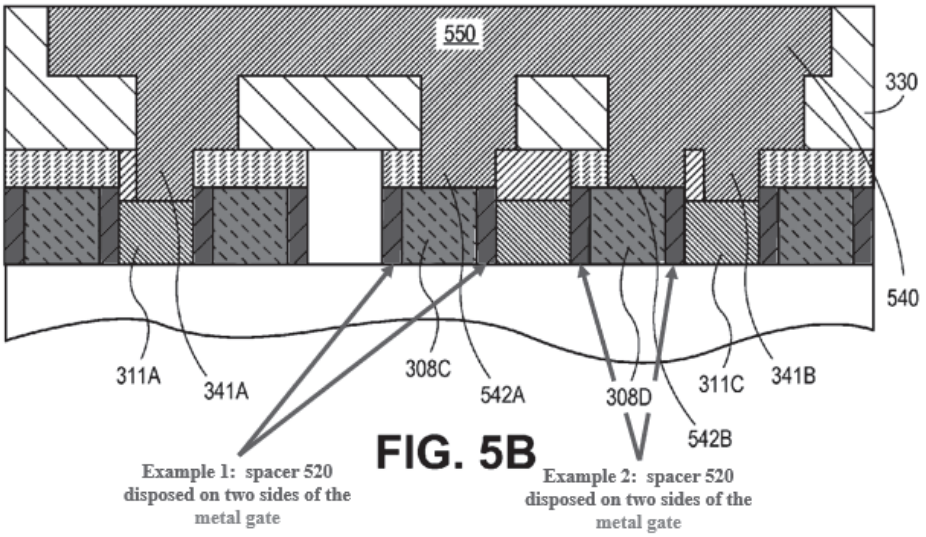


FIG. 5B

Id., FIG. 5B (annotated).

Accordingly, the spacers 520 disposed on two sides of any of the metal gates in the FIG. 5B structure (i.e., gate stack structures 308A-308E) is a "spacer disposed on two sides of the metal gate." For example, the spacers 520 disposed on two sides of either gate stack structure 308C or gate stack structure 308D is each an example of the claimed "spacer disposed on two sides of the metal gate." Ex-03, ¶132.

A POSITA would have also understood that Pethe describes spacers 520 in connection with FIGs. 3A-3F referring to the "tops" of the spacers being "planar" with other structures (*e.g.* "the spacers may be recessed to be essentially planar with the gate structures," PA-01, 12:15-31). Ex-03, ¶¶133-134. Pethe explains that "in contrast to the structure 300 described in association with FIG. 3A, the spacers 520 have been recessed to approximately the same height as the gate stack structures 308A-308E." *Id.*, 12:42-53, 12:62-67. As shown in comparison below, the spacers

520 in FIGs. 5A and 5B are "**recessed**" (see down arrow) and lower in height relative to spacers 320 in FIGs. 3A and 3F so that spacers 520 are "planar with the gate structures" (i.e., gate stack structures 308A-308E) unlike the spacers 320, which are not co-planar with the gate stack structures 308A-308, and thus taller than spacers 520. *Id.*, 12:22-31. Ex-03, ¶¶135-137.

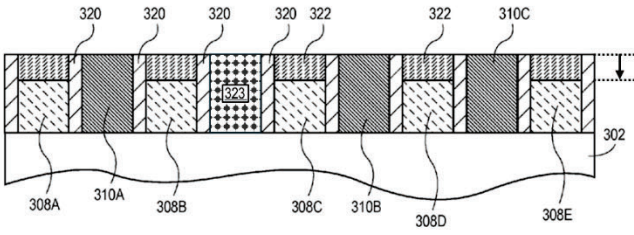


FIG. 3A

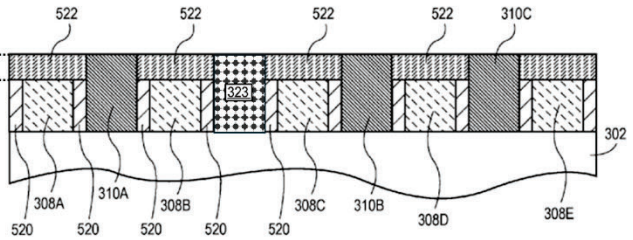


FIG. 5A

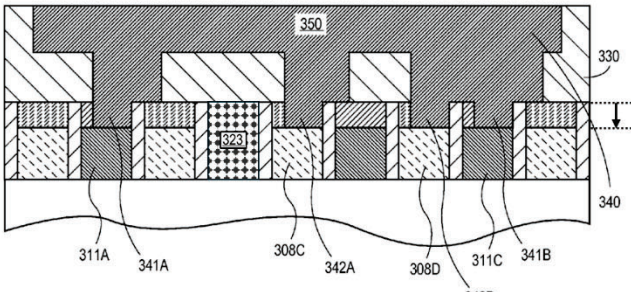


FIG. 3F

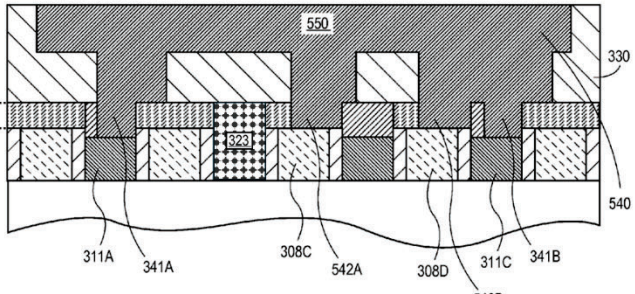


FIG. 5B

PA-01 (Pethe), FIGs. 3A, 3F, 5A-5B. Further, in describing the trench contacts 310A-310C in FIGs. 5A and 5B, Pethe explains that "the trench contacts (including trench contacts labeled 311A and 311C in FIG. 5B) **are recessed lower** relative to the gate stack structures (including gate stack structures labeled 308C and 308D in FIG. 5)." *Id.*, 13:1-5, FIG. 5A-5B (annotated above showing lower recessed trench contacts).

Pethe also describes forming recessed structures by etching. *Id.*, 8:37-51 ("For example, in one embodiment, the trench contacts 310A-310C are recessed by an etch process such as a wet etch process or dry etch process"). Such a process would result in Pethe's spacers 520 in the FIG. 5B structure each having a "truncated top surface" as recited in the Claims of the '747 Patent under Interpretations 1-3 for the following reasons. *See* §II.D.1.

Interpretation 1

Pethe explains that the spacers 520 in the FIG. 5B structure have been "recessed to be essentially ***planar***." *Id.*, 12:22-31, FIGs. 5A-5B; §I.C. Pethe also expressly describes planar spacers in its claims. *See* PA-01, 17:63-67 (Claim 5 as issued, Claim 9 as originally filed), 18:22-25 (Claim 11 as issued, Claim 15 as originally filed, reciting in the originally filed claim "wherein a **top surface of the plurality of gate structures** is approximately **co-planar with a top surface of each of the pair of sidewall spacers**").[10] A POSITA would have understood from Pethe's disclosure that the top surface of each of the spacers 520 in the FIG. 5B

[10] While Pethe was published on October 4, 2016 after the filing date (May 2, 2013) of the '747 Patent, Pethe's claims, and the corresponding disclosures in the specification, were filed on September 19, 2012, before the filing date of the '747 Patent.

structure is planar (i.e., each spacer 520 has a planar top surface, which meets the requirements of Interpretation 1. *See* §II.D.1; Ex-03, ¶138.

In addition, Pethe's spacers 520 look like and have a top surface similar to the spacers 18 with a "truncated top surface" as described in the '747 Patent. Ex-01, FIGs. 1-9, 2:63-3:25 ("since parts of the spacer 18…are removed during another planarization process, so the spacer 18 and CESL 20 have a truncated top surface"), 6:18-24.

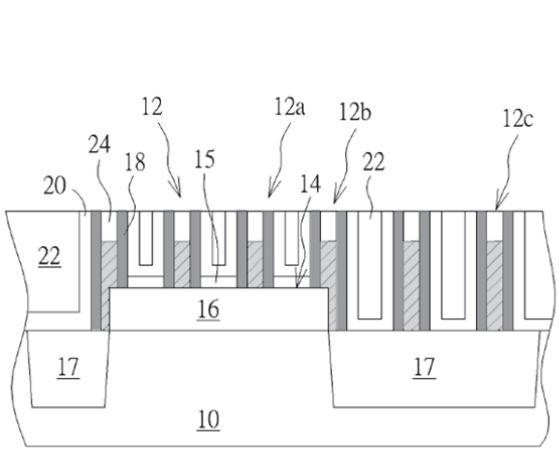


FIG. 1

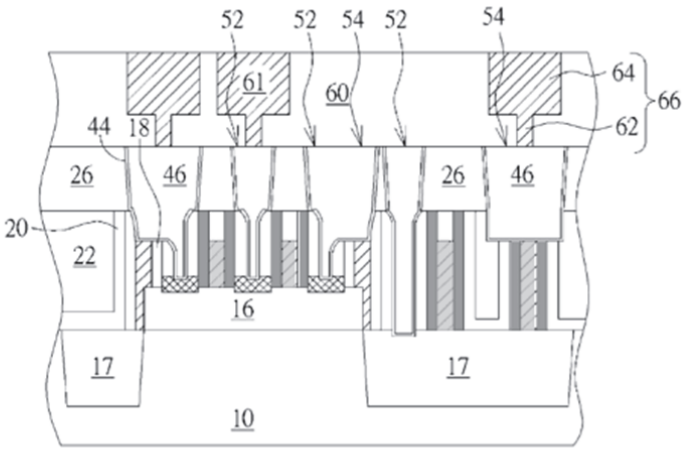


FIG. 9

PA-01, FIGs. 1, 9 (annotated). Pethe's spacers 520 also look like and have a top surface similar to the same spacers 18's identified by Applicant to have a truncated top surface during prosecution.

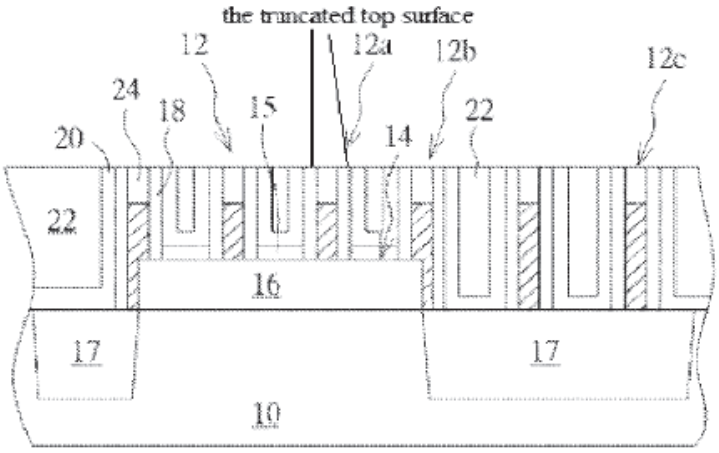


FIG. 1

Ex-02 (File History of '747 Patent), 106; *see also id.*, 104-108.

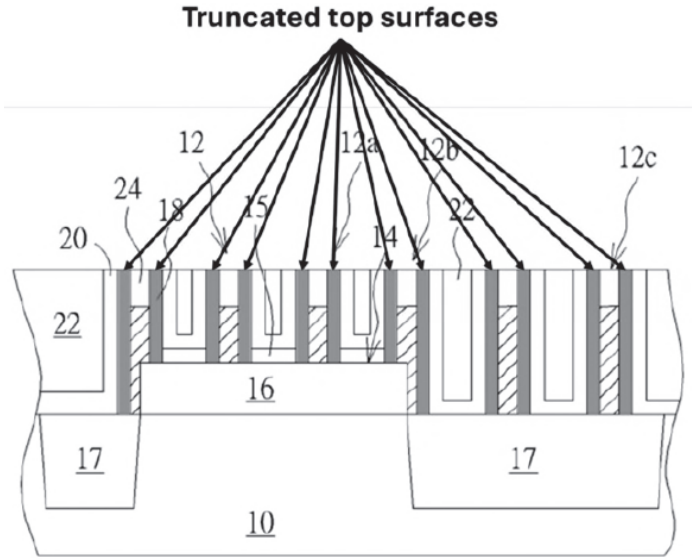


FIG. 1

Ex-37 (Complainants' Initial *Markman* Brief), 18.

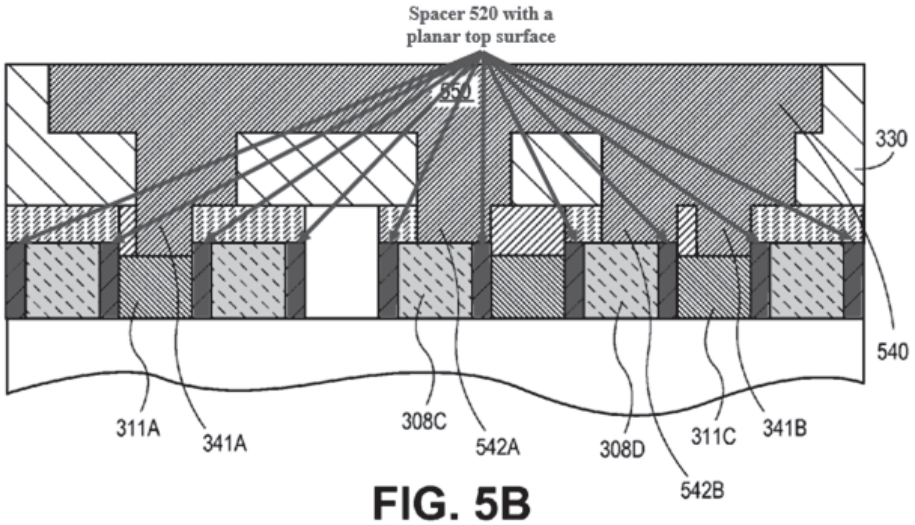


FIG. 5B

PA-01, FIG. 5B (annotated). Ex-03, ¶¶139-140.

As previously mentioned, Pethe states that "the spacers may be recessed to be essentially planar with the gate structures." PA-01, 12:22-23. As shown above in the above FIG. 5B structure, the result of recessing spacers 520 is a top surface that is "planar" with the gate stack structures 308A-308E. Thus, a POSITA would have understood that in order to fabricate the FIG. 5B structure, after their formation, spacers 520 were planarized by a planarization process to attain the planar top surface shown in FIGs. 5A-5B. Ex-03, ¶¶141-142.

Pethe also expressly describes planar spacers in its claims. *See* PA-01, 17:63-67 (Claim 5 as issued, Claim 9 as originally filed), 18:22-25 (Claim 11 as issued, Claim 15 as originally filed, reciting in the originally filed claim "wherein a **top surface of the plurality of gate structures** is approximately **co-planar with a top surface of each of the pair of sidewall spacers**").

Accordingly, Pethe discloses spacers 520 that are disposed on two sides of the metal gate (e.g., gate stack structures 308C or 308D) that have a "truncated top surface" under Interpretation 1 because the spacers 520 each have a planar top surface. *See* Section VI.D.1; Ex-03, ¶¶138-142.

Interpretation 2

As previously mentioned, Pethe states that "the spacers may be recessed to be essentially planar with the gate structures." PA-01, 12:22-23. Pethe generally uses the terminology "recessed" to connote that a given feature has been truncated by removing material from the feature's top surface. PA-01, 8:24-51 (explaining trench contacts 310A-310C "may be recessed by...an etch process such as a wet etch process or dry etch process"); *id.* at 13:1-12, FIGs. 3A-3B; Ex-03, ¶143. A POSITA would have understood "recessed" in context of Pethe's teachings and figures is an etching to remove material or a part from the top surface of the trench contacts and (as shown by Pethe) which results in shorter spacers or shorter trench contacts. As understood by a POSITA, Pethe discloses spacers 520 have a "truncated top surface" under Interpretation 2 because spacers 520 were made shorter by removing a part due to the recessing process. *See* §II.D.1.

Interpretation 3

As to interpretation 3, as shown above in the above FIG. 5B structure, the result of recessing spacers 520 is a top surface that is "planar" with the gate stack

structures 308A-308E. Pethe expressly discloses recessing the spacers to be "essentially planar" with gate stack structures 308A-308E, as shown in FIGs. 5A-5B. PA-01, 12:22-23, 17:63-67 (Claim 5 as issued, Claim 9 as originally filed), 18:22-25 (Claim 11 as issued, Claim 15 as originally filed, reciting in the originally filed claim "wherein a **top surface of the plurality of gate structures** is approximately **co-planar with a top surface of each of the pair of sidewall spacers**"). A POSITA would have understood that the top surface of Pethe's spacer 520 in FIG. 5B, indicate a plane and are co-planar with the other structures in the structure of FIG. 5B, and a POSITA would have understood that the recessed spacers were attained by planarization. As discussed in §I.C, a POSITA would have understood that while planarization can be performed in different ways, the intent of planarization processes in the art was to form a planar surface. Ex-03, ¶144. Consistent with Pethe's teachings and a POSITA's state of art knowledge, such recessed spacers are formed by removing material by a planarization process, which results in the planar top surfaces shown in FIGs. 3A-3F, 5A-5B, Ex-03, ¶144.

Thus, Pethe discloses spacers 520 have a "truncated top surface" under Interpretation 3 because a POSITA would have understood Pethe discloses that the spacers 520 were made shorter by removing a part during a recessing process that results in the planar top surface and thus have a "truncated top surface" under

Interpretation 3 (i.e., make shorter by removing a part during a planarization process). *See* §II.D.1.; Ex-03, ¶145.

Thus, Pethe discloses limitation 1(d) under Interpretations 1-3. Ex-03, ¶146.

(6) [1.e] a source/drain region (S/D region) disposed between two metal gates;

Pethe discloses this limitation. Ex-03, ¶¶147-152. Pethe discloses that the semiconductor structure of FIG. 5B includes a source/drain region (S/D region) disposed between two metal gates. Specifically, Pethe's FIG. 5B structure (as well as the structure of FIG. 5A) include diffusion regions of the substrate 302 of the structure, which includes a source/drain region (S/D region) as claimed. Trench contacts 311A-311C in the FIG. 5B structure and trench contacts 310A-310C in FIG. 5A's structure contact the diffusion regions that include **a S/D region** which is **disposed between gate stack structures** 308A-308E (any two being **two metal gates**). *See* PA-01 (Pethe), 12:32-13:12; FIGs. 5A-5B.

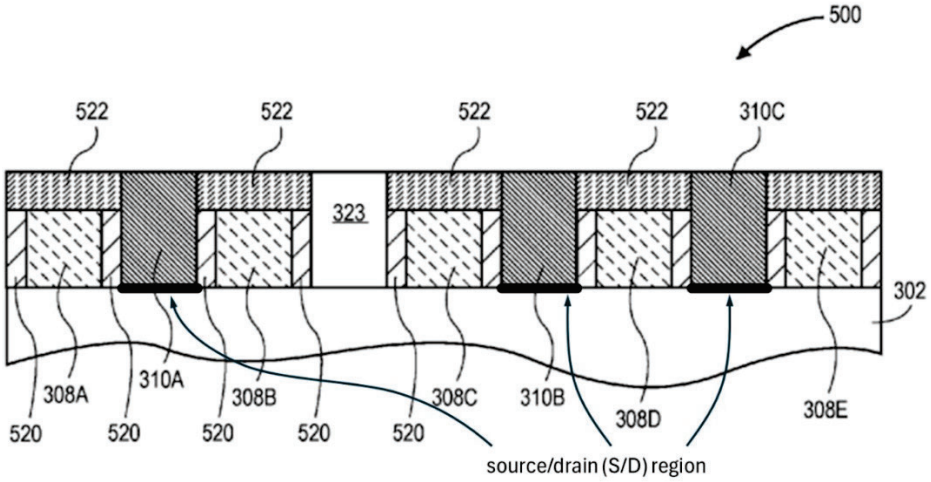


FIG. 5A

PA-01, FIG. 5A (annotated), 12:32-53; Ex-03, ¶148.

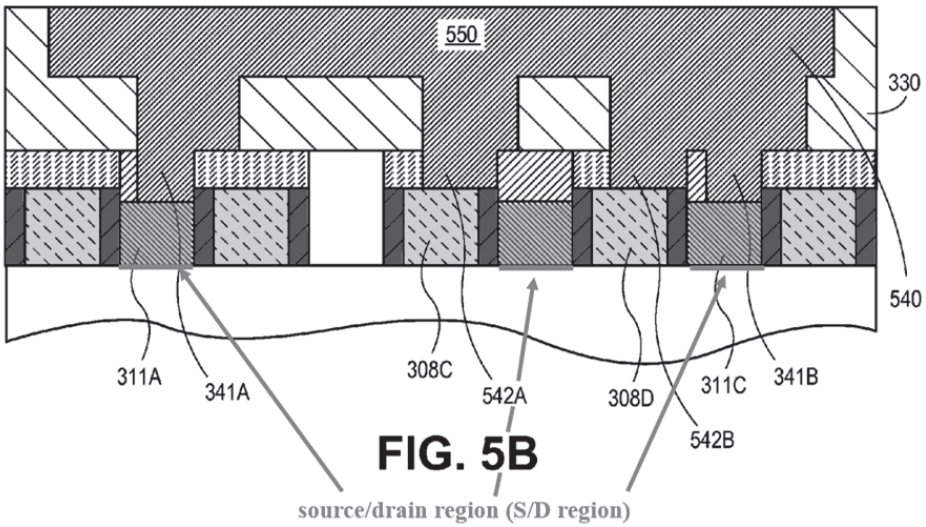


FIG. 5B

PA-01, FIG. 5B (annotated).

Pethe describes trench contacts (e.g., 310, 311) as contacts to diffusion regions, which include source/drain regions. Thus, a POSITA would have understood in Pethe, the trench contacts are contacts to the source/drain regions that are disposed between the gate contact structures (e.g., 308). Ex-03, ¶¶149-150.

Pethe describes "trench contacts, e.g., contacts to diffusion regions of substrate 302, such as trench contacts 310A-310C"." PA-01, 12:42-45, FIG. 5A, which transforms to trench contacts 311A and 311C in the FIG. 5B structure. *Id.*, 12:54-13:9 (describing the same trench contacts 310A-310C), FIG. 5B. *See e.g.*, *id.*, 12:32-13:21, 12:54-67 (describing similar metal contact structure 540 also include portion 550 and "trench contact vias 341A and 341B to trench contacts 311A and 311C"). Pethe also describes that the recessed trench contacts 311A-311C are "contacts to the source to the drain regions of the transistors." *See e.g.*, *id.*, 10:35-36, FIG. 1A; *see also id.*, 3:25-28 ("[**s]ource or drain contacts (also known as trench contacts)**, such as contacts 110A and 110B, **are disposed over source and drain regions of the semiconductor structure** or device 100A"), and 4:33-36 "[s]***ource or drain trench contacts*, such as trench contacts 210A and 210B**, are disposed over **source and drain regions** of the semiconductor structure or device 200A.

Pethe also refers to source/drain regions that are disposed on each side of, or between, gate structures in describing the disclosed invention. *See e.g.*, *Id.*, 15:39-17:19. For example, Pethe describes ("[s]ource and drain regions are disposed in the active region of the substrate, on either side of the portion of the gate structure disposed above the active region"). *Id.*, 15:46-48. *See also id.*, 15:61-66, 16:55-60.

Pethe's teachings are consistent with the source and drain regions as identified in FIG. 1 of the '747 Patent by Patent Owner in its preliminary patent owner response in the IPR proceeding concerning the '747 Patent (although Patent Owner refers to the structure in FIG. 1 and not FIG. 9 of the '747 Patent). *See* Ex-26 (IPR2025-00865, Paper No. 8 (POPR)), 13-14.

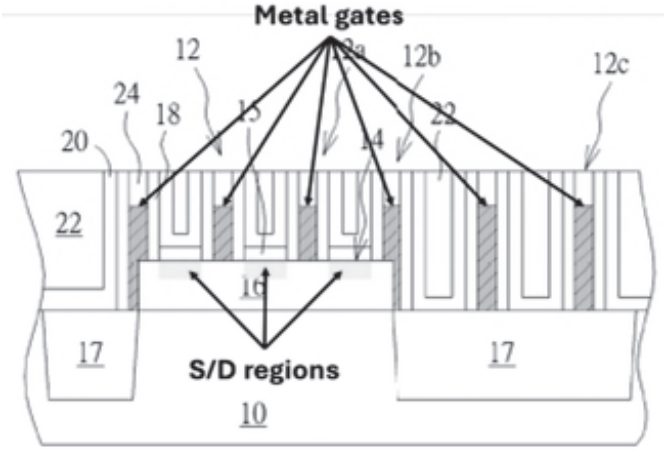


FIG. 1

Ex-26, 14; Ex-03, ¶151.

Therefore, as shown in the annotated FIG. 5B above, the structure in FIG. 5B discloses diffusion regions of substrate (302) that contact trench contacts 311A-311C that include **a source/drain region (S/D region)**, which is **"**disposed between two metal gates" (e.g., gate stack structures 308C/308D, or 308D/308E, or 308A/308B) as claimed in limitation 1(e).

Also, for the same reasons above and to the extent not apparent from Pethe's disclosures, a POSITA would have understood Pethe to necessarily disclose a **source/drain region (S/D region) "**disposed between two metal gates" (e.g., gate

stack structures 308C/308D, or 308D/308E, or 308A/308B) as claimed in limitation 1(e). A POSITA would have understood that to have an operable transistor device as described by Pethe, such a source/drain region would be necessarily included in the semiconductor structure of FIG. 5B, especially given the disclosures Discussed above in Pethe. Ex-03, ¶152.

(7) [1.f] a plurality of first contacts disposed in the first dielectric layer that are electrically connected to parts of the S/D region;

Pethe discloses this limitation. Ex-03, ¶¶153-161. Pethe discloses that the semiconductor structure of FIG. 5B includes a plurality of first contacts disposed in the first dielectric layer (limitation 1(b)) that are electrically connected to parts of the S/D region (limitation 1(e)). For example, Pethe's FIG. 5B structure includes trench contact vias 341A and 341B ("**a plurality of first contacts**") that are disposed in the dielectric layer (of which region 323 is a part of) ("**first dielectric layer**") and also are electrically connected to the source/drain regions of the diffusion area on substrate 302, as shown in the annotated FIG. 5B below. *See* PA-01, 12:54-67.

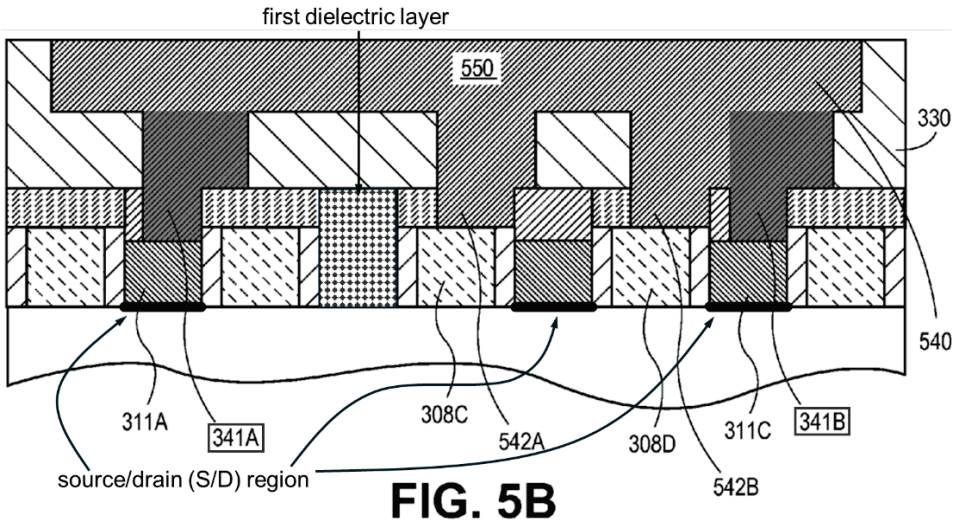
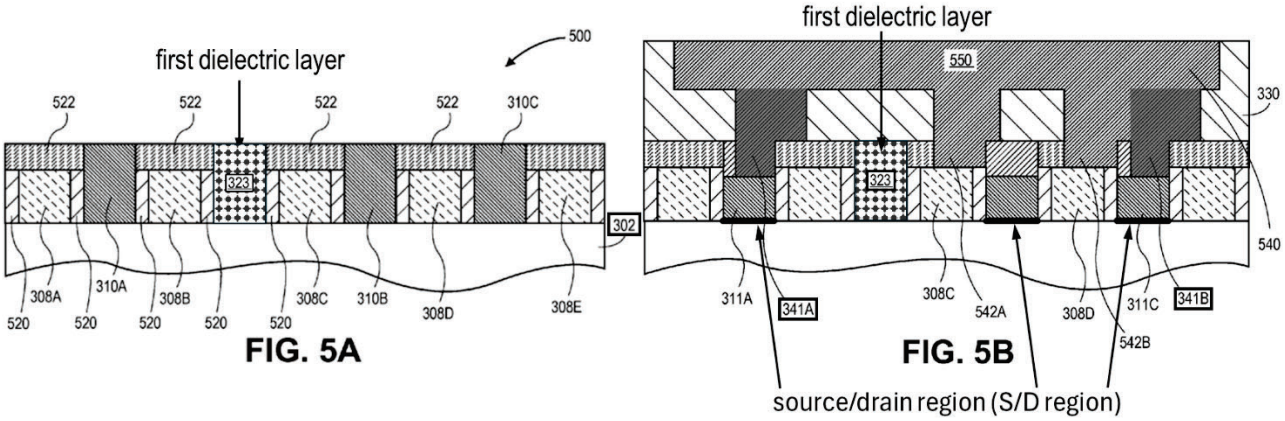


FIG. 5B

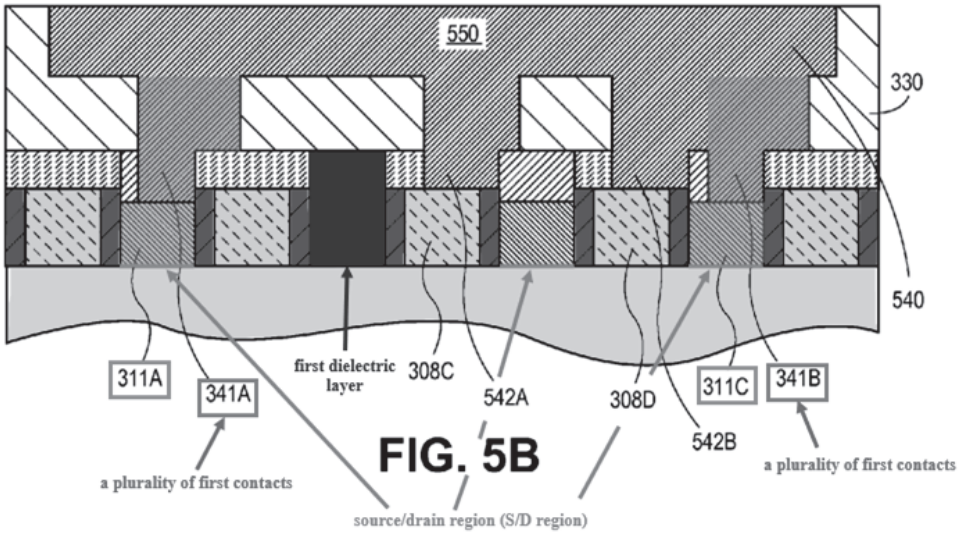
PA-01, 12:54-67; Ex-03, ¶154.

As shown, trench contact vias 341A, 341B are disposed in the first dielectric layer (of which region 323 is a part). *See* §VI.A.1(a)(4).



Pethe describes trench contacts vias 341 when forming the metal contact structure 340 (which is similar to metal contact structure 540 in FIG. 5B) (PA-01, 11:23-31 ("a metal contact structure 340 is formed in…via openings 336")), and uses similar language to describe the same trench contact vias 341 in FIG. 5B (*id.*, 12:54-62). Pethe's trench contact vias 341A, 341B correspond to trench contacts

311A, 311C, respectively and thus are electrically connected to those contacts, respectively. *Id.*,12:54-67, 11:23-29 ("metal contact structure 340 includes…trench contact vias (e.g., trench contact vias 341A and 341B to trench contacts 311A and 311C, respectively)"). *See also id.*, 9:29-10:36; 12:15-13:19.



PA-01, FIG. 5B (annotated). Ex-03, ¶¶155-158.

Trench contacts 311A, 311C are contacts to source and drain regions in the diffusion regions of substrate 302 (see limitation 1(e)). Accordingly, in such context, by disclosing "trench contact vias 341A and 341B to trench contacts 311A and 311C, respectively," a POSITA would have understood Pethe discloses trench contact vias 341A, 341B being **electrically connected** to the source and drain regions through the trench contacts 311A, 311C, which are contacts to such S/D regions. Likewise, trench contact vias 341A, 341B are **electrically connected** to **parts of the** source and drain regions, as shown above in the annotated FIG. 5B. *See*

also Ex-01 ('747 Patent), FIGs. 1-9, 2:39-46 (source/drain region 14 on fin structure 16); Ex-03, ¶159.

Pethe's teachings are consistent with the first contacts as identified in the '747 Patent as identified by Patent Owner in its preliminary patent owner response in the IPR proceeding concerning the '747 Patent. *See* Ex-26, 18-19.

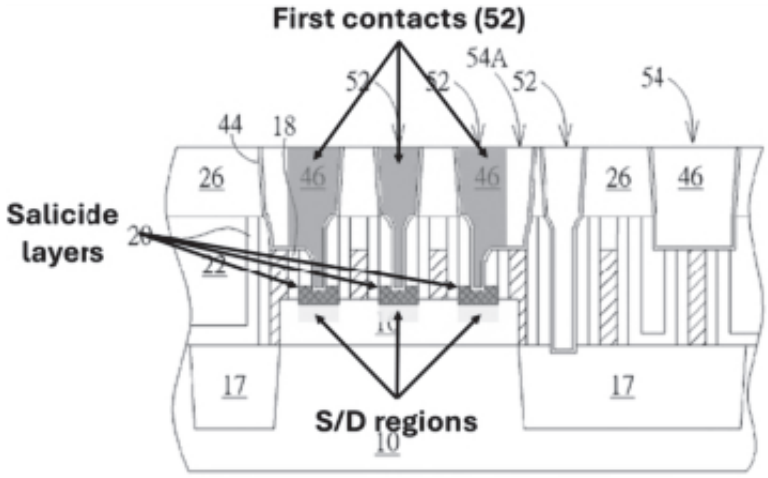


FIG. 8

Ex-26, 19 (annotated); Ex-03, ¶160.

Therefore, as shown in the above annotated FIG. 5B, the structure in FIG. 5B includes **a plurality of first contacts** (e.g., trench contact vias 341A, 341B) **disposed in the first dielectric layer** (e.g., dielectric layer (of which region 323 is a part of) **that are electrically connected to parts of the S/D region** (e.g., source and drain regions in diffusion regions of substrate 302), as claimed in limitation 1(f). Ex-03, ¶161.

(8) [1.g-1] a plurality of second contacts disposed in the first dielectric layer that are electrically connected to one of the metal gates,

Pethe discloses this limitation. Ex-03, ¶¶162-178. Pethe discloses that the semiconductor structure of FIG. 5B includes a plurality of second contacts disposed in the first dielectric layer (limitation 1(b)) that are electrically connected to one of the metal gates (limitation 1(c)), wherein at least one of the first contacts (limitation 1(f)) directly connects at least one of the second contacts, as claimed in limitation 1(g).

Pethe discloses "a plurality of second contacts disposed in the first dielectric layer." For example, Pethe discloses gate contact vias 542A, 542B that are to gate stack structures 308C, 308D, respectively. Ex-03, ¶163.

Pethe explains for the FIG. 5B structure that metal contact structure 540 is formed that includes a metal (0) portion 550 and "gate contact vias (e.g., gate contact vias 542A and 542B to gate stack structures 308C and 308D, respectively)". *Id.*, 12:54-62, FIG. 5B.

As shown in the annotated FIG. 5B below, gate contact vias 542A, 542B are disposed in the dielectric layer (of which region 323 is a part of), and thus the structure includes a "plurality of second contacts disposed in the first dielectric layer" as claimed. Ex-03, ¶¶164-165.

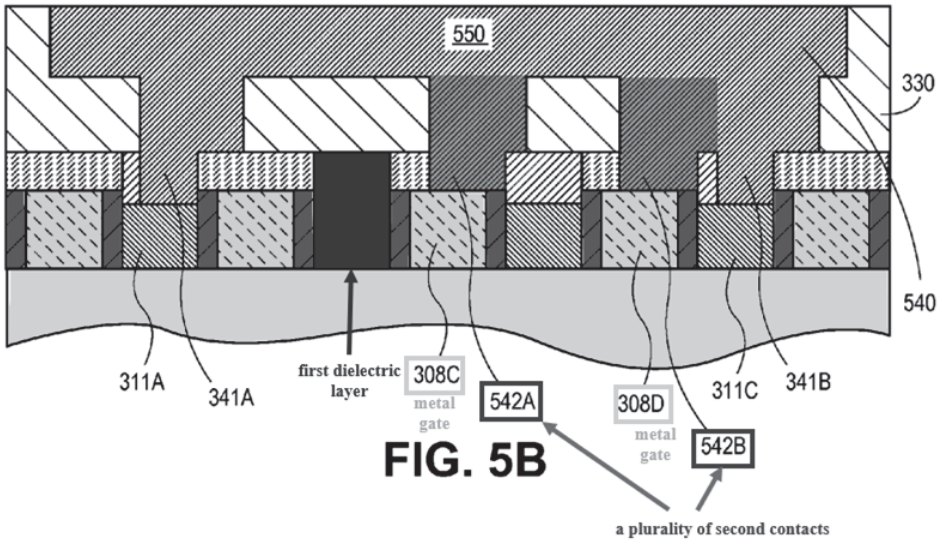


FIG. 5B

PA-01, FIG. 5B (annotated).

Pethe also discloses that the "plurality of second contacts" are "electrically connected to one of the metal gates."

As explained above, it is assumed for purposes of prior art analysis that such claim features at least encompass and are met in the same or similar way that the '747 Patent discloses its semiconductor structure (e.g., where the structure of FIG. 9 simply shows single second contacts 54 connected to individual metal gates 12 with no other discussion of multiple second contacts 54 being electrically connected to a single metal gate). In doing so, Requester does not agree that the '747 Patent adequately discloses or enables the claimed features in limitation 1(g) or does so in such a way that a POSITA could reasonably ascertain the scope of the claimed invention. Ex-03, ¶¶166-167. Under this assumption, Pethe discloses the claimed "plurality of second contacts" that are "electrically connected to one of the metal

gates" in a manner similar to the way that the '747 Patent discloses its semiconductor structure (e.g., where the structure of FIG. 9 simply shows single second contacts 54 connected to individual metal gates 12 with no other discussion of multiple second contacts 54 being electrically connected to a single metal gate). *See, e.g.*, Ex-01 ('747 Patent), FIGs. 8-9, 5:1-6:37; PA-01 (Pethe), FIG. 5B (annotated above), 12:54-13:19. Just like the '747 Patent, Pethe's FIG. 5B structure includes multiple second contacts (e.g., gate contact vias 542A, 542B) that are electrically connected to a respective metal gate (e.g., gate stack structures 308C, 308D). A POSITA would have understood that gate contact vias 542A, 542B provide an electrical connection to the metal gates that are included in gate stack structures 308C, 308D. *Id.*, ¶167.

For instance, in the FIG. 5B structure, gate contact via 542A is electrically connected to 308C (one of the metal gates), and gate contact via 542B is electrically connected to 308D (one of the metal gates), and thus the plurality of second contacts...are electrically connected to one of the metal gates similar to that in the '747 Patent. *See* PA-01, 12:54-67. *See also id.*, 11:23-31 (Pethe discussing gate contact vias in connection with FIGs. 3A-3F), 10:52-11:22 (describing opening 338 that when filled to form gate contact vias 342A and 342B) to gate stack structures 308C and 308D "form the gate contact on active regions of the transistor." Thus, gate contact via 342A is electrically connected to gate stack structure 308C (one of the metal gates), and gate contact via 342B is electrically connected to gate stack

structure 308D (one of the metal gates) (*see e.g.*, *id.* at 11:23-31), and thus Pethe discloses "a plurality of second contacts...are electrically connected to one of the metal gates" in a manner similar to the way that the '747 Patent discloses its semiconductor structure with second contacts 54 and metal gates 12 only showing single second contact with a respective metal gate 12. Ex-03, ¶168.

Pethe's teachings and Requester's arguments above are consistent with representations by Patent Owner regarding this claim feature in the '747 in its preliminary patent owner response in the IPR proceeding concerning the '747 Patent. *See* Ex-26 (IPR2025-00865, Paper No. 8), 19-20 (stating that "a set of second contacts 54 (annotated below in purple) that are 'electrically connected to parts of the metal gate 12'")[11].

[11] Requester notes that the limitation does not recite "parts of the metal gate" but rather "one of the metal gates." Also, Applicant distinguished "one of the metal gates" from "parts of the metal gate" by removing the language when adding the claimed feature to claim 1 during prosecution. Nonetheless, Patent Owner's representations support Requester's arguments that Pethe discloses the claimed "a plurality of second contacts…electrically connected to one of the metal gates" in limitation 1(g) in the same way as described by thee '747 Patent.

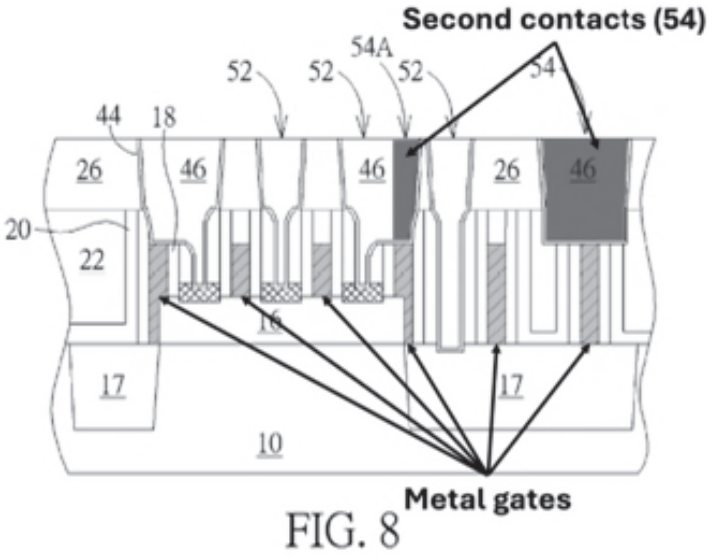


FIG. 8

Ex-26, FIG. 8 (annotated). Ex-03, ¶169.

Additionally, Pethe discloses that gate contact vias 542A, 542B (a plurality of second contacts) that are connected to one of the gate stack structures 308C, 308D (one of the metal gates). For instance, as explained, the structure of FIG. 5B includes a **metal** contact structure 540 that includes **metal** (0) trench 550 that is conductive to gate contact vias 542A, 542B, which are "to gate stack structures 308C and 308D, respectively". PA-01, 12:54-62, FIG. 5B, 11:32-42. As such, each gate contact via 542A, 542B is electrically connected to a respective one of gate stack structures 308C, 308D by the conductive metal (0) trench 550 in the metal contact structure 540, which as shown, are connected. Thus, for this additional reason, Pethe discloses "a plurality of second contacts" that are "electrically connected to one of the metal gates" as claimed in limitation 1(g). Ex-03, ¶170.

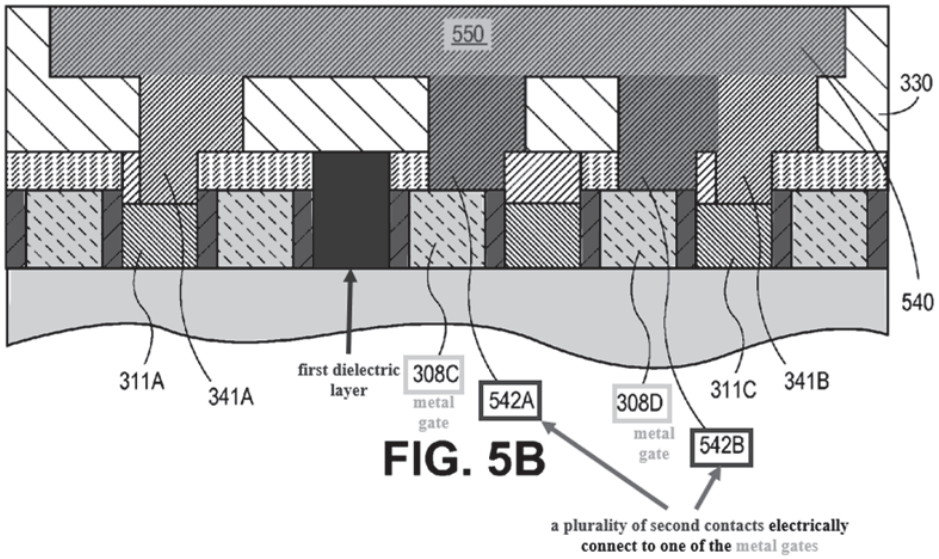


FIG. 5B

PA-01, FIG. 5B (annotated).

[1.g-2] wherein at least one of the first contacts directly connects at least one of the second contacts; and

Pethe also discloses that the structure of FIG. 5B includes "at least one of the first contacts directly connects at least one of the second contacts" as recited in limitation 1(g) under Interpretation 4 for "directly connects" (i.e., "at least one of the first contacts connects with at least one of the second contacts with no intervening layer or material therebetween"). *See* §VI.D.2; Ex-03, ¶171.

As explained above, Pethe's FIG. 5B structure includes metal contact structure 540, which includes metal (0) portion 550 and trench contact vias 341A, 341B and gate contact vias 542A, 542B that are connected to gate stack structures 308C and 308D, respectively. PA-01, 12:54-62. Pethe explains how the metal contact structure and its metal (0) portion and trench and gate contact vias are

formed. Namely, the formation of gate contact vias 542 share the same processes of formation as gate contact vias 342 (same feature but deeper only because of recessed spacers 520). PA-01, 12:54-67 (Figure 5B's structure "[i]n comparison to the structure described in association with FIG. 3F" is just "slightly different since the spacers 522 are not exposed, yet coverage of the insulating cap layers 522 is extended, during etch formation of the via openings leading to gate contact vias 542A and 542B"); Ex-03, ¶172.

Pethe explains "a metal contact structure 340 is formed in…via openings… 338" and that "metal contact structure 340 includes…gate contact vias (e.g., gate contact vias 342A and 342B to gate stack structures 308C and 308D, respectively)." PA-01, 11:23-31. Indeed, gate contact vias 342A/342B comprise metal that fill openings 338 shown in Figure 3E below (black arrows).

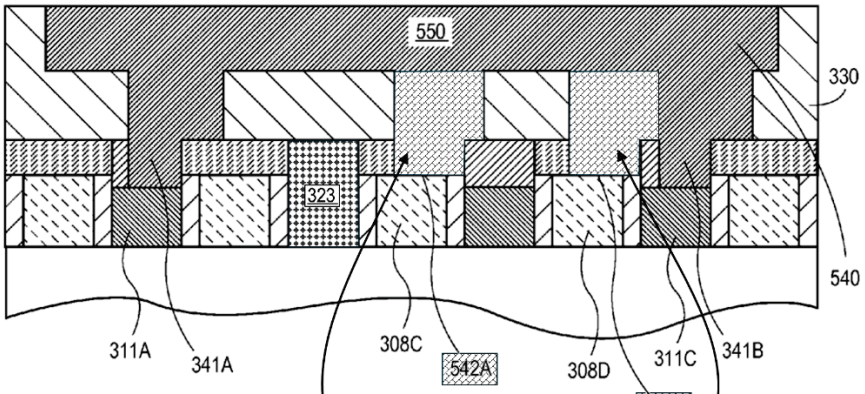


FIG. 5B

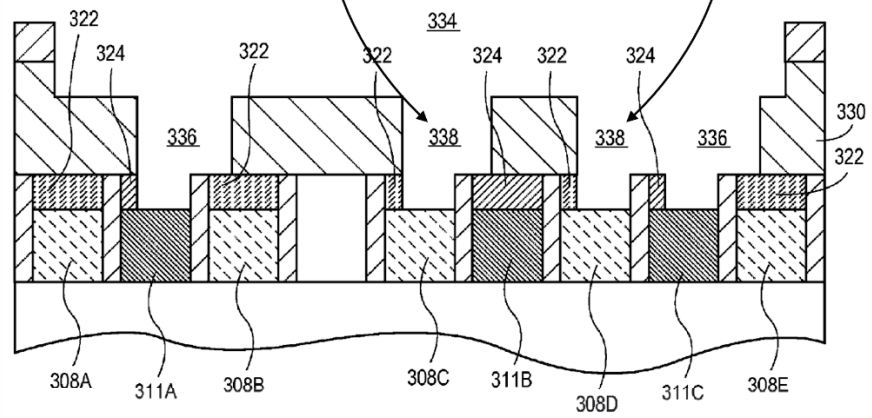


FIG. 3E

PA-01, 11:23-31, 10:37-11:22; Ex-03, ¶173.

Pethe explains metal (0) trench 334, via openings 338, and via openings 336 are formed by etching. PA-01 (Pethe), 9:1-11:22. A single metal deposition (i.e., "of a fill metal layer") fills all three regions, by which metal (0) trench 334 is filled with metal (0) portion 350, gate contact vias 342 fill via openings 338, and trench contact vias 341 fill via openings 336. *Id.*, 11:23-42. Thus, Pethe discloses gate contact vias 542 (**at least one of the first contacts**) directly gate contact via 342B

(**at least one of the second contacts**) with no intervening layers or other barriers in the Figure 5B structure.

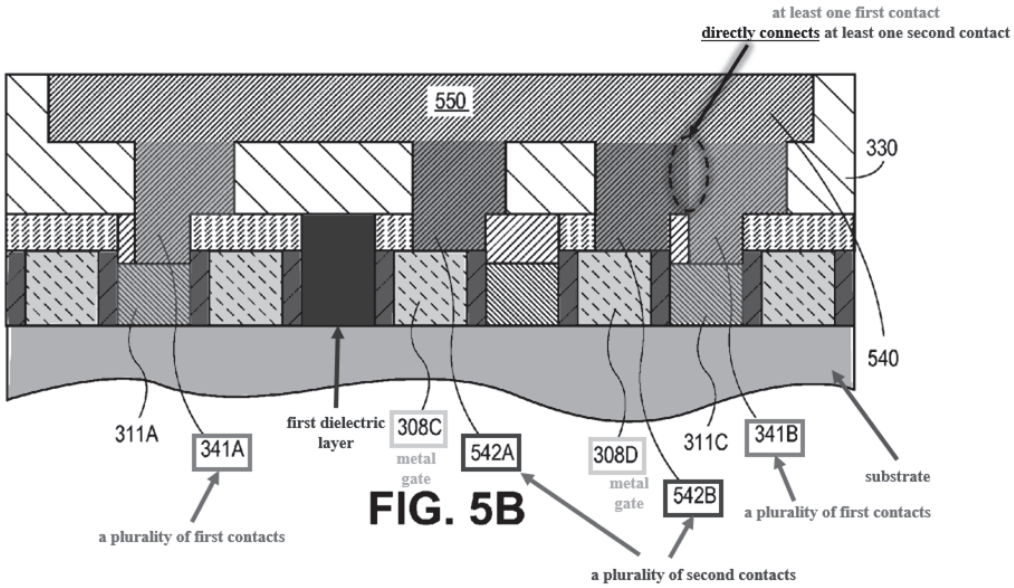


FIG. 5B

Id., FIG. 5B (annotated); 12:54-67; Ex-03, ¶174.

Thus, a POSITA would have understood that by forming metal contact structure 540 in this manner (e.g., metal deposition of a metal fill layer including conductive material) (limitation 1(g)), gate contact via 542B and trench contact via 341B "directly connects" gate contact via 542B. Ex-03, ¶175. Accordingly, the structure of FIG. 5B includes a plurality of first contacts (e.g., trench contact vias 341A/341B; *see* limitation 1(f)) and a plurality of second contacts (e.g., gate contact vias 541A/542B; *see* limitation 1(g)), where "at least one of the first contacts directly connects at least one of the second contacts" (e.g., trench contact via 341B directly connects gate contact via 542B). Further, since trench contact via 341B connects to

gate contact via 542B without any intervening material or layer between them, Pethe's FIG. 5B structure discloses the claimed "at least one of the first contacts **directly connects** at least one of the second contacts" under Interpretation 4 (*see* §§II.D.2, III.A). Ex-03, ¶175.

Pethe's disclosure is similar to the shared contact feature described in the '747 Patent. For instance, the '747 Patent describes the configuration in FIG. 8 (and carried over to FIG. 9) where first and second contacts are formed simultaneously using a metal layer 46 that fills trenches 32 and 42 much like the process described by Pethe. *See* Ex-01 ('747 Patent), 5:1-30; *see also id.*, 5:31-6:37, FIGs. 8-9. Ex-03, ¶176. As exemplified below, the "shared contacts" formed from one second contact 54 and one first contact 52 is similar to the shared contact formed by gate contact via 542B and trench contact via 341B in Pethe's FIG. 5B structure.

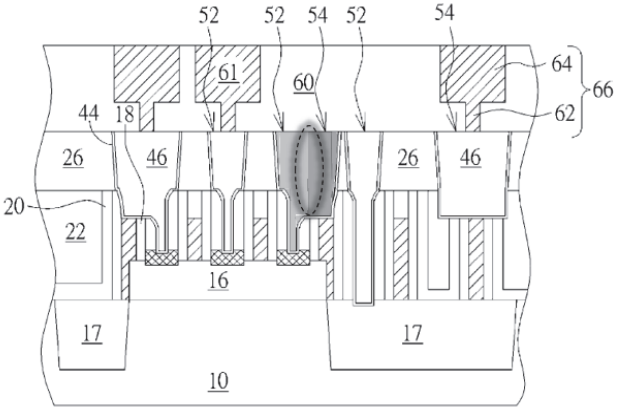


FIG. 9

'747 Patent at FIG. 9 (annotated)

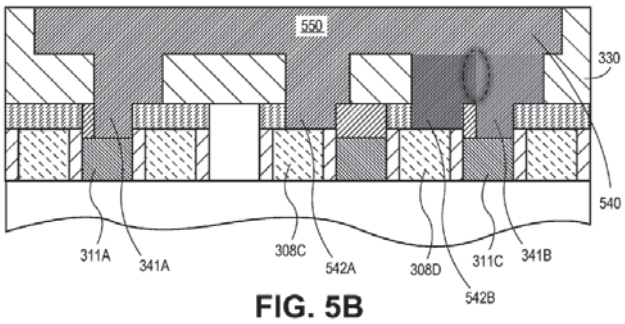
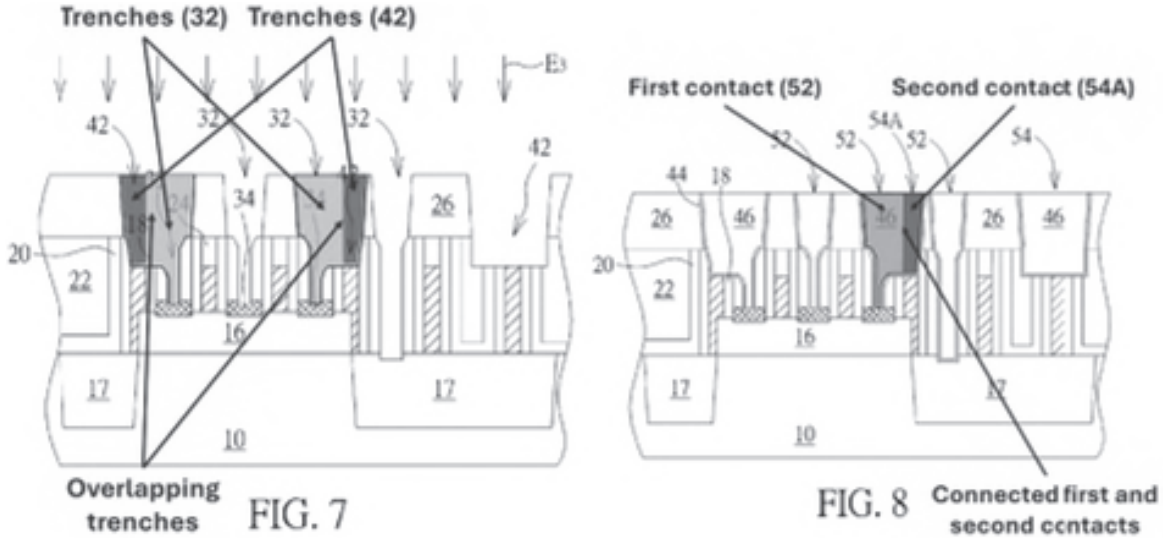


FIG. 5B

Pethe at FIG. 5B (annotated)

Pethe's teachings concerning the '747 Patent's shared contact are nearly identical with a first contact that directly contacts a second contact in the '747 Patent as identified by Patent Owner in its preliminary patent owner response in the IPR proceeding concerning the '747 Patent. *See* Ex-26 (IPR2025-00865, Paper No. 8), 20-21 (stating that "when these trenches are filled to create their respective first contact 52 and second contact 54, part of that first contact is connected to at least part of the second contact, 'such as the second contact 54A'"). Ex-03, ¶177.



Ex-26, 21 (annotated).

Therefore, for the reasons above and as shown in the above annotated FIG. 5B, the structure in FIG. 5B includes "**a plurality of second contacts** (e.g., gate contact vias 542A/542B) **disposed in the first dielectric layer** (e.g., Pethe's first dielectric layer (of which region 323 is a part of) **that are electrically connected to one of the metal gates** (e.g., gate stack structures 308C and/or 308D; *see* discussion

above for this feature of limitation 1(g)) **wherein at least one of the first contacts** (e.g., trench contact vias 341B) **directly connects** (no intervening material or layer) **at least one of the second contacts** (e.g., gate contact vias 542B)," as claimed in limitation 1(g). Ex-03, ¶178.

(9) [1.h] a hard mask disposed on one of the metal gates, wherein the top surface of the hard mask and the top surface of the first dielectric layer are on the same level.

Pethe discloses this limitation. Ex-03, ¶¶179-187. Pethe discloses that the semiconductor structure of FIG. 5B includes "a hard mask disposed on one of the metal gates[12], wherein the top surface of the hard mask and the top surface of the first dielectric layer are on the same level," as claimed in limitation 1(h). Ex-03, ¶179.

For example, Pethe explains that in the structure of FIG. 5A, "an insulating cap layer 522 is disposed on the gate stack structures 308A-308E (e.g., GILA), as is also depicted in Figure 5A." PA-01, 12:45-48, FIG. 5A (below); Ex-03, ¶180. Additionally, although unlabeled, a POSITA would have understood that the same

[12] For purposes of analysis concerning the prior art (here and in the other proposed rejections discussed below), Requester assumes the term "disposed on **two sides of one of the metal gates**" refers to any of the metal gates that are included in the claimed semiconductor structure. Pethe discloses the "hard mask" as recited in limitation 1(h).

insulating cap layer 522 is included in the structure of FIG. 5B, but narrower in some regions to accommodate the formation of the metal contact structure 540, including the trench contact vias 341, gate contact vias 542, as shown below. PA-01, 12:54-67, FIG. 5B (below); Ex-03, ¶181.

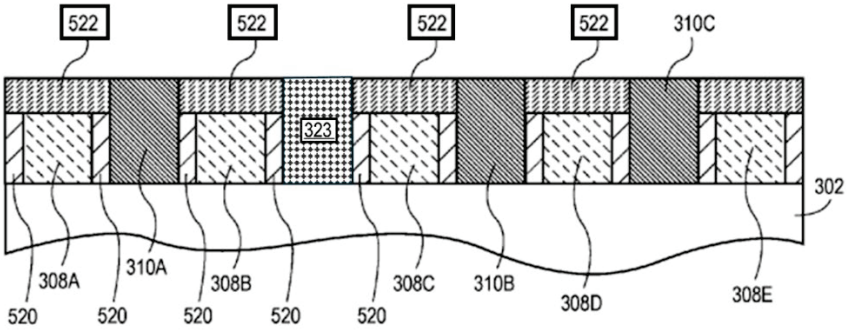


FIG. 5A

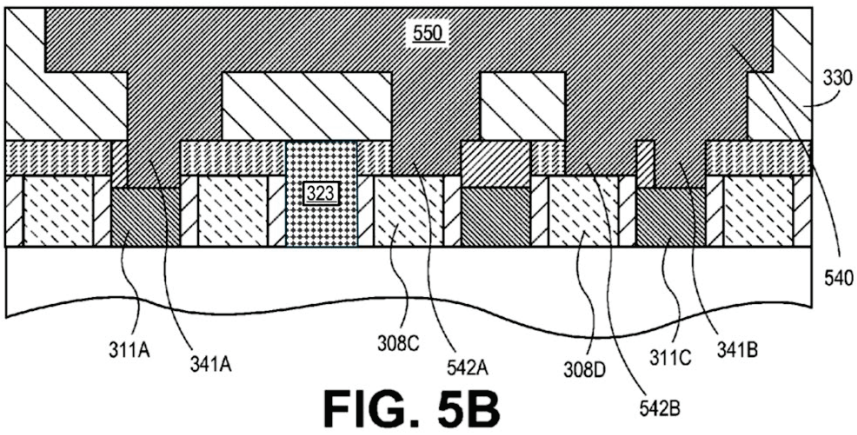


FIG. 5B

PA-01, 12:45-67; Ex-03, ¶181.

Pethe explains that because of the use of recessed spacers 520, the "**insulating cap layers 522** cover the spacers 520 associated with each gate stack, and well as **covering the gate stack**." PA-01, 12:48-53. Pethe explains that an insulating (or dielectric) cap layer disposed on metal gate is "for protecting a metal gate electrode."

Id., 3:48-50 (discussing FIG. 1B where "a dielectric cap layer 154 may be disposed on the gate electrode, e.g., a dielectric cap layer for protecting a metal gate electrode"), 3:67-4:1 (dielectric cap layer of Figure 1C), 4:54-56 (discussing FIG. 2B where "a dielectric cap layer 254 may be disposed on the gate electrode, e.g., a dielectric cap layer for protecting a metal gate electrode"), 5:6-7 (dielectric cap layer 254 of FIG. 2C).) Ex-03, ¶182.

Accordingly, Pethe discloses that the FIG. 5B structure includes "**a hard mask**" (e.g., insulating cap layer 522) that is "**disposed on one of the metal gates**" (e.g., gate stack structures 308A-308E; for example, one of gate stack structure 308C or gate stack structure 308D) as claimed in limitation 1(h). Ex-03, ¶183.

Pethe also discloses that the hard mask (e.g., insulating cap layer 522 disposed over, e.g., gate stack structures 308A-308E; such as for example, one of gate stack structure 308C or gate stack structure 308D) has a "top surface" that is "on the same level" as "the top surface of the first dielectric layer" (Pethe's dielectric layer (of which region 323 is a part of) as claimed in limitation 1(h). For instance, as shown in FIG. 5B (annotated below), insulating cap layer 522 ("hard mask") has a top surface on the same level as the top surface of region 323.

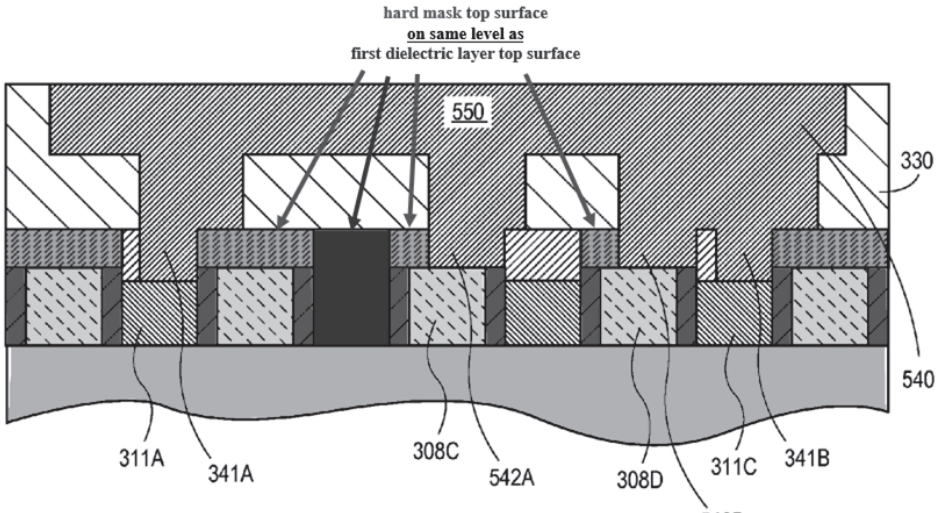


FIG. 5B

PA-01, FIG. 5B (annotated); Ex-03, ¶184.

Based on Pethe's disclosures, a POSITA would have understood that insulating cap layer 522 to have a top surface on the same level as the top surface of Pethe's dielectric layer (of which region 323 is a part of) is consistent with limitation 1(h) of the '747 Patent. Ex-03, ¶185. For instance, Pethe teaches in connection with FIG. 3B that a planarization process (CMP) is performed on cap layer 324, which is conformally deposited over the "entire structure." PA-01, 8:44-51. A POSITA would have thus understood that Pethe's dielectric layer (of which region 323 is a part of), along with insulating cap layers 322 and 324 (and likewise insulating cap layers 522 and Pethe's dielectric layer (of which region 323 is a part of) in the Figure 5B embodiment) would have been planarized during the CMP process that a POSITA would have understood results in the structures as shown in FIG. 3F (e.g., cap layer 322 and region 323) having top surfaces on the same level. Ex-03, ¶185.

Pethe explains that the planarization (e.g., CMP) over the entire structure results in insulating cap layer 324 to be "**only** above 310A-310C," and "**re-expos[es]** spacers 320 and insulating cap layer 322." PA-01, 8:37-51. A POSITA would have understood the same processes and result is applicable to the fabrication of structure of FIG. 5B (where cap layer 522 and region 323 also have respective top surfaces on the same level) for reasons explained above. *See e.g., id.*, 12:15-13:19, FIGs. 5A-5B; Ex-03, ¶185.

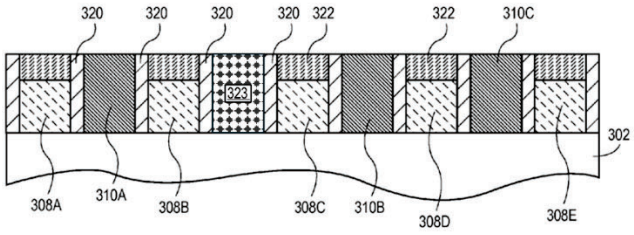


FIG. 3A

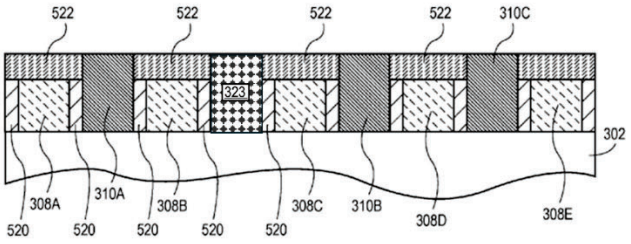


FIG. 5A

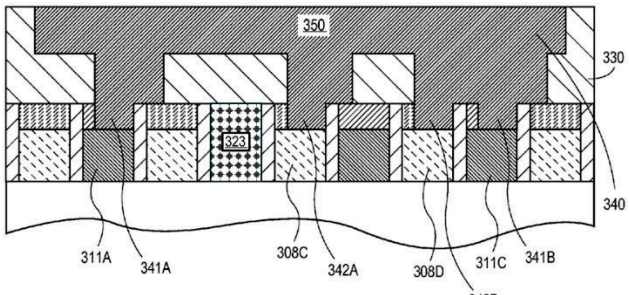


FIG. 3F

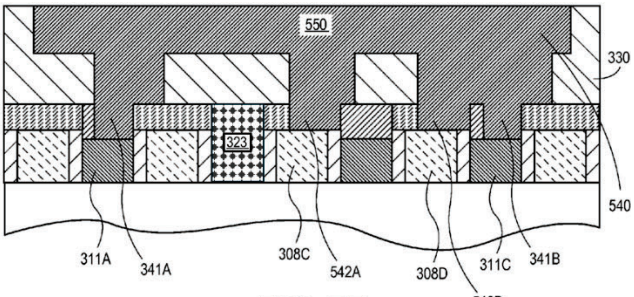


FIG. 5B

PA-01, FIGs. 3A, 3F, 5A-5B (all annotated).

Therefore, for the reasons above and as shown FIG. 5B, the structure in FIG. 5B includes "**a hard mask** (e.g., insulating cap layer 522) "**disposed on one of the metal gates**" (e.g., gate stack structures 308A-308E; such as for example, one of gate stack structure 308C or gate stack structure 308D), "**wherein the top surface**

of the hard mask (e.g., insulating cap layer 522) **and the top surface of the first dielectric layer** (e.g., Pethe's first dielectric layer (of which region 323 is a part of)) **are on the same level**, as claimed in limitation 1(h). Ex-03, ¶186.

In light of the teachings in Pethe above, Pethe anticipates claim 1 and thus the claim is invalid. Ex-03, ¶187.

b. Claim 2: The semiconductor device of claim 1, further comprising a second dielectric layer disposed on the first dielectric layer. [13]

Pethe discloses this limitation. Ex-03, ¶¶188-192. Pethe discloses the structure of Figure 5B including a second dielectric layer disposed on the first dielectric layer. Specifically, Pethe discloses "[r]eferring to FIG. 5B, a metal contact structure 540 is formed in a metal (0) trench and via openings formed in a **dielectric layer 330**." PA-01 (Pethe), 12:54-56. As shown in the annotated Figure 5B below, dielectric layer 330 is disposed on Pethe's dielectric layer (of which region 323 is a part of) (*see* §VI.A.1(a)(5)). *See also id.*, 12:54-67. Ex-03, ¶189.

[13] Claim 1 does not recite a "semiconductor device." However, Requester assumes claims 2-9 refer to the semiconductor "structure" recited in claim 1.

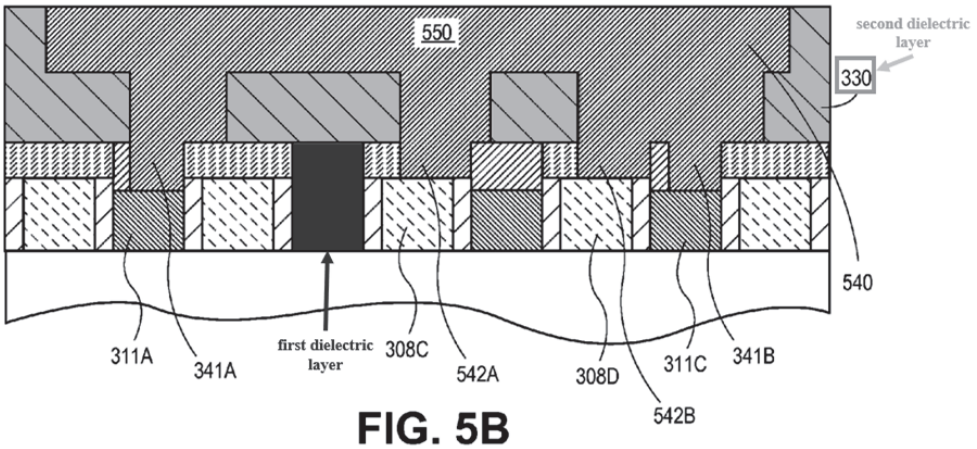


FIG. 5B

PA-01, FIG. 5B (annotated).

Pethe discusses dielectric layer 330 in connection with FIGs. 3A-3F (although Pethe does not repeat its discussion of 330 for FIGs. 3C-3F to describe the similarly labeled element in FIG. 5B). Namely, Pethe explains "Referring to FIG. 3C, an inter-layer dielectric (ILD) 330 and hardmask 332 stack is formed and patterned to provide, e.g., a metal (0) trench 334 patterned above the structure of FIG. 3B." *Id.*, 9:1-43 (ILD 330 "may be composed of a material suitable to electrically isolate metal features"), FIGs. 3F, 5B (comparatively shown below); Ex-03, ¶190.

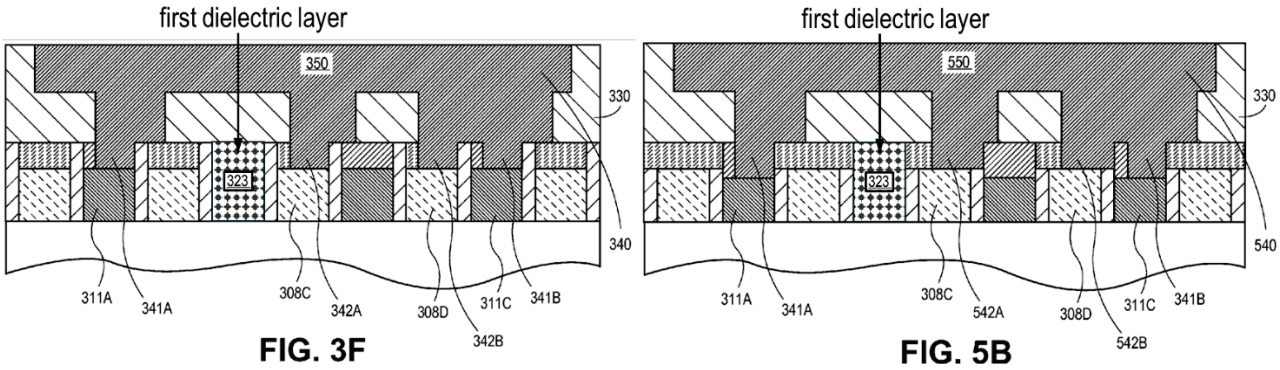


FIG. 3F FIG. 5B

PA-01, FIGs. 3F, 5B (both annotated).

Therefore, the structure in FIG. 5B includes "**a second dielectric layer** (e.g., inter-layer dielectric (ILD) 330) **disposed on the first dielectric layer** (e.g., Pethe's dielectric layer (of which region 323 is a part of)," as claimed in claim 2. Pethe therefore discloses Claim 2, and thus the claim is invalid. Ex-03, ¶¶191-192.

c. Claim 3: The semiconductor device of claim 2, further comprising an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface.

Pethe discloses these limitations. Ex-03, ¶¶193-204. Pethe discloses the structure of FIG. 5B includes an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface as recited in claim 3.[14]

Pethe discloses forming an insulating cap layer 324 that is etched to form via openings 336 that are filled to form trench contact vias 341A/341B to the source and drain region. *See* PA-01, 9:36-43; *see also* §VI.A.1(a)(9). Insulating cap layer 324 may be composed of the same material as CESL 20 in the '747 Patent (i.e., "silicon

[14] For purposes of analysis concerning the prior art (here and in the other proposed rejections discussed below), Requester assumes the term "disposed on two sides of **the metal gate**" refers to any of the metal gates that are included in the claimed semiconductor structure. As explained below, Pethe discloses that insulating cap layer 324 is disposed on two sides of gate stack structure 308D, which is a non-limiting example of the claimed "the metal gate" recited in claim 3.

nitride). *See* Ex-01 ('747 Patent), 3:19-21 ("CESL 20…mainly comprise silicon nitride"), 5:4-7; *see also* PA-01 (Pethe), 10:16-36, FIG. 5B[15]. Ex-03, ¶195.

Pethe discloses how insulating cap layers 322, 324 are involved in the selective etching processes to form openings 336 and 338, that are used to form the contact vias to the metal gates and source drain region in the semiconductor structure of FIG. 3F (and likewise in the structure of FIG. 5B). *See* PA-01, 9:29-10:34 (FIG. 3D, opening 336 formation), 10:35-11:22 (FIG. 3E, opening 338 formation), 11:23-42 (FIG. 3F, contact via formations). *See also id.*, 12:15-17 ("In the process flow, described in association with FIGS. 3A-3C, the tops of the spacers 320 are exposed during via opening formation in cap layers 324 and 322"). Ex-03, ¶196.

A POSITA would have thus understood insulating cap layer 324 is an **etching stop layer** given it protects specific portions of the semiconductor structure during the selective etching processes performed to form openings 338. Ex-03, ¶198.

While not labeled in FIG. 5B, a POSITA would have also understood that the FIG. 5B structure includes insulating cap layer 324, which is selectively etched (along with insulating cap layer 322) during fabrication processes disclosed by Pethe to form the openings 336 and 338 that are used to form the trench contact vias 341

[15] A POSITA would have understood Figure 5B's structure has undergone the fabrication steps of Figures 3B-3E. PA-01, 12:22-53.

and gate contact vias 342/542 in the FIG. 5B structure. Ex-03, ¶197. A POSITA would have understood Pethe discloses the structure of FIG. 5B includes insulating cap layer 324.

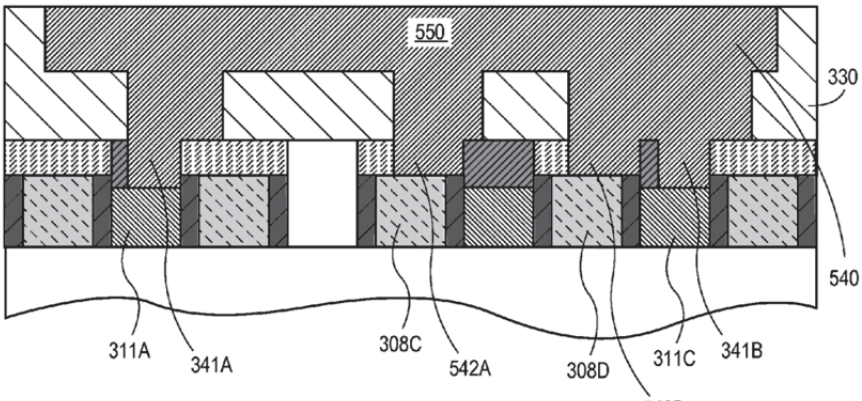


FIG. 5B

PA-01, FIG. 5B (annotated).

Given Pethe's disclosures, a POSITA would have understood that the insulating cap layer 324 in the FIG. 5B structure is formed and is similar to insulating cap layer 324 in the FIG. 3F structure. Moreover, a POSITA would have understood that insulating cap layer 324 in the FIG. 5B structure, like the same layer in the FIG. 3F structure, is a **contact etching stop layer** because it is a layer that protects a specific portion of the structure during the selective etching process disclosed by Pethe to form opening 338, that is subsequently filled to form the gate contact vias 542A/542B in the FIG. 5B structure. *Id.*, 10:37-11:22, 12:15-17. Ex-03, ¶198.

A POSITA would have understood similar selective etching processes is performed to form the opening 338 that is used to form gate contact vias 542 in the

FIG. 5B structure. *See* PA-01, FIG. 5B (showing gate contact vias 542A/542B). Similarly, insulating cap layer 324 in FIG. 5B is an **etching stop layer** and is **disposed on two sides of the metal gate** (e.g., the metal gate in gate stack structure 308D) as shown in the annotated FIG. 5B above.

Pethe's insulating cap layer 324 in the FIG. 5B structure discloses an etching stop layer disposed on two sides of the metal gate, where the etching stop layer has a "truncated top surface" as recited in claim 3 under Interpretations 1-3. *See* §§III.A, II.D.1. Ex-03, ¶¶199-200.

As shown in FIG. 5B, the insulating cap layer 324 has a planar top surface. A POSITA would have understood that insulating cap layer 324 has a planar top surface (consistent with Interpretation 1) because Pethe explains that "insulating cap layer 324 is formed by a chemical vapor deposition (CVD) process as a **conformal layer above the entire structure**" and that "the conformal layer is then **planarized, e.g., by chemical mechanical polishing (CMP)**, to provide insulating cap layer 324 material only above trench contacts 310A-310C, and re-exposing spacers 320 and insulating cap layer 322." *Id.*, 8:44-51; Ex-03, ¶201.

A POSITA would have understood that the removal of the top portion of insulating cap layer 324 by CMP results in a planar top surface, consistent with known planarization process at the time (*see* §I.C), with the structure described and shown by Pethe in FIG. 5B (showing insulating cap layer 324 having a planar top

surface), and with the "truncated top surface" of CESL 20 described by the '747 Patent, which is formed by "another planarization process" resulting in the planar top surfaces shown in FIG. 1 of the '747 Patent (Ex-01, FIG. 1, 3:16-19). Given Pethe's FIG. 5B structure has undergone the fabrication process of FIG. 3B-3E, a POSITA would have understood that insulating cap layer 324 of the FIG. 5B structure likewise was planarized to form a planar top surface as shown in FIG. 5B. *See* §III.A; Ex-03, ¶202.

Pethe also discloses an etching stop layer disposed on two sides of the metal gate, where the etching stop layer has a "truncated top surface" as recited in claim 3 under Interpretations 2 -3. *See* §II.D.1. As discussed above, Pethe's insulating cap layer 324 once formed, is **made shorter by removing a part during a planarization process** (e.g., CMP), which removes a part of the top surface of the cap layer consistent with known planarization (CMP) processes which results in the insulating cap layer 324's planar top surface depicted in FIGs. 5B-5E, and in the structures of FIGs. 3F, 5B. Thus, for the reasons explained above, the FIG. 5B structure's insulating cap layer 324 is an "etching stop layer disposed on two sides of the metal gate, where the etching stop layer has a truncated top surface," under Interpretations 2 and 3. *See* §II.D.1, Ex-03, ¶203.

Thus, Pethe discloses the etching stop layer as claimed in claim 3 under Interpretations 1-3 and plain meaning of the claim language. *See also* §§VI.A.1(a)(5), I.C, III.A, II.D.1.

Pethe anticipates claim 3 and thus the claim is invalid. Ex-03, ¶204.

d. Claim 4: The semiconductor device of claim 2, wherein the first contacts disposed in the first dielectric layer and in the second dielectric layer and each first contact is a monolithically formed structure.

Pethe discloses these limitations. Ex-03, ¶¶205-207. As explained for claim 1, Pethe discloses first contacts (trench contact vias 341A/341B) disposed in Pethe's first dielectric layer (of which region 323 is a part) and in the second dielectric layer (inter-layer dielectric 330), below.

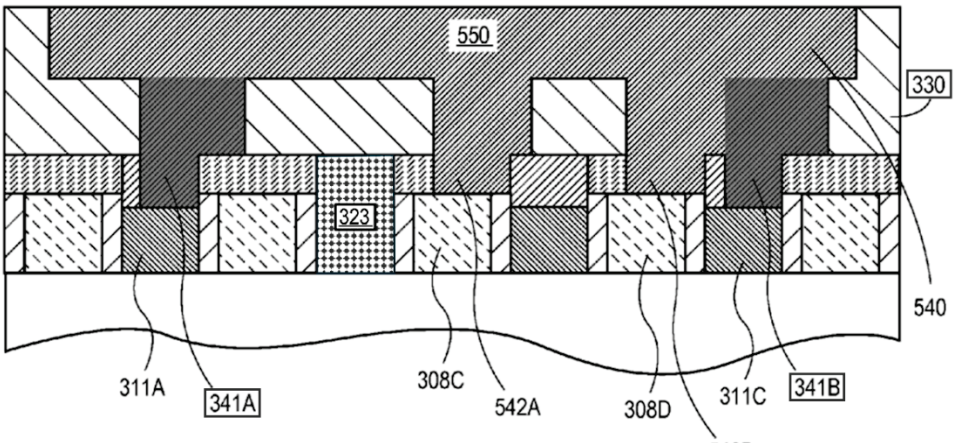


FIG. 5B

PA-01, FIG. 5B, 12:32-13:12; §§VI.A.1.a-c.

As explained by Pethe (PA-01, 9:29-10:36, 12:15-67), each trench contact vias 341A and 341B **is a monolithically formed structure** because each is formed

by filling an opening 336 with a single metal contact structure 340. In Figure 3F, a single metal deposition (*i.e.*, "deposition of **a fill metal layer**") fills openings 336 to form trench contact vias 341A and 341B, each as a **monolithically formed structure**. PA-01, 11:23-42, FIG. 3F; Ex-03, ¶206.

Thus, trench contact vias 341A, 341B in Pethe's Figure 5B structure are each a **monolithically formed structure**, as recited in claim 4. Ex-03, ¶207.

e. Claim 5: The semiconductor device of claim 2, wherein the second contacts disposed in the first dielectric layer and in the second dielectric layer and each second contact is a monolithically formed structure.

Pethe discloses these limitations. Ex-03, ¶¶208-210. As explained for claim 1, Pethe discloses the second contacts (gate contact vias 542A, 542B) disposed in Pethe's first dielectric layer (of which region 323 is a part) and in the second dielectric layer (inter-layer dielectric 330).

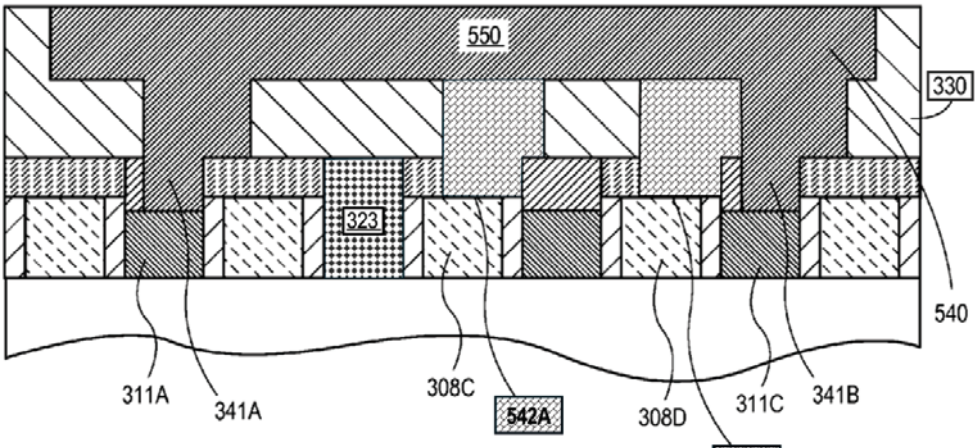


FIG. 5B

PA-01, FIG. 5B (above), 12:54-13:12, 11:23-31, 9:1-43, 7:15-34; §§VI.A.1(a)-(c).

Regarding Figure 5B, Pethe explains "a metal contact structure 540 is formed in a metal (0) trench and via openings formed in a **dielectric layer 330**" (**second dielectric layer**). PA-01, 12:54-56. Pethe also explains "contact structure 540 includes…gate contact vias (e.g., gate contact vias 542A and 542B to gate structures 308C and 308D, respectively)" (PA-01, 12:59-62), further confirming gate contact vias 542 (**second contacts**) are disposed in Pethe's **first dielectric layer** (of which region 323 is a part) and dielectric layer 330 (**second dielectric layer**), and are monolithically formed. Ex-03, ¶209.

As described in §VI.A.1(a)(8), Pethe's disclosures relating to gate contact vias 342A/342B (**second contacts**) further confirms that the gate contact vias 542A/542B are **monolithically formed structures**. The formation of gate contact vias 542 share the same formation processes as gate contact vias 342 (same feature but deeper only because of recessed spacers 520). PA-01, 12:54-67; *id.* 11:23-42, 9:1-43, 7:15-34; Ex-03, ¶¶218-22. Indeed, gate contact vias 542A/542B (**second contacts**) is each formed by filling an opening with a single metal contact structure 540. PA-01, FIG. 5B (above), 12:54-67, 10:37-11:22. Ex-03, ¶210.

f. Claim 6: The semiconductor device of claim 1, further comprising at least one fin structure disposed on the substrate.

Pethe discloses these limitations. Ex-03, ¶¶211-220. Pethe discloses the structure of FIG. 5B including at least one fin structure disposed on the substrate, as recited in claim 6. *See* §VI.A.1(a).

Pethe describes its semiconductor structures in context of non-planar devices that include fin structures. PA-01 (Pethe), 5:36-48, FIGs. 2A-2C. Pethe shows a fin structure in FIG. 2C, which is a non-planar semiconductor device (labeled "tri-gate transistor"). *Id.*, 4:62-5:12; FIG. 2C (below).

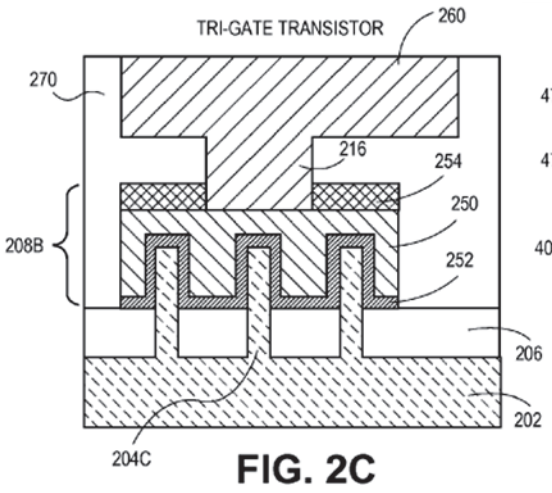


FIG. 2C

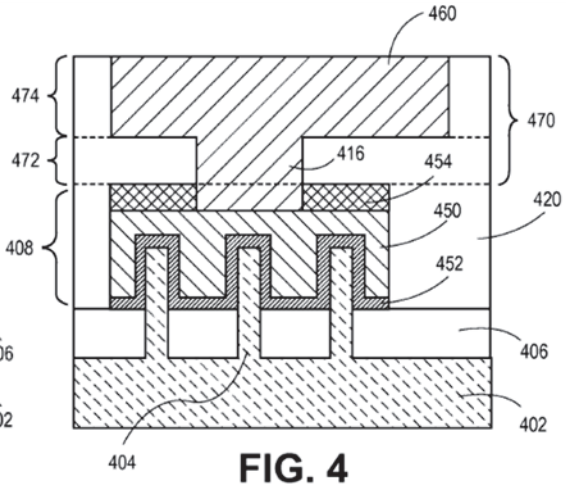


FIG. 4

Pethe discloses similar features in connection with FIGs. 3A-3F, as shown in FIG. 4. PA-01, 11:43-54; FIG. 4 (above); *see also* 14:4-13. Pethe also discloses that the method may include "prior to forming the plurality of gate structures, forming a three-dimensional body from the active regions of the substrate" and that "forming the three-dimensional body includes etching fins in a bulk semiconductor

substrate." *Id.*, 17:14-18. A POSITA would have understood such teaching refers to the non-planar diffusion or active region in the above-discussed "fin structure(s)." *See e.g., id.*, 3:60-67, 4:65-5:3, 11:49-52; *id.*, 5:35-39, 6:7-12 ("fin active regions"), Ex-03, ¶¶214-216.

A POSITA would have also understood Pethe discloses the claimed "fin structure" in recognizing that "multi-gate transistors" at the time were "fundamental building blocks of microelectronic circuitry," "fabricated by conventional processes," and "prevalent as device dimensions continue to scale down." PA-01, 1:27-45. *See also id.*, 1:14-19, 1:36-42 (explaining that "multi-gate transistors" are "consequent[ial]" to address "scaling of features in integrated circuits"—the "driving force behind an ever-growing semiconductor industry"), Ex-03, ¶217.

Pethe also explains that the Figure 5 embodiment's gate structure "may include a gate dielectric layer and a gate electrode, **as described above in FIG. 2**," discloses a multi-gate transistor having a fin structure. *Id.*, 12:39-42. The gate structure disclosed in connection with the Figure 2 embodiment is for use with and "disposed over the non-planar diffusion or active region 204C," which Pethe expressly identified as a "fin structure." PA-01, 4:62-5:5; FIG. 2C (showing "tri-gate transistor" including gate structure comprising gate electrode 205 and gate dielectric layer 252 disposed over **fin structure** 204C). Ex-03, ¶218.

In view of Pethe's disclosures and express features of "fin structure[s] in a non-planar transistor configurations, and the direct reference between the embodiments in Figures 2 and 5, a POSITA would have understood Pethe to disclose the structure of FIG. 5B to include at least one fin structure that is disposed on the substrate 302 of the FIG. 5B structure (consistent with fin structure configurations described by Pethe). Ex-03, ¶¶219-220.

In light of the teachings in Pethe above, Pethe anticipates claim 6 and thus the claim is invalid. *Id.*

g. Claim 7: The semiconductor device of claim 1, further comprising a salicide layer disposed between each S/D region and each first contact.

Pethe discloses the semiconductor structure of FIG. 5B includes a salicide layer disposed between each S/D region and each first contact as recited in claim 7.

As previously discussed, Pethe discloses the claimed "source/drain region" (the source and drain region in the diffusion region of substrate 302) and "first contacts" (e.g., trench contact vias 341A/342B) for limitations 1(e) and 1(f)-1(g). §§VI.A.1(a)(6)-(8). For example, Pethe discloses that trench contact vias 341A/341B (first contacts) are electrically conductive vias to trench contacts 311A, 311C, which are electrically conductive contacts to the source/drain regions. *See id.*, §§VI.A.1(a)(6)-(8); PA-01 (Pethe), 11:23-31, 9:29-10:36, 12:15-13:12; Ex-03, ¶¶221-222. A POSITA would have understood that the conductive and electrical

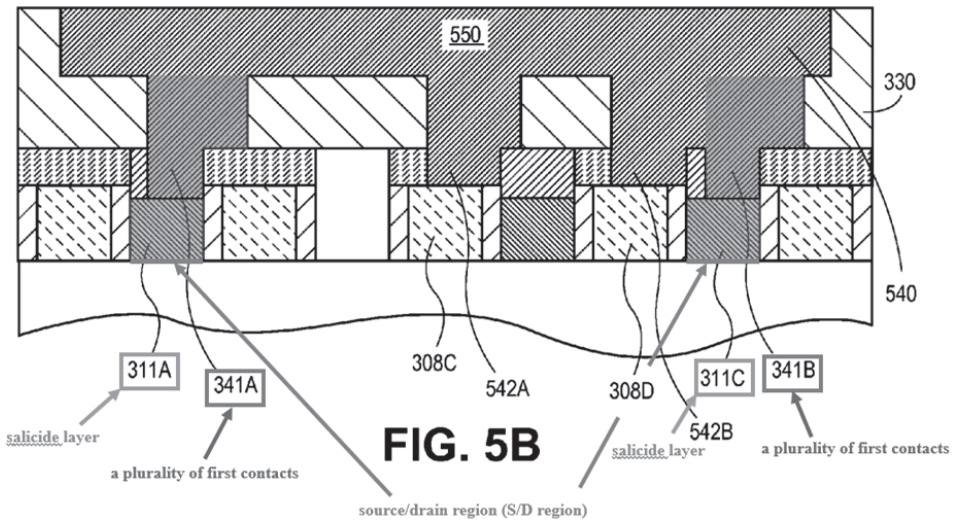
connection to FIG. 5B structure's source/drain regions is through trench contact vias 341A/341B and trench contacts 311A/311C, which Pethe discloses as self-aligned contacts (trench contacts 311A-311C are recessed versions of self-aligned contacts 310A-310C). *See e.g.*, PA-01 (Pethe), 7:39-41 ("self-aligned contacts 310A-310C"), 8:24-28, 12:42-45, 12:56-59, 7:15-16 (structure 300 is "provided following trench contact (TCN) formation"); 12:32-33 (structure 500 is likewise "provided following trench contact (TCN) formation"). Ex-03, ¶¶221-222.

As discussed for claim 1, Pethe's Figure 5 embodiment refers to and incorporates teachings from the Figure 2 embodiment. *See id.*, 12:39-41; 7:22-25; Ex-03, ¶223. §VI.A.1(a). *See also* PA-01, 6:53-59, 4:33-36 ("Source or drain trench contacts, such as trench contacts 210A and 210B, are disposed over source and drain regions of the semiconductor structure or device 200A"), 11:26-31. Pethe also incorporates the teachings of Golonzka (Ex-05) for disclosure on the process used to form the structure of FIG. 5B.

Golonzka likewise explains "[i]n an embodiment, the contacts 142 are formed by deposition and planarization, e.g., by CMP, of a conductive material. Contacts 142 may be composed of a conductive material. In an embodiment, contacts 142 are composed of a metal species. The metal species may be a pure metal, such as nickel or cobalt, or may be an alloy such as a metal-metal alloy or a metal-semiconductor alloy (e.g., such as a silicide material)." Ex-05 (Golonzka), ¶51.

Given Pethe teaches that trench contacts 311A/311C are self-aligned contacts, Pethe's other disclosures (e.g., use of a silicide material for trench contacts (e.g., contacts 210A/210B), and those incorporated by Golonzka, a POSITA would have understood the trench contacts 311A/311C in the FIG. 5B structure are disclosed as being e.g., silicide contacts, which a POSITA would have understood to be a salicide layer in such a trench contact given it is self-aligned to the same trench edges. Ex-03, ¶224. Indeed, a POSITA would have understood and appreciated that a "salicide" was known as a self-aligned silicide that is formed without use of photolithography. *See e.g.*, PA-01 (Pethe), 14:14-28; Ex-03, ¶224. Pethe discloses forming trench contacts 311A/311C (which are recessed versions of trench contacts 310A/310C (PA-01, 8:24-28) in similar fashion.

Accordingly, as shown in FIG. 5B, Pethe's trench contacts 311A, 311C is a "salicide layer" that is disposed between each S/D region in the diffusion region of substrate 302 ("source/drain region") and each trench contact via 341A, 341B ("each first contact"). *See also* §VI.A.1(a), III.A; Ex-03, ¶225.



PA-01, FIG. 5B (annotated).

In light of the teachings in Pethe above, Pethe anticipates claim 7 and thus the claim is invalid. *Id.*

h. Claim 8: The semiconductor device of claim 3, further comprising a plurality of third contacts disposed on parts of the first contacts and on parts of the second contacts, wherein each third contact is a monolithically formed structure.

Pethe discloses these limitations. Ex-03, ¶¶226-228. Metal (0) portion 550 includes **a plurality of third contacts** and is **disposed on** trench contact vias 341A, 341B (**parts of the first contacts**) and on gate contact vias 542A, 542B (**parts of the second contacts**).

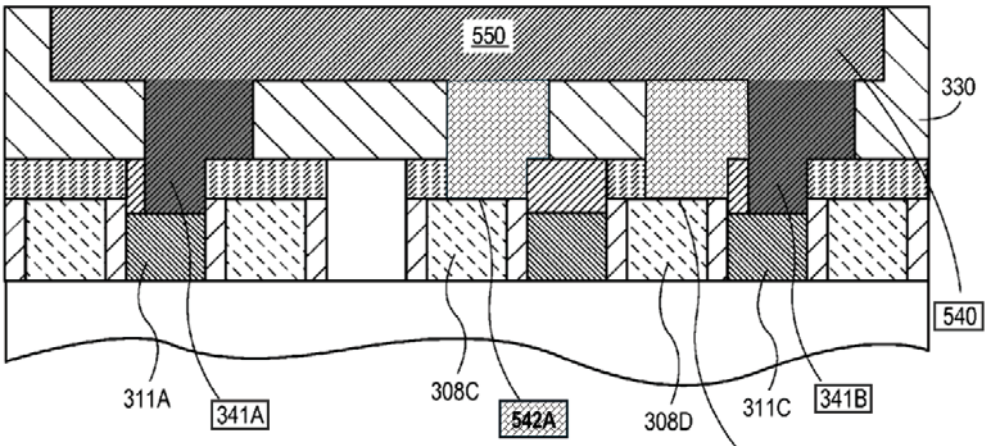


FIG. 5B

PA-01, 12:54-13:12.

Pethe explains that "metal contact structure 540 **is formed in a metal (0) trench and via openings**." PA-01, 12:54-56. Also that "metal (0) portion" is "550," and 540 also comprises "trench contact vias" (341) and "gate contact vias" (542), which contact trench contacts (311) and gate stack structures (308) respectively. PA-01, 12:56-62. Consistent with this disclosure, metal 550 is **monolithically** formed (as part of 540) and as annotated above in Figure 5B **disposed on** trench contact vias 341A, 341B (**parts of the first contacts**) and gate contact vias 542A, 542B (**parts of the second contacts**). Ex-03, ¶227.

A POSITA would have understood 550 comprises a metal line interconnect structure with **a plurality of third contacts** (e.g., metal lines) each connecting to **parts of the first and second contacts**. Ex-03, ¶228; PA-01, 11:26-31. Metal 550 is formed in metal (0) trench, and it was known that "metal (0)" was understood as an interconnect structure of metal lines in the metal (0) layer. Ex-03, ¶228. Pethe

refers to structures above trench contact vias and gate contact vias as a "metal interconnect" structure. PA-01, 3:50-4:8, 4:56-5:10, 11:59-64. Such teachings confirm that "metal interconnect" at the metal (0) layer would have been understood to include a network of metal lines. Ex-03, ¶228.

In light of the teachings in Pethe above, Pethe anticipates claim 8 and thus the claim is invalid. *Id.*

2. Proposed Rejection 1B: Claims 1-8 Are Obvious Over *Pethe*

Proposed Rejection 1A discusses how Pethe anticipates and renders invalid Claims 1-8 of the '747 Patent. Notwithstanding the disclosures in Pethe, a POSITA would have been motivated to consider the teachings and suggestions within the four corners of Pethe, including the various aspects and embodiments disclosed there, and in light of such collective disclosures, found it obvious to configure the FIG. 5B structure to include features described in the various aspects described in the four corners of Pethe. Consequently, such obvious variations gleaned from the teachings throughout Pethe would have predictably resulted in a slightly modified semiconductor structure of the FIG. 5B structure that renders obvious Claims 1-8. Ex-03, ¶229.

To begin, a POSITA reviewing Pethe would have understood, appreciated, and recognized that Pethe discloses related features directed to semiconductor devices and processing and in particular to gate contact structures that are disposed

over active portions of gates, and processes for forming such structures. PA-01 (Pethe), 1:5-11. As explained in §III.A, Pethe frames the disclosed inventions in context of semiconductor devices and structures, including the fabrication of semiconductor devices and integrated circuit devices including MOS transistors, including multi-gate (e.g., tri-gate) transistors, and other semiconductor structural elements, such as gate stack structures, gate and trench contact structures, sidewall spacers, cap layers, etc. *Id.*, 1:14-45, 13:63-14:13, 15:39-17:18. Through FIGs. 1A-8, Pethe describes various embodiments and related aspects directed to semiconductor structures and the fabrication of such devices that include features common to the various disclosed embodiments, including gate and trench contact structures, metal gate structures, cap layers, among others. *Id.*, 1:49-2:46, 2:64-7:14 (disclosing features concerning FIGs. 1-2C), 7:9-11:42 (disclosing features concerning FIGs. 3A-3F), 11:43-12:14 (disclosing features concerning a variation to FIGs. 3A-3F shown in Figure 4), 12:15-13:12 (disclosing the Figure 5 embodiment and FIGs. 5A-5B), 13:13-21 (disclosing variation (not shown) where spacers are recessed to approximately the same height as the trench contacts), 13:23-43 (disclosing a variation as shown in FIG. 6), 13:44-61 (disclosing a variation as shown in Figure 7), 14:29-15:38 (disclosing a computing device 800 with an implementation of the invention as shown in FIG. 8 where MOSFET transistors are

built "in accordance with implementations of the invention"), 14:39-17:18 (disclosing the various aspects of the "present invention"). Ex-03, ¶230.

A POSITA would have thus understood that Pethe discloses semiconductor devices, including MOS transistors (MOSFETs) having gate contact structures disposed over active portions of gates and methods of forming such structures (PA-01 (Pethe), 2:50-52, 2:50-3:10, 7:9-11:42, 12:22-13:12, 14:4-11) and that the fabrication steps that result in the structure of Figure 3F are shown in FIGs. 3A-3F (*id.*, 7:9-16, FIGs. 3A-3F, 7:15-11:42) and that the fabrication of the FIG. 5B structure is shown and described collectively in relation to FIGs. 5A-5B. Consistent with opinions in FIG. 4A, a POSITA would have understood that the fabrication process disclosed in connection with FIGs. 3A-3F is the same as that for FIGs. 5A-5B, where the "slight differences" between the two embodiments is mainly with the recessed spacers 520 used in FIGs. 5A-5F in place of the taller spacers 320 in FIGs. 3A-3F. *Id.*, 12:15-67. Ex-03, ¶231.

As discussed in §§III.A, VI.A.1(a), Pethe describes the Figure 5 embodiment without repeating details concerning features that are common to those discussed for FIGs. 3A-3F. For example, both FIGs. 3A-3F and the Figure 5 embodiment (FIGs. 5a-5B) disclose substrate 302, dielectric layer 330, inter-layer dielectric region 323, trench contact vias 341A and 341B and trench contacts 311A and 311B, metal gate stack structures 308A-308E. *Id.*, FIGs. 3A-3F, 5A-5B. Further, a POSITA would

have understood that the Figure 5 embodiment discloses common features with FIGs. 3A-3F, but uses different labels, such as insulating cap layer (e.g., 322 (FIGs. 3A-3F) and 522 (FIGs. 5A-5B)), metal contact structures (e.g., 340 (FIG. 3F) and 540 (FIG. 5B)), which include a metal (0) portions (e.g., 350 (FIG. 3F) and 550 (FIG. 5B)), trench contact vias (e.g., 341A/341B in FIGs. 3F and 5B), and gate contact vias to gate stack structures 308A-308D (e.g., 342A/342B (FIG. 3F) and 542A/542B (FIG. 5B)). *See id.*, 2:3-3:10, 7:9-11:42, 12:22-13:12. Also, a POSITA would have understood and appreciated that Pethe similarly references other features in discussing the Figure 3 and Figure 5 embodiments, such as the Figure 2 embodiment, and from the teachings relating to FIG. 4 *See e.g.*, *id.*, 7:20-25, 12:37-42; 11:43-12:31 (bi-layer ILD 330 variation shown in FIG. 4). Ex-03, ¶232.

A POSITA would have understood that such common and related features, and the processes described in Pethe to form such features, correspond to the structure of Figure 5B. Further, a POSITA would have recognized that Pethe ties together the teachings and suggestions of the various disclosed aspects, where, for example, after describing the features relating to Figures 1A-8, Pethe explains "[t]hus, embodiments of the present invention include gate contact structures disposed over active portions of gates and methods of forming such gate contact structures." *Id.*, 15:39-41. Pethe expresses similar teachings elsewhere. *Id.*, 2:50-63, Abstract; *see also id.*, 4:39-42, 5:15-34, 7:22-25, 9:15-20, 11:23-25, 12:15-31,

12:39-42, 12:48-53., 15:39-41. And as mentioned above, Pethe's claims link together the various aspects of the disclosed invention in Pethe. *Id.*, 17:20-20:23. Ex-03, ¶233.

In light of such disclosures and suggestions in Pethe, a POSITA would have been motivated to consider the collective teachings and suggestions in Pethe, including all aspects of the disclosed embodiments (including the fabrication processes and related structures disclosed in connection with e.g., FIGs. 1C, 2A-2C, 3A-3F, 4) in considering the configuration and fabrication of the structure of Figure 5B. Ex-03, ¶234. Upon such review, a POSITA would have found ample reasons to consider modifications to the FIG. 5B structure (whether by fabrication process that results in adjusted structural elements, material, dimension, etc.) to successfully achieve a semiconductor structure, such as MOSFET transistors that would have been operable and applicable to the computing devices Pethe contemplates integrating such components. *See e.g.*, 14:29-15:38 (discussing computing devices that include MOSFET transistors "built in accordance with implementations of the invention"). Ex-03, ¶234.

For example, a POSITA would have been guided by Pethe's teachings and suggestions concerning the fabrication and resulting structures for FIGs. 3A-3F, and related disclosures from other embodiments, including the Figure 2 and 4 embodiments, to perform similar processes, and use similar materials and structural

elements to fabricate the structure in FIG. 5B. Ex-03, ¶235. For instance, a POSITA would have considered and been motivated to implement similar processes, materials, and/or configurations disclosed and suggested in Pethe's other embodiments (e.g., Figure 3 embodiment) to fabricate and configure the structural elements, layers, and other features in the FIG. 5B structure, including for example, the trench contacts 311A/311C, recessed spacers 520, trench contact vias 341A/341B, gate contact vias 542A/542B, insulating cap layer 322, insulating cap layer 324, source/drain regions, (metal (0) portion 550, and/or metal contact structure 540. Ex-03, ¶235. For example, a POSITA would have been motivated and found obvious to configure, modify, and/or arrange such features in the Figure 5 embodiment based on the related processes, configurations, arrangements, and/or materials disclosed by Pethe for the embodiments associated with FIGs. 2-4 to form the semiconductor structure described Pethe for FIG. 5B. Ex-03, ¶235.

A POSITA would have had reasons to consider and combine the collective teachings and suggestions in Pethe given that they are all related to semiconductor device structures and fabrication processes for forming such structures, including related structural elements and layers. Ex-03, ¶236. Upon recognizing and appreciating that Pethe relates and references common and overlapping features between embodiments in describing the disclosed invention (*see e.g.* PA-01, 2:50-63, 4:39-42, 5:15-34, 7:22-25, 9:15-20, 11:23-25, 12:15-31, 12:39-42, 12:48-53,

15:39-17:18, 17:20-20:23), a POSITA would have found it obvious to combine the various disclosed aspects in Pethe to form a semiconductor structure that recited in claims 1-8 as discussed in Proposed Rejection 1A. Ex-03, ¶236. A POSITA would have considered integrating adjustments to the FIG. 5B structure (in its fabrication and resulting structure) to accommodate the various applications of MOSFETs (including tri-gate transistors) contemplated by Pethe. *See e.g.*, PA-01, 14:29-15:38 (integrated circuit die of a processor, communication chip, or "another component" included in contemplated computing devices 800 may include "one or more devices, such as MOS-FET transistors built in accordance with implementations of the invention"). Thus, design needs and market-based motivations related to the types of computing devices 800 contemplated by Pethe would have guided a POSITA to consider options and variations in the fabrication processes and configuration of the FIG. 5B structure for appropriate application with the types of devices 800 the market demanded at the relevant time of the '747 Patent. Ex-03, ¶236.

A POSITA would have found combining the various fabrication process and structural elements and materials in the collective teachings and suggestions in Pethe to form the resulting structure of FIG. 5B would have been achieved according to known methods at the time (such as those expressly described and suggested in Pethe for the various embodiments (including the embodiments of FIGs. 2-5) to yield a predictable semiconductor structure like that recited in the Claims of the '747 Patent.

Indeed, given the related teachings between the FIG. 5B embodiment and the other embodiments in Pethe (as Discussed above), a POSITA would have recognized that fabricating and implementing the structural elements, layers, and/or materials in the FIG. 5B structure in accordance with, e.g., FIGs. 3A-3F would have involved a simple substitution of known elements and use of known fabrication processes and techniques to form features in the structure, such as the trench contacts, spacers, gate stack structures, trench contact vias, gate contact vias, insulating cap layers, source/drain regions, metal (0) portion, and metal contact structure described in the embodiments of FIGs. 3 and 5. Moreover, the teachings, suggestions or motivations provided by Pethe with its FIG. 5B embodiment (*see e.g.*, PA-01, 12:15-67 (referring to common elements and variations of elements (e.g., spacer) from Figure 3 embodiment), 17:20-20:23 (claims to a semiconductor structure integrating features applicable to FIGs. 3A-3F and the Figure 5 embodiment), FIG. 3F, 5B) would have led a POSITA to combine the collective teachings in Pethe's embodiments to arrive at a semiconductor structure consistent with that in FIG. 5B and with claims 1-8 of the '747 Patent. Ex-03, ¶237.

Additionally, a POSITA would have understood and appreciated that implementing, integrating, and/or applying features consistent with those from FIGs. 3A-3F (and/or the embodiments discussed regarding other figures in Pethe) with the Figure 5B embodiment would have been a predictable variation that would have

provided foreseeable benefits. For example, a POSITA would have appreciated the advantage to form structural elements and layers in the Figure 5B embodiment in a manner consistent with those taught for the Figure 3 embodiment given the relationship between the beginning and resulting structures as shown for FIGs. 5A-5B and FIGs. 3A, 3F. Ex-03, ¶238. For example, a POSITA would have appreciated the benefit in manufacturing process efficiencies to form the trench contacts 311A/311C, recessed spacers 520, gate stack structures 308A-308E, trench contact vias 341A/341B, gate contact vias 542A/542B, insulating cap layer 322, insulating cap layer 324, source/drain regions, metal (0) portion 550, and metal contact structure 540 in the FIG. 5B structure in a manner consistent with that taught by Pethe for FIGs. 3A-3F. Ex-03, ¶238.

A POSITA would have had a reasonable expectation of success in implementing and achieving the above combination of collective teachings from Pethe given the details and teachings for implementing the resulting structure came from Pethe's own disclosures, which significantly overlap in processes, materials, and features. Ex-03, ¶239. Thus, the knowledge, background, and experience of a POSITA in light of the guidance from the collective teachings from Pethe would have led such a skilled artisan to successfully modify and/or configure the FIG. 5B structure in a manner consistent with that discussed above for claims 1-8 in Proposed Rejection 1A such that the structure provided an operable transistor applicable to the

various types of computing devices contemplated by Pethe (*e.g.*, PA-01, 14:29-15:38). Ex-03, ¶239.

A POSITA would have thus viewed such combined teachings to form one or more of the features/components of Pethe's semiconductor structure as an obvious example of substituting a known element for another to obtain predictable results (e.g., integrating fabrication processes and resulting structural elements, layers, or materials from FIGs. 3A-3F that track (if not being the same) elements, layers, or materials in the Figure 5 embodiment); a choice from among a finite number of identified, predictable solutions (e.g., those disclosed by Pethe regarding FIGs. 2A-4 with those regarding FIGs. 5A-5B), with reasonable expectation of success; and teachings, suggestions, or motivations in Pethe (e.g., PA-01, 2:50-3:10, 12:15-67, 15:39-17:18, 17:20-20:23) that would have led a POSITA to modify Pethe and arrive at the invention claimed in claims 1-8. Ex-03, ¶240.

Combination of Pethe's Embodiments

As explained, in discussing Figure 5, Pethe does not repeat details/discussions related to similarly labeled features in Figure 3 (with same or similar labels), *e.g.*, substrate 302, ILD region 323, dielectric layer 330, trench contact vias 341A/341B, trench contacts 311A/311C, and cap layer 522 (same as cap layer 322 but wider because of recessed spacers 520), gate contact vias 542A/542B (same as gate contact

vias 342A/342B), and metal (0) portion 550 (same as metal (0) portion 350). PA-01, FIGs. 3A-3F, 5A-5B, 2:3-63, 7:9-11:42, 12:22-13:12; Ex-03, ¶241.

In addition to relying on Pethe's disclosure of Figure 5B structure including the discussions of the common features, a POSITA would also found it obvious to consider and apply the teachings of Figure 3 when forming/configuring Figure 5B's structure (as discussed in §§VI.A.1(a)-(h)), and would have had a reasonable expectation of success in doing so. Ex-03, ¶242. Indeed, a POSITA would have recognized/appreciated that Pethe relates/references common features between embodiments in describing the disclosed invention (*e.g.* PA-01, 2:50-63, 4:39-42, 5:15-34, 7:22-25, 9:15-20, 11:23-25, 12:15-31, 12:39-42, 12:48-53, 15:39-41), and thus been motivated to incorporate such combined teachings to yield the predictable result of a structure as discussed above for claims 1-8. Ex-03, ¶242; §§VI.A.1.a-f. *KSR*, 550 U.S. at 416.

In addition to the reasons above, discussed below are obvious variations concerning features relating to specific claim limitations that a POSITA would have been motivated by the collective teachings and suggestions in Pethe to arrive at a semiconductor structure consistent with the FIG. 5B structure and recited in claims 1-8 discussed above in Proposed Rejection 1A. Ex-03, ¶243.

a. Claims 2-5 and 8 [16]

Pethe discloses/suggests these limitations. *See* §VI.A.1(b)-1(e), 1(h) above; *see also* Ex-03, ¶244.

b. Claim 6: The semiconductor device of claim 1, further comprising at least one fin structure disposed on the substrate.

Pethe discloses/suggests this limitation. *See* §VI.A.1(f) above; *see also* Ex-03, ¶245.

As discussed above for Claim 6 in Proposed Rejection 1A, Pethe discloses, the semiconductor device of Pethe's invention can be implemented with tri-gate or FinFET transistors, which were known to include fin structures. PA-01, 14:8-11; 1:27-45 (Pethe recognizing that "multi-gate transistors, such as tri-gate transistors, have become more prevalent" and "fabricated on bulk silicon substrates of silicon-on-insulator substrates").

Further, Pethe describes its semiconductor structures in context of non-planar devices that include fin structures. *See e.g.*, PA-01, 5:36-48 (discussing the Figure 2 embodiment where "the semiconductor structure or device 200 is a non-planar device such as, but not limited to, a fin-FET or a tri-gate device"), 4:62-5:12, FIG.

[16] Claim 1 does not recite a "semiconductor device." However, for purposes of analysis of the prior art, Requester assumes claims 2-9 refer to the semiconductor "structure" recited in claim 1.

2C (describing the fin structure in Figure 2C (showing a "tri-gate transistor" with a "fin structure" 204C), 11:43-54, FIG. 4 (showing a non-planar deice with a "fin structure"), 17:14-18 (discussing "forming [a] three-dimensional body [by] etching fins in a bulk semiconductor substrate"). *See also e.g., id.*, 3:60-67, 4:65-5:3, 11:49-52; *id.*, 5:35-39, 6:7-12 ("fin active regions"). Pethe also explains that the Figure 5 embodiment's gate structure "may include a gate dielectric layer and a gate electrode, **as described above in FIG. 2**," which discloses a multi-gate transistor having a fin structure. *Id.*, 12:39-42; *id.*, 4:62-5:5; FIG. 2C; Ex-03, ¶246.

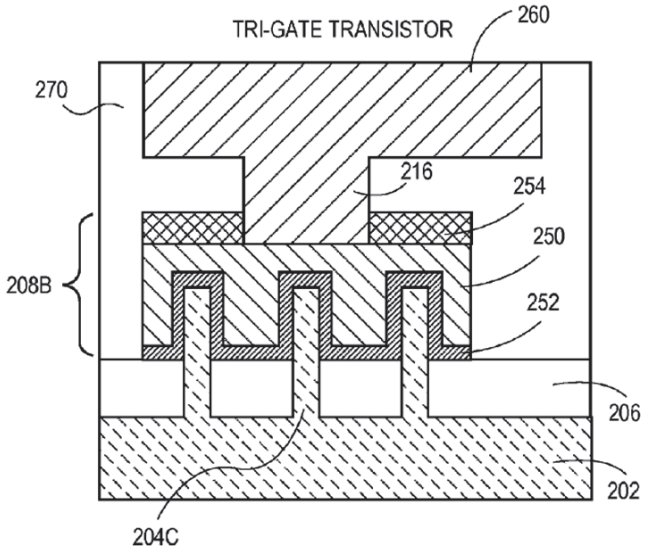


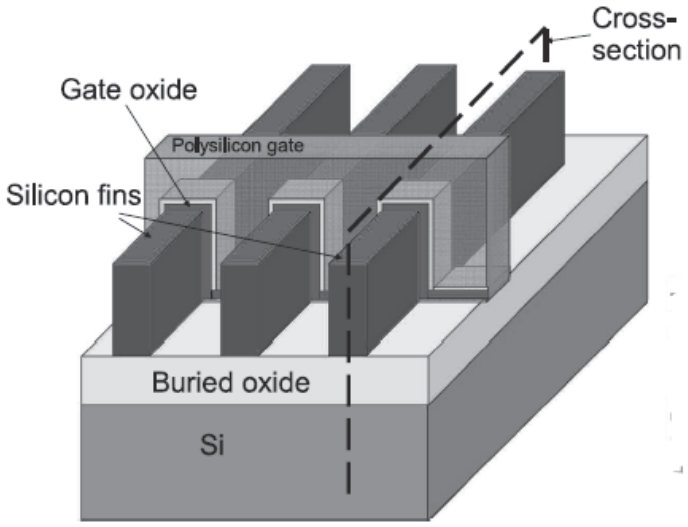
FIG. 2C

PA-01 (Pethe), FIG. 2C.

In light of the collective teachings and suggestions in Pethe, it would have been obvious to configure the Figure 5B structure in context of a multi-gate or FinFET transistor device including at least one fin structure disposed on the substrate

of the structure. A POSITA would have been motivated to implement such a configuration to provide a transistor applicable for the types of computing devices contemplated by Pethe. *Id.*, 14:8-15:38. Ex-03, ¶247. Indeed, Pethe claims a semiconductor structure that includes an active region of the substrate with a "three-dimensional semiconductor body (*id.*, 18:39-41), consistent with multi-gate transistors, such as a FinFET, having a fin structure. Thus, a POSITA reviewing the collective teachings in Pethe (including those in connection with the Figure 2 and Figure 4 embodiments) would have had reasons to consider and configure the Figure 5B structure to include a fin structure, which were known features of the multi-gate, tri-gate, or FinFET transistor devices contemplated by Pethe. Ex-03, ¶¶247-248.

A POSITA was well aware of, and had experience with, FinFET type transistor devices and related structures consistent with those contemplated by Pethe. Ex-03, ¶248. Indeed, FinFET devices were well known to include fin structures, like that described by Pethe (FIGs. 2C, 4). *See e.g.*, Ex-15 (Xiao72-74, 351).



Ex-15 (Xiao), FIG. 9.41(a), 351, 72-74.

A POSITA would have appreciated and recognized the benefits of implementing the Figure 5B structure of Pethe as a non-planar structure with a multi-gate or FinFET transistor, such as scaling to minimize the footprint of the integrated circuit implementing such transistors, consistent with that contemplated by Pethe. *See* PA-01 (Pethe), 1:14-45, 14:29-15:38. *See also* Ex-15 (Xiao), FIG. 15.1, 650-51 (describing features consistent with a POSITA's state of art knowledge at the relevant time such as the known use of "a trigate, [where] fabs can use the same lithographic technology to reduce transistor dimensions while maintaining the same performance, or to improve device performance without increasing device density" and where "IC manufacturers can further improve device performance by making the fin taller" and that "a finFET is easier to build than a trigate. Intel's 22-nm IC chips are built with trigate devices"). Ex-03, ¶249.

In light of such knowledge and experience, and in context of Pethe's teachings and suggestions, a POSITA would have been motivated to configure the Figure 5B structure with a fin structure disposed on top of substrate 302, consistent with known Fin-FET and tri-gate transistor semiconductor structure configurations at the relevant time. Ex-03, ¶250.

A POSITA's knowledge and experience would have led them to implement such fin structure features in the Figure 5B structure with a reasonable expectation of success that the semiconductor structure would provide functional transistor operations consistent with the application of the structure in the various types of computing devices that Pethe contemplates. Ex-03, ¶251. For instance, a POSITA would have recognized that implementing such features would have involved applying known semiconductor fabrication processes and structural elements (e.g., FinFETs, tri-gate transistors and related fabrication processes) that were within the capabilities and knowledge of a POSITA at the relevant time. *Id.* Indeed, Pethe expressly discloses semiconductor structures with fin structures (PA-01 (Pethe), FIGs. 2C, 4), thus expressly guiding a POSITA to integrate the same with the Figure 5B structure. Also, a POSITA would have considered the design needs for such applications, relevant market demands, and related factors and thus found implementing Pethe's structure as a FinFET or tri-gate type device. *Id.*

Accordingly, it would have been obvious to configure the Figure 5B structure to include at least one fin structure disposed on the substrate of the structure, as recited in Claim 6 of the '747 Patent. Thus, for the reasons here, further above for this Proposed Rejection 1B, and the discussion for Proposed Rejection 1A, the collective teachings and suggestions in Pethe render obvious Claim 6 of the '747 Patent. *Id.*, ¶252.

c. Claim 7: The semiconductor device of claim 1, further comprising a salicide layer disposed between each S/D region and each first contact.

Pethe discloses/suggests these limitations. *See* §VI.A.1(g) above; *see also* Ex-03, ¶¶253-259.

In Proposed Rejection 1A for Claim 7, Requester discussed how Pethe's Figure 5 embodiment refers to and incorporates teachings from the Figure 2 embodiment. *See* PA-01 (Pethe), 12:39-41; 7:22-25. *See also id.*, 6:53-59 (explaining that "[a]ny or all of contacts 210A and 210B and vias 212A, 212B and 216 may be composed of a conductive material" that may be a "metal-semiconductor alloy (e.g., such as a silicide material)"); *id.*, 4:33-36 (describing source or drain contacts disposed over S/D regions of the structure), 11:26-31. Golonzka, which Pethe incorporates by reference (*id.*, 7:35-41), describes similar features of the disclosed contacts. Ex-05 (Golonzka), ¶51. Ex-03, ¶254.

In light of such teachings and suggestions, a POSITA would have been motivated to configure the trench contacts 311A-311C in the Figure 5B structure to include a salicide layer that is disposed between each S/D region (part of the diffusion region of substrate 302) and each trench contact via 341A/341B ("first contact"). Ex-03, ¶255. For instance, a POSITA would have appreciated and understood that the use of a salicide layer between a source/drain and a contact, such as in self-aligned trench contacts, was widely known and implemented in semiconductor devices at the relevant time. Ex-15 (Xiao), 157-58, FIG. 5.39 (describing salicide processes involving metal deposition/annealing over source/drain regions consistent with a POSITA's state of art knowledge at the time).

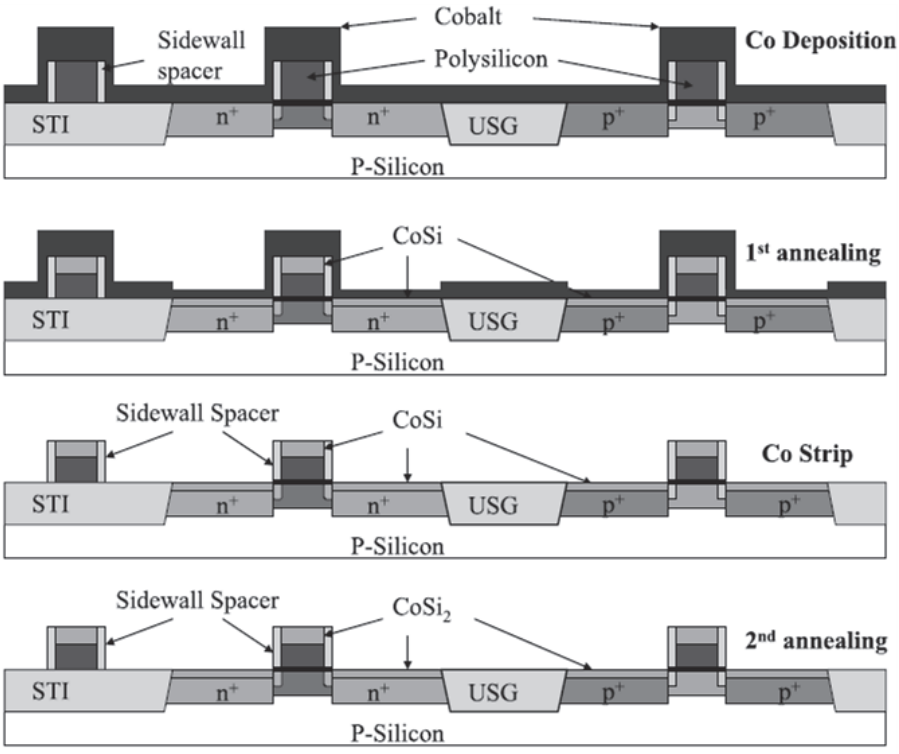


Figure 5.39 Self-aligned cobalt silicide process.

Moreover, a POSITA would have been understood that providing a salicide layer between the S/D region and trench contact via 341A/341B would have reduced electrical resistance with the S/D contact in the Figure 5B structure. *See e.g.*, Ex-15 (Xiao), 585 (describing a POSITA's state of art knowledge at the relevant time that salicide helps reduce contact resistance). Ex-03, ¶256. Thus, a POSITA would have been motivated to implement such a salicide layer in the Figure 5B structure to enhance or establish conductive surfaces to the semiconductor device. *Id.*

A POSITA would have understood and appreciated that providing a salicide layer between the source/drain region and trench contact vias 341A/341B in the Figure 5B structure of Pethe would have been an obvious implementation of conventional and known semiconductor device fabrication and structure features that were well within the experience and capabilities of such a skilled person at the relevant time. Ex-03, ¶257. Accordingly, and in context of the collective teachings in Pethe (including the guidance offered by Pethe's disclosures for the Figure 2 embodiment), a POSITA would have reasonably expected to succeed at implementing such features in the Figure 5B structure.

Therefore, in light of the teachings and suggestions in Pethe, and a POSITA's knowledge and experience at the relevant time, a POSITA would have been motivated and found obvious to include a salicide layer in Pethe's Figure 5B structure to provide a more conductive interface between the S/D region and the

source/drain contact, thus improving performance of the semiconductor device. Ex-03, ¶258.

Accordingly, it would have been obvious to configure the Figure 5B structure to include a salicide layer disposed between each source/drain region and each trench contact via 341A/341B ("first contact"), like that recited in Claim 6 of the '747 Patent. Ex-03, ¶259. Thus, for the reasons here, further above for this Proposed Rejection 1B, and those for claim 7 in Proposed Rejection 1A, the collective teachings and suggestions in Pethe render obvious Claim 7 of the '747 Patent. *Id.*

3. Proposed Rejection 1C: Claims 1-8 Are Obvious Over *Pethe* in view of *Pham*

a. Limitations [1.pre]-[1.c] and [1.e]-[1.f]

Proposed Rejections 1A and 1B are incorporated herein to support Proposed Rejection 1C. *See* §§VI.A.1(a)-(h), VI.A.2(a)-(c). Namely, for reasons discussed above for Proposed Rejection 1B (which incorporates opinions from Proposed Rejection 1A), Pethe discloses and/or renders obvious each of claim limitations 1(pre)-1(c) and 1(e)-1(h). For these reasons and those discussed below for limitation 1(d), the combination of Pethe in view of Pham discloses or suggests Claim 1 and renders the claim obvious. Ex-03, ¶¶260-261.

b. Limitation [1.d]: a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface;

The discussions for Proposed Rejections 1A and 1B are incorporated herein to support Proposed Rejection 1C. *See* §§VI.A.1(a)(5), VI.A.2. In addition, for the reasons below and above in this Proposed Rejection 1C, the combined teachings and suggestions in Pethe and Pham disclose or suggest, and render obvious claim limitation 1(d).[17] Ex-03, ¶¶262-288.

As discussed in Proposed Rejection 1B (which incorporates Proposed Rejection 1A) the teachings and suggestions in Pethe relating to the implementation of the Figure 5 embodiment structure, where, e.g., spacers are disposed on two sides of the gate stack structures 308. *See* discussion of Pethe's teachings in Proposed Rejections 1A-1B concerning structure 500. As explained, the Figure 5 embodiment includes the same gate stack structures 308A-308E disposed above substrate 302

[17] A POSITA would have found it obvious to implement the spacer with a truncated top surface feature in Pethe's Figure 5B structure does not mean Pethe does not disclose such a feature as claimed in Claim 1—Pethe does disclose the claimed spacer for reasons discusses for limitation 1(d) in Proposed Rejection 1A. Rather, the current Proposed Rejection 1C is consistent with Proposed Rejection 1B (further supported by the teachings and suggestions of Pham, which in context of Pethe's teachings), where a POSITA would have found it obvious to form and implement spacers 520 with a "truncated top surface" notwithstanding the disclosures in Pethe.

including a gate dielectric layer and gate electrode "as described above in association with FIG. 2." PA-01 (Pethe), 7:20-25, 12:37-43. Structure 500 likewise includes spacers formed on the sides of the gate stack structures 308 providing spacing between trench contacts 310A-310C and the gate stack structures 308. *Id.*, FIGs. 3A, 3F, 5A, 5F, 7:25-28, 12:15-42-45. *Id.*, FIG. 5A, 12:15-67; §III.A. Ex-03, ¶263.

A POSITA would have been aware of the use and benefits of providing spacers on the sidewalls of a metal gate in a semiconductor structure (e.g., isolation of gate structures from conductive contacts (PA-01, 6:45-49) and that various configurations and processes can be implemented to achieve a structure like that described for Figure 5A (from which the Figure 5B structure is fabricated). Ex-03, ¶264. So while Pethe explains structure 300 (and thus structure 500) may be provided by a process described in the incorporated disclosures of Golonzka (PA-01, 7:35-38; *e.g.*, Ex-05, FIGs. 1A-1K, 2, [0030]-[0051]), a POSITA would have nonetheless been motivated to consider teachings in the art regarding the various ways to achieve a structure compatible with and/or similar to the structure 500 of Figure 5A (with planar top surface spacers coplanar with the metal gate structures), from which the resulting Figure 5B structure is fabricated. Indeed, Pethe explains for the Figure 5 embodiment that it is "understood that the specific arrangement of structure [500] is used for illustration purposes, and that a variety of possible layouts may benefit from embodiments of the invention described herein." PA-01, 7:15-20,

12:32-37. Thus, a POSITA had reasons to consider guidance in the art concerning the formation and implementation of spacers when contemplating the FIG. 5B structure in Pethe.

In doing so, a POSITA would have considered the teachings and suggestions in Pham which discloses similar features, structural elements, and processes for similar semiconductor device applications. Ex-03, ¶264.

For example, Pham discloses methods for forming a semiconductor device and the resulting semiconductor device. PA-02 (Pham), Abstract, 1:6-11. Similar to Pethe, Pham recognized the state of art concerns for providing manufacturing techniques for semiconductor devices with any eye toward performance through the increase of density of FETs on integrated circuit devices. *Id.*, 1:40-2:20; PA-01, 1:14-45. With reference to FIG. 1A, Pham describes conventional structural elements of a semiconductor device, such as sidewall spacers 18 encapsulating and protecting gate structures 11. PA-02, 3:54-4:20. Pham explains its disclosures is directed to methods of forming a semiconductor device and resulting semiconductor device "that may avoid, or at least reduced, the effects of one or more of the problems identified above." *Id.*, 4:21-25, 6:6-14, 6:37-48; Ex-03, ¶265.

In particular, Pham describes forming a semiconductor device with a protected gate cap layer, where a process is performed "to recess a gate structure and a spacer structure of a transistor to thereby form a recessed gate structure and a

recessed spacer structure and forming a gate cap layer in the spacer/gate cap recess." *Id.*, 4:37-54. *See also id.*, 4:55-5:18, 8:9-58, FIGs. 2C-2D. Pham's processes form a metal gate and sidewall spacer configuration where the structures have planar top surfaces and are on the same level. *See e.g.*, *id.*, FIGs. 2A, 3A, 6:51-8:8, 10:13-19. Pham also discloses self-aligned contact processes to form contacts to source/drain regions in the semiconductor device. *See id.*, FIGs. 2J-2K, 3G-3J, 9:31-10:11, 11:1-19; Ex-03, ¶266.

Pham is analogous art. For example, a POSITA would have understood that Pham is in the same field (MOSFETs) and reasonably pertinent to a problem the '747 Patent purports to address (e.g., MOSFET fabrication). *See e.g.*, PA-02 (Pham), 1:5-2:20; PA-01 (Pethe), 1:5-11, 14:1-13, 15:8-29; Ex-01 ('747 Patent), 1:9-2:9, 2:18-20, 2:39-42, 3:1-25, 5:31-6:37. Ex-03, ¶267. Moreover, Pethe, the '747 Patent, and Pham disclose features relating to semiconductor devices, structures, and related fabrication processes applicable to e.g., FinFET or similar transistor devices (PA-02, 1:5-2:20, 6:66-7:5; Ex-01, 1:5-12, 2:18-20, 2:39-6:37; PA-01, 1:5-11, 5:35-39, 7:29-11:42, 12:15-67, 14:1-13, 15:8-29, 15:53-54, 16:47-48, 17:17-18), where metal gates and corresponding sidewall spacers have planar top surfaces. PA-01, FIGS. 5A-5B; PA-02, FIG. 2A; Ex-01, FIG. 1. Ex-03, ¶267. Moreover, a POSITA would have recognized other similarities and compatibilities between Pethe and

Pham, such as the use of a hard mask disposed over the metal gate and sidewall spacers. *See e.g.*, PA-02, FIG. 2D; PA-01, FIGs. 5A-5B. Ex-03, ¶267.

Thus, a POSITA would have also recognized similarities between Pethe and Pham that would have led them to consider their collective teachings to form various transistor device structures for given applications, like those contemplated by Pethe and Pham (*see e.g.*, PA-01, 14:1-15:38; PA-02, 4:37-5:41, 6:3-50). Ex-03, ¶268.

In particular, and as one example, with reference to FIG. 2A, Pham describes a structure (e.g., product 100) including "a plurality of illustrative gate structures 111 that are formed above a substrate 112." PA-02, 6:51-61. "[G]ate structures 111 are intended to be representative in nature of any type of gate structure that may be employed in manufacturing integrated circuit products using so-called gate-first or gate-last (replacement-gate) manufacturing techniques." *Id.*, 7:6-10. In general, gate structures comprise "one or more conductive material layers that act as the gate electrode" including e.g., tungsten, aluminum, etc. *Id.*, 7:10-17. Ex-03, ¶269. In a replacement gate technique, dummy gate structures may be patterned and sidewall spacers 118 are formed adjacent to the dummy gate structure. PA-02, 7:17-22. Pham explains the dummy gate structure remain "as many process operations are performed to form the device (e.g., the formation of raised, doped source/drain regions, performing an anneal process, etc.), consistent with that known in the art. *Id.*, 7:22-27.

Pham further explains that after the dummy gate is removed (consistent with replacement gate techniques), metal or metal alloy layers "that will become the gate electrode" may be deposited in the gate cavity formed by the removed dummy gate. *Id.*, 7:41-43. A POSITA would understand at this stage, the sidewall spacers 118 are on the sides of the replacement metal gate and thus are an example of a "spacer disposed on two sides of a metal gate" similar to that recited in limitation 1(d) of the '747 Patent. Ex-03, ¶270. Pham explains after the metal gate is formed between the spacers 118, '[a] CMP process is then performed." PA-02 (Pham), 7:44-51, FIG. 2A (annotated below).

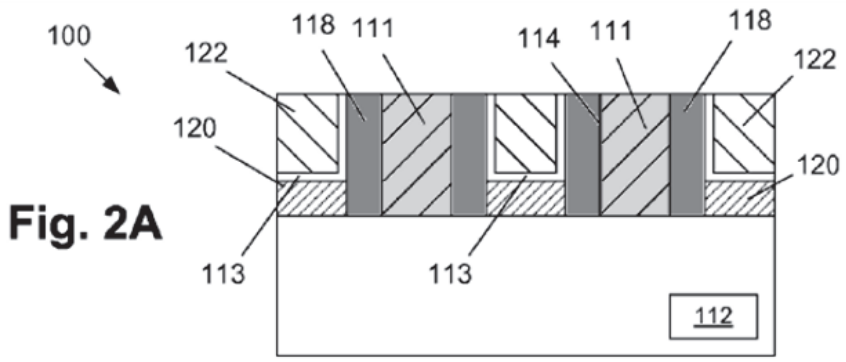


Fig. 2A

As shown and described by Pham, the structure also includes a source/drain regions 120 that may be "any type of source/drain regions, e.g., raised or planar" (*id.*, 7:57-62) and an etch stop layer 113 that may be formed via a "conformal deposition process" (*id.*, 7:63-65). *See also* PA-02, 7:66-8:8.

Thus, a POSITA would have understood that the process and resulting structure of FIG. 2A discloses an example of a spacer (spacer 118) disposed on two

sides of a metal gate (gate 111) that has a truncated top surface consistent with Interpretations 1-3. Ex-03, ¶272. *See* Section II.D.1.

In Pham, the spacer 118 is formed by depositing a layer of spacer material adjacent the dummy gate structure followed by an anisotropic etching process on the layer of the spacer material. PA-02, 7:51-54. A POSITA would understand that during the anisotropic etching process, the spacer 118 is made shorter by removing a part of the spacer material from the top. Thus spacer 118 is truncated according to Interpretation 2. Thereafter, the dummy gate structure is replaced with the metal gate 111. *Id.*, 7:17-47. The spacer 118 (after its formation on the sides of the final metal gate structures) are planarized along with the metal gate structure 111 (e.g., using a CMP process) resulting in the spacer 118 and gate structure 111 having a planar top surface, where the spacer 118 was made shorter by removing a part (material from the top surface) during a planarization process that exposes the "upper surface of the gate structures 111" that are coplanar with the spacers 118 as shown in Figure 2A. A POSITA would understand that in order for the top surfaces of the spacers 118 and metal gate structures 111 to be coplanar following a CMP, some amount of the spacers 118 would have been removed during the CMP process. Thus spacers 118 are truncated according to Interpretations 1 and 3. The metal gate 111 and coplanar spacers 118 structures are similar to the coplanar metal gate stack structures 308 and spacers 502 portions in the FIG. 5A structure of Pethe.

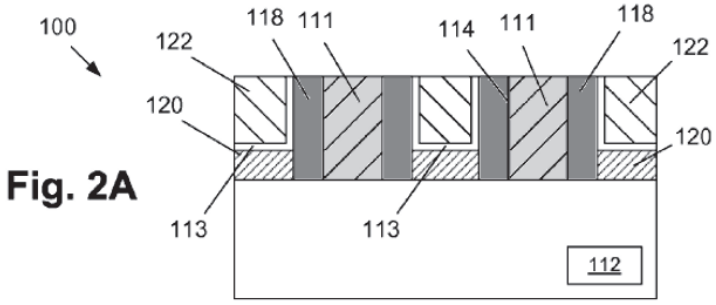


Fig. 2A

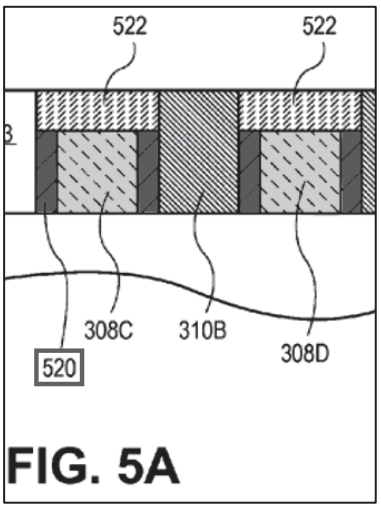


FIG. 5A

PA-02 (Pham) (FIG. 2A) PA-01 (Pethe) (FIG. 5A, excerpt)

Thus, in this example, a POSITA would have likewise understood Pham to disclose processes that would provide the metal gate and spacer structure arrangement included in Pethe's Figure 5 embodiment structure, in a compatible and similar manner. For instance, both Pethe and Pham provide versatile teachings, where, for example, permanent or replacement gate processes are applicable to the formation of the structure. *See e.g.*, PA-01 (Pethe), 7:60-8:1 ("gate stack structures 308A-308E may be fabricated by a replacement gate process…"), 8:12-23, 13:63-14:13 ("dummy gates need not ever be formed prior to fabricating gate contacts over active portions of the gate stacks" and "gate stacks described above may actually be permanent gate stacks as initially formed"), 17:7-9; PA-02 (Pham), 7:6-10 ("gate structures 111 are intended to be representative in nature of any type of gate structure that may be employed in manufacturing integrated circuit products using so-called gate-first or gate-last (replacement gate manufacturing techniques"), 7:10-47, 7:66-

8:8 (in FIG. 2A, "gate structures 111 are formed using a replacement gate manufacturing technique after several process operations have been performed, i.e., …dummy gate removal to thereby define the gate cavities 114 (between the spacers 118) where the final gate structures 111 will be formed, formation of various layers of material that will make up the gate structure 111 and after a CMP process was performed" thus exposing the "upper surface of the gate structures 111" in FIG. 2A). Ex-03, ¶¶273-274.

Thus, Pham discloses processes and structures where a spacer is disposed on two sides of a metal gate that has been made shorter by removing a part (including during a planarization process) and coplanar with the metal gate, similar to the structures in FIGs. 5A, 5B. Consequently, Pham discloses or suggests a semiconductor structure including spacers (e.g., spacer 118) disposed on two sides of a respective metal gate (e.g., gate 111), where the spacers each have a planar top surface (that is coplanar with the gate) and was made shorter by removing a part during a CMP or etch process, which is consistent with Interpretation 1 (planar top surface) and Interpretations 2, 3 (made shorter by removing a part (during a planarization process), and with the similar spacer / gate structures in the Figure 5 embodiment of Pethe. Ex-03, ¶275; §II.D.1.

As another example, Pham further discloses other fabrication processes, where a hard mask is disposed on the metal gates and sidewall spacers similar to that

in Pethe's Figures 5A-5B structures. For instance, with reference to Figures 2B-2D, Pham discloses processes where spacers 118 and etch stop layer 113 are further planarized during formation of gate cap layer 124 over the metal gates 111, spacers 118, and etch stop layer 113. Namely, with respect to FIG. 2A, Pham discloses etching portions of the metal gate structures 111 in the FIG. 2A structure to define a gate cap recess 111A. PA-02, 8:9-18, FIG. 2B (below). Ex-03, ¶276.

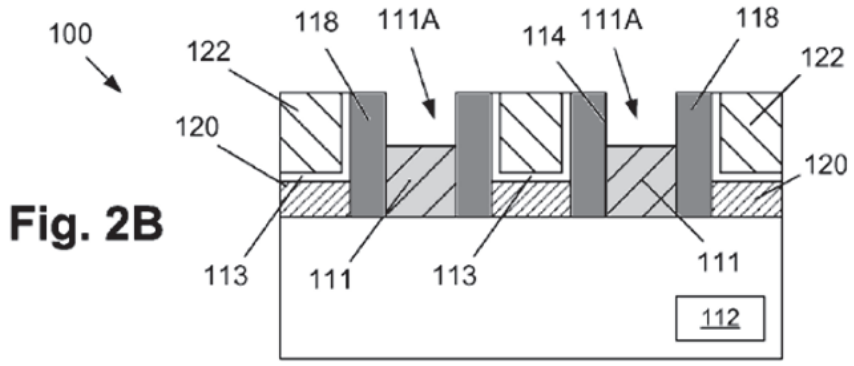


Fig. 2B

Next, Pham's process performs an etching process to "selectively **remove portions of the sidewall spacers 118 and the etch stop layer 113** to thereby define **recessed sidewall spacers 118A** and a **recessed etch stop layer 113A**." *Id.*, 8:19-37. As shown in FIG. 2C below, the etching processes results in forming a planar top surface for each recessed spacers 118A and the recessed etch stop layer 113A, both being coplanar with the recessed metal gate 111.

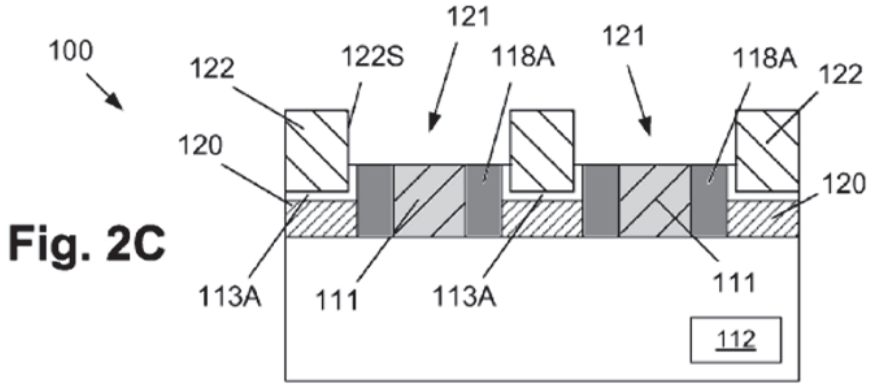


Fig. 2C

A POSITA would have recognized and understood the etching process disclosed by Pham as a planarization etching process because the top surface of each of the spacers 118A and the etch stop layer 113 have planar top surfaces consistent with planarization processes known at the time (e.g., known to include e.g., CMP and etching processes). *See* §I.C. In fact, the planar top surface of recessed spacers 118A and etch stop layer 113 are consistent with the planar top surface formed in FIG. 2A, which was formed by CMP processes (PA-02 (Pham), 7:66-8:8, FIG. 2A), and with the other structures disclosed by Pham that were subject to CMP processes (*e.g.*, *id.*, 7:41-47 (CMP of replacement metal gate resulting in planar top surface metal gate "depicted" in FIG. 2A), 8:38-56, FIG. 2D (CMP to remove gate cap layer 124 (discussed below)), 9:7-13, FIGs. 2E-2F (CMP process to remove portions of cate cap protection layer 126 having a planar top surface), 10:3-9, FIG. 2K (CMP "performed to planarize the upper surface of the layer of insulating material 128 which results in the removal of excess portions" of material above the layer). The planar top surfaces of Pham's recessed spacers 118 and recessed etch stop layer 113

formed by the etching for FIG. 2C is also similar to the "truncated top surface" of spacers 18 and CESL 20 formed by "another planarization process" as described by the '747 Patent. Ex-01, 3:16-19, FIG. 1. Ex-03, ¶278.

In connection with FIG. 2D, Pham discloses forming a gate cap layer 124 in each spacer/gate cap recess 121, which as noted above, is subject to a CMP process to planarize its respective top surface. PA-02, 8:38-58, FIG. 2D (below).

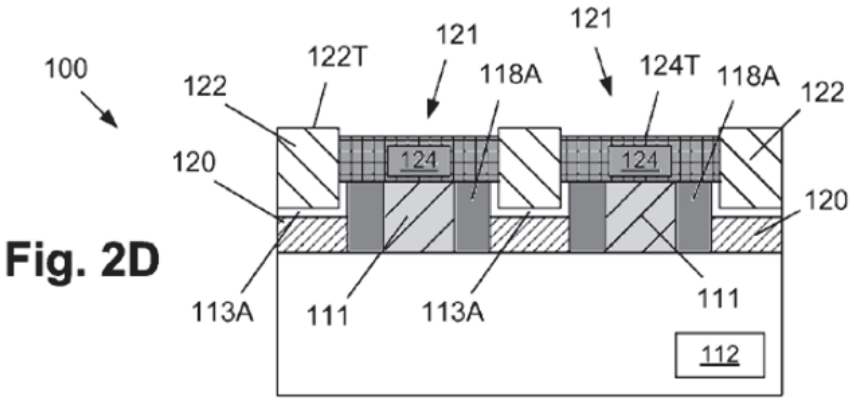


Fig. 2D

Thus, in this example, Pham describes a planarization process where spacers 118 and etch stop layer 113 (already disposed on two sides of the metal gate 111) are again made shorter by removing a part during a planarization process, resulting in each having a planar top surface (and thus meeting the Interpretations 1-3 for the claimed "truncated top surface" term (*see* §II.D.1). Additionally, Pham's FIGs. 2B-2D processes result in a semiconductor structural element configuration where a hard mask (e.g., cap layer 124) is disposed on the top of the metal gate (e.g., 111), spacers 118A, and etch stop layer 113, where the gate, spacer, and etch stop layer are coplanar have planar top surfaces on the same level with each other, that is

similar to the structural element configuration in the Figures 5A-5B structures (with cap layer 322 over gate structures 308 and spacers 502), as shown in comparison below.

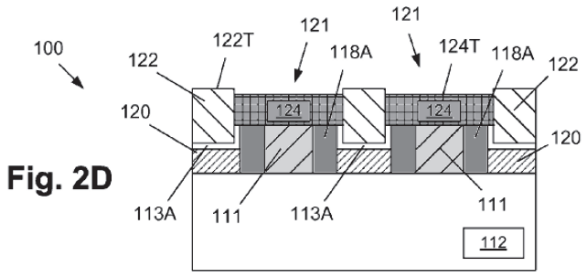


Fig. 2D

Pham (Fig. 2D)

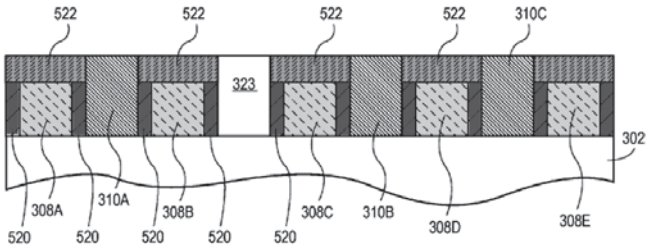


FIG. 5A

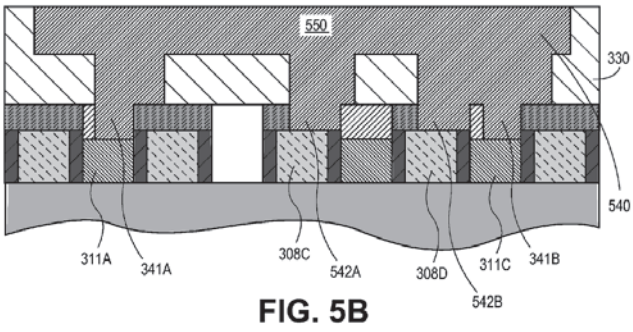


FIG. 5B

Pethe (FIGs. 5A-5B)

A POSITA would have thus recognized the similarities between Pethe and Pham that would have led them to consider their collective teachings to form various transistor device structures for given applications, like those contemplated by Pethe (*see e.g.*, PA-01, 14:1-15:38). Ex-03, ¶281. Indeed, a POSITA reviewing Pham's teachings and suggestions in context of Pethe's disclosures would have understood Pham to provide guidance on ways to form a structure similar to that in Pethe's Figure 5A structure, which leads to the structure in Figure 5B. *See* discussions above

in §§III.A, VI.A.1, 2. For example, upon considering Pham, a POSITA would have recognized and appreciated its teachings and guidance concerning the process details for implementing spacers in a structural element configuration like that in the Figure 5A structure, where spacers are disposed on two sides of a metal gate that have respective planar top surfaces that are covered by a hard mask. Ex-03, ¶281. Given such teachings and guidance providing details pertinent to the processes used to achieve spacers having a planar top (like those in Pethe), a POSITA would thus been motivated to configure and implement in Pethe's processes to form the structure of Figure 5B, where a planarization process(es) (e.g., planarization etching) is performed on previously formed spacers (on the sides of gate stack structures 308) to provide the recessed spacers 520 having a planar top surface that is coplanar with the metal gate structures 308 and have a hard mask disposed thereon, thus resulting in a structure like that in Figure 5B, from which to fabricate the resulting structure in Figure 5B.[18] Ex-03, ¶281.

[18] The combination of Pham and Pethe does not rely on a bodily incorporation of identical features (or implementation of identical processes) disclosed by Pham directly into the structure (or related process) of Pethe. Rather, the teachings and suggestions provided by Pham would have motivated a POSITA to modify or configure processes, consistent with Pham's disclosures, to fabricate and realize Pethe's FIG. 5B structure that includes a spacer disposed on the two sides of the

A POSITA would have recognized Pethe's teachings, including the description of the structure comprising recessed spacers 520 (that have planar top surfaces) in Pethe's FIG. 5 embodiment. *See* PA-01, FIG. 5A-5B, 12:15-67 (disclosing recessed spacer 520 having a planar top surface). To provide such structure—including spacers with planar top surfaces, as taught by Pethe—a POSITA would have considered the teachings of Pham (as discussed above) relating to the processes for forming similar types of "recessed sidewall spacers" (PA-02, 4:37-54, 8:19-58) including performing known planarization processes (e.g., planarization etching) on the spacers disposed on the sides of gate structures), and

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metal gate (e.g., gate stack structure 308C, or 308D as an example) having a planar top surface, consistent with the structure that Pethe discloses in FIGs. 5A-5B. Namely, Pham's teachings and suggestions regarding processes to form spacers on the sides of a metal gate, followed by a planarization to provide the spacers with a planar top surface from which subsequent structures and layers can be disposed, coupled with the teachings in Pethe (e.g., showing spacers with a planar top surface and related processes for providing the recessed spacers 520 in the FIG. 5B structure), coupled with the ordinary skill of a POSITA would have led a POSITA configure Pethe's fabrication processes to form spacers on the sides of the metal gates in gate stack structures 308 and perform planarization processes to provide the planar top surface shown in FIGs. 5A-5B, along with the other structures that are on the same level as recessed spacers 520, such as the gate stack structure 308. Ex-03, ¶281.

configure Pethe's processes to provide the recessed spacers with planar top surfaces like that shown in FIGs. 5A-5B. Ex-03, ¶282.

A POSITA would have recognized Pham's teachings and guidance regarding its recessed gate and spacer processes and resulting structures, along with Pham's guidance concerning decisions and efforts a person of ordinary skill in the art would take to have "benefit of [Pham's] disclosure" (PA-02, 6:1-34), in context of Pethe's similar guidance (*see e.g.*, PA-01, 2:50-63, 14:29-17:18), and tailored such processes to implement Pethe's spacers 520 with planar top surfaces and disposed on two sides of a metal gate structures 308 consistent with Pethe's FIGs. 5A-5B structures. Ex-03, ¶283. Implementation of such a modification would have predictably result in Pethe's process and structures being configured such that Pethe's spacers 502 and metal gate structures 308 were recess etched and planarized resulting in the spacers 502 and gate structures 308 having a planar top surface from which the cap layer 522 would be effectively deposited, consistent with the teachings of Pham (Pham's recessing process where spacers 118 and gate structures 111 are recess etched and planarized prior to deposition of the gate cap layer 124). PA-02, 7:66-8:8, FIGs. 2C-2D; Ex-03, ¶283. Such a modification and implementation would have accordingly, resulted in the spacers in Pethe's FIG. 5B structure have been made shorter by removing a part of the spacer during a planarization process (e.g., CMP, planarization etching process), consistent with the teachings of Pham. Ex-03, ¶283.

Accordingly, in light of the guidance by Pham in context of Pethe's teachings and a POSITA's state of art knowledge at the relevant time, a POSITA would have found it obvious to form the spacers 520 in Pethe's FIG. 5B structure by removing material from the spacers' top surface by known planarization processes in order to provide a planarized top surface spacer structure like that shown in the resulting FIG. 5B structure of Pethe. Ex-03, ¶284. Such features when implemented would have predictably resulted in spacers 520 having a "truncated top surface" consistent with Interpretation 1 (planar top surface) and Interpretations 2-3 (made shorter by removing a part (during a planarization process)). *See* §II.D.1.

A POSITA would have been recognized the benefits of providing known processes (like those of Pham) to provide the planar top surface structures in the FIGs. 5A-5B structures of Pethe. Ex-03, ¶285. For example, a POSITA would have appreciated and understood providing planar top surface structures, like the coplanar spacers and metal gate structures in Pham and Pethe, would have provided a flat, planar, surface upon which other material or layers can be formed during subsequent processing, like the deposition of flowable oxide of uniform thickness to form gate cap layer 124 in Pham, and the cap layers in Pethe's FIG. 5B structure. Ex-03, ¶285.

Likewise, a POSITA would have recognized advantages in providing such planar top surfaces and related structures according to known processes, similar to those taught by Pham (*e.g.*, PA-02, 7:5-8:8) and compatible with Pethe's approaches

(*e.g.*, PA-01, FIGS. 5A-5B). Ex-03, ¶286. Implementing features consistent with the above-discussed teachings and suggestions of Pham would have improved Pethe's manufacturing processes in a manner compatible with the ways Pethe contemplates forming structure 500. Such planarization had added importance in the context of scaling transistors to smaller dimensions, another aim of Pethe. *See* PA-01, 1:36-40; *see also id*., 1:14-26. The teachings of Pham are consistent with achieving such objectives in the context of related semiconductor manufacturing processes and structures. Ex-03, ¶286.

A POSITA would have had a reasonable expectation of success in implementing the above configuration and modification to Pethe's processes given it would have involved standard semiconductor manufacturing process (e.g., CMP, deposition, etching etc.) to provide known structural elements (e.g., spacers on the sides of metal gates), to facilitate the fabrication of a resulting structure applicable to related semiconductor device applications. Ex-03, ¶287. Such appreciation, coupled with their state of art knowledge and experience, would have led a POSITA to consider, develop, and implement successful fabrication processes and integration of known materials to achieve the structure like that shown in FIGs. 5A-5B with a reasonable expectation of success. *Id.* Upon such successful implementation (within the capabilities of such a POSITA), the resulting structure in the Pethe-Pham structure would have includes a spacer disposed on two sides of the metal gate

having a "truncated top surface" as interpreted under Interpretations 1-3 (*see* §II.D.1), similar to the spacers formed by Pham. For the reasons above, Pham renders obvious claim 1 and thus the claim is invalid in view of that prior art combination. Ex-03, ¶288; §§VI.A.1-3. *KSR*, 550 U.S. at 416.

c. Claims 2, 4, 5, and 8 [19]

Pethe in view of Pham discloses/suggests these limitations in view of the disclosures and suggestions in Pethe. *See* §§VI.A.1(b), 1(d), 1(e), 1(h), VI.A.2(a) above; *see also* Ex-03, ¶289.

d. Claim 3: The semiconductor device of claim 2, further comprising an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface.

Pethe in view of Pham discloses/suggests these limitations. Ex-03, ¶¶290-292.

Proposed Rejection 1A discusses how Pethe discloses the limitations in Claim 3 ("The semiconductor device of claim 2, further comprising an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface"). *See* VI.A.1(c). These discussions are incorporated herein to support

[19] As mentioned in §VI.A.2, Claim 1 does not recite a "semiconductor device." However, for purposes of analysis of the prior art, Requester assumes claims 2-9 refer to the semiconductor "structure" recited in claim 1.

Proposed Rejection 1C. In addition to the analysis in Proposed Rejection 1A (which is incorporated herein), for the reasons below and above in this Proposed Rejection 1C, the combined teachings and suggestions in Pethe and Pham disclose or suggest and render obvious Claim 3.

In particular, a POSITA would have found it obvious to implement an etching stop layer having a truncated top surface and disposed on two sides of the metal gate (e.g., the metal gate included in gate stack structure 308D) in the Pethe Figure 5B structure.[20]

For example, Pethe's teachings are discussed above for claim 3 in Proposed Rejection 1A (incorporated herein). As explained above, Pethe discloses forming an insulating cap layer 324 that is etched to form via openings 336 that are filled to form trench contact vias 341A/341B to the source and drain region. *See* PA-01, 9:36-43, 10:16-36. Pethe discloses forming insulating cap layer 324 and its

[20] A POSITA would have found it obvious to implement the etching stop layer with a truncated top surface feature in Pethe's Figure 5B structure does not mean Pethe does not disclose such a feature as claimed in Claim 3—Pethe does disclose the claimed etching stop layer for reasons discussed for Claim 3 in Proposed Rejection 1A. Rather, supported by the teachings and suggestions of Pham in context of Pethe's teachings, a POSITA would have found it obvious to form and implement an etching stop layer with a "truncated top surface" as claimed notwithstanding the disclosures in Pethe that I address above for Proposed Rejection 1A.

subsequent involvement in the fabrication of openings that are subsequently filled to form the trench and gate contact vias in the Figure 3F structure (similar to those in the Figure 5B structure). *Id.*, 8:24-36, FIG. 3B. Insulating cap layer 324 (and insulating cap layer 322) is involved in selective etching processes used to form openings 336 and 338, that are used to form the contact vias to the metal gates and source drain region in the semiconductor structure of FIG. 5B. *See id.*, 9:29-10:34, 10:38-51, 10:62-64, 11:23-42, 12:15-17, FIG. 5B. Insulating cap layer 324 protects specific portions of the semiconductor structure during the selective etching processes performed to form openings 338. Also explained above for claim 3 in Proposed Rejection 1A is that while not labeled in Figure 5B, the Figure 5B structure includes insulating cap layer 324, which is selectively etched (along with insulating cap layer 322) during fabrication processes disclosed by Pethe to form the openings 336 and 338 that are used to form the trench contact vias 341 and gate contact vias 342/542 in the Figure 3F and Figure 5B structures. *Id.* at 10:37-11:22, 12:15-17, FIG. 5B. *See* §VI.A.1(c).

Insulating cap layer 324 can be composed of silicon nitride, which was a known material used for spacer and etch stop layers in semiconductor structure fabrication. *See e.g.*, Ex-15 (Xiao), 164-65, FIGs. 5.46-5.47.

Thus, a POSITA would have appreciated Pethe's concern for protecting material, during etching processes. *See e.g.*, PA-01, 8:44-67, 9:40-43, 10:12-36; Ex-

03, ¶¶293-294. A POSITA was also familiar with and aware that contact etching stop layers (CESLs) and similar etch stop layers were commonly used and known semiconductor structural elements used in the fabrication of semiconductor devices, to protect conductive regions, such as the metal gate during etching processes common in semiconductor fabrication was prevalent at the relevant time. *See* Ex-15 (Xiao), 164-65; Ex-03, ¶¶293-294. The '747 Patent itself recognized that CESLs (including truncated top surface CESLs) were "elements" with "manufacturing methods thereof [were] well known to persons of ordinary skills in the art." Ex-01, 3:16-25.

Thus, the teachings and suggestions in context of Pethe and a POSITA's state of art knowledge relating to known semiconductor manufacturing processes would have led a POSITA to consider options for protecting material and structures during fabrication of Pethe's FIG. 5B semiconductor device. Ex-03, ¶295. A POSITA would have had reasons to explore the prior art and related state of art teachings to consider ways to fabricate Pethe disclosed semiconductor structure in the Figure 5 embodiment. *See* §VI.A.3.(b). For similar reasons, and those above, a POSITA would have looked to the art to consider options for improving or complementing the fabrication of the structural elements and layers in the structure. Ex-03, ¶295. In doing so, a POSITA would have found Pham an exemplary source of such guidance,

which discloses similar features, structural elements, and processes for similar semiconductor device applications. *Id.*

Pham's disclosures have been discussed in §VI.A.3(b) for limitation [1.d], including Pham's etch stop layer 113, which are incorporated herein.

In addition to the aforementioned disclosures, Pham explains the etch stop layer is used in some instance to "protect the []source/drain regions 120 during the etching process(es)." *Id.*, 9:42-47, FIG. 2I, 7:57-61.

Pham explains after the metal gate is formed between the spacers 118, "[a] CMP process is then performed. PA-02, 7:44-51, 7:54-61, FIG. 2A (annotated below, showing etch stop layer 113, spacers 118, and metal gate 111). Ex-03, ¶298.

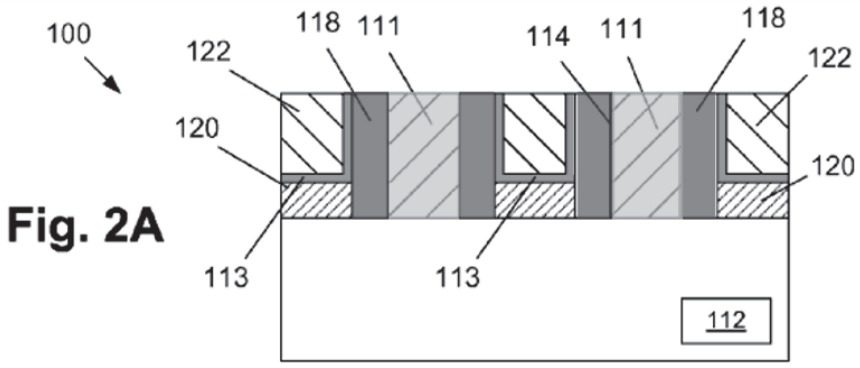

Fig. 2A

As mentioned, the source/drain regions 120 may be "any type of source/drain regions, e.g., raised or planar" (*id.*, 7:57-62) and the etch stop layer 113 that may be formed via a "conformal deposition process" (*id.*, 7:63-65.). *See also* 7:66-8:8.

Thus, a POSITA would have understood that the process and resulting structure of FIG. 2A discloses an example of an etching stop layer (etch stop layer

113) disposed on two sides of a metal gate (gate 111) that has a truncated top surface consistent with Interpretations 1-3. *See* §II.D.1. The etch stop layer 113 (after its formation on the sides of the final metal gate structures) are planarized along with the metal gate and spacers 118 (e.g., CMP process) resulting in the etch stop layer 113 having a planar top surface, where the etch stop layer 113 was made shorter by removing a part (material from the top surface) during a planarization process that exposes the "upper surface of the gate structures 111" that are coplanar with the spacers 118 and etch stop layer 113 as shown in FIG. 2A. Notably, while spacers 118 have been subject to an anisotropic etch prior to being planarized (PA-02, 7:51-54), the etch stop layer 113 is not subject to any prior etching step and is directly planarized (e.g., by CMP, *id.*, 8:4-8), together with the spacers 118 and metal gate 11. The metal gate 111, spacer 118, and coplanar etch stop layer 113 configuration is similar to the coplanar metal gate stack structures 308 and spacers 502 portions in the Figure 5A structure of Pethe. Ex-03, ¶300.

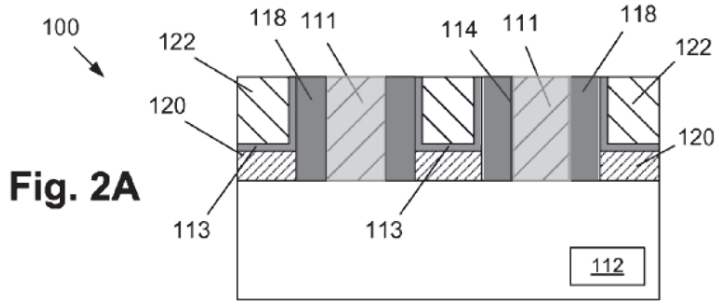

Fig. 2A

Pham (FIG. 2A)

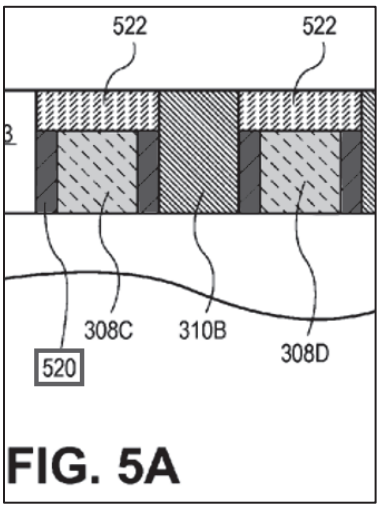

FIG. 5A

Pethe (FIG. 5A, excerpt)

Thus, in this example, a POSITA would have found options to provide further protection to e.g., the source/drain regions in Pethe's FIG. 5B structure during fabrication by providing an etch stop layer on the sides of the spacers 502 (and thus on the sides of each metal gate structure 308) during fabrication of the structural elements and layers in the FIG. 5B structure (which is used to fabricate the Figure 5B structure). Ex-03, ¶301. For instance, a POSITA would have appreciated and recognized Pham to disclose processes that would provide the metal gate and spacer structure arrangement included in Pethe's FIG. 5 embodiment structure, in a compatible and similar manner, while also provide the ability to include a etch stop layer (consistent with that disclosed by Pham) to integrate protection to material during the etching processes in Pethe's fabrication processes, consistent with that widely known use of CESLs in the art. *Id.* Indeed, a POSITA would have

understood that both Pethe and Pham provide versatile teachings, where, for example, permanent or replacement gate processes are applicable to the formation of the structure. *See e.g.*, PA-01, 7:60-8:1 ("gate stack structures 308A-308E may be fabricated by a replacement gate process…"), 8:12-23 ("approaches described herein contemplate essentially a dummy and replacement gate process in combination with a dummy and replacement contact process to arrive at structure 300" in FIG. 3A, which is similar to FIG. 5A (using recessed spacers)), 13:63-14:13 ("dummy gates need not ever be formed prior to fabricating gate contacts over active portions of the gate stacks" and "gate stacks described above may actually be permanent gate stacks as initially formed"), 17:7-9; PA-02, 7:6-10 ("gate structures 111 are intended to be representative in nature of any type of gate structure that may be employed in manufacturing integrated circuit products using so-called gate-first or gate-last (replacement gate manufacturing techniques"), 7:10-47, 7:66-8:8 (in FIG. 2A, "gate structures 111 are formed using a replacement gate manufacturing technique after several process operations have been performed, i.e., …dummy gate removal to thereby define the gate cavities 114 (between the spacers 118) where the final gate structures 111 will be formed, formation of various layers of material that will make up the gate structure 111 and after a CMP process was performed" thus exposing the "upper surface of the gate structures 111" in FIG. 2A). *Id.*

Thus, Pham discloses and provided guidance to those of ordinary skill in the art at the relevant time of processes and structures where a spacer and etch stop layer are disposed on two sides of a metal gate, where the etch stop layer (and spacer) has been made shorter by removing a part (including during a planarization process) and resulting in a planar top surface that is coplanar with the metal gate, similar to the FIGs. 5A-5B structure's metal gate/spacer top surface configurations. Consequently, Pham discloses or suggests a semiconductor structure including an etching stop layer (e.g., etch stop layer 113) disposed on two sides of a respective metal gate (e.g., gate 111), where the etch stop layer has a planar top surface (that is coplanar with the gate (and spacer)) and was made shorter by removing a part during a CMP or planarization etch process, which is consistent with Interpretation 1 of "truncated top surface" (planar top surface) and Interpretations 2-3 of "truncated top surface" (made shorter by removing a part (during a planarization process), and with the similar spacer / gate planar top surface structures in the Figure 5 embodiment of Pethe. *See* §II.D.1. Ex-03, ¶302.

As another example, Pham further discloses other fabrication processes, where a hard mask is disposed on the metal gates and sidewall spacers similar to that in Pethe's FIGs. 5A-5B structures. Pham's process also disposes the hard mask on the etch stop layer 113 along with the spacers 118 and metal gate structure 111. Ex-03, ¶303.

For instance, with reference to FIGs. 2B-2D, Pham discloses processes where spacers 118 and etch stop layer 113 are further planarized during formation of gate cap layer 124 over the metal gates 111, spacers 118, and etch stop layer 113. Namely, with respect to FIG. 2A, Pham discloses etching portions of the metal gate structures 111 in the FIG. 2A structure to define a gate cap recess 111A. PA-02, 8:9-18, FIG. 2B (below). Ex-03, ¶304.

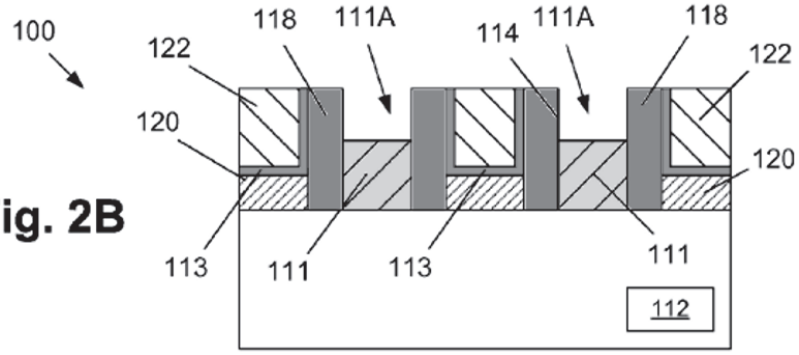

Fig. 2B

Next, Pham's process performs an etching process to "selectively **remove portions of the sidewall spacers 118 and the etch stop layer 113** to thereby define **recessed sidewall spacers 118A** and a **recessed etch stop layer 113A**." *Id.*, 8:19-37. As shown in FIG. 2C below, the etching processes results in forming a planar top surface for each recessed spacers 118A and the **recessed etch stop layer 113A**, both being coplanar with the recessed metal gate 111. Ex-03, ¶305.

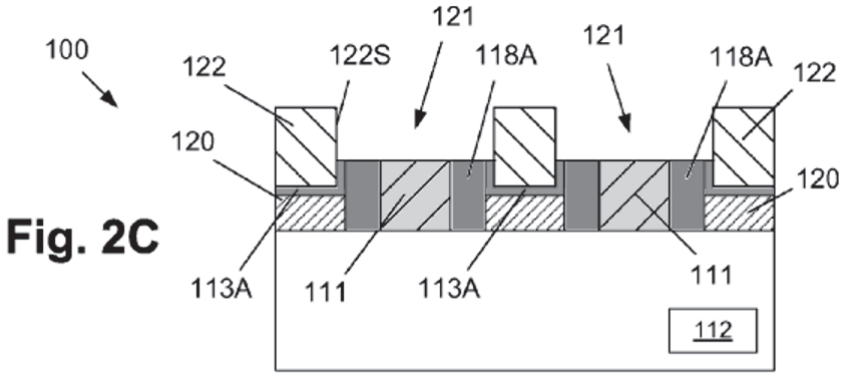

Fig. 2C

A POSITA would have recognized and understood the etching process disclosed by Pham as a planarization etching process because the top surface of each of the spacers 118A and the etch stop layer 113 have planar top surfaces consistent with planarization processes known at the time (e.g., known to include e.g. CMP and etching processes). *See* §I.C. In fact, the planar top surface of recessed spacers 118A and etch stop layer 113 are consistent with the planar top surface formed in Figure 2A, which was formed by CMP processes (PA-02, 7:66-8:8, FIG. 2A), and with the other structures disclosed by Pham that were subject to CMP processes (*e.g.*, *id.*, 7:41-47 (CMP of replacement metal gate resulting in planar top surface metal gate "depicted" in FIG. 2A), 8:38-56, FIG. 2D (CMP to remove gate cap layer 124 (discussed below)), 9:7-13, FIGs. 2E-2F (CMP process to remove portions of cate cap protection layer 126 having a planar top surface), 10:3-9, FIG. 2K (CMP "performed to planarize the upper surface of the layer of insulating material 128 which results in the removal of excess portions" of material above the layer). The planar top surfaces of Pham's recessed spacers 118 and **recessed etch stop layer**

113 formed by the etching for FIG. 2C is also similar to the "truncated top surface" of spacers 18 and CESL 20 formed by "another planarization process" as described by the '747 Patent. Ex-01, 3:16-19, FIG. 1; Ex-03, ¶306.

In connection with Figure 2D, Pham discloses forming a gate cap layer 124 in each spacer/gate cap recess 121, which as noted above, is subject to a CMP process to planarize its respective top surface. PA-02 (Pham), 8:38-58, FIG. 2D (below); Ex-03, ¶307.

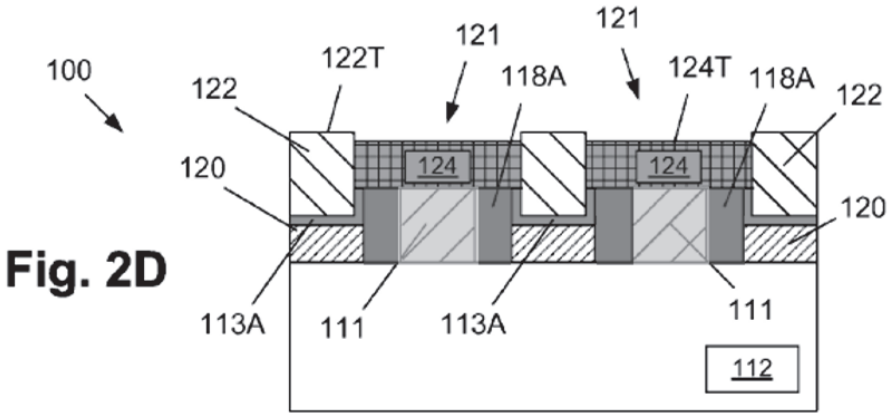

Fig. 2D

Thus, in this example, Pham describes another planarization process where spacers 118 and **etch stop layer 113** (previously formed and disposed on two sides of the metal gate 111) are again made shorter by removing a part during a planarization process, resulting in the etch stop layer 113 and spacer 118 each having a planar top surface (and thus meeting the Interpretations 1-3 for the claimed "truncated top surface" term). *See* §II.D.1. Additionally, Pham's Figures 2B-2D processes result in a semiconductor structural element configuration where a hard

mask (e.g., cap layer 124) is disposed on the top of the metal gate (e.g., 111), spacers 118A, and etch stop layer 113, where the gate, spacer, and etch stop layer are coplanar have planar top surfaces on the same level with each other, that is similar to the structural element configuration in the FIGs. 5A-5B structures (with cap layer 322 over gate structures 308 and spacers 502), as shown in comparison below. Ex-03, ¶308.

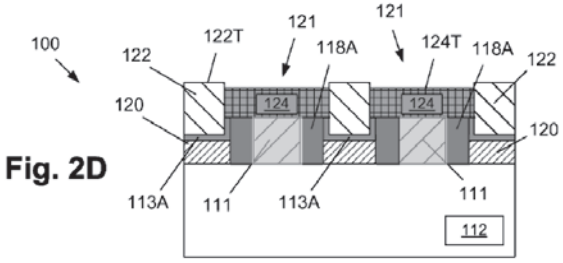

Fig. 2D

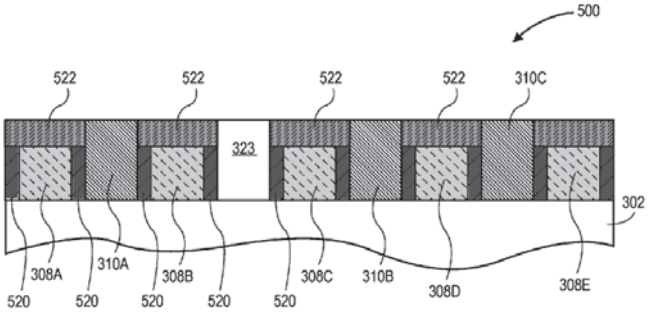

FIG. 5A

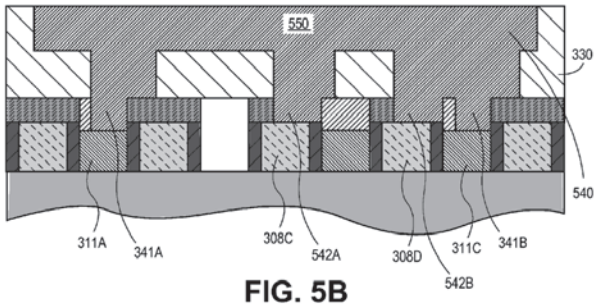

FIG. 5B

Pham (Fig. 2D) Pethe (FIGs. 5A-5B)

A POSITA would have thus recognized the similarities between Pethe and Pham that would have led them to consider their collective teachings to form various transistor device structures for given applications and do so by employing known

protective layers (e.g., etch stop layer 113) that were common place in the fabrication of semiconductor devices, like those contemplated by Pethe (*see e.g.*, PA-01, 14:1-15:38). Indeed, a POSITA reviewing Pham's teachings and suggestions in context of Pethe's disclosures would have understood Pham to provide guidance on ways to form a structure similar to that in Pethe's FIG. 5A structure with the added protection of an etch stop layer to further protect portions of the source/drain regions in Pethe's structure during subsequent etching processes, which leads to the structure in Figure 5B (following processes similar to those described in the Figure 3 embodiment. *See* §§III.A, VI.A.1-2; Ex-03, ¶309.

For example, upon considering Pham, a POSITA would have recognized and appreciated its teachings and guidance concerning the process details for implementing etch stop layers in a structural element configuration like that in the FIG. 5A structure, where an etch stop layer is disposed on two sides of a metal gate (e.g., gate contact structure 308) and spacers 502 that have respective planar top surfaces that are covered by a hard mask, similar to that taught and suggested by Pham (*see e.g.*, PA-02, FIG. 2D). Ex-03, ¶310. Given such teachings and guidance providing details pertinent to the processes used to achieve etching stop layer (and other structures, such as spacers) having a planar top (like the structures in FIG. 5A in Pethe), a POSITA would thus been motivated to configure and implement in Pethe's processes to form the structure of FIG. 5B, where a planarization process(es)

(e.g., CMP, planarization etching) is performed on previously formed etch stop layer and spacers (each disposed on the two sides of gate stack structures 308) to provide a recessed etch stop layer (e.g., like recessed stop layer 113A and recessed spacers 118) similar to the recessed spacer 520 structures in Pethe. *Id.* Such recessed etch stop layer and recessed spacers implemented in Pethe's FIG. 5B structure would have had a planar top surface that is coplanar with the metal gate structures 308, and a hard mask disposed thereon the upper surfaces of those elements, thus resulting in a structure similar to that described for FIG. 5B, from which to fabricate the resulting structure in FIG. 5B.[21] *Id.*

[21] The combination of Pham and Pethe do not rely on a bodily incorporation of identical features (or implementation of identical processes) disclosed by Pham directly into the structure (or related process) of Pethe. Rather, the teachings and suggestions provided by Pham would have motivated a POSITA to modify or configure processes, consistent with Pham's disclosures, to fabricate and realize Pethe's FIG. 5B structure that includes a spacer disposed on the two sides of the metal gate (e.g., gate stack structure 308C, or 308D as an example) and an etch stop layer that is disposed on the two sides of the metal gate (similar to that shown by Pham), where each of the structures have a planar top surface, consistent with the elements in the FIGs. 5A-5B structure of Pethe. Namely, Pham's teachings and suggestions regarding processes to form an etching stop layer and spacers on the sides of a metal gate, followed by a planarization to provide the etching stop layer

A POSITA would have recognized Pethe's teachings, including the description of the structure comprising recessed spacers 520 (that have planar top surfaces) in Pethe's FIG. 5 embodiment and the use of protective layers (e.g., cap layers 322 and 324) and thus been motivated to modify Pethe's fabrication processes and resulting structure to include etching stop layer (like that claimed in Claim 3). *See* PA-01, FIGs. 5A-5B, 12:15-67 (disclosing recessed spacer 520 having a planar top surface). To provide such structure, a POSITA would have considered the teachings of Pham (as discussed above) relating to the processes for forming similar types of "recessed sidewall spacers" and "recessed etch stop layer" (PA-02, 4:37-54, 8:19-58) including performing known planarization processes (e.g., CMP, planarization etching) on the spacers and etch stop layer disposed on the sides of gate structures), and configure Pethe's processes to provide similar features using

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and spacers with planar top surfaces from which subsequent structures and layers can be disposed, coupled with the teachings in Pethe (e.g., showing spacers with a planar top surface and related processes for providing the recessed spacers 520 in the FIG. 5B structure) would have led a POSITA configure Pethe's fabrication processes to form an etching stop layer and spacers on the sides of the metal gates in gate stack structures 308 and perform planarization processes to provide planar top surfaces for the etching stop layer and spacers in the modified structure similar to the spacer and metal gate structures shown in FIGs. 5A-5B, which are on the same level like that described by Pham's structures (e.g., PA-02 (Pham), FIGs. 2A, 2D).

fabrication processes that are designed and configured to result in Pethe's FIG. 5B structure including a protective etch stop layer (with a planar top surface formed by removing a part and making shorter) on two sides of the metal gates (and spacers). Ex-03, ¶311.

A POSITA would have had reasons to consider and glean from the teachings of Pham to provide such an etch stop layer in Pethe's structure. Indeed, Pham's teachings are consistent with the known use of an etching stop layer having a truncated top surface as understood by those of ordinary skill in the art at the time. For example, PA-03 (Huang) discloses a Contact Etch Stop Layer (CESL) 36 that is a dielectric material acting as "an etch stop layer" disposed on two sides of a gate dielectric 24 and gate electrode 26. *See e.g.,* PA-03, [0008]-[0010], [0014], FIG. 1 (below). Ex-03, ¶312.

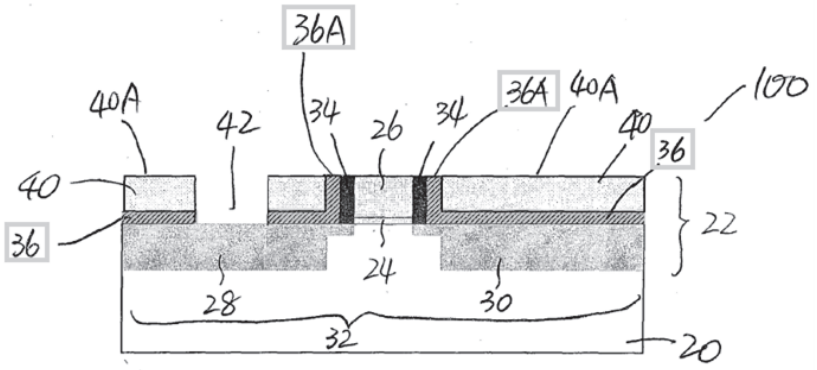


Fig. 1

A POSITA would have understood that CESL 36 is an etch stop layer to protect source/drain region (30) against etching of an opening (56) so etching stops on CESL 36, as shown in Figure 6 (below). Ex-03, ¶313.

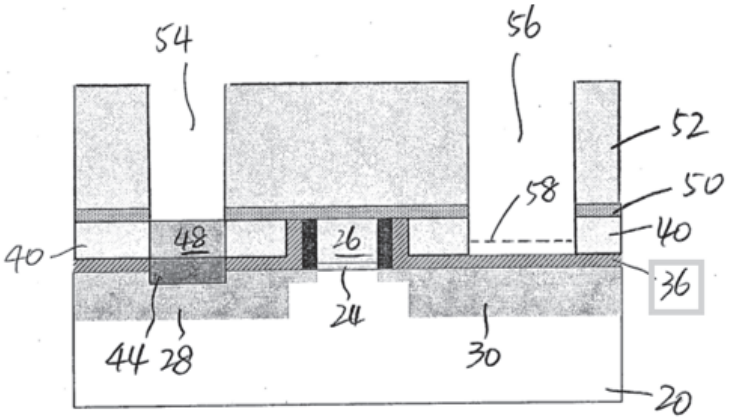


Fig. 6

As shown and described, Huang's etching stop layer 36 has top edges 36A that are planar, that were formed by CMP processes during Huang's last gate approach processes. *See e.g.*, PA-03 (Huang), [0009]. *See also* Ex-15 (Xiao), 544-545 (describing such an approach known at the relevant time).

As another example of such state of the art knowledge, Sell (PA-06) discloses the conventional use of an etching stop layer disposed on two sides of a metal gate having a planar top surface formed by a planarization process consistent with that known in the art at the relevant time. *See e.g.*, PA-06, FIGs. 1a-1c, 1e-1f, 1:50-2:22 (describing metal gate structures, spacer material 106, and "a nitride etch stop layer (nesl) 108, that may be adjacent and in direct contact with the spacer material 106

… [and] may serve as an etch stop layer in some embodiments"), 2:23-34, 2:35-49 ("the etching process may comprise an oxide etch that may be selective to the nitride etch stop layer (nesl) 108 and to the spacer material 106, and may remove the first ILD 110 in a substantially anisotropic manner, leaving the nesl 108 and the spacer material 106 substantially intact"), 2:62-3:5 ("the nitride etch stop layer 108 may be removed that is disposed on a portion of the source/drain region 103 of the substrate 100 utilizing a nitride etching process, for example, so that a source/drain contact area 107 may be exposed (FIG. 1 c)"), 3:17-43). Ex-03, ¶315.

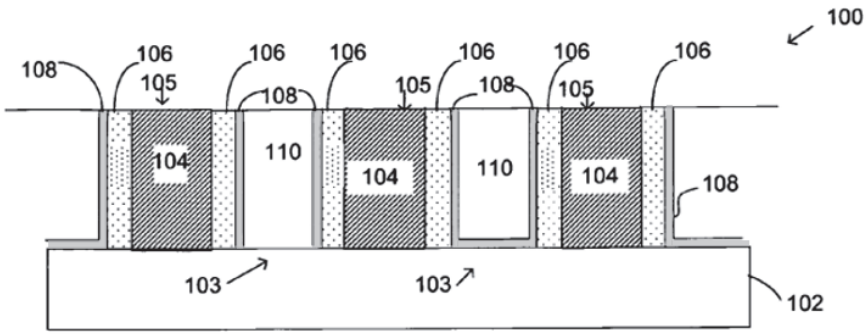


FIG. 1a

Liang (Ex-27) similarly confirms a POSITA's understand of the known use of etching stop layers in semiconductor structures similar to that disclosed by Pethe and Pham. *See* Ex-27, FIGs. 1A-1H, 2:50-65 ("An etch-stop layer 107 can be formed over the substrate 101 and adjacent to sidewalls of the gate electrode 103"), 3:20-41, 4:5-17 ("The etch- stop layers 107 and 111 can have at least one material such as silicon carbide (SiC), silicon nitride (SiN), silicon carbon nitride (SiCN),

silicon carbon oxide (SiCO), silicon oxynitride (SiON), boron nitride (BN), boron carbon nitride (BCN), other material that has a desired selectivity with respect to silicon oxide, or any combinations thereof. The etch-stop layers 107 and 111 can be formed by any suitable process …"). *See also id.*, 1:56-2:23. Ex-03, ¶316.

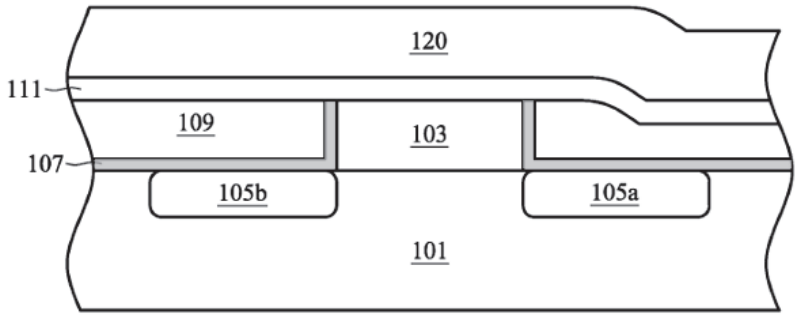


FIG. 1A

These teachings are consistent with the state of art knowledge of etching stop layers, including those that were made shorter by removing a part (including during a planarization process) and having a planar top surface as understood by a POSITA at the relevant time. Ex-03, ¶317.

In light of the guidance by Pham in context of Pethe's teachings and a POSITA's state of art knowledge at the relevant time, a POSITA would have found it obvious to include an etching stop layer in the fabrication and resulting structure of Pethe's Figure 5B structure to provide etch protection to structural elements and layers (such as source/drains, spacers, and gate structures) in the fabrication of Pethe's structure. Ex-03, ¶318. *See*, *e.g.*, PA-01 (Pethe), 3:25-29 ("Source or drain

contacts (also known as trench contacts), such as contacts 110A and 110B, are disposed over source and drain regions of the semiconductor structure or device 100A. Trench contact vias 112A and 112B provide contact to trench contacts 110A and 110B, respectively. "), 4:33-37, 7:25-34. *See also* PA-02 (Pham), 9:42-47 (etch stop layer provides protection to source/drain regions 120). A POSITA would have been further motivated by Pethe's use of similar cap or protection layers (e.g., cap layer 324) and coupled with the teachings and suggestions in Pham, would have looked to provide such conventional features in Pethe's structure to ensure the etching processes used to fabricate the resulting structure results in an operational semiconductor device that performs in accordance with the appropriate application in the computing devices contemplated by Pethe (e.g., PA-01, 14:15-15:38). Ex-03, ¶318.

In light of such teachings of Pham, Pethe, and state of art knowledge, a POSITA would have been motivated and found obvious to form and process an etching stop layer disposed on two sides of the metal gate (e.g., a metal gate in gate stack structure 308D, etc.) by removing material from the etching stop layer's top surface using known planarization processes (e.g., CMP or planarization etch processes) in order to provide a planarized top surface etch stop layer consistent with structures and features shown in the resulting FIG. 5B structure of Pethe. Such an implementation would have predictably resulted in an etching stop layer having a

truncated top surface as claimed and consistent with Interpretation 1 (planar top surface) and Interpretations 2-3 (made shorter by removing a part (during a planarization process). *See* §II.D.1; Ex-03, ¶319.

A POSITA would have appreciated providing an etching stop layer in Pethe's structure in a manner consistent with known fabrication processes (like that described by Pham) would have beneficially provided protection to e.g., transistor gate structures, source/drain regions, and other structural elements in Pethe's structure. *See e.g.*, Ex-15 (Xiao), 164-65, 341-45. Ex-03, ¶320. A POSITA would have also appreciated the benefits in providing an etching stop layer with a planar top surface because, for example, such planarized top surfaces were known to aid in the formation of subsequently formed structural elements and layers during subsequent fabrication processes (e.g., photolithography steps) that deposit such elements or layers on the top surface of the planarized surface. Such planarization had added importance in the context of implementing integrated circuit "products with increased capacity," an aim of Pethe (*see* PA-01, 1:20-23), where issues of non-planarity could compound given the many layers needed to implement and interconnect the product "with increased capacity." Such planarization had added importance also in the context of scaling transistors to smaller dimensions, another aim of Pethe, given the "constraints on the lithographic processes used to pattern these" ever smaller transistors. *See* PA-01, 1:36-45; *see also id*., 1:14-26.

Accordingly, a POSITA would have been motivated to look to ways to provide such protection while promoting effective fabrication processes as known in the art. Ex-03, ¶320.

A POSITA would have reasonably expected success in implementing the above modification/configuration to Pethe's FIG. 5B structure because providing an etching stop layer with a planar top surface (formed by removing a part and making the layer shorter during a planarization process like that disclosed by Pham) would have involved nothing more than applying known semiconductor manufacturing process (e.g., deposition, CMP, etching, etc.) for forming the etching stop layer on the sides of Pethe's metal gates in gate stack structure(s) 308, where the etching stop layer was also planarized to provide a protective layer that had a surface conducive to subsequent formation of other structures and layers formed above e.g., the etching stop layer, spacers, and e.g., metal gate stack structures 308. Designing, configuring, and implementing such an etching stop layer in the Pethe structure would have been within the skill, knowledge, and capabilities of a POSITA at the relevant time. Ex-03, ¶321.

Further, a POSITA would have understood and appreciated that providing an etching stop layer would have been an obvious example of combining prior art elements according to known methods (e.g., combining the teachings of Pham with those of Pethe in accordance with known semiconductor device fabrication

processes (e.g., forming known etch stop layers, polishing or planarization etching processes, etc.). Ex-03, ¶322.

A POSITA would have leveraged their state of art knowledge and experience in considering the design needs and the market demands for computing devices that include a semiconductor structure as contemplated by Pethe (PA-01, 14:29-15:38) and Pham (PA-02, 6:3-14) and thus would have been capable of configuring and designing fabrication processes to successful provide such an etching stop layer in the FIG. 5B structure with a "truncated top surface" (as interpreted under Interpretations 1-3 (*see* §II.D.1)). Ex-03, ¶323.

Accordingly, for the reasons above, the combination of Pethe and Pham discloses and/or suggests the semiconductor structure including an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface as recited in Claim 3 (under Interpretations 1-3 of "truncated top surface," *see* Section VI.D.1). Ex-03, ¶324.

For the reasons above, Pethe in view of Pham renders obvious claim 3 and thus the claim is invalid in view of that prior art combination. Ex-03, ¶324; §§VI.A.1.a-f. *KSR*, 550 U.S. at 416.

e. Claim 6: The semiconductor device of claim 1, further comprising at least one fin structure disposed on the substrate.

Pethe in view of Pham discloses/suggests these limitations. *See* §§VI.A.1(f), VI.A.2(h) above.

Proposed Rejection 1A discusses how Pethe discloses the limitations in Claim 6. Proposed Rejection 1B discusses how the collective teachings and suggestions in Pethe further renders obvious the limitations in Claim 6. The discussion in Proposed Rejections 1A and 1B are incorporated herein to support Proposed Rejection 1C. Additionally, for the reasons below and above in Proposed Rejection 1C, the combined teachings and suggestions in Pethe and Pham disclose or suggest, and render obvious Claim 6[22].

Pethe discloses that the semiconductor device of Pethe's invention can be implemented with tri-gate or FinFET transistors, which were known to include fin structures. PA-01, 14:8-11. *See also id.*, 1:27-45 (Pethe recognizing that "multi-

[22] That a POSITA would have found it obvious to implement Pethe's Figure 5B structure with at least one fin structure disposed on the substrate does not mean Pethe does not disclose such a feature as claimed in Claim 6—Pethe does disclose the claimed fin structure for reasons Discussed for Claim 6 in Proposed Rejection 1A. Rather, a POSITA would have found it obvious to form and implement a fin structure as claimed in Pethe's structure notwithstanding the disclosures in Pethe that are addressed above for Proposed Rejection 1A.

gate transistors, such as tri-gate transistors, have become more prevalent" and "fabricated on bulk silicon substrates of silicon-on-insulator substrates"). Further, Pethe describes its semiconductor structures in context of non-planar devices that include fin structures. *See e.g.*, PA-01, 5:36-48 (discussing the Figure 2 embodiment where "the semiconductor structure or device 200 is a non-planar device such as, but not limited to, a fin-FET or a tri-gate device"), 4:62-5:12, FIG. 2C (describing the fin structure in Figure 2C (showing a "tri-gate transistor" with a "fin structure" 204C), 11:43-54, FIG. 4 (showing a non-planar deice with a "fin structure"), 17:14-18 (discussing "forming [a] three-dimensional body [by] etching fins in a bulk semiconductor substrate"). *See also e.g., id.*, 3:60-67, 4:65-5:3, 11:49-52; *id.*, 5:35-39, 6:7-12 ("fin active regions"). Pethe also explains that the Figure 5 embodiment's gate structure "may include a gate dielectric layer and a gate electrode, as described above in FIG. 2," which discloses a multi-gate transistor having a fin structure. *Id.*, 12:39-42; *id.*, 4:62-5:5; FIG. 2C. *See also* §§III.A, VI.A.1-2; Ex-03, ¶¶327-328.

Pethe also discloses similar features in connection with the Figure 3 embodiment as shown in FIG. 4. *See* PA-01, 11:43-54 ("a semiconductor structure or device 400, e.g. a non-planar device, includes a non-planar diffusion or active region 404 (e.g., **a fin structure**) formed from substrate 402"), 14:4-13 ("the semiconductor devices have a three-dimensional architecture, such as a trigate

device, an independently accessed double gate device, or **a FIN-FET**"), FIG. 4 (below). Ex-03, ¶329.

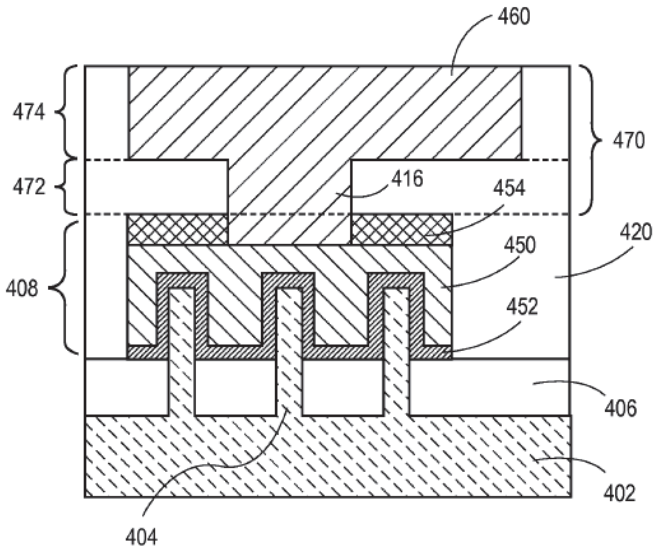


FIG. 4

Pethe also explains that the disclosed method may include "prior to forming the plurality of gate structures, forming a three-dimensional body from the active regions of the substrate" and that "forming the three-dimensional body includes etching fins in a bulk semiconductor substrate." PA-01 (Pethe), 17:14-18. A POSITA would have understood such teaching refers to the non-planar diffusion or active region in the above-discussed "fin structure(s)." *See e.g., id.*, 3:60-67, 4:65-5:3, 11:49-52; *id.*, 5:35-39, 6:7-12 ("fin active regions"). Ex-03, ¶329.

In light of such disclosures in Pethe, a POSITA considering the semiconductor structure disclosed by Pethe would have been motivated to look to and consider

teachings in the art for ways to improve the semiconductor device structure through implementation of FinFET or tri-gate technologies to promote the application of the structure in the types of computing devices contemplated by Pethe. *See e.g.*, PA-01, 14:29-15:38; *see id.*, 14:1-14 (contemplated FinFET or tri-gate devices). Ex-03, ¶330. In doing so, a POSITA would have considered the teachings and suggestions in Pham.

Pham's disclosures have been discussed in §VI.A.3(b) for limitation [1.d], and §VI.A.3(d) for Claim 3, which are incorporated herein. Pham additionally discusses the well-known features of FinFET devices. PA-02 (Pham), 1:54-61. *See also id.*, 1:61-2:20 (explaining that "When an appropriate voltage is applied to the gate electrode of a FinFET device, **the surfaces (and the inner portion near the surface) of the fins, i.e., the substantially vertically oriented sidewalls and the top upper surface of the fin** with inversion carriers, contributes to current conduction" and "In short, the 3D structure of a FinFET device is a superior MOSFET structure as compared to that of a planar FET, especially in the 20 nm CMOS technology node and beyond"), 6:66-7:5 ("**the inventions disclosed herein may be applied to the formation of** planar FET devices **as well as 3D devices, such as FinFET devices**"). Ex-03, ¶¶331-334.

A POSITA was well aware of, and had experience with, FinFET type transistor devices and related structures consistent with those contemplated by Pethe

and Pham. Indeed, for example, FinFET devices were well known to include fin structures, like that described by Pethe (FIGs. 2C, 4) and Pham. *See also e.g.*, Ex-15 (Xiao), 72-74, 351; Ex-03, ¶335.

A POSITA would have appreciated and recognized the benefits of implementing the FIG. 5B structure of Pethe as a non-planar structure with a tri-gate or FinFET transistor, such as scaling to minimize the footprint of the integrated circuit implementing such transistors, consistent with that contemplated by Pethe. *See* PA-01 (Pethe), 1:14-45, 14:29-15:38; PA-02 (Pham), 1:5-2:46. *See also* Ex-15 (Xiao), FIG. 15.1, 650-51 (describing features consistent with a POSITA's state of art knowledge at the relevant time such as the known use of "a trigate, [where] fabs can use the same lithographic technology to reduce transistor dimensions while maintaining the same performance, or to improve device performance without increasing device density" and where "IC manufacturers can further improve device performance by making the fin taller" and that "a finFET is easier to build than a trigate. Intel's 22-nm IC chips are built with trigate devices"). Ex-03, ¶336

In light of such knowledge and experience, and in context of Pethe's and Pham's teachings and suggestions, a POSITA would have been motivated to configure the FIG. 5B structure with a fin structure disposed on top of substrate 302, consistent with known Fin-FET and tri-gate transistor semiconductor structure configurations at the relevant time and taught by Pham and Pethe. Ex-03, ¶337.

A POSITA's knowledge and experience in context of the teachings and suggestions of Pham and Pethe would have led them to implement such fin structure features in the FIG. 5B structure with a reasonable expectation of success that the semiconductor structure would provide functional transistor operations consistent with the application of the structure in the various types of computing devices that Pethe contemplates. Ex-03, ¶338. For instance, a POSITA would have recognized that implementing such features would have involved applying known semiconductor fabrication processes and structural elements (e.g., FinFETs, tri-gate transistors and related fabrication processes like those taught by Pham and Pethe) that were within the capabilities and knowledge of a POSITA at the relevant time. Indeed, as explained above, Pham and Pethe each expressly discloses semiconductor structures with fin structures (PA-01 (Pethe), FIGs. 2C, 4; PA-02 (Pham), 6:66-7:5), thus expressly guiding a POSITA to integrate the same with the FIG. 5B structure. Also, a POSITA would have considered the design needs for such applications, relevant market demands, and related factors and thus found implementing Pethe's structure as a FinFET or tri-gate type device, especially in view of the guidance in Pham. Ex-03, ¶338.

Accordingly, in view of the combined teachings and suggestions of Pethe in view of Pham, a POSITA would have found it obvious to configure the Pethe FIG. 5B structure to include at least one fin structure disposed on the substrate of the

structure, as recited in Claim 6 of the ’747 Patent. Thus, for the reasons here, and those further above for Proposed Rejection 1B, Pethe and Pham discloses and/or suggests, and renders obvious Claim 6 of the ’747 Patent. For the reasons above, Pethe in view of Pham renders obvious claim 6 and thus the claim is invalid in view of that prior art combination. Ex-03, ¶339.

f. Claim 7: The semiconductor device of claim 1, further comprising a salicide layer disposed between each S/D region and each first contact.

Pethe in view of Pham discloses/suggests these limitations. See §§VI.A.1(g), VI.A.2(i) above. The discussion in Proposed Rejections 1A and 1B are incorporated herein to support Proposed Rejection 1C. Additionally, for the reasons below and above in this Proposed Rejection 1C, the combined teachings and suggestions in Pethe and Pham disclose or suggest, and render obvious Claim 7[23]. Specifically, in Proposed Rejection 1B, it was discussed that a POSITA would be motivated to

[23] A POSITA would have found it obvious to implement a salicide layer disposed between each S/D region and each trench contact via (first contact) in Pethe’s FIG. 5B structure does not mean Pethe does not disclose such a feature as claimed in Claim 7—Pethe does disclose the claimed salicide layer for reasons discussed for Claim 7 in Proposed Rejection 1A. Rather, a POSITA would have found it obvious to form and implement a salicide layer as claimed in Pethe’s structure notwithstanding the disclosures in Pethe that are addressed above for Proposed Rejection 1A.

configure the trench contacts 311A-311C in Pethe's FIG. 5B to include a salicide layer that is disposed between each S/D region and each trench contact via 341A/341B. Those discussions are incorporated herein and will not be repeated here for brevity.

Understanding that the use of a salicide layer between a source/drain region and contact would advantageously create a more conductive contact, and that such features were widely known in the art at the time, and that Pethe's semiconductor structure includes a source/drain region and corresponding contact (e.g., trench contact vias), a POSITA would have had reasons to consider ways to likewise improve Pethe's structure. Ex-03, ¶¶340-341. To do so, a POSITA would have looked to teachings in the art to supplement and/or complement their knowledge and experience pertaining to the fabrication and implementation of semiconductor structures. In doing so, a POSITA would have found Pham to provide insight that would have led a POSITA to implement a salicide layer between a source/drain and the trench contact via elements in the FIG. 5B structure of Pethe to enhance or establish conductive surfaces to the semiconductor device. *Id.*

In particular, and in addition to the teachings and suggestions discussed above for limitation 1(d) of Claim 1 and Claim 3 in this Proposed Rejection 1C, a POSITA would have appreciated that Pham also discloses the well-known use of a "metal silicide material (not shown)" that "may be formed on the source/drain regions 120

prior to forming the self-aligned contact structures 140." PA-02 (Pham), 10:9-11. Pham's teachings are in context of Pham's process for forming the self-aligned contacts structure 140 as shown in Figure 2K (below). Ex-03, ¶342.

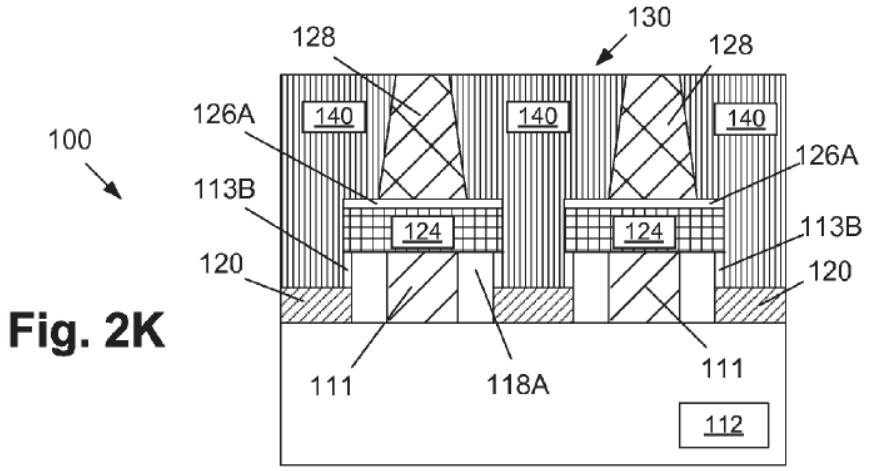


Fig. 2K

PA-02 (Pham), FIG. 2K (annotated to illustrate exemplary silicide (salicide) layers between each contact 140 and each source/drain regions 120).

A POSITA would have recognized hat Pham's contact structures 140 are contacts to the source/drain regions 120, and thus are similar to Pethe's trench contact vias 341A/341B and the "first contacts" recited in Claim 1 and Claim 7 of the '747 Patent (e.g., "a plurality of first contacts … that are electrically connected to parts of the S/D region"). And consistent with that known in the art, and with the source/drain regions and trench contacts 311 as disclosed by Pethe, a POSITA would have understood Pham's disclosure that a silicide layer "may be formed on the source/drain regions 120 **prior to** forming the self-aligned contact structures 140"

means that the silicide layer is disposed between the contact structure 140 and source/drain region 120 as exemplified below. Ex-03, ¶343.

A POSITA would have understood that Pham's metal silicide is a salicide layer consistent with that known in the art. Nonetheless, to the extent not apparent, it would have been obvious to provide such the silicide layer as a self-aligned silicide (which was known as a salicide) in the Pethe-Pham modified structure discussed above for Claim 1. Ex-03, ¶344. A POSITA would have understood the use of a self-aligned silicide layer was apparent for the same reasons above, and known to those of ordinary skill looking to promote conductivity between the source/drain regions and the corresponding contact structure. *See e.g.*, state of art teachings from PA-06 (Sell), 3:6-16, FIG. 1d (describing the state of art knowledge in context of a semiconductor device fabrication process and corresponding structure including spacer, etch stop layer, metal gate, source/drain regions, and corresponding contact structures, that "a salicide 118 may be formed on/in the source/drain contact area 107 using any suitable salicide process as are known in the art, such as but not limited to a nickel salicide process and/or other such salicide process"). Ex-03, ¶344.

In light of the teachings and suggestions of Pham, in context of those of Pethe and a POSITA's state of art knowledge at the time, a POSITA would have been motivated to consider and implement the known use of a salicide layer (and self-aligned silicide layers, or salicide layer) to reduce resistance between the

source/drain region and the trench contact vias 341 in Pethe's structure. Ex-03, ¶345. Given the teachings of Pham in context of a POSITA's knowledge, a POSITA would have appreciated that providing a salicide layer between the source/drain region and trench contact vias 341A/341B in the FIG. 5B structure of Pethe would have been an obvious implementation of conventional and known semiconductor device fabrication and structure features that were well within the experience and capabilities of such a skilled person at the relevant time. Accordingly, and in context of the collective teachings in Pham and Pethe (including the guidance offered by Pethe's disclosures for the Figure 2 embodiment), a POSITA would have reasonably expected to succeed at implementing such features in Pethe's FIG. 5B structure. Ex-03, ¶345.

Therefore, in light of the teachings and suggestions in Pham, Pethe, in context of a POSITA's knowledge and experience at the relevant time, a POSITA would have been motivated and found obvious to include a salicide layer in Pethe's FIG. 5B structure to provide a more conductive interface between the S/D region and the source/drain contact, thus improving performance of the semiconductor device. Such an implementation would have been consistent with the concerns in the art to improve performance of semiconductor devices, as Pethe recognizes. PA-01 (Pethe), 1:14-26 (necessary to optimize the performance of each device). Ex-03, ¶346.

A POSITA would have reasonably expected success in implementing the above modification/configuration to Pethe's FIG. 5B structure because providing a salicide layer would have involved nothing more than applying known semiconductor manufacturing processes for forming a self-aligned silicide layer consistent with the guidance in Pham. *See e.g.,* PA-02 (Pham), 10:9-11, 6:5-50. Designing, configuring, and implementing such a salicide layer in the Pethe structure would have been within the skill, knowledge, and capabilities of a POSITA at the relevant time. Ex-03, ¶347.

Further, a POSITA would have understood and appreciated that providing a salicide layer as Discussed above would have been an obvious example of combining prior art elements according to known methods, e.g., combining the teachings of Pham with those of Pethe in accordance with known semiconductor device fabrication processes (such as use of self alignment processes to form a salicide layer between a source/drain region and a corresponding contact consistent with that widely known in the art). Ex-03, ¶348.

A POSITA would have leveraged their state of art knowledge and experience in considering the design needs and the market demands for computing devices that include a semiconductor structure as contemplated by Pethe (PA-01, 14:29-15:38) and thus would have been motivated to configure and design fabrication processes to successful provide such salicide layer in the FIG. 5B structure. Ex-03, ¶349.

Accordingly, it would have been obvious to configure the FIG. 5B structure to include a salicide layer disposed between each source/drain region and each trench contact via 341A/341B ("first contact"), like that recited in Claim 7 of the '747 Patent. Thus, for the reasons here, further above for this Proposed Rejection 1C, and those for claim 7 in Proposed Rejections 1A and 1B, the collective teachings and suggestions of Pham and Pethe disclose or suggest the features of Claim 7. Ex-03, ¶350.

4. Proposed Rejection 1D: Claim 7 Is Obvious Over *Pethe* and *Sell*

Proposed Rejection 1D discusses how the combined teachings and suggestions of Pethe (as discussed above in both Proposed Rejections 1A and 1B) and Sell in context of a POSITA's state of art knowledge discloses and/or suggests, and renders obvious, certain features recited in Claim 7 of the '747 Patent. The teachings and suggestions in Pethe in both Proposed Rejections 1A and 1B are incorporated herein to render such features obvious. Ex-03, ¶351.

a. Claim 7: The semiconductor device of claim 1, further comprising a salicide layer disposed between each S/D region and each first contact.

The discussions in Proposed Rejections 1A and 1B are incorporated herein to support Proposed Rejection 1D. Additionally, for the reasons below and above in this Proposed Rejection 1D, the combined teachings and suggestions in Pethe and

Sell disclose or suggest, and render obvious Claim 7[24]. Specifically, in Proposed Rejection 1B, it was discussed that a POSITA would be motivated to configure the trench contacts 311A-311C in Pethe's FIG. 5B to include a salicide layer that is disposed between each S/D region and each trench contact via 341A/341B. Those discussions are incorporated herein and will not be repeated here for brevity.

Understanding that the use of a salicide layer between a source/drain region and contact would advantageously create a more conductive contact, and that such features were widely known in the art at the time, and that Pethe's semiconductor structure includes a source/drain region and corresponding contact (e.g., trench contact vias), a POSITA would have had reasons to consider ways to likewise improve Pethe's structure. Ex-03, ¶¶352-353. To do so, a POSITA would have looked to teachings in the art to supplement and/or complement their knowledge and experience pertaining to the fabrication and implementation of semiconductor

[24] A POSITA would have found it obvious to implement a salicide layer disposed between each S/D region and each trench contact via (first contact) in Pethe's FIG. 5B structure does not mean Pethe does not disclose such a feature as claimed in Claim 7—Pethe does disclose the claimed salicide layer for discussed for Claim 7 in Proposed Rejection 1A. Rather, supported by the teachings and suggestions of Sell in context of Pethe's teachings, a POSITA would have found it obvious to form and implement a salicide layer as claimed in Pethe's structure notwithstanding the disclosures in Pethe above for Proposed Rejection 1A.

structures. In doing so, a POSITA would have found Sell to provide insight that would have led a POSITA to implement a salicide layer between a source/drain and the trench contact via elements in the FIG. 5B structure of Pethe to enhance or establish conductive surfaces to the semiconductor device. Ex-03, ¶353.

For instance, a POSITA would have recognized that Sell discloses the known use of a salicide layer disposed between each S/D region and each first contact. For example, Sell discloses processes that form a salicide 118 between source/drain contact and the source/drain in a transistor structure. *See e.g.,* PA-06 (Sell), 1:7-13, 3:6-16, 3:17-30, 4:5-18; FIGs. 1d, 1e, 1f, 11. Ex-03, ¶354.

For example, Sell discloses that the "[m]ethods of the present invention are depicted in FIGS. 1 a-1 g" where "transistor structure 100 comprising a substrate 102, and a gate 104, which may comprise a metal gate in some embodiments, and may comprise such metal gate materials as hafnium, zirconium, titanium, tantalum, or aluminum, or combinations thereof, for example. The gate 104 may comprise a top surface 105." *Id.*, 1:65-2:9. Further, "transistor structure 100 may further comprise a spacer material 106, that may be adjacent and in direct contact with the gate 104." *Id.*, 2:10-22. The etch stop layer 108 and spacer 106 each has a planar top. PA-06, FIG. 1a. Ex-03, ¶355.

Sell also explains that after a sacrificial stopping layer 112 is formed on the top surface 105 of gate 104, and a resist layer 114 formed on the stopping layer 112

(*id.*, 2:23-34), an etching process is performed to form openings 116 leaving the etch stop layer 108 intact. PA-06, 2:35-49, Fig. 1b (below). Ex-03, ¶¶356-361.

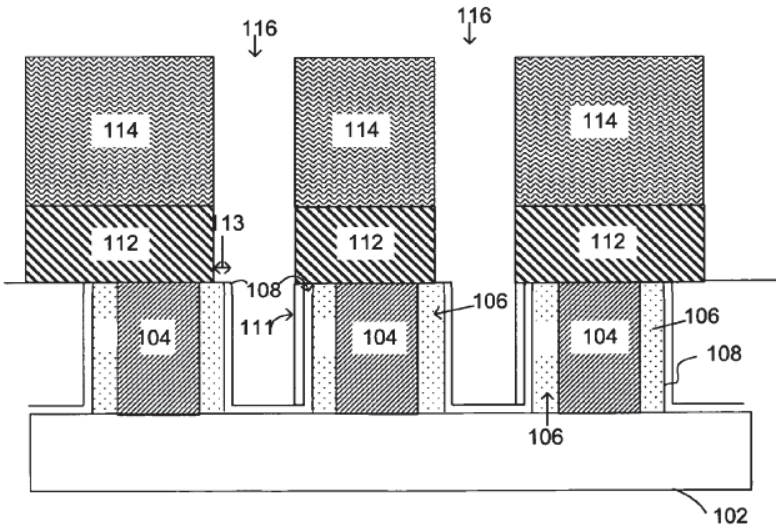


FIG. 1b

Sell discloses the etch stop layer 108 may be removed from the **source/drain region 103** of the substrate leaving a **source/drain contact area 107** exposed. *Id.*, 2:62-66, FIG. 1c (below). *See also*, *id.*, 2:50-61.

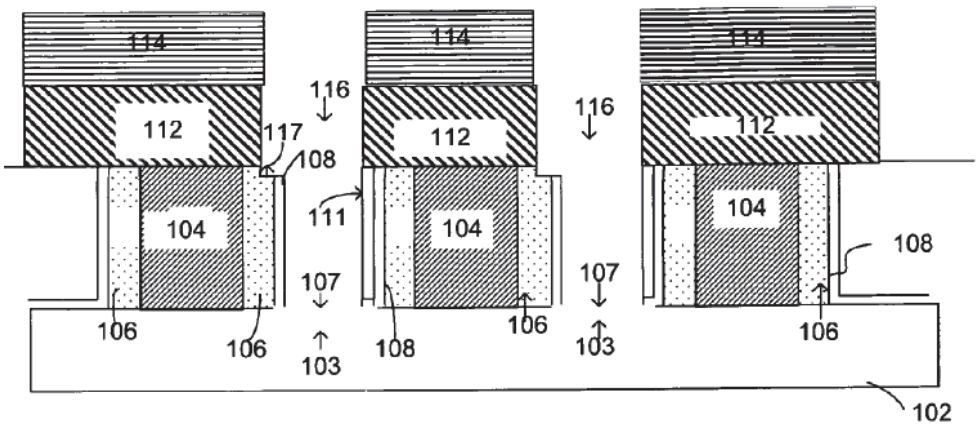


FIG. 1c

Sell also discloses "**a salicide 118 may be formed on/in the source/drain contact area 107 using any suitable salicide process as are known in the art, such as but**

not limited to a nickel salicide process and/or other such salicide process." PA-06 (Sell), 3:6-16; *see id.*, FIG. 1d (below).

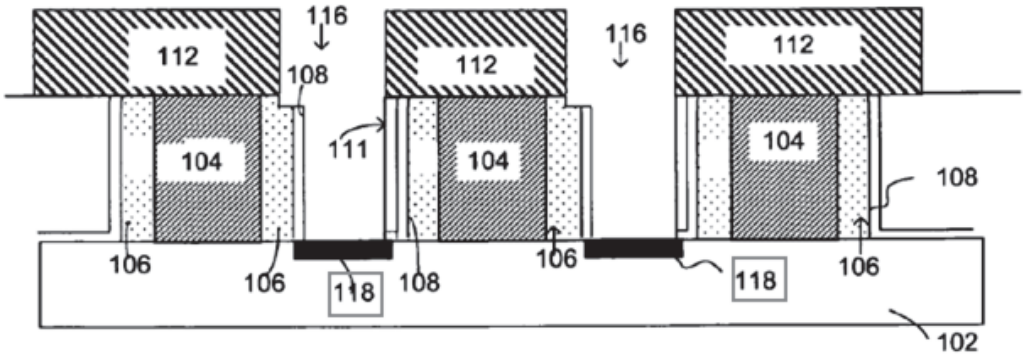


FIG. 1d

Next a **first contact metal** 120 is formed on the **salicide 118**. *Id.* at 3:17-23, FIG. 1e (below).

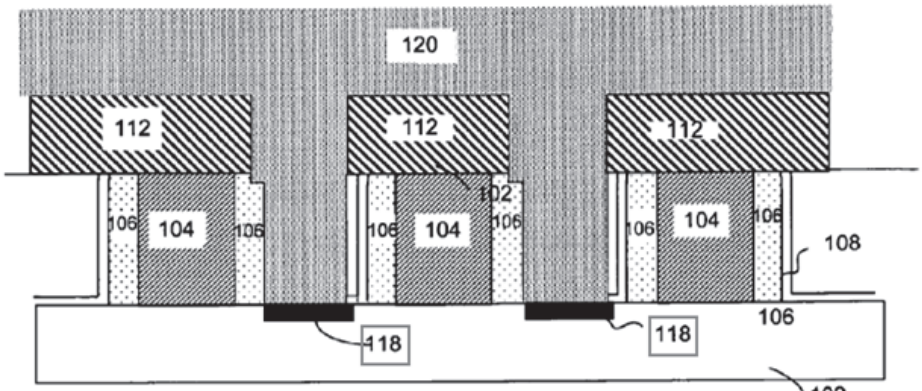


FIG. 1e

Sell then performs a planarization process on the contact metal and other layers that makes the spacer 106 and etch stop layer 108 shorter by removing a part. *Id.*, 3:23-30 ("A polishing process 123 may subsequently be performed, such as a chemical mechanical polishing (CMP) process, for example, to remove the first contact metal 120 (FIG. 1f) and the stopping layer 112."), FIG. 1e (below).

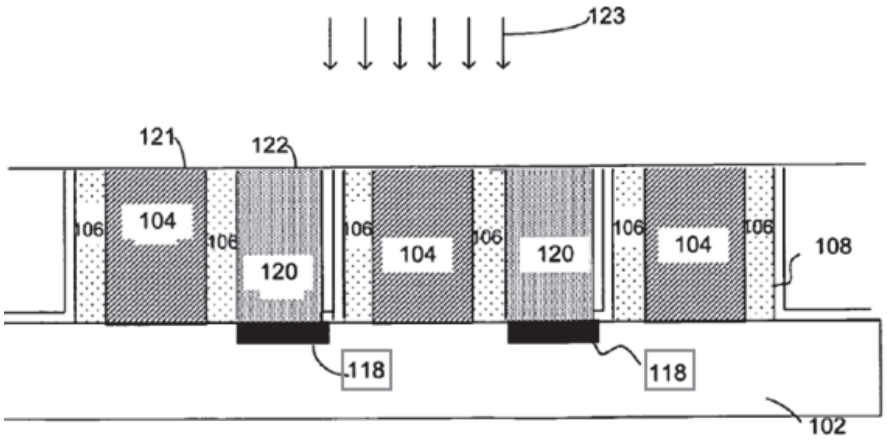


FIG. 1f

Sell explains that the result of these steps is a planarized top surface. *Id.*, 3:31-43. Afterwards a stacked contact structure is formed with contact metal 128 and contact metal 120 to the source/drain region 118 of the device. *Id.*, 3:44-4:26. As shown in FIG. 1g (below), the semiconductor structure includes a salicide layer 118 that is disposed between each source/drain region and each contact.

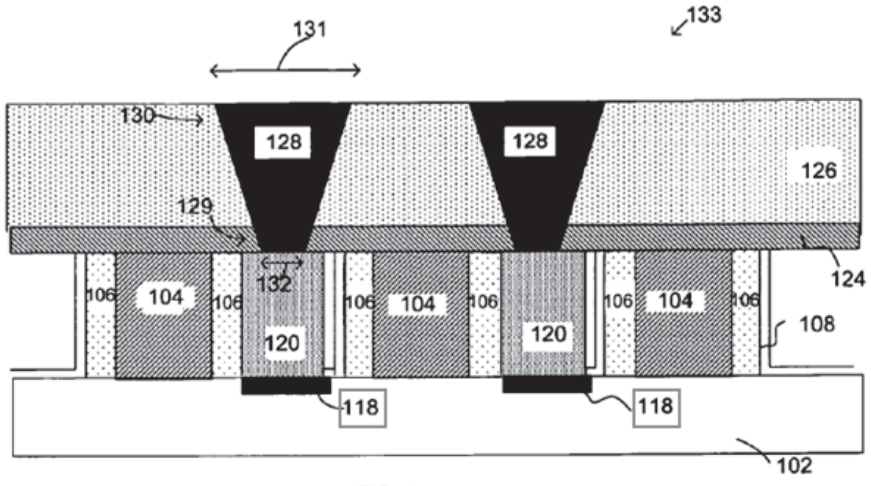


FIG. 1g

Sell therefore discloses a semiconductor structure including a etching stop layer (108) disposed on two sides of a metal gate (104) where the etching stop layer

has a truncated top surface as claimed given it was made shorter by removing a part (including during a planarization process) and having a planar top surface, consistent with Interpretations 1-3. *See* §II.D.1. Ex-03, ¶362.

Based on the above, it is clear that, like Pethe, Sell is analogous art. For example, a POSITA would have understood that Sell's semiconductor structure can include "transistor structure" (PA-06 (Sell), 2:10-22, 3:64-4:2, 4:19-26)), is in the same field (e.g., semiconductor device transistor structures with contacts) and reasonably pertinent to a problem the '747 Patent purports to address (e.g., transistor structure contact fabrication). *See e.g.*, PA-06, 1:5-13, 1:29-2:23, 3:17-4:18; Ex-01 ('747 Patent) 1:9-2:9, 2:18-20, 2:39-42, 3:1-25, 5:31-6:37. Accordingly, a POSITA would have had reasons to consider the teachings and suggestions in Sell when contemplating the semiconductor structure in Pethe's Figure 5B structure. Ex-03, ¶363.

In light of the teachings and suggestions of Sell, in context of those of Pethe and a POSITA's state of art knowledge at the time, a POSITA would have been motivated to consider and implement the known use of a salicide layer to reduce resistance between the source/drain region and the trench contact vias 341 in Pethe's structure. Given the teachings of Sell in context of a POSITA's knowledge, a POSITA would have appreciated that providing a salicide layer between the source/drain region and trench contact vias 341A/341B in the Figure 5B structure of

Pethe would have been an obvious implementation of conventional and known semiconductor device fabrication and structure features that were well within the experience and capabilities of such a skilled person at the relevant time (as demonstrated by Sell). Accordingly, and in context of the collective teachings in Sell and Pethe (including the guidance offered by Pethe's disclosures for the FIG. 2 embodiment), a POSITA would have reasonably expected to succeed at implementing such features in Pethe's FIG. 5B structure. Ex-03, ¶364.

Therefore, in light of the teachings and suggestions in Sell, Pethe, in context of a POSITA's knowledge and experience at the relevant time, a POSITA would have been motivated and found obvious to include a salicide layer in Pethe's FIG. 5B structure to provide a more conductive interface between the S/D region and the source/drain contact, thus improving performance of the semiconductor device. Such an implementation would have been consistent with the concerns in the art to improve performance of semiconductor devices, as Pethe recognizes. PA-01 (Pethe), 1:14-26 (necessary to optimize the performance of each device). Ex-03, ¶365.

Thus, having recognized that the teachings of Sell is consistent with the use of salicide layers in semiconductor structures is consistent like those described by Pethe, a POSITA would have been motivated to implement such features in the Pethe structure, and done so with a reasonable expectation of success. A POSITA would

have looked to provide salicide layer between each source/drain region and each trench contact via 341 in order to provide a more conductive interface to the source/drain region of the structure, thus promoting improved performance of the resulting structure of FIG. 5B in Pethe. Ex-03, ¶366.

A POSITA would have reasonably expected success in implementing the above modification/configuration to Pethe's FIG. 5B structure because providing a salicide layer in the manner discussed above would have involved nothing more than applying known semiconductor manufacturing processes for forming a self-aligned silicide layer consistent with the guidance in Sell. Designing, configuring, and implementing such a salicide layer in the Pethe structure would have been within the skill, knowledge, and capabilities of a POSITA at the relevant time. Ex-03, ¶367.

Further, a POSITA would have understood and appreciated that providing salicide layer as discussed above would have been an obvious example of combining prior art elements according to known methods, e.g., combining the teachings of Sell with those of Pethe in accordance with known semiconductor device fabrication processes. Ex-03, ¶368.

A POSITA would have leveraged their state of art knowledge and experience in considering the design needs and the market demands for computing devices that include a semiconductor structure as contemplated by Pethe (PA-01, 14:29-15:38), and thus would have been motivated to configure and design fabrication processes

to successful provide such salicide layer in the FIG. 5B structure as discussed. Ex-03, ¶369.

Accordingly, it would have been obvious to configure the FIG. 5B structure to include a salicide layer disposed between each source/drain region and each trench contact via 341A/341B ("first contact"), like that recited in Claim 7 of the '747 Patent. Thus, for the reasons here, further above for this Proposed Rejection 1D, and the reasons in Proposed Rejection 1A for Claim 7, the collective teachings and suggestions of Sell and Pethe disclose or suggest the features of Claim 7. Thus, Pethe in view of Sell render obvious Claim 7 of the '747 Patent. *KSR*, 550 U.S. at 416.

For the reasons above, Pethe in view of Sell renders obvious claim 7 and thus the claim is invalid in view of that prior art combination. Ex-03, ¶370.

5. Proposed Rejection 1E: Claims 8-9 Are Obvious Over *Pethe* and *Huang*

a. Claim 8: The semiconductor device of claim 3, further comprising a plurality of third contacts disposed on parts of the first contacts and on parts of the second contacts, wherein each third contact is a monolithically formed structure.

Claim 9: The semiconductor device of claim 8, wherein each third contact comprises a via hole structure and a trace structure, wherein the via hole structure and the trace structure comprise the same material and contact each other directly.

Pethe in view of Huang discloses/suggests these limitations. Ex-03, ¶¶371-401.

As explained for Proposed Rejection 1A, Claims 1 and 8, Pethe teaches the metal (0) portion 550 includes **a plurality of third contacts** and **disposed on** trench contact vias 341A, 341B (**parts of the first contacts**) and on gate contact vias 542A, 542B (**parts of the second contacts**.) §§VI.A.1(a), (g).

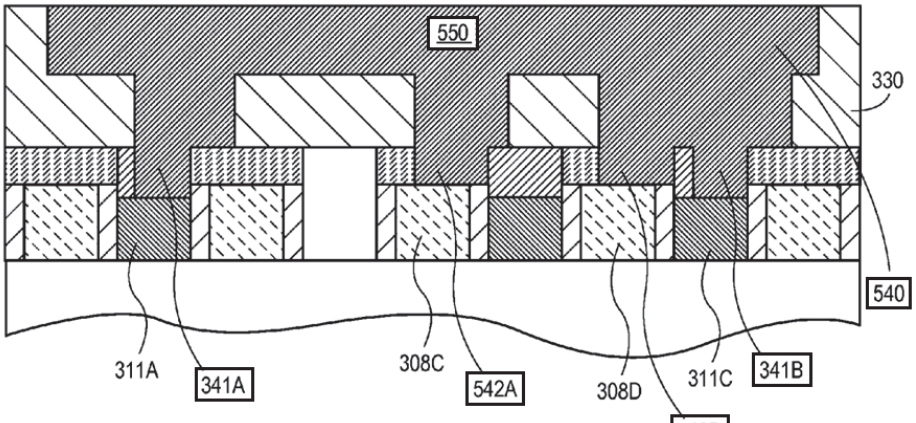


FIG. 5B

PA-01, 12:54-13:12; Ex-03, ¶372.

In addition to Pethe's Figure 5B structure discussed above for claim 3 in §§VI.A.1(a), (c), or as modified as discussed above for claim 3 in §VI.A.2(k) disclosing a plurality of third contacts as claimed, a POSITA would have been motivated to implement such features in view of Huang. Ex-03, ¶373.

It was well-known and conventional to form metal (1) ("M1") metal lines and metal (0) vias (above the metal (0) lines and device contacts) using a dual-damascene process. By the time of the alleged invention, the dual-damascene process was an established technique in semiconductor manufacturing, particularly in the back-end-of-line (BEOL) processing, which is the "formation of the M1 wiring layer to formation of a pad opening to a final passivation... in a wafer level package process." (Ex-11 (Tomimatsu), ¶89.) Ex-03, ¶374.

A number of state of art references confirm such an understanding and provide teachings consistent with a POSITA knowledge of the art at the time of the '747 patent. For example, using a dual-damascene process to provide M1 metal lines and metal (0) vias was conventional and ubiquitous (Ex-15 (Xiao), 345-49, FIG. 9.35, 346 (a via-first dual damascene process), FIG. 9.36, 346 (a trench-first dual damascene process), FIG. 9.37, p. 346 (a via-first dual damascene process)). Ex-03, ¶¶375-376. As another example, state of art teachings from Wolf (Ex-09), explain that in a dual-damascene process, "only a single metal deposition step is used to

simultaneously form the main metal lines and the metal in the vias," after which "CMP is used to remove excess metal." (Ex-09, 696-98.) This "sequence is repeated for the next level of metal" (i.e., M2, M3... M8). Ex-09 (Wolf), FIG. 15-3, p. 697. Ex-03, ¶¶377-378. As another example, May (Ex-10) explains that "[d]amascene processing involves the creation of interconnect lines by first etching a trench or canal in a planar dielectric layer and then filling that trench metal," and [i]n dual damascene processing (Figure 5.13). a second level is involved where a series of holes (i.e., contacts or vias) are etched and filled in addition to the trench." Ex-10 (May), FIG. 5.13, 55-56. Ex-03, ¶378.

As further examples, using a dual-damascene process to provide M1 metal lines and metal (0) vias is referred to in Xiao (Ex-15, 345-49) at the time of the alleged invention to be "mainstream" (Ex-15, 345-49), well developed "[i]n the late 1990s" (p. 453), having "maturity" (*id.*, 464), "dual damascene has **become the process of choice** for copper metallization in IC chip manufacturing" (*id.*, 517-18), "Copper interconnections have become a **mainstream technology in CMOS logic IC** since the development of the 130-nm technology node. Copper CMP processes have been **widely used in** dual damascene processes to form copper interconnections in **advanced IC fabs**" (*id.*, 543), "The dual damascene process, which combines via and trench etching before metal deposition, is **the most commonly used method for copper metallization**" (*id.*, 574-79). Ex-03, ¶379.

A POSITA was also aware of known advantages to implementing a dual-damascene process to provide M1 metal lines and M0 vias, including:

- **simplified fabrication**: "The dual damascene process can eliminate some metal deposition and CMP processes, unlike two single damascene processes." (Ex-15 (Xiao), 574-79); "The dual-damascene process offers the advantage of reducing the number of process steps" (Ex-09 (Wolf), 695); "The reduction in the number of processing steps is another of the benefits that have driven the development of dual-damascene processes" (*id.*, 698).

- **no requirement for metal etching**: "the dual damascene process does not need to etch metal" (Ex-15 (Xiao), 345-49, 497-98), "[t]he fact that the dual damascene process does not require a metal etch step paved the way for copper metallization of IC interconnections in the late 1990s" (*id.*, 464), "[b]ecause copper is very difficult to dry etch, dual damascene has become the process of choice for copper metallization in IC chip manufacturing" (*id.*, 517-18), "The advantage of damascene processing is that it eliminates the need for metal etch" (Ex-10 (May), 56).

- **reduced risk of electromigration failure**: "One special benefit of the dual damascene technique is that the via plug is now of the same material as the metal line and the risk of via electromigration failure is reduced." (*id.*, 92.)

As these state of the art sources further explain that "dual damascene process does not need to etch metal…dual damascene has become the process of choice for copper metallization…and [has] become mainstream." Ex-15, 345-49; *see also id.*, 345-49, FIG. 11.3, 464, 497-98, FIG. 11.38, 517-18, FIG. 12.15, 543, 574-79. Ex-03, ¶¶380-381.

Many other references recognized these advantages. See discussions above in §§VI.A.2, VI.A.3(e).

Accordingly, a POSITA considering Pethe's semiconductor structure would have been motivated to look to teachings in the art for ways to provide a connection of the semiconductor structure to the M1 layer with simplified fabrication, no requirement for metal etching, and reduced risk of electromigration failure. Ex-03, ¶382.

In doing so, a POSITA would have recognized Huang as an example of such relevant teachings. Ex-03, ¶¶383-386. Consistent with the POSITA's knowledge discussed above, Huang (PA-03) teaches the use of a dual-damascene process to provide M1 metal lines and M0 vias. (PA-03, ¶17, FIG. 8A.) Huang teaches metal layer M1 metal lines 74 and M0 vias 72 for "for connecting to contact plugs 60 and 62," as shown in annotated Figure 8A below.

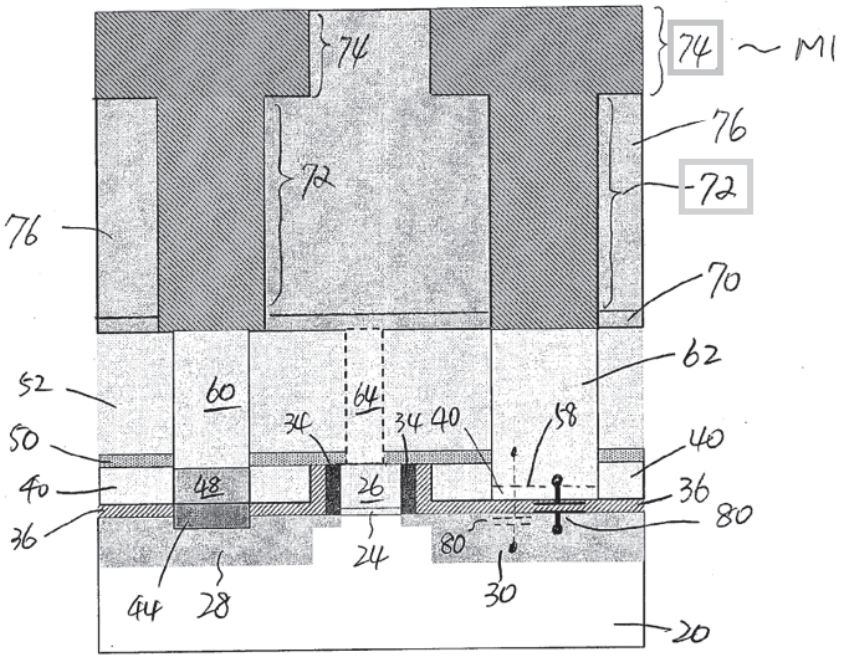


Fig. 8A

PA-03, ¶17, FIG. 8A.

In Huang, "M0 vias 72 and metal lines 74 may be formed using a dual-damascene process, and hence no noticeable interfaces are formed between M0 vias 72 and the respective overlying metal lines 74. PA-03, ¶17.

Huang's aforementioned structure also corresponds to **a via hole structure and a trace structure, wherein the via hole structure and the trace structure comprise the same material and contact each other directly**. For example, Huang's M0 vias 72 structure corresponds to a "via hole structure" and metal lines 74 structure corresponds to the third contact's "trace structure."

Given that the "M0 vias 72 and metal lines 74 may be formed using a dual-damascene process, and hence no noticeable interfaces being formed between M0

vias 72 and respective overlying metal lines 74" (PA-03, ¶17), the via hole structure and the trace structure comprises the same material and contact each other directly.

Huang and Pethe each disclose features relating to semiconductor devices/ structures and/or parts thereof. For example, Pethe and Huang describe semiconductor structures with metal layers to contacts (i.e., gate and source/drain contacts). (*See*, *e.g.*, PA-01 (Pethe), 8:24-51, 9:29-43, 11:23-42; PA-03, ¶17; Ex-01, 5:31-6:37.) Thus, a POSITA would have had reasons to consult Huang when looking to implement a semiconductor structure like that discussed in Pethe. Ex-03, ¶387.

In considering Huang in context of Pethe, a POSITA would have been motivated to consider the collective teachings of Pethe with those of Huang to achieve a dual-damascene process to provide M1 metal lines and M0 vias in Pethe's FIG. 5B structure. PA-03 (Huang), ¶17, FIG. 8A; Ex-03, ¶388.

A POSITA would have been motivated to implement such a dual-damascene process in Pethe's structure and would have reasonably expected such an implementation to be successful in context of Pethe's disclosed structure. Ex-03, ¶389. The implementation of a dual-damascene process to provide M1 metal lines and M0 vias was known in the art by a POSITA before the alleged invention of the '747 patent, as demonstrated by the above-mentioned state of art teachings (*see* discussions above regarding Wolf, May, and Xiao). Ex-03, ¶389. Pethe provides a

metal (0) portion, but does not provide any BEOL interconnection, which a POSITA would have understood is critical to create an integrated circuit with ever-more capacity, as is the driving force of the semiconductor industry and of Pethe. PA-01 (Pethe), 1:14-26; Ex-03, ¶389. A POSITA would have appreciated that the implementation of a dual-damascene process to provide M1 metal lines and M0 vias was at the time, a conventional method to produce such implementations. (*See above and for example*, (Ex-09 (Wolf), 696-98; Ex-10 (May), 55-56; Ex-15 (Xiao), 19, 345-49, 453, 464, 497-98, 517-18, 543, 574-79.) A POSITA would have understood that the combined teachings of Pethe and Huang would merely amount to determining a suitable dual-damascene process to modify the Figure 5B structure as explained above. Ex-03, ¶390.

Under any convention, a POSITA would have understood a dual-damascene process generally involved the conventional steps of patterning and etching the via and trench definition, depositing metal to fill the space of both via and trench, and CMP. (*See above and for example*, Ex-09 (Wolf), 696-98; Ex-10 (May), 55-56; Ex-15 (Xiao), 19, 345-49, 453, 464, 497-98, 517-18, 543, 574-79.) A POSITA would have been able to readily apply conventional methods of dual-damascene processes, such as those taught by Huang, to Pethe with high predictability and success. Ex-03, ¶391.

Accordingly, a POSITA would have been motivated to modify Pethe's metal interconnection to include, above its metal (0) portion 350, Huang's M1 metal lines and M0 vias. Ex-03, ¶392. In fact, Huang explicitly contemplates placing upper metal lines and vias over lower metal lines, such as metal (0) portion 350 in explaining that "In subsequent process steps, more metal layers (not shown) may be formed over metal layer M1." PA-03, ¶17. Ex-03, ¶392.

The above motivation rationale discussed above for claims 8 and 9 would have been applicable to both Pethe's FIG. 5 structure discussed for claims 1 and 3 in §§VI.A.1(a), (c), and to Pethe's modified embodiment discussed for claims 1 and 3 in §VI.A.2(k). Notwithstanding, in addition to Pethe's FIG. 5B structure discussed above (claim 3 in §VI.A.1(c)) or as modified (claims 1 and 3 in §§VI.A.1(a), (i)) a POSITA would have been motivated to implement **a plurality of third contacts** as claimed in claims 8-9 in view of Huang. Ex-03, ¶¶393-394.

In light of Huang's teachings and a POSITA's state of art knowledge as discussed above, Pethe's FIG. 5B structure would have been predictably modified to include, above its metal (0) portion 550, M1 lines and M0 vias, consistent with the teachings of Huang using the dual-damascene processes known in the art and as taught by Huang. Ex-03, ¶395.

As a result, the modified FIG. 5B structure would have included a **plurality of third contacts** (for example, parts of the newly formed M1 lines above Pethe's

M0 line (550) and the associated M0 vias interconnecting the M1 and M0 lines formed based on Huang's teachings) **disposed on parts of the first contacts** (for example, parts of 341A/341B) **and on parts of the second contacts** (for example, parts of 542A/542B), as in claim 8. *Id.* Ex-03, ¶396.

In addition, **each third contact** (in the modified FIG. 5B structure) would have comprised **a via hole structure (M0 vias) and a trace structure (**parts of the newly formed M1 lines (*see* Ex-01, 5:48-53 (trace structure may be "lines")), which would **comprise the same material and contact each other directly** (as in claim 9) given they are formed using the dual-damascene process like that taught by Huang, which would also result in **each third contact** (above) being a **monolithically formed structure (**as in claim 8). Ex-03, ¶397.

A POSITA would have understood and appreciated that such a modification would have involved the application of known technologies/ techniques (for example, dual-damascene process to provide M1 metal lines and M0 vias) to a known device/structure (like Pethe's FIG. 5 embodiment with metal (0) portion 550). Accordingly, such a skilled person would have been motivated to implement such a modification, and would have reasonably expected such an implementation to be successful. A POSITA would have understood upon considering and implementing such knowledge, known techniques, and teachings in the prior art references, such a modification would have yielded the foreseeable result of

providing M1 metal lines and M0 vias to a known device/structure (Pethe's FIG. 5B structure with metal (0) portion 550) with operability to the M1 layer in the structure of FIG. 5B. Ex-03, ¶398. *KSR*, 550 U.S. at 416.

In the combined structure of Pethe and Huang, M0 vias 72 (**a via hole structure**) and metal layer M1 metal lines 74 (**a trace structure**) form **a third contact**. This would have been consistent with the teachings shown FIG. 8A of Huang (above). Ex-03, ¶399.

As discussed in claim 8, a dual-damascene process is used to form M0 vias 72 and metal layer M1 metal lines 74 together in a single deposition, which a POSITA would have understood to mean **the via hole structure and the trace structure comprise the same material and contact each other directly**. Ex-03, ¶400. (PA-03, ¶17 ("no noticeable interfaces are formed between M0 vias 72 and the respective overlying metal lines 74."), FIG. 8A.)

For the reasons above, Pethe in view of Huang renders obvious claims 8 and 9, and thus the claims are invalid in view of that prior art combination. Ex-03, ¶401.

B. Proposed Rejections 2A-2G: Chang

1. Proposed Rejection 2A: Claims 1, 2 and 6 Are Anticipated by *Chang*

Chang teaches two approaches in forming self-aligned contacts and SRAMs containing such contacts: (1) FIGs. 1-16 (no gate protection option) and (2) FIGs.

17-27 (with gate protection option). PA-04 (Chang), ¶¶51-52. Chang teaches "SRAM containing transistor structures with gate-protected self-aligned contacts" in Figures 24-27. PA-04, ¶107. Chang discloses its SRAM in the context of "self-aligned contacts" with a "gate-protection option," which "is described with respect to FIGS. 17-27." *Id.*, ¶52.[25] Specifically, "FIGS. 17 through 23 show wafer cross sections illustrating operations in connection with the gate-protect option with respect to forming self-aligned contacts." PA-04, ¶89. FIGs. 24-27 show an SRAM with those contacts. *Id*., ¶107 ("FIG. 24 is a top view of a layout 1400 of an SRAM containing transistor structures with gate-protected self-aligned contacts…cross sections of the SRAM layout 1400 are shown in FIGS. 25, 26, and 27").

a. Claim 1

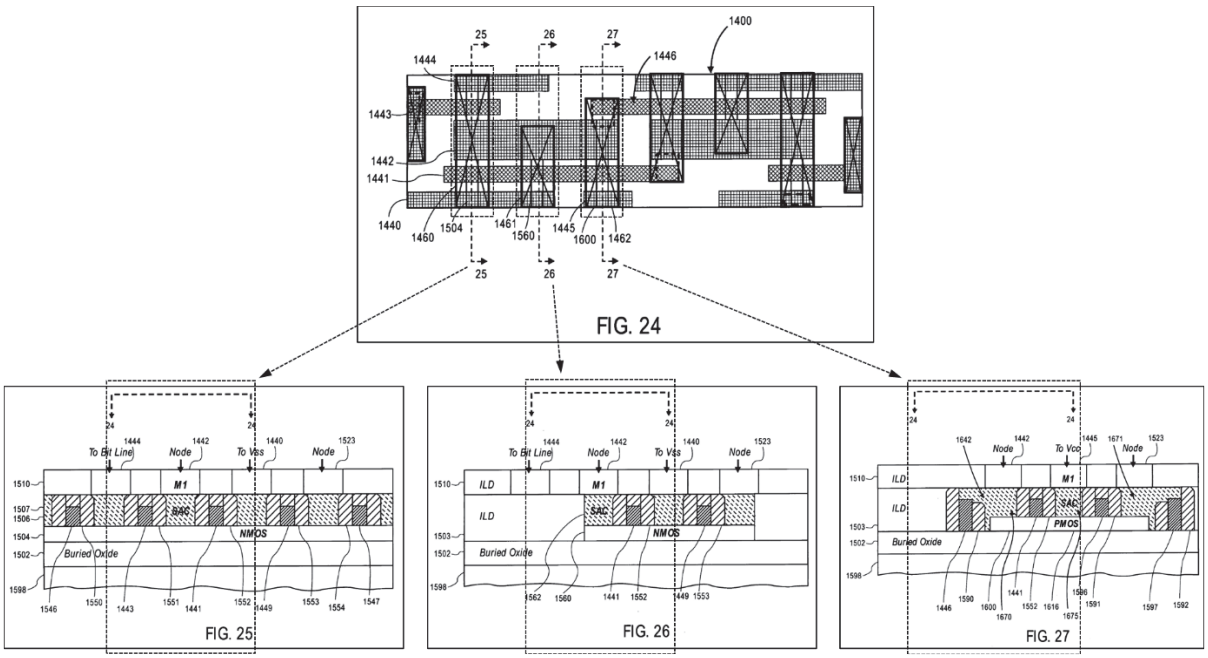
(1) [1.pre] A semiconductor structure, comprising:

To the extent claim 1's preamble is limiting, Chang discloses it. Ex-03, ¶¶402-403; §§VI.B.1(a)(2)-(9). Chang discloses a "semiconductor structure" as claimed. For example, the structure described in connection with the "SRAM containing transistor structures with gate-protected self-aligned contacts" in FIGs. 24-27 and related teachings is a semiconductor structure as further explained below

[25] Chang discloses an alternative "no gate-protect option…in reference to FIGS. 6 through 16." PA-04, ¶51.

for limitations 1(a)-1(h). *See* discussion for §§VI.B.1(a)(2)-(9) for limitations 1(a)-1(h) incorporated herein.

As discussed above in §III.C (incorporated herein) and below, many of Chang's teachings, such as FIGs. 17-23 and related teachings, are further teachings of the SRAM. As Discussed above in §III.C and below, FIGs. 24-27 all describe the same "structure," but provide different views and cross-sections.



PA-04 (Chang), FIGs. 24-27.

(2) [1.a] a substrate;

Chang discloses this limitation. Ex-03, ¶¶404-408. For example, Chang discloses that the SRAM includes a silicon **substrate 1598**. Chang labels silicon substrate 1598 in FIGs. 25-27. PA-04 (Chang), ¶110, FIGs. 24-27 (annotated to show silicon substrate 1598).

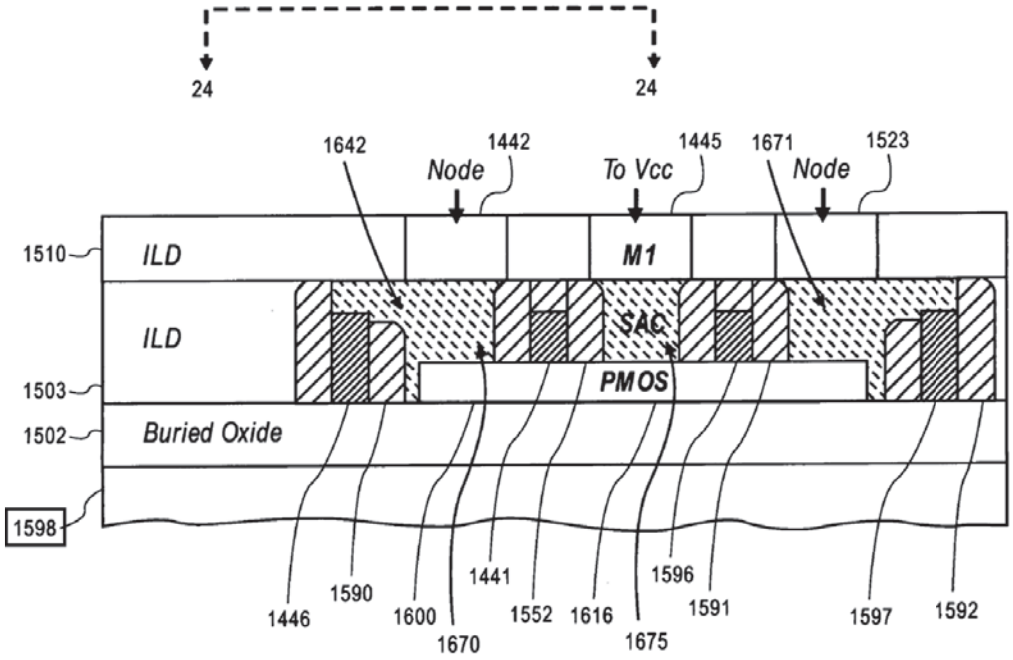


FIG. 27

PA-04, FIG. 27, ¶110.

The combination of silicon substrate 1598 and buried oxide 1502 is also a substrate. The combination of silicon substrate 1598 and buried oxide 1502 form a structure on which the transistor structures of the SRAM is formed or built on, meaning it is a substrate as claimed in the '747 Patent. Ex-03, ¶405.

The combination of silicon substrate 1598, buried oxide 1502, and PMOS diffusion layer 1600 is also a substrate. The combination of silicon substrate 1598, buried oxide 1502, and PMOS diffusion layer 1600 form a structure on which the transistor structures of the SRAM is formed or built on, meaning it is a substrate as claimed in the '747 Patent. Ex-03, ¶406.

Chang describes a silicon substrate/buried oxide/diffusion layer structure as an SOI substrate. PA-04, ¶46, FIG. 5. Chang's description is consistent with a POSITA's understanding of a "substrate" in the context of the'747 Patent, and is satisfied at least by the structure on which the transistors of the SRAM are formed or built on. Ex-03, ¶407.

Thus, Chang discloses a substrate as claimed in limitation 1(a). *See also* §§VI.B.1(a)(1), VI.B.1(a)(3)-(9) for limitations 1(pre), 1(c)-1(h), §III.D, incorporated herein. Ex-03, ¶408.

(3) [1.b] a first dielectric layer disposed on the substrate;

Chang discloses this limitation. Ex-03, ¶¶409-415. For example, Chang discloses that the SRAM includes a first dielectric layer disposed on the substrate. Chang discloses "interlayer dielectric layer 1503" as shown below in FIG. 27, which is disposed on Chang's substrate (under each interpretation of "substrate" discussed in element 1(a)), as annotated below. *See* PA-04, ¶112.

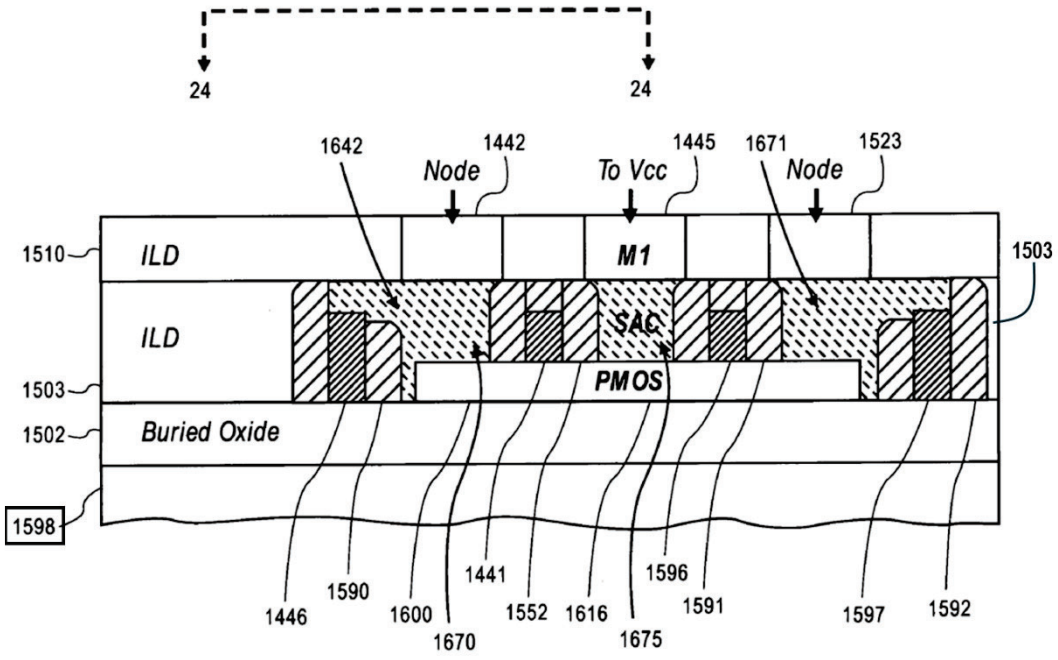


FIG. 27

PA-04, ¶112, FIG. 27.

As shown above, interlayer dielectric layer 1503 is disposed on the silicon substrate 1598, and is disposed on the combination of silicon substrate 1598 and buried oxide 1502, and is disposed on combination of silicon substrate 1598, buried oxide 1502, and PMOS diffusion layer 1600. PA-04, ¶112; §VI.B.1(a)(2); Ex-03, ¶410.

The presence of buried oxide 1502 does not prevent interlayer dielectric layer 1503 from being "disposed on" the silicon substrate 1598 in the based on the ordinary meaning of the term in view of the '747 Patent. If it were found that "disposed on" in the claims of the '747 Patent means "disposed directly on," then the substrate comprised of the combination of silicon substrate 1598 and buried

oxide 1502 and the substrate comprised of the combination of silicon substrate 1598, buried oxide 1502, and PMOS diffusion layer 1600 each satisfy this interpretation. Ex-03, ¶411.

In addition, Chang teaches that interlayer dielectric layer 1503 is disposed on a bulk substrate, which satisfies element 1(b) for the same reasons. Chang discloses that "transistors on bulk substrates" may be used with the invention instead of substrates with a buried oxide (for example, SOI substrates). *See* PA-04, ¶114 ("Embodiments of the invention have been described in detail with respect to transistors on SOI with metal gates."). As another example, Chang states that "[a]lthough a silicon-on-insulator ('SOI') substrate is illustrated, the process is applicable to transistors on bulk substrates." *Id.*, ¶46; Ex-03, ¶¶412-413.

As discussed with respect to Pethe, limitation 1(b) in §VI.B.1(a)(3), incorporated herein, interlayer dielectrics ("ILDs"), such as interlayer dielectric layer 1503, were known by a POSITA at the time. For example, ILDs were known to have been formed in regions of the semiconductor structure as a layer where contact formation is blocked, and were known to fill the space between structural elements in a semiconductor structure. Ex-03, ¶414.

Thus, Chang's interlayer dielectric layer 1503 is a "first dielectric layer disposed on the substrate" as claimed. Chang therefore discloses limitation 1(b).

See also §§VI.B.1(a)(1)-(2), (a)(3)-(9) for limitations 1(pre)-1(a), 1(c)-1(h), and §III.D, incorporated herein. Ex-03, ¶415.

(4) [1.c] at least two metal gates disposed in the first dielectric layer;

Chang discloses this limitation. Ex-03, ¶¶416-435. For example, Chang's SRAM also includes at least two metal gates disposed in the first dielectric layer, as discussed above for limitation 1(b). Namely, the SRAM includes gates 1441, 1443, 1446, 1449, 1546-47, and 1596-97 and are disposed in interlayer dielectric layer 1503 (i.e., the "first dielectric layer"), as shown below. PA-04 (Chang), ¶¶111-12, 108, 114, 47, FIGS. 24, 27 (annotated below).

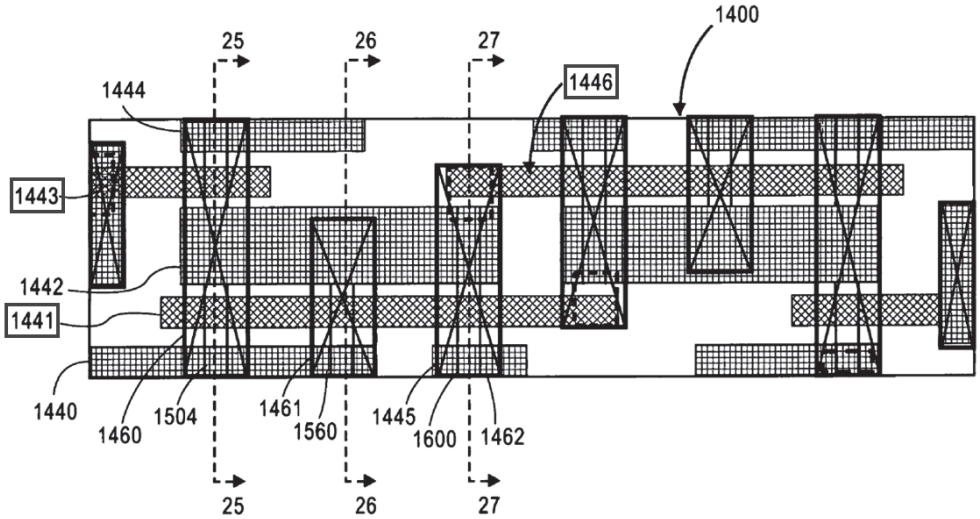


FIG. 24

PA-04 (Chang), FIG. 24.

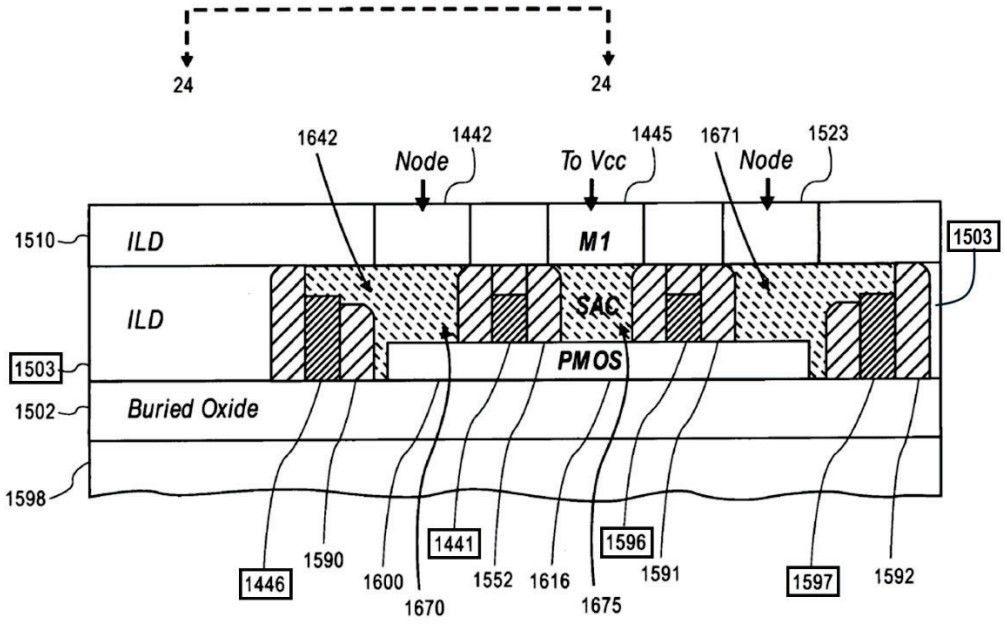


FIG. 27

PA-04, FIG. 27, ¶¶47, 111-12, 114; Ex-03, ¶416.

Chang's gates 1441, 1443, 1446, 1449, 1546-47, and 1596-97 are eight metal gates, which is "at least two", as shown in the annotated FIGs. 24, 27 above. PA-04, ¶¶111-12, 108, 114, 47. In addition, any two or more of gates 1441, 1443, 1446, 1449, 1546-47, and 1596-97 are "at least two." Ex-03, ¶417.

For example, any combination of two or more of the eight gates (e.g., any two of the eight above gates, any three of the above eight gates, any four of the above eight gates, any five of the above eight gates, any six of the above eight gates, any seven of the above eight gates, and all eight gates) each independently satisfy "at least two metal gates." Ex-03, ¶418.

As further non-limiting examples, gates 1441 and 1449, gates 1441 and 1446, gates 1441, 1596, gates 1596 and 1597, and gates 1441, 1446, 1596, 1597 each independently satisfy "at least two metal gates," including as an example (but not limited to, as discussed above), all eight gates above, any combination of two or more of the eight gates. In one specific example, Chang's gates 1441, 1446 discloses the claimed "at least two metal gates.". In another specific example, Chang's gates 1596, 1597 discloses the claimed "at least two metal gates." Ex-03, ¶¶419-420.

Chang's gates 1441, 1443, 1446, 1449, 1546-47, 1596-97 (and all combinations or two or more of these gates) are metal. For example, Chang explicitly refers to gates 1441, 1449 as "**metal** gates 1441, 1449." PA-04, ¶111.

It would have been clear to a POSITA that the other gates disclosed by Chang are metal as well. As an initial matter, a POSITA would have understood that in Chang's SRAM, the gates 1441, 1443, 1446, 1449, 1546-47, 1596-97 would have been, and are, formed in the same one or more gate formation processes, and would have been, and are, formed of the same material (in this case, metal), absent a specific reason to add manufacturing complexity of using different materials. PA-04, ¶114, 47; Ex-03, ¶¶421-423.

A POSITA would have thus understood that Chang clearly discloses that the described SRAM has "been described in detail with respect to transistors on SOI

with **metal gates**." A POSITA would have recognized that Chang's embodiments describe "other types of transistors with metal gates." Ex-03, ¶424.

While Chang notes a "polysilicon" gate may be used, this is merely noted as an alternative possibility, but is not described as being used in the SRAM or a requirement in Chang. Ex-03, ¶425.

Chang also says its teachings are "applicable to transistors with **metal gates**." PA-04, ¶47. Chang explains that its teachings are "not restricted to a particular way the **metal gates** are formed." Thus, Chang (PA-04, ¶47) provides further indication to a POSITA that the SRAM gates are metal. Ex-03, ¶426.

Chang further explains its gate formation process with respect to FIG. 5. PA-04, ¶¶46-49. In these teachings, Chang described this process as "a metal gate process" for creating "metal gates." PA-04, ¶¶46-49. Chang's teachings with respect to FIGs. 17-23 illustrate forming the self-aligned contacts and metal gates. PA-04, ¶¶89-90. These are teachings to form the SRAM structure in FIGs. 24-27, as discussed in §III.D (incorporated herein). PA-04, ¶¶27-35, 52, 89, 107. In these teachings, and Chang does not describe using polysilicon or any other material for the gates in the SRAM structure of FIGs. 24-27. Ex-03, ¶427.

It would have been understood by a POSITA that the fabrication sequences illustrated in FIGs. 5, 17-23 constitute the steps to realize the SRAM of FIGs. 24-27. Furthermore, a POSITA would recognize that the guidance provided concerning

the metal gates in FIGs. 19 and 20 details the processes for constructing the gate structures within the finished SRAM structure of FIGs. 24-27. Ex-03, ¶428. In fact, Chang explains that "self-aligned contacts" with a "gate-protection option" "is described with respect to FIGS. 17-27." PA-04, ¶52. In other words, Chang itself explicitly connects its gate-protection option for self-aligned contacts to the entirety of the drawings spanning FIGs. 17-27. Ex-03, ¶428.

Specifically, Chang explicitly details the fabrication sequence spanning FIGs. 17-23 as the methodology for manufacturing the gate-protection feature in conjunction with self-aligned contacts SACs. PA-04, ¶89 ("FIGS. 17 through 23 show... forming self-aligned contacts"). Furthermore, FIGs. 24-27 exhibit the structural realization of a SRAM employing transistor architectures that feature these gate-protected SACs. PA-04, ¶107 (FIGs. 24 -27 show "an SRAM containing transistor structures with gate-protected self-aligned contacts."). Thus, A POSITA would have appreciated that FIGs. 17-23 describe forming self-aligned contacts, and FIGs. 24-27 is a structure with those contacts. A POSITA would have understood that the procedures for manufacturing the metal gates in FIGs. 17-23 would correspond to the formation of the finalized metal gates in the SRAM of FIGs. 24-27. Ex-03, ¶429.

FIGs. 17-23 and related descriptions show forming structures associated with gates, such forming SiN caps by a "recess etch" of the top of the gates, and the

SRAM of FIGs. 24-27 is a finished fabricated structure with those features. PA-04, ¶¶89-92. *See id.*, FIGs. 18, 27 (below) (showing gates 1441, 1446 (e.g., one example of at least two metal gates). Ex-03, ¶430.

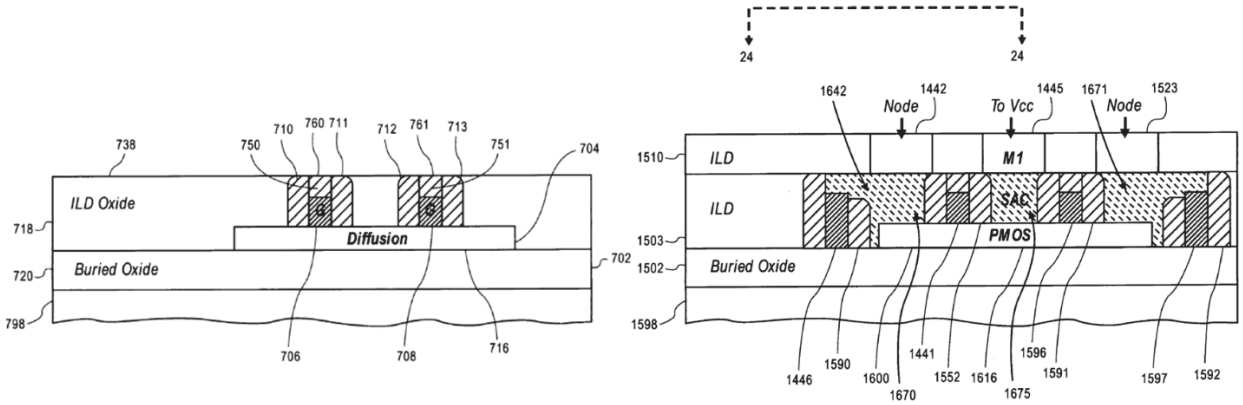


FIG. 18 FIG. 27

PA-04 (Chang), FIGs. 18, 27.

As another example, Chang's FIG. 5 and related disclosures discuss gate formation utilizing a "replacement metal gate process." PA-04, ¶¶46-49. A POSITA would have appreciated that the SRAM shown in FIGs. 24-27 (below) has gates fabricated according to those teachings. Ex-03, ¶431. This is illustrated in the annotated image below. To note, gates 1441, 1596 in FIG. 27 have undergone the "recess etch" to form the silicon nitride caps according to the explanations of FIGs. 17-23.

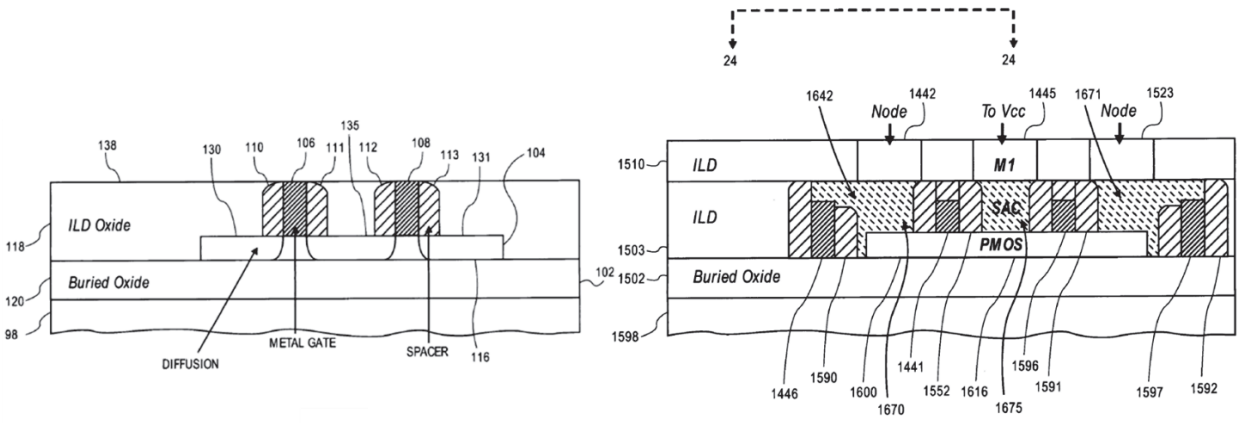
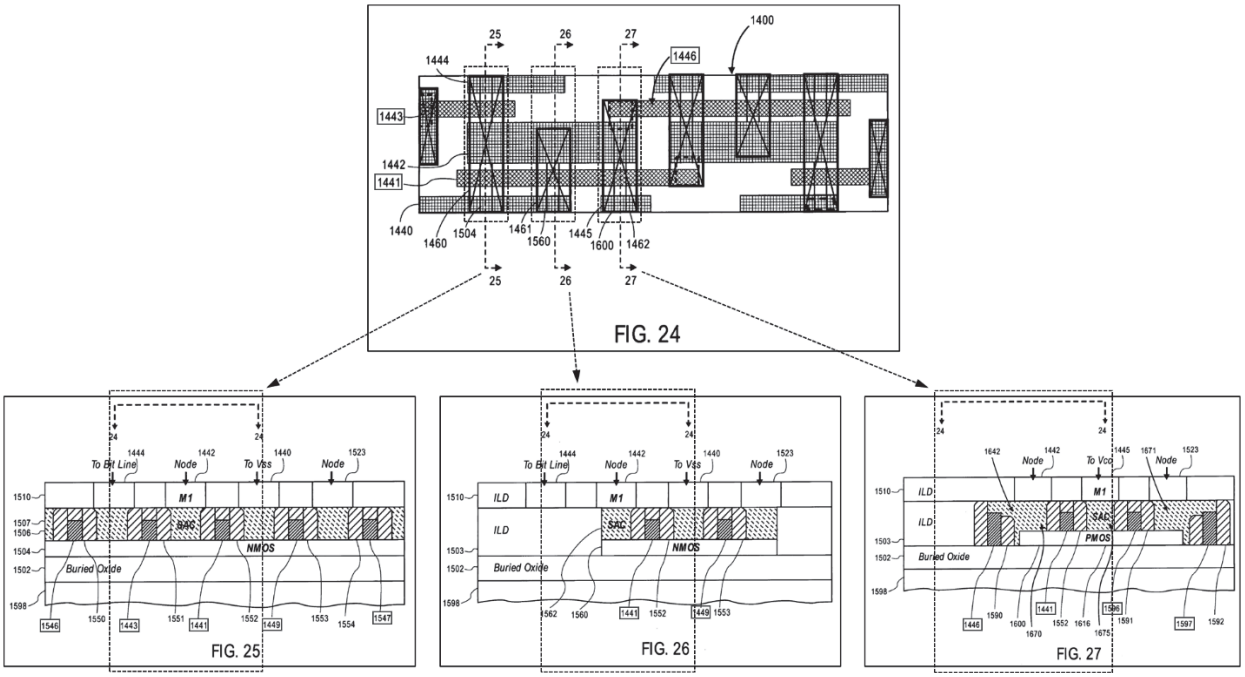


FIG. 5 FIG. 27

PA-04 (Chang), FIGs. 5, 27.

As discussed above, the gate structures of the SRAM are substantially the same, and are consistent with the descriptions related to FIG. 5, as well as the descriptions related to FIGs. 17-23.



PA-04, FIGs. 24-27. Chang's metal gates are "disposed in the first dielectric layer." This is evident from FIGs. 24-27. PA-04, ¶112; Ex-03, ¶¶432-433.

A POSITA's understanding of ILDs reinforces and is consistent with Chang's teachings of ILDs. As discussed in element 1(b), ILDs were known to have been formed in regions of the semiconductor structure as a layer where contact formation is blocked, and were known to fill the space between structural elements in a semiconductor structure. Furthermore, ILDs were known to be dielectric layers that provide insulation between two layers. In addition, electrical contacts or vias are generally made between the layers. This understanding of the metal gates and dielectric layer, for example as shown in FIG. 27, is also consistent with what is taught by the '747 Patent, as shown in the annotated FIG. 27 (Chang) and FIG. 9 ('747 Patent). Ex-03, ¶434.

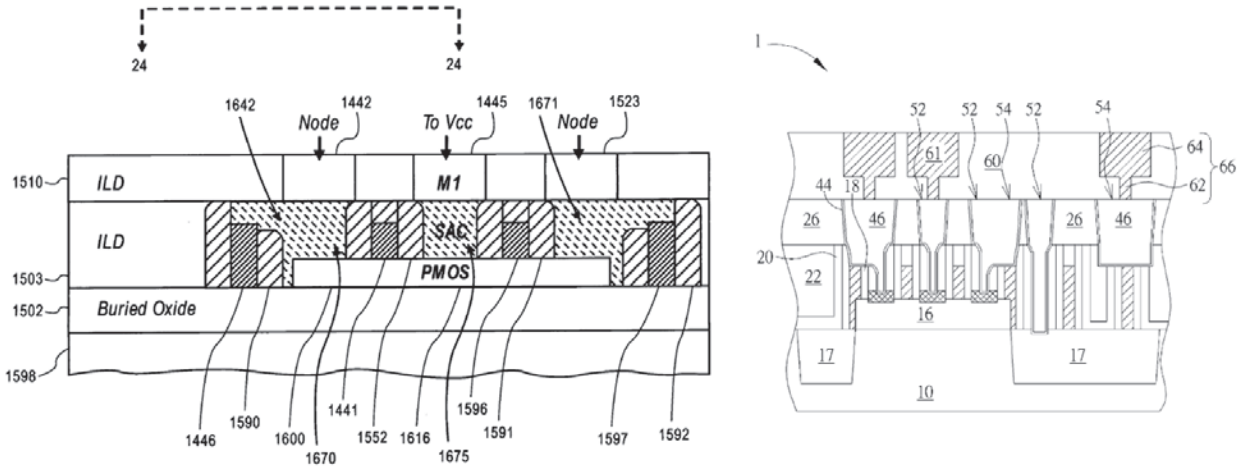


FIG. 27 FIG. 9

PA-04 (Chang), FIG. 27 (left), Ex-01 ('747 Patent), FIG. 9 (right).

Accordingly, Chang discloses that the SRAM includes at least two metal gates (e.g., any two of the gates 1441, 1443, 1446, 1449, 1546-47, 1596-97 disposed in

interlayer dielectric layer 1503 (i.e., the "first dielectric layer"); including as an example (but not limited to, as discussed above), all eight gates above, any combination of two or more of the eight gates, as an example gates 1441, 1449. In other specific examples, gates 1441, 1446 or gates 1596, 1597 discloses "at least two metal gates" that are disposed in interlayer dielectric layer 1503 (i.e., the "first dielectric layer"), as claimed. Thus, Chang discloses limitation 1(c). *See also* §§VI.B.1(a)(1)-(3), (a)(5)-(9) for limitations 1(pre)-1(b), 1(d)-1(h), and §III.D, incorporated herein. Ex-03, ¶435.

(5) [1.d] a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface;

Chang discloses this limitation. Ex-03, ¶436. For example, Chang discloses that the SRAM includes a spacer disposed on two sides of the metal gate,[26] wherein the spacer has a truncated top surface. Chang teaches that "gate structures 1552 and

[26] For purposes of analysis concerning the prior art (here and in the other proposed rejections discussed below), Requester assumes the term "disposed on two sides of **the metal gate**" refers to any of the metal gates that are included in the claimed semiconductor structure. As explained below, Chang discloses that spacers of gate structures 1552, 1591 are disposed on two sides of gates 1441, 1443, 1446, 1449, 1546-47, and/or 1596-97, and as one example on two sides of gates 1441 and/or 1596, which collectively is a non-limiting example of the claimed "at least two metal gates" recited in limitations 1(c).

1591 include spacers along with silicon nitride caps for the respective gates 1441 and 1596." PA-04, ¶112. This is illustrated in the below annotated FIG. 27.

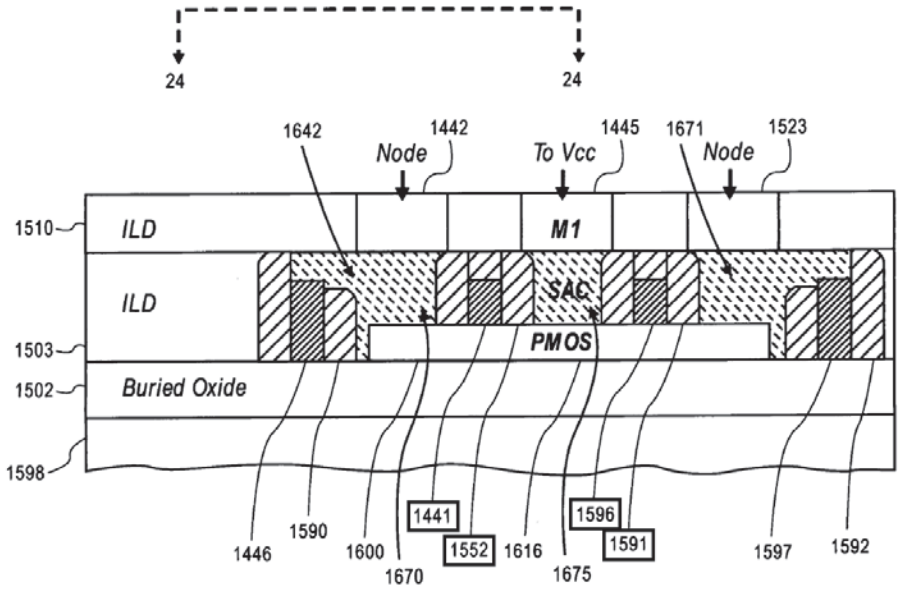


FIG. 27

PA-04, FIG. 27.

Spacers 1552 are "disposed on two sides of" gate 1441 (in this example, "the metal gate" which for example is one of the gates in the exemplary "at least two metal gates" including gates 1441, 1446 discussed in limitation 1(c)). PA-04, ¶112. This is shown in the above annotated FIG. 27, which also shows that spacers 1591 are "disposed on two sides of" gate 1596 (in this example, "the metal gate" which for example is one of the gates in the exemplary "at least two metal gates" including gates 1596, 1597 discussed in limitation 1(c)). PA-04, ¶112.

Chang's spacers in its SRAM disclose a spacer having a "truncated top surface" under Interpretations 1-3. *See* §II.D.1. In particular, Chang's spacers in its

SRAM include "a top surface of the spacer that has been truncated," where "truncated" means "planar" (Interpretation 1, *see* §II.D.1), "made shorter by removing a part" (Interpretation 2, *see id.*), and include "a top surface that has been made shorter by removing a part during a planarization process" (Interpretation 3, *see id.*). Ex-03, ¶¶437-438.

Chang describes in detail the deposition and *planarization process* for the self-aligned contacts in association with FIGs. 19-20. PA-04, ¶¶94-95. As Chang explains, this deposition and *planarization process* first involves depositing metal to fill open areas (which are indicated as, for example, 780, 781, and 782). This can be seen in FIG. 19. After depositing metal to fill open areas, Chang explains that "[a] polishing operation—or, alternatively, an etch operation—is then performed to **planarize the contact metal down to level 737**." PA-04, ¶¶94-95; Ex-03, ¶439.

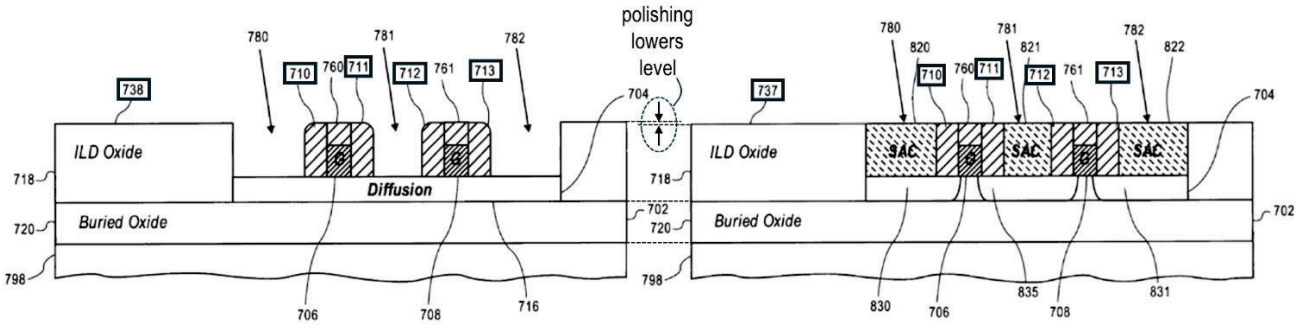


FIG. 19 FIG. 20

Id., FIGs. 19-20 (annotated).

Chang therefore explicitly states, and shows in FIGs. 19-20, that the polishing lowers the level of the top of the wafer from 738 (FIG. 19) to 737 (FIG. 20) during

the planarization process, meaning it has *a top surface that has been made shorter by removing a part during a planarization process*" (Interpretations 2 and 3, *see* §II.D.1). PA-04, ¶¶95 ("Level 737 is a level slightly below the original top level 738."), 94.). The fact that the *planarization process* lowers the level of the top from 738 (FIG. 19) to 737 (FIG. 20) means it *made shorter by removing a part* (Interpretations 2 and 3, *see* §II.D.1). Additionally, because a polishing operation is carried out on Chang's device in FIG. 19 (*see* PA-04, ¶¶94-95), a POSITA would understand that spacers 710-713 in resulting FIG. 20 would have enough of a *planar top surface* to be considered "truncated" (Interpretation 1, *see* §II.D.1). Ex-03, ¶440.

FIGs. 19 and 20 show that the *spacers* are at these respective levels – level 738 *before* the deposition and polish and level 737 *after* the deposition and polish is complete. Thus, the polishing removes spacer material and provides a truncated top surface under Interpretations 1-3 (§II.D.1) because the spacers are made shorter by removing a part during a planarization process, and have a planar top surface after a polishing operation. Ex-03, ¶441.

As previously discussed, it would have been readily apparent to a POSITA that the FIGs. 19 and 20 spacer teachings describe the formation of the spacers of gate structures 1552 and 1591 in the SRAM (described in FIGs. 24-27). Indeed, Chang explicitly states that these gate structures in the SRAM are disclosed in the context of Chang's "self-aligned contacts" with a "gate-protection option," which

Chang explains "is described with respect to FIGS. 17-27" (i.e., including both Figures 19-20 and Figures 24-27). PA-04, ¶52; Ex-03, ¶¶442-444.

As Chang further explains, "FIGS. 17 through 23 show wafer cross sections that illustrate operations in connection with the gate-protect option with respect to forming self-aligned contacts." PA-04, ¶89.

As another example, Chang explains that "FIG. 24 is a top view of a layout 1400 of an SRAM containing transistor structures with gate-protected self-aligned contacts… cross sections of the SRAM layout 1400 are shown in FIGS. 25, 26, and 27." PA-04, ¶107.

A POSITA would have appreciated that the FIGs. 17-23 and its related descriptions and teachings describe the formation of the SRAM (of FIGs. 24-27), as discussed in §II.D.1 and in limitation 1(c) above (each incorporated herein). In particular, FIGs. 17-23 describe forming the self-aligned contacts, and FIGs. 24-27 describe an SRAM that has those contacts. Ex-03, ¶445.

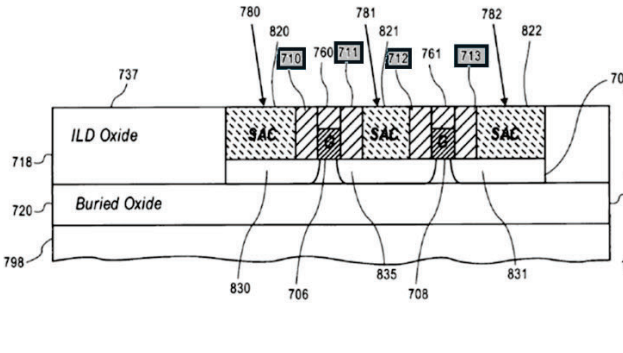


FIG. 20

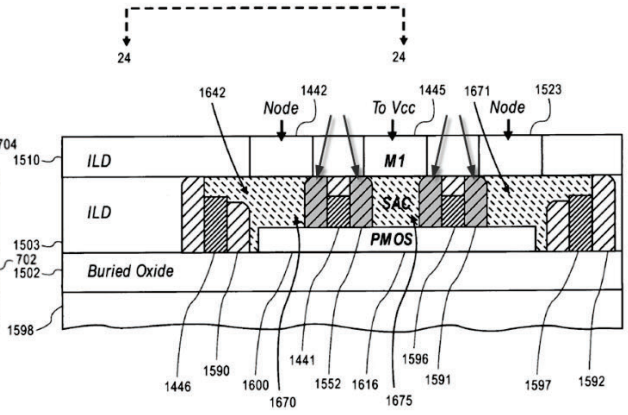


FIG. 27

PA-04 (Chang), FIGs. 20, 27.

A POSITA would have also appreciated this fact because Chang provides explicit explanation of why its spacers must be truncated – because the resulting contact metal areas "are not electrically interconnected with each other." PA-04, ¶¶94-95. Consistent with Chang, it would have been appreciated that electrical isolation, such as between separate contacts on the same or different transistors, has to be upheld to safeguard the functionality and operation of the IC and its transistors. This is applicable to the SRAM described in Chang. Based on these teachings, a POSITA would have understood that the SRAM is susceptible to electrical shorting without truncating the spacers. Ex-03, ¶446.

A POSITA was well aware of the concept of isolation and would have likewise appreciated its applicability to the SRAM described in Chang. For example, it was understood that contacts are not electrically isolated if contact metallization is not fully removed between contacts that are designed to be isolated. Consistent with this understanding of a POSITA, Chang teaches to maintain such isolation between its separate contacts where appropriate. Ex-03, ¶447.

For the reasons explained above, Chang discloses spacers of gate structures 1552 and 1591 that are disposed on two sides of the metal gate (e.g., gates 1441 and 1596) that have a "truncated top surface" under Interpretations 1 and 2 (*see* (§II.D.1). For example, as discussed above, Chang's spacers, once formed, have a *planar top*

surface (Interpretation 1) and are *made shorter by removing a part* (Interpretation 2) to provide the spacers at a lower level. Ex-03, ¶448.

Further, spacers 1552 are "disposed on two sides of" gate 1441 (in this example, "the metal gate" which is one of the gates in the exemplary "at least two metal gates" including gates 1441 and 1446 discussed in limitation 1(c)). Also, spacers 1591 are "disposed on two sides of" gate 1596 (in this example, "the metal gate" which for example is one of the gates in the exemplary "at least two metal gates" including gates 1596 and 1597 discussed in limitation 1(c)).

And, for the reasons explained above, the spacers are made shorter by removing a part during Chang's planarization process and thus have a "truncated top surface" under Interpretation 3 (i.e., make shorter by removing a part during a planarization process) (e.g., spacers 1552 disposed on two sides of metal gate 1441 (which is one of the gates in the exemplary "at least two metal gates" 1446, 1441 discussed for limitation 1(c)), and also spacers 1591 disposed on two sides of metal gate 1596 (which is one of the gates in the exemplary "at least two metal gates" 1596 and 1597 discussed for limitation 1(c)). Ex-03, ¶¶449-450.

Thus, Chang discloses limitation 1(d) at least under Interpretations 1-3 (*see* (§II.D.1) and plain meaning of the claim language. *See also* §§VI.B.1(a)(1)-(4), (a)(6)-(9) for limitations 1(pre)-1(c), 1(e)-1(h), and §III.D, incorporated herein. Ex-03, ¶451.

(6) [1.e] a source/drain region (S/D region) disposed between two metal gates;

Chang discloses this limitation. Ex-03, ¶¶452-462. Chang discloses that the SRAM includes a source/drain region (S/D region) disposed between two metal gates.

As an initial matter, Chang's invention and embodiments, including its SRAM, are taught from the perspective of transistor physics and engineering. PA-04, Title; Abstract; ¶¶1, 39, 41, 45-48, 89-090. Chang discloses what would have been well-known, elementary textbook knowledge to a POSITA – the transistors have basic features such as "gate structures" and "drain and source regions." PA-04, Title; Abstract; ¶¶1, 39, 41, 48, 63, 71, 89, 96, 98. These are all well-known features, and were well-known to be used with field effect transistors. Ex-03, ¶453.

These transistors, such as those shown in FIG. 27, are taught within the framework of Chang's "self-aligned contacts" with a "gate-protection option," that "is described with respect to FIGS. 17-27." PA-04, ¶52. As discussed in §II.D and limitations 1(c)-1(d) above (all incorporated herein), FIGs. 17-23 illustrate forming the self-aligned contacts in such transistor structures, and FIGs. 24-27 show multiple transistors with those contacts in an SRAM circuit configuration. Ex-03, ¶454.

With respect to FIG. 27's transistors, Chang explicitly describes that they include "gate structures" and a "diffusion region" (or "PMOS region" or "PMOS

layer") 1600. PA-04, ¶¶112-13. A POSITA would have appreciated that layer 1600 includes source/drain regions. PA-04, ¶¶112-13, 96-98. These source/drain regions are displayed below in the annotated illustrations of FIGs. 24 and 27, which would have been understood by a POSITA. As also shown in the annotations below, each source/drain region is disposed between two metal gates. PA-04, ¶¶112-13, 96-98. Ex-03, ¶455.

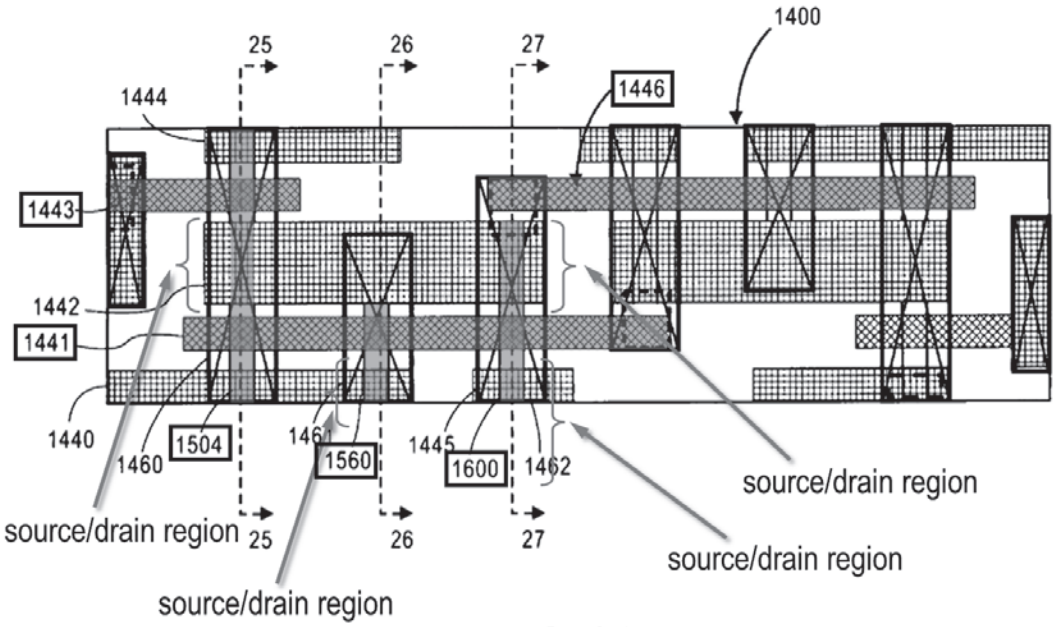


FIG. 24

PA-04 (Chang), FIG. 24.

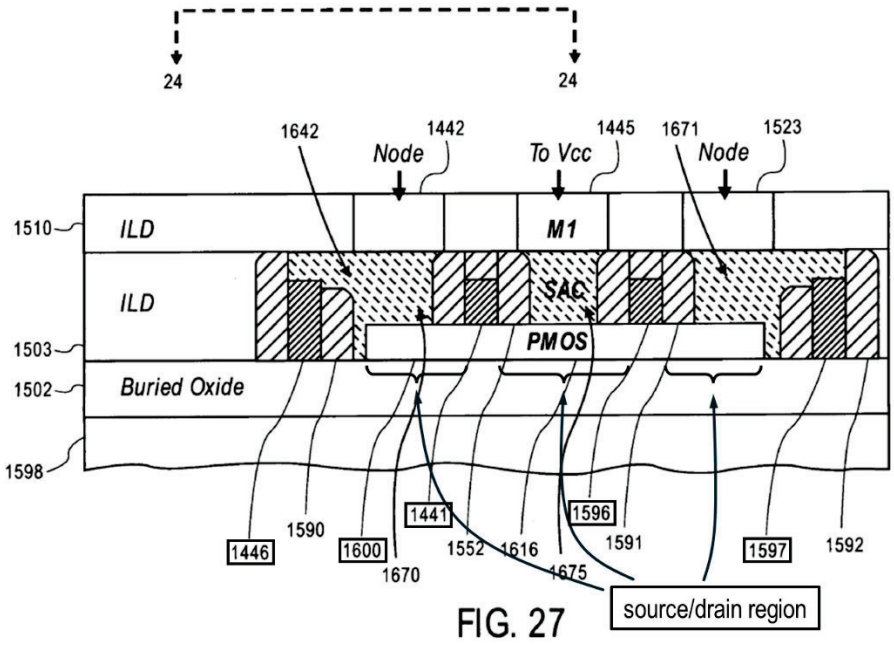


FIG. 27

Id., FIG. 27, ¶¶112-13, 96-98.

For purposes of analysis concerning the prior art (here and in the other prior art proposed rejections discussed below), Requester assumes the term "two metal gates" refers to any of the two metal gates that are included in the claimed semiconductor structure. For the purposes of Chang's disclosure of element 1(e), the aforementioned discussion would not change if the term "two metal gates" were found to refer to any of the "at least two metal gates" identified in element 1(c) (including, e.g., metal gates 1446, 1441 or metal gates 1596, 1597). Ex-03, ¶456.

For instance, as one example, Chang discloses that spacers of gate structures 1552, 1591 are disposed on two sides of gates 1441, 1596 (e.g., gate 1441 being one of the gates in the exemplary "at least two metal gates" 1446, 1441 discussed for

limitation 1(c), and gate 1596 being one of the gates in the exemplary "at least two metal gates" 1596, 1597 discussed for limitation 1(c)). Ex-03, ¶¶457-459.

As shown in the annotated FIG. 27 above, as further non-limiting examples of "two metal gates" that satisfy element 1(e), an S/D region is "disposed between" gates 1441, 1449 ("two metal gates"), gates 1441, 1446 ("two metal gates"), gates 1441, 1596 ("two metal gates"), gates 1596, 1597 ("two metal gates"), gates 1441, 1597 ("two metal gates"), gates 1446, 1597 ("two metal gates"), and gates 1446, 1596 ("two metal gates"), each non-limiting example independently satisfy "two metal gates."

Further regarding Chang's S/D region, Chang's FIG. 20 and its related teachings explicitly describe a "diffusion area 704" that contains drain regions 830, 831 and source region 835, which is a source/drain region (S/D region) disposed between two metal gates 706, 708, as shown in the annotated FIG. 20 below. As also indicated in the annotated FIGs. 24 and 27 above, the source/drain region (S/D region) of diffusion region 1600 are located in the corresponding locations.

As discussed above, FIGs. 20, 24-27 and corresponding descriptions describe Chang's "self-aligned contacts" with a "gate-protection option." PA-04, ¶52. These teachings are methods and operations for forming the SRAM of FIGs. 24-27 for the same reasons previously discussed. *See* §II.D and limitations 1(c)-1(d) above (all incorporated herein). Ex-03, ¶460.

A POSITA would have understood that this arrangement is a conventional source, drain, and gate in a field effect transistor. The relative location and placement of the features and related engineering considerations would have been well-known to a POSITA. Thus, the diffusion layer 1600 of FIG. 27 includes a **source/drain region (S/D region)**, as described above, including a **source/drain region (S/D region)** disposed between the **two metal gates 1441, 1596**, as explicitly taught by Chang and as understood by a POSITA in view of Chang's teachings. Ex-03, ¶461.

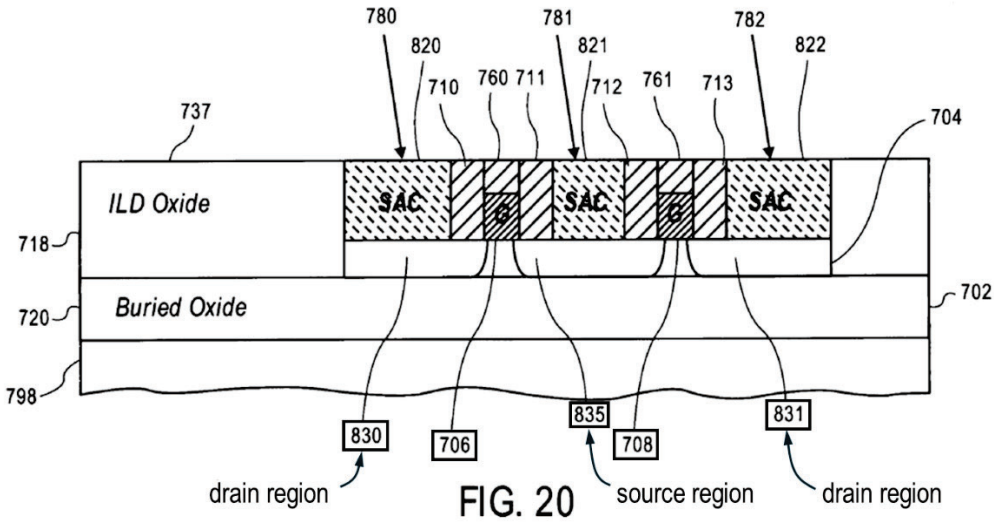


FIG. 20

PA-04, FIG. 20.

Therefore, the SRAM includes **a source/drain region (S/D region)** of PMOS diffusion layer 1600 which is **"**disposed between two metal gates" (e.g., any two of the gates 1441, 1443, 1446, 1449, 1546-47, 1596-97, including as an example, gates 1441, 1596 that are "two metal gates", gates 1441, 1446 that are "two metal gates",

or gates 1596, 1597 that are "two metal gates") as claimed in limitation 1(e). *See also* §§VI.B.1(a)(1)-(5), (a)(7)-(9) for limitations 1(pre)-1(d), 1(f)-1(h), and §III.D, incorporated herein. Ex-03, ¶462.

(7) [1.f] a plurality of first contacts disposed in the first dielectric layer that are electrically connected to parts of the S/D region;

Chang discloses this limitation. Ex-03, ¶¶463-466. Chang discloses that the SRAM includes a plurality of first contacts disposed in the first dielectric layer (discussed for limitation 1(b)) that are electrically connected to parts of the S/D region (as discussed for limitation 1(e)).

For example, parts of self-aligned contacts 1670, 1671, and self-aligned contact 1675 (which are indicated in the annotated illustration of FIG. 27 below) are "a plurality of first contacts that are electrically connected to parts of the" S/D regions of PMOS diffusion layer 1600 and are "disposed in" interlayer dielectric layer 1503 (identified as "the first dielectric layer"). PA-04, ¶¶112-13.

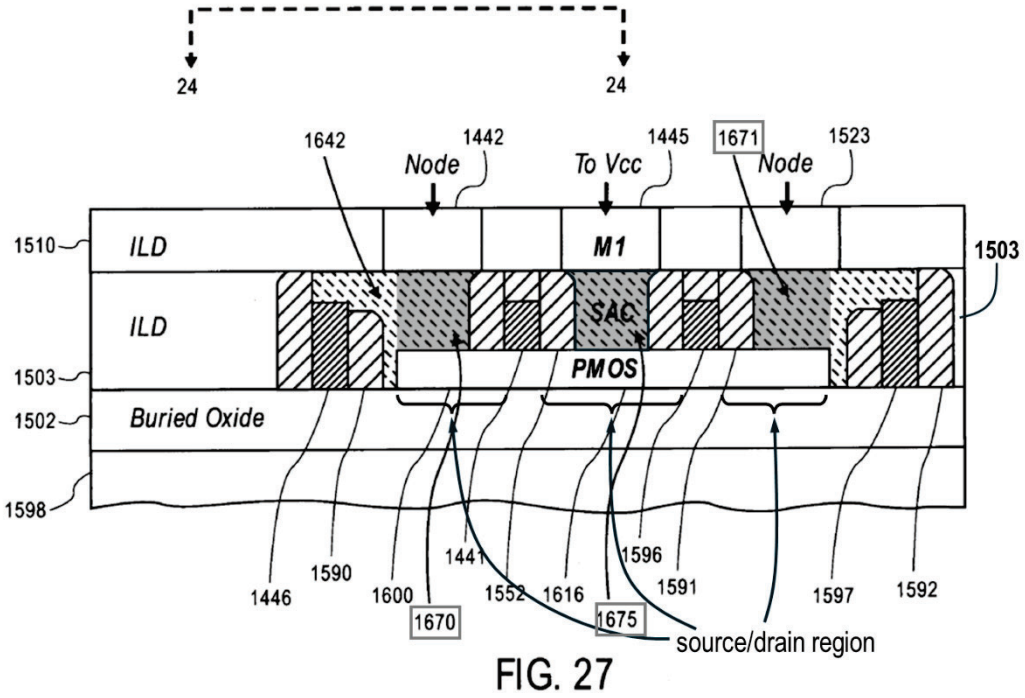


FIG. 27

PA-04 (Chang), FIG. 27, ¶¶112-13.

Chang states that "each of the respective self-aligned contacts 1670 and 1671" contacts the respective "adjacent PMOS diffusion region 1600." PA-04, ¶¶112-13.

Therefore, the SRAM includes "a plurality of first contacts" (e.g., parts of self-aligned contacts 1670, 1671, and self-aligned contact 1675) "disposed in the first dielectric layer" (e.g., interlayer dielectric layer 1503) "that are electrically connected to parts of the S/D region" (e.g., source and drain regions of PMOS diffusion layer 1600), as claimed in limitation 1(f). *See also* §§VI.B.1(a)(1)-(6), (a)(8)-(9) for limitations 1(pre)-1(e), 1(g)-1(h), and §III.D, incorporated herein. Ex-03, ¶¶463-466.

(8) [1.g] a plurality of second contacts disposed in the first dielectric layer that are electrically connected to one of the metal gates, wherein at least one of the first contacts directly connects at least one of the second contacts; and

Chang discloses this limitation. Ex-03, ¶¶467-481. Chang discloses that the SRAM includes a plurality of second contacts disposed in the first dielectric layer (as discussed for limitation 1(b)) that are electrically connected to one of the metal gates[27] (as discussed the metal gates for limitation 1(c)), wherein at least one of the

[27] For purposes of analysis concerning the prior art (here and in the other proposed rejections discussed below), Requester assumes the term "a plurality of second contacts…that are electrically connected to one of the metal gates" encompasses such features in the same way as in the '747 Patent. That is, while the '747 Patent does not disclose or suggest such features, it is assumed for purposes of prior art analysis that such claim features at least encompass and are met in the same or similar way that the '747 Patent discloses its semiconductor structure (e.g., where the structure of FIG. 9 simply shows single second contacts 54 connected to individual metal gates 12 with no other discussion of multiple second contacts 54 being electrically connected to a single metal gate). In doing so, Requester does not agree that the '747 Patent adequately discloses or enables the claimed features in limitation 1(g) or does so in such a way that a POSITA could reasonably ascertain the scope of the claimed invention. Nonetheless, as explained below in this Proposed Rejection 2A, Chang discloses that multiple second contacts (e.g., self-aligned contact such as 1670, 1671) are electrically connected to one of the gates 1446, 1597), thus meeting the claim language in limitation 1(g).

first contacts (as discussed for limitation 1(f)) directly connects at least one of the second contacts, as claimed in limitation 1(g).

For example, Chang discloses self-aligned contacts 1670, 1671 (as indicated in the annotated illustration of FIG. 27 below) that are "a plurality of second contacts" that "are electrically connected to" gates 1446, 1597 and are "disposed in" interlayer dielectric layer 1503. PA-04, ¶¶112-13.

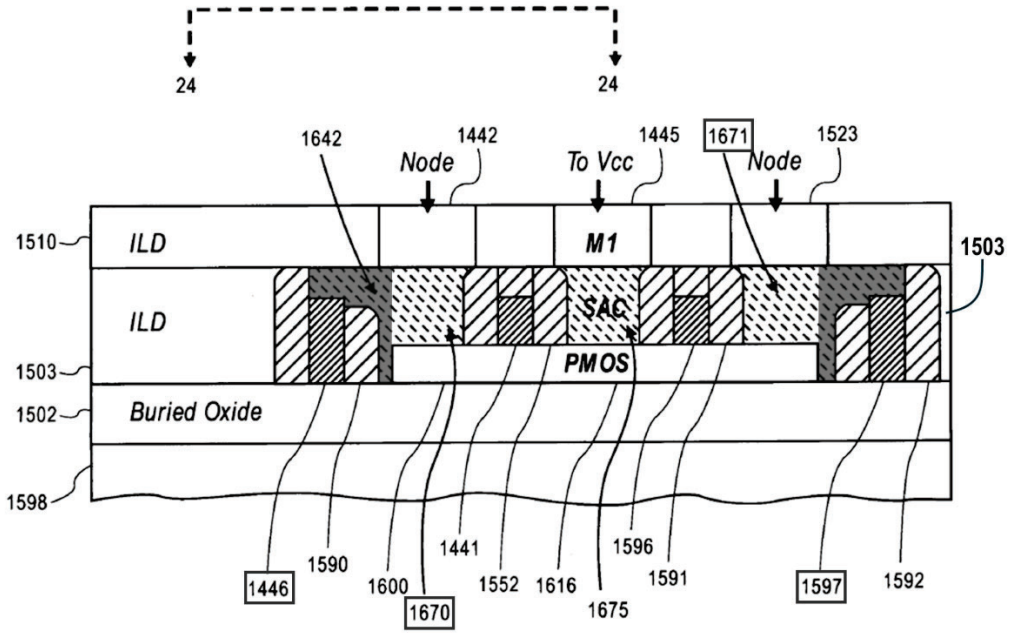


FIG. 27

PA-04 (Chang), ¶¶112-13.

As explained above, Requester assumes for purposes of prior art analysis that such claim features at least encompass and are met in the same or similar way that the '747 Patent discloses its semiconductor structure (e.g., where the structure of FIG. 9 simply shows single second contacts 54 connected to individual metal gates

12 with no other discussion of multiple second contacts 54 being electrically connected to a single metal gate). In doing so, Requester does not agree that the '747 Patent adequately discloses or enables the claimed features in limitation 1(g) or does so in such a way that a POSITA could reasonably ascertain the scope of the claimed invention. Ex-03, ¶469.

Under this assumption, Chang discloses the claimed "plurality of second contacts" that are "electrically connected to one of the metal gates" in a manner similar to the way that the '747 Patent discloses its semiconductor structure (e.g., where the structure of FIG. 9 simply shows single second contacts 54 connected to individual metal gates 12 with no other discussion of multiple second contacts 54 being electrically connected to a single metal gate). *See e.g.*, Ex-01, FIGs. 8-9, 5:1-6:37; PA-04, FIG. 27 (*see e.g.,* annotations above), 12:54-13:19. Ex-03, ¶470. Just like the '747 Patent, Chang's FIG. 27 structure includes multiple second contacts (e.g., parts of self-aligned contacts 1670, 1671) that are electrically connected to a respective metal gate (e.g., gates 1446, 1597). A POSITA would have understood self-aligned contacts 1670, 1671 provide an electrical connection to the metal gates 1446, 1597. *Id.* As discussed above for limitations 1(c)-1(e), metal gate 1446 is one of the exemplary "at least two metal gates" and/or "two metal gates" including gates 1446, 1441 identified for limitations 1(c) and 1(e), and metal gate 1597 is one of the

other exemplary "at least two metal gates" and/or "two metal gates" including gates 1596, 1597 identified for limitations 1(c) and 1(e). *Id.*

For instance, in the SRAM, (at least the identified part) of self-aligned contacts 1670 is electrically connected to gate 1446 (an example of one of the metal gates), and (at least the identified part) of self-aligned contacts 1671 is electrically connected to gate 1597 (an example of one of the metal gates), and thus the plurality of second contacts...are electrically connected to one of the metal gates similar to that in the '747 Patent. *See* PA-04, ¶¶112-13. Thus, (at least the identified part) of self-aligned contacts 1670 is electrically connected to 1446 (one of the metal gates), and (at least the identified part) of self-aligned contacts 1671 is electrically connected to 1597 (one of the metal gates), and thus Chang discloses "a plurality of second contacts...are electrically connected to one of the metal gates" in a manner similar to the way that the '747 Patent discloses its semiconductor structure with second contacts 54 and metal gates 12 only showing single second contact with a respective metal gate 12. Ex-03, ¶471.

Additionally, Chang discloses that the identified parts of self-aligned contacts 1670, 1671 (a plurality of second contacts) that are connected to one of the gates 1446, 1597 (e.g., one of the metal gates). For instance, as explained in element 1(d) (incorporated herein), the self-aligned contacts of the SRAM are formed by a metal deposition and subsequent planarization process. Ex-03, ¶472.

As shown in FIG. 27 below, the "metal one" (i.e., M1) layer, including its electrically connected metal lines, are "deposited directly above the layer containing the self-aligned contact." PA-04, ¶¶52, 112-13. Chang further explains that "the gate contact may be formed at the same time the metal one layer is formed." Chang, ¶105. In either case, the self-aligned contacts (including 1670, 1671) are electrically connected to the M1 layer. PA-04, ¶¶52, 105-108, 95-97, 112-13. Ex-03, ¶473.

As such, each self-aligned contact (including 1670, 1671) is electrically connected to a respective one of gates 1446, 1597 by the conductive M1 layer, including its metal lines that are provided to electrically connect. Thus, for this additional reason, Chang discloses "a plurality of second contacts" that are "electrically connected to one of the metal gates" as claimed in limitation 1(g). Again, as explained above, metal gate 1446 is one of the exemplary "at least two metal gates" and/or "two metal gates" including gates 1446, 1441 identified for limitations 1(c) and 1(e), and metal gate 1597 is one of the other exemplary "at least two metal gates" and/or "two metal gates" including gates 1596, 1597 identified for limitations 1(c) and 1(e). Ex-03, ¶474.

Additional examples of second contacts include metal gate contacts in notch 1105. PA-04, ¶105, FIG. 23. As Chang explains, "each of the respective self-aligned contacts 1670 and 1671" "contacts the respective gate." PA-04, ¶105, FIG. 23. Chang discloses that the SRAM includes "at least one of the first contacts

directly connects at least one of the second contacts" as recited in limitation 1(g) under what is understood an interpretation of "directly connects" (i.e., "at least one of the first contacts connects with at least one of the second contacts with no intervening layer or material therebetween," Interpretation 4). *See* §II.D.2.

Chang discloses that at least one of the first contacts directly connects at least one of the second contacts. Chang teaches that for "gate structures 1590 and 1592, each of the respective self-aligned contacts 1670 and 1671 acts as a **merged contact**." PA-04, ¶¶112. In other words, each self-aligned contacts 1670, 1671 has respective portions that serve as second contacts to the gate and first contacts to parts of PMOS region source/drain region, and are "merged" with no intervening layer or material therebetween. Ex-03, ¶¶475-478.

For example, for "merged contact" 1670, the right portion (as shown in the annotated FIG. 27 below) of self-aligned contact 1670 (at least one of the first contacts) directly connects the left portion (as shown in the annotated FIG. 27 below) of self-aligned contact 1670 (at least one of the second contacts). The same is true for merged contact 1671. PA-04, ¶¶112-13. As shown, there are no intervening layers or materials therebetween. It is apparent from the figures of Chang that there are no intervening layer or material therebetween, and there are also no descriptions of such in the written description. Further, the annotated regions below were formed by a single metal deposition (as explained in element 1(d) and 1(f), incorporated

herein), which means the direct connection is a monolithically formed structure with no intervening layer or material therebetween (*see* Interpretation 4, §II.D.2). Ex-03, ¶479.

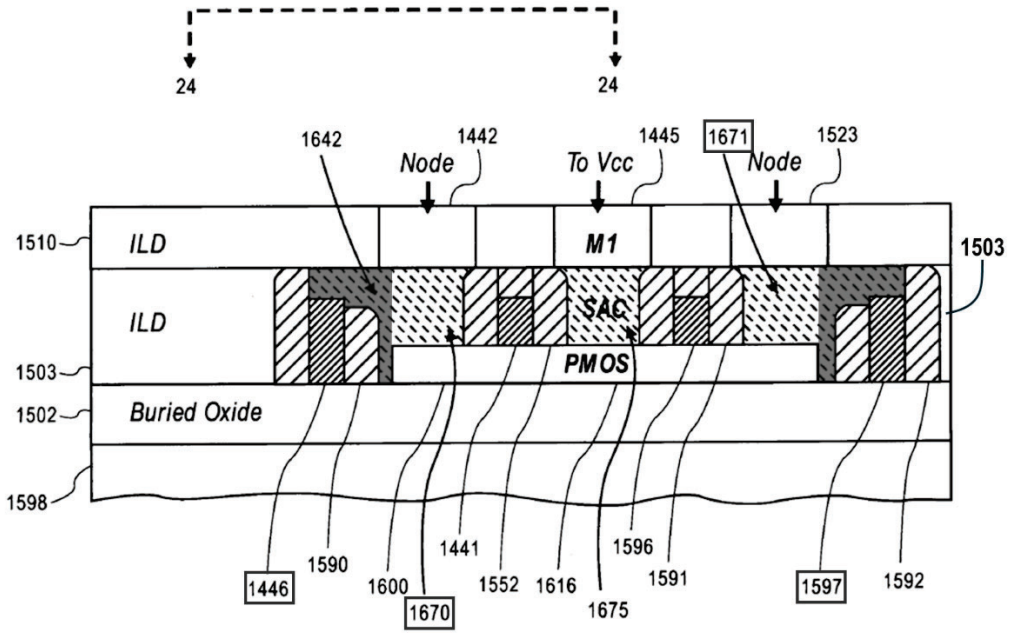


FIG. 27

PA-04, ¶¶112-13.

A "merged contact" generally refers to multiple contacts that are merged together, and Chang uses the term consistently with the ordinary meaning. For example, Chang explains that the two contacts that are "merged" each serve a separate role based on what structure they contact (i.e., either the gate or the PMOS region). PA-04, ¶¶112-13; Ex-03, ¶480.

Therefore, the SRAM includes "a plurality of second contacts (e.g., self-aligned contacts 1670, 1671) disposed in the first dielectric layer (e.g., interlayer

dielectric layer 1503) that are electrically connected to one of the metal gates (e.g., gates 1446, 1597; *see* the discussion above for this feature of limitation 1(g)) wherein at least one of the first contacts directly connects (no intervening material or layer) at least one of the second contacts" (discussed above), as claimed in limitation 1(g). *See also* §§VI.B.1(a)(1)-(7), (a)(9) for limitations 1(pre)-1(f), 1(h), and §III.D, incorporated herein. Ex-03, ¶481.

(9) [1.h] a hard mask disposed on one of the metal gates, wherein the top surface of the hard mask and the top surface of the first dielectric layer are on the same level.

Chang discloses this limitation. Ex-03, ¶¶482-490. Chang discloses that the SRAM includes "a hard mask disposed on one of the metal gates[28], wherein the top surface of the hard mask and the top surface of the first dielectric layer are on the same level," as claimed in limitation 1(h). For example, Chang discloses silicon

[28] For purposes of analysis concerning the prior art (here and in the other proposed rejections discussed below), Requester assumes the term "disposed on **two sides of one of the metal gates**" refers to any of the metal gates that are included in the claimed semiconductor structure. As explained below, Chang discloses the "hard mask" as recited in limitation 1(h).

nitride caps that are a hard mask disposed on the gates 1441, 1596.[29] PA-04, ¶¶111-13; Ex-03, ¶¶482-483.

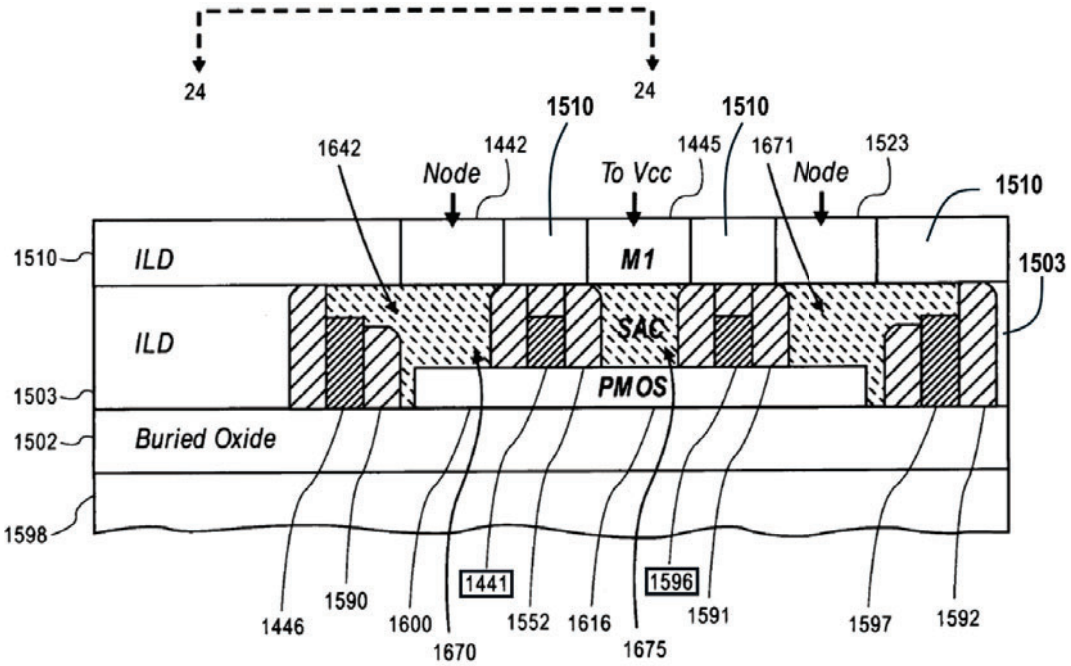


FIG. 27

[29] As explained above for limitations 1(c)-1(e) and 1(g), metal gate 1446 is one of the exemplary "at least two metal gates" and/or "two metal gates" including gates 1446, 1441 identified for limitations 1(c) and 1(e), and metal gate 1597 is one of the other exemplary "at least two metal gates" and/or "two metal gates" including gates 1596, 1597 identified for limitations 1(c) and 1(e). Thus, in such non-limiting examples of gates, metal gate 1446 is an example of "one of the metal gates" as recited in limitation 1(h) that includes e.g., gates 1446, 1441 identified as examples for limitations 1(c) and 1(e), and metal gate 1597 is an example of "one of the metal gates" that includes e.g., gates 1596, 1597 identified as examples for limitations 1(c) and 1(e).

PA-04, FIG. 27.

Chang teaches that the silicon nitride caps are a hard mask, as they provide protection to the structure or structures that are underneath it. For example, Chang further explains that "[i]f there were alignment errors, then the metal one layer 1510 could short to the gates of gate structures 1550-1554 if those gates were not protected by the silicon nitride caps above those respective gates." PA-04, ¶111, ¶¶92-93 (silicon nitride caps "act as protection for" gates), ¶99 ("the metal gates 706 and 708 are protected by respective silicon nitride caps 760 and 761").

A POSITA would have understood that hard masks were well known to be formed of silicon nitride. The '747 Patent acknowledges this, as it explains that "the hard mask 24 mainly comprise silicon nitride." Ex-01, 3:20-21. As shown in the annotated FIG. 27 above, the top surface of silicon nitride caps and the top surface of interlayer dielectric layer 1503 are on the same level, which is the level of the interface between ILD 1503, 1510. This is further confirmed by Chang's disclosure of the process used to form its gate-protected self-aligned contacts whereby a "silicon nitride layer is formed over the top" of the wafer "by deposition," and "planarized by polishing the top of [the] wafer," thereby resulting in the top surface of the silicon nitride cap (hard mask) and the top surface of the ILD (first dielectric layer) on the same level. PA-04, ¶92, FIG. 18; Ex-03, ¶¶484-486.

As Chang explains, "[t]he polishing is done down to the top 738 of wafer 702," which is also the top surface of the first dielectric layer. PA-04, ¶92, FIG. 18. A POSITA would have understood that the subsequent deposition and planarization of its self-aligned contacts (*see* element [1.e]) would have polished down the entire top surface by the same amount (as discussed in element [1.e]), including the silicon nitride caps and interlayer dielectric layer 1503. Ex-03, ¶487.

As discussed above, the silicon nitride caps are to provide protection to the gates below it (in ILD 1503) from the metal one layer (in ILD 1510). Therefore, for the reasons above, the SRAM includes "a hard mask (e.g., silicon nitride caps) "disposed on one of the metal gates" (e.g., gates 1441, 1443, 1449, 1546-47, 1596; such as for example, one of gates 1441, 1596)[30], "wherein the top surface of the hard mask (e.g., silicon nitride caps) and the top surface of the first dielectric layer (e.g., interlayer dielectric layer 1503) are on the same level, as claimed in limitation 1(h). *See also* §§VI.B.1(a)(1)-(8) for limitations 1(pre)-1(g), and §III.D, incorporated herein. Ex-03, ¶¶488-490.

[30] Again, as noted above, metal gate 1446 is an example of "one of the metal gates" as recited in limitation 1(h) that includes e.g., gates 1446, 1441 identified as examples for limitations 1(c) and 1(e), and metal gate 1597 is an example of "one of the metal gates" that includes e.g., gates 1596, 1597 identified as examples for limitations 1(c) and 1(e).

In light of the teachings in Chang above, Chang anticipates claim 1 and thus the claim is invalid.

b. Claim 2: The semiconductor device of claim 1, further comprising a second dielectric layer disposed on the first dielectric layer.

Chang discloses this limitation. Ex-03, ¶¶491-493. Chang discloses the SRAM including a second dielectric layer disposed on the first dielectric layer. For example, Chang's layer 1510 includes an interlayer dielectric (i.e., "a second dielectric layer") that is "disposed on" layer 1503 (i.e., "the first dielectric layer"). This is shown in annotated illustration of FIG. 27 below. PA-04, ¶113.

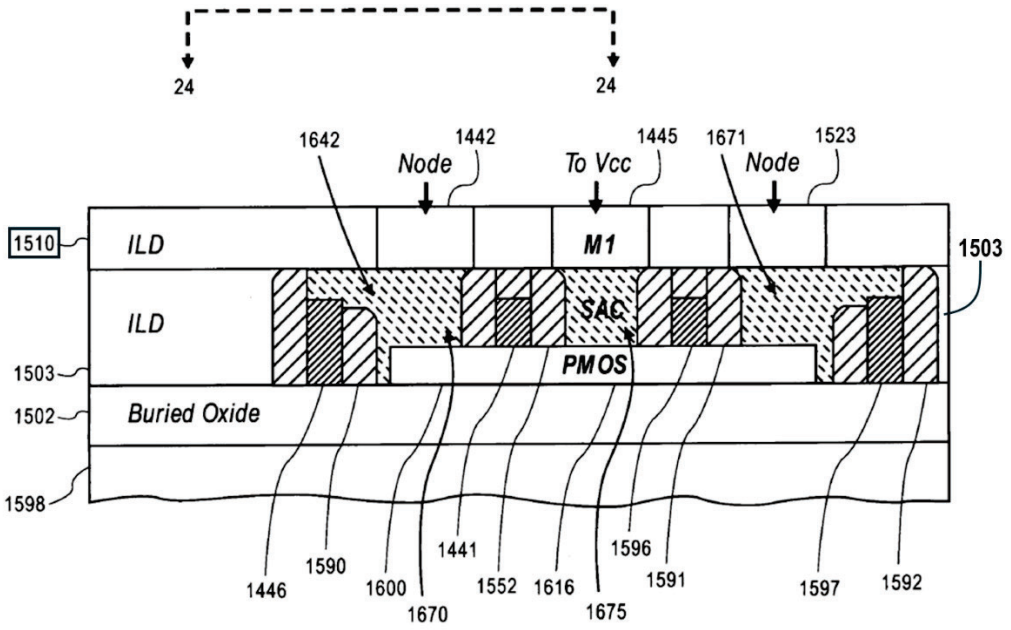


FIG. 27

PA-04, FIG. 27, ¶113.

Chang's "metal one layer 1510 includes an interlayer dielectric that includes openings containing the metal lines 1442, 1445, and 1523." PA-04, ¶113.

Therefore, for the reasons above, the SRAM includes "a second dielectric layer (e.g., an interlayer dielectric of metal one layer 1510) disposed on the first dielectric layer (e.g., interlayer dielectric layer 1503), as claimed in claim 2. Ex-03, ¶¶492-493. *See also* §§VI.B.1(a), III.D, incorporated herein.

c. Claim 6: The semiconductor device of claim 1, further comprising at least one fin structure disposed on the substrate.

Chang discloses this limitation. Ex-03, ¶¶494-498. Chang discloses the SRAM including at least one fin structure disposed on the substrate, as recited in claim 6. The Sections above discuss how Chang discloses the limitations of Claim 1. Those discussions are incorporated here in support of claim 6.

As discussed with respect to element 1(e) (incorporated herein), Chang teaches a "PMOS region" or "diffusion region" 1600, which is "disposed on" silicon substrate 1598 for the same reasons the first dielectric layer is disposed on the substrate in element 1(b) (incorporated herein). PA-04, ¶¶110-112.

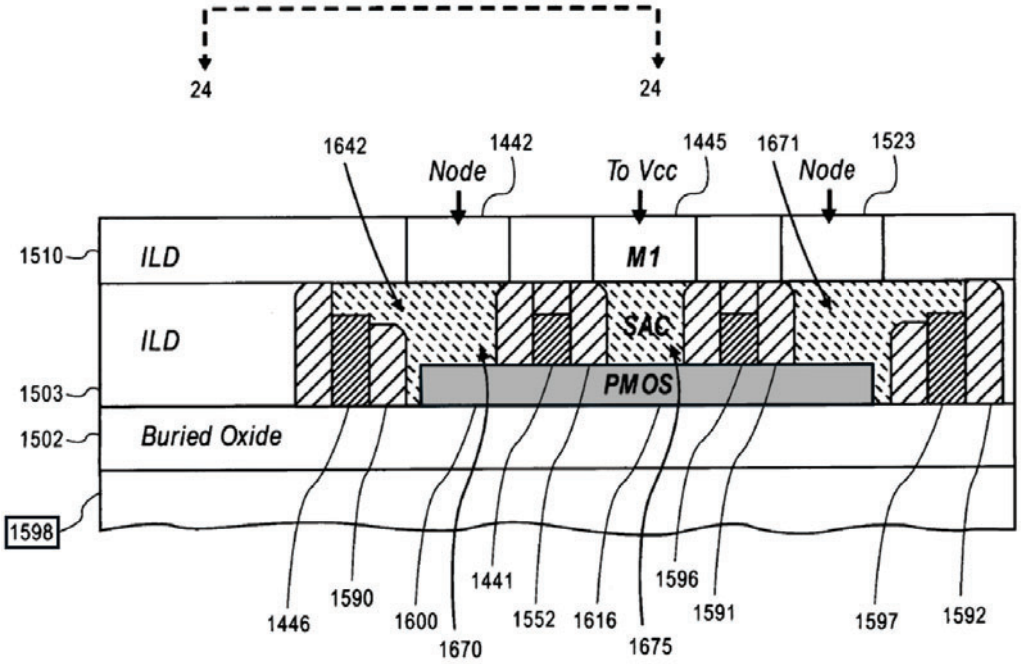


FIG. 27

PA-04, FIG. 27, ¶113.

As discussed in element 1(e) (incorporated herein), this diffusion region would have been implemented as a diffusion area 704 in FIG. 20. A POSITA would have understood this diffusion region would have been implemented as a diffusion area 704. Ex-03, ¶496.

With respect to FIG. 5, Chang further explains that "transistor structure 116 includes diffusion layer 104 (also called diffusion body 104 or **fin 104**)." A POSITA would have understood that diffusion area 704 could be "also called" a fin, which means it is "comprising at least one fin structure disposed on the substrate," as recited in claim 6. PA-04, ¶48; Ex-03, ¶497.

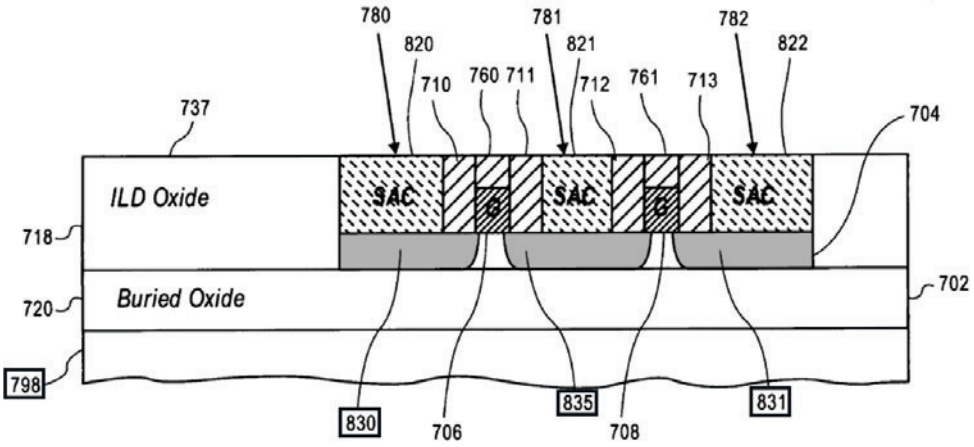


FIG. 20

PA-04, FIG. 20.

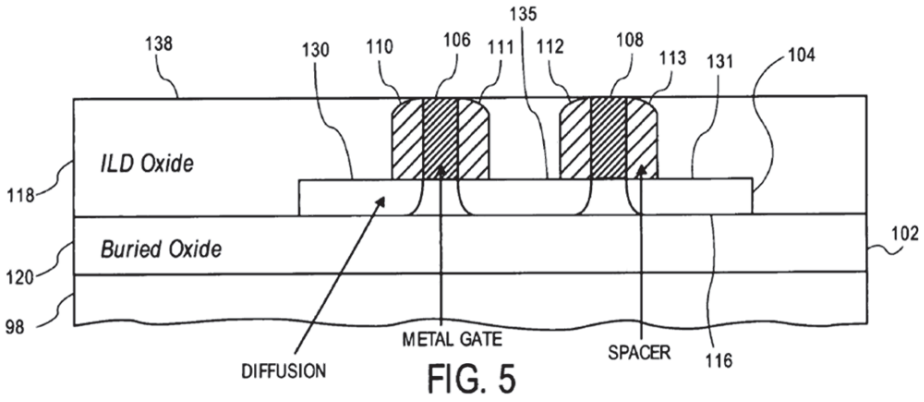


FIG. 5

PA-04, FIG. 5.

In light of the teachings in Chang above, Chang anticipates Claim 6 and thus the claim is invalid. *See also* §§VI.B.1(a), III.D, incorporated herein.

2. Proposed Rejection 2B: Claims 1-2 and 4-6 Are Obvious Over *Chang*

Proposed Rejection 2A discusses how Chang anticipates and renders invalid Claims 1-2 and 6 of the '747 Patent. Notwithstanding the disclosures in Chang, it is explained how and why a POSITA would have been motivated to consider the

teachings and suggestions within the four corners of Chang, including the various aspects and embodiments disclosed there, and in light of such collective disclosures, found it obvious to configure the SRAM to include features described in the various aspects described in the four corners of Chang. Consequently, as discussed below, such obvious variations gleaned from the teachings throughout Chang would have predictably resulted in an unmodified or a slightly modified semiconductor structure of the SRAM that renders obvious Claims 1-2 and 4-6. Ex-03, ¶¶499-551.

To begin, a POSITA reviewing Chang would have understood, appreciated, and recognized that Chang discloses related features directed to semiconductor devices and processing and in particular to gate contact structures that are disposed over active portions of gates, and processes for forming such structures. PA-04, Abstract, ¶¶1-27. As explained in §III.D, Chang frames the disclosed inventions in context of semiconductor devices and structures, including the fabrication of semiconductor devices and integrated circuit devices including MOS transistors, including multi-gate (e.g., tri-gate) transistors, and other semiconductor structural elements, such as self-aligned contacts, gate and trench contact structures, etc. PA-04, Abstract, ¶¶1-27, ¶¶45-117. Chang describes various embodiments and related aspects directed to semiconductor structures and the fabrication of such devices that include features common to the various disclosed embodiments, including self-

aligned contacts and gate and trench contact structures, metal gate structures, cap layers, etc. *Id.*, Ex-03, ¶500.

As discussed in §III.D and throughout Proposed Rejection 2A (incorporated herein), Chang provides teaching directed to the semiconductor structures and self-aligned contacts for transistors, as well as teachings of their fabrication. PA-04, Abstract, ¶¶1-117. Chang's SRAM described in FIGs. 24-27 discloses Claims 1-2 and 6, as asserted in Proposed Rejection 2A. Further, a POSITA would have been motivated to combine teachings from other aspects of Chang in light of a POSITA's state of art knowledge when considering and implementing the SRAM. Ex-03, ¶501.

Chang's embodiments all relate to self-aligned contacts and methods of fabricating such contacts, and the embodiments compliment and build upon each other by describing various aspects of such self-aligned contacts. Accordingly, a POSITA would have been motivated to incorporate various teachings/suggestions from Chang's embodiments, and would have been assisted by a POSITA's state of art knowledge in doing so. PA-04, Abstract, ¶¶36-37, 114-117; Ex-03, ¶502. Given the embodiments compliment and build upon each other by describing various aspects of such self-aligned contacts, a POSITA would have been motivated to consider and implement these related teachings of Chang, and from state of art knowledge, when forming/configuring the SRAM of FIGs. 24-27, and would have

had a reasonable expectation of success in such implementations. Ex-03, ¶¶502-503.

A POSITA would have recognized implementing the SRAM of FIGs. 24-27 would have involved use of the teachings, such as the specific aspects described in greater detail, already contemplated by the teachings of Chang as a whole, and consistent with a POSITA's knowledge, found in the various figures and descriptions of Chang. *Id*. Thus, for these reasons, as well as those discussed below, a POSITA would have been motivated to implement Chang's SRAM with the state of art knowledge of a POSITA and to combine certain teachings and suggestions from the various disclosed aspects of Chang, would have predictably resulted in a structure meeting the identified challenged claims as explained below. *Id*.

In addition to Chang's discussions of features discussed in other portions of Chang's disclosure (e.g., FIGs. 5, 17-23, etc.) being incorporated in the teachings for Chang's SRAM of FIGs. 24-27, a POSITA would have been motivated to consider and implement them when forming/configuring the FIGs. 24-27 structure (as discussed in Proposed Rejection 2A above and below), and would have had a reasonable expectation of success in doing so. Ex-03, ¶504.

Combination of Chang's Embodiments

Chang discloses various aspects regarding the layout and fabrication of semiconductor structures and self-aligned contacts for transistors. *See* PA-04

(Chang), ¶1, ¶¶17-44; *id.*, *generally* ¶¶45-117. While as explained in Proposed Rejection 2A, Chang's discussions relating to FIGs. 24-27 disclose the features of Claims 1-2 and 6 (§III.D), a POSITA would have been motivated to combine teachings from other aspects of Chang in light of a POSITA's state of art knowledge when considering and implementing the structure associated with FIGs. 24-27 as addressed in Proposed Rejection 2A. Ex-03, ¶505.

A POSITA would have been motivated to incorporate various teachings/ suggestions from Chang's embodiments given they all relate to various aspects of self-aligned contacts and methods of fabricating such contacts in a semiconductor structure and do so while leveraging their state of art knowledge. PA-04 (Chang), Abstract, ¶¶36-37, 114-117; Ex-03, ¶506.

Given such related teachings/suggestions, a POSITA would have been motivated to consider and implement from teachings related to other aspects of Chang's invention, and from their state of art knowledge, when forming/configuring the FIGs. 24-27 structure and would have had a reasonable expectation of success in achieving such implementations. Ex-03, ¶¶507-508.

A POSITA would have recognized implementing teachings/ suggestions from the various aspects of Chang's disclosed invention with the FIGs. 24-27 structure would have involved techniques/technologies already contemplated by the collective teachings found in Chang and consistent with a POSITA's knowledge in

the art. *Id*. Thus, for these reasons, and those additionally discussed below, a POSITA would have been motivated to implement a POSITA's state of art knowledge while combining certain teachings/suggestions from various disclosed aspects of Chang to Chang's structure as described by FIGs. 24-27 and would predictably have resulted in a structure meeting the identified challenged claims as explained below. *Id*.

In addition to Chang's discussions of features discussed in other portions of Chang's disclosure (for example, those relating to FIG. 5, 17-23, etc.) being incorporated in the teachings for Chang's FIGs. 24-27 structure, a POSITA would have been motivated to consider and implement them when forming/ configuring the FIGs. 24-27 structure (as discussed above in §§III.C, III.E-G), and would have had a reasonable expectation of success in doing so. Ex-03, ¶509.

A POSITA would have recognized and appreciated that Chang relates/references various features in its disclosure in describing the disclosed invention, which all relate to self-aligned contacts and methods of fabricating such contacts in a semiconductor structure (for example, PA-04 (Chang), FIGs. 5, 17-23, 24-27, Abstract, ¶¶27-35, 36-37, 45-49, 52, 89-90, 107, 114-117), and thus been motivated to incorporate such combined teachings to yield the predictable result of a structure as discussed above for claims 1-2. §§III.C, III.E-G; Ex-03, ¶510. *KSR*, 550 U.S. at 416.

In view of the foregoing, a POSITA would have recognized that Chang relates various features in describing the disclosed invention, which all relate to self-aligned contacts and methods of fabricating such contacts in a semiconductor structure. *See* PA-04, FIGs. 5, 17-27, Abstract, ¶¶27-37, 45-49, 52, 89-90, 107, 114-117. Thus, a POSITA would have been motivated to incorporate such combined teachings to yield the predictable result of a structure as discussed above for claims 1-2 and 4-6. Ex-03, ¶511.

a. Limitation [1.c]: at least two metal gates disposed in the first dielectric layer;

As explained for Proposed Rejection 2A, Chang discloses at least two metal gates disposed in the first dielectric layer as recited in limitation 1(c). *See* discussions above in Proposed Rejection 2A (limitation 1(d)). Chang also suggests such features and thus a POSITA would have found it obvious to configure the SRAM to use metal for gates 1441, 1443, 1446, 1449, 1546-47, 1596-97 (if not apparent from Chang's disclosures as discussed above in FIG. 5A), consistent with known transistor structures at the relevant time.

To begin, the discussions relating to the teachings of Chang concerning this feature as set forth in Proposed Rejection 2A, limitation 1(c), and those in §III.D and immediately above in this Proposed Rejection 2B, are incorporated herein.

A POSITA would have been motivated in view of Chang's disclosures above to configure Chang's gates 1441, 1443, 1446, 1449, 1546-47, 1596-97 to be metal. PA-04, ¶111. A POSITA would have been motivated to, and had a reasonable expectation of success of, implementing these features, which would have involved application of known metal gates structures that were known to a POSITA, consistent with Chang's teachings (as discussed directly above and in Proposed Rejection 2A). Ex-03, ¶¶512-514.

A POSITA would have understood that Chang explicitly discloses gates 1441 and 1449 in the SRAM of FIGs. 24-27 to be "metal" and teaches other similar gate structures in the SRAM. *Id.* Chang also teaches how to fabricate metal gates (as discussed in FIG. 5), and specifically explains how to implement metal gates to the SRAM of FIGs. 24-27 (as discussed in FIGs. 17-23), as discussed in Proposed Rejection 2A, element 1(c), and incorporated herein.

Based on such teachings and express direction, as well as state of art knowledge, a POSITA would have been motivated to simplify the fabrication process of the SRAM of FIGs. 24-27 by conforming its other gates to be also metal. Ex-03, ¶¶515-517. Mixing different gates, such as polysilicon gates would bring complexity and cost by providing gates of different materials, and would be unnecessary for the SRAM. A POSITA would have recognized the benefits and advantages of such an implementation (including e.g., simplifying the fabrication

process, conserving resources such as materials and related costs), and thus had reasons to consider such a modification, which would have been consistent with Chang's teachings of using metal gates 1441, 1449 in the SRAM of FIGs. 24-27. *Id.*

Considering and implementing such knowledge, techniques, and teachings, including those explicitly taught by Chang in FIGs. 5, 17-27, would have yielded the predictable result of the SRAM having at least two metal gates (i.e., any two of Chang's gates 1441, 1443, 1446, 1449, 1546-47, 1596-97), as claimed in limitation [1.d]. *Id.*

Thus, for the reasons here, further above for this Proposed Rejection 2B, and those in Proposed Rejection 2A, the collective teachings and suggestions in Chang disclose and/or suggest limitation 1(c) of the '747 Patent, and render obvious Claim 1, and consequently dependent claims 2 and 4-6. Ex-03, ¶518.

b. Limitation [1.g]: a plurality of second contacts disposed in the first dielectric layer that are electrically connected to one of the metal gates, wherein at least one of the first contacts directly connects at least one of the second contacts; and

As explained for Proposed Rejection 2A, Chang discloses a semiconductor structure including a plurality of second contacts disposed in the first dielectric layer that are electrically connected to one of the metal gates, wherein at least one of the first contacts directly connects at least one of the second contacts, as recited in limitation 1(g). Chang also suggests such features and thus a POSITA would have

found it obvious to configure the SRAM to include a plurality of second contacts disposed in the first dielectric layer that are electrically connected to one of the metal gates (to the extent such feature is not apparent from Chang's disclosures). Thus, for the reasons below and those above for Proposed Rejection 2A and those additional reasons in this Proposed Rejection 2B, the collective teachings and suggestions in Chang render obvious Claims 1-2 and 4-6 of the '747 Patent. Ex-03, ¶519.

As above, Chang discloses limitation 1(g) in Proposed Rejection 2A (incorporated herein). Notwithstanding those disclosures, a POSITA would have found it obvious to configure the SRAM in Chang such that the plurality of self-aligned contacts (e.g., the identified parts of self-aligned contacts 1670, 1671) electrically connect to one of the metal gates. Ex-03, ¶520.

Chang explains the need to optimize the "performance" of integrated circuits including transistors and SRAMs (PA-04, ¶6) and contemplated the use of MOSFET (e.g., including tri-gate or FinFET) transistors having known transistor device structures, such as metal gates, contacts, and the like (discussed above and below with respect to claim 6). Thus, a POSITA would have looked to design and implement the semiconductor structures disclosed by Chang (including the SRAM) with an eye toward performance (while also weighing the application and design

needs for such applications for the types of computing devices Chang contemplated integrating its disclosed semiconductor structures). Ex-03, ¶521.

In one example, a POSITA would have understood that a uniform and constant power (voltage) should be applied to the metal gates of Chang's structure along the area of the gate for optimal operation. A POSITA would have understood that the metal gates in Chang's structure (similar to known gates in such structures in the art at the time) have an associated electrical resistance. Thus, a POSITA would have recognized that electrically connecting a single self-aligned contact (e.g., self-aligned contacts 1670 or 1671) to the metal gate (e.g., gates 1446, 1597) in Chang's structure may cause different voltage to be applied at the point of contact to self-aligned contact that is different than the voltage at other locations along the metal gate. A POSITA would have appreciated that difference may be prominent at locations that are further away from the point of contact with the one self-aligned contact. A POSITA would have appreciated that such a configuration may result in a voltage drop along the gate because of the resistance. A POSITA would have thus looked for and consider ways to minimize such potential voltage drop scenarios because they may hinder the performance of the device, especially in applications and designs with longer gate lengths relative to the device and related components in the structure or relatively high gate resistance (e.g., transistor operation may be

affected at locations further from the electrical connect with the contact (e.g., self-aligned contact 1670 / 1671). Ex-03, ¶522.

In one exemplary configuration to address or mitigate such potential issues in the Chang structure, a POSITA would have been motivated to configure the structure such that multiple gate contacts (e.g., self-aligned contacts 1670 / 1671) are electrically connected to a metal gate (e.g., gate 1446, 1597, etc.) and apply essentially the same voltage to their respective contact points with the metal gate. A POSITA would have recognized the benefit of such a configuration in semiconductor structures where the gates span multiple transistors or fins in FinFET transistor applications (which are contemplated by Chang). Moreover, a POSITA would have understood and appreciated such a configuration in Chang's structure may improve the reliability of the device by providing redundancy in electrical connections with the gate from the gate contacts in the device, thus providing continued operation in the event a fault or other event causes an interruption in the voltage being applied to the metal gate by one of the connected self-aligned contacts 1670 / 1671. In addition, having multiple contacts to a given gate can also provide improved reliability, as would have been understood by a POSITA. Ex-03, ¶523.

Chang's teachings and suggestions (which, explained above for limitation 1(g) in Proposed Rejection 2A) provides configurations that would promote and provide such electrical connection between multiple gate contact vias and one of the

metal gates (e.g., gates 1446 / 1597). *See* discussions for limitation 1(b) in Proposed Rejection 2A. Such disclosures and a POSITA's knowledge and experience at the relevant time, would have motivated a POSITA to configure the SRAM to include a plurality of self-aligned contacts 1670 / 1671 ("second contacts") to be "electrically connected to one of the" metal gates 1446 / 1597 ("one of the metal gates"), like that recited in limitation 1(g) of the '747 Patent. Ex-03, ¶524.

Thus, in light of the teachings and suggestions in Chang (including Chang's recognition of the desire in the art to improve the performance of semiconductor devices), and a POSITA's state of art knowledge and experience, a POSITA would have been motivated and found obvious to configure Chang's structure to include multiple contacts that electrically connect to a respective metal gate (e.g., gates 1446, 1597) in order to support high performance operation for Chang's semiconductor structure. A POSITA would have recognized and appreciated that implementing such features and configuration in Chang's SRAM would have predictably resulted in the structure leveraging existing elements (e.g., self-aligned contacts 1670 / 1671, metal gates, and interconnection points between them, etc.) where a plurality of "second contacts [are] electrically connected to at least one of the metal gates as recited in limitation 1(g). Ex-03, ¶525.

A POSITA would have appreciated that configuring Chang's SRAM in such a manner would have been an obvious combination of known semiconductor

elements that were configured in accordance with known semiconductor fabrication techniques and process that would have foreseeably led to the Chang's structure including electrical connection between multiple gate contact vias in a manner familiar to Chang's disclosed structures and related fabrication processes. Thus, a POSITA would have understood such a configuration as applied to Chang's structure as predictable variation to improve Chang's semiconductor structure in a manner known in the art. Ex-03, ¶526.

Based on their experience and knowledge in context of the teachings in Chang, a POSITA would have also recognized and appreciated, that implementing such features and configuration in Chang's structure would have included applying known semiconductor device manufacturing and design techniques and related structural elements, which Chang's already contemplates or suggests consistent with that understood by a POSITA at the time. Thus, a POSITA would have reasonably expected to succeed at implementing the configuration in the SRAM of Chang. Ex-03, ¶527.

Accordingly, it would have been obvious to configure the SRAM to include a plurality of second contacts disposed in the first dielectric layer that are electrically connected to one of the metal gates, wherein at least one of the first contacts directly connects at least one of the second contacts, as recited in Claim limitation 1(g) of the '747 Patent. Thus, for the reasons provided here, and those above for limitation

1(g) in Proposed Rejection 2A, the collective teachings and suggestions in Chang render obvious Claim 1 of the '747 Patent, and likewise its dependent claims 2 and 4-6, for reasons explained above and below in this Proposed Rejection 2B and further above for Proposed Rejection 2A (including the reasons and analysis concerning other claim limitations). Ex-03, ¶528.

c. Claim 2: The semiconductor device of claim 1, further comprising a second dielectric layer disposed on the first dielectric layer.

As explained for Proposed Rejection 2A, Chang discloses the semiconductor device of claim 1, further comprising a second dielectric layer disposed on the first dielectric layer, as recited in claim 2. Ex-03, ¶¶529-530.

Where, for example, "the semiconductor device of claim 1" is the SRAM described above in this Proposed Rejection 2B, Chang discloses a second dielectric layer disposed on the first dielectric layer, as recited in claim 2 for the same reasons discussed in Proposed Rejection 2A. Any modification to the SRAM discussed in Proposed Rejection 2B, claim 1 (to the extent any modification is deemed necessary) would not affect Chang's disclosure of claim 2. For example, a POSITA would have understood that no proposed or perceived modification to the SRAM discussed in Proposed Rejection 2B, claim 1 would change or otherwise affect the fact that Chang's ILD layer 1510 is disposed on layer 1503 even in the structure discussed here for Proposed Rejection 2B. *Id.*

d. Claim 4: The semiconductor device of claim 2, wherein the first contacts disposed in the first dielectric layer and in the second dielectric layer and each first contact is a monolithically formed structure.

Claim 5: The semiconductor device of claim 2, wherein the second contacts disposed in the first dielectric layer and in the second dielectric layer and each second contact is a monolithically formed structure.

Regarding **claim 5**, as discussed above (§VI.B.1(a)(8) incorporated herein), Chang teaches **a plurality of second contacts** formed by parts of "each of the respective self-aligned contacts 1670 and 1671" (**disposed in the first dielectric layer**). Chang further explains that "the gate contact may be formed at the same time the metal one layer is formed." *See* PA-04 (Chang), ¶105.

The metal one layer is within the ILD 1510 layer, meaning that the gate contact can be formed by a deposition step that deposits the contact material into an opening extending from the ILD 1510 to the gate. Thus, the second contact can be disposed in the first dielectric layer (ILD 1503) and the ILD 1510 (**second dielectric layer**). *See* PA-04 (Chang), ¶¶112-13. This means that the identified **second contacts** are **a monolithically formed structure**, as claimed. *See* PA-04 (Chang), ¶¶105, 112-13, 100-06, FIG. 27. Ex-03, ¶¶531-536.

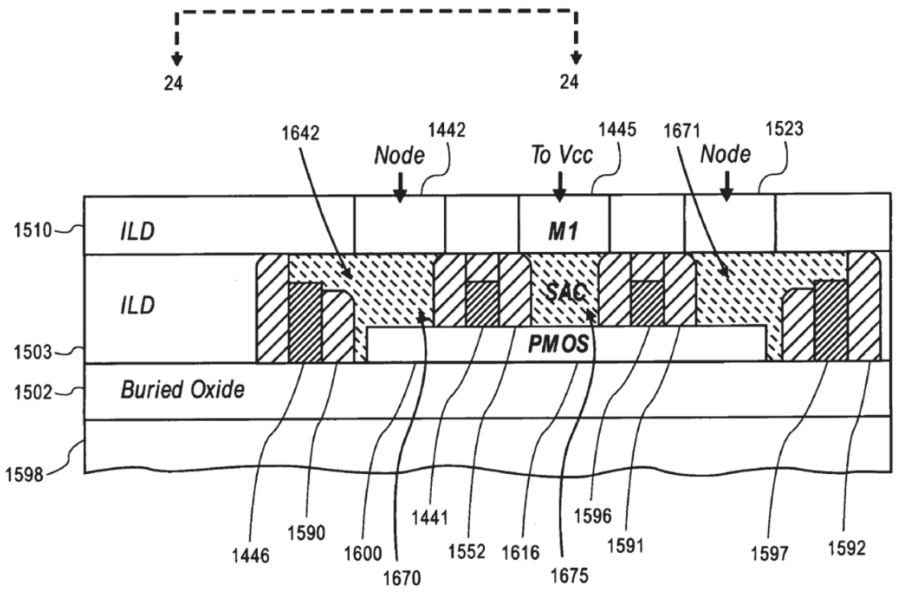


FIG. 27

PA-04 (Chang), FIG. 27.

Notwithstanding Chang's disclosure, a POSITA would have been motivated to form Chang's structure's contacts (such as self-aligned contacts 1670, 1671) during this single deposition. Ex-03, ¶533. Chang recognizes that such a single deposition approach advantageously "result[s] in a higher aspect ratio for etch and metal deposition." *See* PA-04 (Chang), ¶105. A higher aspect ratio (i.e., height divided by width) contact means the density is increased (e.g., contact is achieved with a narrower width), and thus less chip area is required for a given structure/device, and as a result, more structures/devices may be provided on a given chip area. *See* Ex-09 (Wolf), 600; Ex-15 (Xiao), 463-64.

Thus, a POSITA would have been motivated to implement such features resulting in Chang's structure to include each second contact being a monolithically formed structure, as claimed. *Id*.; Ex-03, ¶534.

A POSITA would have a reasonable expectation of success of implementing such a modification, which would have involved application of known deposition techniques such as metal damascene, consistent with Chang's teachings. *See* PA-04 (Chang), ¶97. For example, Chang teaches a damascene technique for its metal one layer formation, which was conventionally known to be able to effectively accommodate different vertical geometries of trenches and vias (for example, using a dual-damascene process. *See* PA-04 (Chang), ¶97; PA-03 (Huang), ¶17; Ex-11 (Tomimatsu), ¶89; Ex-10 (May), 55-56; Ex-09 (Wolf), 674-76 (cited for state of art teachings/knowledge here). A POSITA would have understood that such modification would have predictably yielded Chang's FIGs. 24-27 structure including the second contacts disposed in the first dielectric layer and in the second dielectric layer and each second contact is a monolithically formed structure as claimed in claim 5. Ex-03, ¶535.

As to **claim 4**, as discussed above (§VI.B.1(a)(7) incorporated herein), Chang teaches **a plurality of first contacts** formed by parts of the self-aligned contacts 1670, 1671, and 1675 that reside in ILD 1503 (**disposed in the first dielectric layer**). A POSITA would have understood that forming the gate contacts extending

into the second dielectric layer, as Chang teaches (*see* above; PA-04 (Chang), ¶105), a POSITA would have been motivated to also form source/drain contacts extending into the second dielectric layer in the modified Chang structure discussed above because doing so would allow a single deposition process to be used to form the gate contacts and source/drain contacts simultaneously. Accordingly, the processes for forming the source/drain contacts and gate contacts would therefore share same lithography process, etching processes, and/or deposition processes, which would have reduced process complexity and fabrication cost, and would have predictably led to the above modifications to structure discussed above. *Id*.; Ex-03, ¶536.

e. Claim 6: The semiconductor device of claim 1, further comprising at least one fin structure disposed on the substrate.

As explained for Proposed Rejection 2A, Chang discloses a semiconductor structure including at least one fin structure disposed on the substrate. Chang also suggests such features and thus a POSITA would have found it obvious in configure the SRAM to include at least one fin structure (to the extent such feature is not apparent from Chang's disclosures) consistent with known transistor structures at the relevant time. Thus, for the reasons below and those provided above for Proposed Rejection 2A (incorporated herein), and those additional reasons in this Proposed Rejection 2B, the collective teachings and suggestions in Chang render obvious Claim 6 of the '747 Patent. Ex-03, ¶¶537-551.

Consistent with discussions above for claim 6 in Proposed Rejection 2A and further above in this proposed rejection, a POSITA would have considered the collective teachings and suggestions in Chang when configuring and implementing the SRAM for application to the various implementations contemplated by Chang. Ex-03, ¶538.

In addition to Chang's SRAM disclosing "at least one fin structure disposed on the substrate" as recited in claim 6, a POSITA would have been motivated to implement the SRAM structure to include at least one such fin structure in view of Chang's FIG. 5 teachings, which (as in FIGs. 24-27) shows a "cross section of...a transistor structure." PA-04, ¶¶45-48; Ex-03, ¶539.

Chang describes its semiconductor structures in context of non-planar devices that include fin structures. PA-04, ¶¶2-5, FIGs. 1-3 (discussing and showing tri-gate transistors that were known to include fins), ¶6 ("A device such as a static random-access memory ("SRAM") uses numerous trigate transistors."), ¶45 ("FIGS. 5 through 10 illustrate process steps for forming self-aligned contacts for transistors. The process can be used for various types of transistors. The process is especially beneficial for transistors with an Rext problem. Such transistors can include transistors with a thin diffusion, such as trigate transistors, and even bulk devices on or beyond the 65 nanometer node."), ¶48 ("The transistor structure 116 includes diffusion layer 104 (also called diffusion body 104 or fin 104); gates 106 and 108;

and spacers 110, 111, 112, and 113. The diffusion layer 104 includes drain region 135 and source regions 130 and 131."). Ex-03, ¶¶540-541.

For example, like the SRAM of Figures 24-27, Chang's teachings relating to FIG. 5 disclose a "transistor structure" with a "metal gate" and a "diffusion layer." PA-04, ¶48. Chang also states in these teachings that the "diffusion layer" is "also called" a "fin." PA-04, ¶48.

In light of the collective teachings and suggestions in Chang, it would have been obvious to configure SRAM in context of a multi-gate or FinFET transistor device including at least one fin structure disposed on the substrate of the structure. A POSITA would have been motivated to implement such a configuration to provide a transistor applicable for the types of devices contemplated by Chang, such as SRAMs (see, for example, ¶6). Indeed, Chang claims a (*see* claim 19, 22) "a diffusion layer of the transistor, wherein the diffusion layer includes a source region and a drain region" "wherein the transistor is a trigate transistor", consistent with multi-gate transistors, such as a FinFET, having a fin structure. Thus, a POSITA reviewing the collective teachings in Chang would have had reasons to consider and configure the SRAM to include a fin structure, which were known features of the multi-gate, tri-gate, or FinFET transistor devices contemplated by Chang. Ex-03, ¶542.

Indeed, Chang teaches a "transistor structure" that has a "metal gate" and "diffusion layer," which is "also called" a "fin" in its FIG. 5 explanation. PA-04, ¶48. Given the substantially similar disclosure and teachings, a POSITA would have been motivated to implement Chang's SRAM of FIG. 27 with at least one fin structure disposed on the substrate, as recited in Claim 6. A POSITA would have a reasonable expectation of success of implementing such an implementation. Further, consistent with Chang's teachings, such an implementation would have involved application of known transistor structures/techniques. Ex-03, ¶543.

In addition, Chang states that the "invention can be used with other types of transistors with metal gates, such as trigate transistors." PA-04, ¶¶114, 2-6, 13-15, FIGs. 1-3. Chang explains that "[t]rigate transistors...typically have small geometries. For trigate transistors, the diffusion regions and the gates are typically quite thin" and that "[a] device such as a static random-access memory ('SRAM') uses numerous trigate transistors." PA-04, ¶¶ 2, 6; Ex-03, ¶544.

Tri-gate FETs were prevalent before the relevant time and their function and structure was conventionally understood and mature. Tri-gate FETs conventionally included fin structures, and had known benefits to a POSITA, such as those described above by Chang. In fact, a POSITA would have been knowledgeable of the use and implementation of planar and fin-shaped FETs, and the similarities between them (e.g., channel, source/drain regions, gates, etc.). A number of state of

the art references provide disclosures consistent with a POSITA's knowledge at the time. *See e.g.*, Ex-18 (Sze), 433-34, 438, FIGs. 3, 6; Ex-07 (Neamen), xxiii, 403-405, FIGs. 0.5, 10.34, 10.35; Ex-09 (Wolf), 3, 6; Ex-15 (Xiao), 72-74, 351, 370-371, FIGs. 3.20, 9.31, 10.2; Ex-28 (Lin), 7:54-60, 10:17-23, 12:51-56, 16:35-41; Ex-35 (Chi, 2012), 1; Ex-29 (Ranade), ¶¶ 25, 44; Ex-30 (Hu), Abstract, 2:11-14 (FinFETs are "an extension of conventional planar MOSFET technology"), 5:37-40 (FinFETs fabrication "is compatible with conventional planar MOSFET fabrication techniques"); Ex-31 (Doyle, 2003), 133 (a FinFET "very much resembles [a] bulk transistor from the processing point-of-view"); Ex-32 (Simonelli), ¶¶1, 3-4, 44-45; Ex-33 (Chau), 2:38-41, 5:3-26, 6:35-50; Ex-34 (Chang), 2:61-3:3; Ex-03, ¶545.

A POSITA was thus well aware of, and had experience with, FinFET type transistor devices and related structures consistent with those contemplated by Chang. Indeed, FinFET devices were well known to include fin structures, like that described by Chang (*see* ¶48). *See e.g.*, Ex-15 (Xiao), 72-74, 351; Ex-03, ¶¶546-547.

A POSITA would have appreciated and recognized the benefits of implementing the SRAM of Chang as a non-planar structure with a multi-gate or FinFET transistor, such as scaling to minimize the footprint of the integrated circuit implementing such transistors, consistent with that contemplated by Chang. *See* PA-04, ¶¶2-5; *see also* Ex-15 (Xiao), FIG. 15.1, 650-51 (describing features consistent

with a POSITA's state of art knowledge at the relevant time such as the known use of "a trigate, [where] fabs can use the same lithographic technology to reduce transistor dimensions while maintaining the same performance, or to improve device performance without increasing device density" and where "IC manufacturers can further improve device performance by making the fin taller" and that "a finFET is easier to build than a trigate. Intel's 22-nm IC chips are built with trigate devices").

In light of such knowledge and experience, and in context of Chang's teachings and suggestions, a POSITA would have been motivated to configure the SRAM with a fin structure disposed on top of the substrate, consistent with known Fin-FET and tri-gate transistor semiconductor structure configurations at the relevant time. Ex-03, ¶548.

A POSITA's knowledge and experience would have led them to implement such fin structure features in the SRAM with a reasonable expectation of success that the semiconductor structure would provide functional transistor operations consistent with the application of the structure in the various types of devices (e.g., SRAMs) that Chang contemplates. For instance, a POSITA would have recognized that implementing such features would have involved applying known semiconductor fabrication processes and structural elements (e.g., FinFETs, tri-gate transistors and related fabrication processes) that were within the capabilities and knowledge of a POSITA at the relevant time. Indeed, Chang expressly discloses

semiconductor structures with fin structures (PA-05, FIG. 5), thus expressly guiding a POSITA to integrate the same with the SRAM. Also, a POSITA would have considered the design needs for such applications, relevant market demands, and related factors and thus found implementing Chang's structure as a FinFET or tri-gate type device. Ex-03, ¶549.

Accordingly, a POSITA would have been motivated to make such an implementation, and would have had reasonable expectation of success in doing so. Consistent with the teachings of Chang, this implementation would have involved the application of known transistor structures that were well within the capabilities and knowledge of a POSITA. A POSITA would have understood upon considering and implementing such knowledge, known techniques, and teachings in the prior art references, such a modification would have yielded the foreseeable result of the FIG. 27 structure having at least one fin structure disposed on the substrate, like that recited in Claim 6. Ex-03, ¶550.

In sum, it would have been obvious to configure the SRAM to include at least one fin structure disposed on the substrate of the structure, as recited in Claim 6 of the '747 Patent. Thus, for the reasons here, further above for this Proposed Rejection 2B, and those for Claim 6 in Proposed Rejection 2A, the collective teachings and suggestions in Chang render obvious Claim 6 of the '747 Patent. Ex-03, ¶551.

3. Proposed Rejection 2C: Claims 1-7 Are Obvious Over *Chang* and *Sell*

Proposed Rejection 2C presents how the combined teachings and suggestions of Chang (as discussed above in both Proposed Rejections 2A and 2B) and Sell in context of a POSITA's state of art knowledge discloses and/or suggests, and renders obvious, certain features recited in the claim limitations addressed below. Thus, discussions regarding the teachings and suggestions in Chang in both Proposed Rejections 2A and 2B are relied upon herein to support findings of obviousness of other claim limitations in the Claims. Ex-03, ¶¶552-633.

a. Limitations [1.pre]-[1.c] and [1.e]-[1.h]

Chang discloses/suggests these limitations. *See* §§VI.B.1(a)(1)-(4), (a)(6)-(9) above; *see also* Ex-03, ¶553.

b. Limitation [1.d]: a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface;

Proposed Rejection 2A discuss how Chang discloses each of claim limitation 1(d) ("a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface"). Proposed Rejection 2B discusses how the collective teachings and suggestions in Chang further renders obvious Claims 1-2 and 4-6. The discussions in Proposed Rejections 2A and 2B are incorporated herein to support Proposed Rejection 2C. In addition to those opinions and analysis, for the reasons below and above in this Proposed Rejection 2C, and reasons above in Proposed

Rejection 2B, the combined teachings and suggestions in Chang and Sell disclose or suggest, and render obvious claim limitation 1(d).[31] Ex-03, ¶554.

As discussed for Proposed Rejection 2B the teachings and suggestions in Chang relating to the implementation of a spacer disposed on two sides of the metal gate, are incorporated herein. In context of the disclosures in Chang that are discussed above in Proposed Rejections 2A-2B, a POSITA would have been aware of the use and benefits of providing spacers on the sidewalls of a metal gate in a semiconductor structure (e.g., provide stability, alignment, etc.) and thus had reasons to consider guidance in the art concerning the formation and implementation of spacers when contemplating the Chang structure. In doing so, a POSITA would have considered the teachings and suggestions in Sell. Ex-03, ¶¶555-562.

[31] A POSITA would have found it obvious to implement the spacer with a truncated top surface feature in Chang's structure does not mean Chang does not disclose such a feature as claimed in Claim 1— Chang does disclose the claimed spacer for reasons discussed for limitation 1(d) in Proposed Rejection 2A. Rather, consistent with discussion for Proposed Rejection 2B (further supported by the teachings and suggestions of Sell in context of Chang's teachings), a POSITA would have found it obvious to form and implement spacers with a "truncated top surface" notwithstanding the disclosures in Chang addressed above for Proposed Rejection 2A.

Sell discloses "methods and associated structures of forming a microelectronic structure." Sell, 1:50-51, 1:50-64. *See also id.*, Abstract, 1:50-2:9. FIGs. 1a-1g. Sell discloses that the "[m]ethods of the present invention are depicted in FIGS. 1 a-1 g" where "transistor structure 100 comprising a substrate 102, and a gate 104, which may comprise a metal gate in some embodiments, and may comprise such metal gate materials as hafnium, zirconium, titanium, tantalum, or aluminum, or combinations thereof, for example. The gate 104 may comprise a top surface 105." *Id.*, 1:65-2:9. Further, "transistor structure 100 may further comprise a spacer material 106, that may be adjacent and in direct contact with the gate 104." *Id.*, 2:10-22. The spacer 106 has a planar top. PA-06, FIG. 1a (below).

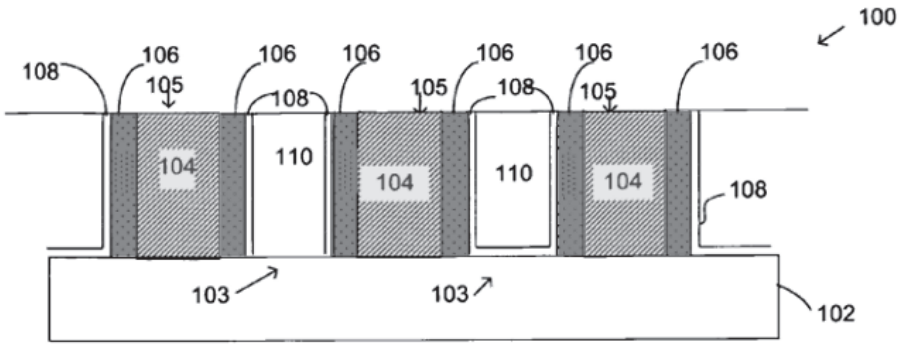


FIG. 1a

PA-06, FIG. 1a. Sell explains that after a sacrificial stopping layer 112 is formed on the top surface 105 of gate 104, and a resist layer 114 formed on the stopping layer 112 (*id.*, 2:23-34), an etching process is performed to form openings 116. *See also* PA-06, 2:35-49; *id.*, Fig. 1b (below).

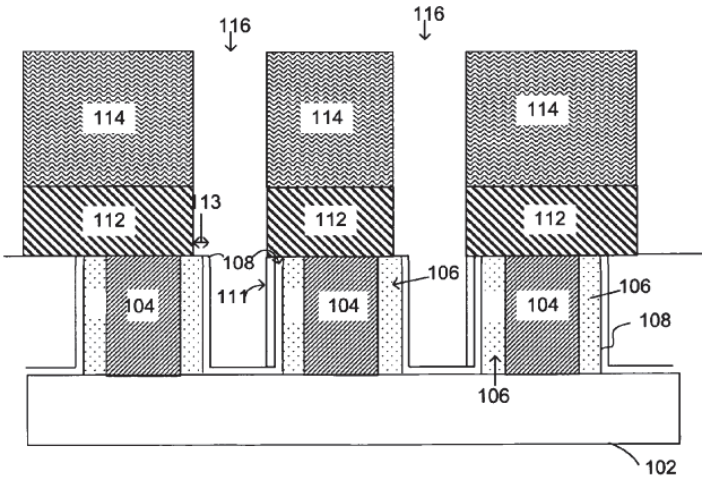


FIG. 1b

Sell discloses the etch stop layer 108 may be removed from the source/drain region 103 of the substrate leaving a source/drain contact area 107 exposed. *Id.*, 2:62-66, FIG. 1c (below). *See also*, *id.*, 2:50-61.

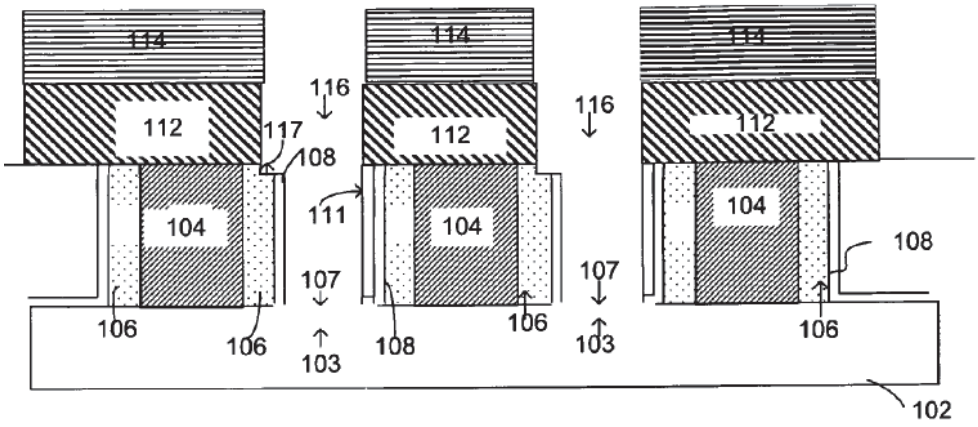


FIG. 1c

See also, PA-06, 2:50-61, ("[a] depth 117 into the exposed portion 113 of the spacer material 106 may be formed by the nesl 108 etch and/or the ILD etch due to the misregistration of the resist layer 114" and resist layer 114 may then be removed and a salicide 118 may be formed on/in the source/drain contact area 107 using any

suitable salicide process as are known in the art, such as but not limited to a nickel salicide process and/or other such salicide process (FIG. 1 d).")

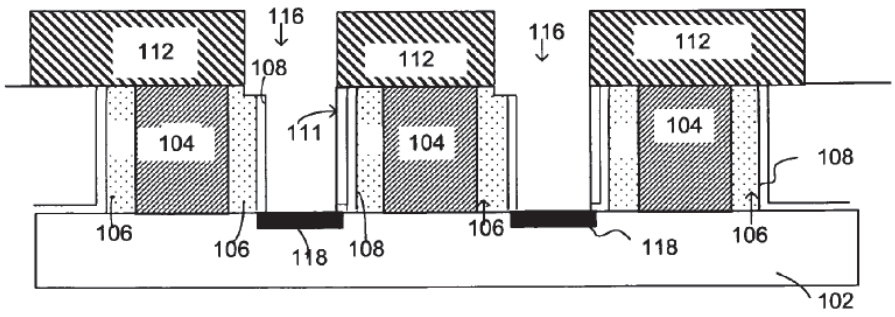


FIG. 1d

Next a first contact metal 120 is formed on the salicide 118. *Id.*, 3:17-23, FIG. 1e (below).

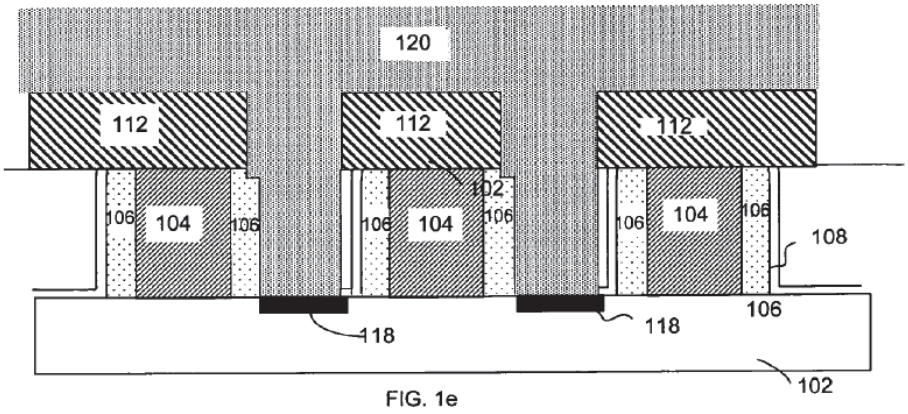


FIG. 1e

Sell then performs a planarization process on the contact metal and other layers that makes the spacer 106 and etch stop layer 108 shorter by removing a part. *Id.*, 3:23-30 ("A polishing process 123 may subsequently be performed, such as a chemical mechanical polishing (CMP) process, for example, to remove the first contact metal 120 (FIG. 1f) and the stopping layer 112."), FIG. 1e (below).

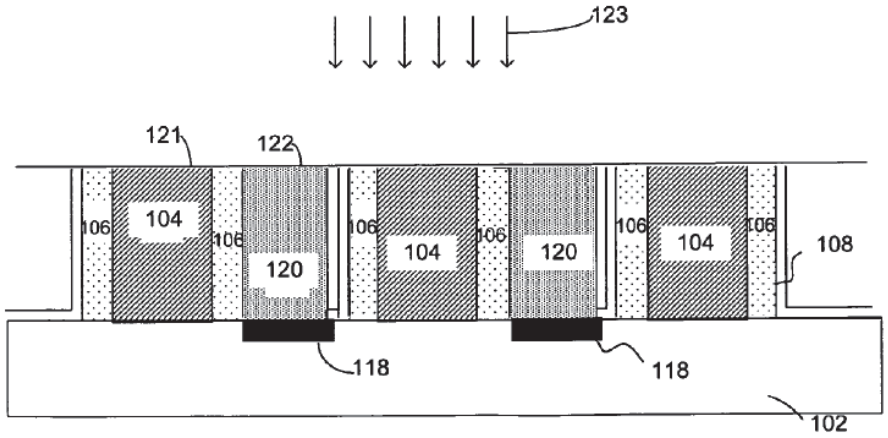


FIG. 1f

Sell explains this results in planarized top surfaces. *See* PA-06 (Sell), 3:31-43. The planarized top surface of gate 104 is co-planar with spacer 106, and thus a POSITA would recognized that Sell's planarization process results in the spacers 106 each having a planar top surface by making the spacer 106 shorter by removing a part (during a planarization process). Ex-03, ¶561.

Afterwards a stacked contact structure is formed with contact metal 128 and contact metal 120 to the source/drain region 118 of the device. *Id.*, 3:44-4:26, Fig. 1g (below).

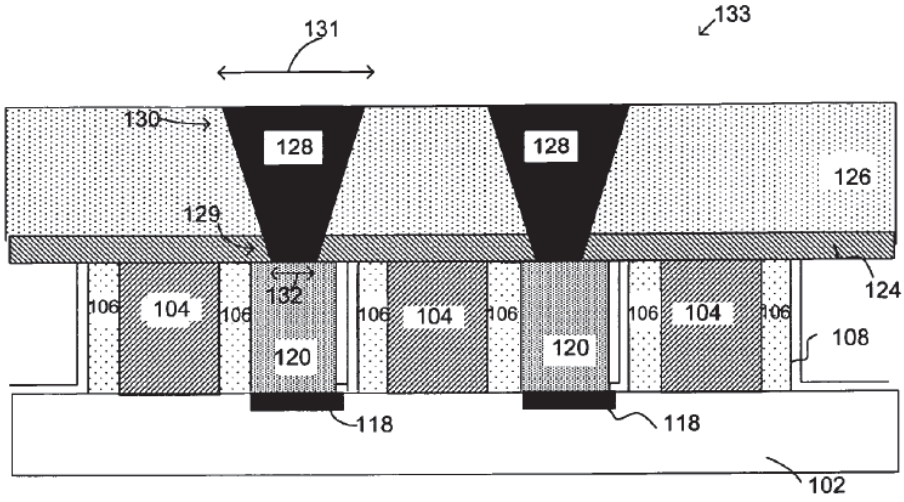


FIG. 1g

Sell therefore discloses a semiconductor structure including a spacer disposed on two sides of a metal gate where the spacer was made shorter by removing a part (including during a planarization process) and having a planar top surface, consistent with Interpretations 1-3. *See* §II.D.1; Ex-03, ¶563.

Sell is analogous art. For example, a POSITA would have understood that Sell's semiconductor structure can include "transistor structure" (PA-06, 2:10-22, 3:64-4:2, 4:19-26)), is in the same field (e.g., semiconductor device transistor structures with contacts) and reasonably pertinent to a problem the '747 Patent purports to address (e.g., transistor structure contact fabrication). *See e.g.*, PA-06, 1:5-13, 1:29-2:23, 3:17-4:18; Ex-01, 1:9-2:9, 2:18-20, 2:39-42, 3:1-25, 5:31-6:37. Accordingly, a POSITA would have had reasons to consider the teachings and suggestions in Sell when contemplating the semiconductor structure of Chang's structure. Upon considering Sell, a POSITA would have recognized and appreciated

the teachings and guidance concerning the implementation of spacers and thus been motivated to modify or configure Chang's spacers used in the structure in light of such disclosures. Ex-03, ¶564.

Namely, a POSITA would have been led by Chang's teachings, (including the description of spacers and the processes involved with their fabrication in context of the resulting structure in Chang, as discussed for limitation1(d) in Proposed Rejection 2A) in view of the teachings of Sell to provide spacers in the structure by performing known planarization processes (e.g., CMP) on the spacers (after being disposed on the sides of the metal gate). *See e.g.,* PA-04 (Chang), FIGs. 17-23, 24-27, ¶¶52, 89 94-95. Such processes would remove material and provide a planar top surface like the top surface of the spacers taught by Sell. Such a modification and implementing would have predicably resulted in the Chang structure including a spacer disposed on two sides of a metal gate that was made shorter by removing a part of the spacer during a planarization process (e.g., CMP). Such a spacer would have a planar top surface like that shown by Sell). PA-06 (Sell), 3:5-30; Ex-03, ¶565.

Sell's teachings are consistent with the use of a POSITA's state of art knowledge at the relevant time of the use and implementation of spacers that were subject to planarization process during semiconductor device fabrication, that results in the spacer being made shorter by removing a part (including during a planarization

process) and ultimately having a planar top surface in the resulting structure. *See e.g.*, PA-05 (Chi), 14:25-15:9, FIGs. 3C-3E, 15:41-16:60, FIG. 3J, FIG. 3I (describing state of the art spacer features consistent with that known by a POSITA at the time; including, e.g., spacers 32 that have been made shorter by removing a part (including during a planarization process). Ex-03, ¶566.

Guided by the teachings in Sell in context of Chang's teachings and a POSITA's state of art knowledge at the relevant time, a POSITA would have found it obvious to form the spacers in Chang's structure by removing material from the spacers' top surface (after the spacers were formed) by known planarization processes (e.g., CMP) in order to provide a planarized top surface spacer structure like that shown in the resulting structure of Chang. Such an implementation would have predictably resulted in spacers having a truncated top surface consistent with Interpretation 1 (planar top surface), and Interpretations 2 and 3 (made shorter by removing a part (during a planarization process). *See* §II.D.1; Ex-03, ¶567.

A POSITA would thus have found it obvious to implement spacers having a truncated top surface consistent with the teachings of Sell in the structure of Chang discussed above for Claim 1 in Proposed Rejection 2B. For example, a POSITA would have recognized and understood that sidewall spacers were well-known and used in semiconductor structures like Chang's structures (indeed Chang discloses spacers (*see* Proposed Rejection 2A (limitation 1(d)), and likewise recognized

advantages in planarizing such structures to provide a flat surface or a co-planar surface with other layers/material upon which other material or layers can be formed and consequently further subsequent processing, including photolithography, to be more reliably performed. The teachings of Sell are consistent with known uses and formations of spacers, and the subsequent planarization processes to provide a planar top surface in semiconductor structures consistent with that described by Chang. In performing such planarization (like that described by Sell), a POSITA would have understood that the spacer is made shorter by removing a part (during a planarization process) resulting in a spacer with a planar top surface in the resulting structure similar to that described by Sell, (which includes structures with planarized top surfaces formed via CMP processes). PA-06 (Sell), 3:17-30, FIG. 1f; Ex-03, ¶568.

A POSITA would have had a reasonable expectation of success in implementing the above modification/configuration to the spacers disposed on the sides of the metal gate in Chang's structure. A POSITA would have appreciated and been led by Sell's teachings relating to known fabrication processes and semiconductor device structures, including spacers on two sides of metal gate structures where the spacers having a planar top surface similar to that described Sell. Moreover, a POSITA would have reasonably expected success in implementing such a modification/configuration because providing a spacer with a planar top surface would have involved nothing more than applying a standard semiconductor

manufacturing process (e.g., deposition, CMP, etc. similar to that taught by Sell) for providing the spacer on the sides of metal gates, where the spacer (once formed) was planarized to provide a planar top surface consistent with that known in the art and disclosed by Sell. PA-06, 3:17-30, FIGs. 1e-1f. A POSITA would have leveraged their state of art knowledge and experience in considering the design needs and the market demands for the applications of the semiconductor structure as contemplated by Chang, and thus would have been motivated to configure and design fabrication processes to successful provide such a spacer in the Chang structure with a "truncated top surface" (as interpreted under Interpretations 1-3, *see* §II.D.1). Ex-03, ¶569; *KSR*, 550 U.S. at 416.

For the reasons above, Chang in view of Sell renders obvious claim 1 and thus the claim is invalid in view of that prior art combination. Ex-03, ¶570.

c. Claim 2: The semiconductor device of claim 1, further comprising a second dielectric layer disposed on the first dielectric layer.

As explained for Proposed Rejection 2A, Chang discloses the semiconductor device of claim 1, further comprising a second dielectric layer disposed on the first dielectric layer, as recited in claim 2. Ex-03, ¶¶571-573.

Where, for example, "the semiconductor device of claim 1" is the SRAM described above in this Proposed Rejection 2B, Chang discloses a second dielectric layer disposed on the first dielectric layer, as recited in claim 2 for the same reasons

discussed in Proposed Rejection 2A. Any modification to the SRAM discussed in Proposed Rejection 2B, Claim 1 (to the extent any modification is deemed necessary) would not affect Chang's disclosure of Claim 2. For example, a POSITA would have understood that no proposed or perceived modification to the SRAM discussed in Proposed Rejection 2B, claim 1 would change or otherwise affect the fact that Chang's ILD layer 1510 is disposed on layer 1503 even in the structure discussed here for Proposed Rejection 2B. Ex-03, ¶572.

Thus, for reasons similar to those discussed above for Proposed Rejection 2A (Claims 2 and 6) and those for Proposed Rejection 2B (Claims 1-2 and 4-6), Chang in view of Sell discloses and/or suggests, and renders obvious, Claim 2 of the '747 Patent and thus the claim is invalid under the combination. Ex-03, ¶573.

d. Claim 3: The semiconductor device of claim 2, further comprising an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface.

Proposed Rejection 2A discusses how Chang discloses the limitations in Claims 1-2 and 6. Proposed Rejection 2B discusses how the collective teachings and suggestions in Chang further renders obvious Claims 1-2 and 4-6. Those discussions are incorporated herein to support Proposed Rejection 2C. In addition to reasoning and analysis provided in Proposed Rejection2A (incorporated herein), for the reasons below and above in this Proposed Rejection 2C, the combined teachings

and suggestions in Chang and Sell disclose or suggest and render obvious Claim 3. Ex-03, ¶¶574-603.

In particular, a POSITA would have found it obvious to implement an etching stop layer having a truncated top surface and disposed on two sides of the metal gate in the Chang structure.

Chang's teachings above for Claim 1 in Proposed Rejection 2A are incorporated herein. For example, as discussed for Claim 1, Chang discloses metal gates in the structure (e.g., gates 1441, 1443, 1446, 1596, 1597). PA-04 (Chang), FIGS. 24, 27. Chang's gates include a "silicon nitride protection layer." *See* PA-04, ¶114. A POSITA would have understood such a layer as an "etch-stop layer for self-aligned contact application." *See* Ex-15 (Xiao), 164-65, FIG. 5.64. Such teachings in context of Chang's collective teachings would have led a POSITA to consider options for protecting material and structures during fabrication of its semiconductor device. Moreover, a POSITA was familiar with and aware that contact etching stop layers (CESLs) and similar etching stop layers were commonly used and known semiconductor structural elements used in the fabrication of semiconductor devices, including those described by Chang. Accordingly, a POSITA would have had reasons to consider teachings from the prior art. Sell is an example of such teachings that would have guided a POSITA at the relevant time. Ex-03, ¶¶575-581.

Sell discloses that the "[m]ethods of the present invention are depicted in FIGS. 1 a-1 g" where "transistor structure 100 comprising a substrate 102, and a gate 104, which may comprise a metal gate in some embodiments, and may comprise such metal gate materials as hafnium, zirconium, titanium, tantalum, or aluminum, or combinations thereof, for example. The gate 104 may comprise a top surface 105." PA-06 (Sell), 1:65-2:9. Further, "transistor structure 100 may further comprise a spacer material 106, that may be adjacent and in direct contact with the gate 104." *Id.*, 2:10-22. Further, Sell explains the "transistor structure 100 may further comprise **a nitride etch stop layer (nesl) 108**…**[t]he nesl 108 may serve as an etch stop layer**." *Id.* The etch stop layer 108 and spacer 106 each has a planar top. PA-06, FIG. 1a (below).

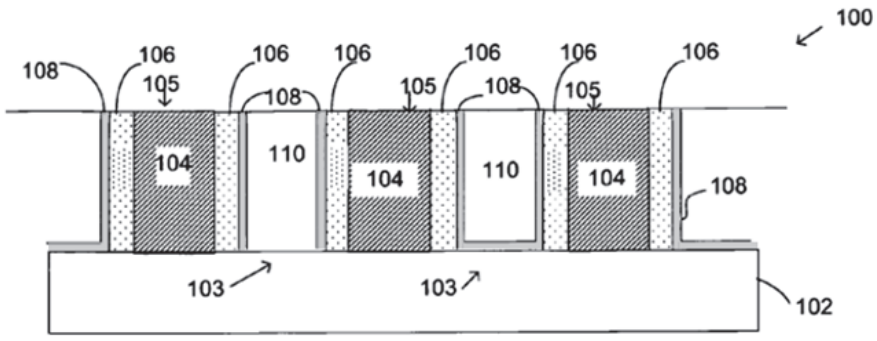


FIG. 1a

PA-06, FIG. 1a. Sell explains that after a sacrificial stopping layer 112 is formed on the top surface 105 of gate 104, and a resist layer 114 formed on the stopping layer

112 (*id.*, 2:23-34), an etching process is performed to form openings 116 leaving the etch stop layer 108 intact. PA-06 (Sell), 2:35-49. *See id.*, Fig. 1b (below).

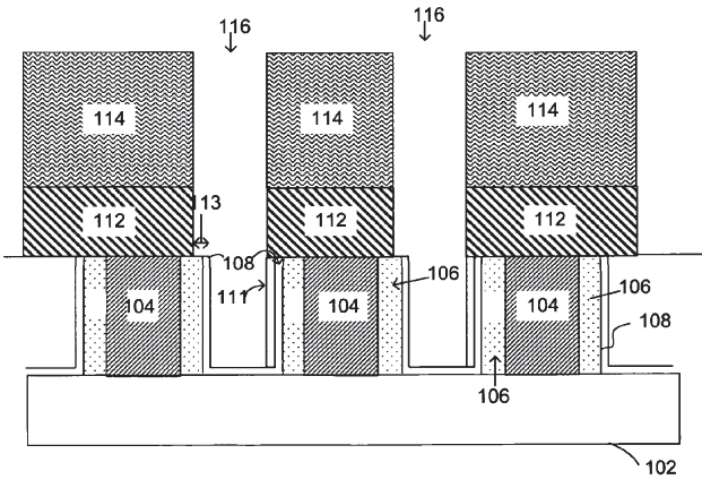


FIG. 1b

Sell discloses the etch stop layer 108 may be removed from the source/drain region 103 of the substrate leaving a source/drain contact area 107 exposed. *Id.*, 2:62-66, FIG. 1c (below). *See also*, *id.*, 2:50-61.

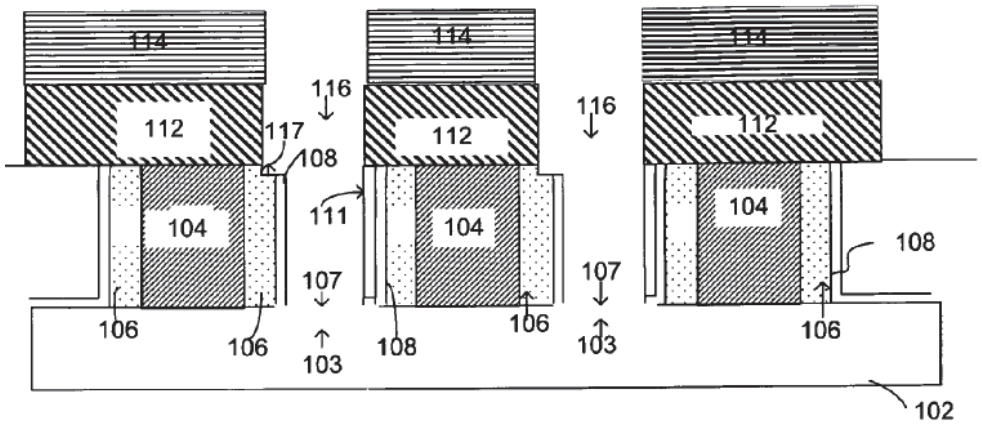


FIG. 1c

See also, PA-06 (Sell), 2:50-61, ("[a] depth 117 into the exposed portion 113 of the spacer material 106 may be formed by the nesl 108 etch and/or the ILD etch due to

the misregistration of the resist layer 114" and resist layer 114 may then be removed and a salicide 118 may be formed on/in the source/drain contact area 107 using any suitable salicide process as are known in the art, such as but not limited to a nickel salicide process and/or other such salicide process (FIG. 1 d).")

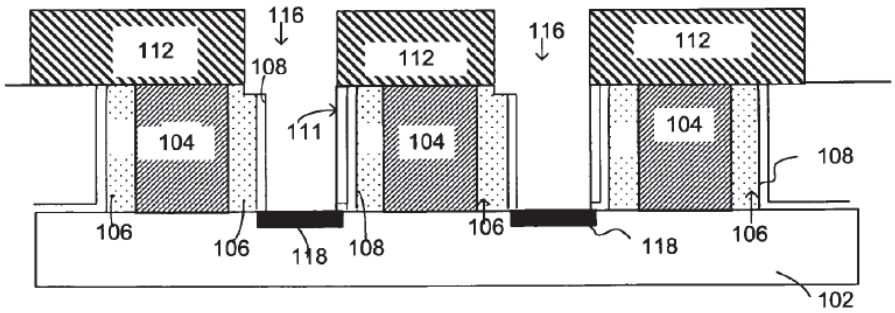


FIG. 1d

Next a first contact metal 120 is formed on the salicide 118. *Id.* at 3:17-23, FIG. 1e (below).

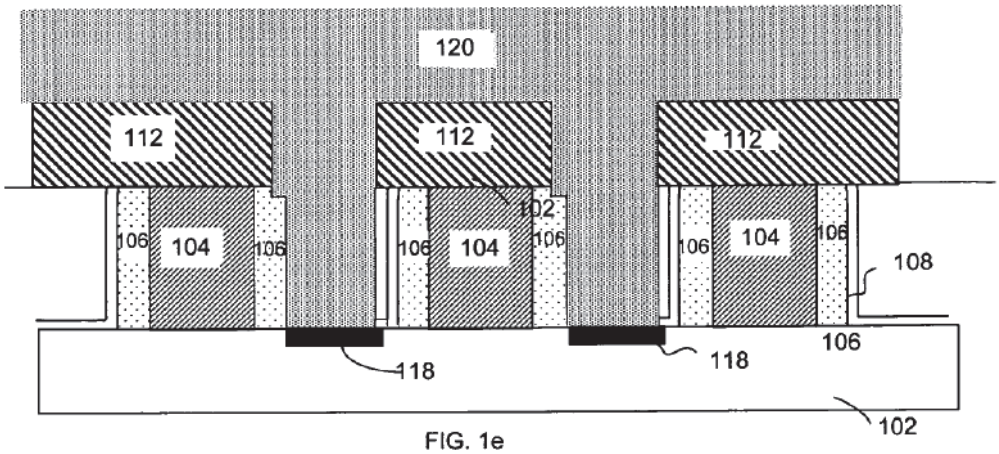


FIG. 1e

Sell then performs a planarization process on the contact metal and other layers that makes the spacer 106 and etch stop layer 108 shorter by removing a part. *Id.*, 3:23-30 ("A polishing process 123 may subsequently be performed, such as a

chemical mechanical polishing (CMP) process, for example, to remove the first contact metal 120 (FIG. 1f) and the stopping layer 112."), FIG. 1e (below).

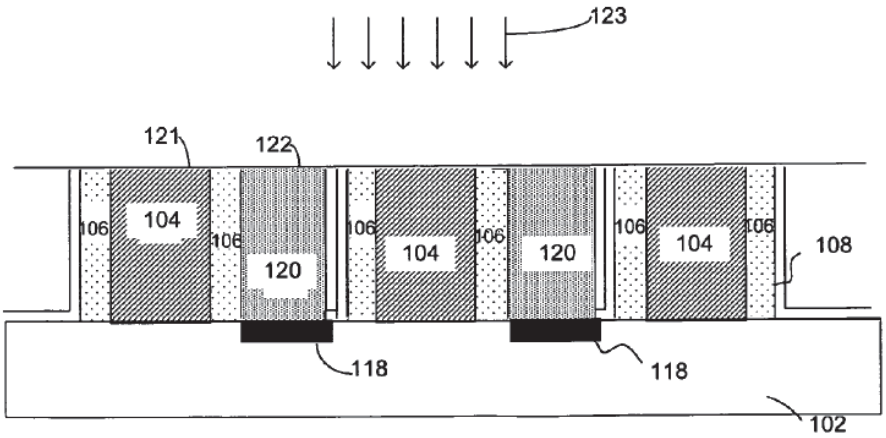


FIG. 1f

Sell explains this results in planarized top surfaces. PA-06, 3:31-43. The planarized top surface of gate 104 is co-planar with etch stop layer 108, and thus a POSITA would recognized that Sell's planarization process results in the etch stop layer 108 that is disposed on two sides of the metal gate 104 having a planar top surface by making the etch stop layer 108 shorter by removing a part (during a planarization process). Ex-03, ¶¶582-584.

Afterwards a stacked contact structure is formed with contact metal 128 and contact metal 120 to the source/drain region 118 of the device. *Id.*, 3:44-4:26, Fig. 1g (below).

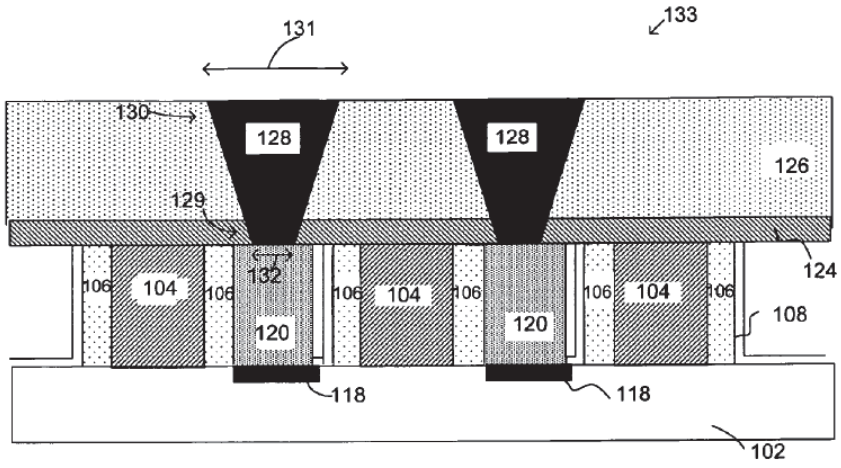


FIG. 1g

Sell therefore discloses a semiconductor structure including a etching stop layer (108) disposed on two sides of a metal gate (104) where the etching stop layer has a truncated top surface as claimed given it was made shorter by removing a part (including during a planarization process) and having a planar top surface, consistent with Interpretations 1-3 (*see* §II.D.1).

In view of the above, Sell is analogous art. For example, a POSITA would have understood that Sell's semiconductor structure can include "transistor structure" (PA-06, 2:10-22, 3:64-4:2, 4:19-26), is in the same field (e.g., semiconductor device transistor structures with contacts) and reasonably pertinent to a problem the '747 Patent purports to address (e.g., transistor structure contact fabrication). *See e.g.*, PA-06, 1:5-13, 1:29-2:23, 3:17-4:18; Ex-01 ('747 Patent), 1:9-2:9, 2:18-20, 2:39-42, 3:1-25, 5:31-6:37. Accordingly, a POSITA would have had reasons to consider the teachings and suggestions in Sell when contemplating the semiconductor structure of Chang's structure. Ex-03, ¶585.

A POSITA would have been motivated to modify Chang's structure with an etching stop layer disposed on two sides of the metal gate where the layer has a truncated top surface (*see* Interpretations 1-3, §II.D.1) to provide the protective benefits of etch stop layers consistent with that known in the art and suggested by Sell. Ex-03, ¶586.

For example, a POSITA would have been led by Chang's teachings in view of the above teachings of Sell to provide an etching stop layer disposed on two sides of the metal gate by performing known planarization processes (e.g., CMP) on the etching stop layer formed on the substrate (between the gate stack structures) that would remove material from the top surface of the etch stop layer along with other structures or layers subject to the planarization (e.g., CMP) processes, consistent with the teachings of Sell. Such a modification and implementing would have predicably resulted in the FIG. 5B structure including an etching stop layer that is disposed on two sides of a metal gate in a gate stack structure 308 that was made shorter by removing a part of the etching stop layer (that was previously formed) during a planarization process (e.g., CMP), consistent with the features disclosed and contemplated by Sell. Ex-03, ¶¶587-589.

Sell's teachings are consistent with the known use of an etching stop layer having a truncated top surface as understood by those of ordinary skill in the art at the time in context of the '747 Patent disclosures. *See e.g.*, Ex-01 ('747 Patent),

3:19-25 (explaining that CESL 20 (with a truncated top surface formed by a planarization process and having a planar top surface like that shown in Figure 1), and "manufacturing methods thereof" was "well known to persons of ordinary skills in the art"). Indeed, the '747 Patent suggests that such features were so "well known" that "details" need not be described to understand such features. *Id.*

Sell's teachings are also consistent with the use of a POSITA's state of art knowledge at the relevant time of the use and implementation of etching stop layers in the fabrication of semiconductor devices (like those of Chang), including those that were subject to planarization process during fabrication, that results in the layer being made shorter by removing a part (including during a planarization process) and ultimately having a planar top surface in the resulting structure.

For example, Huang (PA-03) discloses a Contact Etch Stop Layer (CESL) 36 that is a dielectric material acting as "an etch stop layer" disposed on two sides of a gate dielectric 24 and gate electrode 26. *See e.g.,* PA-03, [0008]-[0010], [0014], FIG. 1 (below). Ex-03, ¶¶590-592.

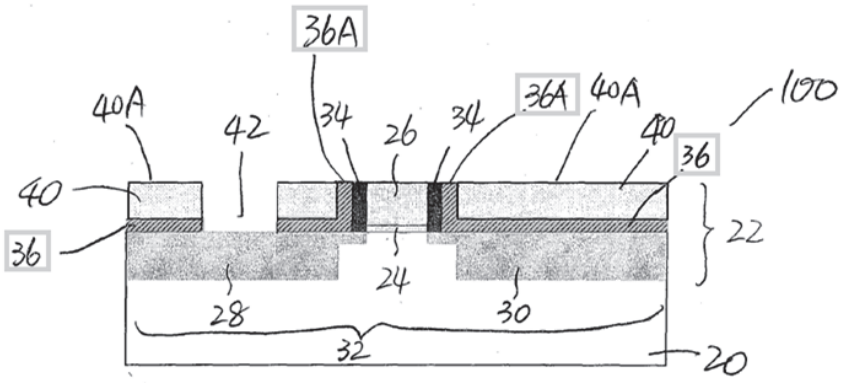


Fig. 1

A POSITA would have understood that CESL 36 is an etch stop layer to protect source/drain region (30) against etching of an opening (56) so etching stops on CESL 36, as shown in Figure 6 (below).

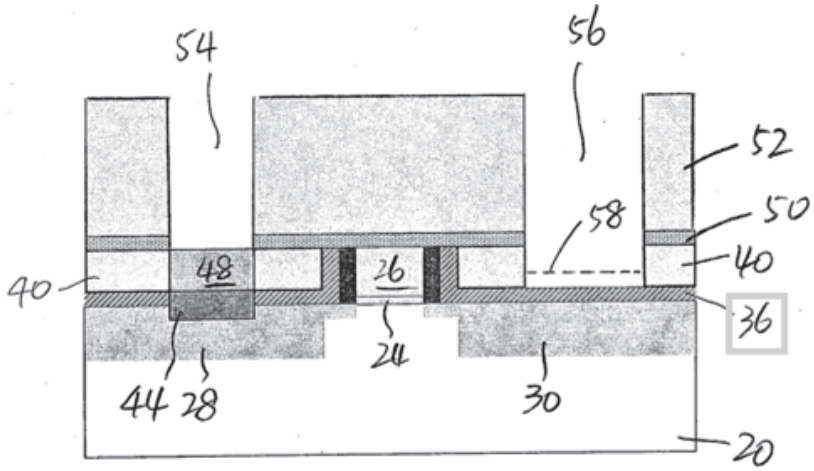


Fig. 6

As shown and described, Huang's etching stop layer 36 has top edges 36A that are planar, that were formed by CMP processes during Huang's last gate

approach processes. *See e.g.*, PA-03, [0009]. *See also* Ex-15 (Xiao), 544-545 (describing such an approach known at the relevant time).

As another example, Chi (PA-05, discussed below in Proposed Rejection 2E) also discloses the known use of etch stop layers disposed on the sides of a metal gate and having a planar top surface that was formed by removing a part and making the layer shorter during a planarization process. *See e.g.*, PA-05 (Chi), FIGs. 2B, 3C-3J, 11:15-24 ("an etch stop layer 34 is conformably deposited above the device 100"), 14:10-24 ("one or more CMP process are performed to remove portions of the … etch stop layer 34 … ."), 10:34-16:60. A POSITA would have understood that Chi discloses an etching stop layer 34 that has been made shorter by removing a part (including during a planarization process) and has a planar top surface. *See* discussions below regarding Chi in Proposed Rejection 2E (Claims 1-7). Ex-03, ¶¶593-595.

Liang (Ex-27) similarly confirms the known use of etching stop layers in semiconductor structures similar to that disclosed by Sell. *See* Ex-27 (Liang), FIGs. 1A-1H, 2:50-65 ("An etch-stop layer 107 can be formed over the substrate 101 and adjacent to sidewalls of the gate electrode 103"), 3:20-41, 4:5-17 ("The etch-stop layers 107 and 111 can have at least one material such as silicon carbide (SiC), silicon nitride (SiN), silicon carbon nitride (SiCN), silicon carbon oxide (SiCO), silicon oxynitride (SiON), boron nitride (BN), boron carbon nitride (BCN), other

material that has a desired selectivity with respect to silicon oxide, or any combinations thereof. The etch- stop layers 107 and 111 can be formed by any suitable process …"). *See also id.*, 1:56-2:23.

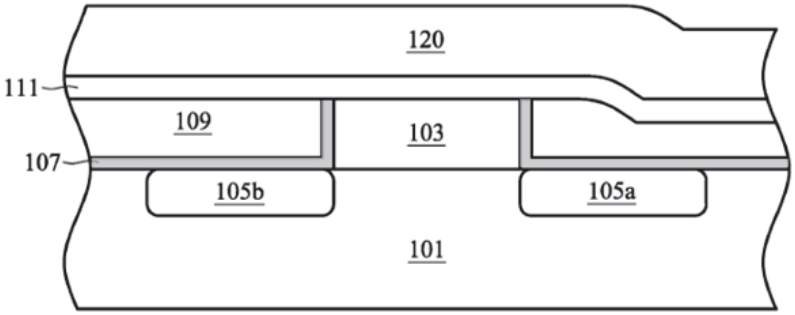


FIG. 1A

These teachings are consistent with the state of art knowledge of etching stop layers, including those that were made shorter by removing a part (including during a planarization process) and having a planar top surface as understood by a POSITA at the relevant time.

In light of the guidance by Sell in context of Chang and a POSITA's state of art knowledge at the relevant time, a POSITA would have found it obvious to include an etching stop layer in the fabrication and resulting structure of Chang's structure to provide etch protection to structural elements and layers in the fabrication of the structure. A POSITA would have been motivated by Chang's use of similar layers (e.g., silicon nitride protection layer) and in light of Sell, would have looked to provide such conventional features in Chang's structure to ensure the selective etching processes used to fabricate the resulting structure results in an operational

semiconductor device that performs in accordance with the appropriate application of the device. Ex-03, ¶596.

In light of such teachings of Sell, Chang, and state of art knowledge, a POSITA would have been motivated and found obvious to form and process an etching stop layer disposed on two sides of the metal gate by removing material from the etching stop layer's top surface using known planarization processes (e.g., CMP) in order to provide a planarized top surface spacer structure consistent with structures shown in the resulting structure of Chang. Such an implementation would have predictably resulted in an etching stop layer having a truncated top surface as claimed and consistent with Interpretation 1 (planar top surface), and Interpretations 2 and 3 (made shorter by removing a part (during a planarization process). *See* §II.D.1; Ex-03, ¶597.

A POSITA would have recognized and understood that etching stop layers spacers were well-known and used in semiconductor structures like Chang's structures, and likewise recognized advantages in using such layers. For example, a POSITA would have appreciated an etching stop layer beneficially provided protection to e.g., transistor gate structures, source/drain regions, and other structural elements in semiconductor structures, like those in Chang's structure. *See e.g.*, Ex-15 (Xiao), 164-65, 341-45. Ex-03, ¶598.

A POSITA would have also appreciated the benefits in providing an etching stop layer with a planar top surface because, for example, such planarized top surfaces were known to aid in the formation of subsequently formed structural elements and layers during subsequent fabrication processes (e.g., photolithography steps) that deposit such elements or layers on the top surface of the planarized surface. Accordingly, a POSITA would have been motivated to look to ways to provide such protection, as taught by Sell and known in the art. Ex-03, ¶599.

Thus, having recognized that the teachings of Sell is consistent with such known use and formation of etching stop layers with planar top surfaces (formed by known processes (e.g., CMP) during fabrication of semiconductor structures is consistent with features known in the art, a POSITA would have been motivated to implement such features, and done so with a reasonable expectation of success, in the semiconductor structure of Chang. Such a POSITA would have thus looked to protect features in the structure during fabrication (e.g., S/D regions, other components/materials) while promoting the formation of other structures and layers formed during subsequent fabrication process in the formation of the resulting structure of Chang. Ex-03, ¶600.

A POSITA would have reasonably expected success in implementing the above modification/configuration because providing an etching stop layer with a planar top surface would have involved nothing more than applying known

semiconductor manufacturing process (e.g., deposition, CMP, etching, etc.) for forming the etching stop layer on the sides of Chang's metal gates, where the etching stop layer (after formation) was planarized to provide a planar top surface that provided a protective surface conducive to subsequent formation of other structures and layers formed above. Designing, configuring, and implementing such an etching stop layer in the Chang structure would have been within the skill, knowledge, and capabilities of a POSITA at the relevant time, as described by Sell (and the state of art references discussed above, which are consistent with a POSITA's state of art knowledge on the use of etch stop layers in semiconductor structures similar to Chang). Ex-03, ¶601.

A POSITA would have leveraged their state of art knowledge and experience in considering the design needs and the market demands for computing devices that include a semiconductor structure as contemplated by Chang, and thus would have been motivated to design and configure fabrication processes to successfully provide such an etching stop layer in Chang's structure with a "truncated top surface" (as interpreted under Interpretations 1-3, *see* §II.D.1). Ex-03, ¶602.

Accordingly, for the reasons above, the combination of Chang and Sell discloses and/or suggests the semiconductor structure (as discussed above for Claim 1) including an etching stop layer disposed on two sides of the metal gate, and the

etching stop layer has a truncated top surface as recited in Claim 3 (under Interpretations 1-3 of "truncated top surface," *see* §II.D.1).

For the reasons above, Chang in view of Sell renders obvious claim 3 and thus the claim is invalid in view of that prior art combination. Ex-03, ¶603.

e. Claim 4: The semiconductor device of claim 2, wherein the first contacts disposed in the first dielectric layer and in the second dielectric layer and each first contact is a monolithically formed structure.

Claim 5: The semiconductor device of claim 2, wherein the second contacts disposed in the first dielectric layer and in the second dielectric layer and each second contact is a monolithically formed structure.

As explained for Proposed Rejection 2A, Chang discloses the semiconductor device of claim 1, comprising first and second contacts disposed in the second dielectric layer, as recited in limitations (1f) and (1g) of Claim 1. Ex-03, ¶604. Where, for example, "the semiconductor device of claim 1" is the SRAM described above in Proposed Rejection 2B, Chang discloses monolithically formed first and second contacts disposed in the second dielectric layer, as recited in claims 4-5. Any modification to the SRAM discussed in Proposed Rejection 2B, Claim 1 (to the extent any modification is deemed necessary) would not affect Chang's disclosure of Claims 4-5. For example, a POSITA would have understood that no proposed or perceived modification to the SRAM discussed in Proposed Rejection 2B, claim 1 would change or otherwise affect the fact that Chang's self-aligned contacts 1670,

1671, 1675 are monolithically formed and disposed in ILD layer 1503 (Claims 4-5) even in the structure discussed here for Proposed Rejection 2C. Ex-03, ¶604.

Thus, for reasons similar to those discussed above for Proposed Rejection 2A (Claims 1-2 and 6) and those for Proposed Rejection 2B (Claims 1-2 and 4-6), Chang in view of Sell discloses and/or suggests, and renders obvious, Claims 4-5 of the '747 Patent and thus the claims are invalid under the combination. Ex-03, ¶605.

f. Claim 6: The semiconductor device of claim 1, further comprising at least one fin structure disposed on the substrate.

Proposed Rejection 2A discusses how Chang discloses the limitations in Claim 6. Proposed Rejection 2B discusses how the collective teachings and suggestions in Chang further renders obvious the limitations in Claim 6. Those opinions are incorporated herein to support Proposed Rejection 2C. For those reasons, and those that are discussed in this Proposed Rejection 2C, Chang in view of Sell discloses and/or renders obvious Claim 6 of the '747 Patent. Such features would have been included in the Chang and Sell combination that is discussed here in this Proposed Rejection 2C. A POSITA would have had the same rationale, expectation of success, and motivation, and similarly found obvious in view Chang's collective teachings, to include at least one fin structure disposed on the substrate of the Chang semiconductor substrate (that is discussed for Claim 1 in Proposed Rejection 2B (and incorporated Proposed Rejection 2A)). Accordingly, the

combination of Chang in view of Sell as discussed in this Proposed Rejection 2C likewise discloses or suggests Claim 6.[32] Ex-03, ¶¶606-610.

Indeed, as explained for Claim 6 in Proposed Rejection 2B, a POSITA would have been knowledgeable of the use and implementation of planar and fin-shaped FETs, and the similarities between them (e.g., channel, source/drain regions, gates, etc.). A number of state of the art references provide disclosures consistent with a POSITA's knowledge at the time. *See e.g.*, Ex-18 (Sze), 433-34, 438, FIGs. 3, 6; Ex-07 (Neamen), xxiii, 403-405, FIGs. 0.5, 10.34, 10.35; Ex-09 (Wolf), 3, 6; Ex-15 (Xiao), 72-74, 351, 370-371, FIGs. 3.20, 9.31, 10.2; Ex-28 (Lin), 7:54-60, 10:17-23, 12:51-56, 16:35-41; Ex-35 (Chi, 2012), 1; Ex-29 (Ranade), ¶¶25, 44; Ex-30 (Hu), Abstract, 2:11-14 (FinFETs are "an extension of conventional planar MOSFET technology"), 5:37-40 (FinFETs fabrication "is compatible with conventional planar MOSFET fabrication techniques"); Ex-31 (Doyle), 133 (a

[32] A POSITA having found it obvious to implement Chang's structure with at least one fin structure disposed on the substrate does not mean Chang does not disclose such a feature as claimed in Claim 6—Chang does disclose the claimed fin structure for reasons discussed for Claim 6 in Proposed Rejection 2A. Rather, as explained here, supported by the teachings and suggestions of Chang (including in context of Sell as applied for Claim 1), a POSITA would have found it obvious to form and implement a fin structure as claimed in Chang's structure notwithstanding the disclosures in Chang that are addressed above for Proposed Rejection 2A.

FinFET "very much resembles [a] bulk transistor from the processing point-of-view"); Ex-32 (Simonelli), ¶¶1, 3-4, 44-45; Ex-33 (Chau), 2:38-41, 5:3-26, 6:35-50; Ex-34 (Chang '728), 2:61-3:3. Further, a POSITA would have appreciated and recognized the benefits of implementing the Chang structure as a non-planar structure with a multi-gate or FinFET transistor, such as scaling to minimize the footprint of the integrated circuit implementing such transistors. *See* Ex-15 (Xiao), FIG. 15.1, 650-51. Ex-03, ¶607.

Such knowledge coupled with the collective teachings and suggestions in Chang (discussed above for Claim 6 in Proposed Rejection 2B), would have led a POSITA to configure the Chang's structure in context of a multi-gate or FinFET transistor device including at least one fin structure disposed on the substrate of the structure. Ex-03, ¶608.

Accordingly, it would have been obvious to configure the Chang-Sell structure to include at least one fin structure disposed on the substrate of the structure, as recited in Claim 6 of the '747 Patent for reasons similar to those explained for Claim 6 in Proposed Rejection 2B.

For the reasons above, Chang in view of Sell renders obvious claim 6 and thus the claim is invalid in view of that prior art combination. Ex-03, ¶¶609-610.

g. Claim 7: The semiconductor device of claim 1, further comprising a salicide layer disposed between each S/D region and each first contact.

Proposed Rejection 2A discuss how Chang discloses the limitations in Claims 1-2 and 6. Those discussions are incorporated here in Proposed Rejection 2C. In addition to the reasons explained for Proposed Rejection 2A (which are incorporated herein), for the reasons below and above in this Proposed Rejection 2C, the combined teachings and suggestions in Chang and Sell disclose or suggest, and render obvious Claim 7. Ex-03, ¶¶611-632.

A POSITA would have would have been motivated to implement in Chang's structure a self-aligned silicide ("salicide") layer disposed between each S/D region and each first contact in view Sell. Ex-03, ¶612.

A POSITA would have appreciated and understood that the use of a salicide layer between a source/drain and a contact, such as in self-aligned trench contacts, was widely known and implemented in semiconductor devices at the relevant time. Ex-15 (Xiao), 157-58, FIG. 5.39 (describing salicide processes involving metal deposition/annealing over source/drain regions consistent with a POSITA's state of art knowledge at the time). Ex-03, ¶613.

Moreover, a POSITA would have been understood that providing a salicide layer between the S/D diffusion region 1600 and the self-aligned contacts 1670, 1671 would have reduced electrical resistance with the S/D contact in Chang's FIG.

27 structure. *See e.g.*, Ex-15 (Xiao), 585 (describing a POSITA's state of art knowledge at the relevant time that salicide helps reduce contact resistance).) Ex-03, ¶614.

Understanding that the use of a salicide layer between a source/drain region and contact would advantageously create a more conductive contact , and that such features were widely known in the art at the time, and that Chang's semiconductor structure includes a source/drain region and corresponding contact (*see* Proposed Rejection 2A, limitations 1(e)-1(f)), a POSITA would have had reasons to consider ways to likewise improve Chang's structure. To do so, a POSITA would have looked to teachings in the art to supplement and/or complement their knowledge and experience pertaining to the fabrication and implementation of semiconductor structures. A POSITA would have found Sell to provide insight that would have led a POSITA to implement a salicide layer between a source/drain and the contacts in the structure of Chang to enhance or establish conductive surfaces to the semiconductor device. Ex-03, ¶615.

For instance, a POSITA would have recognized that Sell discloses the known use of a salicide layer disposed between each S/D region and each first contact. For example, Sell discloses processes that form a salicide 118 between source/drain contact and the source/drain in a transistor structure. *See e.g.,* PA-05 (Sell), 1:7-13, 3:6-16, 3:17-30, 4:5-18; FIGs. 1d, 1e, 1f, 11. Ex-03, ¶616.

For example, as explained above, Sell discloses that the "[m]ethods of the present invention are depicted in FIGS. 1 a-1 g" where "transistor structure 100 comprising a substrate 102, and a gate 104, which may comprise a metal gate in some embodiments, and may comprise such metal gate materials as hafnium, zirconium, titanium, tantalum, or aluminum, or combinations thereof, for example. The gate 104 may comprise a top surface 105." PA-06, 1:65-2:9. Further, "transistor structure 100 may further comprise a spacer material 106, that may be adjacent and in direct contact with the gate 104." *Id.*, 2:10-22. The etch stop layer 108 and spacer 106 each has a planar top. PA-05, FIG. 1a. Ex-03, ¶¶617-624.

Sell also explains that after a sacrificial stopping layer 112 is formed on the top surface 105 of gate 104, and a resist layer 114 formed on the stopping layer 112 (*id.*, 2:23-34), an etching process is performed to form openings 116 leaving the etch stop layer 108 intact. PA-05, 2:35-49, Fig. 1b (below).

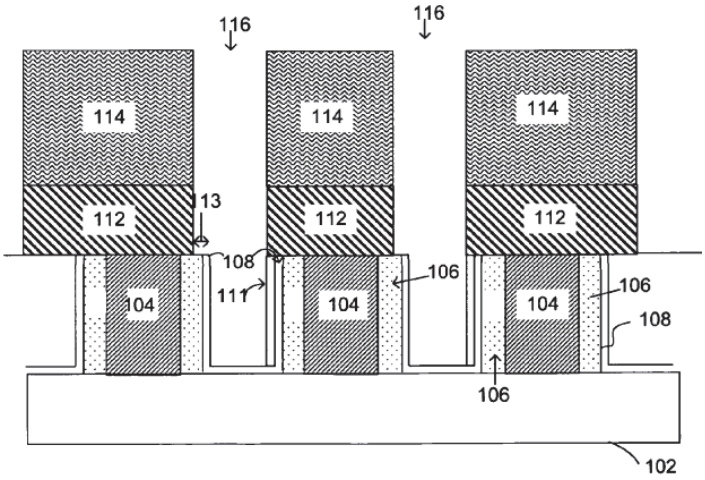


FIG. 1b

Sell discloses the etch stop layer 108 may be removed from the **source/drain region 103** of the substrate leaving a **source/drain contact area 107** exposed. *Id.*, 2:62-66, FIG. 1c (below). *See also*, *id.*, 2:50-61.

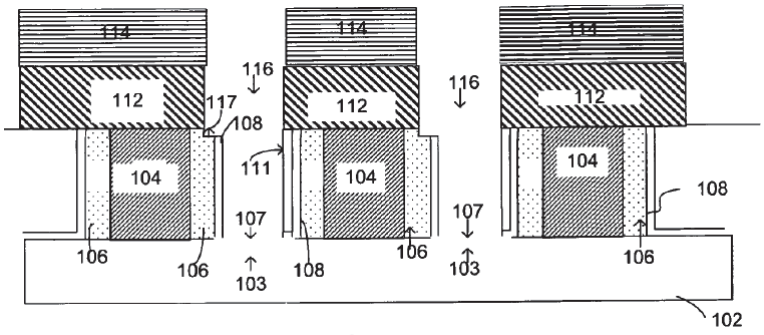


FIG. 1c

Sell also discloses "**a salicide 118 may be formed on/in the source/drain contact area 107 using any suitable salicide process as are known in the art, such as but not limited to a nickel salicide process and/or other such salicide process**." *Id.*, 3:6-16. *See id.*, FIG. 1d (below).

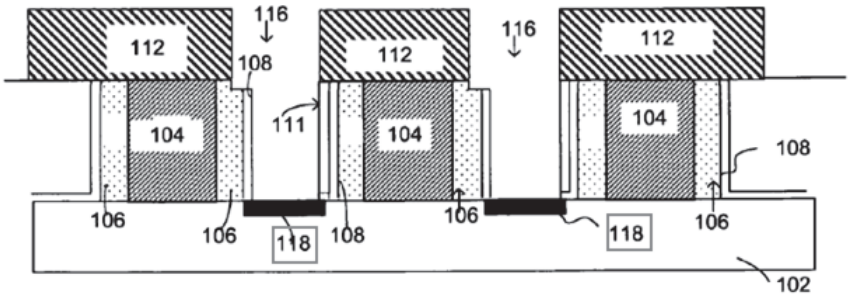


FIG. 1d

Next a **first contact metal** 120 is formed on the **salicide 118**. *Id.*, 3:17-23, FIG. 1e (below).

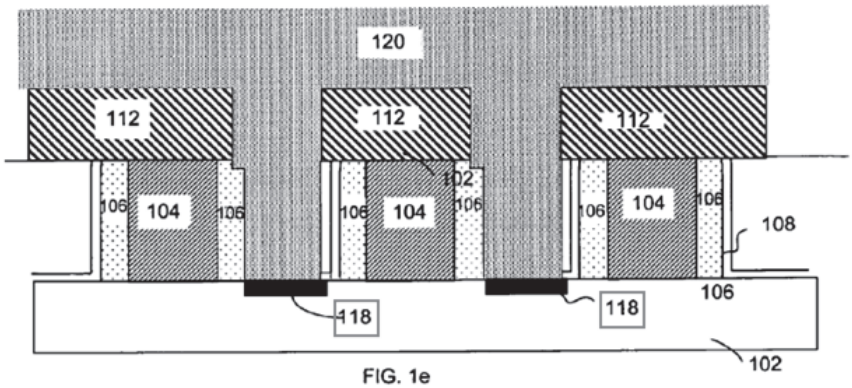


FIG. 1e

Sell then performs a planarization process on the contact metal and other layers that makes the spacer 106 and etch stop layer 108 shorter by removing a part. *Id.* at 3:23-30 ("A polishing process 123 may subsequently be performed, such as a chemical mechanical polishing (CMP) process, for example, to remove the first contact metal 120 (FIG. 1f) and the stopping layer 112."), FIG. 1e (below).

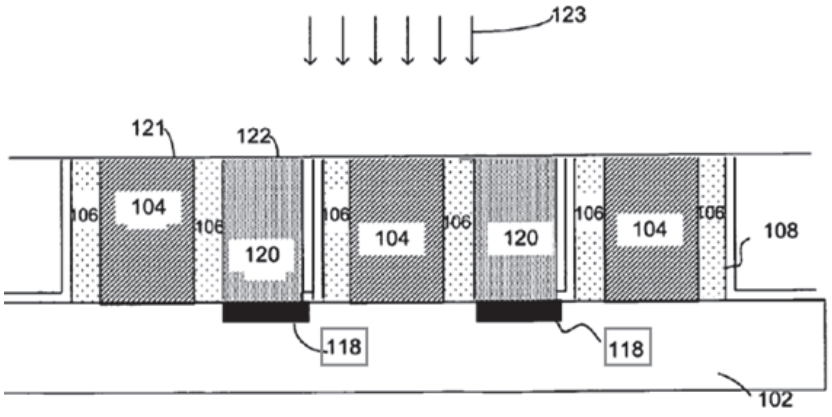


FIG. 1f

Sell explains this results in planarized top surfaces. *Id.*, 3:31-43. Afforwards a stacked contact structure is formed with contact metal 128 and contact metal 120 to the source/drain region 118 of the device. *Id.* at 3:44-4:26 As shown in Fig. 1g

(below), the semiconductor structure includes a salicide layer 118 that is disposed between each source/drain region and each contact.

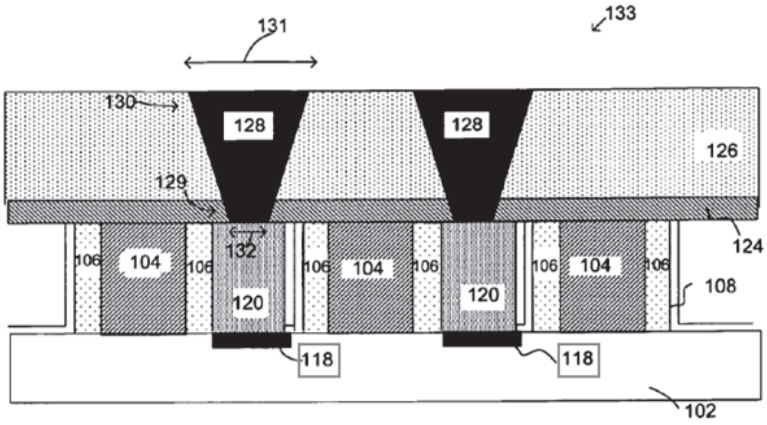


FIG. 1g

Sell therefore discloses a semiconductor structure including a etching stop layer (108) disposed on two sides of a metal gate (104) where the etching stop layer has a truncated top surface as claimed given it was made shorter by removing a part (including during a planarization process) and having a planar top surface, consistent with Interpretations 1-3. *See* §II.D.1.

Based on the foregoing, Sell is analogous art. For example, a POSITA would have understood that Sell's semiconductor structure can include "transistor structure" (PA-06 (Sell), 2:10-22, 3:64-4:2, 4:19-26)), is in the same field (e.g., semiconductor device transistor structures with contacts) and reasonably pertinent to a problem the '747 Patent purports to address (e.g., transistor structure contact fabrication). *See e.g.*, *id.*, 1:5-13, 1:29-2:23, 3:17-4:18; Ex-01 ('747 Patent), 1:9-2:9, 2:18-20, 2:39-42, 3:1-25, 5:31-6:37. Accordingly, a POSITA would have had

reasons to consider the teachings and suggestions in Sell when contemplating the semiconductor structure of Chang's structure. Ex-03, ¶625.

In light of the teachings and suggestions of Sell, in context of those of Chang and a POSITA's state of art knowledge at the time, a POSITA would have been motivated to consider and implement the known use of a salicide layer to reduce resistance between the source/drain region and the contacts in Chang's structure. Given the teachings of Sell in context of a POSITA's knowledge, a POSITA would have appreciated that providing a salicide layer between the source/drain region and contacts in the structure of Chang would have been an obvious implementation of conventional and known semiconductor device fabrication and structure features that were well within the experience and capabilities of such a skilled person at the relevant time (as demonstrated by Sell). Accordingly, and in context of the collective teachings in Sell and Chang, a POSITA would have reasonably expected to succeed at implementing such features in Chang's structure. Ex-03, ¶626.

Therefore, in light of the teachings and suggestions in Sell, Chang, in context of a POSITA's knowledge and experience at the relevant time, a POSITA would have been motivated and found obvious to include a salicide layer in Chang's structure to provide a more conductive interface between each S/D region and each source/drain contacts, thus improving performance of the semiconductor device. Such an implementation would have been consistent with the concerns in the art to

improve performance of semiconductor devices, as known in the art at the relevant time. Ex-03, ¶627.

Thus, having recognized that the teachings of Sell is consistent with the use of salicide layers in semiconductor structures is consistent like those described by Chang, a POSITA would have been motivated to implement such features in the Chang structure, and done so with a reasonable expectation of success. A POSITA would have looked to provide salicide layer between each source/drain region and each trench contact via 341 in order to provide a more conductive interface to the source/drain region of the structure, thus promoting improved performance of the resulting structure of Chang. Ex-03, ¶628.

A POSITA would have reasonably expected success in implementing the above modification/configuration to the structure of Chang because providing a salicide layer in the manner Discussed above would have involved nothing more than applying known semiconductor manufacturing processes for forming a self-aligned silicide layer consistent with the guidance in Sell. Designing, configuring, and implementing such a salicide layer in the Chang structure would have been within the skill, knowledge, and capabilities of a POSITA at the relevant time. Ex-03, ¶629.

Further, a POSITA would have understood and appreciated that providing salicide layer as Discussed above would have been an obvious example of

combining prior art elements according to known methods, e.g., combining the teachings of Sell with those of Chang in accordance with known semiconductor device fabrication processes. Ex-03, ¶630.

A POSITA would have leveraged their state of art knowledge and experience in considering the design needs and the market demands for computing devices that include a semiconductor structure and thus would have been motivated to configure and design fabrication processes to successful provide such a salicide layer in the Chang structure. Ex-03, ¶631.

Accordingly, it would have been obvious to configure the Chang structure to include a salicide layer disposed between each source/drain region and each S/D contact ("first contact"), like that recited in Claim 7 of the '747 Patent. Thus, for the reasons here, and above for this Proposed Rejection 2C, and those for claim 1 in Proposed Rejection 2A, the collective teachings and suggestions of Sell and Chang disclose or suggest the features of Claim 7. Thus, Chang in view of Sell render obvious Claim 7 of the '747 Patent. Ex-03, ¶632.

For the reasons above, Chang in view of Sell renders obvious claim 7 and thus the claim is invalid in view of that prior art combination.

4. Proposed Rejection 2D: Claims 8-9 Are Obvious Over *Chang*, *Sell* and *Huang*

a. Claim 8: The semiconductor device of claim 3, further comprising a plurality of third contacts disposed on parts of the first contacts and on parts of the second contacts, wherein each third contact is a monolithically formed structure.

Claim 9: The semiconductor device of claim 8, wherein each third contact comprises a via hole structure and a trace structure, wherein the via hole structure and the trace structure comprise the same material and contact each other directly.

Chang in view of Sell and Huang discloses and/or suggests these limitations. Proposed Rejection 2C (incorporated by reference herein) explains how Chang in view of Sell and Huang discloses and/or suggests claims 1 and 3. *See* §VI.B.3(a), (b), (d). Ex-03, ¶¶633-666.

As explained for Proposed Rejection 2C (which incorporates Proposed Rejection 2A), Claim 1, Chang teaches "a plurality of first contacts" (e.g., parts of self-aligned contacts 1670, 1671, and self-aligned contact 1675) "disposed in the first dielectric layer" (e.g., interlayer dielectric layer 1503) "that are electrically connected to parts of the S/D region" (e.g., source and drain regions of PMOS diffusion layer 1600), as claimed in limitation 1(f). *See* §VI.B.1(a)(7). Chang also teaches self-aligned contacts 1670 and 1671 (as indicated in the annotated illustration of FIG. 27 below) that are "a plurality of second contacts" that "are

electrically connected to" gates 1446, 1597 and are "disposed in" interlayer dielectric layer 1503, as claimed in limitation 1(g). *See* §VI.B.1(a)(8); *see also* PA-04, FIG. 27.

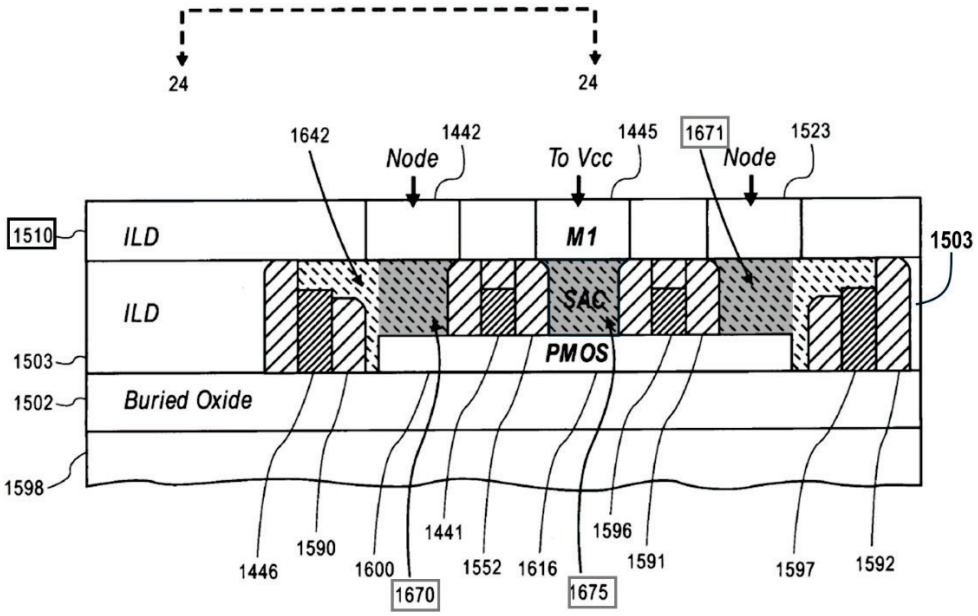


FIG. 27

PA-04 (Chang), ¶¶112-13. In addition to Chang's FIG. 27 structure, Sell discloses a semiconductor structure including a etching stop layer (108) disposed on two sides of a metal gate 104 where the etching stop layer has a truncated top surface, as claimed in Claim 3. *See* §VI.B.3(d); *see also* PA-06 (Sell), FIG. 1a. Ex-03, ¶634.

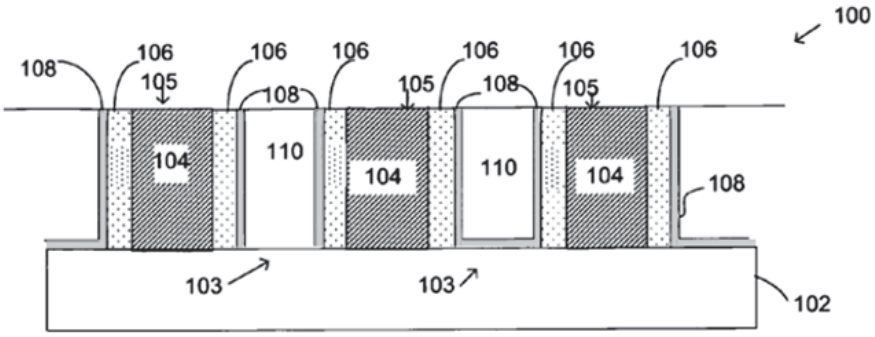


FIG. 1a

PA-06, FIG. 1a.

Further, it was well-known and conventional to form metal (1) ("M1") metal lines and metal (0) vias (above the metal (0) lines and device contacts) using a dual-damascene process. By the time of the alleged invention, the dual-damascene process was an established technique in semiconductor manufacturing, particularly in the back-end-of-line (BEOL) processing, which is the "formation of the M1 wiring layer to formation of a pad opening to a final passivation... in a wafer level package process." (Ex-11, ¶89.) Ex-03, ¶¶635-640.

A number of state of art references confirm such an understanding and provide teachings consistent with a POSITA knowledge of the art at the time of the '747 patent. For example, using a dual-damascene process to provide M1 metal lines and metal (0) vias was conventional and ubiquitous, as discussed in Xiao. *See* Ex-15, 345-49, FIG. 9.35, 346 (a via-first dual damascene process), FIG. 9.36, 346 (a

trench-first dual damascene process), FIG. 9.37, 346 (a via-first dual damascene process), 19.

As another example, Wolf explains that in a dual-damascene process, "only a single metal deposition step is used to simultaneously form the main metal lines and the metal in the vias," after which "CMP is used to remove excess metal." (Ex-09 (Wolf), 696-98.) This "sequence is repeated for the next level of metal" (i.e., M2, M3... M8). Ex-09, FIG. 15-3, p. 697.

As another example, May (Ex-10, May) explains that "[d]amascene processing involves the creation of interconnect lines by first etching a trench or canal in a planar dielectric layer and then filling that trench metal," and "[i]n dual damascene processing (Figure 5.13) a second level is involved where a series of holes (i.e., contacts or vias) are etched and filled in addition to the trench." Ex-10 (May), FIG. 5.13, 55-56.

As further examples, using a dual-damascene process to provide M1 metal lines and metal (0) vias is referred to Xiao (Ex-15 (Xiao), 345-49) at the time of the alleged invention to be "mainstream" (Ex-15, 345-49), well developed "[i]n the late 1990s" (p. 453), having "maturity" (*id.*, 464), "dual damascene has **become the process of choice** for copper metallization in IC chip manufacturing" (*id.*, 517-18), "Copper interconnections have become a **mainstream technology in CMOS logic IC** since the development of the 130-nm technology node. Copper CMP processes

have been **widely used in** dual damascene processes to form copper interconnections in **advanced IC fabs**" (*id.*, 543), "The dual damascene process, which combines via and trench etching before metal deposition, is **the most commonly used method for copper metallization**" (*id.*, 574-79).

A POSITA was also aware of known advantages to implementing a dual-damascene process to provide M1 metal lines and M0 vias, including the following.

- **simplified fabrication**: "The dual damascene process can eliminate some metal deposition and CMP processes, unlike two single damascene processes." (Ex-15 (Xiao), 574-79); "The dual-damascene process offers the advantage of reducing the number of process steps" (Ex-09 (Wolf), 695); "The reduction in the number of processing steps is another of the benefits that have driven the development of dual-damascene processes" (*id.*, 698).

- **no requirement for metal etching**: "the dual damascene process does not need to etch metal" (Ex-15 (Xiao), 345-49, 497-98), "[t]he fact that the dual damascene process does not require a metal etch step paved the way for copper metallization of IC interconnections in the late 1990s" (*id.*, 464), "[b]ecause copper is very difficult to dry etch, dual damascene has become the process of choice for copper metallization in IC chip manufacturing" (*id.*, 517-18), "The advantage of damascene processing is that it eliminates the need for metal etch" (Ex-10 (May), 56).

- **reduced risk of electromigration failure**: "One special benefit of the dual damascene technique is that the via plug is now of the same material as the metal line and the risk of via electromigration failure is reduced." (*Id.*, 92.)

As these state of the art sources further explain that "dual damascene process does not need to etch metal…dual damascene has become the process of choice for copper metallization…and [has] become mainstream." Ex-15, 345-49; *see also id.*, 345-49, FIG. 11.3, 464, 497-98, FIG. 11.38, 517-18, FIG. 12.15, 543, 574-79. Ex-03, ¶¶641-643.

Many other references recognized these advantages. (Ex-09 (Wolf), 695 ("The dual-damascene process offers the advantage of reducing the number of process steps"), 698 ("The reduction in the number of processing steps is another of the benefits that have driven the development of dual-damascene processes."); Ex-10 (May), 56 ("The advantage of damascene processing is that it eliminates the need for metal etch"), 92 ("One special benefit of the dual damascene technique is that the via plug is now of the same material as the metal line and the risk of via electromigration failure is reduced.").

Accordingly, a POSITA considering the semiconductor structure of the Chang-Sell combination would have been motivated to look to teachings in the art for ways to provide a connection of the semiconductor structure via the first contacts

and the second contact to the M1 layer with simplified fabrication, no requirement for metal etching, and reduced risk of electromigration failure. Ex-03, ¶644.

In doing so, a POSITA would have recognized Huang as an example of such relevant teachings. Consistent with the POSITA's knowledge discussed above, Huang (PA-03) teaches the use of a dual-damascene process to provide M1 metal lines and M0 vias. PA-03, ¶17, FIG. 8A. Huang teaches metal layer M1 metal lines 74 and M0 vias 72 for "for connecting to contact plugs 60 and 62," as shown in annotated FIG. 8A below. Ex-03, ¶¶645-648.

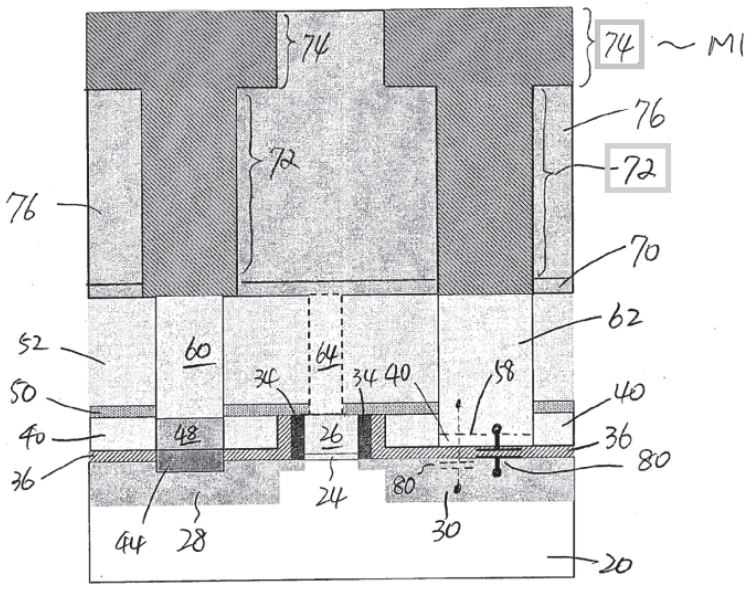


Fig. 8A

PA-03, ¶17, FIG. 8A.

In Huang, "M0 vias 72 and metal lines 74 may be formed using a dual-damascene process, and hence no noticeable interfaces are formed between M0 vias 72 and the respective overlying metal lines 74." PA-03, ¶17.

Huang's aforementioned structure also corresponds to **a via hole structure and a trace structure, wherein the via hole structure and the trace structure comprise the same material and contact each other directly**. For example, Huang's M0 vias 72 structure corresponds to a "via hole structure" and metal lines 74 structure corresponds to the third contact's "trace structure."

Given that the "M0 vias 72 and metal lines 74 may be formed using a dual-damascene process, and hence no noticeable interfaces being formed between M0 vias 72 and respective overlying metal lines 74" (PA-03, ¶17), the via hole structure and the trace structure comprises the same material and contact each other directly.

Huang and Chang each disclose features relating to semiconductor devices/structures and/or parts thereof. For example, Chang and Huang describe semiconductor structures with metal layers to contacts (i.e., gate and source/drain contacts). (*See*, *e.g.*, PA-04 (Chang), ¶¶108, 112-13, FIG. 27; PA-03 (Huang), ¶17; Ex-01 ('747 Patent), 5:31-6:37.) Thus, a POSITA would have had reasons to consult Huang when looking to implement a semiconductor structure like that discussed in Chang. Ex-03, ¶649.

In considering Huang in context of Chang, a POSITA would have been motivated to consider the collective teachings of Chang in view of Sell with those of Huang to achieve a dual-damascene process to provide M1 metal lines and M0

vias in the structure resulting from the combination of Chang and Sell. PA-03 (Huang), ¶17, FIG. 8A. Ex-03, ¶650.

A POSITA would have been motivated to implement such a dual-damascene process in the structure resulting from the combination of Chang and Sell, and would have reasonably expected such an implementation to be successful in context of Chang's disclosed structure. The implementation of a achieve a dual-damascene process to provide M1 metal lines and M0 vias was known in the art by a POSITA before the alleged invention of the '747 patent, as demonstrated by the above-mentioned state of art teachings (*see* discussions above regarding Wolf, May, and Xiao). A POSITA would have readily appreciated the possibility of using a dual-damascene process to provide M1 metal lines and M0 vias, as disclosed by Huang. Chang provides a metal self-aligned contacts 1670, 1671 connected to metal one lines 1442, 1523 (PA-04 (Chang), ¶¶108, 112-13), but does not provide any BEOL interconnection, which a POSITA would have understood is critical to create an integrated circuit with multiple trigate transistors for devices such as SRAMs that have predictable design and performance, as is the driving force of the semiconductor industry and of Chang. PA-04 (Chang), ¶6; Ex-03, ¶651.

A POSITA would have appreciated that the implementation of a dual-damascene process to provide M1 metal lines and M0 vias was at the time, a conventional method to produce such implementations. (*See above and for example*,

(Ex-09 (Wolf), 696-98; Ex-10 (May), 55-56; Ex-15 (Xiao), 19, 345-49, 453, 464, 497-98, 517-18, 543, 574-79.) A POSITA would have understood that the combined teachings of Chang, Sell and Huang would merely amount to determining a suitable dual-damascene process to modify the metal one line in Chang's FIG. 27 structure as explained above. Ex-03, ¶652.

Whether a POSITA considers Chang's metal one line to be what is known in the art as an M1 layer would not change the aforementioned discussions. A POSITA would have understood and appreciated that there was no universal convention as to what such skilled artisans considered the "M1" or "M0" layer in semiconductor structures/devices. In Chang, the metal one line is what connects to the MOS diffusion layer and the self aligned contacts of the metal gates. PA-04 (Chang), ¶¶112-13; Ex-03, ¶653.

Accordingly, a POSITA would have been reasonable in considering the "M0" process to be an "M1" process because it is the first metalized trench/via process. As discussed, the dual damascene process was known to be generally repeated a number of times. *See* Ex-09 (Wolf), 696-98; Ex-15 (Xiao), 19; Ex-03, ¶¶654-655.

FIG. 13.30 and other figures (for example, FIGs. 14.17-20) below illustrate a via-first dual damascene copper low-k interconnection process for an M2 metal layer and M1 via over an M1 metal layer. *See* Ex-15 (Xiao), 578, 611-14, FIGs. 13.30, 14.17.

Under any convention, a POSITA would have understood a dual-damascene process generally involved the conventional steps of patterning and etching the via and trench definition, depositing metal to fill the space of both via and trench, and CMP. (*See above and for example*, Ex-09 (Wolf), 696-98; Ex-10 (May), 55-56; Ex-15 (Xiao), 19, 345-49, 453, 464, 497-98, 517-18, 543, 574-79.) A POSITA would have been able to readily apply conventional methods of dual-damascene processes, such as those taught by Huang, to modified structure of Chang in view of Sell with high predictability and success. Ex-03, ¶656.

Accordingly, a POSITA would have been motivated to modify Chang's metal contacts to include, above its metal zero lines, Huang's M1 metal lines and M0 vias. In fact, Huang explicitly contemplates placing upper metal lines and vias over lower metal lines, such as metal (0) portion 350 in explaining that "In subsequent process steps, more metal layers (not shown) may be formed over metal layer M1." *See* PA-03 (Huang), ¶17; Ex-03, ¶657.

The above motivation rationale discussed above for claims 8 and 9 would have been applicable to both Chang's FIG. 27 structure discussed for claim 1 in §VI.B.1(a) and to Chang's modified embodiment discussed for claims 1 and 3 in §§VI.B.3(a), (b), (d).

Proposed Rejections 2B-2C explain how Chang discloses and/or suggests claims 1-2 and 4-6. *See* §§VI.B.1-2, incorporated herein. However, in addition to

Chang's FIG. 27 structure discussed above (claim 1 in §VI.B.1) or as modified (claims 1 and 3 in §§VI.B.3(a), (b), (d)) a POSITA would have been motivated to implement **a plurality of third contacts** as claimed in claims 8-9 in view of Huang.

In light of Huang's teachings and a POSITA's state of art knowledge as discussed above, Chang's FIG. 27 structure would have been predictably modified to include, above its metal one lines 1442, 1523, consistent with the teachings of Huang using the dual-damascene processes known in the art and as taught by Huang. *See above*. Ex-03, ¶¶658-661.

As a result, the modified FIG. 27 structure would have included a **plurality of third contacts** (for example, parts of the newly formed M1 lines above Chang's metal contacts 1670, 1671 and metal lines 1442, 1523 the M1 and M0 lines formed based on Huang's teachings) **disposed on parts of the first contacts** (for example, parts of 1670, 1671) **and on parts of the second contacts** (for example, parts of 1670, 1671), as in claim 8. *Id.*

In addition, **each third contact** (in the modified FIG. 5B structure) would have comprised **a via hole structure (M0 vias) and a trace structure (**parts of the newly formed M1 lines (*see* Ex-01, 5:48-53 (trace structure may be "lines")), which would **comprise the same material and contact each other directly** (as in claim 9) given they are formed using the dual-damascene process like that taught by

Huang, which would also result in **each third contact** (above) being a **monolithically formed structure (**as in claim 8). Ex-03, ¶662.

A POSITA would have understood and appreciated that such a modification would have involved the application of known technologies/ techniques (for example, dual-damascene process to provide M1 metal lines and M0 vias) to a known device/structure (like Chang's FIG. 27 embodiment with metal zero lines 1442, 1523). Accordingly, such a skilled person would have been motivated to implement such a modification, and would have reasonably expected such an implementation to be successful. A POSITA would have understood upon considering and implementing such knowledge, known techniques, and teachings in the prior art references, such a modification would have yielded the foreseeable result of providing M1 metal lines and M0 vias to a known device/structure (Chang's FIG. 27 structure with metal zero lines 1442, 1523) with operability to the M1 layer in the structure of FIG. 27. Ex-03, ¶663.

In the combined structure of Chang, Sell and Huang, M0 vias 72 (**a via hole structure**) and metal layer M1 metal lines 74 (**a trace structure**) form **a third contact**. This would have been consistent with the teachings shown in annotated FIG. 8A of Huang above. Ex-03, ¶664.

As discussed in claim 8, a dual-damascene process is used to form M0 vias 72 and metal layer M1 metal lines 74 together in a single deposition, which a POSITA

would have understood to mean **the via hole structure and the trace structure comprise the same material and contact each other directly**. (PA-03, ¶17 ("no noticeable interfaces are formed between M0 vias 72 and the respective overlying metal lines 74."), FIG. 8A.) Ex-03, ¶665.

For the reasons above, Chang in view of Sell and Huang renders obvious claims 8 and 9, and thus the claims are invalid in view of that prior art combination. Ex-03, ¶666; *KSR*, 550 U.S. at 416.

5. Proposed Rejection 2E: Claims 1-7 Is Obvious Over *Chang* and *Chi*

Proposed Rejection 2E discusses how the combined teachings and suggestions of Chang (as discussed above in both Proposed Rejections 2A and 2B) and Chi in context of a POSITA's state of art knowledge discloses and/or suggests, and renders obvious, certain features recited in the claim limitations addressed below. Thus, the discussions regarding the teachings and suggestions in Chang in both Proposed Rejections 2A and 2B are incorporated herein to support Proposed Rejection 2E.

a. Claim Limitations [1.pre]-[1.c] and [1.e]-[1.h]

Proposed Rejection 2A discusses how Chang discloses each of the claim limitations in Claims 1-2 and 6. Proposed Rejection 2B discusses how the collective teachings and suggestions in Chang further renders obvious claim limitations in Claims 1-2 and 4-6. Those opinions are incorporated herein to support Proposed

Rejection 2E. Namely, in addition to the reasons discussed above for Proposed Rejection 2B (and incorporated opinions from Proposed Rejection 2A), Chang discloses and/or renders obvious each of claim limitations 1(pre)-1(e) and 1(f)-1(h). For these reasons and those discussed below for limitation 1(d), the combination of Chang in view of Chi discloses or suggests Claim 1 and renders the claim obvious. Ex-03, ¶668.

b. [1.d] a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface;

Proposed Rejection 1A discusses how Chang discloses claim limitation 1(d) ("a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface"). Proposed Rejection 2B discusses how the collective teachings and suggestions in Chang further renders obvious Claims 1-2 and 4-6. Those opinions are incorporated herein to support Proposed Rejection 2E. In addition to those opinions and analysis, for the reasons below and above in this Proposed Rejection 2E, supported by reasoning above provide for Proposed Rejection 2B, the combined teachings and suggestions in Chang and Chi disclose or suggest, and render obvious claim limitation 1(d).[33] Ex-03, ¶¶669-688.

[33] A POSITA would have found it obvious to implement the spacer with a truncated top surface feature in Chang's structure does not mean Chang does not disclose such a feature as claimed in Claim 1— Chang does disclose the claimed spacer for reasons

Proposed Rejection 2B discusses the teachings and suggestions in Chang relating to the implementation of a spacer disposed on two sides of the metal gate, which are incorporated herein. In context of the disclosures in Chang discussed above in Proposed Rejections 2A and 2B, a POSITA would have been aware of the use and benefits of providing spacers on the sidewalls of a metal gate in a semiconductor structure (e.g., provide stability, alignment, etc.) and thus had reasons to consider guidance in the art concerning the formation and implementation of spacers when contemplating the Chang structure. In doing so, a POSITA would have considered the teachings and suggestions in Chi. Ex-03, ¶¶670-680.

Chi discloses a method for forming gate structures for transistors above a semiconductor substrate and contacts on a semiconductor device. PA-05 (Chi), Abstract, 3:48-57. Chi's processes are applicable to planar and non-planar devices, such as FinFETs. PA-05, 1:48-57, 5:42-56, FIGs. 1A-1D; *id.* 9:40-44 ("those skilled in the art will recognize that additional operations need to be performed to complete

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discussed for limitation 1(d) in Proposed Rejection 2A. Rather, as explained above, and consistent with those in Proposed Rejection 2B (further supported by the teachings and suggestions of Chi in context of Chang's teachings), a POSITA would have found it obvious to form and implement spacers with a "truncated top surface" notwithstanding the disclosures in Chang that is addressed above for Proposed Rejection 2A.

the fabrication of the isolation structure 103 (e.g., fill with insulating material and polish) and the rest of steps to complete the FinFET device"). With reference to FIGs. 1E-1F (below) Chi describes processes for forming implant regions during fabrication of a semiconductor device. *Id.*, FIGs. 1E-1F, 4:50-54, 9:13-10:8.

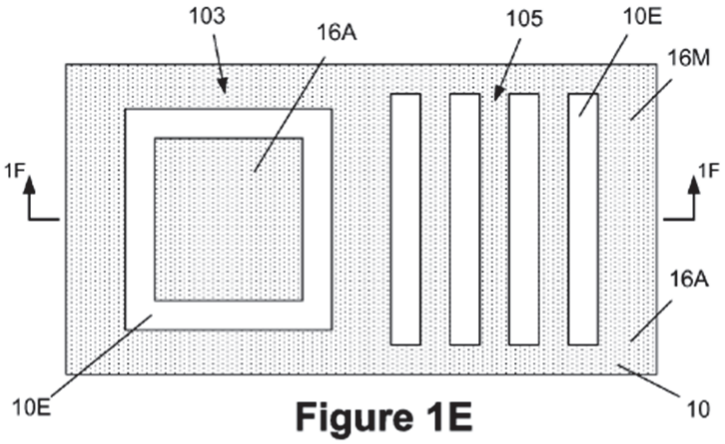

Figure 1E

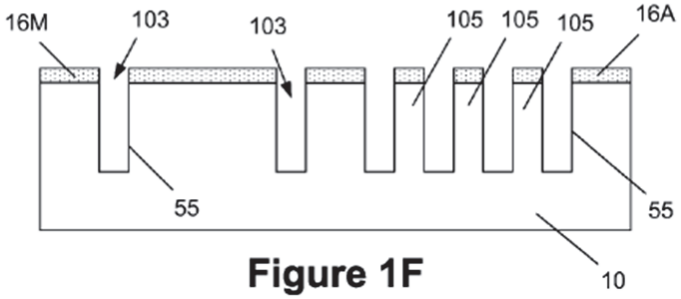

Figure 1F

PA-05 (Chi), FIGs. 1E, 1F.

Chi also discloses processes for forming conductive contact structures and metal silicide regions in the source/drain regions between transistors of a device. *Id.*, 10:9-25, FIGs. 2A-2G. Among other things, Chi discloses that the transistors each comprises a gate structure comprised of one or more conductive gate electrode layers 30B and a gate cap layer 31, and **sidewall spacers 32**. *Id.*, 10:26-40, FIG. 2A. *Id.*,

10:41-11:14 ("sidewall spacers 32 may be formed by performing a conformable deposition process to form a layer of spacer material above the device 100 and thereafter performing an anisotropic etching process").

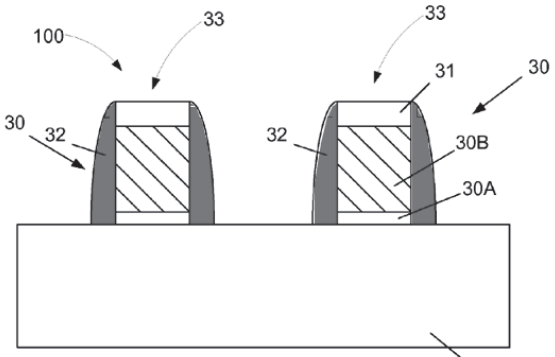

Figure 2A

Chi explains that an etch stop layer 34 is conformably deposited above the device 100 (FIG. 2B) and then a plurality of angle implant processes 40 is perform to implant etch-inhibiting species 40A into portions of the tech stop layer 34 (shown as dots 40A in FIG. 2C below). *Id.*, 11:15-12:5.

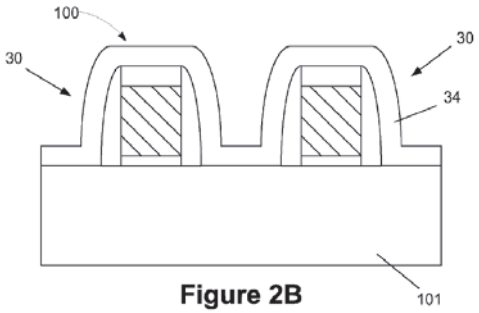

Figure 2B

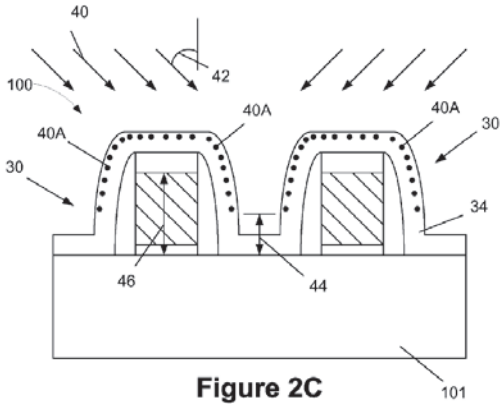

Figure 2C

Chi also discloses methods concerning gate-last techniques in connection with FIGs. 3A-3J. PA-05 (Chi), 13:63-14:9, FIGs. 3A-3B. Chi explains "as shown in

FIG. 3C one or more CMP processes are performed to remove portions of the layer of insulating material 70, the etch stop layer 34 and the gate cap layer. *Id.*, 14:20-24. FIG. 3C below shows the results of such CMP process resulting in sidewall spacers with a truncated top surface. Thus, Chi discloses spacers 32 that have been made shorter by removing a part (including during a planarization process). *See also* PA-05, 14:25-15:9, FIGs. 3C-3E, 15:41-16:60, FIG. 3J, FIG. 3I (below).

Chi also explains "FIGS. 3A-3J depict various specific methods disclosed herein for forming self-aligned contacts for an integrated circuit product" and that "FIG. 3A depicts the device at a point wherein the etch-inhibiting species 40A have been implanted into the etch stop layer 34 as previously described." *Id.*, 13:63-14:9, FIG. 3A. As annotated FIG. 3A below shows, the same spacers (unlabeled in FIG. 3A) is included in the device (shaded).

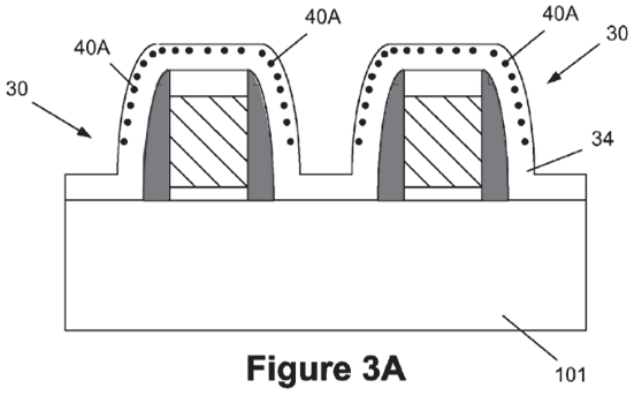

Figure 3A

After an insulating material 70 is formed above the device 100 (as shown in FIG. 3B), which itself may be planarized (*id.*, 14:10-19, FIG. 3B).

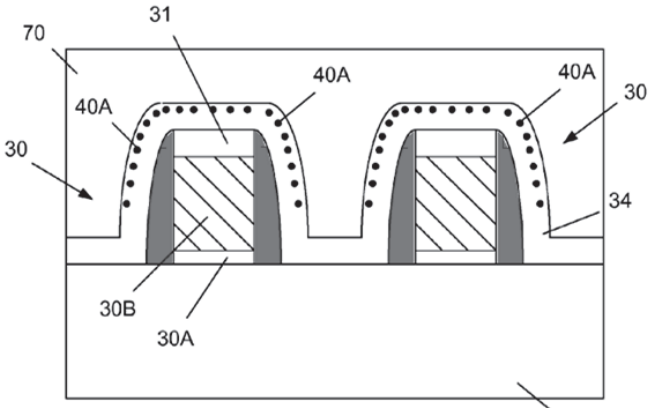

Figure 3B

Chi discloses that "as shown in FIG. 3C **one or more CMP processes** are performed to **remove portions** of the layer of insulating material 70, the etch stop layer 34 and the gate cap layer 31. The process results in the exposure of the gate structure 30 (more specifically the gate electrode 30B) for further processing" (*id.*, 14:20-26). *Id.*, FIG. 3C (annotated below). FIG. 3C below shows the results of such CMP process resulting in sidewall spacers that have been made shorter by removing a part (including during a planarization process) and have a planar top surface. *See also* PA-05, 14:25-15:9, FIGs. 3C-3E, 15:41-16:60, FIG. 3J, FIG. 3I (below); *see also id.*, 14:25-33, FIG. 3D (annotated below).

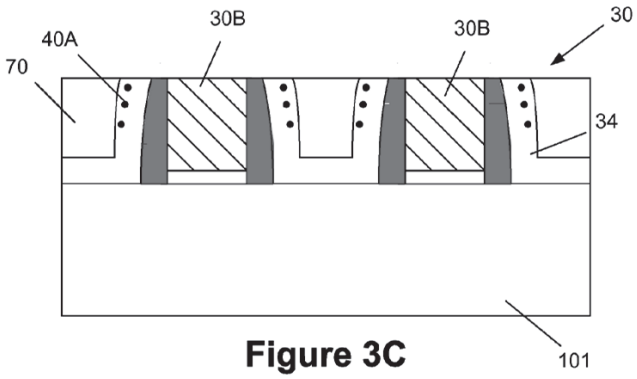

Figure 3C

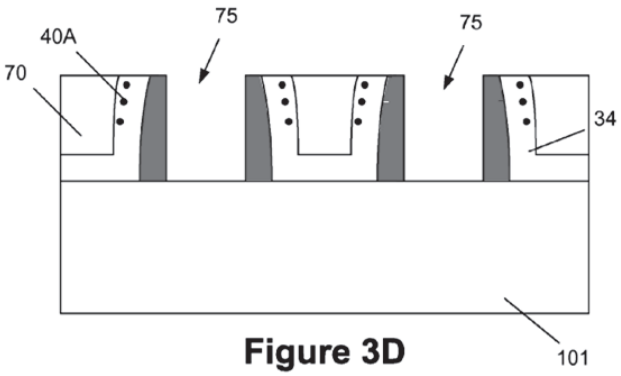

Figure 3D

Chi further discloses [n]ext, as shown in FIG. 3E, replacement gate structures 80 are formed in the gate cavities 75." *Id.*, 14:34-35. Chi also discloses, "[u]ltimately, as shown in FIG. 3E, **one or more CMP processes are performed to remove excess portions of the gate insulation layer, the work-function adjusting layer and the bulk metal layer positioned outside of the gate cavity 75** to define the replacement gate structure 80.

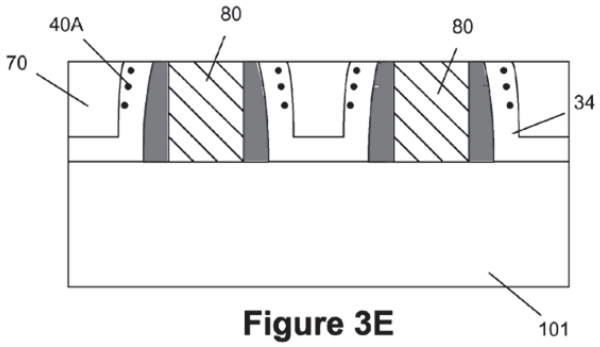

Figure 3E

Chi continues with other processes (FIG. 3F ("ion implant process 90), FIG. 3G (patterned implant mask 84 removal and wet or dry etching process 92), (FIGs. 3H-3J (formation of self-aligned contacts 62 and metal silicide regions 35 for the device 100)). PA-05, 15:10-16:60, FIGs. 3F-3I (FIG. 3I showing structure with

same spacers from FIG. 3C. Figure 3I shows the same spacers from the Figure 3C structure, which have a planar top surface and were made shorter removing a part, during a planarization process (e.g., CMP).

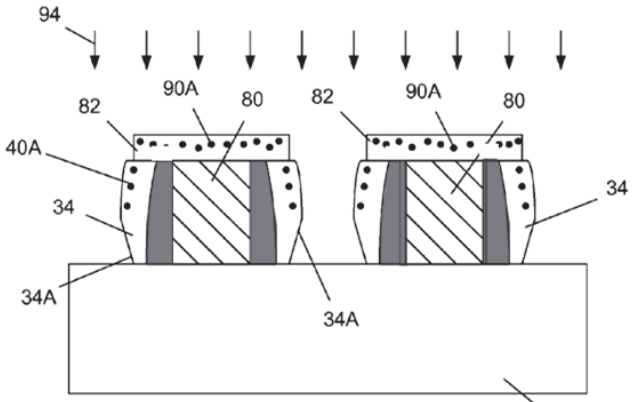

Figure 3I

Thus, Chi discloses or suggests a semiconductor structure including a spacer (e.g., spacer 32) disposed on two sides of a metal gate of the structure, where spacers 32 have a planar top surface that were made shorter by removing a part, including during a planarization process. *See e.g.*, PA-05 (Chi). 11:7-14 ("The sidewall spacers 32 may be formed by performing a conformable deposition process to form a layer of spacer material above the device 100 and thereafter performing an anisotropic etching process. Moreover, as will be appreciated by one skilled in the art after having read the present application, the methods disclosed in FIGS. 2A-2G may be employed on planar field effect transistor devices as well as on three dimensional devices such as FinFET devices"). Also, as explained above, the spacers in Chi's semiconductor structure are made shorter by removing a part of the

spacer material during a planarization process (after being formed) that results in the spacers having a planar top surface. *See e.g.*, PA-05, FIGs. 3C-3I (showing the spacer (unlabeled) that is shortened and having a planar top surface), 14:4-9, 14:20-33 (disclosing CMP processes that are performed "to remove portions" of material and layers resulting the spacers having a planar top surface as shown in FIGs. 3C-3I). Chi therefore a spacer with that was made shorter by removing a part (including during a planarization process) and having a planar top surface, consistent with Interpretations 1-3. *See* §II.D.1; Ex-03, ¶681.

In view of the foregoing, Chi is analogous art. For example, a POSITA would have understood that Chi is in the same field (FETs) and reasonably pertinent to a problem the '747 Patent purports to address (e.g., FET fabrication). *See e.g.*, PA-05 (Chi), 1:5-35, 3:40-57, 3:48-57, 5:39-52, 13:63-14:9; PA-04 (Chang), ¶¶2-6, 10, 45-46, 112, 114-15; Ex-01 ('747 Patent), 1:9-2:9, 2:18-20, 2:39-42, 3:1-25, 5:31-6:37. Indeed, Chi and the '747 Patent disclose features relating to semiconductor devices, structures, and related fabrication processes, including FinFET transistors. *See e.g.*, PA-05, 1:5-35, 3:40-57; Ex-01, 1:5-12, 2:18-20, 2:39-6:37. Accordingly, a POSITA would have had reasons to consider the teachings and suggestions in Chi when contemplating the semiconductor structure of Chang. Ex-03, ¶682.

Namely, a POSITA would have been led by Chang's teachings, (including the description of spacers and the processes involved with their fabrication in context of

the resulting structure in Chang, as discussed for limitation1(d) above in Proposed Rejection 2A) in view of the teachings of Chi to provide spacers in the structure by performing known planarization processes (e.g., CMP) on the spacers (after being disposed on the sides of the metal gate). *See e.g.,* PA-04 (Chang), FIGs. 17-23, 24-27, ¶¶52, 89 94-95; Ex-03, ¶683. Such processes would remove material and provide a planar top surface like the top surface of the spacers taught by Chi. Such a modification and implementing would have predicably resulted in the Chang structure including a spacer disposed on two sides of a metal gate that was made shorter by removing a part of the spacer during a planarization process (e.g., CMP). Such a spacer would have a planar top surface like that shown by Chi. *See* discussion of Chi above this in Proposed Rejection 2E.

Chi's teachings are consistent with the use of a POSITA's state of art knowledge at the relevant time of the use and implementation of spacers that were subject to planarization process during semiconductor device fabrication, that results in the spacer being made shorter by removing a part of the spacer (including during a planarization process) and ultimately having a planar top surface in the resulting structure. *See e.g.*, PA-06 (Sell), 3:23-30 ("A polishing process 123 may subsequently be performed, such as a chemical mechanical polishing (CMP) process, for example, to remove the first contact metal 120 (FIG. 1f) and the stopping layer 112."), FIG. 1e. *See also* discussion of Sell in Proposed Rejections 2C-2D.

Guided by the teachings in Chi in context of Chang's teachings and a POSITA's state of art knowledge at the relevant time, a POSITA would have found it obvious to form the spacers in Chang's structure by removing material from the spacers' top surface (after the spacers were formed) by known planarization processes (e.g., CMP) in order to provide a planarized top surface spacer structure like that shown in the resulting structure of Chang. Such an implementation would have predictably resulted in spacers having a truncated top surface consistent with Interpretation 1 (planar top surface), and Interpretations 2 and 3 (made shorter by removing a part of the spacer (during a planarization process). *See* §II.D.1; Ex-03, ¶¶683-685.

A POSITA would thus have found it obvious to implement spacers having a truncated top surface consistent with the teachings of Chi in the structure of Chang discussed above for Claim 1 in Proposed Rejection 2B. For example, a POSITA would have recognized and understood that sidewall spacers were well-known and used in semiconductor structures like Chang's structures. Indeed Chang discloses spacers, *see* Proposed Rejection 2A (limitation 1(d)), and likewise recognized advantages in planarizing such structures to provide a flat surface or a co-planar surface with other layers/material upon which other material or layers can be formed and consequently further subsequent processing, including photolithography, to be more reliably performed. The teachings of Chi are consistent with known uses and

formations of spacers, and the subsequent planarization processes to provide a planar top surface in semiconductor structures consistent with that described by Chang. In performing such planarization (like that described by Chi), a POSITA would have understood that the spacer is made shorter by removing a part (during a planarization process) resulting in a spacer with a planar top surface in the resulting structure similar to that described by Chi, (which includes structures with planarized top surfaces formed via CMP processes). Ex-03, ¶686.

A POSITA would have had a reasonable expectation of success in implementing the above modification/configuration to the spacers disposed on the sides of the metal gate in Chang's structure. A POSITA would have appreciated and been led by Chi's teachings relating to known fabrication processes and semiconductor device structures, including spacers on two sides of metal gate structures where the spacers having a planar top surface similar to that described Chi. Moreover, a POSITA would have reasonably expected success in implementing such a modification/configuration because providing a spacer with a planar top surface would have involved nothing more than applying a standard semiconductor manufacturing process (e.g., deposition, CMP, etc. similar to that taught by Chi) for providing the spacer on the sides of metal gates, where the spacer (once formed) was planarized to provide a planar top surface consistent with that known in the art and disclosed by Chi. A POSITA would have leveraged their state

of art knowledge and experience in considering the design needs and the market demands for the applications of the semiconductor structure as contemplated by Chang and thus would have been motivated to configure and design fabrication processes to successful provide such a spacer in the Chang structure with a "truncated top surface" (as interpreted under Interpretations 1-3, *see* §II.D.1). Ex-03, ¶687; *KSR*, 550 U.S. at 416.

For the reasons above, Chang in view of Chi renders obvious claim 1 and thus the claim is invalid in view of that prior art combination.

c. Claim 2: The semiconductor device of claim 1, further comprising a second dielectric layer disposed on the first dielectric layer.

As explained for Proposed Rejection 2A, Chang discloses the semiconductor device of claim 1, further comprising a second dielectric layer disposed on the first dielectric layer, as recited in claim 2. Ex-03, ¶¶689-691.

Where, for example, "the semiconductor device of claim 1" is the SRAM described above this in Proposed Rejection 2B, Chang discloses a second dielectric layer disposed on the first dielectric layer, as recited in claim 2 for the same reasons discussed in Proposed Rejection 2A. Any modification to the SRAM discussed in Proposed Rejection 2B, Claim 1 (to the extent any modification is deemed necessary) would not affect Chang's disclosure of Claim 2. For example, a POSITA would have understood that no proposed or perceived modification to the SRAM

discussed in Proposed Rejection 2B, claim 1 would change or otherwise affect the fact that Chang's ILD layer 1510 is disposed on layer 1503 even in the structure discussed here for Proposed Rejection 2B.

Thus, for reasons similar to those discussed above for Proposed Rejection 2A (Claim 2) and those for Proposed Rejection 2B (Claims 1-2 and 4-6), Chang in view of Chi discloses and/or suggests, and renders obvious, Claim 2 of the '747 Patent and thus the claim is invalid under the combination. Ex-03, ¶691.

d. Claim 3: The semiconductor device of claim 2, further comprising an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface.

Proposed Rejection 2A discusses how Chang discloses the limitations in Claims 1-2 and 6. Proposed Rejection 2B discusses how the collective teachings and suggestions in Chang further renders obvious Claims 1-2 and 4-6. Those opinions are incorporated herein to support Proposed Rejection 2E. In addition to the analysis in Proposed Rejection 2A (which is incorporated herein), for the reasons below and above this in Proposed Rejection 2E, the combined teachings and suggestions in Chang and Chi disclose or suggest and render obvious Claim 3. Ex-03, ¶¶692-727.

In particular, a POSITA would have found it obvious to implement an etching stop layer having a truncated top surface and disposed on two sides of the metal gate in the Chang structure. Ex-03, ¶¶693-694.

Chang's teachings were discussed above for Claim 1 in Proposed Rejection 2A (incorporated herein). For example, as discussed for Claim 1, Chang discloses metal gates in the structure (e.g., gates 1441, 1443, 1446, 1596, 1597). PA-04 (Chang), FIGs. 24, 27. Chang's gates include a "silicon nitride protection layer." *See* PA-04, ¶114. A POSITA would have understood such a layer as an "etch-stop layer for self-aligned contact application." *See* Ex-15 (Xiao), 164-65, FIG. 5.64.

Such teachings in context of Chang's collective teachings would have led a POSITA to consider options for protecting material and structures during fabrication of its semiconductor device. Moreover, a POSITA was familiar with and aware that contact etching stop layers (CESLs) and similar etching stop layers were commonly used and known semiconductor structural elements used in the fabrication of semiconductor devices, including those described by Chang. Accordingly, a POSITA would have had reasons to consider teachings from the prior art. Chi is an example of such teachings that would have guided a POSITA at the relevant time. Ex-03, ¶694.

As discussed above, Chi discloses and/or suggests the use of an etching stop layer (e.g., etch stop layer 34) disposed on two sides of the metal gate (e.g., the metal

gate in gate electrodes, e.g., 30B), where the etching stop layer has a truncated top surface as claimed and interpreted under Interpretations 1-3. *See* §II.D.1; Ex-03, ¶¶695-696. For example, as explained in further detail below, Chi discloses depositing an etch stop layer 34, 34A (e.g., FIGs. 3A-3J) on two sides of metal gate and subsequently planarizing the layer thus making it shorter by removing apart (during a planarization process) resulting in the etching stop layer 34 having a planar top surface. *See e.g.*, PA-05, FIGs. 3A-3J (showing the etch stop layer that is shortened and having a planar top surface), 14:4-9, 14:20-33 (CMP processes performed "to remove portions" of material and layers resulting the etch stop layer 34 having a planar top surface as shown in FIGs. 3C-3J). Chi therefore provided guidance to a POSITA of the known use and implementation of an etching stop layer disposed on two sides of the metal gate, where the etching stop layer has a planar top surface and was made shorter by removing a part (including during a planarization process).

Specifically, Chi's teachings were discussed above for limitation [1.d] in this Proposed Rejection 2E (incorporated herein). As discussed in limitation [1.d], Chi discloses an etching stop layer (e.g., etch stop layer 34) disposed on two sides of the metal gate (e.g., the metal gate in gate electrodes, e.g., 30B), where the etching stop layer has a truncated top surface as claimed and interpreted under Interpretations 1-3. *See* §II.D.1; PA-05, 14:4-9, 14:20-33, FIGs. 3A-3J; Ex-03, ¶697.

As explained above for limitation 1(d) in this Proposed Rejection 2C, Chi is analogous art. For example, a POSITA would have understood that Chi in the same field (MOSFETs) and reasonably pertinent to a problem the '747 Patent purports to address (e.g., MOSFET fabrication). *See e.g.*, PA-05 (Chi), 1:5-35, 3:40-57, 3:48-57, 5:39-52, 13:63-14:9; Ex-01 ('747 Patent), 1:9-2:9, 2:18-20, 2:39-42, 3:1-25, 5:31-6:37. Indeed, Chi and the '747 Patent disclose features relating to semiconductor devices, structures, and related fabrication processes, including FinFET transistors. *See e.g.*, PA-05, 1:5-35, 3:40-57; Ex-01, 1:5-12, 2:18-20, 2:39-6:37. Accordingly, a POSITA would have had reasons to consider the teachings and suggestions in Chi when contemplating the semiconductor structure of Chang's. Ex-03, ¶¶697-708.

Upon considering Chi in context of their state of art knowledge, a POSITA would have recognized and appreciated the teachings and guidance concerning the implementation of an etching stop layer 34 and thus been motivated to modify or configure Chi structure to include an etching stop layer that is disposed on two sides of a metal gate that was planarized during a planarization process (e.g., CMP) during fabrication where the resulting structure has an etching stop layer with a planar top surface and was made shorter by removing a part during the planarization process (i.e., has a truncated top surface under the various constructions addressed above). Ex-03, ¶709.

A POSITA would have been motivated to modify Chang's structure with an etching stop layer disposed on two sides of the metal gate where the layer has a truncated top surface (per Interpretations 1-3, *see* §II.D.1) to provide the protective benefits of etch stop layers consistent with that known in the art and suggested by Chi. Ex-03, ¶710.

For example, a POSITA would have been led by Chang's teachings in view of the above teachings of Chi to provide an etching stop layer disposed on two sides of the metal gate by performing known planarization processes (e.g., CMP) on the etching stop layer formed on the substrate (between the gate stack structures) that would remove material from the top surface of the etch stop layer along with other structures or layers subject to the planarization (e.g., CMP) processes, consistent with the teachings of Chi. Such a modification and implementing would have predicably resulted in the FIG. 27 structure including an etching stop layer that is disposed on two sides of a metal gate in a gate stack structure 308 that was made shorter by removing a part of the etching stop layer (that was previously formed) during a planarization process (e.g., CMP), consistent with the features disclosed and contemplated by Chi.

Chi's teachings are consistent with the known use of an etching stop layer having a truncated top surface as understood by those of ordinary skill in the art at the time in context of the '747 Patent disclosures. *See e.g.,* Ex-01 ('747 patent),

3:19-25 (explaining that CESL 20 (with a truncated top surface formed by a planarization process and having a planar top surface like that shown in Figure 1), and "manufacturing methods thereof" was "well known to persons of ordinary skills in the art"). Indeed, the '747 Patent suggests that such features were so "well known" that "details" need not be described to understand such features. *Id.*

Chi's teachings are also consistent with a POSITA's state of art knowledge at the relevant time of the use and implementation of etching stop layers in the fabrication of semiconductor devices (like those of Chang), including those that were subject to planarization process during fabrication, that results in the layer being made shorter by removing a part (including during a planarization process) and ultimately having a planar top surface in the resulting structure. Ex-03, ¶¶713-714.

For example, Huang (PA-03) discloses a Contact Etch Stop Layer (CESL) 36 that is a dielectric material acting as "an etch stop layer" disposed on two sides of a gate dielectric 24 and gate electrode 26. *See e.g.,* PA-03, ¶¶8-10, 14, FIG. 1 (below).

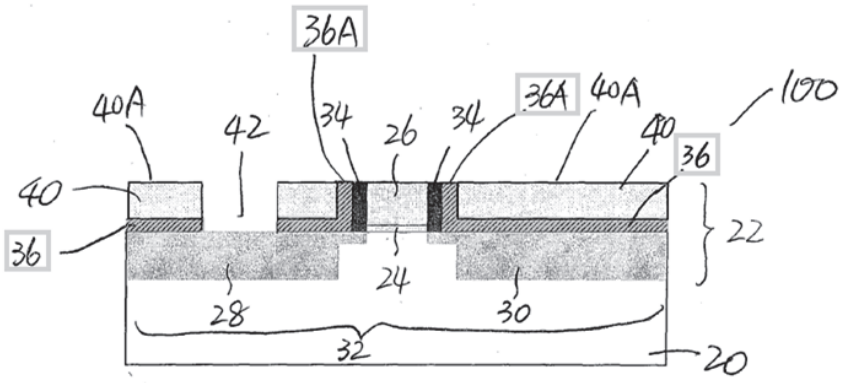

Fig. 1

A POSITA would have understood that CESL 36 is an etch stop layer to protect source/drain region (30) against etching of an opening (56) so etching stops on CESL 36, as shown in FIG. 6 (below). Ex-03, ¶¶715-717.

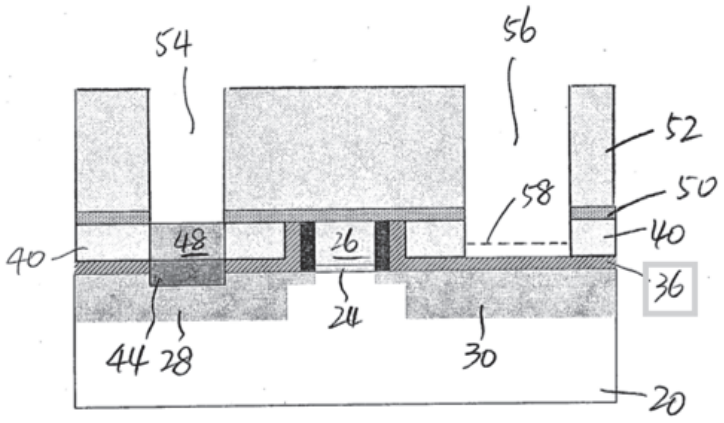

Fig. 6

As shown and described, Huang's etching stop layer 36 has top edges 36A that are planar, that were formed by CMP processes during Huang's last gate

approach processes. *See e.g.*, PA-03, ¶9. *See also* Ex-15 (Xiao), 544-545 (describing such an approach known at the relevant time).

As another example, Liang (Ex-27) similarly confirms the known use of etching stop layers in semiconductor structures similar to that disclosed by Chi. *See* Ex-27, FIGs. 1A-1H, 2:50-65 ("An etch-stop layer 107 can be formed over the substrate 101 and adjacent to sidewalls of the gate electrode 103"), 3:20-41, 4:5-17 ("The etch- stop layers 107 and 111 can have at least one material such as silicon carbide (SiC), silicon nitride (SiN), silicon carbon nitride (SiCN), silicon carbon oxide (SiCO), silicon oxynitride (SiON), boron nitride (BN), boron carbon nitride (BCN), other material that has a desired selectivity with respect to silicon oxide, or any combinations thereof. The etch- stop layers 107 and 111 can be formed by any suitable process …"). *See also id.*, 1:56-2:23.

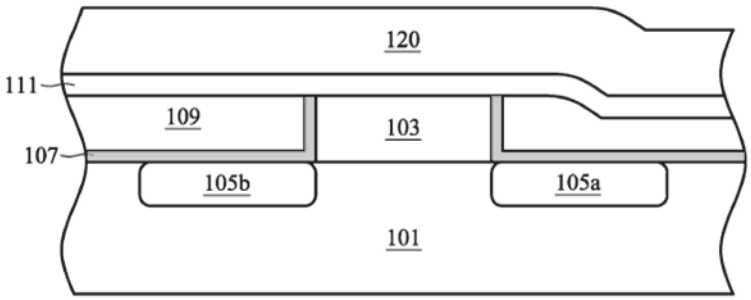

FIG. 1A

These teachings are consistent with the state of art knowledge of etching stop layers, including those that were made shorter by removing a part (including during

a planarization process) and having a planar top surface as understood by a POSITA at the relevant time. Ex-03, ¶718.

In light of the guidance by Chi in context of Chang and a POSITA's state of art knowledge at the relevant time, a POSITA would have found it obvious to include an etching stop layer in the fabrication and resulting structure of Chang's structure to provide etch protection to structural elements and layers in the fabrication of the structure. A POSITA would have been motivated by Chang's use of similar layers (e.g., silicon nitride protection layer) and in light of Chi, would have looked to provide such conventional features in Chang's structure to ensure the selective etching processes used to fabricate the resulting structure results in an operational semiconductor device that performs in accordance with the appropriate application of the device. Ex-03, ¶¶719-720.

In light of such teachings of Chi, Chang, and state of art knowledge, a POSITA would have been motivated and found obvious to form and process an etching stop layer disposed on two sides of the metal gate by removing material from the etching stop layer's top surface using known planarization processes (e.g., CMP) in order to provide a planarized top surface spacer structure consistent with structures shown in the resulting structure of Chang. Such an implementation would have predictably resulted in an etching stop layer having a truncated top surface as claimed and consistent with Interpretation 1 (planar top surface), and Interpretations

2 and 3 (made shorter by removing a part (during a planarization process). *See* §II.D.1.

A POSITA would have recognized and understood that etching stop layers spacers were well-known and used in semiconductor structures like Chang's structures, and likewise recognized advantages in using such layers. For example, a POSITA would have appreciated an etching stop layer beneficially provided protection to, for example, transistor gate structures, source/drain regions, and other structural elements in semiconductor structures, like those in Chang's structure. *See e.g.*, Ex-15 (Xiao), 164-65, 341-45; Ex-03, ¶721.

A POSITA would have also appreciated the benefits in providing an etching stop layer with a planar top surface because, for example, such planarized top surfaces were known to aid in the formation of subsequently formed structural elements and layers during subsequent fabrication processes (e.g., photolithography steps) that deposit such elements or layers on the top surface of the planarized surface. Accordingly, a POSITA would have been motivated to look to ways to provide such protection, as taught by Chi and known in the art. Ex-03, ¶722.

Thus, having recognized that the teachings of Chi is consistent with such known use and formation of etching stop layers with planar top surfaces (formed by known processes (e.g., CMP) during fabrication of semiconductor structures is consistent with features known in the art, a POSITA would have been motivated to

implement such features, and done so with a reasonable expectation of success, in the semiconductor structure of Chang. Such a POSITA would have thus looked to protect features in the structure during fabrication (e.g., S/D regions, other components/materials) while promoting the formation of other structures and layers formed during subsequent fabrication process in the formation of the resulting structure of Chang. Ex-03, ¶723.

A POSITA would have reasonably expected success in implementing the above modification/configuration because providing an etching stop layer with a planar top surface would have involved nothing more than applying known semiconductor manufacturing process (e.g., deposition, CMP, etching, etc.) for forming the etching stop layer on the sides of Chang's metal gates, where the etching stop layer (after formation) was planarized to provide a planar top surface that provided a protective surface conducive to subsequent formation of other structures and layers formed above. Designing, configuring, and implementing such an etching stop layer in the Chang structure would have been within the skill, knowledge, and capabilities of a POSITA at the relevant time, as described by Chi (and the state of art references discussed above, which are consistent with a POSITA's state of art knowledge on the use of etch stop layers in semiconductor structures similar to Chang). Ex-03, ¶724.

A POSITA would have leveraged their state of art knowledge and experience in considering the design needs and the market demands for computing devices that include a semiconductor structure as contemplated by Chang, and thus would have been motivated to design and configure fabrication processes to successfully provide such an etching stop layer in Chang's structure with a "truncated top surface" (as interpreted under Interpretations 1-3, *see* §II.D.1). Ex-03, ¶725.

Accordingly, for the reasons above, the combination of Chang and Chi discloses and/or suggests the semiconductor structure (as Discussed above for Claim 1) including an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface as recited in Claim 3 (under as interpreted under Interpretations 1-3 of "truncated top surface," *see* §II.D.1). Ex-03, ¶¶726-727.

For the reasons above, Chang in view of Chi renders obvious Claim 3 and thus the claim is invalid in view of that prior art combination.

e. Claim 4: The semiconductor device of claim 2, wherein the first contacts disposed in the first dielectric layer and in the second dielectric layer and each first contact is a monolithically formed structure.

Claim 5: The semiconductor device of claim 2, wherein the second contacts disposed in the first dielectric layer and in the second dielectric layer and each second contact is a monolithically formed structure.

As explained for Proposed Rejection 2A, Chang discloses the semiconductor device of claim 1, comprising first and second contacts disposed in the second dielectric layer, as recited in limitations (1f) and (1g) of Claim 1. Where, for example, "the semiconductor device of claim 1" is the SRAM described above in Proposed Rejection 2B, Chang discloses monolithically formed first and second contacts disposed in the second dielectric layer, as recited in claims 4-5. Any modification to the SRAM discussed in Proposed Rejection 2B, Claim 1 (to the extent any modification is deemed necessary) would not affect Chang's disclosure of Claims 4-5. For example, a POSITA would have understood that no proposed or perceived modification to the SRAM discussed in Proposed Rejection 2B, claim 1 would change or otherwise affect the fact that Chang's self-aligned contacts 1670, 1671, 1675 are monolithically formed and disposed in ILD layer 1503 (Claims 4-5) even in the structure discussed here for Proposed Rejection 2C. Ex-03, ¶¶728-729.

Thus, for reasons similar to those Discussed above for Proposed Rejection 2A (Claims 1, 2 and 6) and those for Proposed Rejection 2B (Claims 1-2 and 4-6), Chang

in view of Chi discloses and/or suggests, and renders obvious, Claims 4-5 of the '747 Patent and thus the claims are invalid under the combination. *Id.*

f. Claim 6: The semiconductor device of claim 1, further comprising at least one fin structure disposed on the substrate.

Proposed Rejection 2A above discusses how Chang discloses the limitations in Claim 6. Proposed Rejection 2B discusses how the collective teachings and suggestions in Chang further renders obvious the limitations in Claim 6. Those opinions are incorporated herein to support Proposed Rejection 2E. For those reasons, and those that are discuss in this Proposed Rejection 2E, Chang in view of Chi discloses and/or renders obvious Claim 6 of the '747 Patent. Such features would have been included in the Chang and Chi combination that is discussed here in this Proposed Rejection 2E. A POSITA would have had the same rationale, expectation of success, and motivation, and similarly found obvious in view Chang's collective teachings, to include at least one fin structure disposed on the substrate of the Chang semiconductor substrate (that is discussed for Claim 1 in Proposed Rejection 2B (and incorporated Proposed Rejection 2A). Accordingly, the

combination of Chang in view of Chi as discussed in this Proposed Rejection 2E likewise discloses or suggests Claim 6.[34] Ex-03, ¶¶730-740.

A POSITA considering the semiconductor structure disclosed by Chang would have been motivated to look to and consider teachings in the art for ways to improve the semiconductor device structure through implementation of FinFET or tri-gate technologies to promote the application of the structure in the types of computing devices contemplated by Chang. In doing so, a POSITA would have considered the teachings and suggestions in Chi. Ex-03, ¶731.

Chi discloses a method for forming gate structures for transistors above a semiconductor substrate and contacts on a semiconductor device. PA-05 (Chi), Abstract, 3:48-57. Chi's processes are applicable to planar and non-planar devices, such as FinFETs. PA-05, 1:48-57, 5:42-56 ("As will be readily apparent to those skilled in the art upon a complete reading of the present application, the present

[34] A POSITA would have found it obvious to implement Chang's structure with at least one fin structure disposed on the substrate does not mean Chang does not disclose such a feature as claimed in Claim 6—Chang does disclose the claimed fin structure for reasons Discussed for Claim 6 in Proposed Rejection 2A. Rather, as explained here, supported by the teachings and suggestions of Chang (including in context of Chi as applied for Claim 1), a POSITA would have found it obvious to form and implement a fin structure as claimed in Chang's structure notwithstanding the disclosures in Chang that I address above for Proposed Rejection 2A.

method is applicable to a variety of devices (e.g., planar devices and **non-planar devices such as FinFETs**) and technologies, e.g., NFET, PFET, CMOS, etc., and is readily applicable to a variety of integrated circuit products, including, but not limited to, ASIC's, logic devices, memory devices, etc."), FIGs. 1A-1D; *id.* 9:40-44 ("those skilled in the art will recognize that additional operations need to be performed to complete the fabrication of the isolation structure 103 (e.g., fill with insulating material and polish) and the rest of steps to complete the FinFET device"), 13:63-14:9 ("Moreover, as will be appreciated by one skilled in the art after having read the present application, the methods disclosed in FIGS. 3A-3J may be employed on planar field effect transistor devices as well as on three dimensional devices such as **FinFET** devices"). Ex-03, ¶732.

As discussed above, Chi is analogous art. For example, a POSITA would have understood that Chi in the same field (MOSFETs) and reasonably pertinent to a problem the '747 Patent purports to address (e.g., MOSFET fabrication). *See e.g.*, PA-05 (Chi), 1:5-35, 3:40-57, 3:48-57, 5:39-52, 13:63-14:9; Ex-01 ('747 Patent), 1:9-2:9, 2:18-20, 2:39-42, 3:1-25, 5:31-6:37. Indeed, Chi and the '747 Patent disclose features relating to semiconductor devices, structures, and related fabrication processes, including FinFET transistors. *See e.g.*, PA-05, 1:5-35, 3:40-57; Ex-01, 1:5-12, 2:18-20, 2:39-6:37. Accordingly, a POSITA would have had reasons to consider the teachings and suggestions in Chi when contemplating the

semiconductor structure of Chang's structure. Upon considering Chi, a POSITA would have recognized and appreciated the teachings and guidance concerning the implementation of FinFET or tri-gate technologies consistent with those taught by Chang, and thus been motivated to modify or configure Chang's structure with such multi-gate devices having at least one fin structure disposed on the substrate. Ex-03, ¶733.

Chi's teachings are consistent with those of Pethe, and consistent with the state of art knowledge of a POSITA at the relevant time regarding the types of field effect transistors commonly used, including non-planar FETs. Indeed, a POSITA would have been knowledgeable of the use and implementation of planar and fin-shaped FETs, and the similarities between them (e.g., channel, source/drain regions, gates, etc.). Indeed, as explained for Claim 6 in Proposed Rejection 2B, a POSITA would have been knowledgeable of the use and implementation of planar and fin-shaped FETs, and the similarities between them (e.g., channel, source/drain regions, gates, etc.). A number of state of the art references provide disclosures consistent with a POSITA's knowledge at the time. *See e.g.*, Ex-18 (Sze), 433-34, 438, FIGs. 3, 6; Ex-07 (Neamen), xxiii, 403-405, FIGs. 0.5, 10.34, 10.35; Ex-09 (Wolf), 3, 6; Ex-15 (Xiao), 72-74, 351, 370-371, FIGs. 3.20, 9.31, 10.2; Ex-28 (Lin), 7:54-60, 10:17-23, 12:51-56, 16:35-41; Ex-35 (Chi, 2012), 1; Ex-29 (Ranade), ¶¶ [0025], [0044]; Ex-30 (Hu), Abstract, 2:11-14 (FinFETs are "an extension of conventional

planar MOSFET technology"), 5:37-40 (FinFETs fabrication "is compatible with conventional planar MOSFET fabrication techniques"); Ex-31 (Doyle), 133 (a FinFET "very much resembles [a] bulk transistor from the processing point-of-view"); Ex-32 (Simonelli), ¶¶ [0001], [0003], [0004], [0044], [0045]; Ex-33 (Chau), 2:38-41, 5:3-26, 6:35-50; Ex-34 (Chang), 2:61-3:3. Further, a POSITA would have appreciated and recognized the benefits of implementing the Chang structure as a non-planar structure with a multi-gate or FinFET transistor, such as scaling to minimize the footprint of the integrated circuit implementing such transistors. *See* Ex-15 (Xiao), FIG. 15.1, 650-51; Ex-03, ¶734.

Such knowledge coupled with the collective teachings and suggestions in Chang and Chi (discussed above for Claim 6 in Proposed Rejection 2B), would have led a POSITA to configure the Chang's structure in context of a multi-gate or FinFET transistor device including at least one fin structure disposed on the substrate of the structure. Ex-03, ¶735.

A POSITA was well aware of, and had experience with, FinFET type transistor devices and related structures consistent with those contemplated by Chang and Chi. Indeed, for example, FinFET devices were well known to include fin structures, like that described by Chi. *See also e.g.*, Ex-15 (Xiao), 72-74, 351; Ex-03, ¶736.

A POSITA would have appreciated and recognized the benefits of implementing the structure of Chang as a non-planar structure with a tri-gate or FinFET transistor, such as scaling to minimize the footprint of the integrated circuit implementing such transistors. PA-05 (Chi), 3:48-57, 5:39-52, 11:10-14, 14:5-9, 18:13-14. *See also* Ex-15 (Xiao), FIG. 15.1, 650-51 (describing features consistent with a POSITA's state of art knowledge at the relevant time such as the known use of "a trigate, [where] fabs can use the same lithographic technology to reduce transistor dimensions while maintaining the same performance, or to improve device performance without increasing device density" and where "IC manufacturers can further improve device performance by making the fin taller" and that "a finFET is easier to build than a trigate. Intel's 22-nm IC chips are built with trigate devices"). Ex-03, ¶737.

In light of such knowledge and experience, and in context of Chang's and Chi's teachings and suggestions, a POSITA would have been motivated to configure the Chang structure with a fin structure disposed on top of the substrate, consistent with known Fin-FET and tri-gate transistor semiconductor structure configurations at the relevant time and taught by Chi. Ex-03, ¶738.

A POSITA's knowledge and experience in context of the teachings and suggestions of Chi and Chang would have led them to implement such fin structure features in the Chang structure with a reasonable expectation of success that the

semiconductor structure would provide functional transistor operations consistent with the application of the structure in the various types of computing devices that Chang contemplates. For instance, a POSITA would have recognized that implementing such features would have involved applying known semiconductor fabrication processes and structural elements (e.g., FinFETs, tri-gate transistors and related fabrication processes like those taught by Chi and Chang) that were within the capabilities and knowledge of a POSITA at the relevant time. Indeed, as explained above, Chi expressly discloses semiconductor structures with fin structures (PA-05 (Chi), 3:48-57, 5:39-52, 11:10-14, 14:5-9, 18:13-14), thus guiding a POSITA to integrate the same with the Chang structure. Ex-03, ¶739. Also, a POSITA would have considered the design needs for such applications, relevant market demands, and related factors and thus found implementing Chang's structure as a FinFET or tri-gate type device, especially in view of the guidance in Chi. *Id.*

Accordingly, in view of the combined teachings and suggestions of Chang in view of Chi, a POSITA would have found it obvious to configure the structure to include at least one fin structure disposed on the substrate of the structure, as recited in Claim 6 of the '747 Patent. Thus, for the reasons here, and those further above for Proposed Rejection 2B, Chang and Chi discloses and/or suggests, and renders obvious Claim 6 of the '747 Patent, rendering the claim invalid. Ex-03, ¶740.

g. Claim 7: The semiconductor device of claim 1, further comprising a salicide layer disposed between each S/D region and each first contact.

Proposed Rejection 2A discusses how Chang discloses the limitations in Claims 1-2 and 6. The discussions in Proposed Rejections 2A and 2B are incorporated herein for Proposed Rejection 2E. Additionally, for the reasons below and above in this Proposed Rejection 2E, the combined teachings and suggestions in Chang and Chi disclose or suggest, and render obvious Claim 7. Further, for brevity, in Proposed Rejection 2C, it was discussed that a POSITA would be motivated to configure the self-aligned contacts 1670, 1671 in Chang's FIG. 27 to include a salicide layer that is disposed between each S/D diffusion region 1600 and each self-aligned contacts 1670, 1671. Those discussions are incorporated herein and will not be repeated here. Ex-03, ¶¶741-756.

A POSITA would have would have been motivated to implement in Chang's structure a self-aligned silicide ("salicide") layer disposed between each S/D region and each first contact in view Chi. Ex-03, ¶742.

Understanding that the use of a salicide layer between a source/drain region and contact would advantageously create a more conductive contact , and that such features were widely known in the art at the time, and that Chang's semiconductor structure includes a source/drain region and corresponding contact (*see* Proposed Rejection 2A, limitations 1(e)-1(f)), a POSITA would have had reasons to consider

ways to likewise improve Chang's structure. Ex-03, ¶743. To do so, a POSITA would have looked to teachings in the art to supplement and/or complement their knowledge and experience pertaining to the fabrication and implementation of semiconductor structures. *Id.* A POSITA would have found Chi to provide insight that would have led a POSITA to implement a salicide layer between a source/drain and the contacts in the structure of Chang to enhance or establish conductive surfaces to the semiconductor device. *Id.*

In particular, a POSITA would have appreciated that Chi discloses a method for forming gate structures for transistors above a semiconductor substrate and contacts on a semiconductor device. PA-05 (Chi), Abstract, 3:48-57; Ex-03, ¶744. Among other features, Chi describes formation of conductive contact structures and metal silicide regions in the source/drain regions between transistors of a device. PA-05, 6: 26-35, FIG. 2A. The transistors comprise a gate structure including conductive gate electrode layer[s] 30B and a gate cap layer 31, and sidewall spacers 32. *Id.*, 6:35-40, 11:7-14. Chi also discloses methods concerning gate-last techniques in connection with Figures 3A-3J. PA-05, 13:63-14:9, FIGs. 3A-3B. Chi explains "as shown in FIG. 3C one or more CMP processes are performed to remove portions of the layer of insulating material 70, the etch stop layer 34 and the gate cap layer. *Id.*, 14:20-24; Ex-03, ¶¶744-747.

Relevant here, and consistent with known semiconductor devices employing transistors (e.g., FinFETs, etc.), Chi discloses a silicide layer between source/drain regions and contacts for the source/drain regions. *See e.g.*, PA-05 (Chi), 15:41-43 ("With reference to FIGS.3H-3J, the next sequence of operations involves the formation of the conductive self-aligned contacts 62 and metal silicide regions 35 for the device 100"), FIGs. 3H-3J. Chi also discloses with reference to FIG. 3J "as shown in FIG. 3J, metal silicide regions 35 are formed in the source/drain regions of the device 100." *Id.*, 16:57-60. FIG. 3J (below).

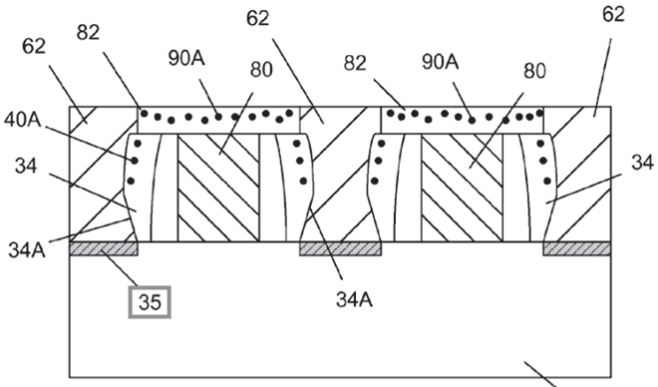

Figure 3J

Chi also teaches the known use of a silicide layer between source/drain regions and contacts elsewhere. *See e.g., id.*, 10:25-31 (Chi discussing FIG. 2A where "the next major activity to be performed involves the formation of conductive contact structures and metal silicide regions in the source/drain regions of the device 100"), 13:30-33 ("as shown in FIG. 2G, metal silicide regions 35 are formed in the source/drain regions of the device 100 an a plurality of conductive self-aligned

contacts 62 are formed in the openings 50A in the layer of insulating material 50"); *see also id.*, 13:33-50.

A POSITA would have understood that Chi' silicide 35 is a salicide layer consistent with that known in the art. For instance, as explained, Chi's silicide is formed by a process whereby a refractory metal is deposited, and upon heating, selectively forms a refractory metal silicide in the regions where the deposited refractory metal was in contact with a silicon containing material. *See* PA-05 (Chi), 13:30-50. Because the silicide formation is in the regions where the refractory metal was in contact with the silicon containing material, this silicide formation is a self-aligned process (e.g., process achieved without photolithography). The result is a self-aligned silicide or "salicide." Ex-03, ¶748.

As explained above for limitation 1(d) in this Proposed Rejection 2E, Chi is analogous art. For example, a POSITA would have understood that Chi in the same field (MOSFETs) and reasonably pertinent to a problem the '747 Patent purports to address (e.g., MOSFET fabrication). *See e.g.*, PA-05 (Chi), 1:5-35, 3:40-57, 3:48-57, 5:39-52, 13:63-14:9; Ex-01 ('747 Patent), 1:9-2:9, 2:18-20, 2:39-42, 3:1-25, 5:31-6:37. Indeed, Chi and the '747 Patent disclose features relating to semiconductor devices, structures, and related fabrication processes, including FinFET transistors. *See e.g.*, PA-05, 1:5-35, 3:40-57; Ex-01, 1:5-12, 2:18-20, 2:39-6:37. Accordingly, a POSITA would have had reasons to consider the teachings and

suggestions in Chi when contemplating the semiconductor structure of Chang's. Ex-03, ¶¶749-750.

In light of the teachings and suggestions of Chi, in context of those of Chang and a POSITA's state of art knowledge at the time, a POSITA would have been motivated to consider and implement the known use of a salicide layer to reduce resistance between the source/drain region and the contacts in Chang's structure. Given the teachings of Chi in context of a POSITA's knowledge, a POSITA would have appreciated that providing a salicide layer between the source/drain region and contacts in the structure of Chang would have been an obvious implementation of conventional and known semiconductor device fabrication and structure features that were well within the experience and capabilities of such a skilled person at the relevant time (as demonstrated by Chi). Accordingly, and in context of the collective teachings in Chi and Chang, a POSITA would have reasonably expected to succeed at implementing such features in Chang's structure.

Therefore, in light of the teachings and suggestions in Chi, Chang, in context of a POSITA's knowledge and experience at the relevant time, a POSITA would have been motivated and found obvious to include a salicide layer in Chang's structure to provide a more conductive interface between each S/D region and each source/drain contacts, thus improving performance of the semiconductor device. Such an implementation would have been consistent with the concerns in the art to

improve performance of semiconductor devices, as known in the art at the relevant time. Ex-03, ¶751.

Thus, having recognized that the teachings of Chi is consistent with the use of salicide layers in semiconductor structures is consistent like those described by Chang, a POSITA would have been motivated to implement such features in the Chang structure, and done so with a reasonable expectation of success. A POSITA would have looked to provide salicide layer between each source/drain region and each trench contact via 341 in order to provide a more conductive interface to the source/drain region of the structure, thus promoting improved performance of the resulting structure of Chang. Ex-03, ¶752.

A POSITA would have reasonably expected success in implementing the above modification/configuration to the structure of Chang because providing a salicide layer in the manner discussed above would have involved nothing more than applying known semiconductor manufacturing processes for forming a self-aligned silicide layer consistent with the guidance in Chi. Designing, configuring, and implementing such a salicide layer in the Chang structure would have been within the skill, knowledge, and capabilities of a POSITA at the relevant time. Ex-03, ¶753.

Further, a POSITA would have understood and appreciated that providing salicide layer as discussed above would have been an obvious example of combining prior art elements according to known methods, e.g., combining the teachings of Chi

with those of Chang in accordance with known semiconductor device fabrication processes. Ex-03, ¶754.

A POSITA would have leveraged their state of art knowledge and experience in considering the design needs and the market demands for computing devices that include a semiconductor structure and thus would have been motivated to configure and design fabrication processes to successful provide such a salicide layer in the Chang structure. Ex-03, ¶755.

Accordingly, it would have been obvious to configure the Chang structure to include a salicide layer disposed between each source/drain region and each S/D contact ("first contact"), like that recited in Claim 7 of the '747 Patent. Thus, for the reasons here, and above for this Proposed Rejection 2E, the collective teachings and suggestions of Chi and Chang disclose or suggest the features of Claim 7. Thus, Chang in view of Chi render obvious Claim 7 of the '747 Patent. Ex-03, ¶756.

For the reasons above, Chang in view of Chi renders obvious claim 7 and thus the claim is invalid in view of that prior art combination.

6. Proposed Rejection 2F: Claims 1-9 Are Obvious Over *Chang* and *Huang*

a. Limitations [1.pre]-[1.c] and [1.e]-[1.h]

Proposed Rejection 2A discuss how Chang discloses each of the claim limitations in Claims 1-2 and 6. Proposed Rejection 2B discuss how the collective

teachings and suggestions in Chang further renders obvious claim limitations in Claims 1-2 and 4-6. Those opinions are incorporated herein to support Proposed Rejection 2F. Namely, in addition to the reasons discussed above for Proposed Rejection 2B (and incorporated opinions from Proposed Rejection 2A), Chang discloses and/or renders obvious each of claim limitations 1(pre)-1(e) and 1(f)-1(h). For these reasons and those discussed below for limitation 1(d), the combination of Chang in view of Huang discloses or suggests Claim 1 and renders the claim obvious. Ex-03, ¶757.

b. Limitation [1.d]: a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface;

Proposed Rejection 2A discuss how Chang discloses each of claim limitation 1(d) ("a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface"). Proposed Rejection 2B discuss how the collective teachings and suggestions in Chang further renders obvious Claims 1-2 and 4-6. Those opinions herein to support Proposed Rejection 2F. In addition to those opinions and analysis, for the reasons below and above in this Proposed Rejection 2F, and reasons above in Proposed Rejection 2B, the combined teachings and suggestions in Chang

and Huang disclose or suggest, and render obvious claim limitation 1(d).[35] Ex-03, ¶¶758-770.

As discussed for Proposed Rejection 2B the teachings and suggestions in Chang relating to the implementation of a spacer disposed on two sides of the metal gate, are incorporated herein. In context of the disclosures in Chang that are discussed above in Proposed Rejections 2A-2B, a POSITA would have been aware of the use and benefits of providing spacers on the sidewalls of a metal gate in a semiconductor structure (e.g., provide stability, alignment, etc.) and thus had reasons to consider guidance in the art concerning the formation and implementation of spacers when contemplating the Chang structure. In doing so, a POSITA would have considered the teachings and suggestions in Huang. Ex-03, ¶759.

[35] A POSITA would have found it obvious to implement the spacer with a truncated top surface feature in Chang's structure does not mean Chang does not disclose such a feature as claimed in Claim 1— Chang does disclose the claimed spacer for reasons discussed for limitation 1(d) in Proposed Rejection 2A. Rather, consistent with discussion for Proposed Rejection 2B (further supported by the teachings and suggestions of Sell in context of Chang's teachings), a POSITA would have found it obvious to form and implement spacers with a "truncated top surface" notwithstanding the disclosures in Chang addressed above for Proposed Rejection 2A.

Huang discloses methods for forming a semiconductor memory device comprising FETs including FinFETs, which are semiconductor devices used in many application, such as SRAMs. PA-03, ¶¶3-5, 7-8, FIG. 1; Ex-03, ¶¶760-763. Huang's device shown in FIG. 1 has a planarized top surface due to the "gate last approach," which conventionally involves a planarization by two CMP processes of the top surface of the structure, including gate spacers 34 and top edges 36A of CESL 36 (**a truncated top surface**). PA-03, ¶¶8, 9, 11 ("[a] Chemical Mechanical Polish (CMP) is then performed, wherein the CMP is stopped on the top surface of ILD 40"), 14, FIGs. 1, 3.

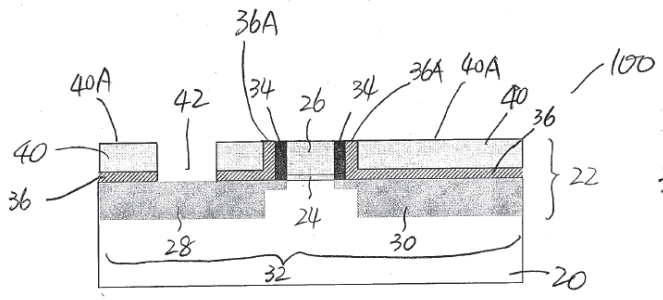

Fig. 1

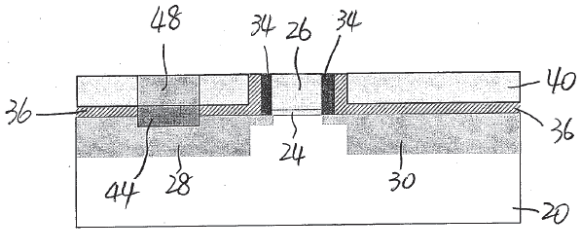

Fig. 3

PA-03, FIGs. 1, 3 (showing gate spacer 34 and CESL 36 subject to CMP up to the level of ILD40).

Huang's device also includes a silicide region 44 that is formed on the surface of the source/drain region 28 and in an opening 42. *Id.*, 11, FIG. 2. As seen in the

figure, silicide region 44 is contained within opening 42 and aligned with the edges of the opening.

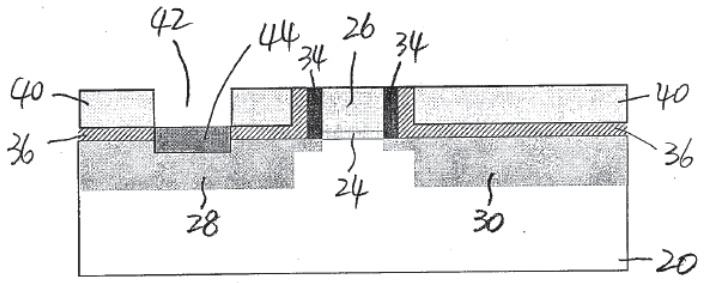

Fig. 2

PA-03, FIG. 2 (showing silicide region 44 formed on source/drain regions 33 and within opening 42, silicide region 44 being aligned to the sidewalls of the opening).

Huang also teaches the use of a dual-damascene process to provide M1 metal lines and M0 vias. (PA-03, ¶17, FIG. 8A.) Huang teaches metal layer M1 metal lines 74 and M0 vias 72 for "for connecting to contact plugs 60 and 62," as shown in FIG. 8A.

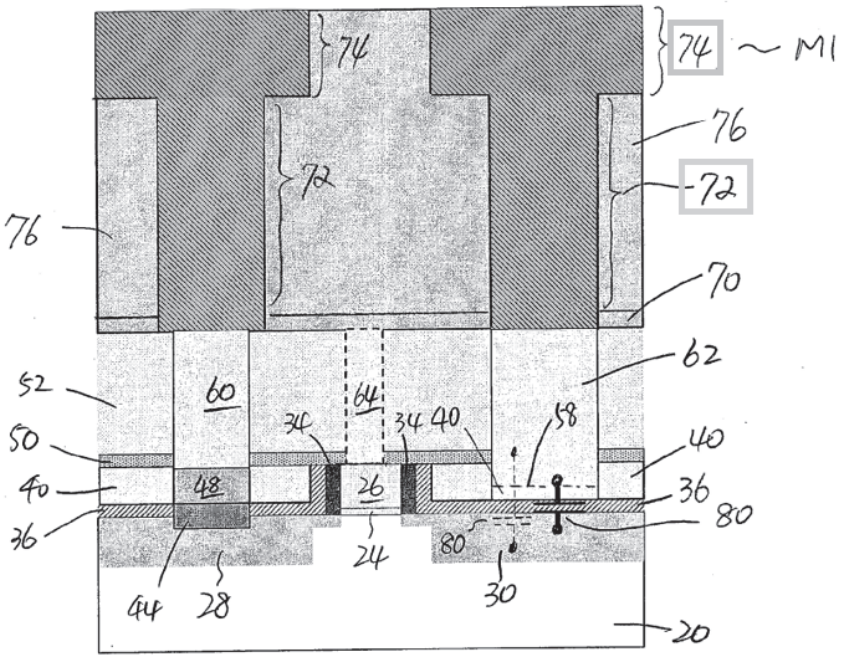

Fig. 8A

PA-03, ¶17, FIG. 8A (annotated).

Huang therefore discloses a semiconductor structure including a spacer disposed on two sides of a metal gate where the spacer was made shorter by removing a part (including during a planarization process) and having a planar top surface, consistent with Interpretations 1-3. *See* §II.D.1.

Huang is analogous art. For example, a POSITA would have understood that Huang's semiconductor structure can include "transistor structure" (PA-03, ¶¶3-5, 7-8, FIG. 1), is in the same field (e.g., semiconductor device transistor structures with contacts) and reasonably pertinent to a problem the '747 Patent purports to address (e.g., transistor structure contact fabrication). *See e.g.*, PA-03, ¶¶2-11, 14, 17; Ex-01, 1:9-2:9, 2:18-20, 2:39-42, 3:1-25, 5:31-6:37. Accordingly, a POSITA

would have had reasons to consider the teachings and suggestions in Huang when contemplating the semiconductor structure of Chang's structure. Upon considering Huang, a POSITA would have recognized and appreciated the teachings and guidance concerning the implementation of spacers (and including etching stop and salicide layers, see claims 3 and 7 below), and thus been motivated to modify or configure Chang's spacers used in the structure in light of such disclosures. Ex-03, ¶764.

Namely, a POSITA would have been led by Chang's teachings, (including the description of spacers and the processes involved with their fabrication in context of the resulting structure in Chang, as discussed for limitation1(d) in Proposed Rejection 2A) in view of the teachings of Huang to provide spacers in the structure by performing known planarization processes (e.g., CMP) on the spacers (after being disposed on the sides of the metal gate). *See e.g.,* PA-04 (Chang), FIGs. 17-23, 24-27, ¶¶52, 89 94-95. Such processes would remove material and provide a planar top surface like the top surface of the spacers taught by Huang. Such a modification and implementing would have predicably resulted in the Chang structure including a spacer disposed on two sides of a metal gate that was made shorter by removing a part of the spacer during a planarization process (e.g., CMP). Such a spacer would have a planar top surface like that shown by Huang). PA-03 (Huang), ¶¶8, 9, 11, 14, FIGs. 1-3; Ex-03, ¶765.

Huang's teachings are consistent with the use of a POSITA's state of art knowledge at the relevant time of the use and implementation of spacers that were subject to planarization process during semiconductor device fabrication, that results in the spacer being made shorter by removing a part (including during a planarization process) and ultimately having a planar top surface in the resulting structure. *See e.g.*, PA-05 (Chi), 14:25-15:9, FIGs. 3C-3E, 15:41-16:60, FIG. 3J, FIG. 3I (describing state of the art spacer features consistent with that known by a POSITA at the time; including, e.g., spacers 32 that have been made shorter by removing a part (including during a planarization process). Ex-03, ¶¶766-767.

Guided by the teachings in Huang in context of Chang's teachings and a POSITA's state of art knowledge at the relevant time, a POSITA would have found it obvious to form the spacers in Chang's structure by removing material from the spacers' top surface (after the spacers were formed) by known planarization processes (e.g., CMP) in order to provide a planarized top surface spacer structure like that shown in the resulting structure of Chang. Such an implementation would have predictably resulted in spacers having a truncated top surface consistent with Interpretation 1 (planar top surface), and Interpretations 2 and 3 (made shorter by removing a part (during a planarization process). *See* §II.D.1.

A POSITA would thus have found it obvious to implement spacers having a truncated top surface consistent with the teachings of Huang in the structure of

Chang discussed above for Claim 1 in Proposed Rejection 2B. For example, a POSITA would have recognized and understood that sidewall spacers were well-known and used in semiconductor structures like Chang's structures (indeed Chang discloses spacers (*see* Proposed Rejection 2A (limitation 1(d)), and likewise recognized advantages in planarizing such structures to provide a flat surface or a co-planar surface with other layers/material upon which other material or layers can be formed and consequently further subsequent processing, including photolithography, to be more reliably performed. The teachings of Huang are consistent with known uses and formations of spacers, and the subsequent planarization processes to provide a planar top surface in semiconductor structures consistent with that described by Chang. In performing such planarization (like that described by Huang), a POSITA would have understood that the spacer is made shorter by removing a part (during a planarization process) resulting in a spacer with a planar top surface in the resulting structure similar to that described by Huang, (which includes structures with planarized top surfaces formed via CMP processes). PA-03 (Huang), ¶¶8, 9, 11, 14, FIGs. 1-3; Ex-03, ¶768.

A POSITA would have had a reasonable expectation of success in implementing the above modification/configuration to the spacers disposed on the sides of the metal gate in Chang's structure. A POSITA would have appreciated and been led by Huang's teachings relating to known fabrication processes and

semiconductor device structures, including spacers on two sides of metal gate structures where the spacers having a planar top surface similar to that described Huang. Moreover, a POSITA would have reasonably expected success in implementing such a modification/configuration because providing a spacer with a planar top surface would have involved nothing more than applying a standard semiconductor manufacturing process (e.g., deposition, CMP, etc. similar to that taught by Huang) for providing the spacer on the sides of metal gates, where the spacer (once formed) was planarized to provide a planar top surface consistent with that known in the art and disclosed by Huang. PA-03, ¶¶8, 9, 11, 14, FIGs. 1-3. A POSITA would have leveraged their state of art knowledge and experience in considering the design needs and the market demands for the applications of the semiconductor structure as contemplated by Chang, and thus would have been motivated to configure and design fabrication processes to successful provide such a spacer in the Chang structure with a "truncated top surface" (as interpreted under Interpretations 1-3, *see* §II.D.1). Ex-03, ¶¶769-770; *KSR*, 550 U.S. at 416.

For the reasons above, Chang in view of Huang renders obvious claim 1 and thus the claim is invalid in view of that prior art combination.

c. Claim 2: The semiconductor device of claim 1, further comprising a second dielectric layer disposed on the first dielectric layer.

As explained for Proposed Rejections 2A-2B, Chang discloses the semiconductor device of claim 1, further comprising a second dielectric layer disposed on the first dielectric layer, as recited in claim 2. Ex-03, ¶¶771-773.

Where, for example, "the semiconductor device of claim 1" is the SRAM described above in this Proposed Rejection 2F, Chang discloses a second dielectric layer disposed on the first dielectric layer, as recited in claim 2 for the same reasons discussed in Proposed Rejection 2B. Any modification to the SRAM discussed in Proposed Rejection 2B, claim 1 (to the extent any modification is deemed necessary) would not affect Chang's disclosure of claim 2. For example, a POSITA would have understood that no proposed or perceived modification to the SRAM discussed in Proposed Rejection 2B, claim 1 would change or otherwise affect the fact that Chang's ILD layer 1510 is disposed on layer 1503 even in the structure discussed here for Proposed Rejection 2F. *Id.*

d. Claim 3: The semiconductor device of claim 2, further comprising an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface.

Proposed Rejection 2A discusses how Chang discloses the limitations in Claims 1-2 and 6. Proposed Rejection 2B discusses how the collective teachings

and suggestions in Chang further renders obvious Claims 1-2 and 4-6. Those opinions are incorporated herein to support Proposed Rejection 2F. In addition to the analysis in Proposed Rejection 2A (incorporated herein), for the reasons below and above in this Proposed Rejection 2F, the combined teachings and suggestions in Chang and Huang disclose or suggest and render obvious Claim 3. Ex-03, ¶¶774-802.

As explained for Proposed Rejections 2A and 2B, Claim 1, Chang teaches **metal gates**, for example, Chang's gates 1441, 1443, 1446, 1596, 1597 are shown in the annotated FIG. 27 below.

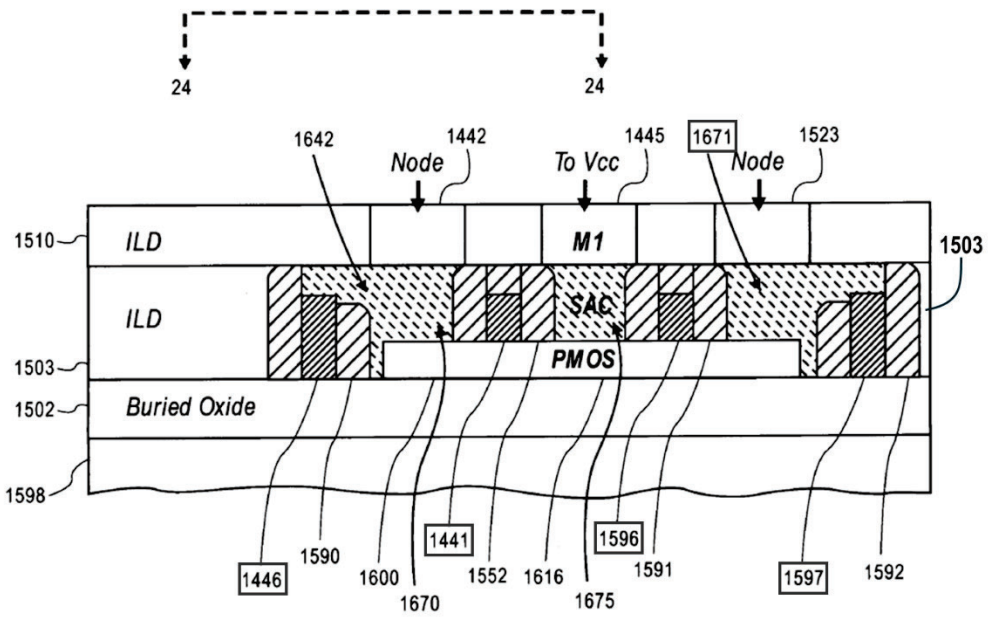

FIG. 27

Chang's gates include a "silicon nitride protection layer" (PA-04 (Chang), ¶114), which is a known "etch-stop layer for self-aligned contact application." Ex-15 (Xiao), 164-65, FIG. 5.64.

Notwithstanding Chang's disclosures, a POSITA would have been motivated to implement in Chang's structure **an etching stop layer having a truncated top surface and disposed on two sides of the metal gate**, in view of Huang's teachings. Ex-03, ¶777.

A POSITA would have had reasons to consider Huang in context of Chang given they each disclose features relating to semiconductor devices/structures and/or parts thereof. Thus, a POSITA had reasons to consider the teachings of Huang when considering the structure and related features disclosed by Chang. Ex-03, ¶¶778-783.

For instance, a POSITA would have recognized that Huang discloses the use of a conventional Contact Etch Stop Layer (CESL) 36, which is a dielectric material and acts as "an etch stop layer" (**an etching stop layer**), and is disposed on both sides of gate dielectric 24 and gate electrode 26 (**an etching stop layer disposed on two sides of the metal gate**).

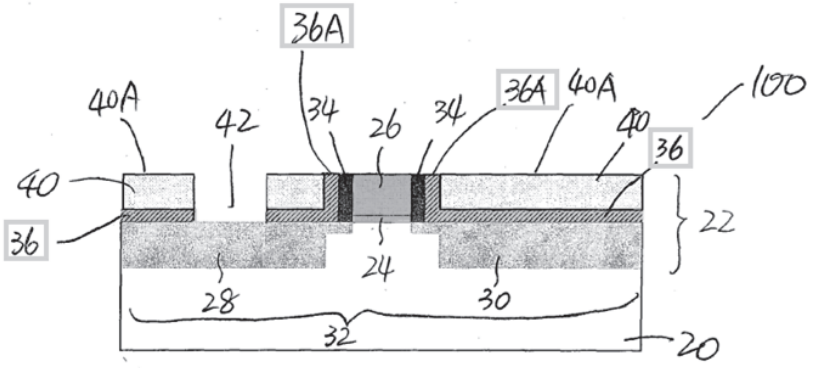

Fig. 1

PA-03 (Huang), FIG. 1, ¶¶ 8-10, 14.

As shown in Figure 6, the CESL is an etch stop layer to protect a source/drain regions (30) against etching of opening (56). *See* PA-03, ¶14 ("**Opening 56 also extends down through CESL 50, and ILD 40 may be etched. In some embodiments, the etching uses CESL 36 as an etch stop layer**"), FIG. 6. Annotated FIG. 6 below shows CESL acting as an etch stop layer to protect a source/drain regions (30) against etching of opening (56).

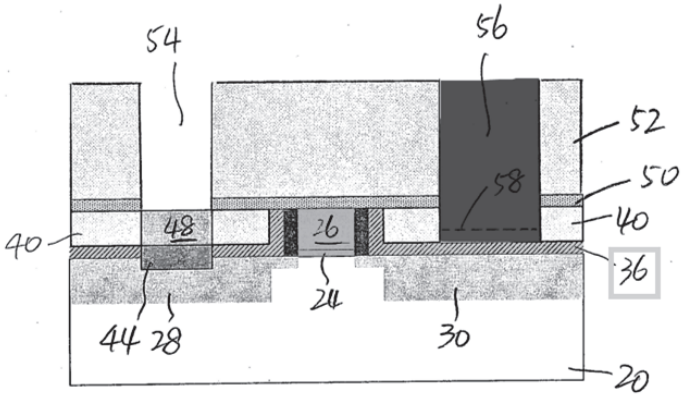

Fig. 6

Huang's device shown in FIG. 1 has a planarized top surface due to the "gate last approach," which conventionally involves a planarization by two CMP processes of the top surface of the structure, including top edges 36A of CESL 36 (**a truncated top surface**).

A POSITA would have understood that well before the relevant time of the '747 patent, it was conventional that an etch stop layer would be planarized during a gate-last process like that disclosed by Huang. Ex-03, ¶¶784-789.

As an initial matter, for the gate-replacement/gate-last process, a POSITA understood that a CMP process is required in order to "open up" the dummy gate for removal, as shown in Xiao's FIGs. 12.49 below.

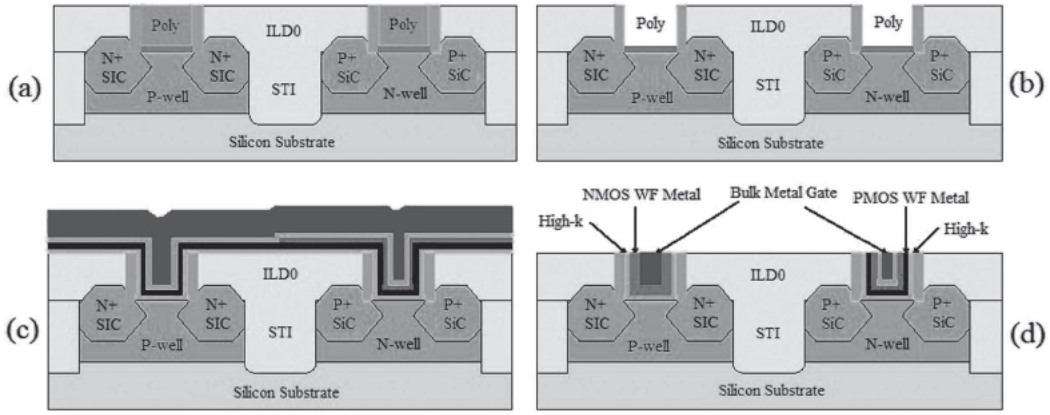

Figure 12.49 Gate-last HKMG processes: (a) ILD0 CMP or poly-open CMP, (b) polysilicon dummy gate removal, (c) high-κ and metal layer deposition, and (d) metal CMP to form HKMG MOSFETs.

Ex-15 (Xiao), FIG. 12.49, 544-45.

Chi is another example, and further shows truncation of the etch stop layer during the CMP to open up the gates for replacement. Chi's "FIGS. 3A-3J depict

various specific methods disclosed herein for forming self-aligned contacts for an integrated circuit product wherein a 'gate-last' or a replacement metal gate technique (RMG) is employed." PA-05 (Chi), 13:63-66.

Figure 3A of Chi shows the initial formation of etch stop layer 34, which is previously described in the process of Figure 2.

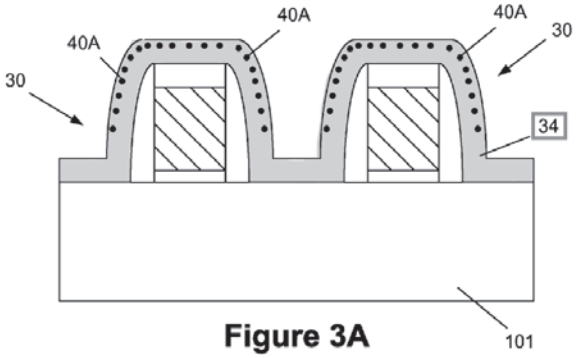

Figure 3A

PA-05 (Chi), FIG. 3A, 13:66-14:9.

Afterwards, "as shown in FIG. 3C one or more CMP processes are performed to remove portions of the layer of insulating material 70, the etch stop layer 34 and the gate cap layer 31. The process results in the exposure of the gate structure 30 (more specifically the gate electrode 30B) for further processing."

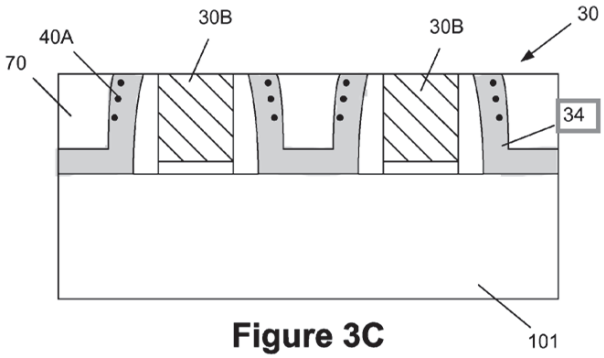

Figure 3C

Id., 14:20-24.

In the remaining steps of FIG. 3, in particular FIGs. 3D through 3F, Chi then describes performing the gate replacement process (i.e., replacing the dummy gates with the permanent gates). PA-05 (Chi), 14:25-15:9. Similar conventional process are shown in Baars (Ex-16, FIGs. 2H-2J (layer 221)) and Griebenow (Ex-36, 16:30-47). While Chang describes metal gates, and discusses replacement processes, it does not provide detail on how to implement such process, and a POSITA would have looked to the art on how to implement such processes. As Huang explicitly acknowledges, as a result of the gate-last approach "the top surface of gate electrode 26 is level with top surface 40A of ILD 40 and top edges 36A of CESL 36." PA-03 (Huang), ¶9.

In light of such knowledge in context of Huang's teachings, a POSITA would have had motivation to implement features consistent with Huang's CESL 36 in Chang's structure. CESLs were well-known in the art at the time of the alleged invention, and a POSITA would have recognized numerous advantages in so implementing such layers. For example, to protect transistor gate structures, source/drain regions). Ex-15 (Xiao), 341-45, 164-65; Ex-03, ¶¶790-791.

A POSITA understood that well before the time of the alleged invention, it was well-known and conventional to use CESLs to protect gate structures and source

drain regions. A number of state of the art references confirm such an understanding. *Id.*

For example, Chi states that an effective etch stop layer is "highly resistant to the etch chemistry," which prevents an etch process (performed on the inter layer dielectric) from "expos[ing] the source/drain region" and ensures "the integrity of the gate encapsulation is not jeopardized" in the etch process. *See* PA-05 (Chi), 2:16-31. Chang seeks to protect transistors features (PA-05 (Chang), ¶114), a POSITA would have been motivated to look to ways to provide such protection, like that taught by Huang. These advantages of using CESLs would have been readily apparent to a POSITA. Ex-03, ¶¶792-793.

As an example of ensuring integrity of the gate encapsulation, Xiao explains that a "Nitride liner" (i.e., silicon nitride layer) can "serve as an etch-stop layer for self-aligned contact application, as shown in Fig. 5.46." *See* Ex-15 (Xiao), 164-65. As shown in the figure, the nitride liner protects the gate structure during etching to form openings for self-aligned contact, which was a "common" use of silicon nitride.

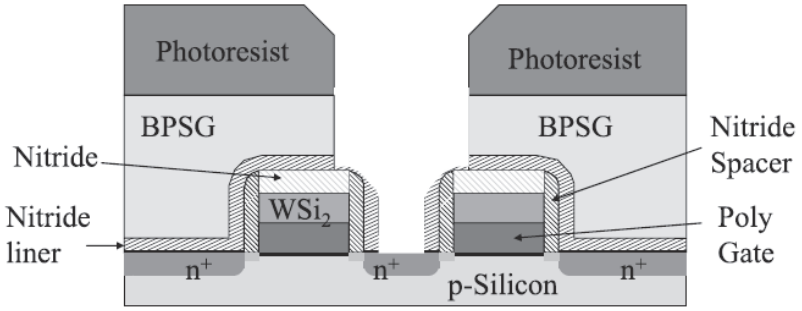

Figure 5.46 Silicon nitride sidewall spacer and self-aligned contact etch stop.

Ex-15, FIG. 5.46.

Accordingly, a POSITA considering semiconductor structures taught by Chang would have been motivated to look to teachings in the art for options in ways to protect its gates and source/drain regions. Huang is an example of such relevant teachings that a POSITA would have considered. Huang teaches the CESL described above, and further explains that it will act as an etch stop layer to protect source/drain region 30 against etching of opening 54. PA-03 (Huang), ¶14, FIG. 6; Ex-03, ¶¶794-795. A POSITA would have been motivated to modify Chang's structure with an etching stop layer having a truncated top surface and disposed on two sides of Chang's metal gate to provide the protective benefits of etch stop layers consistent with that taught by Huang and known in the art, for example, as discussed above. *Id.*

A POSITA would have understood implementing features consistent with Huang's CESL 36 with Chang's structure would have predictably resulted in such a CESL being **disposed on two sides of** Chang's gates 1441, 1596 (**the metal gate**) and would have had a truncated top surface as a result of the truncation process taught by Huang. A POSITA would have had a reasonable expectation of success in implementing such features given it would have involved known processes/techniques predictably resulting in features providing such desired protection (for example, CESL layers). *Id*.

In addition to the CMP process discussed above, a POSITA would have further understood that the proposed combination of Chang with Huang would have had a truncated top surface because Huang teaches to provide the spacer and etch stop layer to have the same top surface. PA-03 (Huang), ¶9, FIG. 1. Accordingly, in the combined structure of Chang and Huang, the etch stop layer would have a truncated top surface as a result of the truncation process discussed in §VI.B.1(a)(5) (regarding "the spacer has a truncated top surface"), §VI.B.2(b), which are herein incorporated by reference. Ex-03, ¶796.

A POSITA would have had the rationale to implement such etching stop layer features in Chang's FIGs. 24-27 structure and would have had a reasonable expectation that the implementation and modification would have been successful. In fact, a POSITA would have understood and appreciated the above-described modification would have leveraged known processes to achieve CESL layers, and their protective characteristics. Such knowledge and expectations, coupled with the teachings of Huang in context of Chang's disclosures, which provides gates and source/drain regions (*see* citations/analysis above for claim 1 of Chang) that would be degraded by over etching, would have led a POSITA to consider and implement the above-discussed modifications to Chang's FIGs. 24-27 structure to provide such protection. Ex-03, ¶797.

A POSITA would have had reasons to consider Huang in context of Chang given they both disclose features relating to semiconductor structures and methods of forming such structures and/or parts thereof. Given such disclosures, a POSITA would have been motivated to combine the teachings of Chang with those of Huang to provide the protective benefits of etch stop layers discussed above. Ex-03, ¶798.

A POSITA would have been motivated to implement, and had a reasonable expectation of success of implementing, such etch stop features in Chang's FIGs. 24-27 structure. For example, the implementation to achieve CESL layers were known in the art well before the alleged invention of the '747 patent, as demonstrated by the state of art teachings Chi and Xiao as discussed above. A POSITA would have readily appreciated the possibility of using a CESL, as disclosed by Huang. Chang provides source drain regions (*see* above §VI.B.1(a)(6)) and gate structures (*see* §VI.B.1(a)(4)) that require protection from over etching. Ex-03, ¶799.

Notwithstanding Chang's disclosure, a POSITA would have had motivation to modify Chang's FIGs. 24-27 structure to provide a CESL to provide protection from overetching. Ex-03, ¶800.

A POSITA would have appreciated that such a modification would have involved applying known technologies/techniques (*e.g.*, CESL layer along the sides of gates and on top of source drain regions) to a known device/structure (Chang's FIGs. 24-27 embodiment with gates and source drain regions) and thus would have

had the motivation and reasonable expectation of success in implementing such a modification to Chang. Considering and implementing such knowledge, techniques, and teachings would have yielded the predictable result of providing etch protection to a known device/structure (Chang's FIGs. 24-27 structure with gates and source/drain regions) by providing an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface in such structure. Ex-03, ¶801.

e. Claim 4: The semiconductor device of claim 2, wherein the first contacts disposed in the first dielectric layer and in the second dielectric layer and each first contact is a monolithically formed structure.

Claim 5: The semiconductor device of claim 2, wherein the second contacts disposed in the first dielectric layer and in the second dielectric layer and each second contact is a monolithically formed structure.

As explained for Proposed Rejections 2A-2B, Chang discloses the semiconductor device of claim 1, further comprising monolithically formed first and second contacts, each disposed in the first and second dielectric layers, as recited in claims 4-5. Ex-03, ¶¶803-804.

Where, for example, "the semiconductor device of claim 1" is the SRAM described above in this Proposed Rejection 2F, Chang discloses first and second contacts, each disposed in the first and second dielectric layers, as recited in claims 4-5 for the same reasons discussed in Proposed Rejections 2A-2B. Any modification

to the SRAM discussed in Proposed Rejection 2B, claim 1 (to the extent any modification is deemed necessary) would not affect Chang's disclosure of claims 4-5. For example, a POSITA would have understood that no proposed or perceived modification to the SRAM discussed in Proposed Rejection 2B, claim 1 would change or otherwise affect the fact that Chang's self-aligned contacts 1670, 1671 and self aligned contacts 1670, 1671, and 1675 are monolithically formed and disposed in ILD 1503 and ILD 1510 even in the structure discussed here for Proposed Rejection 2F. *Id.*

f. Claim 6: The semiconductor device of claim 1, further comprising at least one fin structure disposed on the substrate.

As explained for Proposed Rejections 2A-2B, Chang discloses the semiconductor device of claim 1, further comprising at least one fin structure disposed on the substrate, as recited in claim 6. §§VI.B.1(c), VI.B.2(g); Ex-03, ¶¶805-807.

Where, for example, "the semiconductor device of claim 1" is the SRAM described above in this Proposed Rejection 2F, Chang discloses at least one fin structure disposed on the substrate, as recited in claim 6 for the same reasons discussed in Proposed Rejections 2A-2B. Any modification to the SRAM discussed in Proposed Rejection 2B, claim 1 (to the extent any modification is deemed necessary) would not affect Chang's disclosure of claim 6. For example, a POSITA

would have understood that no proposed or perceived modification to the SRAM discussed in Proposed Rejection 2B, claim 1, would change or otherwise affect the fact that Chang's transistor structure 116 includes diffusion layer/diffusion body/fin 104 even in the structure discussed here for Proposed Rejection 2F. *Id.*

g. Claim 7: The semiconductor device of claim 1, further comprising a salicide layer disposed between each S/D region and each first contact.

The discussions in Proposed Rejections 2A and 2B are incorporated herein to support Proposed Rejection 2F. Additionally, for the reasons below and above in this Proposed Rejection 2F, the combined teachings and suggestions in Chang and Huang disclose or suggest, and render obvious Claim 7. Further, for brevity, in Proposed Rejection 2C, it was discussed that a POSITA would be motivated to configure the self-aligned contacts 1670, 1671 in Chang's FIG. 27 to include a salicide layer that is disposed between each S/D diffusion region 1600 and each self-aligned contacts 1670, 1671. Those discussions are incorporated herein and will not be repeated here. Ex-03, ¶¶808-819.

A POSITA would have would have been motivated to implement in Chang's structure a self-aligned silicide ("salicide") layer disposed between each S/D region and each first contact in view Huang. Ex-03, ¶809.

Understanding that the use of a salicide layer between a source/drain region and contact would advantageously create a more conductive contact, and that such

features were widely known in the art at the time, and that Chang's semiconductor structure includes a source/drain region and corresponding contact (*see* Proposed Rejection 2A, limitations 1(e)-1(f)), a POSITA would have had reasons to consider ways to likewise improve Chang's structure. To do so, a POSITA would have looked to teachings in the art to supplement and/or complement their knowledge and experience pertaining to the fabrication and implementation of semiconductor structures. A POSITA would have found Huang to provide insight that would have led a POSITA to implement a salicide layer between a source/drain and the contacts in the structure of Chang to enhance or establish conductive surfaces to the semiconductor device. Ex-03, ¶810.

For instance, a POSITA would have recognized that Huang discloses the known use of a salicide layer disposed between each S/D region and each first contact. For example, Huang discloses processes that forms a silicide region 44 on the surface of the source/drain region 28 and in an opening 42, where the silicide region 44 is contained within opening 42 and aligned with the edges of the opening. *See e.g.,* PA-03 (Huang), ¶11 ("after the formation of opening 42, source/drain silicide region 44 is formed on the surface of source/drain region 28 and in opening 42"), FIG. 2, *see also id.*, ¶¶2-10, 14, 17, FIGs. 1, 3, 8a. Ex-03, ¶811.

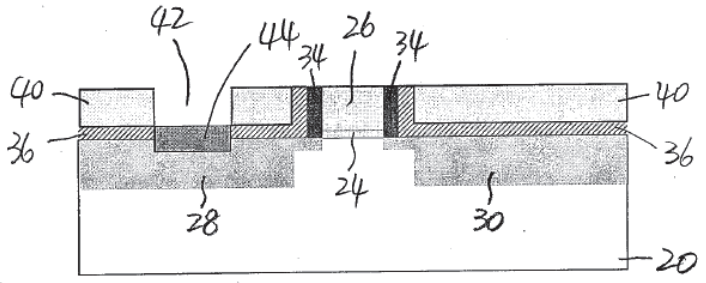

Fig. 2

PA-03, FIG. 2 (showing silicide region 44 formed on source/drain regions 33 and within opening 42, silicide region 44 being aligned to the sidewalls of the opening).

As previously discussed, Huang is analogous art. *See* §VI.B.6(b) (when discussing the combination of Chang and Huang for limitation 1(d)). Accordingly, a POSITA would have had reasons to consider the teachings and suggestions in Huang when contemplating the semiconductor structure of Chang's structure. Ex-03, ¶812.

In light of the teachings and suggestions of Huang, in context of those of Chang and a POSITA's state of art knowledge at the time, a POSITA would have been motivated to consider and implement the known use of a salicide layer to reduce resistance between the source/drain region and the contacts in Chang's structure. Given the teachings of Huang in context of a POSITA's knowledge, a POSITA would have appreciated that providing a salicide layer between the source/drain region and contacts in the structure of Chang would have been an

obvious implementation of conventional and known semiconductor device fabrication and structure features that were well within the experience and capabilities of such a skilled person at the relevant time (as demonstrated by Huang). Accordingly, and in context of the collective teachings in Huang and Chang, a POSITA would have reasonably expected to succeed at implementing such features in Chang's structure. Ex-03, ¶813.

Therefore, in light of the teachings and suggestions in Huang, Chang, in context of a POSITA's knowledge and experience at the relevant time, a POSITA would have been motivated and found obvious to include a salicide layer in Chang's structure to provide a more conductive interface between each S/D region and each source/drain contacts, thus improving performance of the semiconductor device. Such an implementation would have been consistent with the concerns in the art to improve performance of semiconductor devices, as known in the art at the relevant time. Ex-03, ¶814.

Thus, having recognized that the teachings of Huang is consistent with the use of salicide layers in semiconductor structures like those described by Chang, a POSITA would have been motivated to implement such features in the Chang structure, and done so with a reasonable expectation of success. A POSITA would have looked to provide salicide layer between each source/drain region and each trench contact via 341 in order to provide a more conductive interface to the

source/drain region of the structure, thus promoting improved performance of the resulting structure of Chang. Ex-03, ¶815.

A POSITA would have reasonably expected success in implementing the above modification/configuration to the structure of Chang because providing a salicide layer in the manner. Discussed above would have involved nothing more than applying known semiconductor manufacturing processes for forming a self-aligned silicide layer consistent with the guidance in Huang. Designing, configuring, and implementing such a salicide layer in the Chang structure would have been within the skill, knowledge, and capabilities of a POSITA at the relevant time. Ex-03, ¶816.

Further, a POSITA would have understood and appreciated that providing salicide layer as discussed above would have been an obvious example of combining prior art elements according to known methods, e.g., combining the teachings of Huang with those of Chang in accordance with known semiconductor device fabrication processes. Ex-03, ¶817.

A POSITA would have leveraged their state of art knowledge and experience in considering the design needs and the market demands for computing devices that include a semiconductor structure and thus would have been motivated to configure and design fabrication processes to successful provide such a salicide layer in the Chang structure. Ex-03, ¶818.

Accordingly, it would have been obvious to configure the Chang structure to include a salicide layer disposed between each source/drain region and each S/D contact ("first contact"), like that recited in Claim 7 of the '747 Patent. Thus, for the reasons here, and above for this Proposed Rejection 2F, and those for claim 1 in Proposed Rejection 2A, the collective teachings and suggestions of Huang and Chang disclose or suggest the features of Claim 7. Thus, Chang in view of Huang render obvious Claim 7 of the '747 Patent. Ex-03, ¶819.

For the reasons above, Chang in view of Huang renders obvious claim 7 and thus the claim is invalid in view of that prior art combination.

h. Claim 8: The semiconductor device of claim 3, further comprising a plurality of third contacts disposed on parts of the first contacts and on parts of the second contacts, wherein each third contact is a monolithically formed structure.

Claim 9: The semiconductor device of claim 8, wherein each third contact comprises a via hole structure and a trace structure, wherein the via hole structure and the trace structure comprise the same material and contact each other directly.

Chang in view of Huang discloses and/or suggests these limitations. Proposed Rejection 2D (incorporated by reference herein) explains how Chang in view of Sell and Huang discloses and/or suggests claims 8-9, and Proposed Rejections 2A-2B (incorporated by reference herein) explains how Chang discloses and/or suggests Claim 1. *See* §§VI.B.1-2, 4; Ex-03, ¶¶820-841.

As explained for Proposed Rejection 2A, Claim 1, Chang teaches "a plurality of first contacts" (e.g., parts of self-aligned contacts 1670, 1671, and self-aligned contact 1675) "disposed in the first dielectric layer" (e.g., interlayer dielectric layer 1503) "that are electrically connected to parts of the S/D region" (e.g., source and drain regions of PMOS diffusion layer 1600), as claimed in limitation 1(f). *See* §VI.B.1(a)(7). Chang also teaches self-aligned contacts 1670 and 1671 (as indicated in the annotated illustration of FIG. 27 below) that are "a plurality of second contacts" that "are electrically connected to" gates 1446, 1597 and are "disposed in" interlayer dielectric layer 1503, as claimed in limitation 1(g). *See* §VI.B.1(a)(8); *see also* PA-04, FIG. 27.

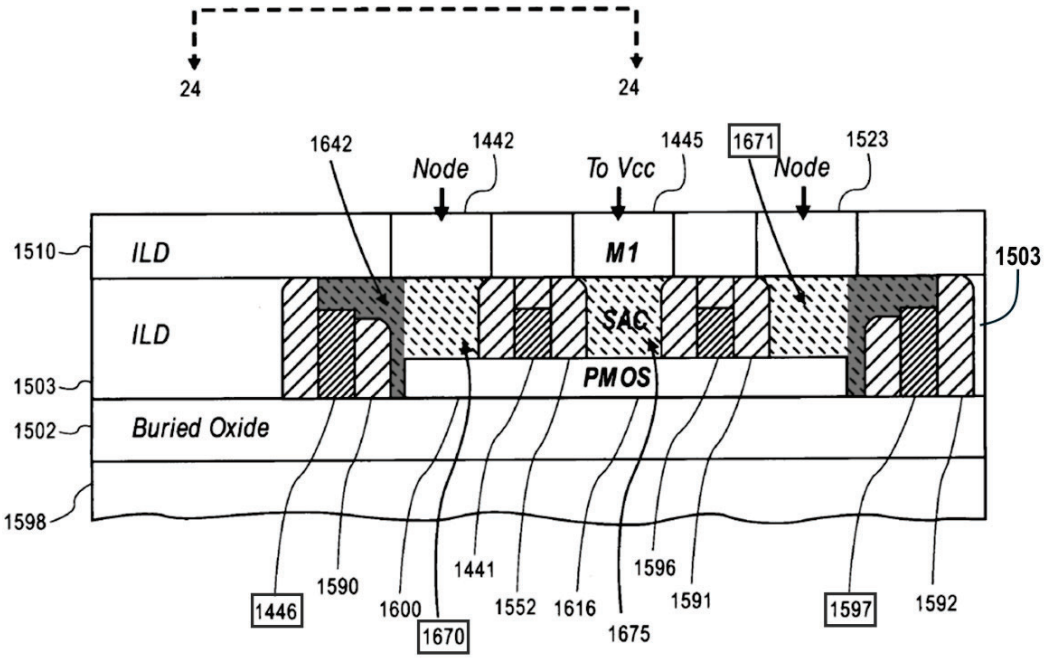

FIG. 27

PA-04 (Chang), ¶¶112-13.

Further, it was well-known and conventional to form metal (1) ("M1") metal lines and metal (0) vias (above the metal (0) lines and device contacts) using a dual-damascene process. By the time of the alleged invention, the dual-damascene process was an established technique in semiconductor manufacturing, particularly in the back-end-of-line (BEOL) processing, which is the "formation of the M1 wiring layer to formation of a pad opening to a final passivation…in a wafer level package process." (Ex-11, ¶89.)

A number of state of art references confirm such an understanding and provide teachings consistent with a POSITA knowledge of the art at the time of the '747 patent. These references have been discussed in Proposed Rejection 2D and will be omitted here for the sake of brevity. Ex-03, ¶823.

As discussed in Proposed Rejection 2D, a POSITA considering the semiconductor structure in Chang would have been motivated to look to teachings in Huang for ways to provide a connection of the semiconductor structure via the first contacts and the second contact to the M1 layer with simplified fabrication, no requirement for metal etching, and reduced risk of electromigration failure. Ex-03, ¶824.

In considering Huang in context of Chang, a POSITA would have been motivated to consider the collective teachings of Chang with those of Huang to

achieve a dual-damascene process to provide M1 metal lines and M0 vias in the Chang FIG. 27 structure. *See* PA-03 (Huang), ¶17, FIG. 8A; Ex-03, ¶825.

In my opinion, a POSITA would have been motivated to implement such a dual-damascene process in the Chang's FIG. 27 structure, and would have reasonably expected such an implementation to be successful in context of Chang's disclosed structure. The implementation of a achieve a dual-damascene process to provide M1 metal lines and M0 vias was known in the art by a POSITA before the alleged invention of the '747 patent, as seen by the above-mentioned state of art teachings (*see* discussions above regarding Wolf, May, and Xiao). A POSITA would have readily appreciated the possibility of using a dual-damascene process to provide M1 metal lines and M0 vias, as disclosed by Huang. Ex-03, ¶826. Chang provides a metal self-aligned contacts 1670, 1671 connected to metal one lines 1442, 1523 (PA-04 (Chang), ¶¶108, 112-13), but does not provide any BEOL interconnection, which a POSITA would have understood is critical to create an integrated circuit with multiple trigate transistors for devices such as SRAMs that have predictable design and performance, as is the driving force of the semiconductor industry and of Chang. PA-04 (Chang), ¶6; Ex-03, ¶826.

A POSITA would have appreciated that the implementation of a dual-damascene process to provide M1 metal lines and M0 vias was at the time, a conventional method to produce such implementations. *See above and for example*,

(Ex-09 (Wolf), 696-98; Ex-10 (May), 55-56; Ex-15 (Xiao), 19, 345-49, 453, 464, 497-98, 517-18, 543, 574-79. A POSITA would have understood that the combined teachings of Chang and Huang would merely amount to determining a suitable dual-damascene process to modify the metal one line in Chang's FIG. 27 structure as explained above. Ex-03, ¶827.

Whether a POSITA considers Chang's metal one line to be what is known in the art as an M1 layer would not change my analysis or opinions. A POSITA would have understood and appreciated that there was no universal convention as to what such skilled artisans considered the "M1" or "M0" layer in semiconductor structures/devices. In Chang, the metal one line is what connects to the MOS diffusion layer and the self aligned contacts of the metal gates. PA-04 (Chang), ¶¶112-13; Ex-03, ¶828.

Accordingly, a POSITA would have been reasonable in considering the "M0" process to be an "M1" process because it is the first metalized trench/via process. As discussed, the dual damascene process was known to be generally repeated a number of times. *See* Ex-09 (Wolf), 696-98; Ex-15 (Xiao), 19; Ex-03, ¶¶829-830.

Xiao's FIG. 13.30 and other figures (for example, FIGs. 14.17-20) below illustrate a via-first dual damascene copper low-k interconnection process for an M2 metal layer and M1 via over an M1 metal layer. Ex-15 (Xiao), 578, 611-14, FIG. 13.30.

Under any convention, a POSITA would have understood a dual-damascene process generally involved the conventional steps of patterning and etching the via and trench definition, depositing metal to fill the space of both via and trench, and CMP. (*See above and for example*, Ex-09 (Wolf), 696-98; Ex-10 (May), 55-56; Ex-15 (Xiao), 19, 345-49, 453, 464, 497-98, 517-18, 543, 574-79.) A POSITA would have been able to readily apply conventional methods of dual-damascene processes, such as those taught by Huang, to Chang with high predictability and success. Ex-03, ¶831.

Accordingly, a POSITA would have been motivated to modify Chang's metal contacts to include, above its metal zero lines, Huang's M1 metal lines and M0 vias. In fact, Huang explicitly contemplates placing upper metal lines and vias over lower metal lines, such as metal (0) portion 350 in explaining that "In subsequent process steps, more metal layers (not shown) may be formed over metal layer M1." PA-03 (Huang), ¶17; Ex-03, ¶¶832-833.

The above motivation rationale discussed above for Claims 8-9 would have been applicable to both Chang's FIG. 27 structure discussed for claim 1 in §VI.B.1(a) and to Chang's modified embodiment discussed for claims 1 and 3 in §§VI.B.3(a), (b), (d).

Proposed Rejection 2B explain how Chang discloses and/or suggests claims 1-2 and 4-6. (§VI.B.1-2, incorporated herein.) However, in addition to Chang's

FIG. 27 structure discussed above (claim 1 in (§VI.B.1(a)) or as modified (Claims 1 and 3 in §§VI.B.3(a), (b), (d)) a POSITA would have been motivated to implement **a plurality of third contacts** as claimed in Claims 8-9 in view of Huang. Ex-03, ¶834.

In light of Huang's teachings and a POSITA's state of art knowledge as discussed above, Chang's FIG. 27 structure would have been predictably modified to include, above its metal one lines 1442, 1523, consistent with the teachings of Huang using the dual-damascene processes known in the art and as taught by Huang. *See above*. Ex-03, ¶¶835-837.

As a result, the modified FIG. 27 structure would have included a **plurality of third contacts** (for example, parts of the newly formed M1 lines above Chang's metal contacts 1670, 1671 and metal lines 1442, 1523 the M1 and M0 lines formed based on Huang's teachings) **disposed on parts of the first contacts** (for example, parts of 1670, 1671) **and on parts of the second contacts** (for example, parts of 1670, 1671), as in Claim 8. *Id.*

In addition, **each third contact** (in the modified FIG. 5B structure) would have comprised **a via hole structure (M0 vias) and a trace structure (**parts of the newly formed M1 lines (*see* Ex-01, 5:48-53 (trace structure may be "lines")), which would **comprise the same material and contact each other directly** (as in claim 9) given they are formed using the dual-damascene process like that taught by

Huang, which would also result in **each third contact** (above) being a **monolithically formed structure (**as in Claim 8).

A POSITA would have understood and appreciated that such a modification would have involved the application of known technologies/techniques (for example, dual-damascene process to provide M1 metal lines and M0 vias) to a known device/structure (like Chang's FIG. 27 embodiment with metal zero lines 1442, 1523). Accordingly, such a skilled person would have been motivated to implement such a modification, and would have reasonably expected such an implementation to be successful. Ex-03, ¶838. A POSITA would have understood upon considering and implementing such knowledge, known techniques, and teachings in the prior art references, such a modification would have yielded the foreseeable result of providing M1 metal lines and M0 vias to a known device/structure (Chang's FIG. 27 structure with metal zero lines 1442, 1523) with operability to the M1 layer in the structure of FIG. 27. *Id.*

In the combined structure of Chang and Huang, M0 vias 72 (**a via hole structure**) and metal layer M1 metal lines 74 (**a trace structure**) form **a third contact**. This would have been consistent with the teachings shown in annotated FIG. 8A of Huang above.

As discussed in claim 8, a dual-damascene process is used to form M0 vias 72 and metal layer M1 metal lines 74 together in a single deposition, which a POSITA

would have understood to mean **the via hole structure and the trace structure comprise the same material and contact each other directly**. PA-03, ¶17 ("no noticeable interfaces are formed between M0 vias 72 and the respective overlying metal lines 74."), FIG. 8A; Ex-03, ¶¶839-841.

For the reasons above, Chang in view of Huang renders obvious Claims 8-9, and thus the claims are invalid in view of that prior art combination.

7. Proposed Rejection 2G: Claims 4 and 5 Are Obvious Over *Chang* and *Hong*

a. Claim 4: The semiconductor device of claim 2, wherein the first contacts disposed in the first dielectric layer and in the second dielectric layer and each first contact is a monolithically formed structure.

Chang in view of Hong discloses and/or suggests these limitations. As discussed in §§VI.B.1(a)(8), VI.B.1(b) (limitation [1.g] and claim 2, respectively), the identified parts of self-aligned contacts 1670 and 1671, and self-aligned contact 1675 (**first contacts**) are disposed in layer 1503 (**the first dielectric layer**), and each is a homogeneous metal fill layer formed from a single metal deposition (see PA-04 (Chang), ¶¶93-94, FIGs. 19-20, 27) and therefore is **a monolithically formed structure**. *See* §§VI.B.1(a)(8), VI.B.1(b) above, incorporated herein.) Ex-03, ¶¶842-858.

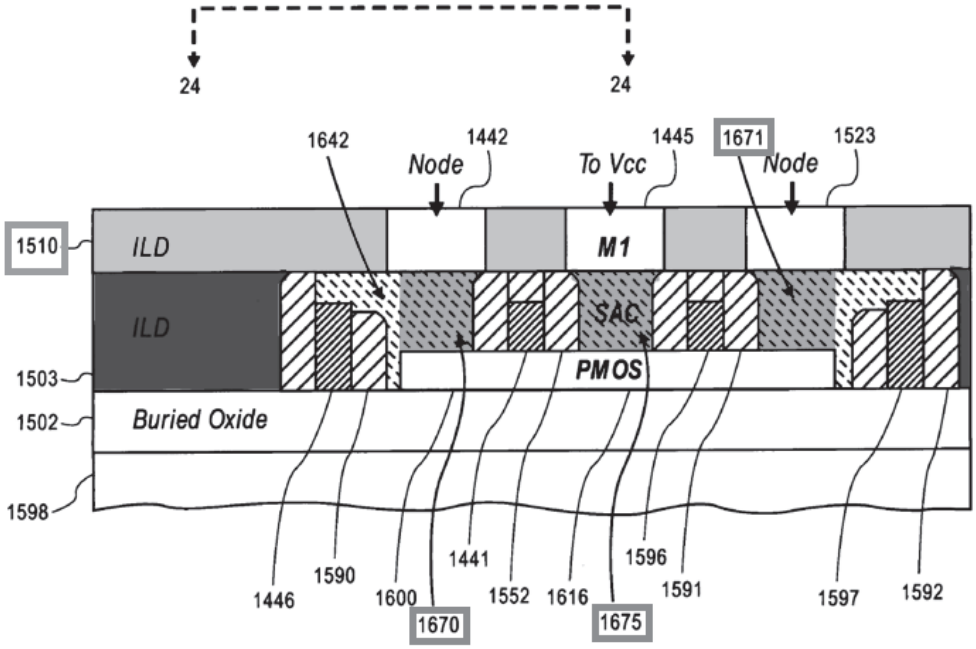

FIG. 27

PA-04 (Chang), FIG. 27 (annotated), ¶¶113, 93-94.

Notwithstanding Chang's disclosures, a POSITA would have had motivation to implement Chang's self-aligned contacts (**first contacts**) also **disposed in a second dielectric layer** based on Hong. Ex-03, ¶¶844-846.

Hong discloses improved structures for electrically contacting semiconductor device features. *See* PA-07 (Hong), Abstract, 2:13-58, 8:53-9:27, 10:46-67; *see also*, 2:4-10, 9:55-64, 11:1-9. For example, Hong discloses a "share contact" for FETs that includes contact 442 formed simultaneously between a metal gate 411 and source/drain region 402, and within a plurality of dielectric layers (e.g., layer 406 on layer 401). *Id*., 8:53-9:27, 10:46-67, FIGs. 7, 9.

500. In Hong, first contact layer 442 is formed in both a first dielectric layer 401 and a second dielectric layer 406. *See* PA-07, 8:54-9:27. A third dielectric layer 409 (i.e., a capping layer) is formed on a second metal gate 421, as shown in annotated FIG. 7 below.

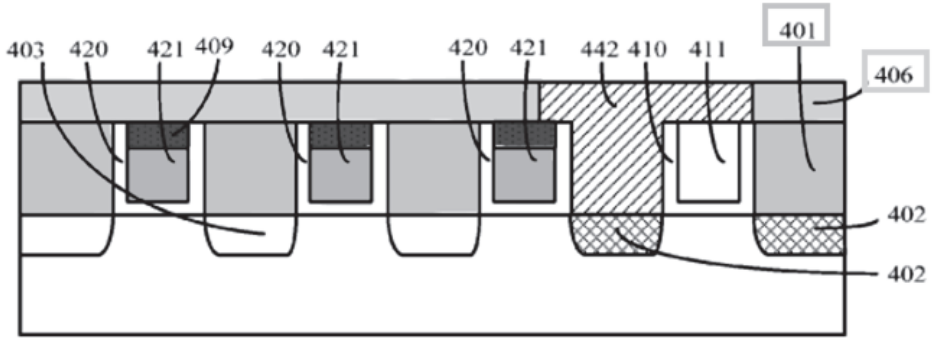

FIG. 7

PA-07 (Hong), FIG. 7.

A POSITA would have had reasons to consider Hong in context of Chang given they each disclose features relating to semiconductor devices/ structures and/or parts thereof. For example, Hong, Chang, and the '747 patent are all concerned with forming contact areas over transistor structures. (*See* e.g., PA-04 (Chang), ¶¶108-113; PA-07 (Hong), 8:54-10:56; Ex-01 ('747 Patent), 1:9-13, 5:66-6:37.) Thus, a POSITA would have had reasons to consult Hong when looking to implement a structure like that disclosed by Chang, including contact areas and related structures. Ex-03, ¶847.

A POSITA would have been motivated to combine the teachings of Chang with those of Hong to provide a second dielectric layer beneath the metal (1) layer

of Chang. This modification of Chang would be implemented as shown below according to known techniques. Ex-03, ¶¶848-849.

A POSITA would have been motivated to implement, and had a reasonable expectation of success of implementing, such a second dielectric layer beneath the metal (1) layer of Chang's structure.

For example, as previously discussed, a POSITA would have recognized that creating metal contacts typically involved depositing a metal fill layer, and polishing it back with a CMP process to remove it from outside the desired location of the contact. Hong recognizes that this CMP may damage the underlying transistor structures, and further recognizes that use of a second dielectric layer beneath the metal (1) layer protects the underlying transistor structures, resulting in "relatively less damage." *See* PA-07 (Hong), 11:1-9, 9:55-64. Ultimately, use of the second dielectric layer beneath the metal (1) layer will "aid to increase the stability of the transistor." *Id*.; Ex-03, ¶850.

Chang's metal (1) layer is fabricated the same way – by a "metal damanscene process" where a metal deposition "covers surface 965 and fills opening 940, 941, and 942" and then is "planarized by polishing" to remove the metal everywhere except the openings. *See* PA-04 (Chang), ¶97. A POSITA would have understood based on the teachings of Hong that Chang's transistor structures would be at risk of damage during such polishing, and therefore would have recognized the benefits of

Hong's second dielectric layer beneath the metal (1) layer to protect the underlying transistor structures. Ex-03, ¶¶851-853.

As Hong notes, a POSITA would have also recognized the known problems caused by damage to the metal gate and spacers during the etching process to create the opening for first contact layer 442. Hong addresses this issue by providing "an etching selectivity" between the third dielectric layer 409 and the second dielectric layer 406. *See* PA-07 (Hong), 8:54-9:27, 8:3-13, 7:43-54.

As a result, the second gate dielectric layer 420 and the third dielectric layer 409 provide full protection to the second metal gate 421 during the etching process to create the opening for first contact layer 442. In other words, this solution addresses "[t]he problem of exposing the second metal gate 421 caused by technology errors during a process for exposing the first metal gate 411," "thus it may ensure the stability of the transistor." *See* PA-07 (Hong), 8:54-64.

Guided by such teachings, and by the knowledge in the art, a POSITA would have been motivated to form an additional dielectric layer (**a second dielectric layer**) in Chang beneath the metal (1) layer comprising ILD 1510, such that the identified self-aligned contacts (**first contacts**) are **disposed in** the **second dielectric layer**. Ex-03, ¶854.

A POSITA would have been motivated to implement such a modification, and would have reasonably expected it to be successful. In fact, such a skilled person

would have appreciated that the above modification to Chang's structure would have involved the application of known semiconductor device structure and process technologies (i.e., dielectric deposition), including gate protection techniques for Chang's similar gate structures, that were well within the capabilities and knowledge of such a person at the time. Considering and implementing such knowledge, techniques, and teachings would have yielded the predictable and advantageous result of an enhanced protection of its gates during the etching processes to create the openings for self-aligned contacts. Ex-03, ¶¶855-856.

The above motivation rationales discussed above for claim 4 would have been applicable to both Chang's structure discussed for claim 1 in §§VI.B.1(a), VI.B.1(a)-(d) and to the modified Chang structure discussed for claim 1 in §VI.B.1(d).

A POSITA would have understood that Hong's gate protection technique was applicable to Chang's gates, which have substantially the same structure and purpose. For example, both Chang and Hong have spacers provided on two sides of metal gates, a dielectric cap on the gates, and etching processes that form openings for contacts that risk damaging the gates. *See* PA-04 (Chang), ¶¶111-13, ¶¶93-94; PA-07 (Hong), 8:53-9:45. Implementing an additional dielectric layer with etch selectivity in such contexts were well known by those of ordinary skill at the time to have successfully worked before the time of the alleged invention, and it would have been well within the ability of a POSITA. Ex-03, ¶¶857-858.

For the reasons above, Chang in view of Hong renders obvious Claim 4, and thus the claim is invalid in view of that prior art combination.

b. Claim 5: The semiconductor device of claim 2, wherein the second contacts disposed in the first dielectric layer and in the second dielectric layer and each second contact is a monolithically formed structure.

Chang in view of Hong discloses and/or suggests these limitations. As discussed in §§VI.B.1(a)(7), VI.B.1(b) (limitation [1.h] and claim 2, respectively), the identified parts of (as indicated in the annotated Figure 27 below) self-aligned contacts 1670 and 1671 (**second contacts**) are disposed in layer 1503 (**the first dielectric layer**), and each is a homogeneous metal fill layer formed from a single metal deposition (see ¶¶93-94, FIGs. 19-20) and therefore is **a monolithically formed structure**. (§§VI.B.1(a)(7), VI.B.1(b), incorporated herein), as shown in annotated below. Ex-03, ¶¶859-862.

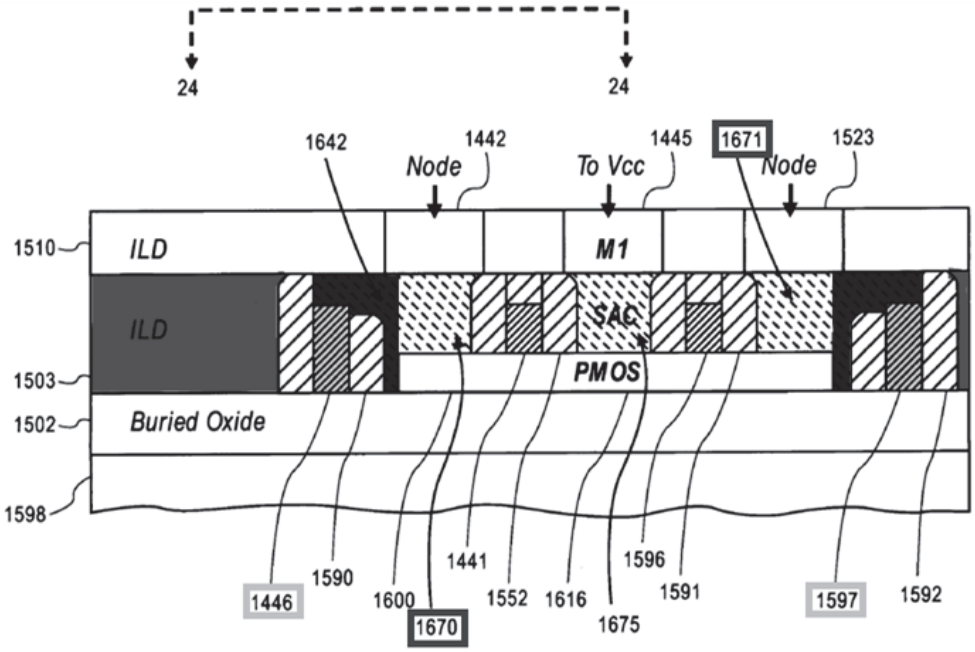

FIG. 27

PA-04 (Chang), FIG. 27, ¶¶112-13.

Chang in view of Hong discloses this limitation for the same reasons as explained in §VI.B.7(a) (Claim 4), which is incorporated herein by reference. *See* §VI.B.7(a); Ex-03, ¶860.

Such features are consistent with the Chang's teachings in view of Hong as explained for claim 4. Thus, for similar reasons, a POSITA would have had the same motivation, rationale, and expectation of success to configure Chang's structure such that the second contacts disposed in the first dielectric layer and second dielectric layer and each second contact is a monolithically formed structure, as recited in claim 5. *See* §VI.B.7(a) (incorporated herein). The above motivation rationales discussed above for claim 4 would have been applicable to both Chang's

structure discussed for claim 1 in §VI.B.1(a) and to the modified Chang structure discussed for claim 1 in §VI.B.1(d). Ex-03, ¶861.

For the reasons above, Chang in view of Hong renders obvious Claim 4, and thus the claim is invalid in view of that prior art combination. Ex-03, ¶862.

VII. SERVICE, STATUTORY ESTOPPEL, AND OTHER PROCEEDINGS

A. Certification of Service on Patent Owner

Per 37 C.F.R. § 1.510(b)(5), Requestor has served copies of this request on counsel for Marlin Semiconductor Limited, which is listed as the assignee of the '747 Patent at reel/frame: 056991/0292.

B. Certification Regarding Statutory Estoppel

As required by 37 C.F.R. § 1.510(b)(6), Requester Requestor certifies that the statutory estoppel provisions of 35 U.S.C. § 315(e)(1) and 35 U.S.C. § 325(e)(1) do not prohibit Requestor from filing the instant request for ex parte reexamination.

C. Other Proceedings

The '747 Patent has been asserted against Requestor in *Longitude Licensing Ltd. et al. v. Apple, Inc. et al.*, Case No. 1:25-cv-00215 (W.D.Tex.) and *Longitude Licensing Ltd. et al. v. Lenovo Group Limited et al.*, Case No. 2:25-cv-00171 (E.D.Tex.). The '747 Patent was also previously at issue in *Longitude Licensing Ltd. et al. v. Apple, Inc. et al.*, Case No. 337-TA-1443 before the International Trade Commission (ITC), but was dropped by Patent Owner from the proceeding. The

'747 Patent also was previously at issue in *Taiwan Semiconductor Manufacturing Company Limited et al v. Marlin Semiconductor Limited*, IPR2025-00865 (PTAB).

VIII. REQUEST FOR EXPEDITED REEXAMINATION

Due to the ongoing nature of the above-identified lawsuit, Requester respectfully urges that, pursuant to 35 U.S.C. § 305, this Request be granted and reexamination be conducted not only with "special dispatch," but also with "priority over all other cases" in accordance with M.P.E.P. § 2261.

IX. CONCLUSION

Reexamination should be granted and the challenged claims cancelled.

Respectfully submitted,

Dated: December 3, 2025

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