IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of Liu *et al*.		§	Attorney Docket No.: 433123.000006
		§	
U.S. Patent	8,502,757	§	
		§	
Issue Date:	August 6, 2013	§	Customer No.: 47604
		§	
Filing Date:	November 14, 2011	§	
		§	
For:	ORGANIC LIGHT EMITTING DISPLAY HAVING THRESHOLD VOLTAGE COMPENSATION MECHANISM AND DRIVING METHOD THEREOF	§	

REQUEST *FOR EX PARTE* REEXAMINATION OF U.S. PATENT 8,502,757

Mail Stop "Ex *Parte* Reexam"
Attn: Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

Pursuant to the provisions of 35 U.S.C. §§ 301-307, BOE Technology Group Co., Ltd. ("Requester") hereby requests an *Ex Parte* Reexamination of claims 1, 11, 13 and 16 (the "Challenged Claims") of U.S. Patent No. 8,502,757 (the '757 patent, Ex. 1001), which issued on August 6, 2013 to AU Optronics Corp. from U.S. Patent Application 13/296,238 (the "'238 Application"), filed on November 15, 2011. The '757 patent claims priority to foreign Taiwanese Patent No. TW1436335 filed on March 17, 2011; therefore, the earliest possible priority date of the '757 patent is March 17, 2011.[1] The '757 patent is currently assigned to Optronic Sciences

[1] Because the references asserted herein qualify as prior art under the earliest possible priority date, Requester takes no position on whether the Challenged Claims are entitled to this earliest possible priority date..

LLC. ("Optronic" or "Patent Owner"). The most current assignment is recorded in the U.S. Patent and Trademark Office ("USPTO") at reel/frame 064658/0572.

Requester submits that this Request presents prior art references and analyses that are noncumulative of the prior art that was before the Examiner during the original prosecution of the '757 patent and that the Challenged Claims are invalid over these references. Requester therefore requests that an order for reexamination and an Office Action rejecting claims 1, 11, 13, and 16 be issued.

Ex Parte Patent Reexamination Filing Requirements

Pursuant to 37 C.F.R. § 1.510(b)(1), statements pointing out at least one substantial new question of patentability based on material, non-cumulative reference patents and printed publications for the Challenged Claims of the '757 patent are provided in Sections IV-VII of this Request.

Pursuant to 37 C.F.R. § 1.510(b)(2), reexamination of the Challenged Claims of the '757 patent is requested, and a detailed explanation of the pertinence and manner of applying the cited references to the Challenged Claims is provided in Section I.C of this Request.

Pursuant to 37 C.F.R. § 1.510(b)(3), copies of every patent or printed publication relied upon or referred to in the statement pointing out each substantial new question of patentability or in the detailed explanation of the pertinence and manner of applying the cited references are provided as Exhibits 1003-1008, and 1011-1013 of this Request.

Pursuant to 37 C.F.R. §1.510(b)(4), a copy of the '757 patent is provided as Exhibit 1001 ("EX1001") of this Request, as well as a copy of any disclaimer, certificate of correction, and reexamination certificate issued corresponding to the patent is included in Exhibit 1001.

Pursuant to 37 C.F.R. § 1.510(b)(5), the attached Certificate of Service indicates that a copy of this Request, in its entirety, has been served on Patent Owner at the following address of record for Patent Owner, in accordance with 37 C.F.R. § 1.33(c):

Michael J. Cherskov
903 Commerce Dr, Suite 310
Oak Brook, IL 60523

Also submitted herewith is the fee set forth in 37 C.F.R. § 1.20(c). Pursuant to 37 C.F.R. § 1.98(a), Requester certifies that no fee is due under 37 U.S.C. § 1.17(v) because there are fewer than 50 documents cited in the IDS accompanying this Request.

Pursuant to 37 C.F.R. § 1.510(b)(6), Requester hereby certifies that the statutory estoppel provisions of 35 U.S.C. § 315(e)(1) and 35 U.S.C. § 325(e)(1) do not prohibit Requester from filing this *ex parte* patent reexamination request.

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TABLE OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 8,502,757 ("**757 patent**")
1002	Declaration of R. Jacob Baker, Ph.D., P.E.
1003	File History of U.S. Patent No. 8,502,757
1004	U.S. 2007/0103406 ("**Kim406**")
1005	U.S. 2005/0110730 ("**Kim730**")
1006	U.S. 2009/0040150 ("**Senda**")
1007	R. Jacob Baker, et al., CMOS Circuit Design, Layout, and Simulations (1st ed. 1998)
1008	U.S. Pat. App. Pub. No. 2007/0170990 ("**Park**")
1009	Curriculum Vitae of Dr. R. Jacob Baker
1010	Patent Owner's Infringement Contentions for the '757 patent dated January 21, 2025
1011	Dong-Wook Park, et. al., *53.5: High-Speed AMOLED Pixel Circuit and Driving Scheme*, SID 10 Digest (2010).
1012	Jung Chul Kim, et. al., *A Novel OLED Pixel Circuit with Controllable Threshold Voltage Compensation Time*, IDW '19 (2019).
1013	Chih-Lung Lin, et. al., *Compensation Pixel Circuit to Improve Image Quality for Mobile AMOLED Displays*, IEEE Journal of Solid-State Circuits (2018).
1014	*Optronic Sciences LLC v. BOE Tech. Group Co., Ltd.*, Case No. 2:24-cv-557-JRG (E.D. Tex.), Dkt. 48, Joint Claim Construction and Prehearing Statement
1015	IPR2025-00239, Paper 10 ("**Patent Owner Preliminary Response**")
1016	IPR2025-00239, Paper 1 ("**Petition**")

I. SUBSTANTIAL NEW QUESTIONS OF PATENTABILITY

Prior to describing the substantial new questions of patentability presented in this Request, provided below is an overview of the Challenged Patent, a discussion of claim construction, and a summary of the prior art being discussed in the present Request.

A. U.S. Patent No. 8,502,757

1. Summary

The '757 patent relates generally "to an organic light emitting display, and more particularly, to an organic light emitting display having a threshold voltage compensation mechanism and driving method thereof." EX1001, 1:9-12. The '757 patent purports to improve on a prior art pixel driving circuit (EX1001, Figure 1) by adding reset and threshold voltage compensation mechanisms to avoid image retention and pixel brightness distortion. EX1001, 7:4-9 ("To sum up, with the *aid of the reset and threshold voltage compensation mechanism* according to the present invention described above, occurrences of image retention phenomenon and pixel brightness distortion can be avoided in the operation of the organic light emitting display, thereby achieving high image display quality on the OLED screen."), 1:26-27 ("Fig. 1 is a structure diagram schematically showing a prior-art active matrix organic light display 100."); EX1002, ¶46. The '757 patent discloses a pixel driving circuit having a reset and threshold voltage compensation mechanism with two embodiments—Figures 2 and 4. EX1001, 3:33-35 ("FIG. 2 is a structure diagram schematically showing an organic light emitting display 200 in accordance with a first embodiment."), 6:22-24 ("FIG. 4 is a structure diagram schematically showing an organic light emitting display 300 in accordance with a second embodiment.").

In the embodiment in Figure 2, the pixel driving unit includes the "first reset unit 235" and the "voltage adjustment unit 220." *Id.* 3:49-51. The "first reset unit 235 … is used for resetting the

driving voltage Vdr according to the second scan signal SS2_n and a first reference voltage Vref1." *Id.*, 4:2-5. The "voltage adjustment unit 220 … is put in use for adjusting the preliminary control voltage Vctr_p according to the emission signal EM_n and the first power voltage Vdd." EX1001, 3:57-61. Therefore, the embodiment in Figure 2 uses Vdd as the second reference voltage. *See* EX1001, Fig. 2 (unit 220 is transistor 221 with electrode connected to Vdd); EX1002, ¶47.

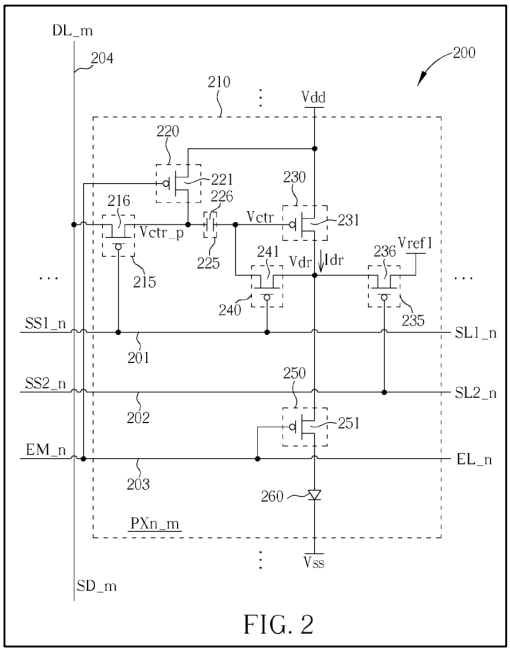


FIG. 2

In the embodiment in Figure 4, "organic light emitting display 300 is similar to the organic light emitting display 220 shown in FIG. 2" except the voltage adjustment unit uses "a second reference voltage Vref2." *See id.*, Fig. 4 (unit 320 is transistor 321 with electrode connected to Vref2), 6:22-36 (explaining that the voltage adjustment unit uses Vref2.).

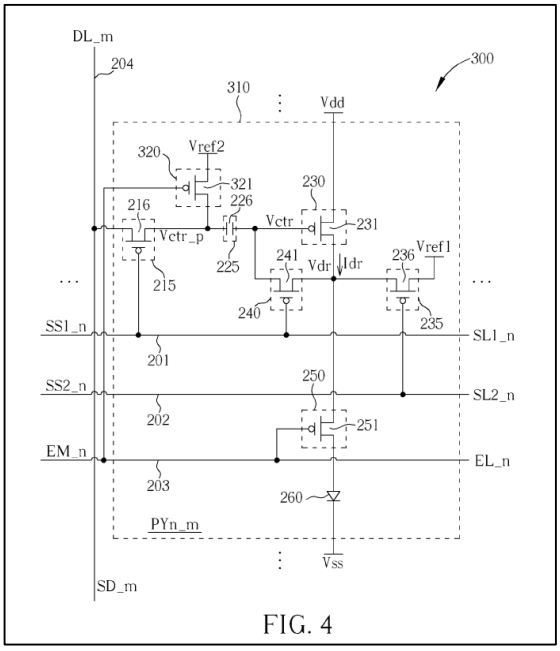


FIG. 4

The embodiments are otherwise identical, especially as it relates to the scan signals, scan lines, emission line, and transmission line. *Compare id.*, Fig. 2*, with* Fig. 4. The timing of the circuits in Figure 2 and Figure 4, which is the same for both, is provided in Figure 3 and accompanying text. EX1002, ¶47.

2. Prosecution History

The claims of the ’757 patent were allowed on the first office action (with amendments to claim 17 under *Ex Parte Quayle*). EX1003, 80-92 (April 25, 2013 Office Action). The Examiner found none of the prior art of record disclosed the voltage adjustment unit and first reset unit in combination with the other limitations of the claims. *Id.* The prior art asserted herein discloses those limitations as shown below, raising a substantial new question of patentability. EX1002, ¶48.

3. *Inter Partes* Review

The ’757 patent was the subject IPR2025-00239, filed by Requestor, challenging the claims in view of the prior art identified in this Request. However, the Petition (EX1016) was discretionarily denied by the Director of the USPTO before the merits could be addressed.

B. Level of Ordinary Skill in the Art

A person of ordinary skill in the art ("POSITA") at the time of the alleged invention of the '757 patent (March 17, 2011), and for that matter, at all subsequent times through the present, would have had a Bachelors' degree in electrical engineering or a comparable field of study, plus approximately one or more years of professional experience with electronic and optoelectronic system design. Additional graduate education could substitute for professional experience, and significant experience in the field could substitute for formal education. EX1002, ¶49.

C. Claim Construction

"During patent examination, the pending claims must be 'given their broadest reasonable interpretation consistent with the specification.'" M.P.E.P § 2111. The '757 patent has not yet expired and therefore, the broadest reasonable interpretation standard applies. *See* M.P.E.P. § 2258(G) ("During reexamination ordered under 35 U.S.C. 304 ... claims are given the broadest reasonable interpretation consistent with the specification and limitations in the specification are not read into the claims.") (internal citation omitted).

As explained below, the claims are invalid under their ordinary meaning (which Patent Owner proposes in the litigation) and under a proper means-plus-function construction (which Requestor proposes in the litigation). Requestor reserves the right to advocate different claim interpretations in other forums or proceedings if necessary.

1. Means-Plus-Function Limitations

Claim 1 recites several limitations that are subject to Section 112f—namely, limitations [1e], [1f], [1g], [1h], [1i], [1j], [1l].

Each of these limitations recite a "… unit … for" performing a claimed function. The lack of the word "means" raises the presumption that these terms are not subject to Section 112f, but

that presumption is rebutted because none of the terms recite sufficient structure for performing the claimed function. EX1002, ¶51.

Each term follows the same format: a functional qualifier, the nonce word "unit," an appositive reciting connections, and "for" followed by a function. By way of example, the "voltage adjustment unit" in limitation [1f] is reproduced below.

> a voltage adjustment unit, electrically connected to the transmission line and the input unit, for adjusting the preliminary control voltage according to the emission signal and a second reference voltage

EX1001, [1f]. EX1002, ¶52.

In each limitation, the initial functional qualifier is merely a shorthand paraphrasing of the function and does not impart structure to a POSITA. The word "unit" does not recite structure because it is merely a nonce word for any circuitry that would perform the function. The claimed connections add some limitations as to how the structure is connected but is not sufficient structure for performing the claimed function. The "for" clause then recites the function without any structure for performing the function. Thus, each limitation would not be recognized by one of ordinary skill in the art as reciting sufficiently definite structure for performing the claimed function. EX1002, ¶53.

Notwithstanding, in currently ongoing litigation between Requestor and Patent Owner (*Optronic Sciences LLC v. BOE Tech. Group Co., Ltd.*, Case No. 2:24-cv-557-JRG (E.D. Tex.); hereinafter, "*Optronic v. BOE* Litigation"), Patent Owner contends that each limitation is not subject to 112f. Accordingly, this Request applies the prior art under both the ordinary meaning of the claim and under the correct means-plus-function constructions. The prior art invalidates the claims under each construction. EX1002, ¶54.

Each limitation subject to 112f is presented below with its function underlined (the functions are entitled to their ordinary meaning and do not require further construction) followed by the corresponding structure disclosed and linked in the specification for performing the claimed function. EX1002, ¶55.

a. [1e] "an input unit…"

"[A]n input unit, electrically connected to the data line and the first scan line, for outputting a preliminary control voltage according to the data signal and the first scan signal[.]"

In the *Optronic v. BOE* Litigation, Patent Owner agrees that, if this limitation is subject to 112f, the function is the underlined text and the corresponding structure is as follows:

1) input unit 215 in Fig. 2 (3:54-57, 4:17-18, 4:34-38) and equivalents; or

2) input unit 215 in Fig. 4 (4:34-38, 5:13-15) and equivalents.

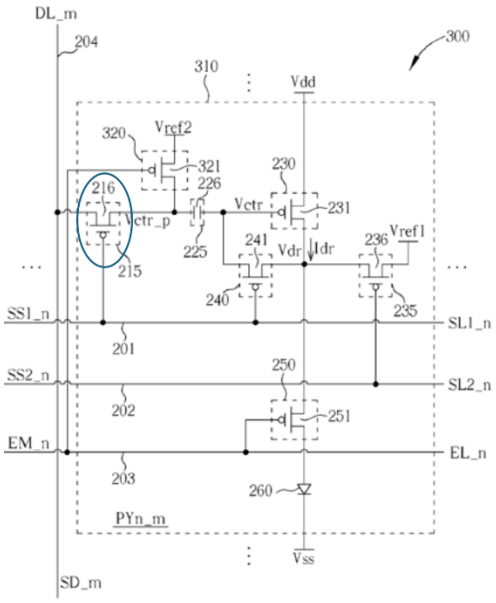


FIG. 4

This structure is linked to this function. EX1001, Fig. 3, 3:54-57, 4:17-18, 4:34-38, 5:13-15. EX1002, ¶¶56-57; EX1014, Exhibit A, pp.17-18.

In IPR2025-00239, Requestor identified substantively identical structure for this limitation using slightly different language. EX1016 at III.D.1.a (transistor 216 connected as disclosed in Figures 2, 4 and 4:34-38). The agreed structure includes a reference to the structure in Figure 4, which is identical to and redundant of the structure in Figure 2, so this is not a substantive change. These changes are a result of Requestor's effort to promote judicial economy in the *Optronic v. BOE* Litigation by agreeing to Patent Owner's substantively identical proposed structure for this limitation, should it be found subject to 112f.

b. [1f] "a voltage adjustment unit…"

"[A] voltage adjustment unit, electrically connected to the transmission line and the input unit, for adjusting the preliminary control voltage according to the emission signal and a second reference voltage[.]" In the *Optronic v. BOE* Litigation, Patent Owner agrees that, if this limitation is subject to 112f, the function is the underlined text and the corresponding structure is as follows:

1) voltage adjustment unit 220 in Fig. 2, (3:57-61, 4:54-58) and equivalents; or

2) voltage adjustment unit 320 in Fig. 4 (6:24-42) and equivalents.

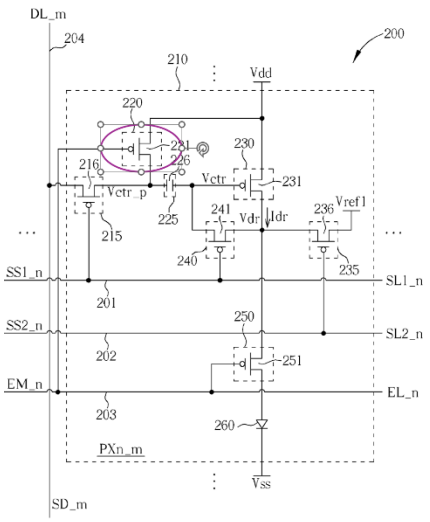


FIG. 2

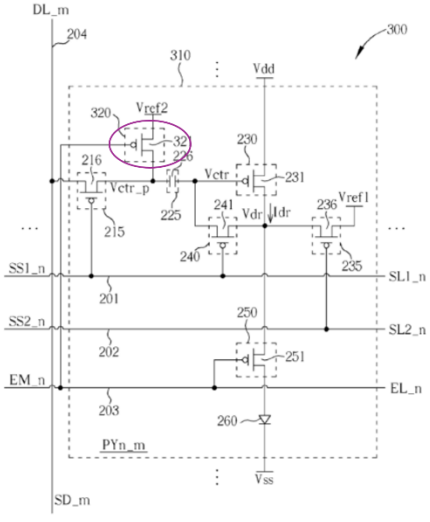


FIG. 4

Each of these structures is linked to this function. EX1001, Fig. 3, 3:58-61 (221), 4:34-38, 4:54-58, 5:45-55 (Vdd), 6:31-63 (321), 6:43-51 (Vref2). EX1002, ¶¶58-59; EX1014, Exhibit A, pp.18-19.

In IPR2025-00239, Requestor identified the substantively identical structure for this limitation using slightly different language. EX1016 at III.D.1.b (transistor 221 connected as disclosed in Figure 2 and 4:34-38 (to Vdd), or transistor 321 connected as disclosed in Figure 4 and 6:36-42 (to Vref2)). The differences are not substantive and were a compromise to promote judicial efficiency as described above.

c. [1g] "a couple unit…"

"[A] couple unit, electrically connected to the input unit and the voltage adjustment unit, for adjusting a control voltage through coupling a change of the preliminary control voltage[.]" In the *Optronic v. BOE* Litigation, Patent Owner agrees that, if this limitation is subject to 112f, the function is the underlined text and the corresponding structure is as follows:

1) coupling unit 225 in Fig. 2 (3:62-65, 4:18-19, 4:42-44) and equivalents; or

2) coupling unit 225 in Fig. 4 (4:42-44; 6:33-36, 6:47-50) and equivalents.

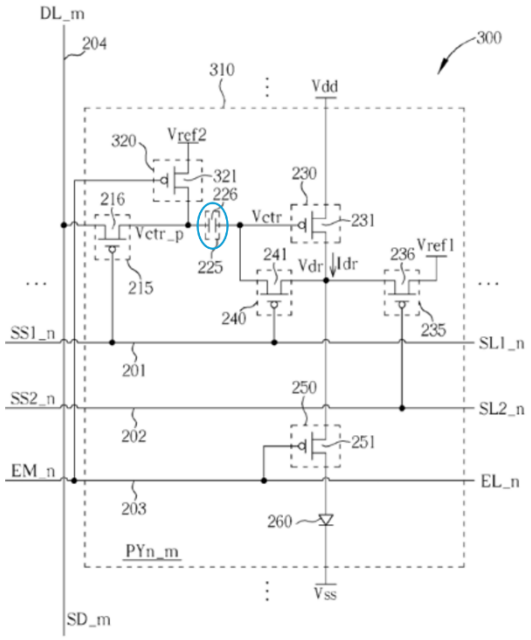


FIG. 4

This structure is linked to this function. EX1001, Fig. 3, 3:62-65, 4:18-19, 4:42-44, 5:50-55, 6:33-36, 6:46-51. EX1002, ¶¶60-61; EX1014, Exhibit A, pp.19-20.

In IPR2025-00239, Requestor identified the substantively identical structure for this limitation using slightly different language. EX1016 at III.D.1.c (capacitor 226 connected as disclosed in Figures 2 and 4 and 4:42-44). The differences are not substantive and were a compromise to promote judicial efficiency as described above.

d. [1h] "a driving unit…"

"[A] driving unit, electrically connected to the couple unit, <u>for providing a driving current and a driving voltage according to the control voltage and a first power voltage</u>[.]" In the *Optronic v. BOE* Litigation, Patent Owner agrees that, if this limitation is subject to 112f, the function is the underlined text and the corresponding structure is as follows:

1) driving unit 230 in Fig. 2 (3:65-4:2, 4:19-20, 4:38-41) and equivalents; or

2) driving unit 230 in Fig. 4 (4:38-41) and equivalents.

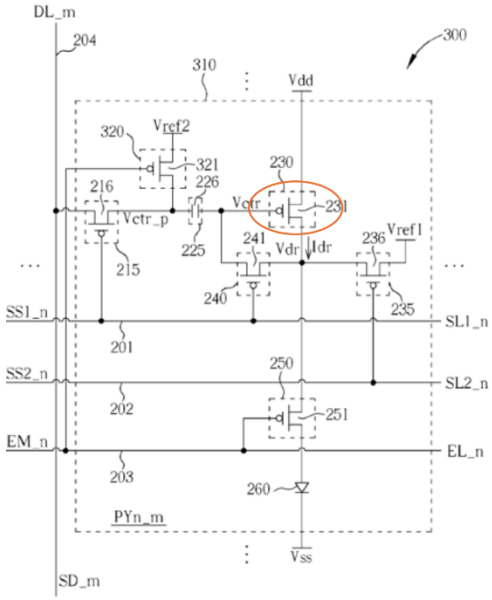


FIG. 4

This structure is linked to this function. EX1001, Fig. 3, 3:65-4:2, 4:19-20, 4:38-41, 5:56-60, 6:53-64; EX1002, ¶¶62-63; EX1014, Exhibit A, pp.20-21.

In IPR2025-00239, Requestor identified the substantively identical structure for this limitation using slightly different language. EX1016 at III.D.1.d (transistor 231 connected as disclosed in Figures 2, 4 and 4:38-41). The differences are not substantive and were a compromise to promote judicial efficiency as described above.

e. [1i] "a first reset unit…"

"[A] first reset unit, electrically connected to the driving unit and the second scan line, for resetting the driving voltage according to the second scan signal and a first reference voltage[.]" In the *Optronic v. BOE* Litigation, Patent Owner agrees that, if this limitation is subject to 112f, the function is the underlined text and the corresponding structure is as follows:

1) reset unit 235 in Fig. 2 (4:2-5, 4:20-31, 4:44-48) and equivalents; or

2) reset unit 235 in Fig. 4 (4:44-48) and equivalents.

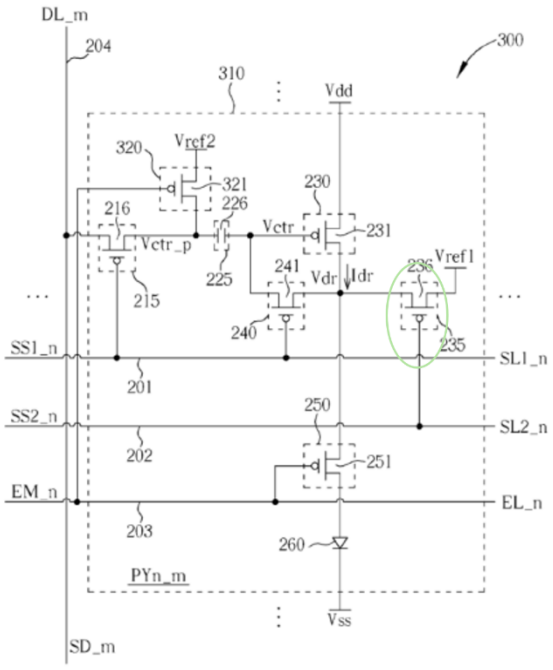


FIG. 4

This structure is linked to this function. EX1001, Fig. 3, 4:2-5, 4:20-31, 4:44-48; EX1002, ¶¶64-65; EX1014, Exhibit A, pp.21-22.

In IPR2025-00239, Requestor identified the substantively identical structure for this limitation using slightly different language. EX1016 at III.D.1.e (transistor 236 connected as disclosed in Figures 2, 4 and 4:44-48). The differences are not substantive and were a compromise to promote judicial efficiency as described above.

f. [1j] "a second reset unit…"

"[A] second reset unit, electrically connected to the driving unit, the first reset unit and the first scan line, <u>for resetting the control voltage according to the first scan signal and the driving voltage</u>[.]" In the *Optronic v. BOE* Litigation, Patent Owner agrees that, if this limitation is subject to 112f, the function is the underlined text and the corresponding structure is as follows:

1) reset unit 240 in Fig. 2 (4:5-9, 4:21, 4:48-52) and equivalents; or

2) reset unit 240 in Fig. 4 (4:48-52) and equivalents.

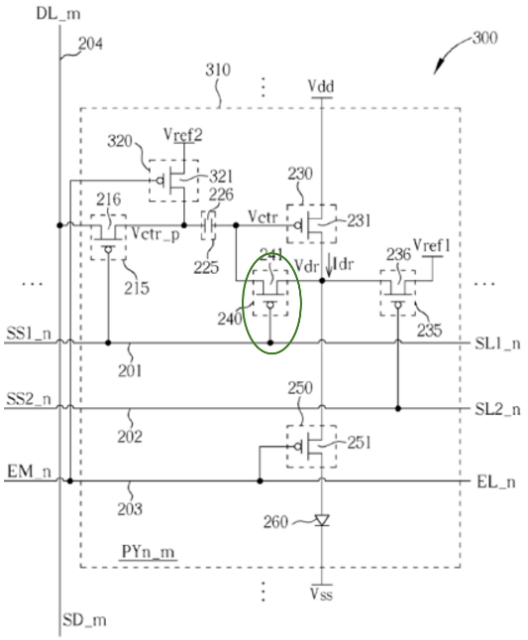


FIG. 4

This structure is linked to this function. EX1001, Fig. 3, 4:5-9, 4:21, 4:48-52; EX1002, ¶¶66-67; EX1014, Exhibit A, pp.22-23.

In IPR2025-00239, Requestor identified the substantively identical structure for this limitation using slightly different language. EX1016 at III.D.1.f (transistor 241 connected as disclosed in Figures 2, 4 and 4:48-52). The differences are not substantive and were a compromise to promote judicial efficiency as described above.

g. [1l] "an emission enable unit…"

"[A] n emission enable unit, electrically connected to the transmission line, the driving unit and the organic light emitting diode, for providing a control of furnishing the driving current to the organic light emitting diode according to the emission signal[.]" In the *Optronic v. BOE* Litigation, Patent Owner agrees that, if this limitation is subject to 112f, the function is the underlined text and the corresponding structure is as follows:

1) emission enable unit 250 in Fig. 2 (4:9-14, 4:23-24, 4:54-58) and equivalents; or

2) emission enable unit 250 in Fig. 4 (4:54-58) and equivalents.

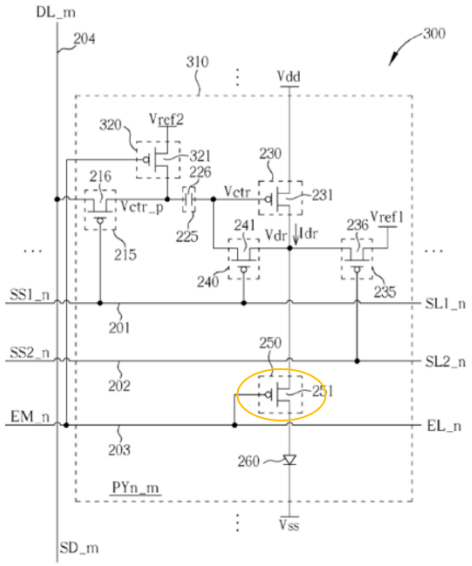


FIG. 4

This structure is linked to this function. EX1001, Fig. 3, 4:9-14, 4:23-24, 4:54-58; EX1002, ¶¶68-69; EX1014, Exhibit A, pp.23-24.

In IPR2025-00239, Requestor identified the substantively identical structure for this limitation using slightly different language. EX1016 at III.D.1.g (transistor 221 connected as disclosed in Figures 2, 4 and 4:54-58). The differences are not substantive and were a compromise to promote judicial efficiency as described above.

h. Abridged Claim Listing Summary

An abridged claim listing summarizing the 112f terms is reproduced below next to the corresponding structure as shown in Figure 4 (the alternative structure of 220/221 for the voltage adjustment unit in Figure 2 is not shown). EX1002, ¶70.

[1pre] An organic light emitting display, comprising:
[1a] a data line [DL_m];
[1b] a first scan line [SS1_n];
[1c] a second scan line [SS2_n];
[1d] a transmission line [EM_n];
[1e] an input unit [215/216]
[1f] a voltage adjustment unit [320/321]
[1g] a couple unit [225/226]
[1h] a driving unit [230/231]
[1i] a first reset unit [235/236]
[1j] a second reset unit [240/241]
[1k] an organic light emitting diode [260]
[1l] an emission enable unit [250/251]

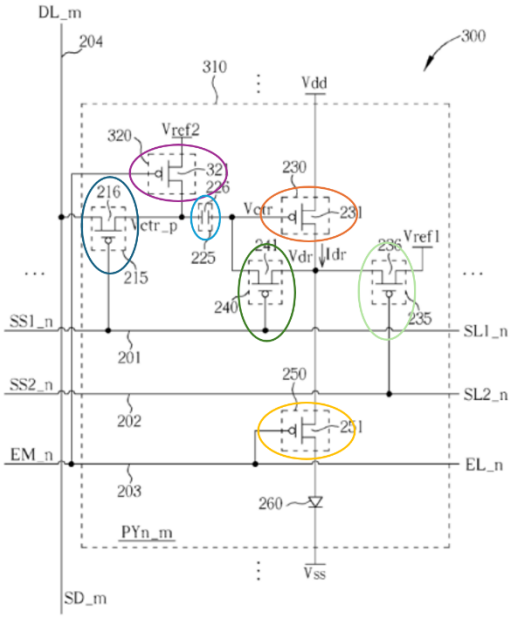


FIG. 4

2. "first/second reference voltage"

a. Primary Construction

In the *Optronic v. BOE* Litigation, Patent Owner agreed that the terms "first reference voltage" and "second reference voltage" should be construed in accordance with their plain and ordinary meaning, such that there is no requirement that the first and second voltages are different voltages. EX1014, p. 2.

This construction is consistent with the '757 patent's claims and specification. For example, the claims use "first" and "second" as labels to refer to two reference voltages in the independent claims. The claims themselves require that differently labelled voltages in the independent claims can be the same voltage or different voltages. For example, claim 1 recites a "second reference voltage" and a "first power voltage" and then dependent claim 13 recites "wherein the second reference voltage is the first power voltage." EX1001, claims 1, 13. Thus, differently labelled voltages in the independent claim (e.g., "first power voltage," "first reference voltage," "second reference voltage") can literally be the same voltage—no differentiation is

required. Of course, in the independent claim they can be different voltages and only dependent claim 13 requires two of the differently labelled voltages be the same voltage. There is no definition or disclaimer in the specification or file history that requires limiting the "first" and "second" reference voltages to only the same voltage or to only different voltages. The disclosed embodiments do not explicitly state, or implicitly require, that the reference voltages be different from each other, so it is not possible to read such a limitation in from the specification (which would be legally improper, even if it were possible). Finally, the ordinary meaning of "first" and "second" reference voltages encompasses reference voltages that are the same or different. *See. e.g.,* EX1007 (Figs. 29, 30); EX1008, [0039] (VREF1 and VREF2 may be the same or different voltage values). Thus, the claims encompass "first" and "second" reference voltages that are the same voltage or different voltages. EX1002, ¶71.

Before Patent Owner agreed in the district court to this construction, in IPR2025-00239, Patent Owner had previously argued that the claimed "first reference voltage" and "second reference voltage" required different "sources." *See* EX1015 (Patent Owner Preliminary Response), at 6-7. Patent Owner was wrong because the term "source," in the context of the claimed voltages, does not exist in the claims or the specification. *See generally* EX1001 & claim 1. Accordingly, Patent Owner's interpretation that the first and second reference voltage must have different sources improperly adds a limitation to the claims, and there is no cognizable justification for doing so. Indeed, the claims and embodiments preclude Patent Owner's previous argument of different "sources." As discussed above, dependent claim 13 requires that "the second reference voltage is the first power voltage." Thus, differently labelled voltages in the independent claim must encompass the possibility of voltages with the same source. In fact, this is the case for the

only disclosed embodiment of claim 13, wherein the "second reference voltage" and the "first power voltage" have the same source—Vdd. *See* EX1001, Fig. 2 (annotated):

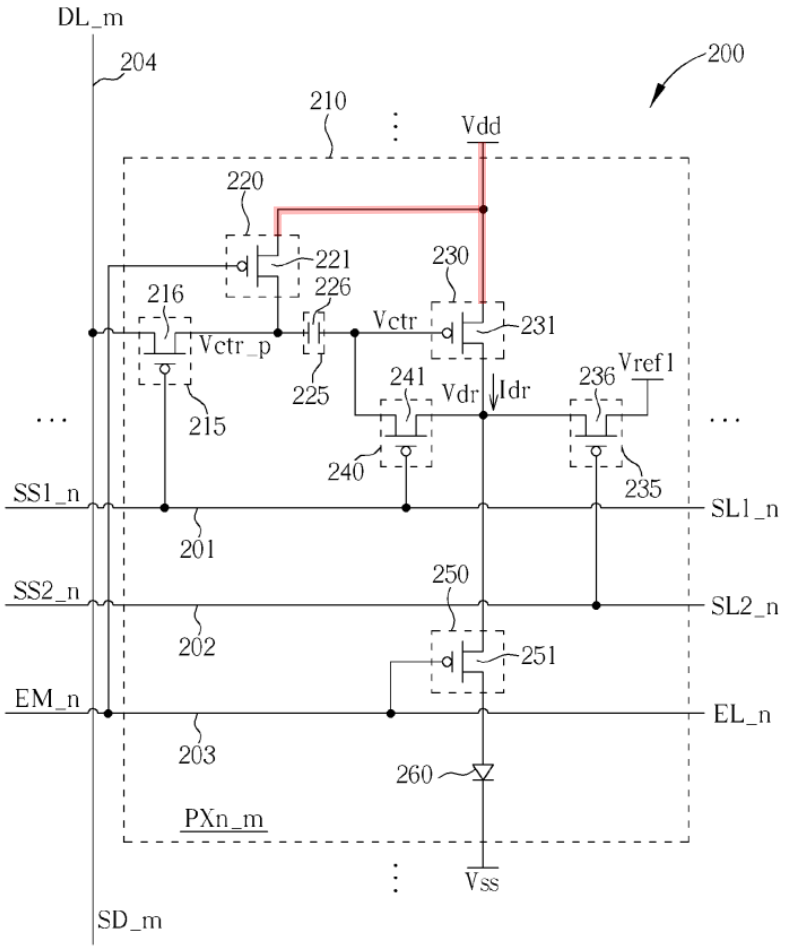


FIG. 2

EX1002, ¶72.

Finally, a POSITA would have understood that a "reference voltage," in the context of the '757 patent is a known voltage that is used to reset a node or circuit into a known state. EX1002, ¶73. *See* EX1001, 5:15-22 ("the first reset unit 235 resets the driving voltage Vdr according to … the first reference voltage Vref1, and the second reset unit 240 resets the control voltage Vctr according to … the driving voltage Vdr. In view of that, the driving operation of the driving unit 230 is reset for avoiding an occurrence of image retention phenomenon."), 5:26-29 ("At this time,

the second reset unit 240 and the driving unit 230 perform a threshold voltage compensation operation on the control voltage Vctr according to the first scan signal SS1_n and the first power voltage Vdd."). The unclaimed purpose of resetting the circuit by using a reference voltage in the embodiments disclosed in the '757 patent (and prior art Senda and Kim406 references) is to eliminate image retention (ghosting), which is the same unclaimed purpose for which it is used in the prior art asserted herein. EX1002, ¶73; *see also infra* Section IV.A.

b. Alternative Construction

Under an incorrect, alternative construction, the "first" and "second" voltages are limited to different voltages. EX1002, ¶74.

II. THE PRIOR ART REFERENCES PRESENT SUBSTANTIAL NEW QUESTIONS OF PATENTABILITY

A. Listing of Prior Art Patents

Reexamination of the Challenged Claims is requested in view of the following references:

- **EX1004 – Kim406:** U.S. Pat. App. Pub. 2007/0103406 to Kim406 was published on May 10, 2007 and is prior art under pre-AIA Section 102(b). EX1002, ¶75.
- **EX1005 – Kim730:** U.S. Pat. App. Pub. 2005/0110730 to Kim730 was published on May 26, 2005 and is prior art under pre-AIA Section 102(b). EX1002, ¶76.
- **EX1006 – Senda:** U.S. Pat. App. Pub. 2009/0040150 to Senda was published on February 12, 2000 and is prior art under pre-AIA Section 102(b). EX1002, ¶77.

None of the references listed above were cited during the original prosecution of, or considered during any previous examination of, the '757 patent. A Form SB-08 and copies of the cited references are submitted herewith.

B. The Prior Art Presents Substantial New Questions of Patentability

As shown below, the prior art references raise a new "substantial question of patentability" because "the teaching of the (prior art) patents and printed publications is such that a reasonable Examiner would consider the teaching to be important in deciding whether or not the claim is patentable." *See* MPEP § 2242. For example, the references discussed below and in further detail in the attached charts, when considered as an ordered combination, teach each limitation of the Challenged Claims (claims 1, 11, 13, and 16), even under very narrow means-plus-function constructions. The prior art includes two reset units to reset the internal voltages of the pixel between every frame to eliminate image retention, and a voltage compensation unit to compensate for variations in threshold voltage of the driving unit. In short, the prior art provides identical structures claimed in the claims to accomplish the two unclaimed purposes described in the '757 patent. Further, they are new; the combinations of prior art references asserted in this Request were not previously considered and address the subject matter the Examiner relied on in allowing the claims. Accordingly, the "same question of patentability as to the claim has not been decided by the Office in an earlier concluded examination or review of the patent" at least because none of the art referenced in this Request, as presented as combination herein, was before the Office during prosecution of the '757 patent or during a prior post-grant proceeding challenging any claim of the '757 patent, any of which that are known to Requester have been listed in Sections IV-VII, *infra*.

The table below summarizes the grounds of unpatentability presented in this Request, governed by pre-AIA 35 U.S.C. § 103. Requestor submits that the grounds below raise substantial new questions of patentability (SNQ) for at least one claim of the '757 patent.

SNQ	Claims	Stat. Basis	Prior Art
1	1, 11, 16	35 U.S.C. § 102	Kim406

2	1, 11, 13, and 16	35 U.S.C. § 103	Kim406 in view of Kim730
3	1, 11, 13, and 16	35 U.S.C. § 102 and § 103	Senda

1. Overview of Kim406

Kim406 "relates to a pixel and an organic light emitting display device using the same, and more particularly, to a pixel for displaying an image with uniform brightness and an organic light emitting display device using the same." EX1004, ¶3, Abstract.

2. Overview of Kim730

Kim730 "relates to a light emitting display and a driving method thereof. More specifically, the present invention relates to an organic electroluminescent (EL) display," also referred to as an "OLED." EX1005, ¶¶3, 7.

3. Overview of Senda

Senda "relates to a display device and more particularly to an electric current driving type display device such as an organic EL display or FED." EX1006, ¶1.

III. DETAILED APPLICATION OF THE PRIOR ART TO EVERY CLAIM FOR WHICH REEXAMINATION IS REQUESTED

The present Request presents proposed rejections based on the references Kim406, Kim730, and Senda.

Requester notes that the proposed rejections below are based on obviousness under 35 U.S.C. §§ 102 and 103. Regarding the proposed rejections under 35 U.S.C. § 103, Requester notes that, even if there are minor differences between cited disclosures of the prior art and the claimed concepts, the claims are still obvious, as a POSITA would not have appreciated "some new

synergy" or unexpected results from the limitations given the disclosures of the prior art and the general knowledge of a POSITA. *KSR Intern. Co. v. Teleflex Inc.*, 550 US 398, 417 (2007). When compared with the prior art described below and in light of the knowledge of a POSITA, any "differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains." 35 U.S.C. § 103.

The proposed rejections (SNQs) listed above are described below in further detail.

IV. SNQ 1: Kim406 Anticipates Claims 1, 11, and 16

A. The Two Unclaimed Purported Advantages of the '757 Patent Are Disclosed or Taught by Kim406 to a POSITA

Kim406 discloses to a POSITA the unclaimed purported advantages of 1) reducing image retention between frames and 2) threshold voltage compensation for consistent brightness. The circuit structure of Kim406 is the same as the circuit structure of the claims of the '757 patent and the working sequence is also the same as shown below, even under narrow 112f constructions. Thus, any argument by Patent Owner that Kim406 does not teach or achieve the two purported advantages just confirms the fact that those purported advantages are not claimed.

Regarding reducing image retention between frames, the '757 patent provides a reset operation to "avoid[] an occurrence of image retention phenomenon" wherein the gate voltage of a driving transistor is reset to a known voltage, thereby resetting the driving operation of the driving unit. EX1001, 5:15-22 ("the first reset unit 235 resets the driving voltage Vdr according to the second scan signal SS2_n and the first reference voltage Vref1 and the second reset unit 240 resets the control voltage Vctr according to the first scan signal SS1_n and the driving voltage Vdr. In view of that, the driving operation of the driving unit 230 is reset for avoiding an occurrence of image retention phenomenon"). Like the '757 patent, Kim406 discloses a substantively identical

reset operation wherein the gate voltage of a driving transistor is reset to a known voltage between each frame. EX1004, Figs. 6-7, [0058], [0063] (PMOS), [0064]; *see also infra* Section IV.B.11 (limitation 1.j) (resetting gate voltage N22 of driving transistor). A POSITA would have understood that, by resetting the voltage at the gate of the driving transistor to an initialization voltage between each frame as disclosed by Kim406, the information from the prior frame would be eliminated, thereby eliminating image retention. EX1002, ¶¶79-80. Further, in IPR2025-00239, Patent Owner argued that the circuit structure responsible for eliminating image retention phenomena is claimed in claim 1 of the '757 patent. EX1015, at 3-5. Because Kim406 discloses each limitation of claim 1, as explained below, Kim406 must likewise solve the image retention phenomena. EX1002, ¶80. Accordingly, a POSITA would have understood that Kim406 discloses, or at least teaches, reducing image retention between frames. *Id.*

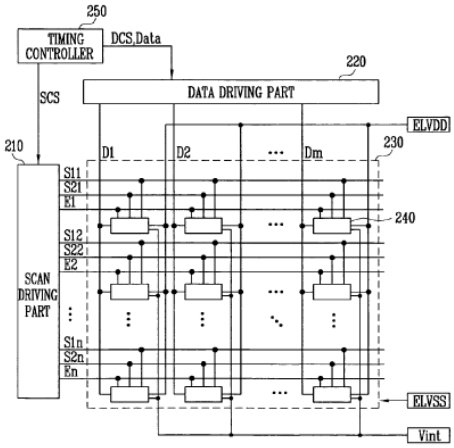
Regarding threshold voltage compensation for consistent brightness, Kim406 expressly teaches that a benefit of its disclosed invention is that it "can display an image with substantially uniform brightness regardless of the threshold voltages of the [transistors] used in each of the pixels []." EX1004, [0043]; *id.*, Abstract, [0003], [0011], [0069], [0071]. Accordingly, a POSITA would have understood that Kim406 discloses threshold voltage compensation for consistent brightness. EX1002, ¶81.

B. Claim 1

1. 1[pre]

Kim406 discloses "[a]n organic light emitting display, comprising (see following limitations)." EX1002, ¶82.

FIG. 5



EX1004, Title, Figs. 5-7, [0003], [0045] ("organic light emitting display device"), [0046]-[0072], claims 1-20; EX1002, ¶83.

2. [1a]

Kim406 discloses "a data line (Dm) for transmitting a data signal (data signal)." EX1002, ¶84.

FIG. 5

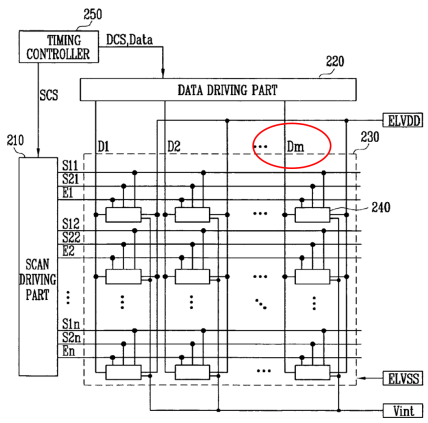
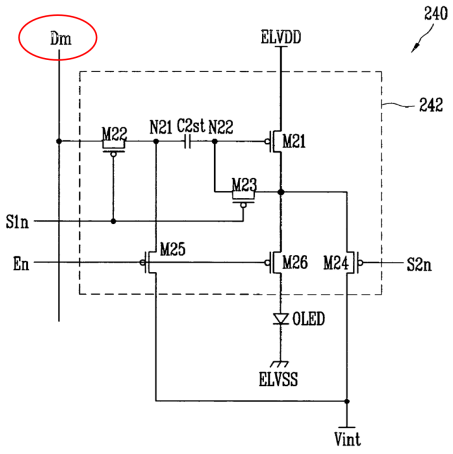


FIG. 6



EX1004, Figs. 5 (Data Driving Part 220 and lines D1 to Dm), Fig. 6 (line Dm), [0049] (Data Driving Part 220 sends data signals on data lines Dm), [0054] (pixel receives data signals from data lines Dm), [0064] (data signal supplied on Dm). EX1002, ¶85.

3. [1b]

Kim406 discloses "a first scan line (S1n) for transmitting a first scan signal (first scan signal)." EX1002, ¶86.

FIG. 5

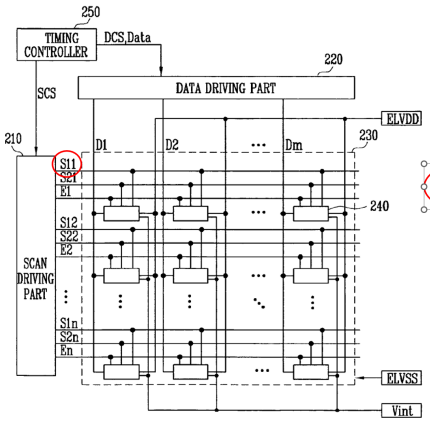
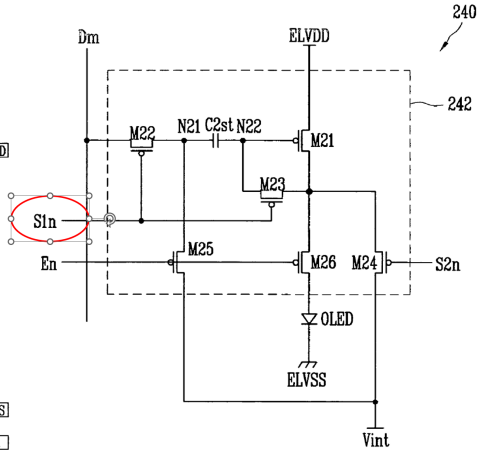


FIG. 6



EX1004, Figs. 5 (Scan Driving Part 210), Fig. 6 (S1n), Fig. 7 (S1n), [0048] (scan driving part 210 transmits first scan signal on S1n), [0054] (pixel receives first scan signal on S1n), [0062]-[0064] (first scan signal supplied on S1n). EX1002, ¶87.

4. [1c]

Kim406 discloses "a second scan line (S2n) for transmitting a second scan signal (second scan signal)." EX1002, ¶88.

FIG. 5

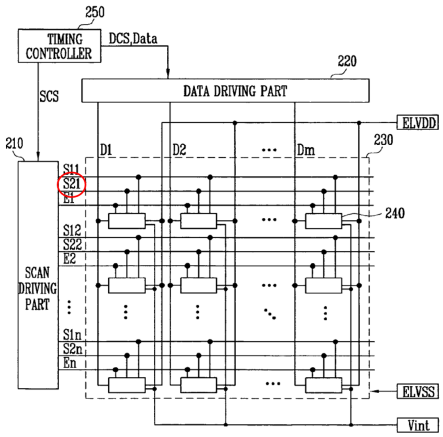
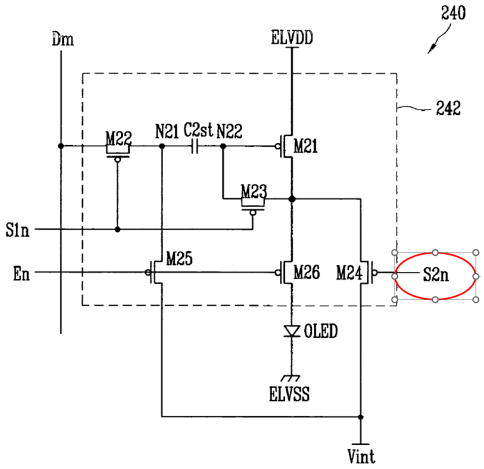


FIG. 6



EX1004, Fig. 5 (Scan Driving Part 210), Fig. 6 (S2n), Fig. 7 (S2n), [0048] (scan driving part 210 transmits second scan signal on S2n), [0054] (pixel receives second scan signal on S2n), [0062]-[0064] (second scan signal supplied on S2n). EX1002, ¶89.

5. [1d]

Kim406 discloses "a transmission line (En) for transmitting an emission signal (emission control signal)." EX1002, ¶90.

FIG. 5

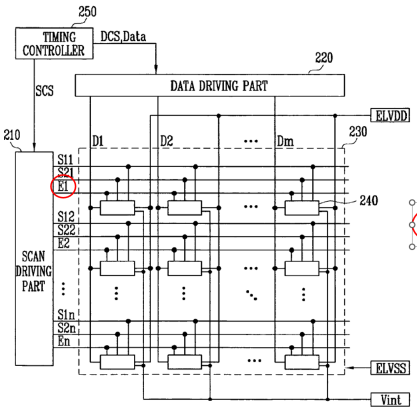
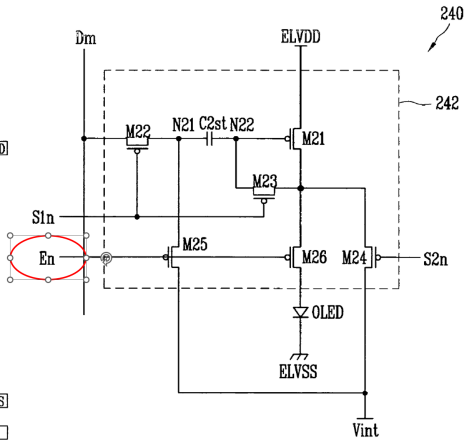


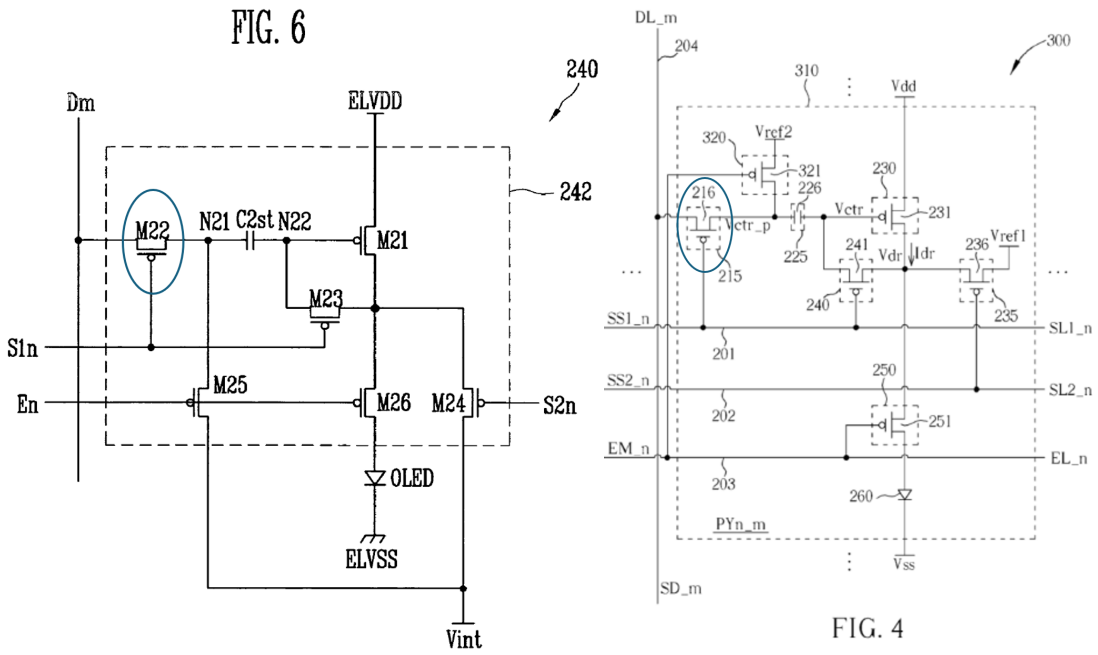
FIG. 6



EX1004, Fig. 5 (Scan Driving Part 210), Fig. 6 (En), Fig. 7 (En), [0048] (scan driving part 210 transmits emission control signal on En), [0062]-[0063], [0067] (emission control signal). EX1002, ¶91.

6. [1e]

Kim406 discloses "an input unit (M22), electrically connected to the data line (Dm) and the first scan line (S1n), for outputting a preliminary control voltage (outputting preliminary control voltage to node N21) according to the data signal (data signal on Dm) and the first scan signal (first scan signal on S1n)." EX1002, ¶92.



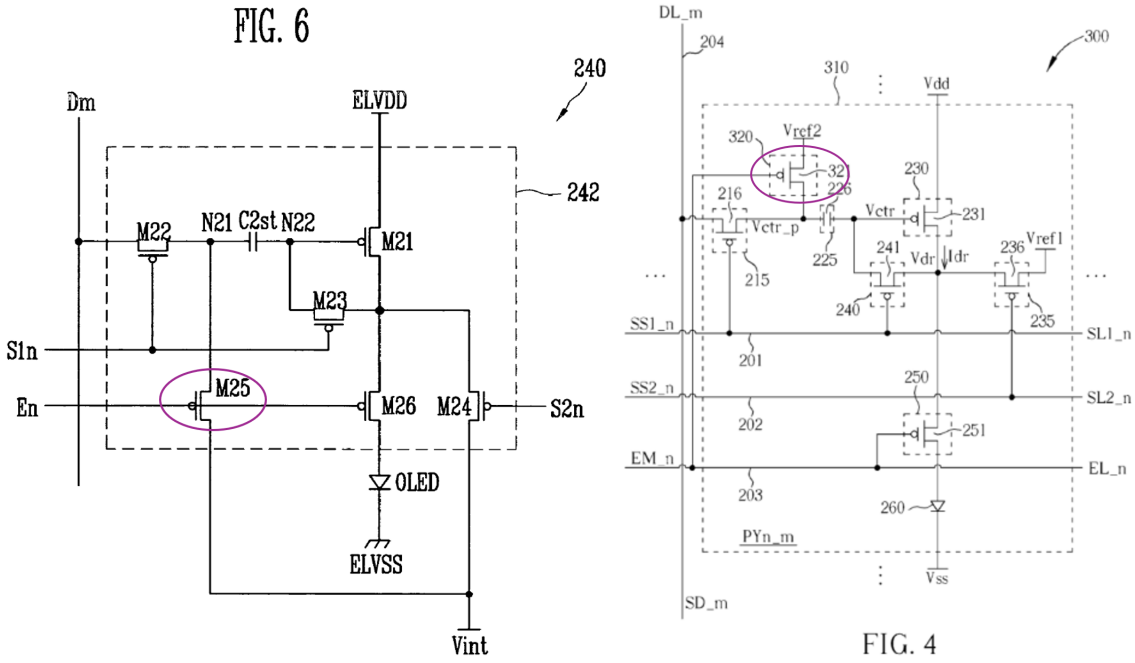
Annotated Kim406 Figure 6 (left) and '757 patent Figure 4 (right) are shown above. Kim406 discloses M22 is a PMOS transistor with a gate coupled to S1n, a first electrode coupled to the data line Dm, and a second electrode coupled to first node N21, such that during T2 and T3, M22 outputs a preliminary control voltage to the first node N21 according to the data signal on Dm and the low first scan signal on S1n. EX1004, Figs. 6-7, [0055], [0063] (PMOS), [0064] (T2 and T3). The second electrode of M22 is electrically connected to the voltage adjustment unit (M25) and couple unit (C2st). *Id.*, Fig. 6, [0055], [0059], [0061].

Under 112f, Kim406's PMOS transistor M22 as connected performs the claimed function and is identical to the corresponding structure for the input unit 215 (PMOS transistor 216 as connected). EX1001, Fig. 2, Fig. 4, 3:54-57, 4:17-18, 4:34-38, 5:13-15; EX1002, ¶93.

7. [1f]

Kim406 discloses "a voltage adjustment unit (M25), electrically connected to the transmission line (En) and the input unit (M22), for adjusting the preliminary control voltage

(voltage at N21) according to the emission signal (emission control signal on En) and a second reference voltage (Vint).” EX1002, ¶94.



Annotated Kim406 Figure 6 (left) and ’757 patent Figure 4 (right) are shown above. Kim406 discloses M25 is a PMOS transistor with a gate coupled to En, a first electrode connected to M22 and C2st (first node N21), and a second electrode coupled to initialization power source Vint, such that during T5, M25 adjusts the preliminary control voltage (voltage on first node N21) according to the low emission control signal on En and Vint. EX1004, Figs. 6-7, [0059], [0063] (PMOS), [0067] (when the fifth transistor M25 is turned on, the voltage value of the first node N21 is reduced to the voltage value of the initialization power source Vint). *See* EX1001, 5:47-52, 6:43-48.

Under 112f, Kim406’s PMOS transistor M25 as connected performs the claimed function and is identical to the corresponding structure for the voltage adjustment unit 320 disclosed in the ’757 patent (PMOS transistor 321 as connected). EX1001, Fig. 2, Fig. 4, 3:57-61, 4:54-58, 6:24-42; EX1002, ¶95.

Kim406 discloses M25 is connected to "Vint" while the corresponding structure 321 is connected to "Vref2," but this difference in naming convention is not relevant. Vint in Kim406 is a reference voltage because it is a known value used to reset the circuit into a known state, which is all that is required under the primary construction. Under the alternative construction, see below for [1i]. EX1002, ¶96.

Patent Owner's Incorrect Interpretation of "Reference Voltage" in IPR2025-00239

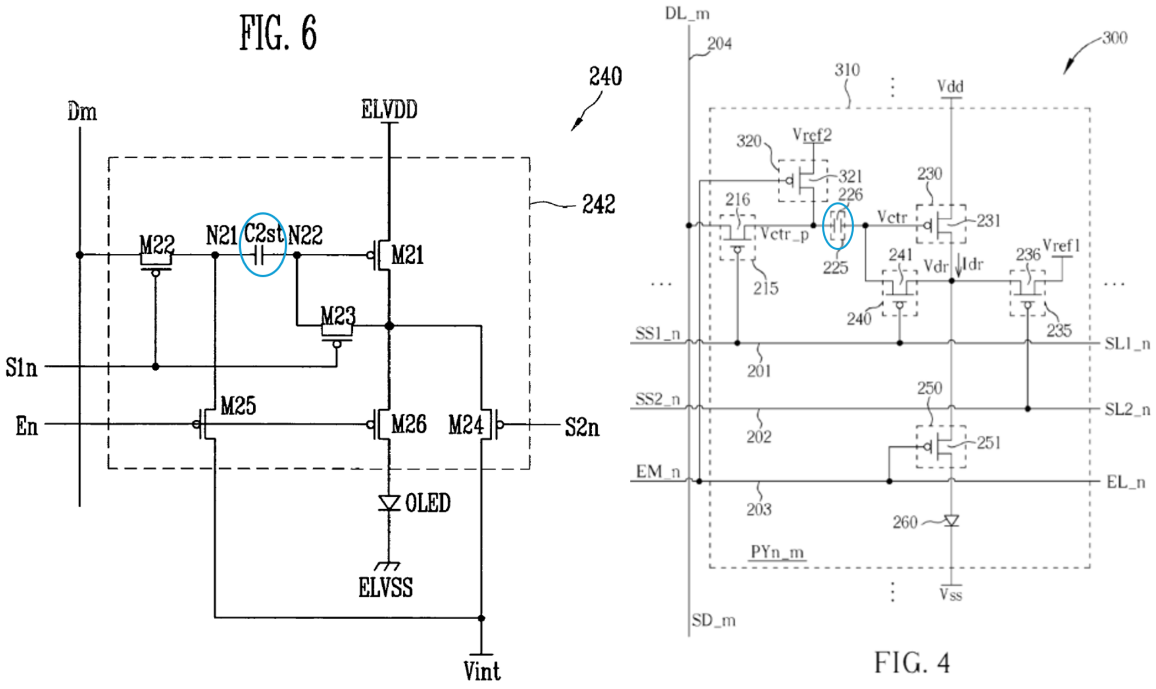
In IPR2025-00239, Patent Owner incorrectly asserted, without any explanation, that Kim406's initialization voltage Vint is not a reference voltage. EX1015, at 8. As discussed above in Section I.C.2 (claim construction), the proper interpretation of a "reference voltage" encompasses a voltage that provides a known reference, i.e., a known voltage. In both the '757 patent and Kim406, the reference/initialization voltage is a known (unstated) voltage and is used to reset a circuit to a known state. *See* Kim406 at [0059] ("When turned on, the fifth transistor M25 changes the voltage value of the first node N21 to the voltage value of the initialization power source Vint."). Thus, Vint is a known voltage used to reset a circuit to a known state (node N21 is reset to Vint each frame). EX1002, ¶¶95-96.

Additionally, as previously explained, the '757 patent's claims expressly provide that a "reference voltage" may be a "power voltage." EX1001, claims 1, 13. Put simply, the patent itself acknowledges that a voltage may be a reference voltage even if a different term is used to describe the voltage. There is no definition or disclaimer in the specification or file history that would require limiting "reference voltage" to only voltages expressly labelled as "reference."

8. [1g]

Kim406 discloses "a couple unit (C2st), electrically connected to the input unit (M22) and the voltage adjustment unit (M25), for adjusting a control voltage (voltage on N22) through

coupling a change of the preliminary control voltage (capacitor C2st couples the change of the preliminary control voltage at N21 to adjust the voltage at N22)." EX1002, ¶97.



Annotated Kim406 Figure 6 (left) and '757 patent Figure 4 (right) are shown above. Kim406 discloses storage capacitor C2st is between N21 and N22 and is charged during T3 to the voltage difference between N21 and N22. EX1004, Fig. 6, [0061], [0065]. N22 is floated in T4 and T5 by turning off M23, and in T5 when the preliminary control voltage at N21 is changed from the preliminary data signal voltage by application of Vint (*see* [1f]), capacitor C2st couples that change in voltage to N22, causing the voltage on N22 to change by the same amount. *Id.*, Fig. 7, [0066] (T4 turns off M22 and M23), [0067] (reducing voltage of N21 from data to Vint, and adjusting voltage of N22 with a reduction corresponding to the reduction of N21 to maintain a difference in C2st), [0069], claims 7 (second terminal (N22) floats), 8 (explaining how voltage at second terminal of capacitor (N22) is reduced corresponding to the voltage drop at first terminal (N21)). EX1002, ¶98.

Under 112f, Kim406's capacitor C2st as connected performs the claimed function and is identical to the corresponding structure for the couple unit 225 in the '757 patent (capacitor 226 as connected). EX1001, Fig. 2, Fig. 4, 3:62-65, 4:18-19; 4:42-44, 6:33-36, 6:47-50; EX1002, ¶99.

9. [1h]

Kim406 discloses "a driving unit (M21), electrically connected to the couple unit (C2st), for providing a driving current and a driving voltage (current and voltage at second electrode of M21), according to the control voltage (voltage at N22) and a first power voltage (ELVDD)." EX1002, ¶100.

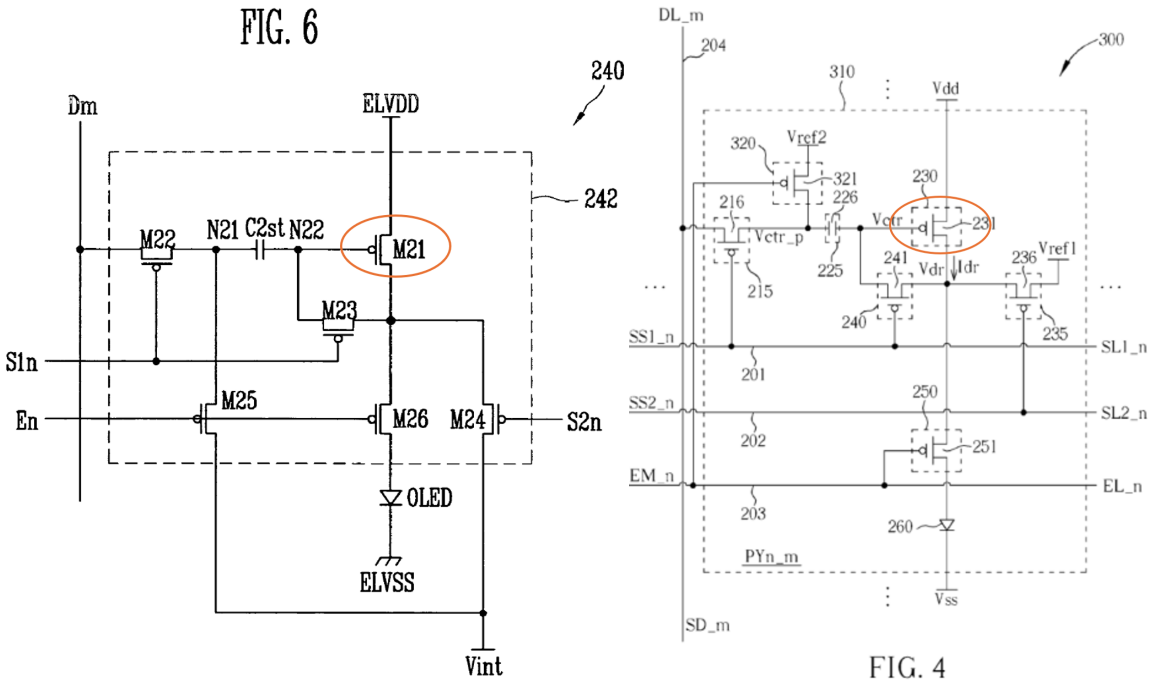


FIG. 4

Annotated Kim406 Figure 6 (left) and '757 patent Figure 4 (right) are shown above. Kim406 discloses M21 is a PMOS transistor with a gate coupled to C2st via node N22, a first electrode coupled to ELVDD, and a second electrode coupled to an unlabeled node with M23, M24, and M26, such that during T5 when M21 is turned on by the control voltage at N22 and EN turns on M26, M21 provides a driving current and driving voltage at its second electrode. EX1004, Figs. 6-7, [0056], [0063] (PMOS), [0067]-[0070] (describing M21 driving OLED through M26).

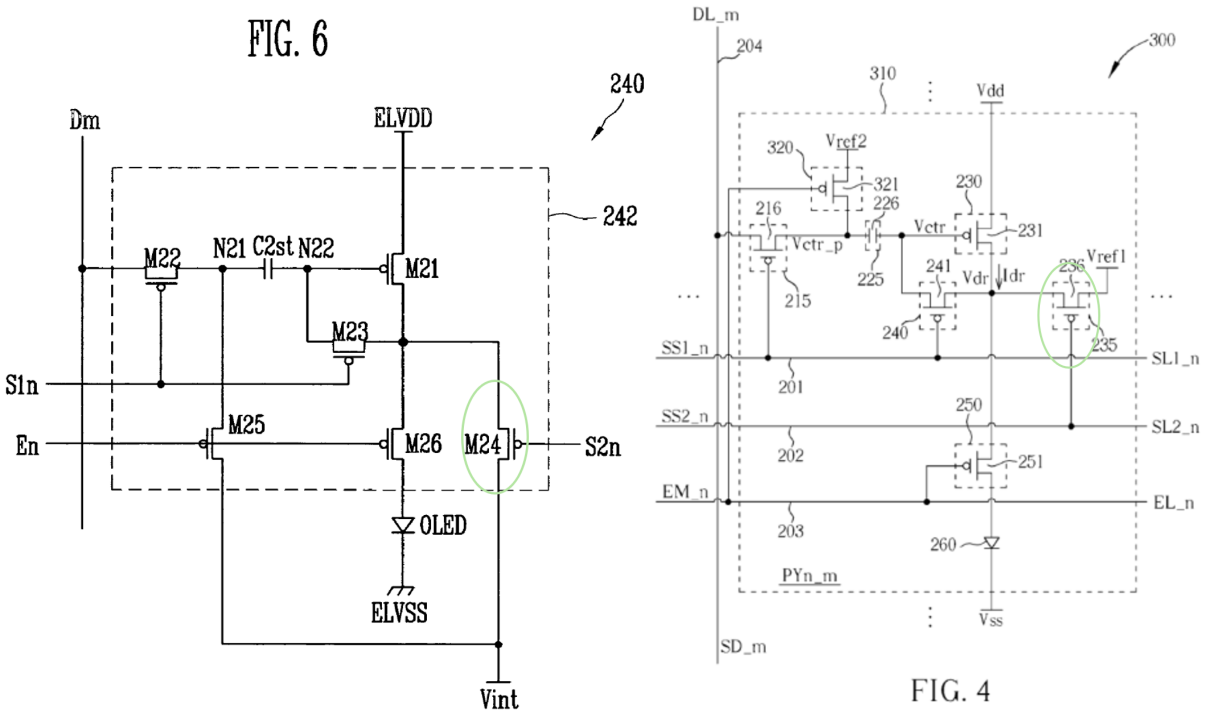
Under 112f, Kim406's PMOS transistor M21 as connected performs the claimed function and is identical to the corresponding structure for the driving unit 230 disclosed in the '757 patent (PMOS transistor 231 as connected). EX1001, Fig. 2, Fig. 4, 3:65-4:2, 4:19-20, 4:38-41; EX1002, ¶101.

Kim406 explicitly discloses that M21 provides a driving current at its second electrode which, during T5 when M26 is on, will drive the OLED. EX1004, Fig. 7, [0056], [0067]-[0070]. And Kim406 discloses that driving current provided by M21 is provided according to ELVDD and the control voltage at N22 applied to the gate of M21. *Id.*; EX1002, ¶102.

Kim406 inherently discloses that M21 provides a "driving voltage." A POSITA would have known it was inherent from the electrical properties of Kim406's circuit that M21 is also providing a driving voltage with the driving current. To provide a driving current as disclosed in Kim406 a POSITA would have known that there must also be a driving voltage, i.e., the difference in potential between the second electrode of M21 and ELVSS. A POSITA would have known that without that difference in potential, there would be no driving current as disclosed in Kim406 and the OLED would not emit light. A POSITA would have known that the precise magnitude of the driving voltage provided by M21 would be ELVDD minus the voltage drop across M21. EX1004, [0065], [0069]; EX1002, ¶103 (explaining diode equation).

10. [1i]

Kim406 discloses "a first reset unit (M24), electrically connected to the driving unit (M21) and the second scan line (S2n), for resetting the driving voltage (voltage at second electrode of M21) according to the second scan signal (S2n) and a first reference voltage (Vint)." EX1002, ¶104.



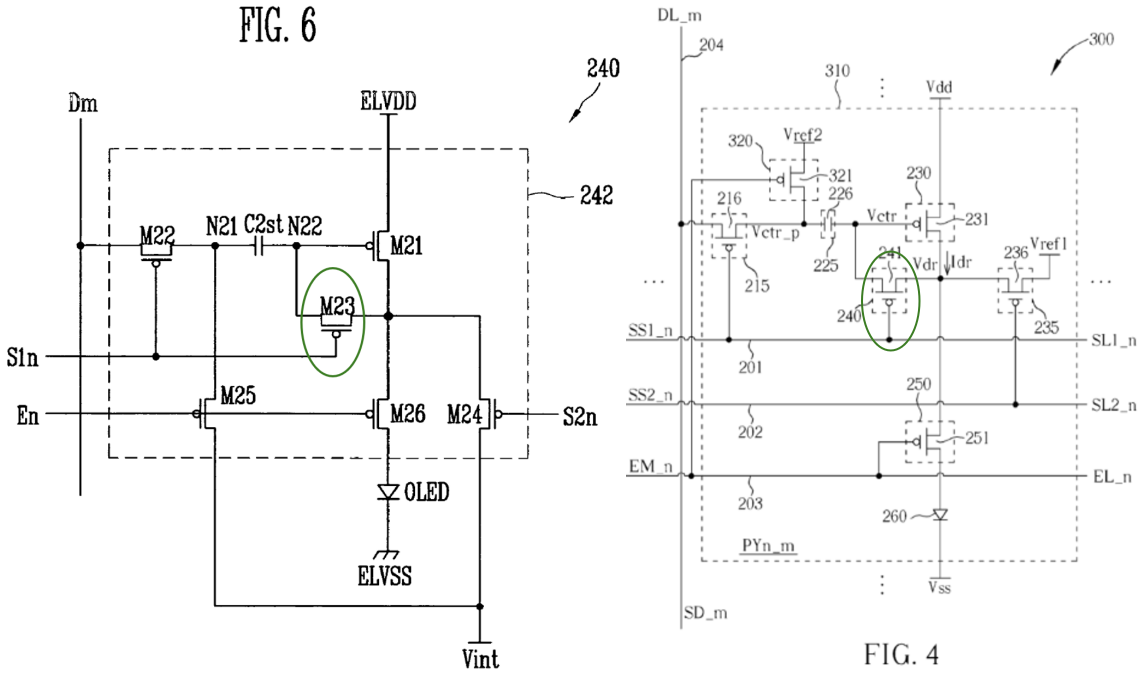
Annotated Kim406 Figure 6 (left) and '757 patent Figure 4 (right) are shown above. Kim406 discloses M24 is a PMOS transistor with a gate coupled to S2n, a first electrode coupled to the second electrode of M21 (and first electrode of M23 and first electrode of M26), and a second electrode coupled to the initialization power source Vint, such that during T2 when M24 is turned on by the second scan signal on S2n, it resets the driving voltage at the second electrode of M21 to Vint. EX1004, Figs. 6-7, [0058], [0063] (PMOS), [0064] (disclosing how during T2 M24 provides Vint to the node including the second electrode of M21, so that M23 can provide Vint to N22). *See* EX1001, 5:16-22. Vint provides a first reference voltage for M24 and a second reference voltage for M25 under the primary construction that encompasses the same voltage.

Under 112f, Kim406's PMOS transistor M24 as connected performs the claimed function and is identical to the corresponding structure for the first reset unit 235 disclosed in the '757 patent (PMOS transistor 236 as connected). EX1001, Fig. 2, Fig. 4, 4:2-5, 4:20-31, 4:44-48; EX1002, ¶105.

Kim406 discloses M24 is connected to "Vint" while the corresponding structure 236 is connected to "Vref1," but this difference in naming convention is not relevant. Vint in Kim406 is a reference voltage because it is a known value used to reset the circuit into a known state, which is all that is required under the primary construction. *See supra* Section IV.B.8 (discussing proper interpretation of "reference voltage"); EX1002, ¶106.

11. [1j]

Kim406 discloses "a second reset unit (M23), electrically connected to the driving unit (M21), the first reset unit (M24), and the first scan line (S1n), for resetting the control voltage (voltage at N22) according to the first scan signal (S1n) and the driving voltage (voltage at second electrode of M21)." EX1002, ¶107.



Annotated Kim406 Figure 6 (left) and '757 patent Figure 4 (right) are shown above. Kim406 discloses M23 is a PMOS transistor with a gate coupled to S1n, a first electrode coupled to the second electrode of M21 (and M24 and M26), and a second electrode coupled to the gate of the M21 and C2st (N22), such that when M23 is turned on by the first scan signal on S1n, the driving

voltage (voltage at second electrode of M21) is applied to reset the control voltage at N22. EX1004, Figs. 6-7, [0057], [0063]-[0065]. EX1002, ¶108.

During T2, the control voltage (N22) is reset according to low scan signal (S1n) and the driving voltage Vint (voltage at second electrode of M21). Specifically, S1n and S2n are supplied turning M23 and M24 on, such that the voltage on Node N22 is reset to Vint. EX1004, Figs. 6-7, [0064]; EX1002, ¶109.

During T3, the control voltage (N22) is reset according to low scan signal (S1n) and the driving voltage ELVDD-|Vth| (voltage at second electrode of M21). Specifically, S1n is still supplied keeping M23 on, but S2n is not supplied and M24 is turned off, such that the voltage on Node N22 is reset to ELVDD-|Vth|. EX1004, Figs. 6-7, [0065] (disclosing how current flows through M21 as a diode until "the voltage value of the second node N22 is obtained by subtracting the threshold voltage value of the first transistor M21 from the voltage value of the first power source ELVDD"). Kim406 discloses this reset is performed to compensate for the threshold voltage of M21. *Id.*, [0067]-[0069]; EX1002, ¶110.

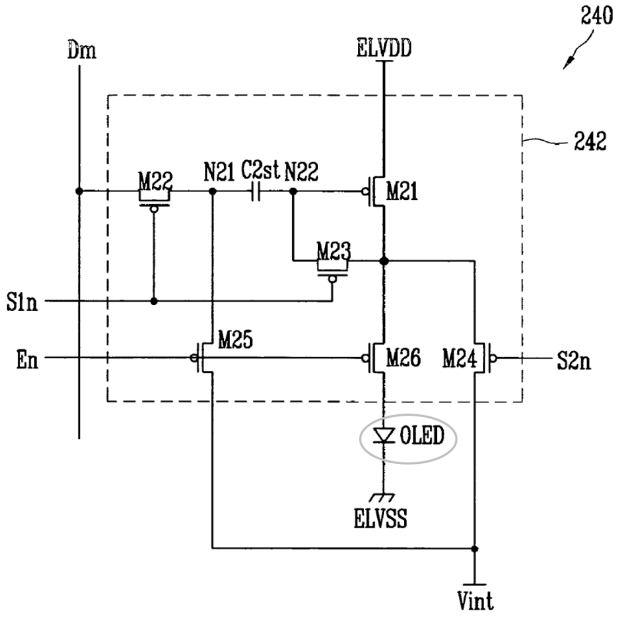
Kim406's disclosure in this regard is identical to the disclosure of the '757 patent wherein during T1, Vctrl is reset to Vref1 through 236 and 241 to ensure the driving transistor is in a conductive state, and during T2, Vctrl is reset to VDD-|Vth| through 241 to compensate for the threshold voltage of the driving transistor. EX1001, Fig. 3, 5:15-22 (T1), 5:23-38 (T2). EX1002, ¶111.

Under 112f, Kim406's PMOS transistor M23 as connected performs the claimed function and is identical to the corresponding structure for the second reset unit 240 disclosed in the '757 patent (PMOS transistor 241 as connected). EX1001, Fig. 2, Fig. 4, 4:5-9, 4:21, 4:48-52; EX1002, ¶112.

12. [1k]

Kim406 discloses "an organic light emitting diode (OLED) for generating output light according to the driving current." EX1002, ¶113.

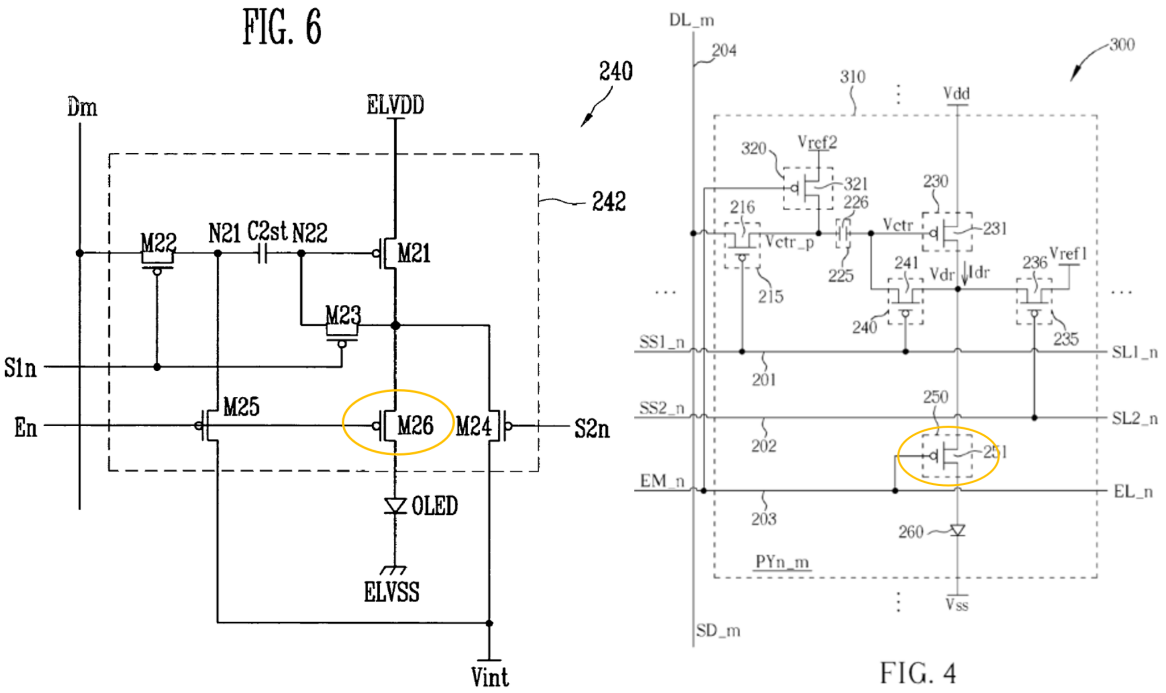
FIG. 6



Kim406 discloses that the OLED is driven by the driving current provided by M21 to generate output light. EX1004, Fig. 6, [0052]-[0054], [0056], [0060], [0067]-[0070]. The amount of control voltage at N22 on the gate of M21 determines the amount of driving current M21 provides and, therefore, the brightness of the OLED. *Id.* EX1002, ¶114.

13. [1l]

Kim406 discloses "an emission enable unit (M26), electrically connected to the transmission line (En), the driving unit (M21), and the organic light emitting diode (OLED), for providing a control of furnishing the driving current to the organic light emitting diode according to the emission signal (En)." EX1002, ¶115.



Annotated Kim406 Figure 6 (left) and ’757 patent Figure 4 (right) are shown above. Kim406 discloses M26 is a PMOS transistor with a gate coupled to En, a first electrode coupled to the second electrode of M21 (and M23 and M24), and a second electrode coupled to the anode of the OLED, such that during T5 when M26 is turned on by the emission control signal on En, it furnishes the driving current from the second electrode of M21 to the OLED. EX1004, Figs. 6-7, [0060], [0063] (PMOS), [0067]-[0070] (disclosing how during T5 the low emission control signal causes M26 to turn on such that the driving current from the second electrode of M21 flows through M26 and drives the OLED).

Under 112f, Kim406’s PMOS transistor M26 as connected performs the claimed function and is identical to the corresponding structure for the emission enable unit 250 disclosed in the ’757 patent (PMOS transistor 251 as connected). EX1001, Fig. 2, Fig. 4, 4:9-14, 4:23-24, 4:54-58; EX1002, ¶116.

C. Claim 11:

Kim406 discloses claim 1 "wherein the voltage adjustment unit (M25) comprises a fifth transistor (M25), the fifth transistor having a first end for receiving the second reference voltage (Vint), a gate end electrically connected to the transmission line (En), and a second end electrically connected to the input unit (M22) and the couple unit (C2st)." *See* [1f], [1e]-[1g]. EX1002, ¶117.

D. Claim 16:

Kim406 discloses claim 1 "wherein the organic light emitting diode (OLED) comprises an anode electrically connected to the emission enable unit (M26) and a cathode for receiving a second power voltage (ELVSS)." *See* [1k]; EX1004, Fig. 6, [0053] ("The anode electrode of the OLED is coupled to the pixel circuit 242 and the cathode electrode of the OLED is coupled to the second power source ELVSS."); EX1002, ¶118.

V. SNQ 2: Claims 1, 11, 13, and 16 are Obvious Over the Combination of Kim406 and Kim730

Kim406 discloses the second reference voltage is Vint. *See* [1f]. It would have been obvious to a POSITA that Vint could have been ELVDD, the first power voltage. EX1002, ¶119.

A. Combination Rationale

Kim730 shares the common inventor with Kim406 and discloses similar OLED pixel driving circuits. EX1002, ¶120.

FIG.8

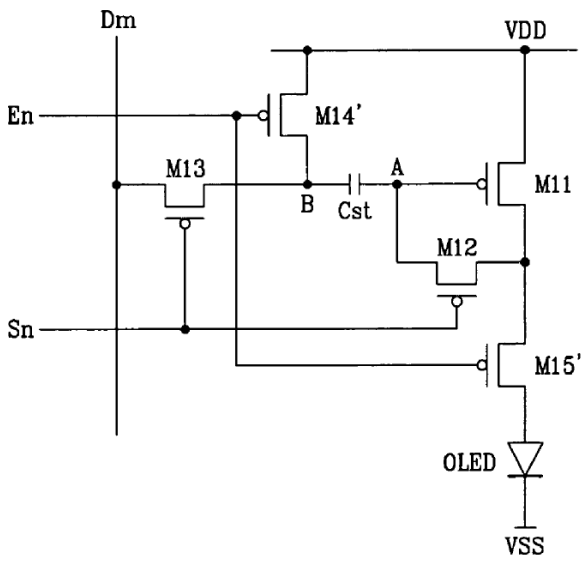
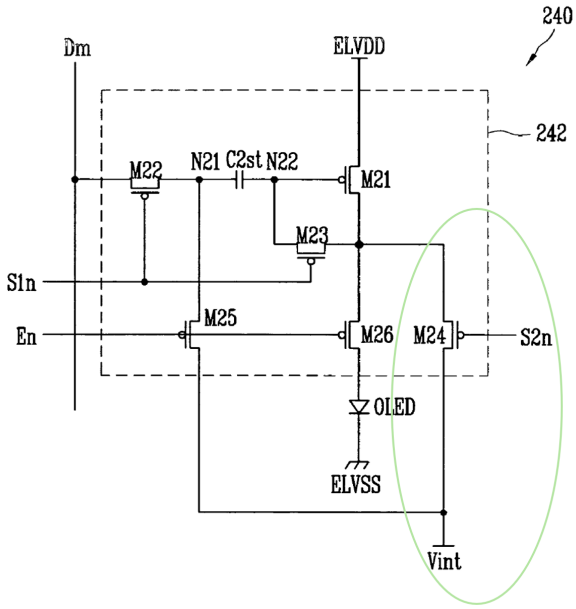


FIG. 6



Above are Figure 8 (left) of Kim730 and Figure 6 (right) of Kim406. The differences in the circuits are 1) Kim730's voltage adjustment unit (M14') is connected to VDD while Kim406's (M25) is connected to Vint and 2) Kim406 includes a first reset unit M24 for resetting the driving voltage using S2n, first reference voltage Vint and also as a second reference voltage Vint for M25. EX1002, ¶121.

It would have been obvious to a POSITA to modify the adjustment unit in Kim406 (M25) to use VDD as the reference voltage, instead of Vint, based on the teachings of Kim730. Kim730 explains how the voltage adjustment unit M14' can be connected to VDD to make a voltage adjustment. EX1005, Figs. 7-8, [0052]-[0060], [0067]. Kim730 explains how M14' can be connected to a third voltage "V_{sus}" to make a voltage adjustment. *Id.*, Fig. 10 [0062]-[0068]. Thus, a POSITA would have understood each of these options was a known design choice. And because it was known to connect voltage adjustment units to VDD, VSS, or a third voltage source, none of those design choices is novel or non-obvious. In the combination a POSITA would have also understood to continue to use Vint (instead of VDD) at M24 to ensure M23 and M24 ensure M21

is put in a conductive state for reset as disclosed by Kim406 and because the voltage value of the "initialization power source Vint is set to be smaller than the voltage value of the data signal" which would not be true for VDD. EX1004, [0064]; EX1002, ¶122.

A POSITA would also have been motivated to use different reference voltage sources for each unit in order to use the optimum reference voltage for that unit to improve the efficiency and performance of the pixel circuit. Each of these voltage adjustments is different. Thus, using a reference voltage that is tailored to each particular desired voltage adjustment would improve the speed of the pixel circuit and reduce the overall power consumption of the pixel circuit. It was known that using different reference voltage sources would also reduce the voltage swing for driving the OLED display. A POSITA would have known of these advantages and how significant they can become for large displays with thousands or millions of pixels. EX1002, ¶123.

A POSITA would have had a reasonable expectation of success in making the modification. Kim730 teaches it was a known technique in the art to use VDD to perform a positive voltage adjustment and that each of the design choices could be used for a circuit. EX1004, Figs. 6-10 and accompanying text. EX1002, ¶124.

Despite the above, in IPR2025-00239, Patent Owner argued that there is not adequate motivation to combine Kim406 and Kim730 because "the inquiry of what would be obvious to a hypothetical POSITA is easy because it is not hypothetical—the common inventor of Kim had both references in front of him and did not find it obvious to provide an embodiment with the combination [Requestor] proposes." EX1015, p. 9. The fact that the inventor chose to illustrate one of the two obvious implementations in Kim730 and the other in Kim406 does not mean that either one of those implementations is nonobvious. Moreover, this argument regarding the subjective decision of the patentee is clearly legally improper because "[t]he question is ***not***

whether the combination was obvious to the patentee but whether the combination was obvious to a person with ordinary skill in the art." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 420, 127 S. Ct. 1727, 1742 (2007) (emphasis added).

1. The Combination for Claim 13 Under the Primary Construction of "first/second reference voltage"

The combination discloses "the organic light emitting display of claim 11, wherein the second reference voltage is the first power voltage" (claim 13). *See* Ground 1, claim 11. In this combination, Kim406's voltage adjustment unit (M25) would have been connected to the first power voltage ELVDD in Kim406, based on the teachings in Kim730 as explained above. *See* [1f] (M25 connected to Vint), 11 (same); EX1005, Figs. 7-8, [0052]-[0061]; EX1002, ¶125.

2. The Combination for Claims 1, 11, 13, 16 Under the Alternative Construction of "first/second reference voltage"

Under the alternative construction that requires the first and second voltages in independent claim 1 to be different voltages, claims 1, 11, 13, and 16 are rendered obvious by the combination because, in the combination, the first reference voltage is still Vint as taught by Kim406, while the second reference voltage has been changed to VDD as taught by Kim730 as explained above. EX1002, ¶126.

VI. SNQ 3: Claims 1, 11, 13, and 16 are Anticipated or at least Rendered Obvious by Senda

A. The Two Unclaimed Purported Advantages of the '757 Patent Are Disclosed by Senda to a POSITA

Senda discloses the unclaimed purported advantages of 1) reducing image retention between frames and 2) threshold voltage compensation for consistent brightness. The circuit structure of Senda is the same as the circuit structure of the claims of the '757 patent and the working sequence is also the same as shown below, even under narrow 112f constructions. Thus,

any argument by Patent Owner that Senda does not teach or achieve the two purported advantages just confirms the fact that those purported advantages are not claimed.

Regarding reducing image retention between frames, the '757 patent provides a reset operation to "avoid[] an occurrence of image retention phenomenon" wherein the gate voltage of a driving transistor is reset to a known voltage, thereby resetting the driving operation of the driving unit. EX1001, 5:13-22 ("the first reset unit 235 resets the driving voltage Vdr according to the second scan signal SS2_n and the first reference voltage Vref1 and the second reset unit 240 resets the control voltage Vctr according to the first scan signal SS1_n and the driving voltage Vdr. In view of that, the driving operation of the driving unit 230 is reset for avoiding an occurrence of image retention phenomenon").

Senda explicitly addresses the image retention (ghosting) issue in the prior art and discloses the claimed reset units to minimize it. For example, Senda, in discussing a prior art pixel circuit and its corresponding timing chart (EX1006, [0015], [0017], Figs. 19 & 20), provides that because "the potential VA at the connection point A at time to in FIG. 20 varies depending on a data potential written to the pixel circuit 920 ***last time***[,] [t]he potential at the connection point A is, for example, furthest from (VDD+Vth) when the organic EL element 927 emits light at the maximum luminance before time t0 and closest to (VDD+Vth) when the organic EL element 927 does not emit light before time t0." EX1006, [0028] (emphasis added). In other words, a POSITA would have understood that the image retention phenomena (ghosting) in the prior art is caused by the difference in the state of a current frame is caused by the difference in the previous data potential. EX1002, ¶129. To solve this problem, Senda discloses adding T114, T214, T314, T414, T514 which reset the gate voltage of the driver transistor to eliminate the image residue. EX1006, [0144] ("The reference potential Vstd of the reference supply wiring line Vs is determined such that the

driving TFT 110 goes into a conduction state when the reference potential Vstd is applied to the gate terminal."), [0169] ("The reference potential Vstd of the reference supply wiring line Vs is, as with the first embodiment, determined such that the driving TFT 310 goes into a conduction state when the reference potential Vstd is applied to the gate terminal.").

Like the '757 patent, Senda discloses a substantively identical reset operation wherein the gate voltage of a driving transistor is reset to a known voltage. EX1006, Figs. 6-7, [0163]-[0164], [0169]-[0170], Fig. 15, [0210]-[0214], [0218]-[0219]; *see also infra* Section VI.B.11 (limitation 1.j). Further, in IPR2025-00239, Patent Owner argued that the circuit structure which solves image retention phenomena is claimed in claim 1 of the '757 patent. EX1015, at 3-5. It therefore follows that because Senda discloses each limitation of claim 1 (and claim 17), as explained below, Senda must likewise solve the image retention phenomena. EX1002, ¶130. Accordingly, a POSITA would have understood that Senda discloses, or at least teaches, reducing image retention between frames. *Id.*

Regarding threshold voltage compensation for consistent brightness, Senda expressly provides that a benefit of its disclosed invention is that it "properly compensates for variations in the threshold voltage of a drive element and prevents unwanted light emission from an electro-optical element." EX1006, [0029]; *id.*, Abstract, [0077]-[0078], [0154], [0162], [0220]-[0221]. Accordingly, a POSITA would have understood that Senda discloses threshold voltage compensation for consistent brightness. EX1002, ¶131.

B. Senda's Modified Third Embodiment

Senda anticipates the claims because Senda expressly discloses, as explained below, a modified third embodiment that practices the claims, thereby disclosing to a POSITA within its four corners all elements of the claims as arranged in the claims.

1. The Modified Third Embodiment Circuit

Senda discloses its third embodiment (Fig. 6) should be modified as explained with respect to the seventh embodiment (Fig. 15) by connecting the PMOS transistor 314 shown in Figure 6 to Node C as illustrated by transistor 714 in Figure 15. EX1006, [0218]-[0219]. Senda discloses the modification initially with reference to the fifth embodiment (Fig. 11) by explaining that the first reset transistor connected to Node A (as showing in Fig. 11) should instead be connected to Node C (as shown in Fig. 15). *Id.* Senda explains this modification reduces leakage at Node A and thereby enhances display quality. *Id.* Senda then discloses this modification should also be made for embodiments 1-4 and 6. *Id.* Senda discloses no other modification should be made to the third embodiment, other than to move the connection of the relevant transistor (PMOS transistor 314 in the case of the third embodiment) from Node A to Node C. *Id.* Senda claims the modified third embodiment in dependent claim 5. *Id.*, claim 1 (claiming fourth switching element in either position), claim 3 (claiming position of third embodiment), claim 5 (claiming position of modified third embodiment). Thus, Senda's "Modified 3rd Embodiment" can also be referred to as Senda's "claim 5 embodiment." EX1002, ¶132.

Figures 6 and 15 of Senda are shown below with annotations highlighting transistors 314 and 714. EX1002, ¶133.

Fig. 6

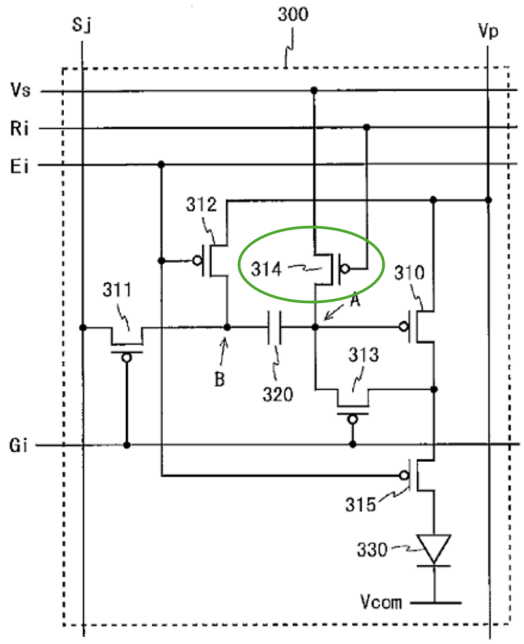
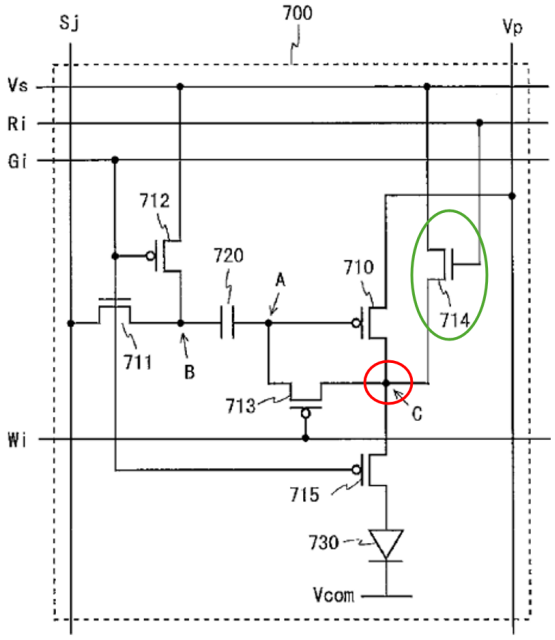
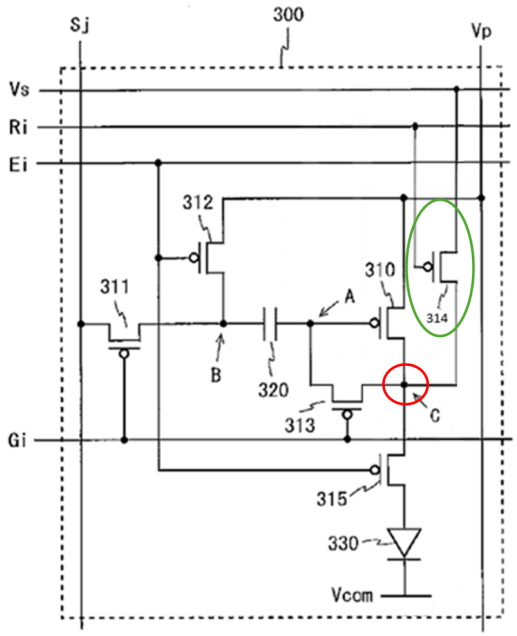


Fig. 15



A modified Figure 6 is shown below, which illustrates Senda's Modified 3rd Embodiment with PMOS transistor 314 connected to Node C, with no other changes to the third embodiment, as disclosed and claimed by Senda. EX1006, [0218]-[0219]; EX1002, ¶134.

Senda's Modified 3rd Embodiment



This modification of Figure 6 illustrating Senda's Modified 3rd Embodiment will be used in the analysis of the claims below. Evidentiary citations will still be made to the original Figure 6 transistor 314, as well as Senda's disclosure to connect that transistor to Node C. EX1002, ¶135.

Based on Senda's disclosure that the only modification that should be made to the third embodiment is to connect the transistor to Node C, a POSITA would have understood the Modified 3rd Embodiment to still use the timing chart of Figure 7. EX1002, ¶136.

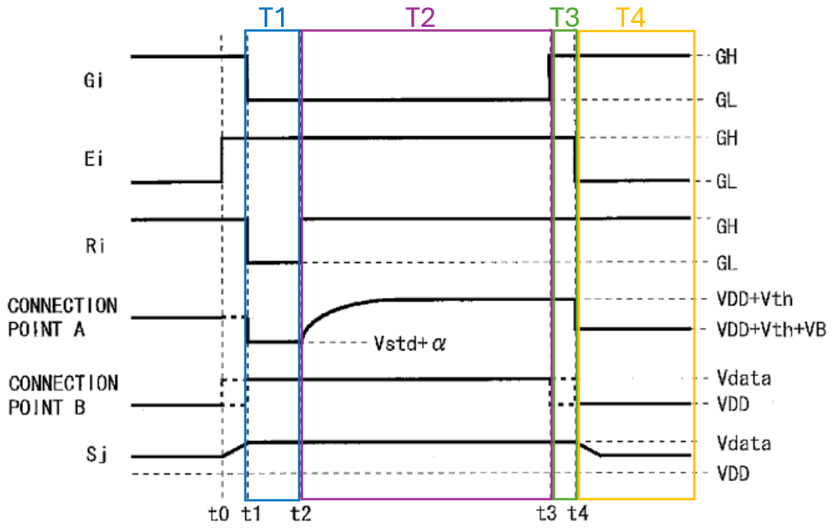
2. Senda's Figure 7 Timing Diagram Applies to the Modified Third Embodiment Circuit

A POSITA would have understood Figure 7 still provides the correct timing diagram for the Modified 3rd Embodiment. In the modified 3rd Embodiment, from t0 to t1, "current does not flow through the organic EL element 130 and thus the organic EL element 130 does not emit light. EX1006, [0141] (discussing pixel circuit 100), [167] (same re the third embodiment, Fig. 6), [0212] (modified seventh embodiment, Fig. 15, "operates in the same manner as" pixel circuit 100 from time t0 to t1). Then, from t1 to t2 (T1), reset transistor 314 connected to Node C still performs its function of resetting the voltage at Node A to "a little higher" than Vstd to ensure the driving transistor 310 is in a conductive state, prior to the voltage compensation period in T2. EX1006, [0169]-[0175], [0209]-[0217]. Because Ri turns off 314 in every period except T1, the operation of the circuit is not impacted in any other time period, other than to achieve a reduction of leakage current at Node A as disclosed by Senda. EX1002, ¶137. Indeed, in the Modified 3rd Embodiment, from t2 to t3 (T2), the control line Ri is changed such that the current flowing through 314 is interrupted, which causes the potential at the connection point A to rise to (VDD+Vth) and the driving transistor 314 goes into a threshold state. EX1006, [0171], [0215]; EX1002, ¶¶138-139. From t3 to t4 (T3), the switching transistor 313 changes to a non-conductive state, causing the potential difference between the connection points A and B to be held in the capacitor 320. *See*

EX1006, [0148], [0216] (stating that after t3, pixel circuit 700 operates in the same manner as the pixel circuit 100 does after time t4 (*see* [0189])); EX1002, ¶140. Lastly, after t4 (T4), regardless of the value of the threshold voltage Vth of the driving transistor, current of an amount according to the data potential Vdata flows through the organic EL element 330. EX1006, [0174], [0216]; EX1002, ¶141.

An annotated Figure 7 is shown below adding annotations for time period T1 (time after t1), T2 (time after t2), T3 (time after t3) and T4 (time after t4). This annotated timing diagram will be used in the analysis below. EX1002, ¶¶136-141 (explaining the application of the timing in annotated Figure 7 to the Modified 3rd Embodiment).

Fig. 7

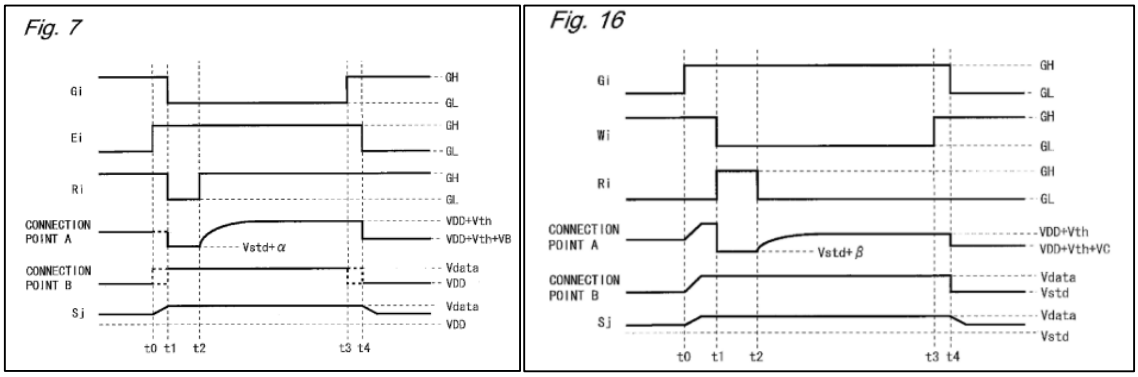


3. Patent Owner's Incorrect Timing Diagram Argument

In IPR2025-00239, Patent Owner incorrectly argued the timing diagram in Senda's Figure 7 does not apply to the modified third embodiment. EX1015, 10-12. There is no merit to Patent Owner's unsubstantiated argument because the timing diagram in Figure 7 is clearly applicable as explained above.

Patent Owner could not explain why the timing diagram in Figure 7 was not applicable to the modified third embodiment. Instead, Patent Owner argued that because modifying the fifth embodiment required modifying its timing diagram, modifying the third embodiment must require some (unidentified) modification of its timing diagram. EX1015, at 10-11. Not so. The fifth embodiment (Fig. 11) used two reset circuits which were turned on separately, one after the other, with an intervening time period to reset the control node A, requiring time periods t0-t5 as shown in the timing diagram in Figure 12. EX1006, Fig. 12 (timing diagram for fifth embodiment, Fig. 11). In the modified fifth embodiment (Fig. 15), the two reset circuits must be turned on together to reset the control node A with the reference voltage Vs because the two reset circuits are connected in series to apply the reference voltage Vs through node C to node A. This required a change to the timing diagram such that the reset circuits are first turned on together and then one is turned off, eliminating one time period such that there are only time periods t0-t4 as shown in the timing diagram for the modified fifth embodiment (Fig. 16). EX1006, Fig. 12, Fig. 16.

A similar change is <u>not</u> necessary when modifying the third embodiment, because, as provided above, the third embodiment already used the arrangement with time periods t0-t4. *See id.*, Fig. 7 and Fig. 16 (each having only time periods t0-t4).



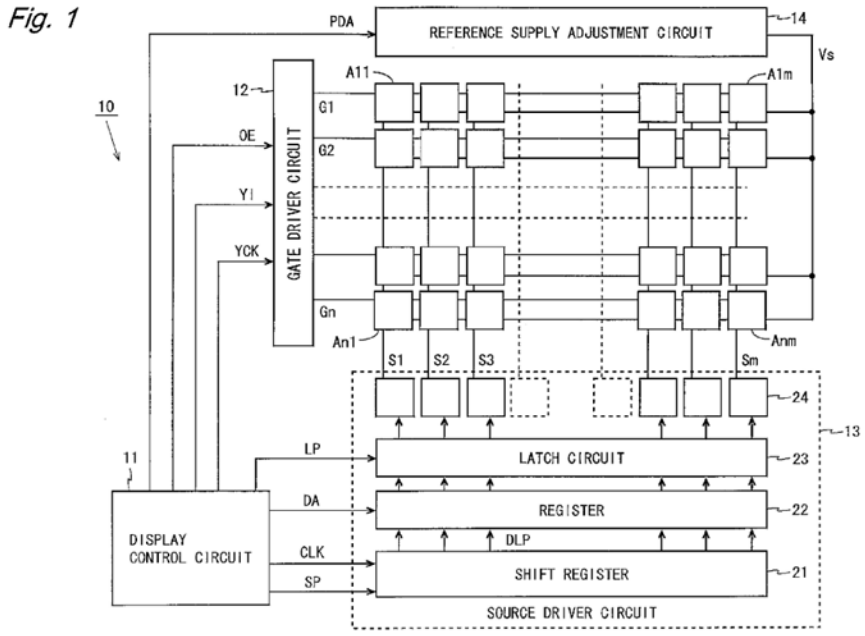
As shown in Fig. 7 (original third embodiment), both reset circuits are turned on together in the time period t1-t2 and only one is on from t2-t3. This is the same timing relationship that is required

in the modified third embodiment to first reset the control node A with the reference voltage Vs (t1-t2), and then to perform the voltage compensation operation (t2-t3). Thus, a POSITA would have understood that the corresponding timing diagram for the modified third embodiment would, like Figure 7, include time periods t0-t4. And, for the reasons set forth above, the timing diagram in Figure 7 would apply to the modified third embodiment. EX1002, ¶142.

C. Claim 1

1. [1pre]

Senda discloses "An organic light emitting display, comprising (see following limitations)." EX1002, ¶143.



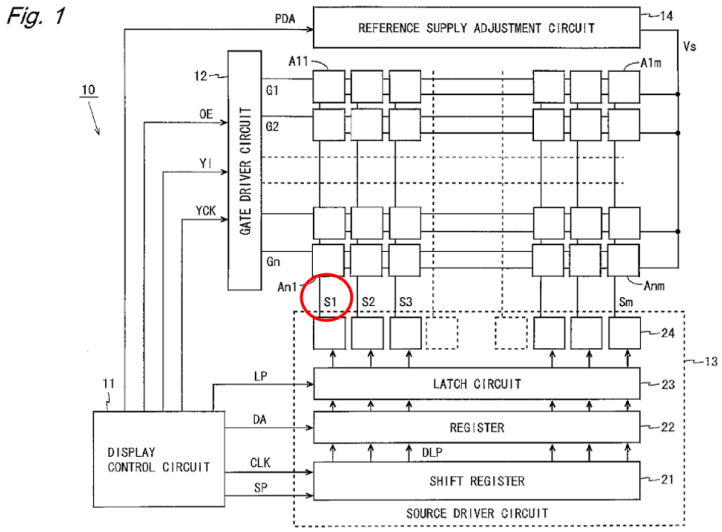
EX1006, Figs. 1-16, Abstract, [0001] (invention relates to a display device such as an organic EL display, [0117] ("130 … 330, and 730: organic EL element"), [0125] ("[a] display device

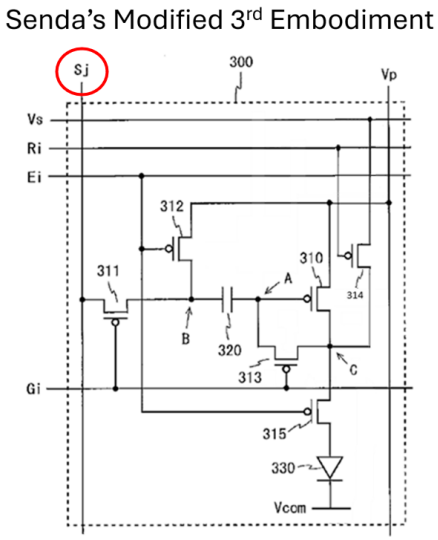
according to each embodiment includes a pixel circuit … the pixel circuit includes an organic EL element"), [0135]-[0137], [0163], [0209]; EX1002, ¶144.

As discussed above, Senda discloses a Modified 3rd Embodiment, wherein Senda's third embodiment (Figs. 6-7, [0163]-[0174]) is modified as disclosed for the seventh embodiment (Fig. 15, [0209]-[0220]) to connect PMOS transistor 314 to Node C to reduce leakage at Node A. EX1006, [0218]-[0219], claims 1, 3, and 5. Senda discloses figure 1 and [0125]-[0134] apply to each of the first, third, and seventh embodiments. *Id.*, [0125]-[0127]. Thus, Senda discloses all elements of the challenged claims, as arranged in the claims, as further explained for each limitation below. EX1002, ¶145.

2. [1a]

Senda discloses "a data line (Sj) for transmitting a data signal (Vdata)." EX1002, ¶146.

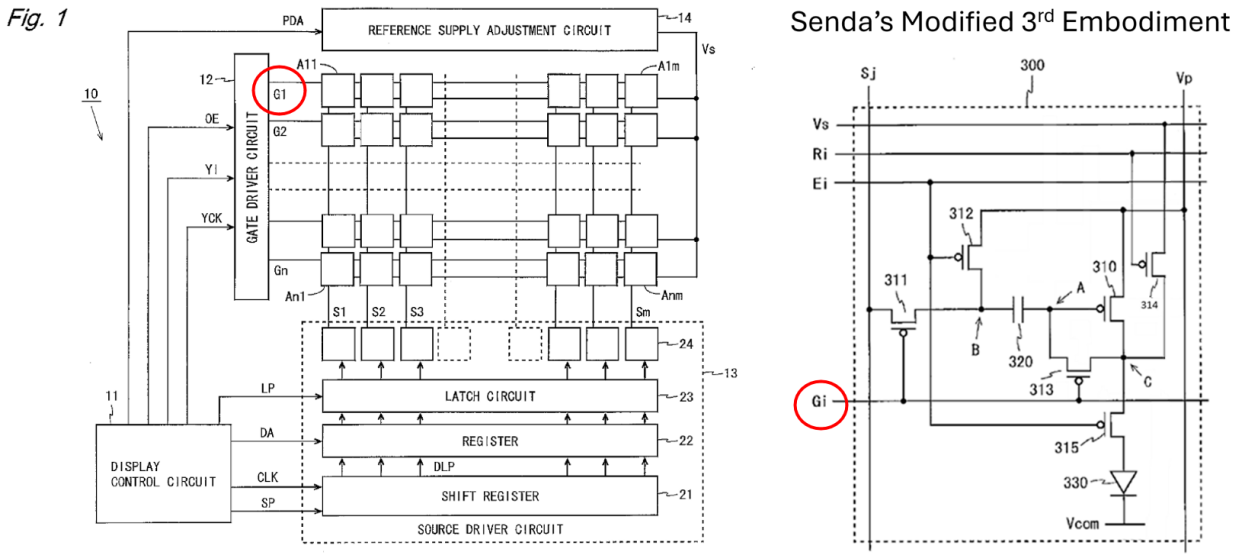




EX1006, Figs. 1 (annotated) (left), 6 (annotated and modified) (right) (data lines Sj are connected to the source driver circuit 13), 7 (data on Sj), [0128]-[0131] (circuit 13 functions as a display signal output circuit that provides potentials according to display data to the data lines Sj), [0124], [0163]-[0164], [0166] (data on Sj), [0169]-[0171] (Vdata on Sj); EX1002, ¶147.

3. [1b]

Senda discloses "a first scan line (Gi) for transmitting a first scan signal." EX1002, ¶148.

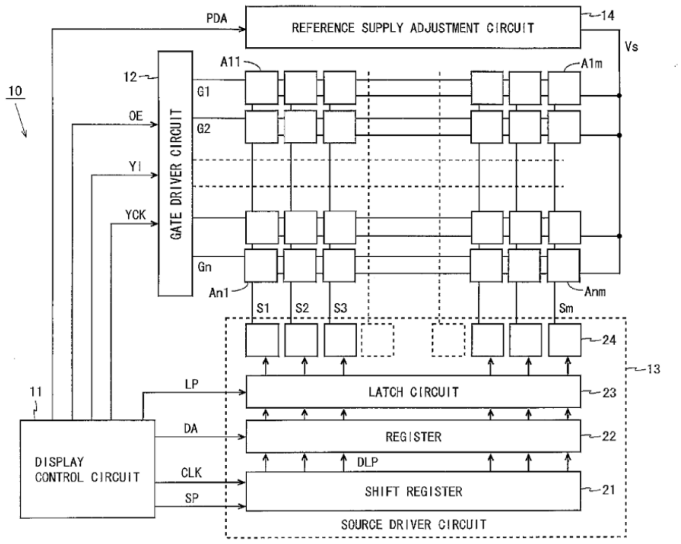


EX1006, Fig. 1 (annotated) (left) (a plurality of scanning lines Gi), 6 (annotated and modified) (right) (Gi), 7 (GL and GH on Gi), 15 (scanning line Gi), [0123] (Gi: scanning line), [0127]-[0128] (scanning lines Gi … are connected to the gate driver circuit 12), [0130] (gate driver circuit 12 functions as a scanning signal output circuit that selects a write-target pixel circuit using a corresponding scanning line Gi), [0136]-[0142], [0163]-[0172] (GL and GH on Gi), [0211]-[0212]; EX1002, ¶149.

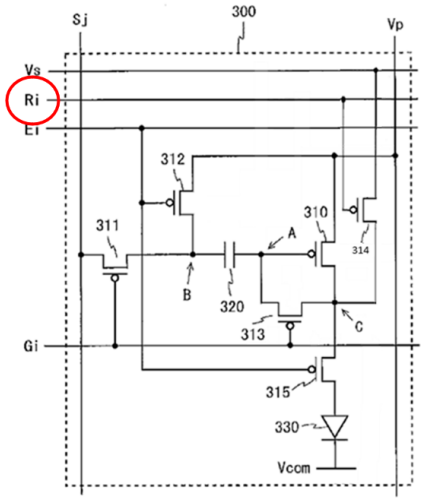
4. [1c]

Senda discloses "a second scan line (Ri) for transmitting a second scan signal." EX1002, ¶150.

Fig. 1



Senda's Modified 3rd Embodiment

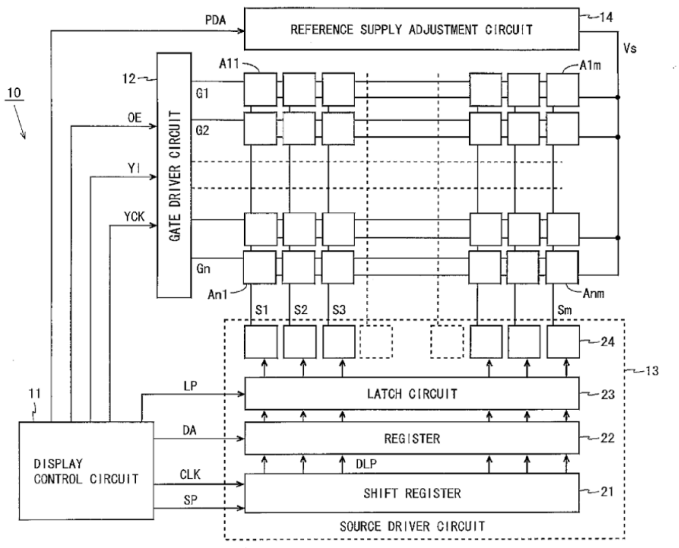


EX1006, Fig. 1, Fig. 6 (annotated and modified) (right) (Ri), 7 (GL and GH on Ri), 15 (Ri), [0122] (Wi, Ri, and Ei: control line), [0128] (scanning lines Gi and control lines Wi, Ri, etc. are connected to the gate driver circuit 12), [0130] (output from the logic operation corresponding control lines Wi, Ri, etc.), [0136], [0138]-[0140], [0143]-[0148], [0164]-[0174] (GL and GH on Ri control line), [0211]-[0218]; EX1002, ¶151.

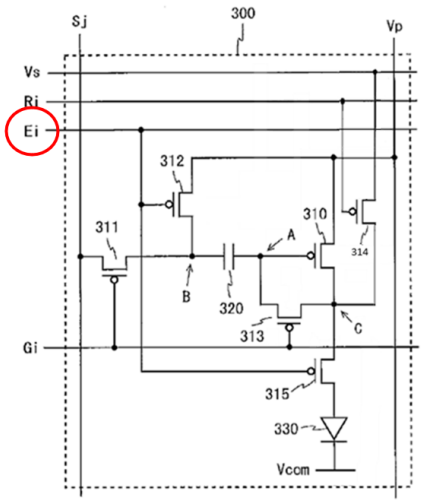
5. [1d]

Senda discloses "a transmission line (Ei) for transmitting an emission signal." EX1002, ¶152.

Fig. 1



Senda's Modified 3rd Embodiment



EX1006, Figs. 1, 6 (annotated and modified) (right) (control line Ei), 7 (GL and GH on Ei), [0122] (Wi, Ri, and Ei: control line), [0164] ("[t]he potential of the control line Ei is controlled by the gate driver circuit 12"), [0165]-[0174] (GL and GH on Ei), [0211]-[0218]; EX1002, ¶153.

6. [1e]

Senda discloses "an input unit (311), electrically connected to the data line (Sj) and the first scan line (Gi), for outputting a preliminary control voltage (outputting preliminary control voltage to Node B) according to the data signal (data signal on Sj) and the first scan signal (first scan signal on Gi)." EX1002, ¶183.

Senda's Modified 3rd Embodiment

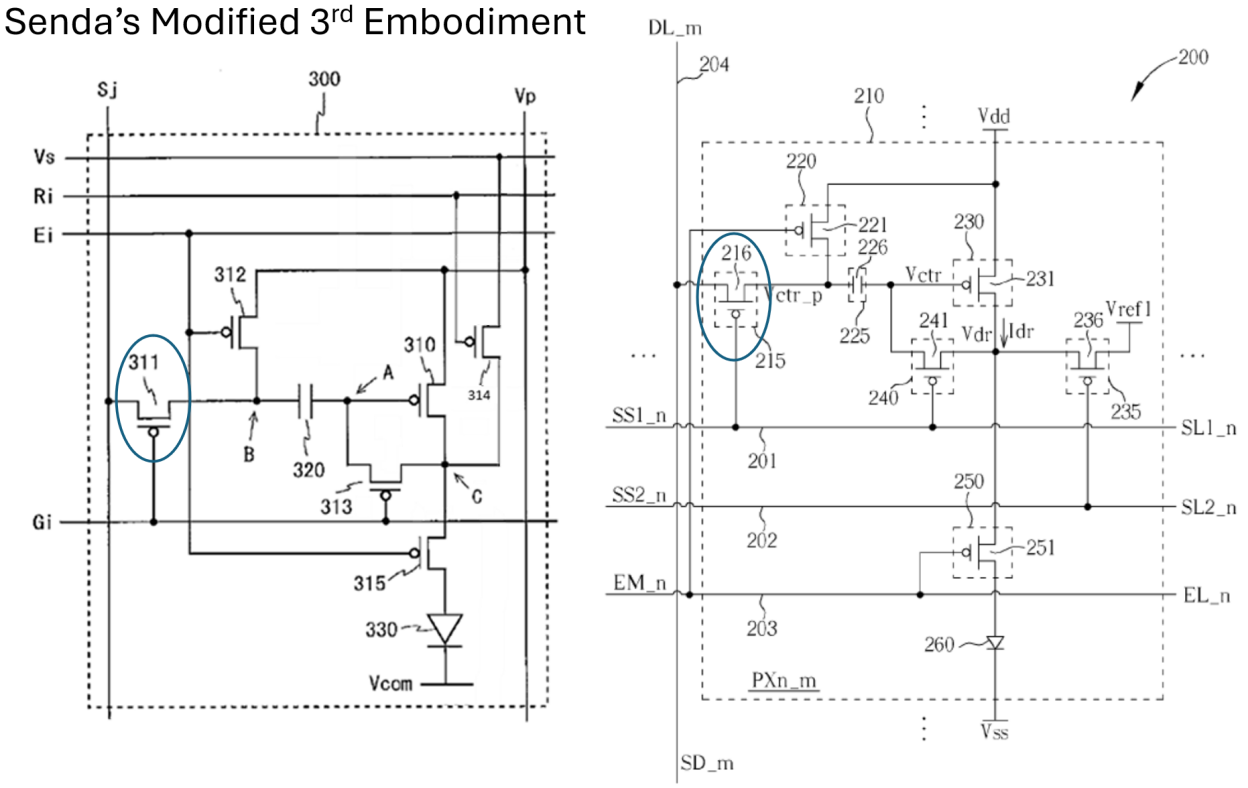


FIG. 2

Senda's Modified 3rd Embodiment (left) and '757 patent Figure 2 (right) are shown annotated above. Senda discloses 311 is a PMOS transistor with a gate coupled to Gi, a first electrode coupled to the data line Sj, and a second electrode coupled to Node B, such that during T1 and T2, 311 outputs a preliminary control voltage to the first Node B according to the data signal on Sj and the low level first scan signal on Gi. EX1006, Figs. 6-7 (showing Vdata on Sj and as output to Node B), [0135]-[0152], [0163]-[0164] (PMOS transistors, Gi, Sj), [0165]-[0175] (311 is turned on by GL on Gi such that it outputs Vdata to Node B from the data signal on Sj), [0169] ("B is connected to the data line Sj through the switching TFT 311, and thus, the potential at the connection point B is changed to Vdata"). The second electrode of TFT 311 is electrically connected to the voltage adjustment unit (312) and couple unit (320) at Node B. *Id.* PMOS transistor 311 outputs Vdata to Node B after t1 and after t2 while GL is on Gi as shown in Figure 7. EX1002, ¶155.

Under 112f, Senda's PMOS transistor 311 as connected performs the claimed function and is identical to the corresponding structure for the input unit 215 (PMOS transistor 216 as connected). EX1001, Fig. 2, Fig. 4, 3:54-57, 4:17-18, 4:34-38, 5:13-15; EX1002, ¶156.

7. [1f]

Senda discloses "a voltage adjustment unit (312), electrically connected to the transmission line (Ei) and the input unit (311), for adjusting the preliminary control voltage (adjusting Vdata preliminarily stored at Node B) according to the emission signal (Ei) and a second reference voltage (VDD on Vp)." EX1002, ¶157.

Senda's Modified 3rd Embodiment

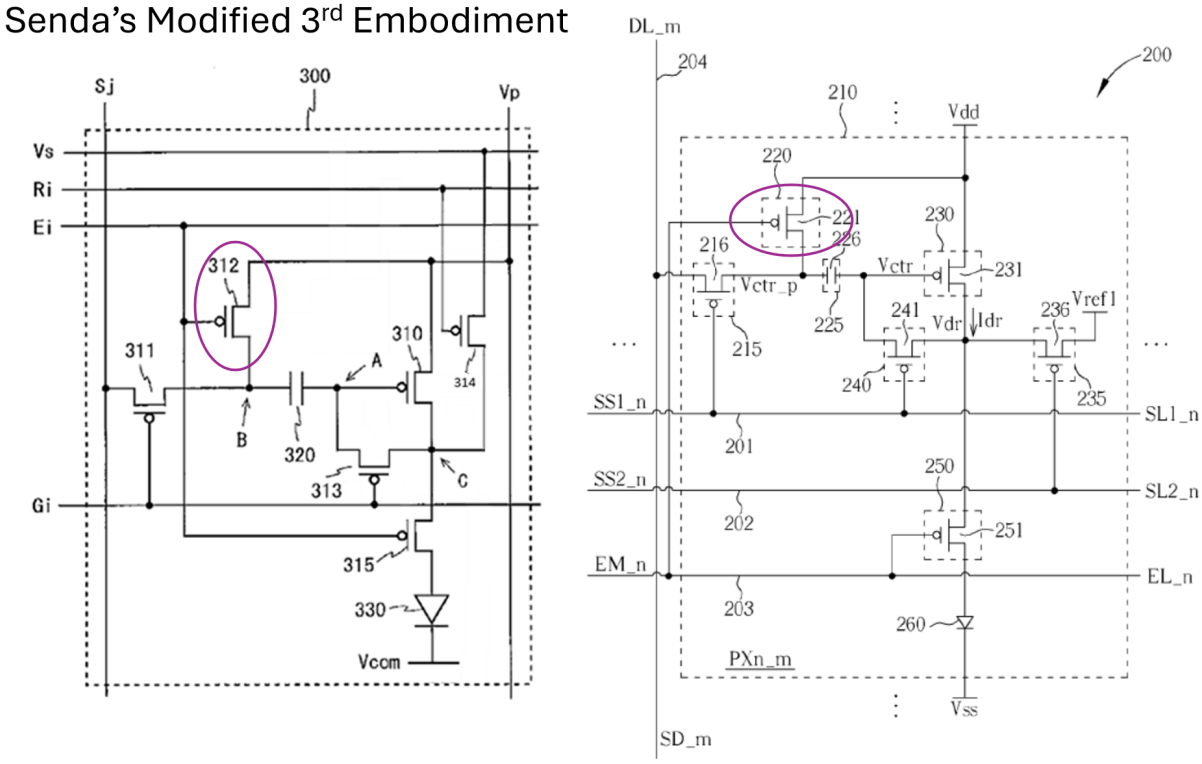


FIG. 2

Senda's Modified 3rd Embodiment (left) and '757 patent Figure 2 (right) are shown annotated above. Senda discloses 312 is a PMOS transistor with a gate coupled to Ei, a first electrode connected to 311 and 320 at Node B and a second electrode coupled to power supply wiring line Vp. EX1006, Figs. 6-7, [0163]-[0164] (connections for TFT 312). When 312 is turned on by a low

emission control signal on Ei, 312 adjusts the preliminary control voltage Vdata at Node B to VDD. EX1006, Figs. 6-7 (after t4, showing adjustment of voltage at Node B from Vdata to Vdd), [0165]-[0174] (in T4, TFT 312 is switched on by low voltage on Ei, connecting Node B to power supply wiring line Vp to change voltage from Vdata to VDD). TFT 312 is on during the light emitting period, after t4 in Figure 7. EX1002, ¶158.

Under 112f, Senda's PMOS transistor 312 as connected performs the claimed function and is identical to the corresponding structure for the voltage adjustment unit 220 disclosed in the '757 patent (PMOS transistor 221 as connected). EX1001, Fig. 2, Fig. 4, 3:57-61, 4:45-58, 6:24-42; EX1002, ¶159. Note that the relevant corresponding structure in the '757 patent for this ground is the structure corresponding to Figure 2 (and dependent claim 13) (discussed at 3:57-61 and 4:45-58) where the voltage adjustment unit is connected to power supply voltage VDD as the second reference voltage. *See* Section I.C.1.b (Claim Construction [1f]) above; EX1002, ¶160.

8. [1g]

Senda discloses "a couple unit (320), electrically connected to the input unit (311) and the voltage adjustment unit (312), for adjusting a control voltage (voltage at Node A) through coupling a change of the preliminary control voltage (capacitor 320 couples change in voltage at Node B to Node A)." EX1002, ¶161.

Senda's Modified 3rd Embodiment

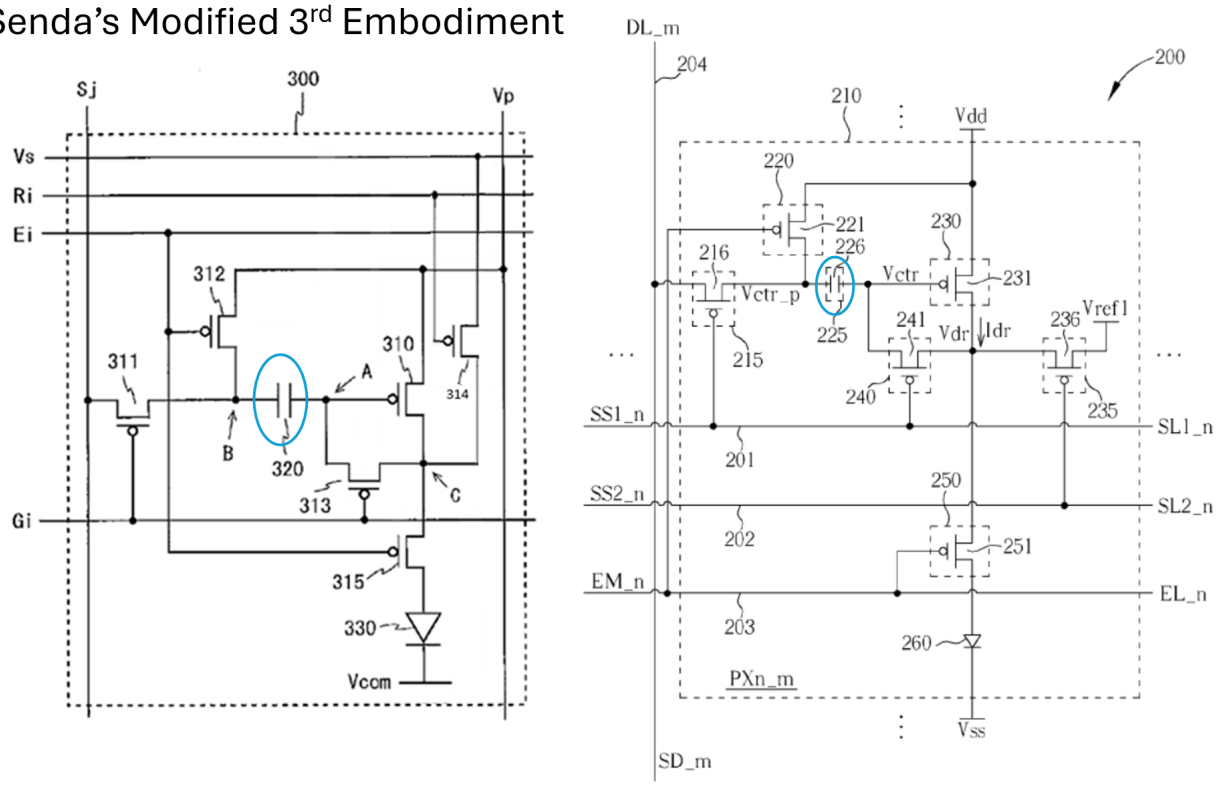


FIG. 2

Senda's Modified 3rd Embodiment (left) and '757 patent Figure 2 (right) are shown annotated above. Senda discloses storage capacitor 320 is coupled between Nodes A and B and, at time t3, is charged to the voltage difference between the preliminary control voltage Vdata on Node B and the voltage VDD+Vth on Node A. EX1006, Figs. 6-7, [0137], [0163]-[0164], [0169]-[0171] (charging of Nodes A and B), [0172] (at time t3 capacitor 320 holds the potential difference VDD+Vth-Vdata). After t4, when the preliminary control voltage on Node B is changed by 312 to VDD (potential of power supply line Vp), capacitor 320 couples that change in voltage to Node A. EX1006, Fig. 6-7 (showing after t4 the change in voltage at Node B and the corresponding change in voltage at Node A), [0163]-[0164] (PMOS), [0173] ("the potential at the connection point B is changed from Vdata to VDD and accordingly the potential at the connection point A is changed by the same amount … and becomes (VDD+Vth+VB)."). The coupling of the change in voltage occurs after t4, during the light emission period in Figure 7. EX1002, ¶162.

Under 112f, Senda's capacitor 320 as connected performs the claimed function and is identical to the corresponding structure for the couple unit 225 in the '757 patent (capacitor 226 as connected). EX1001, Fig. 2, Fig. 4, 3:62-65, 4:18-19, 4:42-44, 6:33-36, 6:47-50; EX1002, ¶163.

9. [1h]

Senda discloses "a driving unit (310), electrically connected to the couple unit (320), for providing a driving current and a driving voltage (current and voltage at second electrode of 310, Node C), according to the control voltage (voltage at Node A) and a first power voltage (VDD on Vp)." EX1002, ¶164.

Senda's Modified 3rd Embodiment

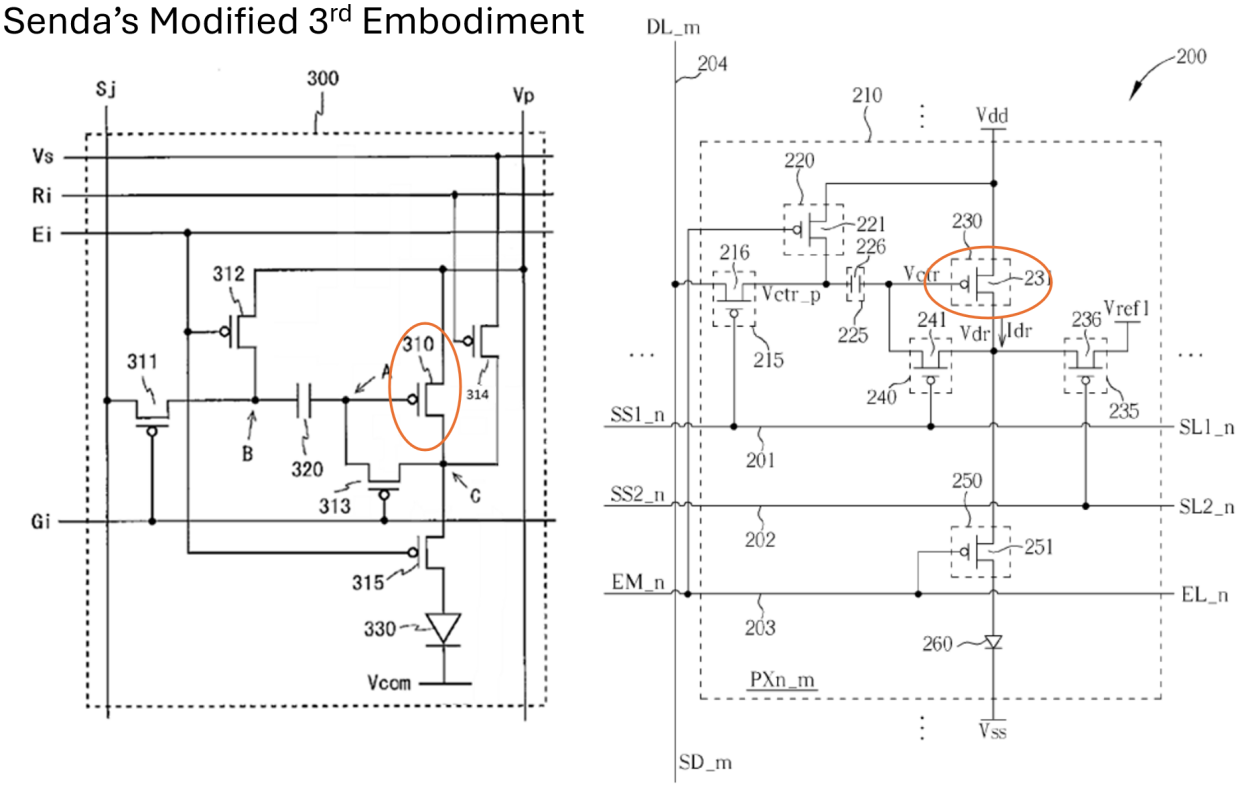


FIG. 2

Senda's Modified 3rd Embodiment (left) and '757 patent Figure 2 (right) are shown annotated above. Senda discloses 310 is a PMOS transistor with its gate terminal coupled to Node A (one electrode of capacitor 320), first electrode coupled to Vp providing VDD, and a second electrode coupled to Node C (313, 314, 315). After t4, when 310 is turned on by the control voltage at Node

A and a low signal on Ei turns on 315, transistor 310 provides a driving current and driving voltage at its second electrode (Node C) to drive the organic EL element ("OLED") 330. EX1006, Figs. 6-7, [0163]-[0164] (PMOS), [0169]-[0174] (describing 310 driving after t4). Transistor 310 provides the driving current and driving voltage during the light emission period T4 in Figure 7. EX1002, ¶165.

Under 112f, Seanda's PMOS transistor 310 as connected performs the claimed function and is identical to the corresponding structure for the driving unit 230 disclosed in the '757 patent (PMOS transistor 231 as connected). EX1001, Fig. 2, Fig. 4, 3:65-4:2, 4:19-20, 4:38-41; EX1002, ¶166. Senda explicitly discloses that 310 provides a current at its second electrode, Node C, to drive OLED 330. EX1006, Fig. 6-7, [0173]-[0174], [0210] (Node C). And Senda discloses that driving current provided by 310 is provided according to Vdd and the control voltage at Node A applied to the gate of 310. *Id.*; EX1002, ¶167. Senda inherently discloses that 310 provides a "driving voltage." A POSITA would have known it was inherent from the electrical properties of Senda's pixel circuit 300 that TFT 310 is also providing a driving voltage with the driving current. To provide a driving current as disclosed in Senda, a POSITA would have known that there must be a driving voltage, i.e., a difference in potential between the second electrode of 310 at Node C and Vcom at the common cathode. EX1006, [0120], [0133]. A POSITA would have known that without that difference in potential, there would be no driving current as disclosed in Senda and the OLED 330 would not emit light. A POSITA would have known that the magnitude of the driving voltage provided by 310 at Node C would be Vdd minus the voltage drop across 310. EX1006, [0171]; EX1002, ¶168 (explaining diodes).

10. [1i]

Senda discloses "a first reset unit (314), electrically connected to the driving unit (310) at Node C and the second scan line (Ri), for resetting the driving voltage (voltage at Node C) according to the second scan signal (Ri) and a first reference voltage (Vstd on Vs)." EX1002, ¶169.

Senda's Modified 3rd Embodiment

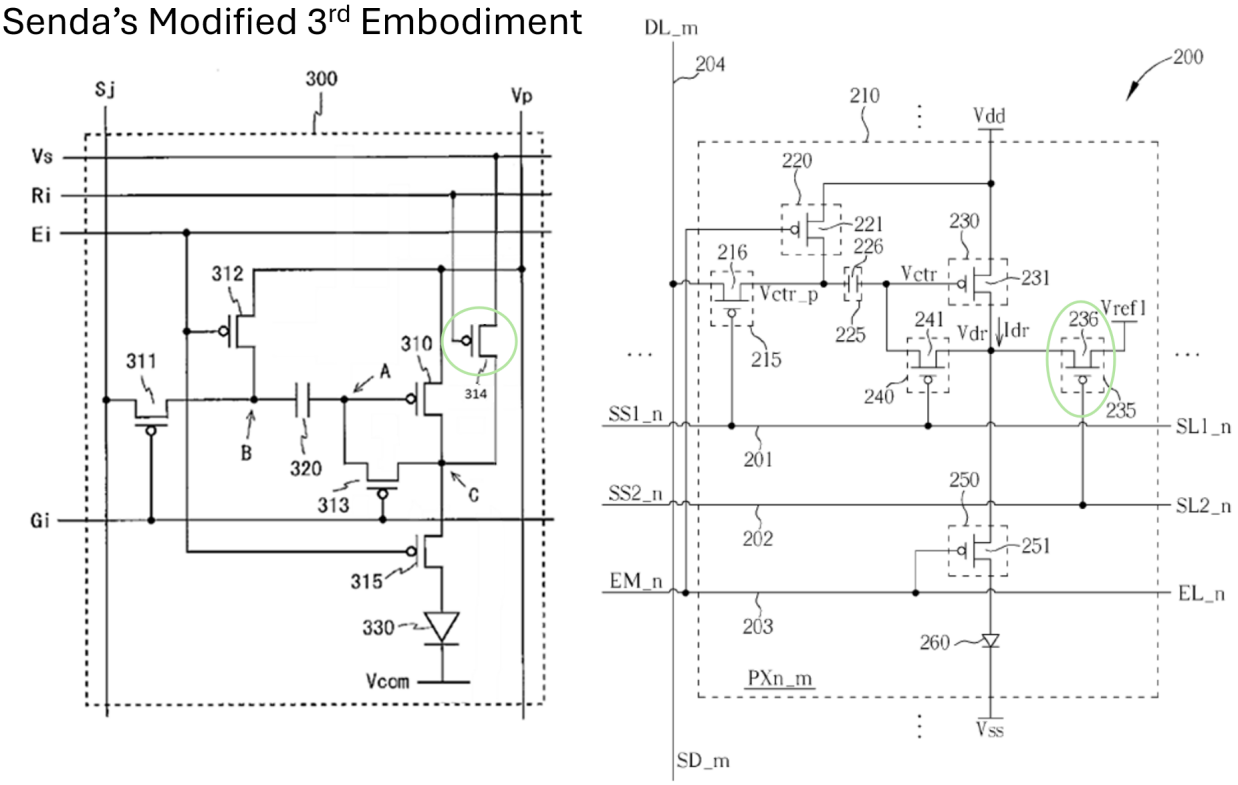


FIG. 2

Senda's Modified 3rd Embodiment (left) and '757 patent Figure 2 (right) are shown annotated above. Senda discloses transistor 314 is a PMOS transistor with a gate coupled to Ri, a first electrode coupled to transistor 310 at Node C, and a second electrode coupled to Vs, such that after t1 when 314 is turned on by the low second scan signal on Ri, the potential at Node C is reset according to Vstd. EX1006, Figs. 6-7, [0163]-[0164] (PMOS), [0169]-[0170] (disclosing how during T1, TFT 314 is conductive), Fig. 15, [0210]-[0214], [0218]-[0219] (disclosing PMOS transistor 314 should be connected to Node C), claims 1 and 5 (claiming the modified third embodiment). As explained above, the Modified 3rd Embodiment discloses 314 will reset Node C

according to the timing diagram in Figure 7 such as that when Ri is low, the driving voltage at Node C is rest according to Vstd. *See* Section X.B; EX1002, ¶170.

Under 112f, Senda's PMOS transistor 314 as connected performs the claimed function and is identical to the corresponding structure for the first reset unit 235 disclosed in the '757 patent (PMOS transistor 236 as connected). EX1001, Fig. 2, Fig. 4, 4:2-5, 4:20-31, 4:44-48; EX1002, ¶171.

Senda discloses transistor 314 is connected to Vstd on Vs while the corresponding structure 236 is connected to "Vref1," but this difference in naming convention is not relevant. *See supra* Sections I.C.2 and IV.B.8 (discussing proper interpretation of "reference voltage" and noting that there is no definition or disclaimer in the specification or file history that would require limiting "reference voltage" to only voltages expressly labelled as "reference."). Notwithstanding, Vstd on Vs in Senda is a reference voltage, because it is a known value used to reset the circuit into a known state, that is different from the second reference voltage VDD. EX1006, [0133] (Vstd is a "reference potential" that is adjustable and set by control signal PDA), [0155] (Vstd must be lower than VDD and is desirably close to VDD+Vth to ensure compensation for 310); EX1002, ¶172.

11. [1j]

Senda discloses "a second reset unit (313), electrically connected to the driving unit (310), the first reset unit (314), and the first scan line (Gi), for resetting the control voltage (voltage at Node A) according to the first scan signal (Gi) and the driving voltage (voltage at Node C)." EX1002, ¶173.

Senda's Modified 3rd Embodiment

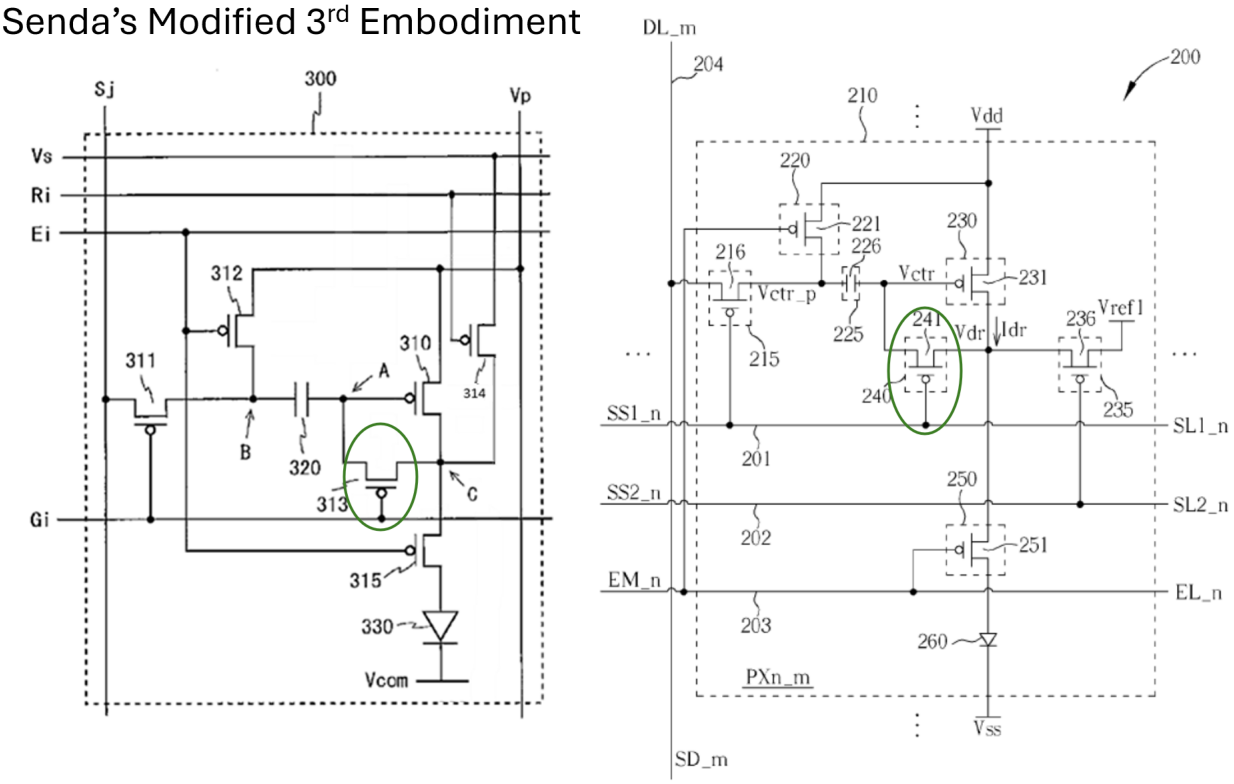


FIG. 2

Senda's Modified 3rd Embodiment (left) and '757 patent Figure 2 (right) are shown annotated above. Senda discloses 313 is a PMOS transistor with a gate coupled to Gi, a first electrode coupled to Node C (second electrode of 310, 314, and 315), and a second electrode coupled to Node A (the gate of 310 and an electrode of 320), such that when 313 is turned on by a low signal on Gi, the driving voltage (voltage at Node C) is applied to reset the control voltage at Node A. EX1006, Figs. 6-7, [0163]-[0164], [0169]-[0172], [0211]-[0214]; EX1002, ¶174.

After t1 (during T1), the voltage at Node A is reset (to a little higher than Vstd) according to the low signal on Gi and the driving voltage at Node C. Specifically, low signals on Gi and Ri turn 313 and 314 on, such that the voltage on Node A is reset to Vstd plus alpha. EX1006, Figs. 6-7 (showing after t1, Node A at Vstd plus alpha), [0163]-[0164] (PMOS), [0169]-[0172], [0211]-[0214] (resetting voltage at Node A through 713 and 714); EX1002, ¶¶199 (explaining a little higher than Vstd), 175, 137.

After t2 (during T2), the voltage at Node A is reset (to VDD+Vth) according to the low signal on Gi and the driving voltage at Node C. Specifically, a low signal on Gi is still supplied keeping 313 on, but a high signal on Ri causes 314 to turn off, such that the voltage on Node A is reset to VDD+Vth. EX1006, Figs. 6-7 (showing after t2, Node A reaches VDD+Vth, and that Vth is a negative value), [0163]-[0164], [0169]-[0171]. Senda discloses that after t2, 310 operates in a conduction state until Node A reaches VDD+Vth, at which point 310 goes into a threshold state. *Id.*, [0171]. Senda discloses this reset is performed to compensate for the threshold voltage of 310. *Id.*, [0174]; EX1002, ¶176.

Senda's disclosure in this regard is identical to the disclosure of the '757 patent wherein during T1, Vctrl is reset to Vref1 through 236 and 241, and during T2, Vctrl is reset to VDD-|Vth| through 241. EX1001, Fig. 3, 5:15-22 (T1), 5:23-38 (T2). Senda discloses Vth is a negative value (EX1006, [0171]), so Senda's VDD+Vth is the same as the '757 patent's VDD-|Vth|. EX1002, ¶177.

Under 112f, Senda's PMOS transistor 313 as connected performs the claimed function and is identical to the corresponding structure for the second reset unit 240 disclosed in the '757 patent (PMOS transistor 241 as connected). EX1001, Fig. 3, 4:5-9, 4:21, 4:48-52; EX1002, ¶178.

12. [1k]

Senda discloses "an organic light emitting diode (330) for generating output light according to the driving current." EX1002, ¶179.

Senda's Modified 3rd Embodiment

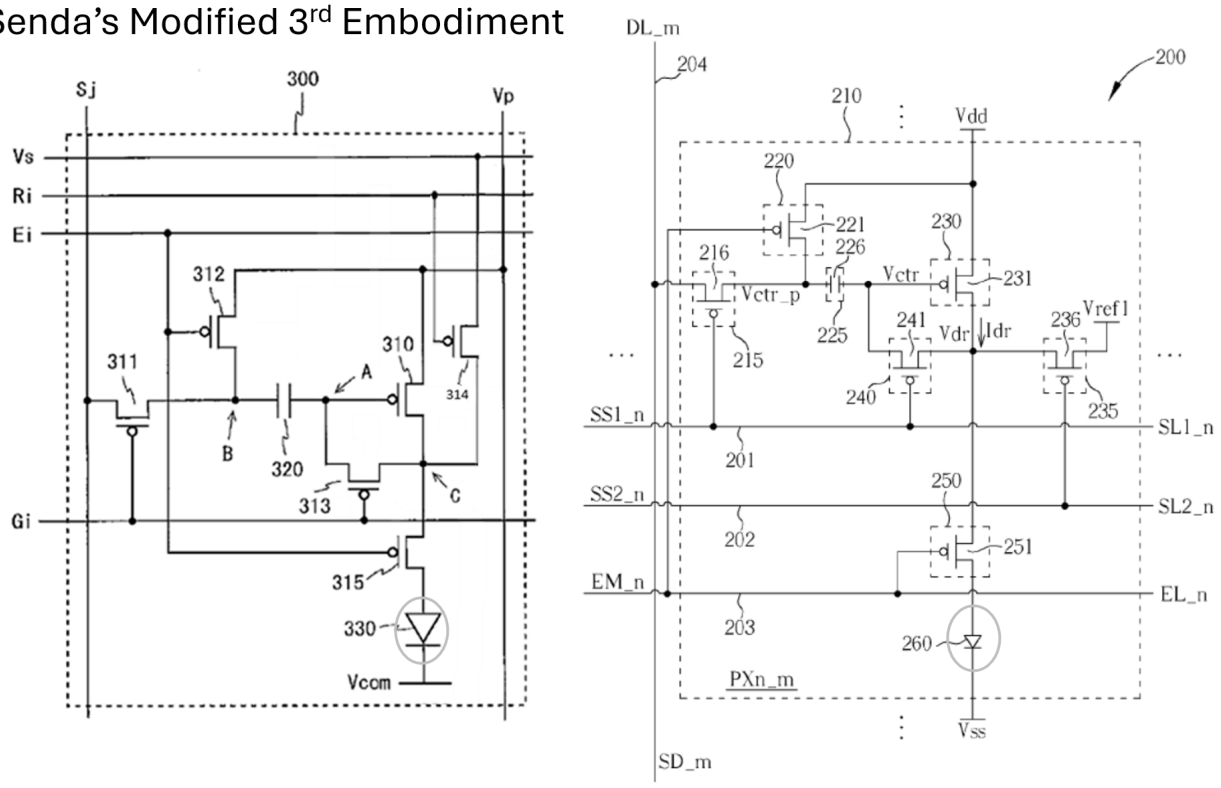


FIG. 2

Senda's Modified 3rd Embodiment (left) and '757 patent Figure 2 (right) are shown annotated above. Senda discloses that the OLED 330 is driven by the driving current provided by 310 to generate output light. EX1006, Fig. 6-7, [0117], [0163]-[0164], [0174] (disclosing the current through 310 drives the OLED to emit light). The amount of control voltage at Node A on the gate of 310 determines the amount of driving current 310 provides and, therefore, the brightness of the OLED. *Id*. EX1002, ¶180.

13. [1l]

Senda discloses "an emission enable unit (315), electrically connected to the transmission line (Ei), the driving unit (310), and the organic light emitting diode (330), for providing a control of furnishing the driving current to the organic light emitting diode according to the emission signal (GL and GH on Ei)." EX1002, ¶181.

Senda's Modified 3rd Embodiment

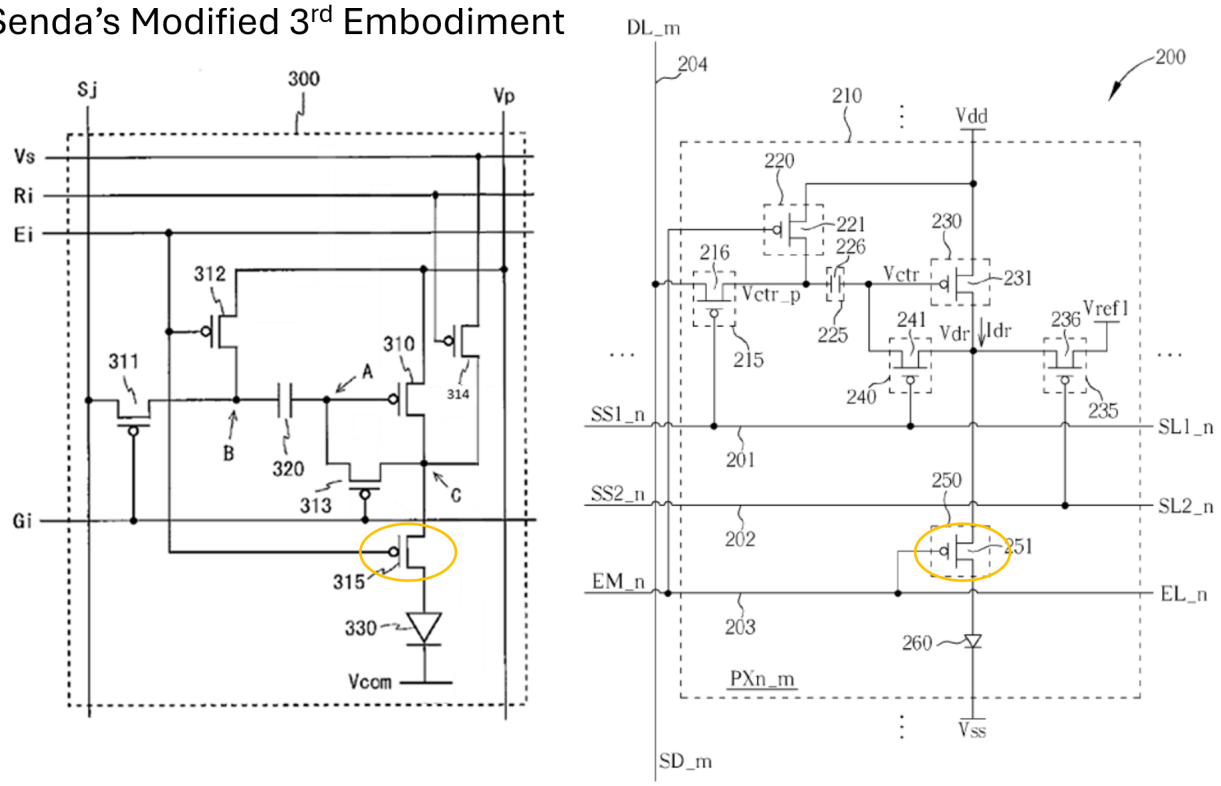


FIG. 2

Senda's Modified 3rd Embodiment (left) and '757 patent Figure 2 (right) are shown annotated above. Senda discloses 315 is a PMOS transistor with a gate coupled to Ei, a first electrode coupled to the second electrode of 310 at Node C and a second electrode coupled to OLED 330, such that when 315 is turned on by a low emission control signal on Ei, the driving current from the second electrode of 310 is applied to OLED 330. EX1006, Fig. 6-7, [0117], [0163]-[0164], [0174]; EX1002, ¶182.

Under 112f, Senda's PMOS transistor 315 as connected performs the claimed function and is identical to the corresponding structure for the second reset unit 250 disclosed in the '757 patent (PMOS transistor 251 as connected). EX1001, Fig. 3, 4:9-14, 4:23-24, 4:54-58; EX1002, ¶183.

D. Claim 11:

Senda discloses claim 1 "wherein the voltage adjustment unit (312) comprises a fifth transistor (312), the fifth transistor having a first end for receiving the second reference voltage (VDD on Vp), a gate end electrically connected to the transmission line (Ei), and a second end electrically connected to the input unit (311) and the couple unit (320)." *See* [f], [1e]-[1g]. EX1002, ¶184.

E. Claim 13:

Senda discloses "the organic light emitting display of claim 11, wherein the second reference voltage (VDD on Vp) is the first power voltage (VDD on Vp)." *See* [1f], [1h], 11; EX1002, ¶185.

F. Claim 16:

Senda discloses claim 1 "wherein the organic light emitting diode (330) comprises an anode electrically connected to the emission enable unit (315) and a cathode for receiving a second power voltage (Vcom)." *See* [1k]; EX1006, Figs. 1, 6 (illustrating diode with anode (base of triangle) connected to 315 and cathode (line at tip of triangle) connected to Vcom), [0120] ("Vcom: COMMON CATHODE"), [0133] ("a common cathode Vcom (or a cathode wiring line CAi)"), [0135]-[0137] (disclosing one end of OLED connected to common cathode Vcom and other end (anode) connected to 315 and eventually to VDD), [0163]-[0164]; EX1002, ¶186 (explaining meaning of diode symbol to POSITA and how disclosure that one electrode is a cathode means the other electrode must be the anode).

G. Secondary Considerations

This Request demonstrates that the Challenged Claims of the '757 patent are unpatentable as obvious in view of the prior art references. Patent Owner did not identify any evidence of secondary considerations during prosecution or to date in the litigation. Further, the clear teachings in the prior art outweigh any supposed "secondary considerations." *Graham* v. *John Deere Co. of Kansas City,* 383 U.S. 1, 36 (1966).

VII. DISCLOSURE OF CONCURRENT LITIGATION, REEXAMINATION, AND RELATED PROCEEDINGS

Based on information available to Requester, the '757 patent is the subject of one currently pending District Court litigation (*Optronic Sciences LLC v. BOE Technology Group Co., Ltd.*, Case No. 2:24-cv-00577-JRG (E.D. Tex. July 23, 2024)) and, as noted above in Section I.3, IPR2025-00239, which was discretionarily denied.

Requester is unaware of any additional prior reexaminations or other post-grant proceedings in which the '757 patent is or has been involved.

VIII. CONCLUSION

The Commissioner is hereby authorized to charge Deposit Account 503266 under Docket No. 433123.000006 the *Ex Parte* Reexamination fee of $13,545 under 37 C.F.R. § 1.20(c). Requester believes no other fee is due with this submission, however the Commissioner is hereby authorized to charge any fee deficiency or credit any over-payment to Deposit Account 503266. Pursuant to 37 C.F.R. § 1.98(a), Requester certifies that no fee is due under 37 U.S.C. § 1.17(v) because there are fewer than 50 documents cited in the IDS accompanying this Request.

Please direct all correspondence in this matter to the undersigned.

Dated: October 17, 2025

Respectfully submitted.

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