IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

EMPIRE TECHNOLOGY DEVELOPMENT LLC,	)	
Plaintiff,	)	C.A. No.
v.	)	**JURY TRIAL DEMANDED**
ADVANCED MICRO DEVICES, INC.,	)	
Defendant.	)	

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Empire Technology Development LLC ("Empire") brings this action and makes the following allegations of patent infringement of U.S. Patent Nos. 9,367,370 (the "'370 Patent") and 9,671,850 (the "'850 Patent") (collectively, "Patents-in-Suit") against Defendant Advanced Micro Devices, Inc. ("AMD") as follows:

THE PARTIES

1. Empire is a limited liability company organized and existing under the laws of the State of Delaware.

2. AMD is a public corporation organized and existing under the laws of the State of Delaware with its principal place of business at 2485 Augustine Drive, Santa Clara, California. AMD may be served with process through its registered agent, The Corporation Trust Company, Corporation Trust Center, 1209 Orange Street, Wilmington, Delaware 19801.

JURISDICTION AND VENUE

3. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1 *et seq*. This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a) because this is a civil action arising under the Patent Act.

4. This Court has personal jurisdiction over AMD under the laws of the State of Delaware, due at least to its status as a corporate entity organized and existing under the laws of the State of Delaware.

5. Venue is proper in this District under 28 U.S.C. §§ 1391 and 1400(b) because AMD has committed, and continues to commit, acts of infringement in this District, and AMD is a resident of the State of Delaware and this District, at least because it is a corporation organized and existing under the laws of the State of Delaware.

THE PATENTS-IN-SUIT

A. U.S. Patent No. 9,367,370

6. On June 14, 2016, the United States Patent and Trademark Office duly issued U.S. Patent No. 9,367,370, entitled "NOC LOOPBACK ROUTING TABLES TO REDUCE I/O LOADING AND OFF-CHIP DELAYS." A true and correct copy of the '370 Patent is attached hereto as Exhibit A.

7. The '370 Patent is directed to devices and methods for efficient message routing in multicore processors.

8. A multicore processor is an integrated circuit, or chip, containing multiple dependent processing units that are called cores. The multiple processing units, or cores, of a microprocessor need to communicate with each other, and they can do so on the processor ("on chip") or off the processor ("off chip"). Off-chip messaging between cores can present various challenges, such as delays and impacts on overall processor performance. The '370 Patent recognizes these challenges:

> [F]or situations in which both the originating and destination instances reside on the same physical hardware, such as different cores on a multicore processor, routing messages through a network external to the hardware (in other words, an

> "off-chip" network) may introduce undesirable and unnecessary network delays and input/output loading at the hardware.

'370 Patent at 3:26-33.

9. The '370 Patent identifies and addresses problems associated with off-chip messaging by teaching and claiming a technique that enables advanced on-chip routing of inter-core messages. That technique involves implementing a "loopback simulation" of inter-core messages.

10. The '370 Patent describes a loopback simulator that intercepts inter-core messages that otherwise might go off chip and redirects those messages on chip.

11. By reducing messages that travel off chip to be communicated, the '370 Patent's technology decreases the distance and computational power required to communicate between cores. This solution results in efficient message routing, substantially increasing microprocessor performance and efficiency.

12. The '370 Patent's application publication has been cited during the prosecution of various patent applications, including U.S. Patent Appl. No. 14/866,869 filed by Intel Corporation, a competitor of AMD in the field of multicore processors.

B. U.S. Patent No. 9,671,850

13. On June 6, 2017, the United States Patent and Trademark Office duly issued U.S. Patent No. 9,671,850, entitled "LEAKAGE CURRENT VARIABILITY BASED POWER MANAGEMENT." A true and correct copy of the '850 Patent is attached hereto as Exhibit B.

14. The '850 Patent is directed to devices, methods, and systems for power management of multicore processors based on leakage current variability.

15. Microprocessors integrate various components that work together, including transistors that control the flow of electrical signals. The '850 Patent explains that smaller

fabrication processes have allowed for a great number of transistors to be packed onto a single chip, resulting in additional processing capacity. However, the use of additional transistors may also result in greater power consumption because transistors and similar components on semiconductor devices, as well as connections between such components, may be subject to leakage current. The ’850 Patent also recognizes that there may be a high variation in the amount of leakage current (or leakage current variability) in different components or areas of the chip.

16. The ’850 Patent addresses problems associated with leakage current by teaching a technique for power management based on leakage current variability. The technique includes generating a micro-architectural leakage map for one or more cores. The technique also includes thread migration and activating or deactivating one or more sub-units of a core in response to certain detections.

17. The ’850 Patent’s technology enables advanced power management within the microprocessor microarchitecture, resulting in better power consumption while still delivering high processor performance.

18. The ’850 Patent’s application publication has been cited during the prosecution of various patent applications, including U.S. Patent Appl. No. 16/833,328 filed by Intel Corporation.

BACKGROUND OF THE ACTION

19. Dr. Ezekiel Kruglick is the inventor of both Patents-in-Suit. Dr. Kruglick holds a Ph.D. in electrical engineering and computer science from the University of California, Berkeley.

20. Dr. Kruglick assigned all of his rights, title, and interests to the Patents-in-Suit to Empire.

COUNT I

(Infringement of U.S. Patent No. 9,367,370)

21. Empire incorporates herein by reference paragraphs 1 through 20 above as if set forth in full.

22. AMD designs, manufactures, uses, sells, and/or offers for sale in the United States products comprising multicore processors that perform on-chip loopback of inter-core messages.

23. Upon information and belief, all AMD products that include, e.g., Zen 3 microarchitecture and/or a later-released generation of Zen microarchitecture infringe at least claim 14 of the '370 Patent.

24. AMD released Ryzen processors with Zen 3 microarchitecture in the U.S. on November 5, 2020, marking AMD's first infringement of the '370 Patent.[1] AMD has also released processors in the Ryzen line that operate with later-released generations of Zen, including Zen 3+, Zen 4, Zen 4c, Zen 5, and Zen 5c.

25. On information and belief, AMD's products that operate with, e.g., Zen 3 microarchitecture and/or a later-released Zen microarchitecture include the following series of processors in AMD's Ryzen line, and are further identified by series and model number in Exhibit C: 5000, PRO 5000, Embedded 5000, Threadripper PRO 5000 WX, 6000, PRO 6000, Z2, 7000, PRO 7000, Threadripper 7000, Threadripper PRO 7000 WX, 8000, PRO 8000, 200, PRO 200, 9000, Z1, AI 300, AI Max 300, AI Max PRO 300, AI PRO 300, Threadripper 9000, and Threadripper PRO 9000 WX.

26. AMD released EPYC processors with Zen 3 microarchitecture in the U.S. on March 15, 2021. AMD has also released processors in the EPYC line that operate with later-

[1] https://ir.amd.com/news-events/press-releases/detail/972/amd-launches-amd-ryzen-5000-series-desktop-processors-the-fastest-gaming-cpus-in-the-world.

released generations of Zen, including Zen 4, Zen 4c, and Zen 5c. On information and belief, AMD's products that operate with, e.g., Zen 3 and/or a later-released Zen microarchitecture include the following series of processors in AMD's EPYC line, and are further identified by series and model number in Exhibit C: 7003, 4004, 4005, 8004, 9004, and 9005.

27. At least all AMD products identified above that operate with Zen 3 or newer Zen microarchitectures infringe the '370 Patent, including the Ryzen and EPYC series products (the "'370 Patent Infringing Products").

28. AMD has infringed and continues to infringe the '370 Patent, including at least claim 14 of the '370 Patent, pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling, exporting from, and/or importing into the United States the '370 Patent Infringing Products, without authority or license.

29. AMD indirectly infringes the '370 Patent, including at least claim 14 of the '370 Patent, pursuant to 35 U.S.C. § 271(b), by (among other things) and with specific intent or willful blindness, actively aiding and abetting infringement by others, such as AMD's customers and end-users, in this District and elsewhere in the United States. For example, AMD's customers and end-users directly infringe through their use of the inventions claimed in the '370 Patent. AMD induces this direct infringement through its affirmative acts of manufacturing, selling, distributing, and/or otherwise making available the '370 Patent Infringing Products, and providing instructions, documentation, and other information to customers and end-users instructing them to use the '370 Patent Infringing Products in an infringing manner, including (i) instruction, technical support and services, (ii) training, white papers, product manuals, datasheets, marketing, and advertisements, and (iii) software providing the foregoing and enabling customers and end-users to use the '370 Patent Infringing Products in an infringing manner. As a result of AMD's inducement, AMD's

customers and end-users use the ’370 Patent Infringing Products in the way that AMD intends and that directly infringes the ’370 Patent. At least since receiving notice of this Complaint, AMD has known of the ’370 Patent, and that the ’370 Patent Infringing Products infringe the ’370 Patent, or has been willfully blind to such infringement. Despite this knowledge of the ’370 Patent and that the ’370 Patent Infringing Products infringe the ’370 Patent, AMD has continued to perform these affirmative acts with the intent, or willful blindness, that the induced acts directly infringe the ’370 Patent.

30. AMD also indirectly infringes the ’370 patent, including at least claim 14 of the ’370 Patent, pursuant to 35 U.S.C. § 271(c), by contributing to direct infringement committed by others, such as customers and end-users, in this District and elsewhere in the United States. AMD’s affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the ’370 Patent Infringing Products and causing the ’370 Patent Infringing Products to be manufactured, used, sold, and offered for sale, contribute to AMD’s customers’ and end-users’ use of the ’370 Patent Infringing Products, such that the ’370 Patent is directly infringed. The ’370 Patent Infringing Products are a material part of the invention of the ’370 Patent, are not a staple article or commodity of commerce, have no substantial non-infringing use, and are known by AMD to be especially made or adapted for use in the infringement of the ’370 Patent. At least since receiving notice of this Complaint, AMD has known of the ’370 Patent, and that the ’370 Patent Infringing Products infringe the ’370 Patent, or has been willfully blind to such infringement. Despite this knowledge of the ’370 Patent and that the ’370 Patent Infringing Products infringe the ’370 Patent, AMD has continued to perform these affirmative acts with knowledge of the ’370 Patent and with intent, or willful blindness, that these acts cause the direct infringement of the ’370 Patent.

31. Claim 14 of the ’370 Patent is reproduced below with the addition of labels [a], [b], [c], [d], [e], and [f] corresponding to portions of the claim.

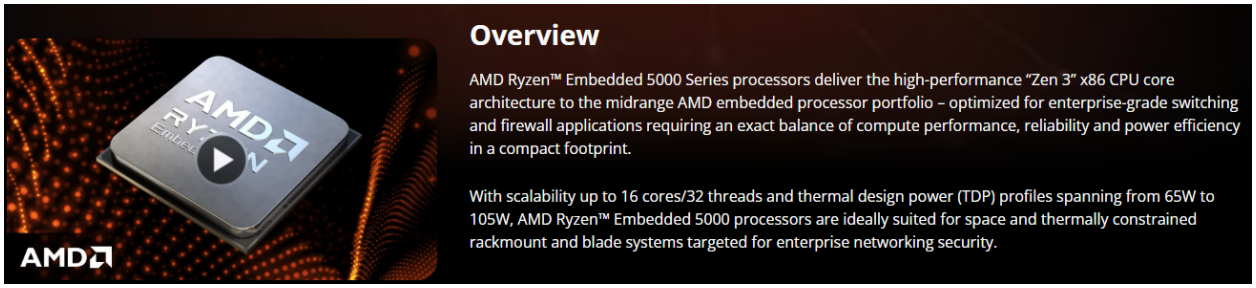
> 14. A multicore processor adapted to perform on-chip loopback, the multicore processor comprising:
>
> [a] a plurality of processor cores;
>
> [b] a controller configured to identify one or more processes executing on the plurality of processor cores, the processes adapted to communicate with each other via an off-chip network, wherein the controller is further configured to:
>
> [c] generate a core-process-to-IP-address map;
>
> [d] identify a designation processor core for a message based on the core-process-to-IP-address map; and
>
> [e] identify data associated with a message to be delivered to the identified destination processor core; and
>
> [f] a loopback simulator at a processor hardware layer, the loopback simulator configured to deliver messages between the one or more processes via on-chip communication by processing the identified data back into one or more on-chip flits to be delivered to the identified destination processor core.

32. The ’370 Patent Infringing Products embody each and every limitation of at least claim 14 of the ’370 Patent, literally or under the doctrine of equivalents, as described in the non-limiting examples set forth below. These non-limiting examples are preliminary and are not intended to limit Empire’s right to modify these non-limiting examples or allege that other aspects of AMD’s products infringe the identified claim, or any other claims, of the ’370 Patent.

33. The ’370 Patent Infringing Products comprise a multicore processor adapted to perform on-chip loopback.

34. AMD’s Zen 3 microarchitecture and later generations of AMD’s Zen microarchitecture are intended for multicore processors. For example, AMD’s EPYC 7003 Series processors, which feature Zen 3 microarchitecture, comprise processors that contain up to 64 cores.[2]

35. As another example, AMD’s Ryzen Embedded 5000 Series processors “deliver the high-performance performance ‘Zen 3’ x86 CPU core architecture” and with “scalability up to 16 cores.”



https://www.amd.com/en/products/embedded/ryzen/ryzen-5000-series.html#specifications.

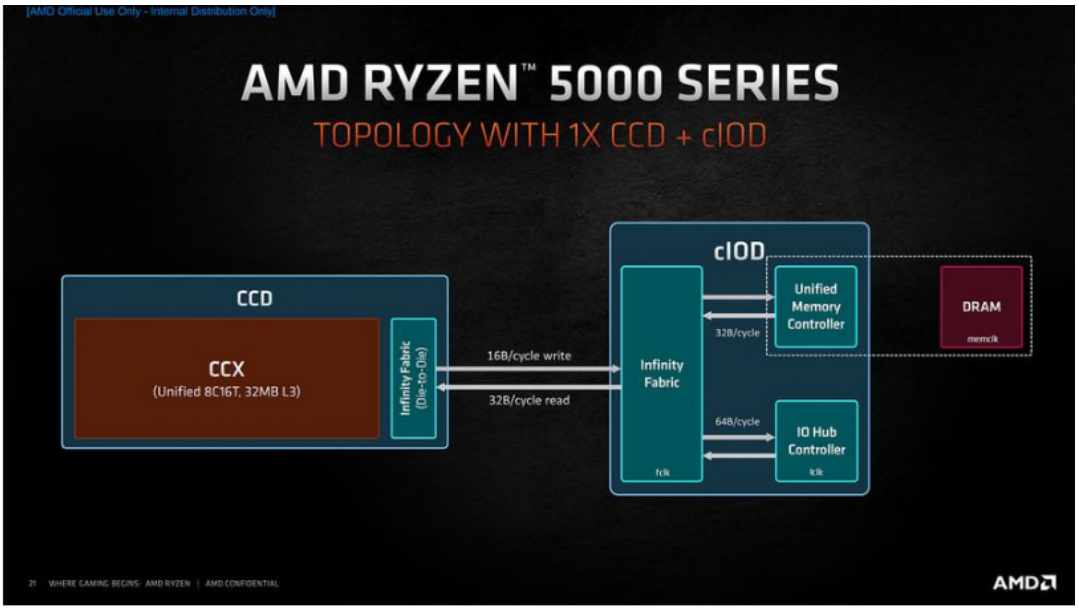
36. As yet another example, AMD’s EPYC 9005 Series processors, which feature Zen 5 microarchitecture, contain up to 192 cores.[3]

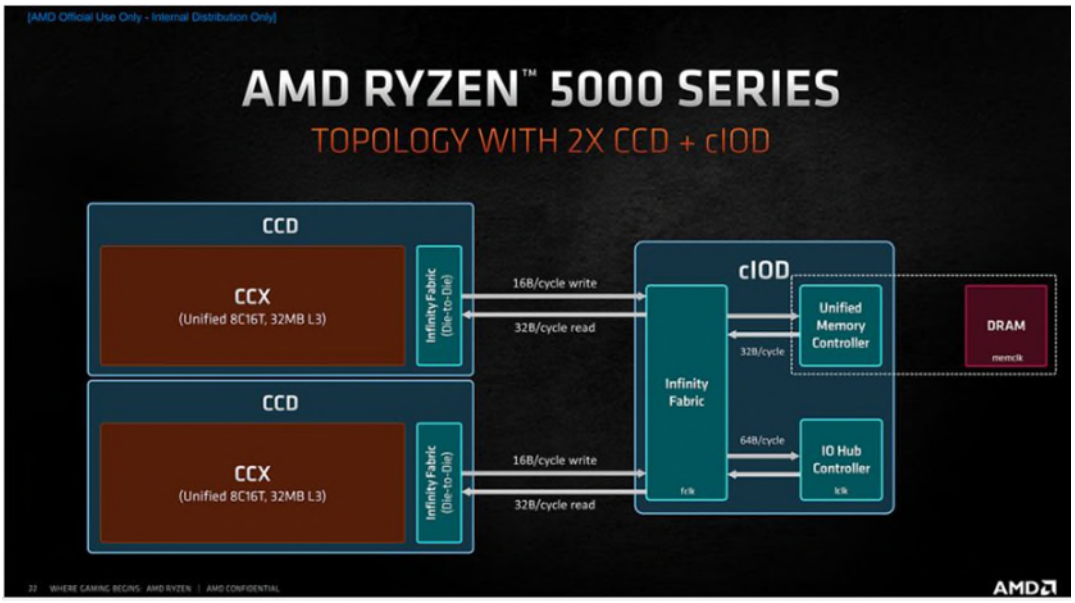
37. The on-chip loopback capabilities of the ’370 Patent Infringing Products are discussed below in connection with claim element [f]. See paragraphs 53-59 below.

38. The ’370 Patent Infringing Products contain a plurality of processor cores.

[2] https://www.amd.com/content/dam/amd/en/documents/epyc-technical-docs/white-papers/overview-amd-epyc7003-series-processors-microarchitecture.pdf at 1.
[3] https://www.amd.com/content/dam/amd/en/documents/epyc-technical-docs/user-guides/58462_amd-epyc-9005-tg-architecture-overview.pdf at 3.

39. AMD's Zen 3 microarchitecture includes a Core Complex Die ("CCD"), a physical die that houses a single group of processor cores called a Core Complex ("CCX"). The images below show the topology of the Zen 3 microarchitecture with, e.g., one CCD or two CCDs, where each CCD contains one CCX.





https://www.geeks3d.com/20201106/amd-ryzen-5000-series-processors-launched-zen-3-architecture/; https://www.semiaccurate.com/2020/11/07/a-long-look-at-amds-zen-3-core-and-chips/.

40. Each CCX in AMD's Zen 3 microarchitecture includes up to eight cores.[4] For example, in connection with the EPYC 70003 Series processor, AMD explains that "up to eight 'Zen 3' core compute units share a L3 or Last Level Cache (LLC)" and "this grouping is called a Core Complex (CCX)."[5] The diagram below further demonstrates that each CCX in the Zen 3 microarchitecture includes eight cores.

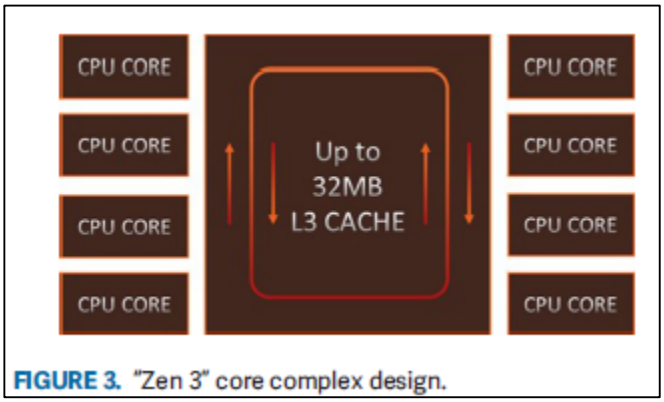


FIGURE 3. "Zen 3" core complex design.

https://ieeexplore.ieee.org/document/9718180 at 11.

41. The '370 Patent Infringing Products include a controller configured to identify one or more processes executing on the plurality of processor cores, the processes adapted to communicate with each other via an off-chip network.

42. For example, in connection with AMD's EPYC 7003 Series processors, which implement Zen 3 microarchitecture, AMD states that the "CCDs connect to memory, I/O" (input/output), "and each other through the I/O die (IOD)."[6] As demonstrated in the illustration below, the IOD contains, e.g., Unified Memory Controllers ("UMCs"). The controllers are

[4] https://nas.nasa.gov/assets/nas/pdf/ams/2021/AMS_20210720_Hogan-ONeill.pdf at 12.
[5] https://www.amd.com/content/dam/amd/en/documents/epyc-technical-docs/white-papers/overview-amd-epyc7003-series-processors-microarchitecture.pdf at 4.
[6] https://www.amd.com/content/dam/amd/en/documents/epyc-technical-docs/white-papers/overview-amd-epyc7003-series-processors-microarchitecture.pdf at 5.

configured to identify one or more processes executing on the plurality of processor cores, where the processes are adapted to communicate with each other via an off-chip network.

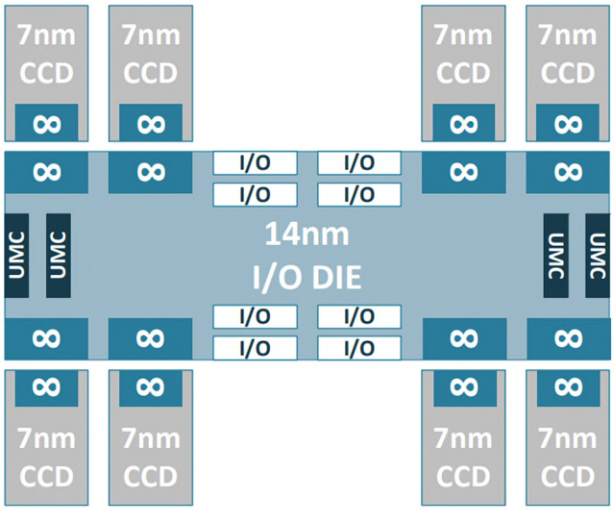
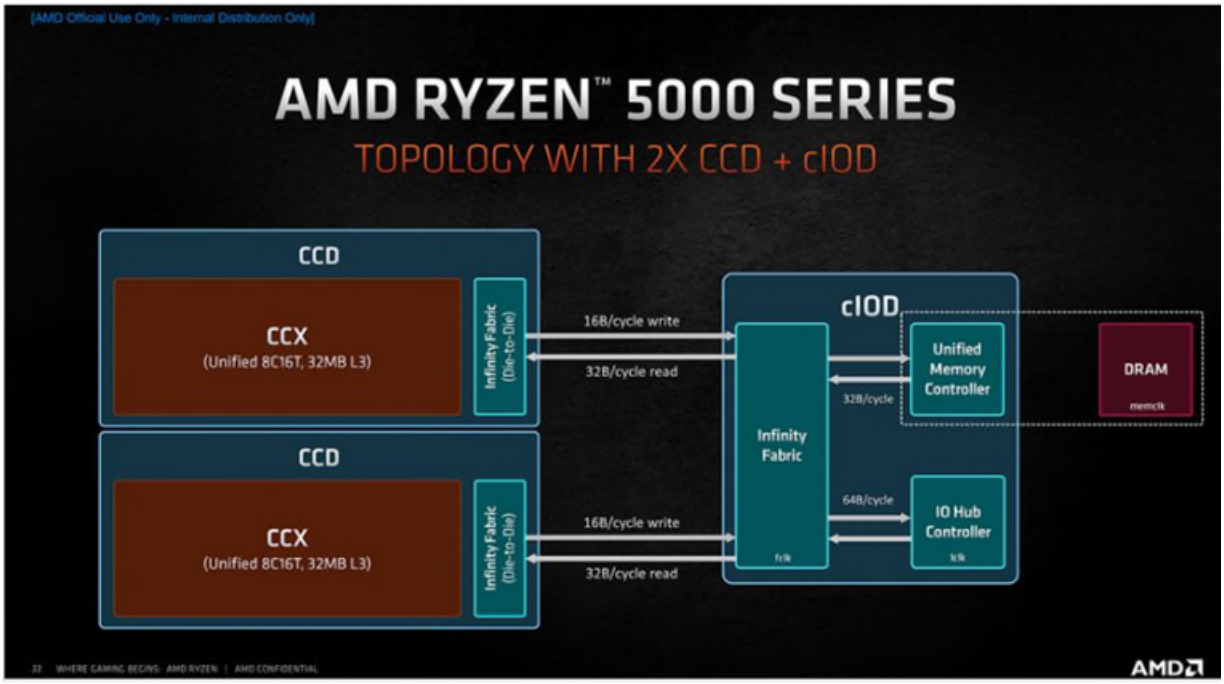


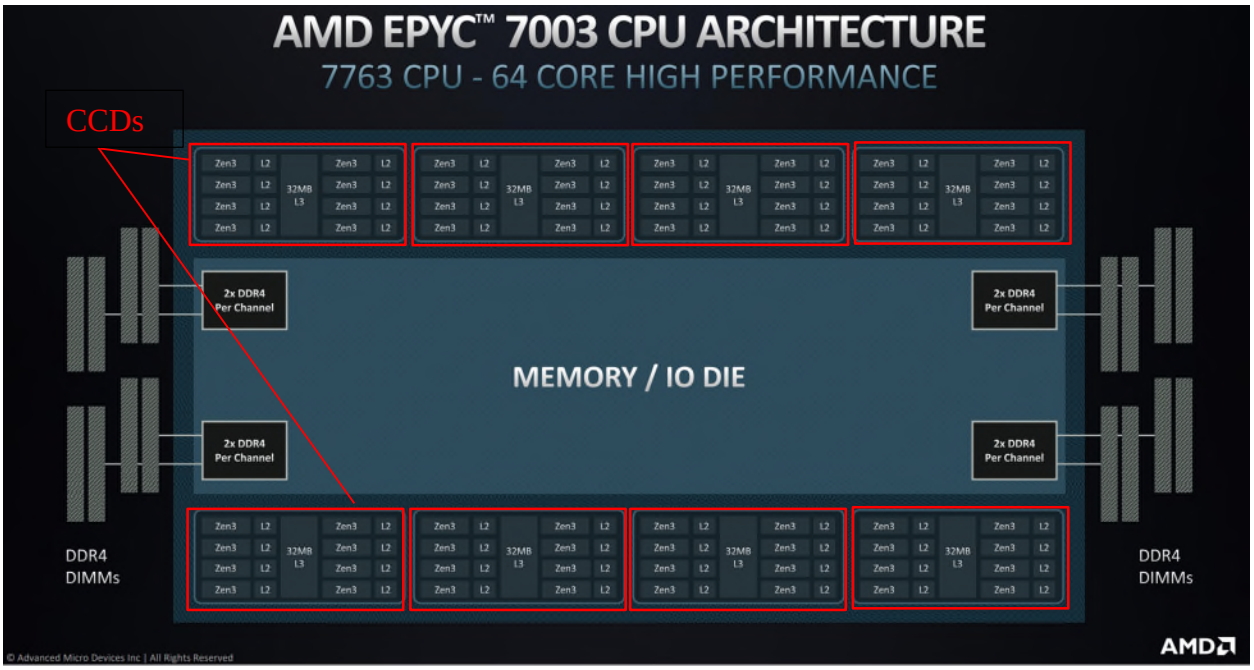
Figure 2-4: AMD EPYC 7003 Series Processor internal CCD, I/O, and Unified Memory Controller (UMC) topology to AMD Infinity Fabric

https://www.amd.com/content/dam/amd/en/documents/epyc-technical-docs/white-papers/overview-amd-epyc7003-series-processors-microarchitecture.pdf at 5.

43. The illustrations below demonstrate that the Zen 3 microarchitecture incorporated into the Infringing Products connects CCDs to a memory, such as Unified Memory Controller and IO Hub Controller, and other components via Infinity Fabric technology.



https://www.geeks3d.com/20201106/amd-ryzen-5000-series-processors-launched-zen-3-architecture/; https://www.semiaccurate.com/2020/11/07/a-long-look-at-amds-zen-3-core-and-chips/.



https://nas.nasa.gov/assets/nas/pdf/ams/2021/AMS_20210720_Hogan-ONeill.pdf at 13 (annotated).

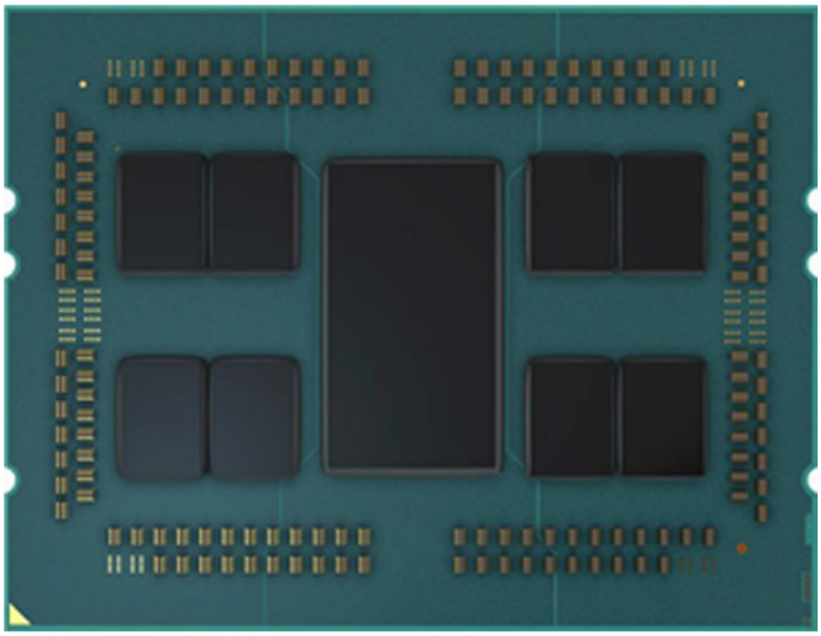
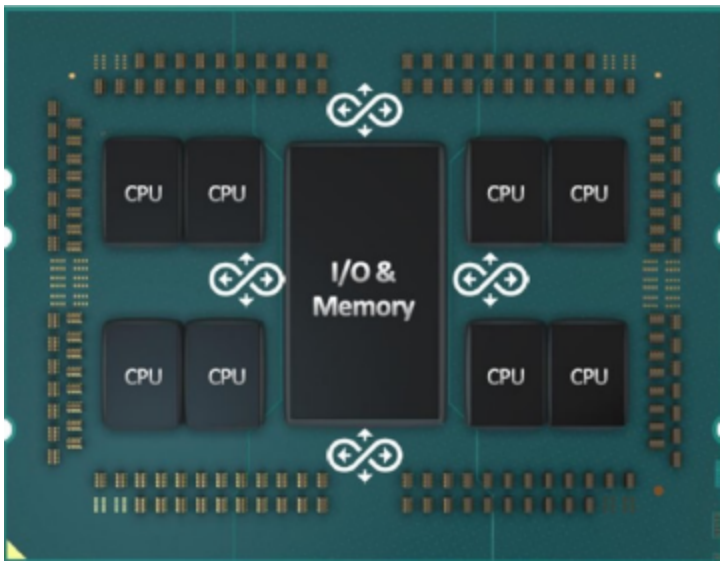


Figure 2-1: AMD EPYC 7003 configuration with 8 Core Complex Dies (CCD) surrounding central I/O Die (IOD)

https://www.amd.com/content/dam/amd/en/documents/epyc-technical-docs/white-papers/overview-amd-epyc7003-series-processors-microarchitecture.pdf at 3.

44. Similarly, AMD's Ryzen Threadripper Pro Series processors "integrate multiple 8-core 'Zen 3' CCX (Core Complex) chiplets, each tied to memory, I/O and each other via AMD Infinity Fabric architecture interconnect."



https://www.amd.com/content/dam/amd/en/documents/processor-tech-docs/white-papers/threadripperpro-white-paper-third-wave-workstation-computing.pdf at 3.

45. As another example, in AMD's EPYC 9005 Series processors with Zen 5 microarchitecture, the "CCDs connect to memory, I/O, and each other's CCXs through the I/O die (IOD)."[7] As demonstrated in the illustration below, the IOD contains, e.g., UMCs. The controllers are configured to identify one or more processes executing on the plurality of processor cores, the processes adapted to communicate with each other via an-off chip network.

[7] https://www.amd.com/content/dam/amd/en/documents/epyc-technical-docs/user-guides/58462_amd-epyc-9005-tg-architecture-overview.pdf at 5.

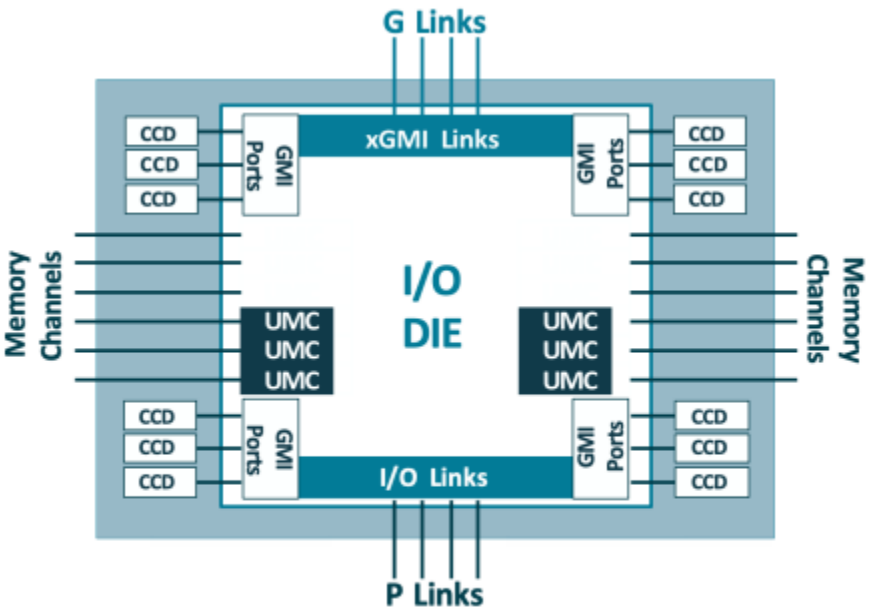


Figure 2-5: AMD EPYC 9005 IOD AMD

https://www.amd.com/content/dam/amd/en/documents/epyc-technical-docs/user-guides/58462_amd-epyc-9005-tg-architecture-overview.pdf at 5.

46. The image below further illustrates AMD's EPYC 9005 Series processors incorporating "compute cores, memory controllers, I/O controllers" into an "integrated System on a Chip (SoC)." The SoC includes the CCDs which contain CCXs, which contain the cores. The CCDs "surround the central high-speed I/O Die (and interconnect via the Infinity Fabric)."

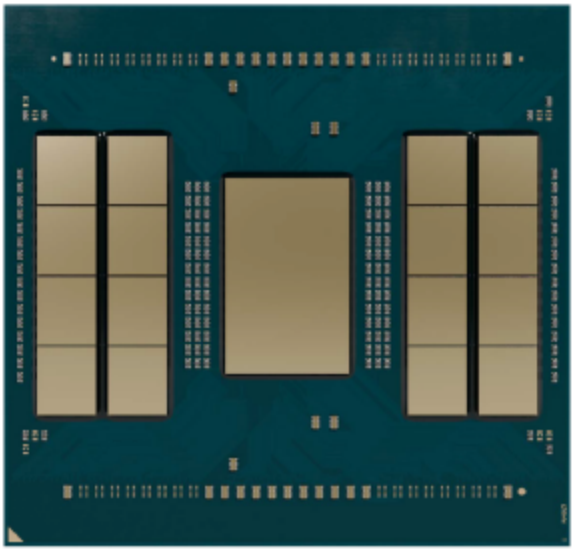


Figure 2-1: AMD EPYC 9005 processor with central I/O Die and 16 Zen 5 Classic-based Core Complex Dies

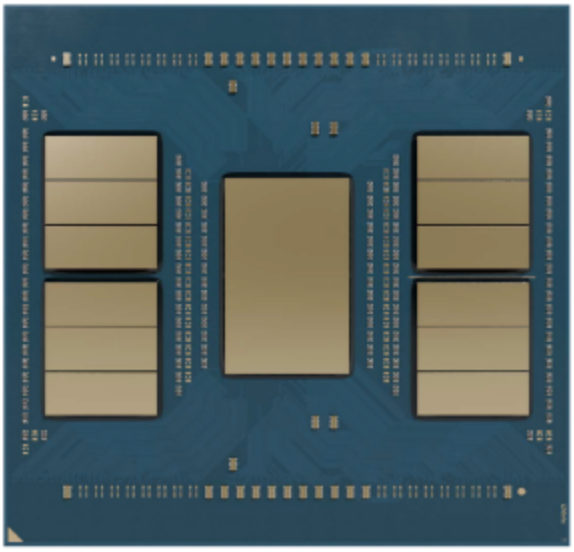


Figure 2-2: AMD EPYC 9005 processor with central I/O Die and 12 Zen 5c "Dense"-based Core Complex Dies

https://www.amd.com/content/dam/amd/en/documents/epyc-technical-docs/user-guides/58462_amd-epyc-9005-tg-architecture-overview.pdf at 4.

47. AMD describes its "Infinity Architecture" as follows:

> The heart of the AMD Infinity Architecture is a leadership interconnect that supports extraordinary levels of scale at every layer. Components communicate using AMD Infinity Fabric technology—a connection that is used between CPUs, between components in the multi-chip architecture, and to connect processor cores, memory, PCIe® Gen 5 I/O, and security mechanisms. As a result, the architecture delivers breakthrough performance and efficiency to deliver on the promise of next-generation computing.[8]

48. This architecture further demonstrates that the '370 Patent Infringing Products include a controller configured to identify one or more processes executing on the plurality of processor cores, where the processes are adapted to communicate with each other via an off-chip network.

49. The '370 Patent Infringing Products include a controller configured to generate a core-process-to-IP-address map, identify a designation processor core for a message based on the

[8] https://www.amd.com/en/products/processors/server/epyc/4th-generation-architecture.html at 7.

core-process-to-IP address map, and identify data associated with a message to be delivered to the identified designation processor core.

50. For example, in AMD's EPYC 7003 Series processors with Zen 3 microarchitecture, the "CCDs connect to memory, I/O, and each other through the I/O die (IOD)," where the IOD contains, e.g., UMCs.[9] The controllers are configured to generate a core-process-to-IP-address map, identify a designation processor core for a message based on the core-process-to-IP-address map, and identify data associated with a message to be delivered to the identified destination processor core.

51. As another example, AMD's Ryzen Threadripper Pro Series processors "integrate multiple 8-core 'Zen 3' CCX (Core Complex) chiplets, each tied to memory, I/O and each other via AMD Infinity Fabric architecture interconnect."[10]

52. As a further example, in AMD's EPYC 9005 Series processors with Zen 5 microarchitecture, the "CCDs connect to memory, I/O, and each other's CCXs through the I/O die (IOD)."[11]

53. The '370 Patent Infringing Products include a loopback simulator at a processor hardware layer, where the loopback simulator is configured to deliver messages between the one or more processes via on-chip communication by processing the identified data back into one or more on-chip flits[12] to be delivered to the identified destination processor core.

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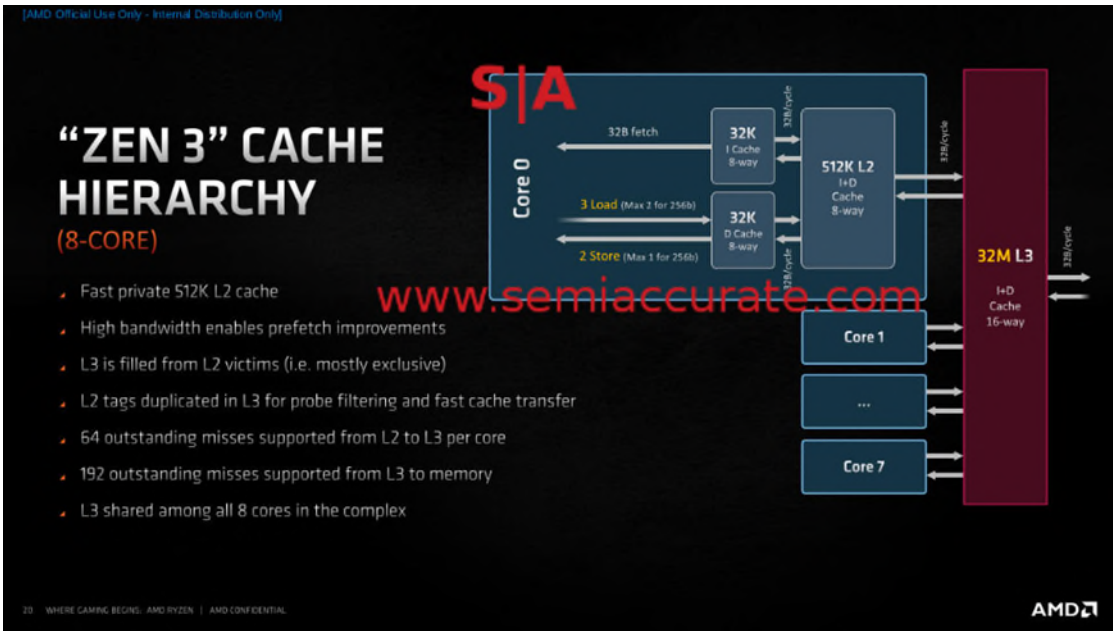
[9] https://www.amd.com/content/dam/amd/en/documents/epyc-technical-docs/white-papers/overview-amd-epyc7003-series-processors-microarchitecture.pdf at 5.
[10] https://www.amd.com/content/dam/amd/en/documents/processor-tech-docs/white-papers/threadripperpro-white-paper-third-wave-workstation-computing.pdf at 3.
[11] https://www.amd.com/content/dam/amd/en/documents/epyc-technical-docs/user-guides/58462_amd-epyc-9005-tg-architecture-overview.pdf at 5.
[12] In Network-on-Chip ("NoC") architectures, which are communication networks that may enable communication between cores, messages may be broken down into smaller units called packets, which also may be split into smaller units.

54. The images below demonstrate certain differences between the Zen 2 and Zen 3 microarchitectures that AMD contends improved performance of Zen 3. In AMD's Zen 2 microarchitecture, the CCXs in a CCD were not directly connected, and as result, communication between certain cores had to be routed off the die, or off chip.[13] Zen 3 redesigned the CCXs with eight cores that share a common "L3 cache," allowing for on-chip communication between the cores.[14]

[13] https://www.semiaccurate.com/2020/11/07/a-long-look-at-amds-zen-3-core-and-chips/.
[14] https://www.semiaccurate.com/2020/11/07/a-long-look-at-amds-zen-3-core-and-chips/; https://ieeexplore.ieee.org/document/9718180.



https://www.semiaccurate.com/2020/11/07/a-long-look-at-amds-zen-3-core-and-chips/.

55. AMD's EPYC 7003 Series processors, for example, implement Zen 3 microarchitecture that comprises eight CCDs, where each CCD contains one CCX, and each CCX contains eight cores that share a common L3 cache. This configuration is demonstrated in the figure below.

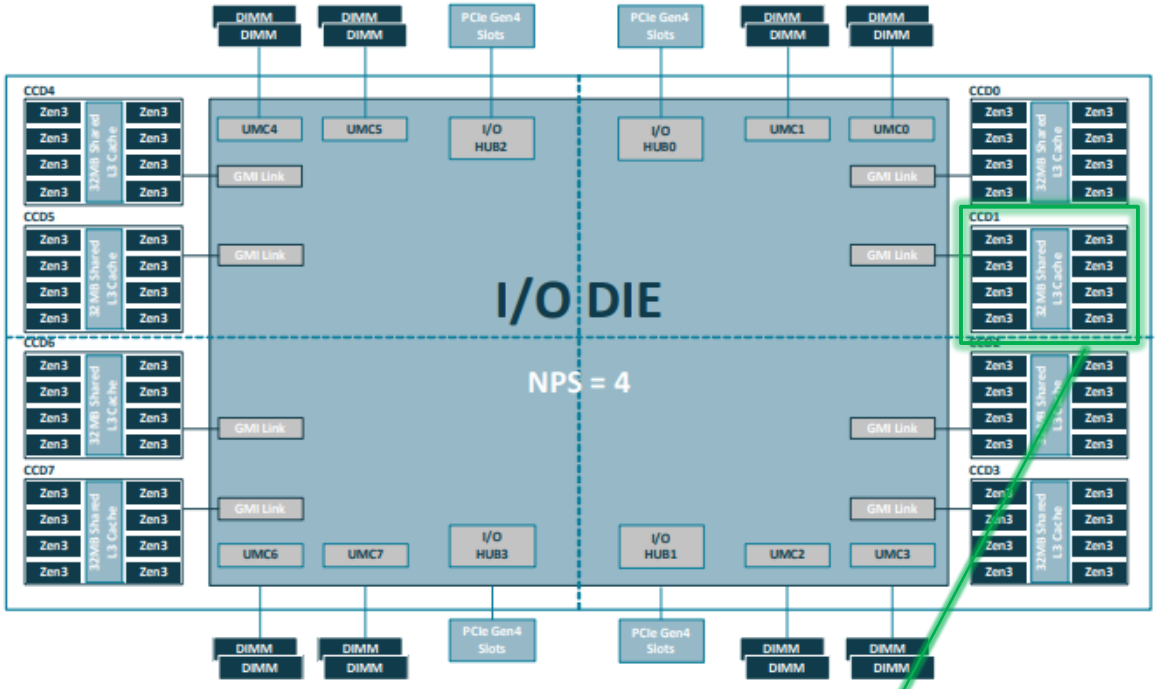
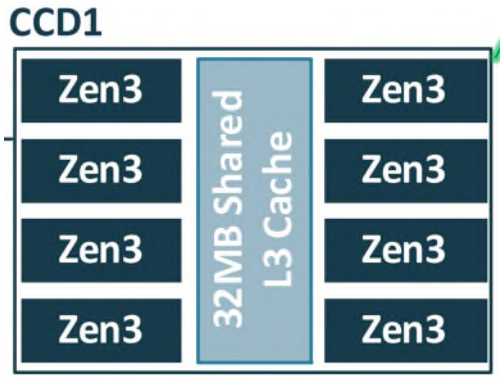


Figure 2-5: EPYC 7003 System on Chip (SoC) consists of 8 CCDs and central IOD



https://www.amd.com/content/dam/amd/en/documents/epyc-technical-docs/white-papers/overview-amd-epyc7003-series-processors-microarchitecture.pdf at 6 (annotated).

56. As another example, in AMD's EPYC 9005 Series processors that implement Zen 5 microarchitecture, each CCX has up to eight "cores sharing a 32 MB L3 cache."[15]

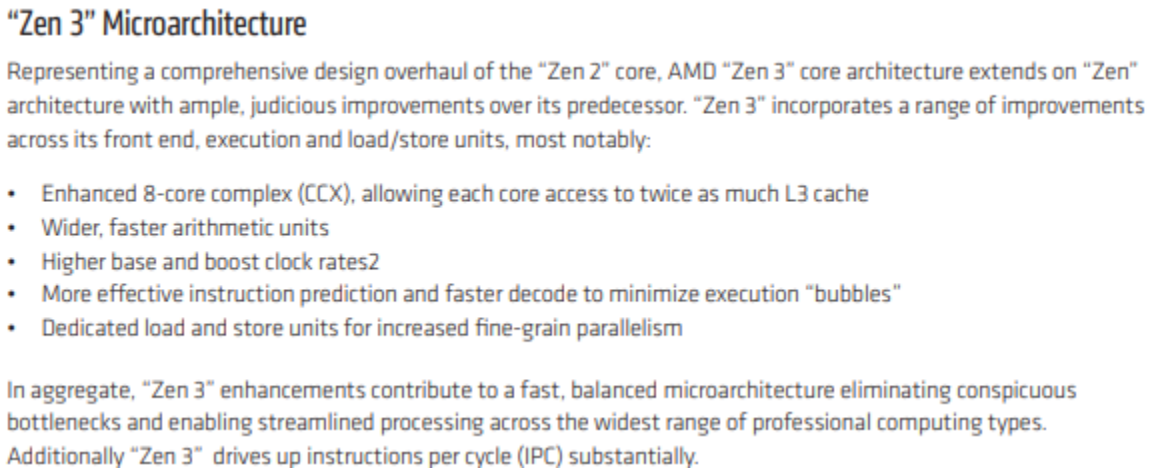
57. "L3 cache" refers to "Level 3 cache," which is a type of memory containing, e.g., frequently used data shared by cores. Alone and/or in combination with other features of the '370

[15] https://www.amd.com/content/dam/amd/en/documents/epyc-technical-docs/user-guides/58462_amd-epyc-9005-tg-architecture-overview.pdf at 4.

Patent Infringing Products, L3 caches play a critical role in facilitating, and demonstrate the capability of, loopback and inter-core messaging. For example, Zen 3's "L3 complex . . . offers better inter-core latencies" (or communication times). Inter-core latencies within Zen 3's L3 cache "lie in at 15-19ns" while "latencies between cores in different CCDs still incur[] a larger latency penalty of 79-80ns."[16]

58. The configuration of the CCXs with cores that share a common L3 cache demonstrate that the '370 Patent Infringing Products comprise a loopback simulator at a processor hardware layer, the loopback simulator configured to deliver messages between the one or more processes via on-chip communication by processing the identified data back into one or more on-chip flits to be delivered to the identified destination processor core.

59. For example, in describing the improvements of the Zen 3 microarchitecture over the Zen 2 microarchitecture, AMD states that the "enhancements contribute to a fast, balanced microarchitecture eliminating conspicuous bottlenecks and enabling streamlined processing across the widest range of professional computing types."



"Zen 3" Microarchitecture

Representing a comprehensive design overhaul of the "Zen 2" core, AMD "Zen 3" core architecture extends on "Zen" architecture with ample, judicious improvements over its predecessor. "Zen 3" incorporates a range of improvements across its front end, execution and load/store units, most notably:

- Enhanced 8-core complex (CCX), allowing each core access to twice as much L3 cache
- Wider, faster arithmetic units
- Higher base and boost clock rates2
- More effective instruction prediction and faster decode to minimize execution "bubbles"
- Dedicated load and store units for increased fine-grain parallelism

In aggregate, "Zen 3" enhancements contribute to a fast, balanced microarchitecture eliminating conspicuous bottlenecks and enabling streamlined processing across the widest range of professional computing types. Additionally "Zen 3" drives up instructions per cycle (IPC) substantially.

https://www.amd.com/content/dam/amd/en/documents/processor-tech-docs/white-papers/threadripperpro-white-paper-third-wave-workstation-computing.pdf at 5.

[16] https://web.archive.org/web/20201106074312/https://www.anandtech.com/show/16214/amd-zen-3-ryzen-deep-dive-review-5950x-5900x-5800x-and-5700x-tested/5.

60. At least since receiving notice of this Complaint, AMD's infringement of the '370 Patent is willful.

61. Without permission from or compensation to Empire, AMD has sold—and continues to sell—very substantial numbers of '370 Patent Infringing Products in the U.S. based on the pioneering technology in the '370 Patent.

62. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '370 Patent. Empire has satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law for the infringement of the '370 Patent.

63. As a result of AMD's infringement of the '370 Patent, Empire has suffered monetary damages, and seeks recovery in an amount adequate to compensate for AMD's infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

COUNT II

(Infringement of U.S. Patent No. 9,671,850)

64. Empire incorporates herein by reference paragraphs 1 through 63 above as if set forth in full.

65. AMD designs, manufactures, uses, sells, and/or offers for sale in the United States products that perform leakage current variability based power management.

66. All AMD products that include, e.g., Zen 3+ microarchitecture and/or a later-released generation of Zen microarchitecture infringe at least claim 12 of the '850 Patent.

67. AMD released products that operate with Zen 3+ on April 1, 2022, marking AMD's first infringement of the '850 Patent.

68. On information and belief, AMD's products that operate with, e.g., Zen 3+ microarchitecture and/or a later-released Zen microarchitecture include the following series of

processors in AMD's Ryzen line, and are further identified by series and model number in Exhibit D: 6000, PRO 6000, Z2, 7000, PRO 7000, Threadripper 7000, Threadripper PRO 7000 WX, 8000, PRO 8000, 200, PRO 200, 9000, Z1, AI 300, AI Max 300, AI Max PRO 300, AI PRO 300, Threadripper 9000, and Threadripper PRO 9000 WX. On information and belief, AMD's products that operate with, e.g., Zen 3+ and/or a later-released Zen microarchitecture include the following series of processors in AMD's EPYC line, and are further identified by series and model number in Exhibit D: 4004, 4005, 8004, 9004, and 9005.

69. At least all AMD products identified above that operate with Zen 3+ or newer Zen microarchitecture infringe the '850 Patent, including the Ryzen and EPYC series products (the "'850 Patent Infringing Products").

70. AMD has infringed and continues to infringe the '850 Patent, including at least claim 12 of the '850 Patent, pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling, exporting from, and/or importing into the United States the '850 Patent Infringing Products, without authority or license.

71. AMD indirectly infringes the '850 Patent, including at least claim 12 of the '850 Patent, pursuant to 35 U.S.C. § 271(b), by (among other things) and with specific intent or willful blindness, actively aiding and abetting infringement by others, such as AMD's customers, and end-users, in this District and elsewhere in the United States. For example, AMD's customers and end-users directly infringe through their use of the inventions claimed in the '850 Patent. AMD induces this direct infringement through its affirmative acts of manufacturing, selling, distributing, and/or otherwise making available the '850 Patent Infringing Products, and providing instructions, documentation, and other information to customers and end-users instructing them to use the '850 Patent Infringing Products in an infringing manner, including (i) instruction, technical support and

services, (ii) training, white papers, product manuals, datasheets, marketing, and advertisements, and (iii) software providing the foregoing and enabling customers and end-users to use the ’850 Patent Infringing Products in an infringing manner. As a result of AMD’s inducement, AMD’s customers and end-users use the ’850 Patent Infringing Products in the way that AMD intends and that directly infringes the ’850 Patent. At least since receiving notice of this Complaint, AMD has known of the ’850 Patent, and that the ’850 Patent Infringing Products infringe the ’850 Patent, or has been willfully blind to such infringement. Despite this knowledge of the ’850 Patent and that the ’850 Patent Infringing Products infringe the ’850 Patent, AMD has continued to perform these affirmative acts with the intent, or willful blindness, that the induced acts directly infringe the ’850 Patent.

72. AMD also indirectly infringes the ’850 Patent, including at least claim 12 of the ’850 Patent, pursuant to 35 U.S.C. § 271(c), by contributing to direct infringement committed by others, such as customers and end-users, in this District and elsewhere in the United States. AMD’s affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the ’850 Patent Infringing Products and causing the ’850 Patent Infringing Products to be manufactured, used, sold, and offered for sale, contribute to AMD’s customers’ and end-users’ use of the ’850 Patent Infringing Products, such that the ’850 Patent is directly infringed. The ’850 Patent Infringing Products are a material part of the invention of the ’850 Patent, are not a staple article or commodity of commerce, have no substantial non-infringing use, and are known by AMD to be especially made or adapted for use in the infringement of the ’850 Patent. At least since receiving notice of this Complaint, AMD has known of the ’850 Patent, and that the ’850 Patent Infringing Products infringe the ’850 Patent, or has been willfully blind to such infringement. Despite this knowledge of the ’850 Patent and that the ’850 Patent Infringing

Products infringe the ’850 Patent, AMD has continued to perform these affirmative acts with knowledge of the ’850 Patent and with intent, or willful blindness, that these acts cause the direct infringement of the ’850 Patent.

73. Claim 12 of the ’850 Patent is reproduced below with the addition of labels [a], [b], [c], [d], [e], [f], [g], [h], and [i] corresponding to portions of the claim.

> 12. A method to provide a leakage current variability based power management, the method comprising:
>
> [a] a memory; and
>
> [b] a processor coupled to the memory, wherein the processor includes one or more cores and is configured to execute a power management application in conjunction with one or more instructions stored in the memory,
>
> [c] wherein the power management application is configured to: receive computation data from a power controller and one or more processor instruction counters (PIC) of one of the one or more cores of the processor;
>
> [d] generate a table of linear combination samples from the computation data, wherein the one or more instructions are grouped based on one or more sub-units of a selected core associated with each one of the one or more instructions, and wherein each of the linear combination samples include a power usage value for a sub-unit of the selected core;
>
> [e] generate a micro-architectural leakage map of the selected core from the linear combination samples within the table;

[f] in response to detection that a second sub-unit being deactivated based on the micro-architectural leakage map, direct a thread of a subset of the one or more instructions to a first sub-unit;

[g] in response to detection that the first sub-unit is unable to compensate the deactivation of the second sub-unit, reactivate the second sub-unit;

[h] execute a thread migration operation to move the thread from the first sub-unit to the second sub-unit, the thread to be executed by the second sub-unit; and

[i] in response to a completion of an execution of the thread: move the thread back to the first sub-unit, and deactivate the second sub-unit.

74. The ’850 Patent Infringing Products embody each and every limitation of at least claim 12 of the ’850 Patent, literally or under the doctrine of equivalents, as described in the non-limiting examples set forth below. These non-limiting examples are preliminary and are not intended to limit Empire’s right to modify these non-limiting examples or allege that other aspects of AMD’s products infringe the identified claim, or any other claims, of the ’850 Patent.

75. The ’850 Patent Infringing Products perform a method to provide a leakage current variability based power management.

76. AMD states that the “‘Zen 3+’ core delivers power and efficiency, through new adaptive power management features that adjust speed quickly, and new deep sleep states that help save on power.”[17]

77. Zen 3+ features the following “five-pronged approach” in power management:

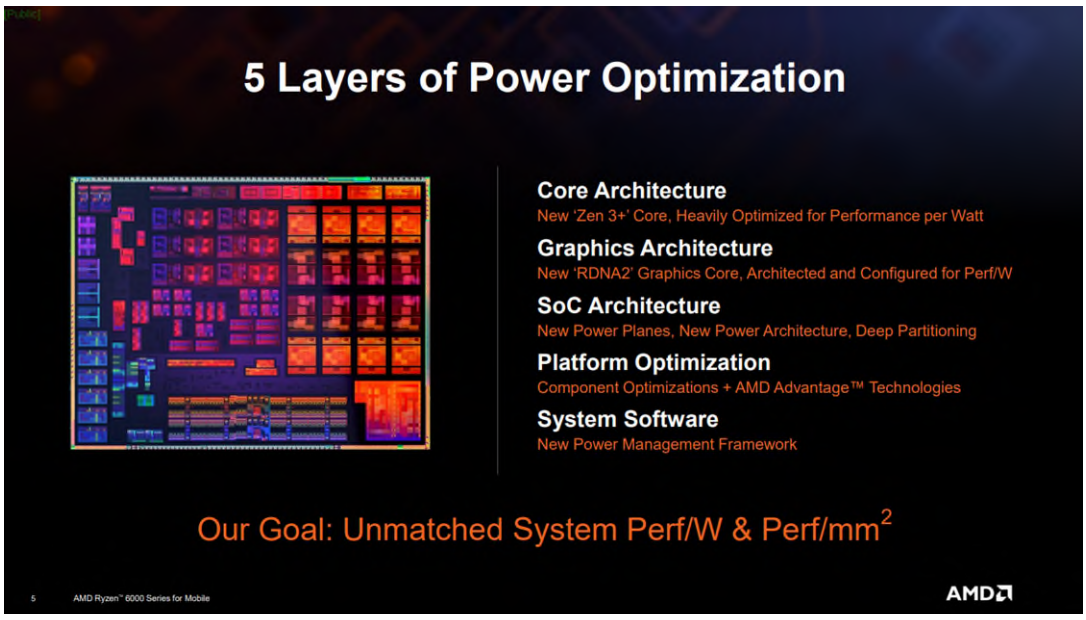
> The first of course is the energy-efficiency gains obtained from the switch to the 6 nm process, which yields a roughly 18% transistor density gain, and improvements with iso-power.

[17] https://ir.amd.com/news-events/press-releases/detail/1039/amdunveils-new-ryzen-mobile-processors-uniting-zen-3-core-with-amd-rdna-2-graphics-in-powerhousedesign.

> ***The second is optimizations to the CPU microarchitecture, with fine-grained power-gating of individual cores within the CPU.***
>
> ***The third includes the SoC-level power optimization that introduces several new power-planes, deep-partitioning of components that allows pretty much all redundant/scalable components to be turned off when not needed.***
>
> ***The fourth is firmware-level optimization. The system firmware now has greater interactivity with the OS [Operating System] to understand the nature of the performance demand.***
>
> And lastly, at the platform-level, AMD works with notebook OEMs to choose the most efficient discrete components that make up the system, along with AMD Advantage device co-engineering.

https://www.techpowerup.com/292118/amd-zen3-architecture-and-ryzen-6000-rembrandt-mobile-processors-detailed (emphasis added).

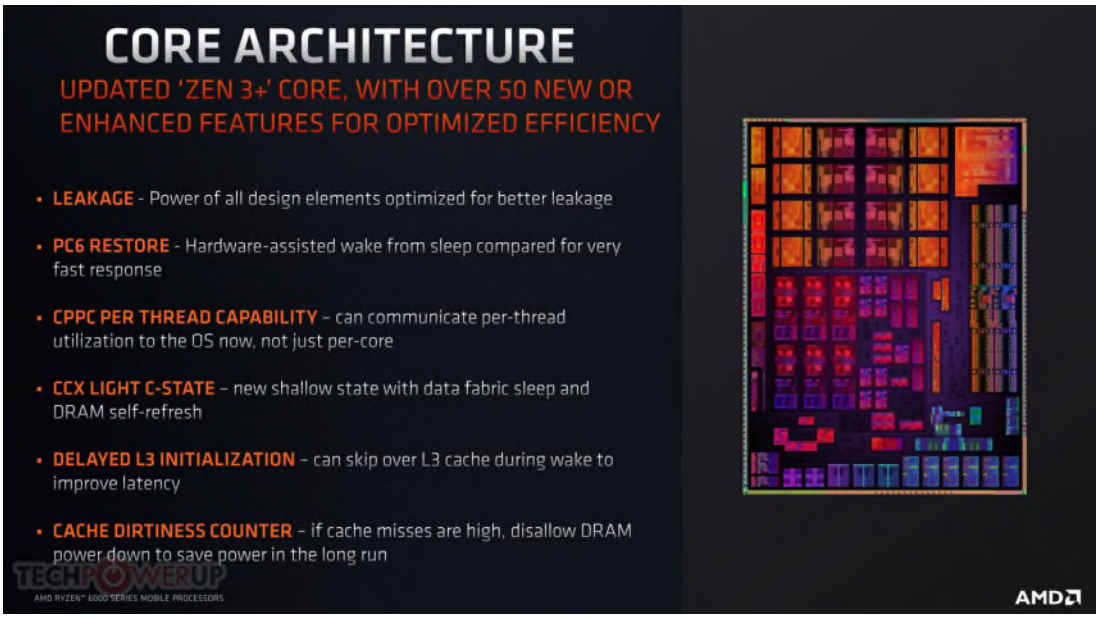
78. AMD describes Zen 3+ as featuring "5 layers of power optimization"[18] with layers it calls "core architecture," "SoC architecture," and "system software."



https://hc34.hotchips.org/assets/program/conference/day2/Mobile%20and%20Edge/AMD%20Ryzen%206000%20Series%20Processor%20-%20Hotchips34%20Final%2008222022.pdf.

[18] The capitalization of quoted language in paragraphs 78-97 has been modified to improve readability.

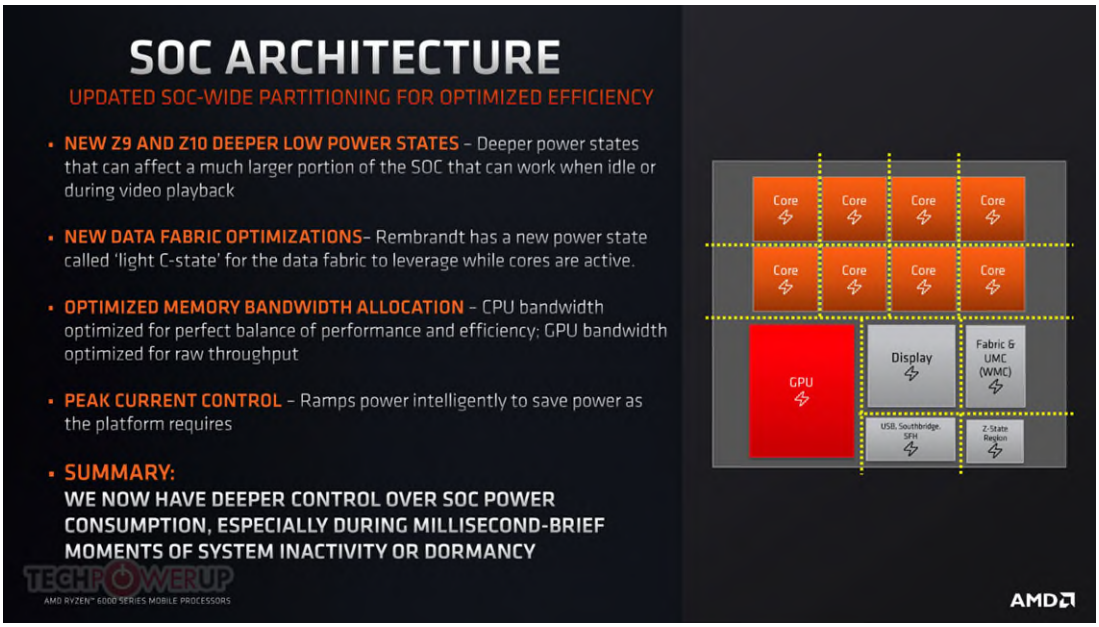
79. In connection with the "core architecture" layer, AMD states that Zen 3+ has "over 50 new or enhanced features for optimized efficiency." AMD claims that the "new 'Zen 3+' core" is "heavily optimized for performance per watt," and that "power of all design elements [is] ***optimized for better leakage***."[19]



https://www.techpowerup.com/292118/amd-zen3-architecture-and-ryzen-6000-rembrandt-mobile-processors-detailed.

80. Additionally, AMD claims that Zen 3+ provides "deeper control over SoC power consumption, especially during millisecond-brief moments of system inactivity or dormancy."

[19] https://www.techpowerup.com/292118/amd-zen3-architecture-and-ryzen-6000-rembrandt-mobile-processors-detailed (emphasis added).



https://www.techpowerup.com/292118/amd-zen3-architecture-and-ryzen-6000-rembrandt-mobile-processors-detailed.

81. AMD's Ryzen 6000 Series products (among other series of products in AMD's Ryzen line) are built with AMD's Zen 3+ microarchitecture. Advanced power management is one of the most heavily marketed benefits of AMD's Ryzen 6000 Series processors. For example, AMD boasts "in-depth power optimization" of the Ryzen 6000 Series processor lineup that implements Zen 3+ microarchitecture and calls the processor series "a leap ahead in power and efficiency." AMD states, "Starting with a new 6nm manufacturing process and enhanced microarchitecture ('Zen 3+' core) the entire AMD Ryzen 6000 Series processor lineup is designed to enable the best battery life for x86 Windows 11 notebooks without the typical application performance trade-offs."[20]

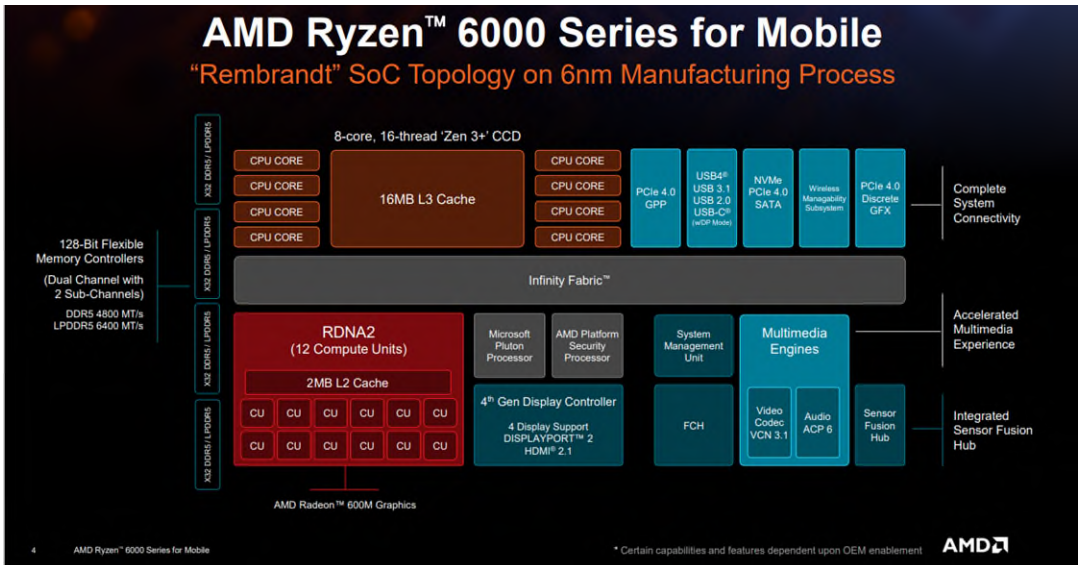
82. AMD also markets later generations of Zen microarchitecture as having advanced power management capabilities. For example, AMD states the following with respect to power management in EPYC 9004 and 8004 Series processors that feature Zen 4 microarchitecture: "We

[20] https://www.amd.com/en/partner/articles/ryzen-6000-series-mobile-processors.html.

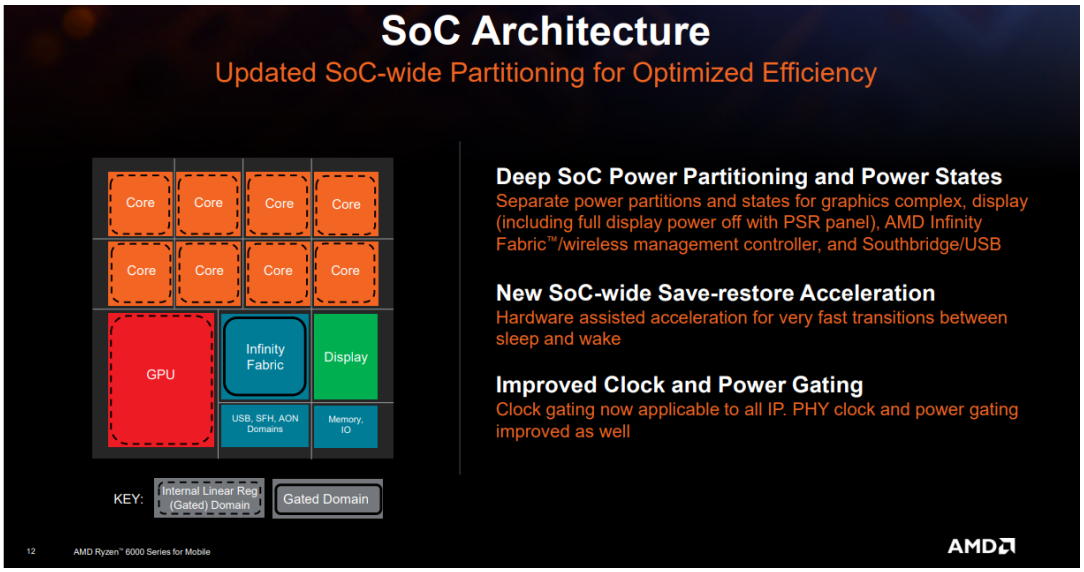
believe in providing all of the performance our CPUs are capable of delivering, ***even if it means taking advantage of the inherent variabilities between parts***."[21] AMD describes EPYC 9004 Series processors that implement Zen 4 microarchitecture as "performance without the energy Price Tag." AMD claims that these processors "improv[e] power efficiency measurably over previous generation and competitor products" and "prioritize low power usage, lower energy costs, and more performance output per server."[22] As yet another example, AMD states that EPYC 4005 Series processors based on the Zen 5 microarchitecture "[h]elp reduce your power consumption with CPU energy usage as low as 65W."[23]

83. The '850 Patent Infringing Products include a memory.

84. For example, AMD's Ryzen 6000 Series processors that incorporate Zen 3+ microarchitecture contain a memory.



[21] https://www.amd.com/content/dam/amd/en/documents/products/processors/server/epyc/epyc-8004-and-9004-series-cpu-power-management-white-paper.pdf at 7 (emphasis added).
[22] https://www.amd.com/en/partner/articles/4th-generation-amd-epyc.html.
[23] https://www.amd.com/content/dam/amd/en/documents/epyc-business-docs/other/5-reasons-why-amd-epyc-4005-series-processors.pdf.

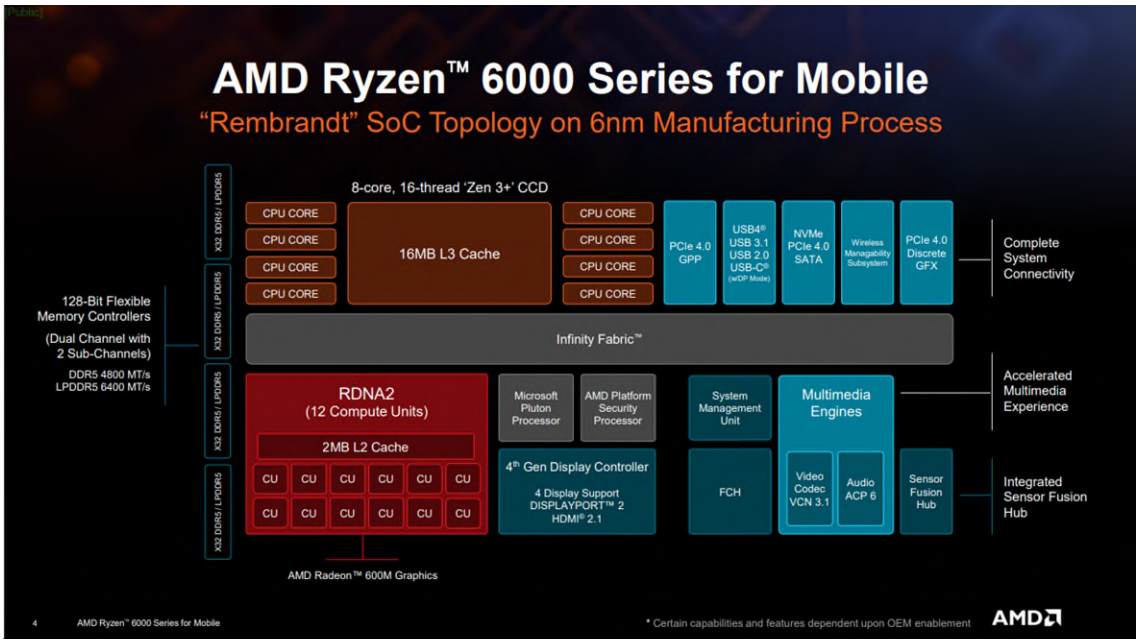


https://hc34.hotchips.org/assets/program/conference/day2/Mobile%20and%20Edge/AMD%20Ryzen%206000%20Series%20Processor%20-%20Hotchips34%20Final%2008222022.pdf.

85. The ’850 Patent Infringing Products include a processor coupled to the memory, wherein the processor includes one or more cores and is configured to execute a power management application in conjunction with one or more instructions stored in the memory.

86. For example, AMD’s Ryzen 6000 Series of products that feature Zen 3+ microarchitecture include at least one CCD, where each CCD contains one CCX containing eight cores.[24] The products additionally include a processor coupled to a memory and configured to execute a power management application in conjunction with one or more instructions stored in the memory.

[24] https://hc34.hotchips.org/assets/program/conference/day2/Mobile%20and%20Edge/AMD%20Ryzen%206000%20Series%20Processor%20-%20Hotchips34%20Final%2008222022.pdf; *see also supra* ¶ 45 (illustrating the configuration of CCDs in AMD’s EPYC 9005 Series processors with Zen 5 microarchitecture).



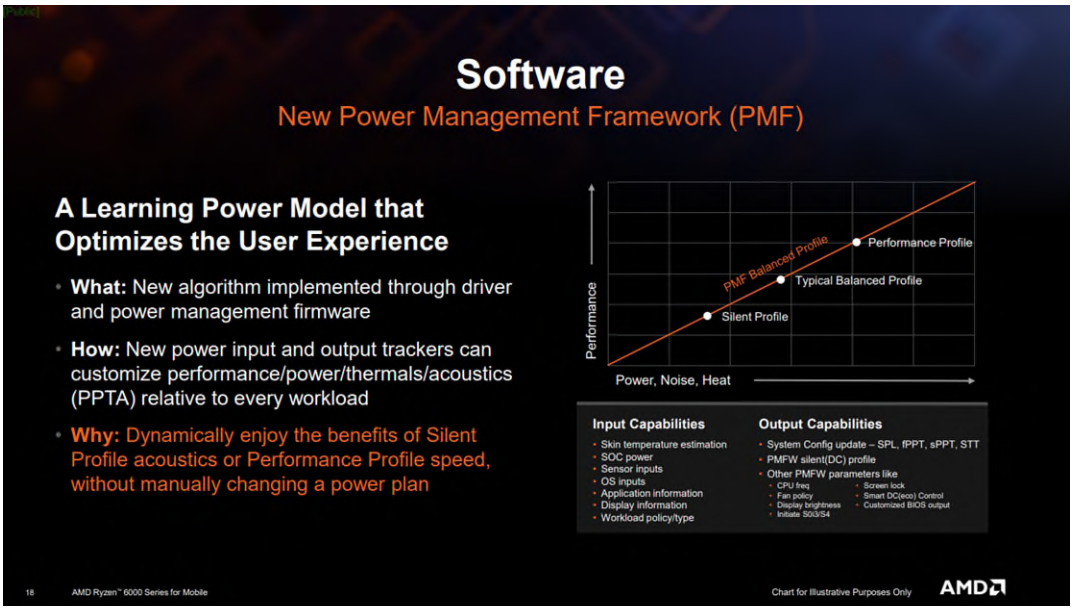
https://hc34.hotchips.org/assets/program/conference/day2/Mobile%20and%20Edge/AMD%20Ryzen%206000%20Series%20Processor%20-%20Hotchips34%20Final%2008222022.pdf.

87. The power management application of the '850 Patent Infringing Products is configured to receive computation data from a power controller and one or more processor instruction counters of one of the one or more cores of the processor.

88. In connection with the "core architecture" layer of the "power optimization" in Zen 3+, AMD states that Zen 3+ can "look at previous core utilization before waking some cores unnecessarily" and "trigger sleep if a core isn't being utilized." AMD also boasts "CPPC [Collaborative Processor Performance Control] per thread capability" that "can communicate per-thread utilization to the OS now, not just per-core." AMD also says the following with respect to Zen 3+: "We now have deeper control over every individual processing thread's power level and clock. This is how we secure more performance per watt from a single core complex."[25]

[25] https://hc34.hotchips.org/assets/program/conference/day2/Mobile%20and%20Edge/AMD%20Ryzen%206000%20Series%20Processor%20-%20Hotchips34%20Final%2008222022.pdf.

89. With respect to the "software" layer of the "power optimization in Zen 3+," AMD explains, "New power input and output trackers can customize performance/power/thermals/acoustics (PPTA) relative to every workload." AMD also specifies many other "input capabilities."



https://hc34.hotchips.org/assets/program/conference/day2/Mobile%20and%20Edge/AMD%20Ryzen%206000%20Series%20Processor%20-%20Hotchips34%20Final%2008222022.pdf.

90. As another example, AMD describes advanced power management capabilities in EPYC 9004 and 8004 Series processors with Zen 4 microarchitecture as follows:

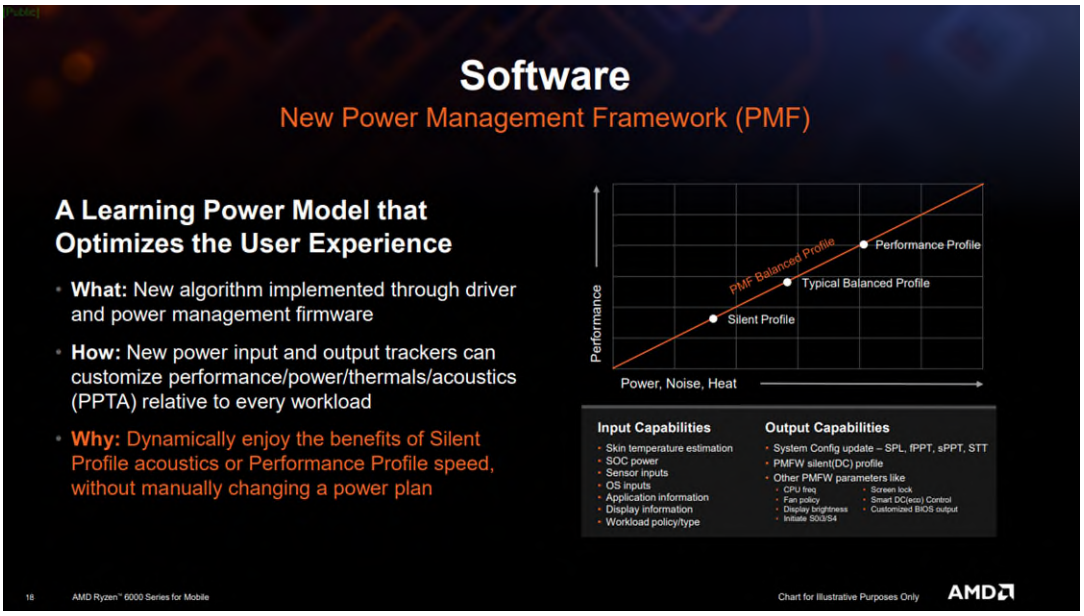
> The CPU's system management unit (SMU) resides on the processor's I/O die, where it manages power consumption for the entire system on chip. It has agents residing on each CPU die that can autonomously implement power policies set by the SMU across the CPU die or on a per-CPU-core basis. ***The SMU constantly integrates the telemetry it obtains from these agents*** and allocates power based on its real-time observations. ***New to the AMD EPYC 9004 and 8004 Series is the addition of directly observed thermals to the list of variables it manages, including performance, power, voltage, amperage, and core idle states.*** More power generally supports more performance, however the CPU also monitors current and voltage so it does not exceed the boundaries of the chip or the supporting infrastructure.
> …

> One of the principles on which the SMU is based is that its power management is entirely self-contained, and ***decisions are made using internal parameters*** while honoring external settings from the BIOS or operating system.
> …
> The determinism settings dictate which policies the SMU should use to manage the frequency of each core ***based on real-time input from the telemetry agents placed across the system on chip***. The SMU optimizes the variables of performance, power, voltage, current, thermals, and number of active cores to keep each variable within bounds.

https://www.amd.com/content/dam/amd/en/documents/products/processors/server/epyc/epyc-8004-and-9004-series-cpu-power-management-white-paper.pdf at 4-5 (emphasis added).

91. The power management application of the ’850 Patent Infringing Products is configured to generate a table of linear combination samples from the computation data, wherein the one or more instructions are grouped based on one or more sub-units of a selected core associated with each one of the one or more instructions, and wherein each of the linear combination samples include a power usage value for a sub-unit of the selected core. It is further configured to generate a micro-architectural leakage map of the selected core from the linear combination samples within the table.

92. With respect to the “software” layer of the “power optimization in Zen 3+,” AMD explains, “New power input and output trackers can customize performance/power/thermals/acoustics (PPTA) relative to every workload.” AMD boasts “a learning power model that optimizes the user experience,” with a “new algorithm implemented through driver and power management firmware.”



https://hc34.hotchips.org/assets/program/conference/day2/Mobile%20and%20Edge/AMD%20Ryzen%206000%20Series%20Processor%20-%20Hotchips34%20Final%2008222022.pdf.

93. As another example, AMD describes power management in EPYC 9004 and 8004 Series processors with Zen 4 microarchitecture as follows:

> The CPU's system management unit (SMU) resides on the processor's I/O die, where it manages power consumption for the entire system on chip. ***It has agents residing on each CPU die that can autonomously implement power policies set by the SMU across the CPU die or on a per-CPU-core basis.*** The SMU constantly integrates the telemetry it obtains from these agents and allocates power based on its real-time observations. ***New to the AMD EPYC 9004 and 8004 Series is the addition of directly observed thermals to the list of variables it manages, including performance, power, voltage, amperage, and core idle states.*** More power generally supports more performance, however the CPU also monitors current and voltage so it does not exceed the boundaries of the chip or the supporting infrastructure.

https://www.amd.com/content/dam/amd/en/documents/products/processors/server/epyc/epyc-8004-and-9004-series-cpu-power-management-white-paper.pdf at 5 (emphasis added).

94. The power management application of the '850 Patent Infringing Products is configured to, in response to detection that a second sub-unit being deactivated based on the micro-architectural leakage map, direct a thread of a subset of the one or more instructions to a first sub-

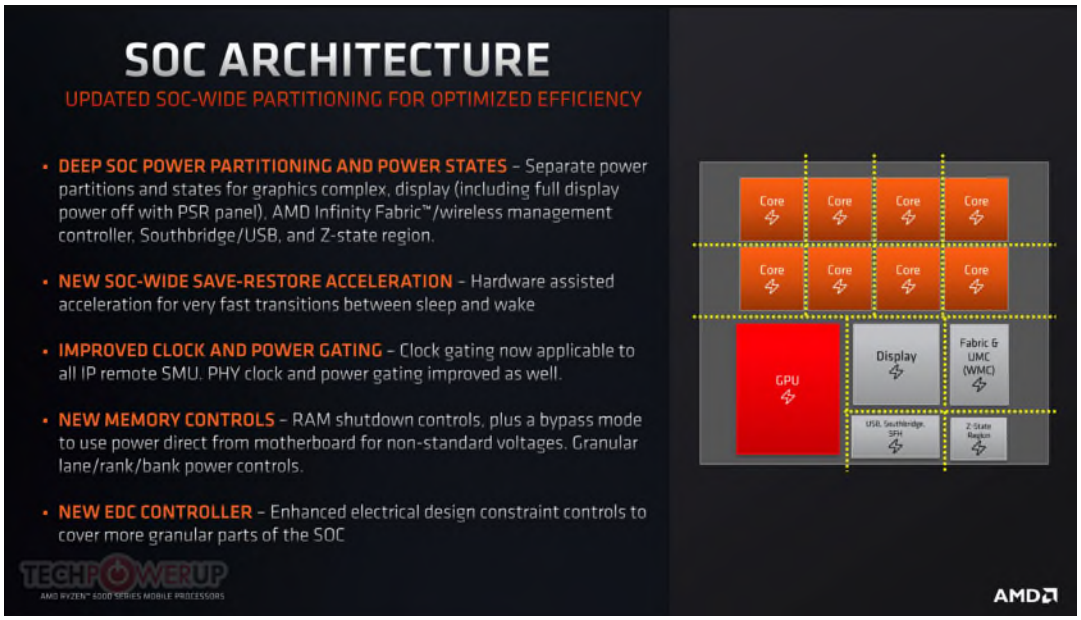
unit. In response to detection that the first sub-unit is unable to compensate the deactivation of the second sub-unit, the application is configured to reactivate the second sub-unit. The application is also configured to execute a thread migration operation to move the thread from the first sub-unit to the second sub-unit, the thread to be executed by the second sub-unit. In response to a completion of an execution of the thread, the application is configured to move the thread back to the first sub-unit and deactivate the second sub-unit.

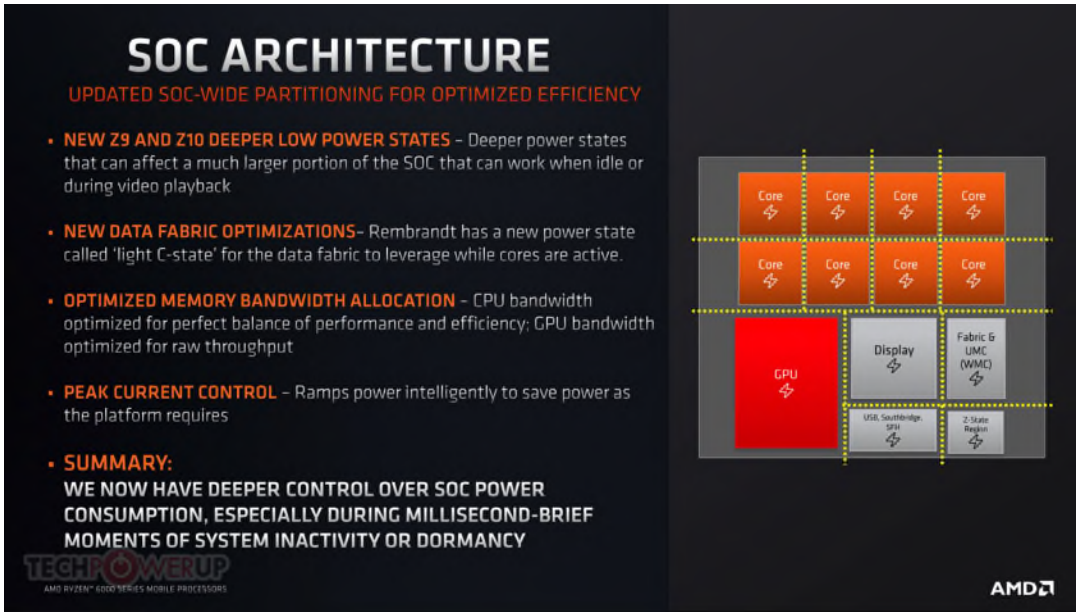
95. AMD describes the "core architecture" layer of the "power optimization" in Zen 3+ as featuring "selective SCFCTP save," which it describes as follows: "On PC6 entry – look at previous core utilization before waking some cores unnecessarily." AMD further describes the "core architecture" layer as featuring an "enhanced CC1 state," which AMD describes as a "new way to trigger sleep if a core isn't being utilized."[26]

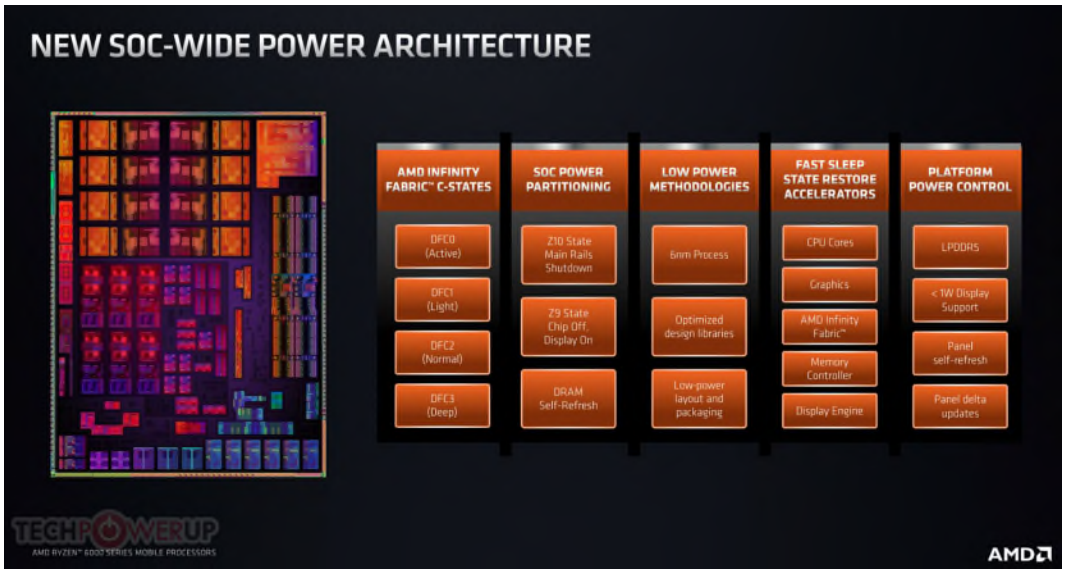
96. The "SoC architecture" layer of the "power optimization" in AMD's Zen 3+ includes the following features:

- "Updated SoC-wide partitioning for optimized efficiency";
- "Deep SoC power partitioning and power states – separate power partitions and states for graphics complex, display . . . AMD Infinity Fabric/wireless management controller . . . .";
- "New SoC-wide save-restore acceleration – hardware assisted acceleration for very fast transitions between sleep and wake"';
- "Fast sleep state restore accelerators" including for "CPU cores";
- "New EDC controller – enhanced electrical design constraint controls to cover more granular parts of the SoC";
- "Peak current control - ramps power intelligently to save power as the platform requires."

[26] https://hc34.hotchips.org/assets/program/conference/day2/Mobile%20and%20Edge/AMD%20Ryzen%206000%20Series%20Processor%20-%20Hotchips34%20Final%2008222022.pdf.


SOC ARCHITECTURE
UPDATED SOC-WIDE PARTITIONING FOR OPTIMIZED EFFICIENCY
• DEEP SOC POWER PARTITIONING AND POWER STATES – Separate power partitions and states for graphics complex, display (including full display power off with PSR panel), AMD Infinity Fabric™/wireless management controller, Southbridge/USB, and Z-state region.
• NEW SOC-WIDE SAVE-RESTORE ACCELERATION – Hardware assisted acceleration for very fast transitions between sleep and wake
• IMPROVED CLOCK AND POWER GATING – Clock gating now applicable to all IP remote SMU. PHY clock and power gating improved as well.
• NEW MEMORY CONTROLS – RAM shutdown controls, plus a bypass mode to use power direct from motherboard for non-standard voltages. Granular lane/rank/bank power controls.
• NEW EDC CONTROLLER – Enhanced electrical design constraint controls to cover more granular parts of the SOC
Core
Core
Core
Core
Core
Core
Core
Core
GPU
Display
Fabric & UMC (WMC)
AMD

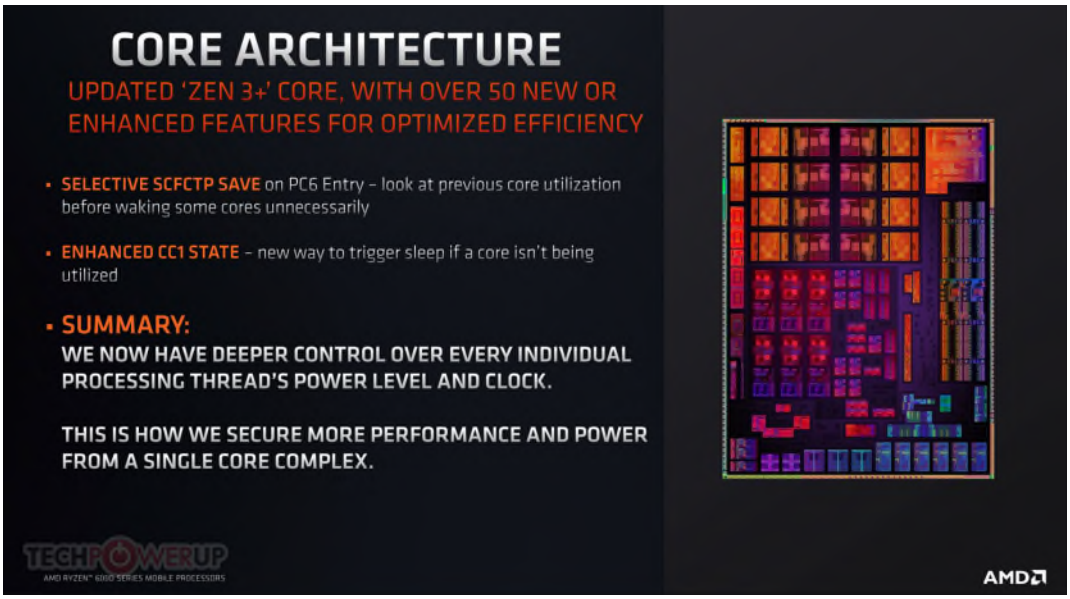

SOC ARCHITECTURE
UPDATED SOC-WIDE PARTITIONING FOR OPTIMIZED EFFICIENCY
• NEW Z9 AND Z10 DEEPER LOW POWER STATES – Deeper power states that can affect a much larger portion of the SOC that can work when idle or during video playback
• NEW DATA FABRIC OPTIMIZATIONS– Rembrandt has a new power state called 'light C-state' for the data fabric to leverage while cores are active.
• OPTIMIZED MEMORY BANDWIDTH ALLOCATION – CPU bandwidth optimized for perfect balance of performance and efficiency; GPU bandwidth optimized for raw throughput
• PEAK CURRENT CONTROL – Ramps power intelligently to save power as the platform requires
• SUMMARY:
WE NOW HAVE DEEPER CONTROL OVER SOC POWER CONSUMPTION, ESPECIALLY DURING MILLISECOND-BRIEF MOMENTS OF SYSTEM INACTIVITY OR DORMANCY
Core
Core
Core
Core
Core
Core
Core
Core
GPU
Display
Fabric & UMC (WMC)
AMD



https://www.techpowerup.com/292118/amd-zen3-architecture-and-ryzen-6000-rembrandt-mobile-processors-detailed.

97. AMD states that Zen 3+ "has even deeper control over every processing thread's power level and clock speed."[27] For example, "CPPC per thread capability . . . can communicate per-thread utilization to the OS now, not just per-core." AMD also states, "We now have deeper control over every individual processing thread's power level and clock. This is how we secure more performance and power from a single core complex."[28]

[27] https://www.amd.com/en/partner/articles/ryzen-6000-series-mobile-processors.html.
[28] https://www.techpowerup.com/292118/amd-zen3-architecture-and-ryzen-6000-rembrandt-mobile-processors-detailed.



https://www.techpowerup.com/292118/amd-zen3-architecture-and-ryzen-6000-rembrandt-mobile-processors-detailed.

98. AMD incorporates simultaneous multithreading ("SMT") technology in its Zen 3+ microarchitectures and later Zen generations. SMT allows a core to execute two threads simultaneously. In other words, multiple threads can run on the same core at the same time. As a result, "a second thread [can] use shared core resources while the other thread is stalled or otherwise awaiting data." Furthermore, Zen 3+ allows for the reassignment of threads.[29]

99. While the foregoing analysis of claim 12 has focused primarily on Zen 3+, AMD's products incorporating later-released microarchitectures, including Zen 4 and Zen 5, practice claim 12 through similar means.

100. At least since receiving notice of this Complaint, AMD's infringement of the '850 Patent is willful.

[29] https://www.amd.com/en/blogs/2025/simultaneous-multithreading-driving-performance-a.html.

101. Without permission from or compensation to Empire, AMD has sold—and continues to sell—very substantial numbers of ’850 Patent Infringing Products in the U.S. based on the pioneering technology in the ’850 Patent.

102. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the ’850 Patent. Empire has satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law for the infringement of the ’850 Patent.

103. As a result of AMD’s infringement of the ’850 Patent, Empire has suffered monetary damages, and seeks recovery in an amount adequate to compensate for AMD’s infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

PRAYER FOR RELIEF

WHEREFORE, Empire prays for a judgment in its favor and against AMD and respectfully requests the following relief:

A. A judgment in favor of Empire that AMD infringes, either literally or under the doctrine of equivalents, the ’370 and ’850 Patents;

B. Damages for infringement of the ’370 and ’850 Patents in an amount to be determined at trial;

C. For other monetary relief, including costs, expenses, and pre- and post-judgment interest;

D. An order pursuant to 35 U.S.C. § 283 enjoining AMD, its officers, directors, agents, servants, employees, attorneys, and those persons in active concert or participation with them, from further acts of infringement of the ’370 and ’850 Patents;

E. A determination that AMD's infringement of the '370 and '850 Patents is willful, and an award of enhanced damages, up to and including trebling of the damages awarded to Empire under 35 U.S.C. § 284;

F. A determination that this is an exceptional case under 35 U.S.C. § 285 and an award of attorneys' fees and costs to Empire;

G. An order awarding Empire any such other relief as the Court may deem just and proper under the circumstances.

JURY DEMAND

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, Empire hereby demands a jury trial as to all issues so triable.

Respectfully submitted,

POTTER ANDERSON & CORROON LLP

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Dated: August 21, 2025