**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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Silicon Motion Inc.

Petitioner,

v.

K.Mizra, LLC

Patent Owner.

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Case No. IPR2024-01241
U.S. Patent No. 9,111,608

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# PETITION FOR *INTER PARTES* REVIEW OF CLAIMS 1-2, 4-15 OF U.S. PATENT NO. 9,111,608

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| 1002 | Prosecution History of U.S. Pat. No. 9,111,608 B2. |
| 1003 | Declaration of R. Jacob Baker, Ph.D., P.E., Regarding U.S. Patent No. 11,640,359. |
| 1004 | U.S. Pat. No. 6,434,081, entitled "CALIBRATION TECHNIQUE FOR MEMORY DEVICES", to Johnson, et al. ("Johnson"). |
| 1005 | U.S. Pub. No. 2003/0099135 A1, entitled "PER-BIT SET-UP AND HOLD TIME ADJUSTMENT FOR DOUBLE-DATA RATE SYNCHRONOUS DRAM," to Stubbs ("Stubbs"). |
| 1006 | U.S. Pat. No. 6,646,929 B1, entitled "METHODS AND STRUCTURE FOR READ DATA SYNCHRONIZATION WITH MINIMAL LATENTCY," to Moss et al. ("Moss"). |
| 1007 | U.S. Pub. No. 2003/0179611 A1, entitled "METHOD AND DEVICE FOR CONTROLLING DATA LATCH TIME", to Liou ("Liou") |

## Claims Appendix

| # | Limitation Text |
|---|---|
| 1[pre] | An integrated circuit (IC) memory controller comprising: |
| 1[a] | a first pin to receive a first data signal; a first adjustable delay element to delay the received first data signal and generate a first delayed data signal; |
| 1[b] | a second pin to receive a second data signal; a second adjustable delay element to delay the received second data signal and generate a second delayed data signal; |
| 1[c] | a pin to receive a strobe signal; |
| 1[d] | a first sampling circuit to sample the first delayed data signal based on the strobe signal; and |
| 1[e] | a second sampling circuit to sample the second delayed data signal based on the received strobe signal. |
| 2 | The IC memory controller according to claim 1, further comprising storage to store each of first and second delay values corresponding to the delays imparted to the first and second data signals. |
| 4 | The IC memory controller according to claim 1, wherein the first and second data signals are delayed to compensate for timing offset between the received first and second data signals. |
| 5 | The IC memory controller according to claim 4, further comprising: a first timing signal delay element associated with the first pin; and a second timing signal delay element associated with the second pin; wherein each of the first and second timing signal delay elements impart first and second delays to the strobe signal. |
| 6 | The IC memory controller according to claim 1, wherein: each of the first and second delay elements comprise locked-loop circuits having plural serially connected delay elements. |
| 7 | The IC memory controller according to claim 6, wherein the first delay value is used to select delay elements of the first delay circuit and the second delay value is used to select delay elements of the second delay circuit. |
| 8 | The IC memory controller according to claim 1, further comprising a calibration strobe delay element to impart a calibrated delay to the strobe signal. |
| 9 | The IC memory controller according to claim 1, further comprising a calibration circuit to, in a calibration mode, determine the first and second delay values. |

| | |
|---|---|
| 10[pre] | A method of operation in an IC memory controller, the method comprising: |
| 10[a] | receiving first and second data signals from a memory device at respective first and second pins; |
| 10[b] | aligning the received first and second data signals with a strobe signal, the aligning comprising imparting a first delay to the first data signal, the first delay corresponding to a first delay value, imparting a second delay to the second data signal, the second delay corresponding to a second delay value. |
| 11 | The method according to claim 10, further comprising: in a calibration mode, determining the first and second delay values; and storing the first and second delay values. |
| 12 | The method according to claim 11, wherein: during the receiving mode, the imparting the first and second delays includes retrieving the stored first and second delay values. |
| 13 | The method according to claim 12, wherein: the first and second data signals are delayed by the first and second delay values. |
| 14 | The method according to claim 11, further comprising: during the calibration mode, calibrating a timing signal delay value corresponding to a delay for application to the strobe signal. |
| 15 | The method according to claim 14, further comprising: during the calibration mode, storing the calibrated timing delay value. |

## I. Introduction

U.S. Patent 9,111,608 (the "'608 Patent") is invalid. The '608 Patent purports to claim systems and methods for calibrating a memory controller for use with double data rate dynamic random access memory (DDR DRAM). The '608 Patent claims that there was a need "for per-pin (data bit) strobe-offset control and timing calibration to minimize . . . timing offsets for each [data] pin individually." (EX1001, at 2:21-25). But per-pin calibration was already well-known in the art as of the August 20, 2004 priority date. Indeed, numerous prior art references, including those described in this Petition, illustrate per-pin calibration techniques, which they recognize as prior art methods with problems that they aim to overcome.

Further, the claims of the '608 Patent were issued without any substantive rejections by the USPTO, suggesting that the claims were not fully vetted during prosecution. This is apparent in the structure of the claims themselves, which merely claim performing calibration of two pins individually, with no limitations describing how such calibration occurs. Nor are any novel or non-obvious calibration methods specifically claimed. The dependent claims merely add obviously inherent elements of any practical application of a memory controller in DDR DRAM memory. In view of the '608 Patent's attempts to lay claim merely to the concept of per-pin calibration – a technique well known in the art – the Board should hold each challenged claim invalid.

## II. Mandatory Notices under 37 C.F.R. § 42.8

### A. Real Party in Interest

Petitioner Silicon Motion Inc. is the real party-in-interest. In the litigation identified below, Patent Owner added infringement claims against Silicon Motion Technology Corporation on July 26, 2024. Patent Owner has further alleged that Silicon Motion, Inc. a California corporation ("SM-US"), is an agent or alter ego of Petitioner, which Petitioner disputes. Petitioner's immediate parent company is Silicon Motion Technology (Hong Kong) Limited ("SMHK"). Solely out of an abundance of caution, Petitioner identifies these three related entities as real parties-in-interest, but Petitioner maintains that these entities do not satisfy the legal criteria for being real parties-in-interest. Neither SM-US nor SMHK have been sued by Patent Owner.

### B. Related Matters

The following judicial or administrative matters may be affected by a decision in this proceeding:

- *K.Mizra LLC v. Silicon Motion Inc.*, No. 2:24-cv-00101 (E.D. Tex. Feb. 15, 2024) ("District Court Litigation").
- U.S. Patent Application 18/094,895, which claims priority to the application issued as the '608 Patent.

### C. Designation of Lead and Back-Up Counsel

Petitioner appoints the following as lead and backup counsel:

| LEAD COUNSEL | BACK-UP COUNSEL |
|---|---|
| Jeffrey Johnson<br>**BAKER BOTTS L.L.P.**<br>910 Louisiana Street<br>Houston, TX 77002<br>Phone: (713) 229-1222<br>Fax: (713) 229-7922<br>Jeffrey.Johnson@bakerbotts.com<br>USPTO Reg. No. 53,078 | Parker Hancock<br>**BAKER BOTTS L.L.P.**<br>910 Louisiana Street<br>Houston, TX 77002<br>Phone: (713) 229-11196<br>Fax: (713) 229-2896<br>Parker.Hancock@bakerbotts.com<br>USPTO Reg. No. 73,667<br><br>Robert Benson<br>(Pro hac vice forthcoming)<br>**BAKER BOTTS L.L.P.**<br>101 California Street, Suite 3200<br>San Francisco, CA 94111<br>Phone: (415) 291-6285<br>Fax: (415) 291-6385<br>Robert.Benson@bakerbotts.com |

### D. Service Information

Petitioners consent to electronic service at DLSiliconIPR608@bakerbotts.com. A Power of Attorney is filed concurrently herewith under 37 C.F.R. § 42.10(b).

### E. Payment of Fees – 37 C.F.R. § 42.103

Silicon Motion authorizes the USPTO to charge Deposit Account No. 02-0384 for the fee set forth in 37 C.F.R. § 42.15(a) for this Petition and further authorizes payment for any additional fees to be charged to this deposit account.

## III. Petitioner Meets Standing and Eligibility Requirements for *Inter Partes* Review.

Petitioner certifies under 37 C.F.R. § 42.104(a) that the '608 Patent "is available for *inter partes* review and that the Petitioner is not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in the petition." Patent Owner sued Petitioner and other real parties in interest less than one year ago, on February 15, 2024.

## IV. Background

The '608 Patent is directed to the field of double-data rate dynamic random access memory (DDR DRAM). (EX1001, EX1003, ¶30). DDR DRAM systems are memory devices used in computer systems as a form of high-speed read/write volatile memory. (EX1003, ¶30). The "double data rate" refers to the fact that DDR DRAM systems can read and write data on both the rising and falling edges of a system clock signal, and thus can transfer data at double the system clock speed. (EX1003, ¶30). In read-and-write operations, DDR DRAM systems use a "data clock" or "strobe signal," sometimes referred to as DQS or DCLK, to indicate when data on various pins should be read. . (EX1003, ¶30).

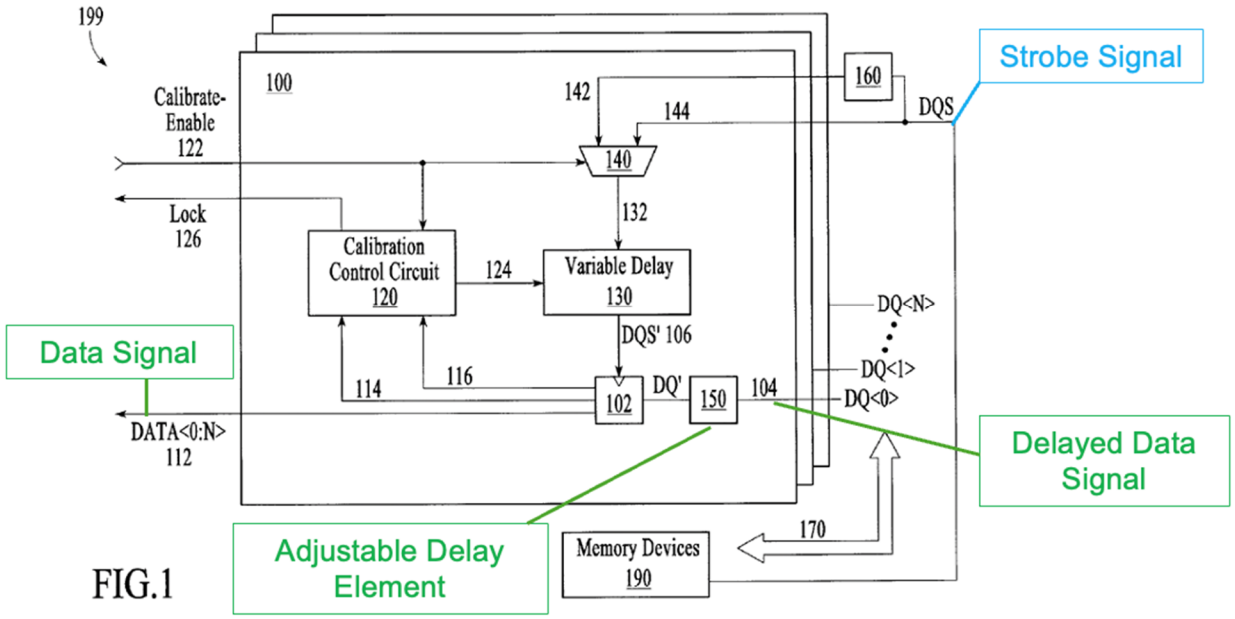
A known problem with such systems is that propagation delay caused by the physical path between the data and the strobe signal can cause a misalignment between the data present on a specific pin and the strobe signal. (EX1003, ¶30). Thus, it was known in the art to insert delay elements between the strobe signal and/or the data pin and to calibrate these delay elements to ensure the strobe signal data signals are aligned. (EX1003, ¶32).

Adjustable delay elements, such as delay-locked loop (DLL) devices, were also well-known at the time of the alleged invention of the ’608 patent. (EX1003, ¶31). DLL devices contain a chain of serially connected delay elements that introduce controllable delays into an output signal, each delay element creating a delayed version of the input signal. (EX1003, ¶31). The device also includes a phase detector that compares the phase difference between a reference signal and the delayed output signal, producing an error signal. (EX1003, ¶31). It was well-known at the time of the invention of the ’608 Patent that DLLs could be used as delay elements to solve the problem of misaligned data and strobe signals caused by propagation delay. (EX1003, ¶31).

Further, at the time of the alleged invention, it was well-known that calibration of data paths in a memory controller could be performed on a per-bit, half-byte (4 bits), per-byte (8 bits), or per-word (16 bits) basis. (EX1003, ¶34).

## V. Summary of the '608 Patent

The '608 Patent is directed to alleged improvements in memory controllers using delay elements to ensure alignment between data and strobe signals. (EX1001, at 3:16-34, EX1003, ¶38). The '608 Patent purports to solve problems related to propagation delay by providing systems and methods for automatically calibrating the strobe delay on a per-bit basis, rather than on a per-byte basis. (Id.) Figure 1 illustrates an embodiment:




(EX1001, Fig 1 (annotated excerpt)).

The issued claims of the '608 Patent recite only a few components. (EX1003, ¶¶38-40). Independent Claim 1 recites two data pathways, each comprising a pin to receive a data signal, an adjustable delay element to delay the data signal, and a sampling circuit that samples the delayed data signal. (EX1003, ¶38). Claim 1 also

recites a pin to receive a strobe signal, and the sampling circuits of the two data pathways sample the delayed data signal based on that strobe signal. (EX1003, ¶¶38-40). Independent claim 10 and dependent claim 9 recite aligning two data pathways, each pathway including a data pin, and aligning them by imparting a delay to each data line. (EX1003, ¶41).

The remaining claims likewise recite only generic components or merely describe the purpose of elements already disclosed. (EX1003, ¶42). Dependent claims 2, 11, and 12 merely recite storage and retrieval of delay values for the first and second pins. (EX1003, ¶43). Dependent Claim 4 merely recites the purpose of the claimed invention, namely, that the delays applied to the first and second pins are to "compensate for timing offset between the received first and second data signals." (EX1003, ¶44). Claim 5 merely recites that each data pin likewise has a "timing signal delay element" associated with that pin to delay the strobe signal provided to each. (EX1003, ¶45). Claims 6 and 7 merely recite the use of a well-known delay-locked loop device as the delay devices in each of the data paths. (EX1003, ¶46). Claims 8, 14, and 15 recite the use of a "calibrated delay" applied to a data strobe signal during calibration. (EX1003, ¶47).

Finally, claim 13 (which is indefinite) recites delaying the data signals by a delay value. (EX1003, ¶56). Claim 13 is indefinite because its antecedent claim 10 recites that the actual delay imparted to the data signal "correspond[s] to" the actual

delay value. (Id.). This would make sense to a POSITA, because such delay values are likely control signals or voltages applied to the delay element. (Id.). However, Claim 13 recites delaying the signals "by" the "first and second delay values." Such a claim makes no sense, because delays are measured in seconds, whereas the delay values are voltages or signals. (Id.). Nonetheless, if it is assumed that Claim 13 were rewritten to recite that the data signals are "delayed by a delay corresponding to the first and second delay values," the claim is still invalid as it merely recites the basic functioning of the device claimed in Claim 10. (Id.).

### A. Effective Filing Date and Date of Invention

The '608 Patent claims priority through a chain of continuation applications back to Application No. 10/923,421, filed on August 20, 2004. EX1001, cover. Solely for the purposes of this IPR, Petitioner assumes, but does not concede, an effective filing date of August 20, 2004 for the '608 Patent. Pre-AIA 35 U.S.C. §§ 102 and 103 apply.

### B. Prosecution History of the '608 Patent

The application, which was issued as the '608 Patent, was filed on March 31, 2014. (EX1002, 140). In a Preliminary Amendment filed on May 1, 2014, the Applicant amended the claims to strip out numerous substantive limitations. (EX1002, 59-63). The application, with the amended claims, was allowed on April

16, 2015, without receiving any substantive rejections from the Examiner. (EX1002, 17-23).

### C. Level or Ordinary Skill in the Art

A POSITA, as of August 20, 2004, would have at least a Bachelor's degree in Electrical Engineering, Computer Engineering, or a related field, and 2-3 years of experience in memory system design. (EX1003, ¶ 26-29). Alternatively, a POSITA could have a Master's degree in one of those fields and 1-2 years of relevant experience. (EX1003, ¶¶26-29).

## VI. Claim Construction

The Board construes claims under the same construction standard as civil actions in federal district court. Petitioner asserts that no construction is necessary for any terms for the purposes of this Petition as the challenged claims are invalid under any reasonable construction.

Nonetheless, and to avoid any unnecessary disputes, Petitioner proposes that the term "pin" carry its plain and ordinary meaning as would be understood by a person of ordinary skill, which is simply a "signal path." (EX1003, ¶¶52-55). This understanding is consistent with how that term is used in the '908 Patent, which refers to "pin-to-pin offsets in the DRAM," by which it simply refers to data traveling on a signal path. (EX1004, at 1:63-66, EX1003, ¶¶52-55).

Further, Claim 13 is indefinite, and no reasonable construction can save that claim from indefiniteness. (EX1003, ¶¶ 56-57). Claim 13 recites that "the first and second data signals are delayed by the first and second delay values." (EX1003, ¶¶ 56-67). But this does not make sense, as would have been appreciated by a POSITA. (EX1003, ¶¶ 56-67). In digital systems, delay values are typically represented as control signals or voltages that are applied to delay elements (EX1003, ¶¶ 56-67). But delays are measured in terms of seconds or fractions thereof. (EX1003, ¶¶ 56-67). These control signals or voltages instruct the delay elements on how much delay to introduce, but they are not the delays themselves, which are measured in seconds. (EX1003, ¶¶ 56-67).

Even if it were assumed that Claim 13 was rewritten to recite that the data signals are "delayed by a delay corresponding to the first and second delay values," the claim is still invalid as it merely recites the basic functioning of the device claimed in Claim 10, and thus adds no further limitation to that claim. (EX1003, ¶ 57). Nonetheless, solely for the purposes of this Petition, Petitioner assumes that Claim 13 is so rewritten.

## VII. Relief Requested

### A. Proposed Grounds

#### a. Ground 1

Claims 1-2, 4-7, and 9-15 are invalid under 35 U.S.C. § 103 over Johnson (EX1004) in view of Moss (EX1006).

**b. Ground 2**

Claim 8 is invalid under 35 U.S.C. § 103 over Johnson (EX1004), in view of Moss (EX1006), in further view of Liou (EX1007).

**c. Ground 3**

Claims 1-2, 4-7, and 9-15 are invalid under 35 U.S.C. § 103 over Stubbs (EX1005), in view of Moss (EX1006).

**d. Ground 4**

Claim 8 is invalid under 35 U.S.C § 103 over Stubbs (EX1005), in view of Moss (EX1006), in further view of Liou (EX1007).

**e. Ground 5**

Claims 10-12 are invalid under 35 U.S.C. § 103 over Stubbs (EX1005), in view of Moss (EX1006), in further view of Johnson (EX1004).

## B. Qualifying Prior Art

The references relied upon in the grounds above qualify as prior:

| Prior Art Reference | Filing Date | Publication / Issue Date | Applicable Section of 35 U.S.C. § 102 |
|---|---|---|---|
| U.S. Patent 6,434,081 to Johnson et al. ("Johnson", EX1004) | May 12, 2000 | Aug. 13, 2002 | (b) and (e) |
| U.S. Pub. 2003/0099135 to Stubbs ("Stubbs", EX1005) | Nov. 26, 2001 | May 29, 2003 | (b) and (e) |

| | | | |
|---|---|---|---|
| U.S. Patent 6,646,929 to Moss et al. ("Moss", EX1006) | Dec. 5, 2001 | Nov. 11, 2003 | (b) and (e) |
| U.S. Pub. 2003/0179611 to Liou ("Liou", EX1007) | Dec. 26, 2002 | Sept. 25, 2003 | (e) |

## VIII. The Prior Art

### A. Summary of Johnson

U.S. Patent 6,434,081, entitled "Calibration Technique for Memory Devices," to Johnson et al. ("Johnson")(EX1004) discloses systems and methods for calibrating data paths in a DDR DRAM memory device. (EX1003, ¶58; EX1004, Abstract, 1:11-2:2). Johnson discloses an improvement in existing calibration methods that ensures the synchronization of per-bit calibration across various data pins. (EX1004, ¶58; EX1004, at 2:3-14). That is, Johnson recognizes the existence of per-bit calibration techniques and solves a problem that can be created in such systems. Fig. 4 illustrates the system described in Johnson:

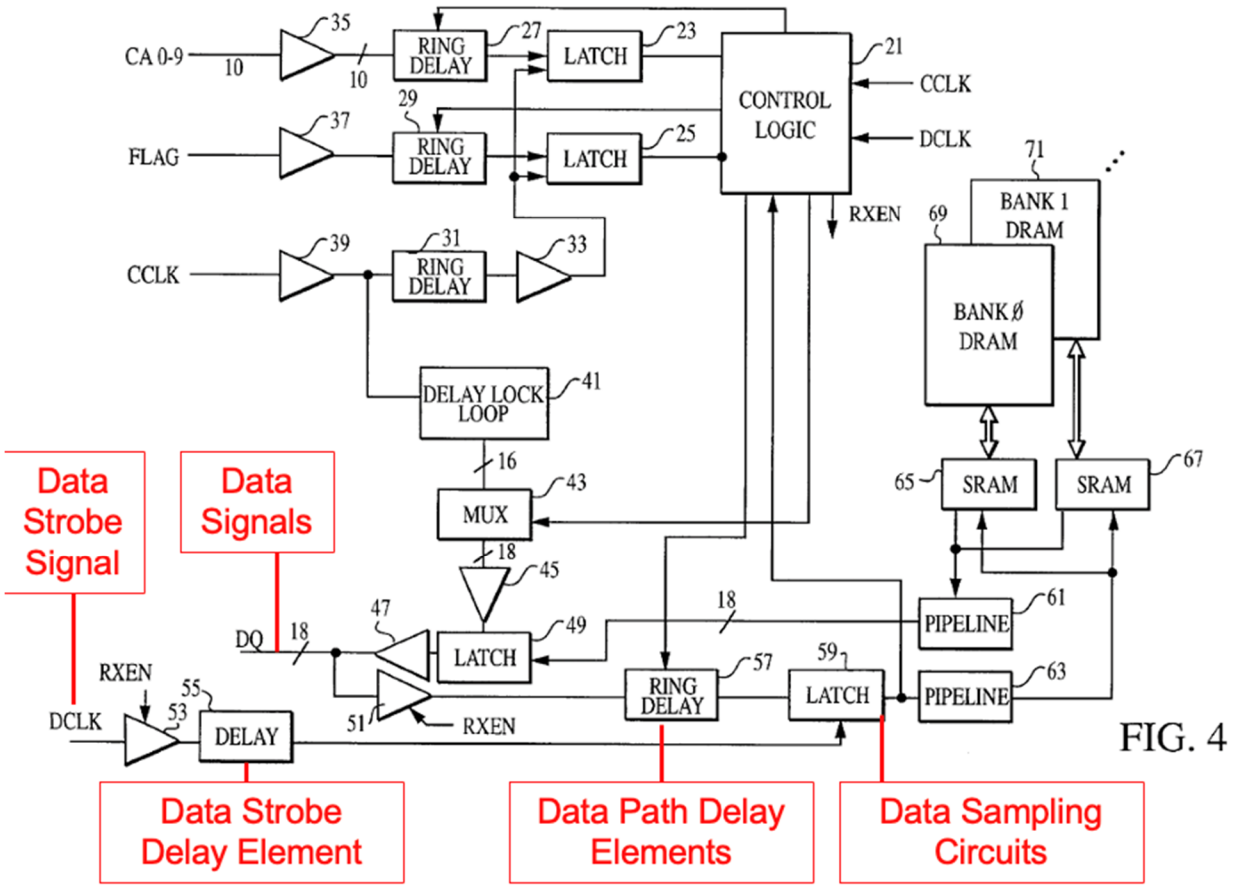
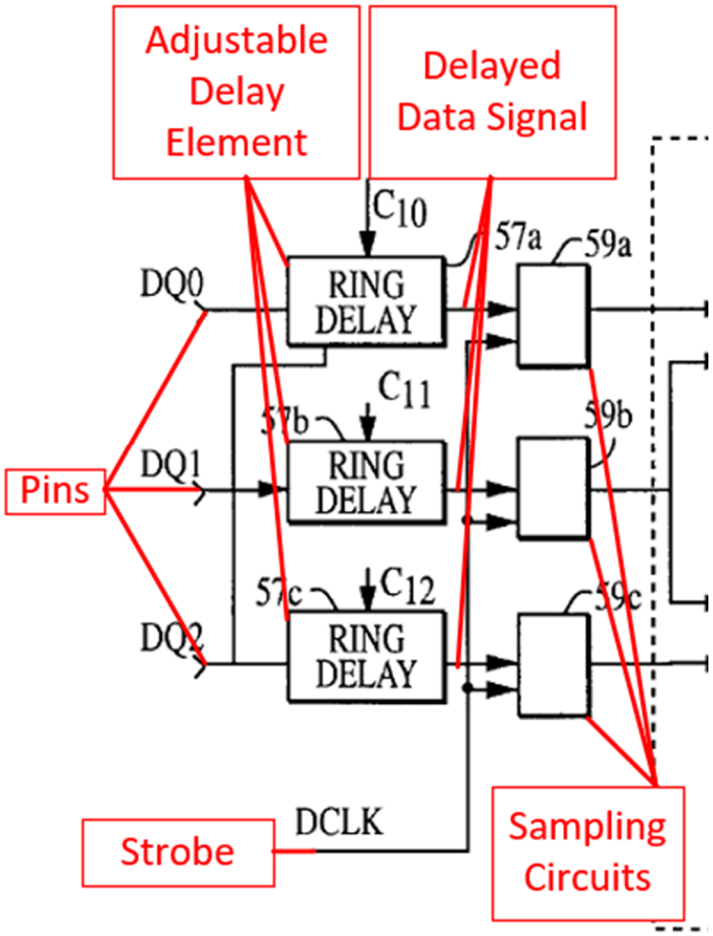



FIG. 4

(EX1004, ¶59; EX1004, Fig. 4 (annotated excerpt)). Johnson describes that "[d]ata which is to be input into memory banks 69, 71" passes "through ring delays 57 on each path of the data bus, into latches 59." (EX1004, ¶¶60-62; EX1004, 4:12-19).

Johnson further discusses improvements to the per-bit calibration system shown in Fig. 4. (EX1003, ¶63). An example embodiment is shown in Fig. 10:




(EX1004, at Fig. 10 (annotated excerpt)). Pins DQ0, DQ1, and DQ2 represent three pins in a data bus. (EX1003, ¶¶64-66; EX1004, at 7:35-36). Ring delay elements 57a-c are adjustable delay circuits that delay the data received at pins DQ0, DQ1, and DQ2 by a delay controlled by control signals C10, C11, and C12. (EX1003, ¶¶64-66; EX1004, 3:49-67, 7:30-35). Latches 59a-c are used to sample the delayed data received from the ring delay elements 57a-c in response to the data strobe signal DCLK. (EX1003, ¶¶64-66; EX1004, at 4:12-26). The control logic circuit 21 is responsible for determining appropriate control signals C10, C11, and C12 to enable

the memory device to properly read data lines DQ0, DQ1, and DQ2. (EX1003, ¶¶67-71; EX1004, 7:25-60). The control logic circuit stores delay values corresponding to the delays that result in the successful alignment of the data signals. (EX1003, ¶¶67-71; EX1004, 5:32-6:1, 7:45-61). During operation, the stored delay values are retrieved and used to delay the data signals. (EX1003, ¶¶67-71; EX1004, 5:32-6:1, 7:45-61).

### B. Summary of Stubbs

Stubbs (EX1005) discloses a memory controller for a DDR DRAM device. (EX1003, ¶72; EX1005, Abstract). Stubbs explains that a known problem is that different devices can have different propagation delays, causing misalignment between a data strobe and a data read/write operation. (EX1003, ¶72; EX1005, [0006], [0013-0015]). To solve this problem, Stubbs describes using delay-locked loop ("DLL") circuits to account for differences in propagation delay. (EX1003, ¶73; EX1005, [0010-0013]). Stubbs describes as prior art a system applying DLL circuits to both a data strobe and a data signal, as shown in Fig. 2:

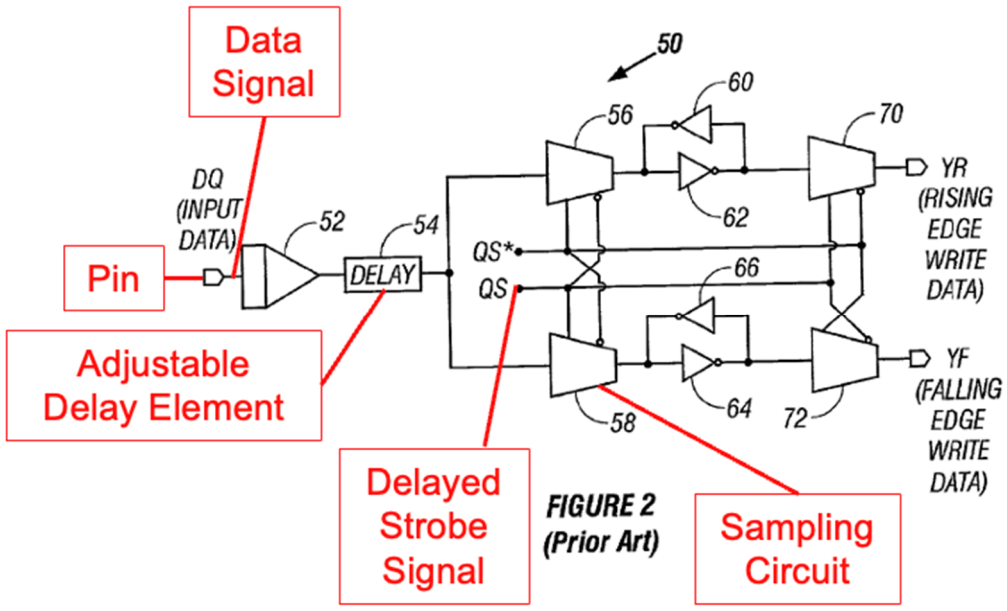



FIGURE 2 (Prior Art)

(EX1005, Fig. 2 (annotated excerpt)). The "pin" is the data line DQ data input line. (EX1003, ¶73; EX1005, [0033]). Delay element 54 is a variable delay element applied to the data signal. (EX1003, ¶73; EX1005, [0033]). The data strobe signal (QS/QS*) and the delayed data signal are provided to pass gate 58, which are sampling devices that "function to selectively allow the data appearing at their respective inputs to be presented at their respective outputs under the control of the data strobe (clock) signal QS/QS*." (EX1003, ¶73; EX1005, [0034]). Stubbs further discloses that the data strobe signal (QS/QS*) can be produced using a DLL circuit and is, thus, itself a delayed strobe signal. (EX1003, ¶73; EX1005, [0035]).

Stubbs explains that this prior art method of using DDL circuits on a per-bit basis to adjust the delay in reading data can cause problems if the propagation delays on the rising edge and falling edge are different. (EX1003, ¶74; EX1005, [0041-

0045]). Stubbs, therefore, discloses an improved memory controller device that provides two adjustable delay elements for each pin, one for the rising edge and the other for the falling edge of the clock signal. (EX1003, ¶75; EX1005, Abstract, [0018]). The delays are separately adjustable for data present during the rising edge of the data strobe signal and for data present during the falling edge of the data strobe signal, allowing the setup and hold window for write data to be optimized on a per-bit basis rather than a per-cycle basis. (EX1003, ¶75; EX1005, Abstract, [0018]). Fig. 4 is illustrative.

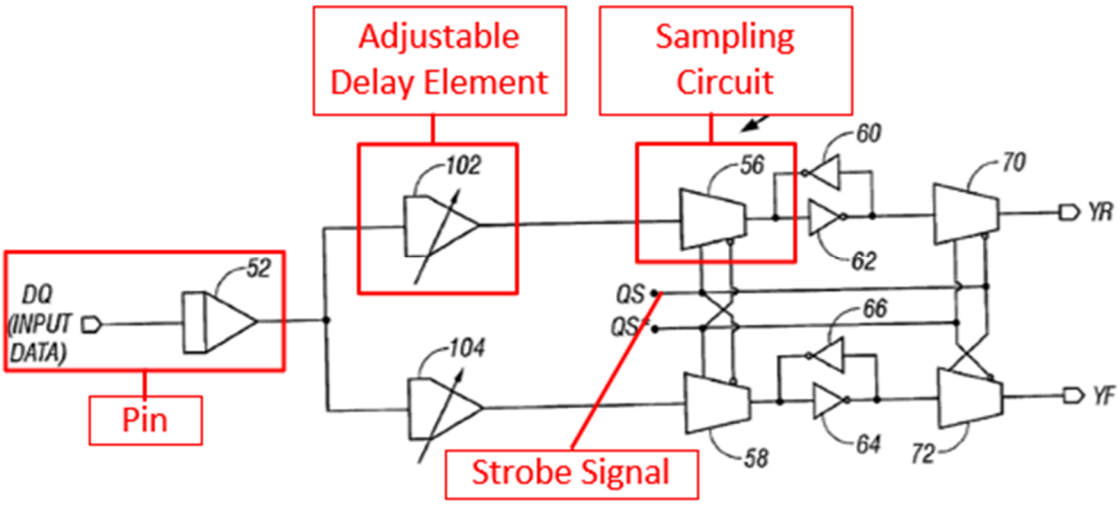


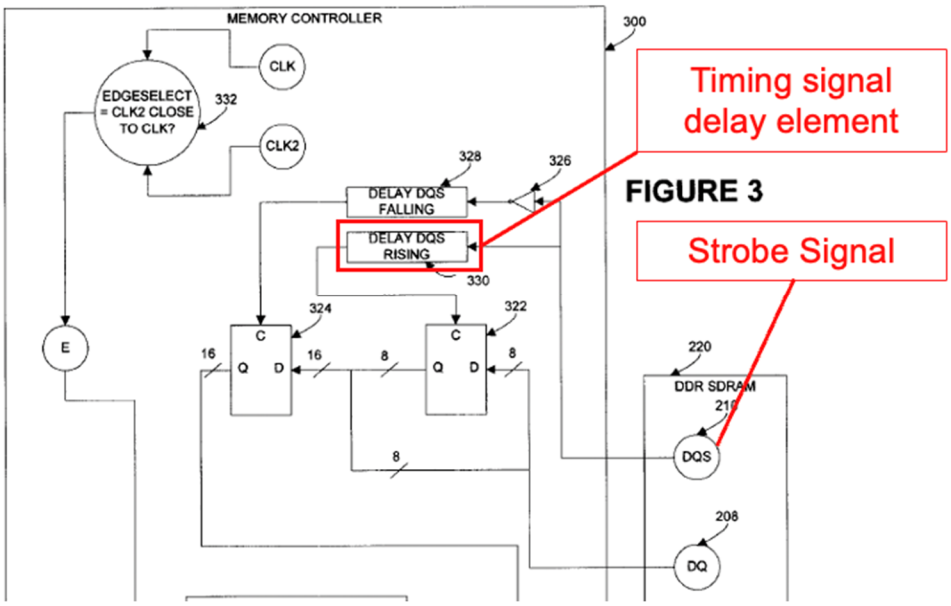

FIGURE 4

(EX1005, Fig. 4 (annotated)). Stubbs discloses various embodiments of the write path circuitry. In one embodiment shown in Figure 4, the write path circuitry includes an input buffer 52 that receives the input data signal, with the output of the input buffer coupled to first and second adjustable delay elements 102 and 104.

(EX1003, ¶76; EX1005, [0047]). The delayed data signal output from delay element 102 is applied to the input of a first pass gate 56, while the delayed data signal output from delay element 104 is applied to the input of a second pass gate 58. (EX1003, ¶76; EX1005, [0047]). The pass gates 56 and 58 are controlled by the data strobe signal to pass the delayed data signals at the appropriate time. (EX1003, ¶76; EX1005, [0047-0048]).

### C. Summary of Moss

Moss (EX1006) discloses a memory controller for use with DDR DRAM devices to compensate for timing differences between the memory controller's clock signal (CLK) and a strobe signal (DQS) from the memory devices. (EX1003, ¶77; EX1006, Abstract, 4:17-36, 5:34-47, Fig. 3). The memory controller includes programmable delay lines (306, 328, 330) that delay the CLK and DQS signals to align the timing of the signals for capturing read data (DQ). (EX1003, ¶77; EX1006, 5:52-6:25).




(EX1006, Fig. 3 (annotated excerpt)). The delay values for the programmable delay lines are predetermined during a calibration phase based on an analysis of the design or through automated measurements. (EX1003, ¶78; EX1006, 6:52-65). These delay values are then used during normal operation to adjust the timing of the CLK and DQS signals to compensate for propagation delays and align the read data capture. (EX1003, ¶79; EX1006, 5:55-6:3, 6:26-36, 7:55-8:4). By delaying the CLK and DQS signals using the calibrated delay values, the memory controller can capture the read data using the delayed clock signal (CLK2) in alignment with the delayed DQS signal. (EX1003, ¶80; EX1006, 2:18-42, 3:1-8, 6:48-58).

### D. Summary of Liou

Liou (EX1007) discloses a device and method for controlling data latch timing in a memory system. (EX1003, ¶81; EX1007, Abstract, [1003]). The device includes

a control chip that couples to a storage element, receives a data strobe signal (DQS) and memory data signal (MD), and delays DQS to latch the MD signal. (EX1003, ¶81; EX1007, [0018], Fig. 2). The control chip includes a back edge data comparison circuit that receives a first DQS signal and first MD signal, delays DQS by a controlled delay value and by the controlled delay value plus an offset, latches MD at both delay values, and compares the latched data. (EX1003, ¶83-86; EX1007, [0019], [0023], Claims 1, 6). Similarly, a front edge data comparison circuit receives a second DQS signal (DQS8) and second MD signal (MD71), delays DQS8 by the controlled delay value and by the controlled delay value minus an offset, latches MD71 at both delay values, and compares the latched data. (EX1003, ¶83-86; EX1007, [0019], [0024], Claims 1, 7).

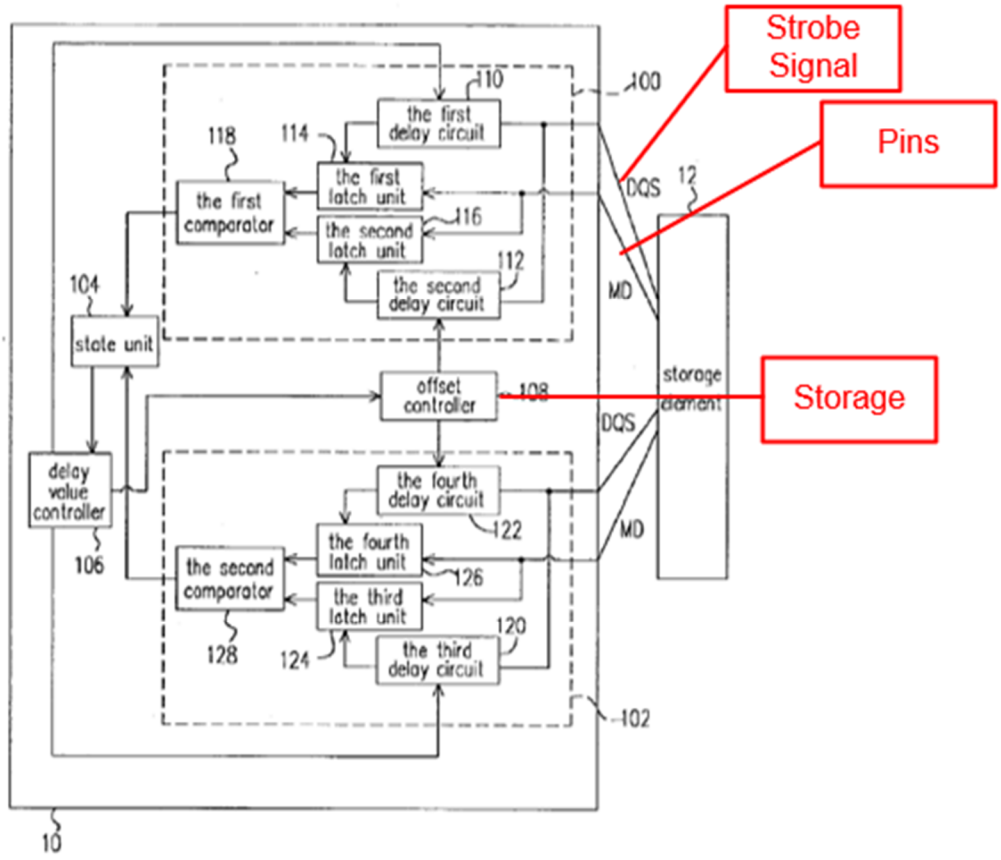



FIG. 2

(EX1007, Fig. 2 (annotated)). A delay value controller provides the controlled delay value, which can be initially set by the BIOS during system initialization. (EX1003, ¶84; EX1007, [0021]). The delay value controller adjusts the controlled delay value based on the comparison results to compensate for timing offsets caused by temperature and voltage variations. (EX1003, ¶85; EX1007, [0025-0031], Claims 8-10, 17-18). In this way, Liou discloses a broad, adjustable memory interface that can ensure accurate data capture despite variable operating conditions. (EX1003, ¶87; EX1007, [0007], [0011-0012], [0028-0030]).

## IX. Motivations to Combine

A POSITA would have been motivated to combine each of the asserted combinations to arrive at the challenged claims. (EX1003; ¶88. Each of Johnson, Stubbs, Moss, and Liou relate to memory controllers for use in DDR DRAM devices and, more specifically, to systems and methods for overcoming issues associated with propagation delays that can cause misalignment between strobe signals and data signals. (EX1003, ¶88; EX1004, 2:44-54; EX1005, [0006-0007]; EX1006, 4:37-64, EX1007, [0005-0007]). Thus, all the references asserted here are analogous art because they are in the same field of endeavor, specifically, memory controllers and components thereof for DDR DRAM devices. (EX1003, ¶88).

### A. Motivation to Combine Johnson and Moss

A POSITA would have been motivated to combine Johnson and Moss. (EX1003, ¶¶89-93). As discussed above, both Johnson and Moss are in the same field of endeavor. (EX1003, ¶¶89-93). A POSITA in possession of Johnson would look to Moss for further disclosure on systems and methods for delaying the data strobe (DQS) signal to produce an improved memory controller. (EX1003, ¶¶89-93). In particular, Johnson already discloses the concept of adding a delay element to the data strobe signal. (EX1004, Fig. 4, element 55). (EX1003, ¶¶89-93). To provide enhanced flexibility, a POSITA in possession of Johnson would look to Moss to incorporate a plurality of delay elements to the data strobe signal. (EX1003, ¶¶89-

93). Moss discloses applying a delay element to the data strobe signal DQS 210 using delay element 330. (EX1006, Fig. 3). (EX1003, ¶¶89-93). Moss further discloses that the size of the data path – i.e. the number of data pins in each data path – is a design choice well within the knowledge and ability of a POSITA, and expressly recites examples of 4, 8, and 16-bit wide data paths. (EX1003, ¶¶89-93; EX1006, 6:47-48).

### B. Motivation to Combine Johnson-Moss in further view of Liou

As discussed above, a POSITA would have been motivated to combine Johnson and Moss to arrive at a memory controller with multiple delay elements, one for each data path. (EX1003, ¶¶94-96). A POSITA would have been further motivated to combine Johnson-Moss with Liou. (EX1003, ¶¶94-96). Liou, like Johnson and Moss, discloses a memory controller for DRAM memory. (EX1003, ¶¶94-96). EX1007, at Abstract, [0005]). Liou provides further disclosure regarding the use of delay elements on the data strobe signal. (EX1003, ¶¶94-96). A POSITA in possession of Johnson-Moss for further disclosure and details regarding the use of delay elements on the data strobe signal. (EX1003, ¶¶94-96).

### C. Motivation to Combine Stubbs with Moss

A POSITA would have been motivated to combine Stubbs with Moss. (EX1003, ¶¶97-100). As discussed above, both Stubbs and Moss are in the same field of endeavor. (EX1003, ¶¶97-100). A POSITA in possession of Stubbs would

look to Moss for additional details disclosing how to provide a delayed data strobe signal. (EX1003, ¶¶97-100; EX1006, [0035]). Moss provides additional details on delaying a data strobe signal using a delay element. (EX1003, ¶¶97-100; EX1006, Fig. 3, 6:47-48). Further, Moss further discloses that the size of the data path – i.e., the number of data pins in each data path – is a design choice well within the knowledge and ability of a POSITA and expressly recites examples of 4, 8, and 16-bit wide data paths. (EX1003, ¶¶97-100; EX1006, 6:47-48). Thus, a POSITA in possession of Stubbs and Moss would realize that delay elements on the data strobe line could be further modified to provide a delay element for each bit. (EX1003, ¶¶97-100).

### D. Motivation to Combine Stubbs-Moss in further view of Liou

A POSITA would have been motivated to combine Stubbs and Moss to arrive at a memory controller with multiple delay elements, one for each data path. (*See supra,* § IX.C). A POSITA would have been further motivated to combine Stubbs-Moss with Liou. (EX1003, ¶¶100-103). Liou, like Stubbs and Moss, discloses a memory controller for DRAM memory. (EX1003, ¶¶100-103; EX1007, at Abstract, [0005]). Liou provides further disclosure, as discussed below, regarding the use of delay elements on the data strobe signal. (EX1003, ¶¶100-103). A POSITA in possession of Johnson-Moss for further disclosure and details regarding the use of delay elements on the data strobe signal. (EX1003, ¶¶100-103).

### E. Motivation to Combine Stubbs-Moss in further view of Johnson

As discussed above, a POSITA would have been motivated to combine Stubbs and Moss to arrive at a memory controller with multiple delay elements, one for each data path. (*See supra*, § IX.C; EX1003, ¶¶104-108). A POSITA would further be motivated to combine Stubbs-Moss with Johnson to provide a specific calibration method for use with the physical systems provided in Stubbs and Moss. (EX1003, ¶¶104-108). The calibration technique and associated control circuitry of Johnson could be used directly with the Stubbs-Moss combination to arrive at the claimed methods. (EX1003, ¶¶104-108). This would have been a simple substitution of components, replacing the delay circuity of Johnson with the systems described in Stubbs-Moss. (EX1003, ¶¶104-108).

## X. Ground 1: Obvious over Johnson, in view of Moss

### A. Claim 1

#### a. Element 1[pre]: "An integrated circuit (IC) memory controller comprising"

If the preamble is limiting, Johnson discloses this limitation. (EX1003, ¶110). Johnson describes an "integrated memory circuit." (EX1003, ¶110; EX1004, Claim 67). Moss also discloses this limitation. Moss implements a memory controller as an integrated circuit, allowing for efficient signal routing and timing control within a single chip. (EX1003, ¶111; EX1006, Fig. 3).

**b. Element 1[a]: "a first pin to receive a first data signal; a first adjustable delay element to delay the received first data signal and generate a first delayed data signal;"**

Johnson discloses limitation 1[a]. Johnson's memory device includes multiple data paths for receiving data signals, each with an associated adjustable delay element. (EX1003, ¶¶112-14; EX1004, Fig. 4).

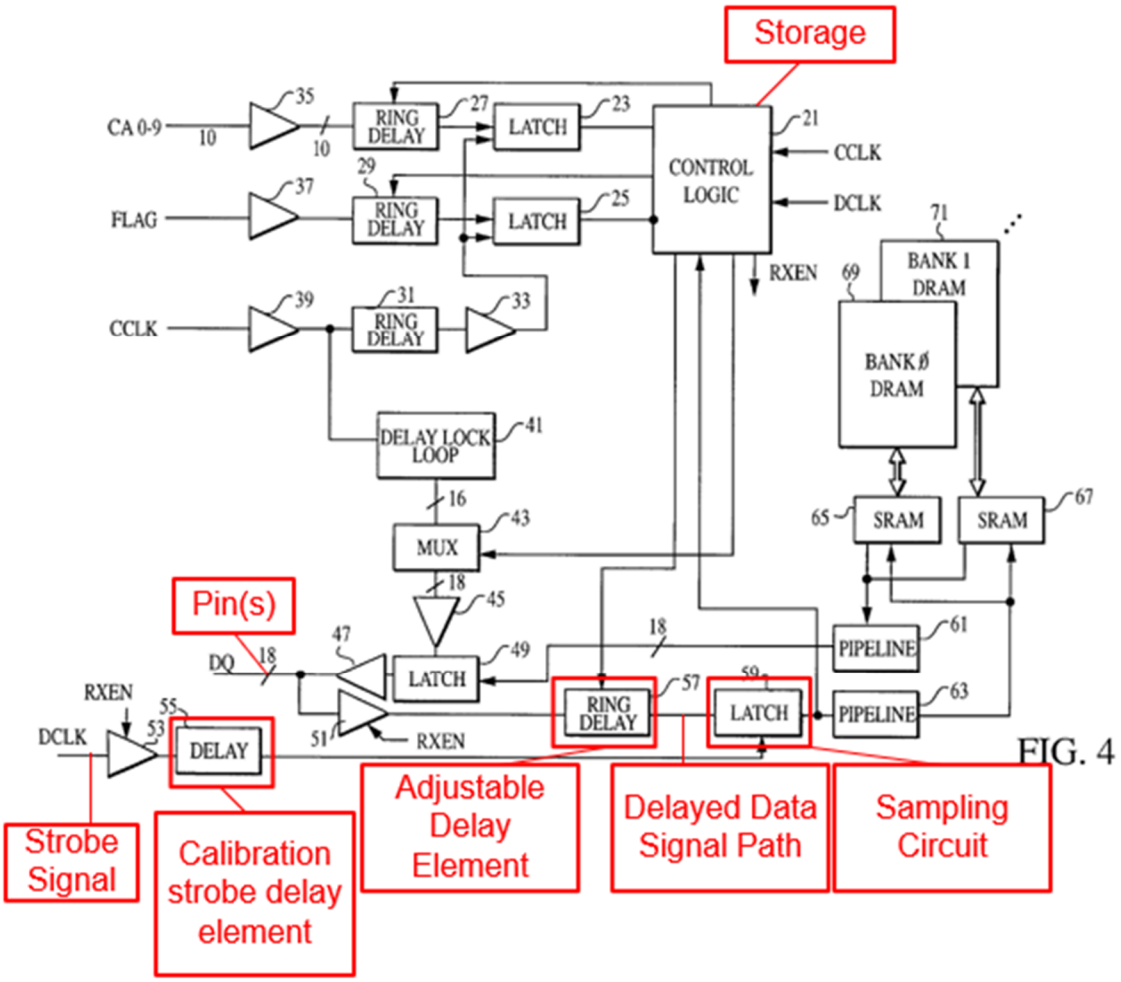



FIG. 4

(EX1004, Fig. 4 (annotated)). Specifically, Johnson shows a data path DQ that includes a pin to receive an incoming data signal and a ring delay 57 to delay that received data signal. (EX1003, ¶¶112-14; EX1004, Fig. 4, 7:25-60). The ring delay

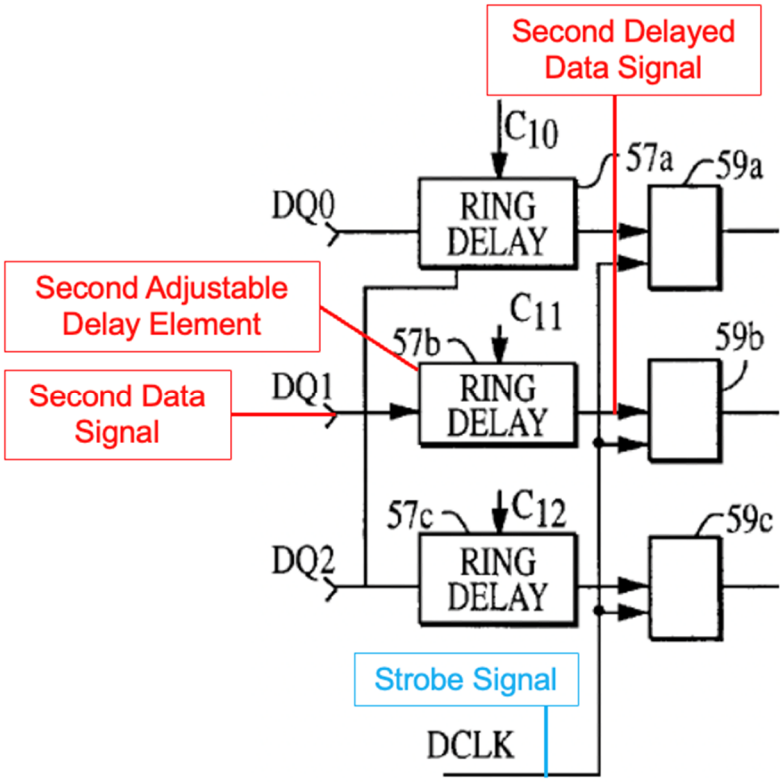
57 is an adjustable delay element that can impart different amounts of delay to the received data signal, generating a delayed version which is then provided to latch 59. (EX1003, ¶¶112-14; EX1004, Fig. 4, 4:13-18, 7:25-60).

The adjustable nature of the delay element allows the memory device to calibrate the timing of data signals relative to a clock signal, compensating for timing variations and ensuring proper sampling of the data signal. (EX1003, ¶¶112-14; EX1004, 1:38-43, 4:38-43, 7:54-59). Thus, Johnson discloses both a first pin to receive a first data signal and a first adjustable delay element to delay the received first data signal and generate a first delayed data signal as recited in limitation 1[a].

Even if Johnson did not disclose this feature, Moss also discloses limitation 1[a]. Moss describes a memory controller that receives data signals, including data signal DQ, from a memory component via pins. (EX1003; ¶¶115-17; EX1006, Fig. 3, 5:51-55, 6:28-36). The controller includes delay line 330, an adjustable delay element that delays the data strobe signal DQS controlling the sampling of the data signal DQ, effectively delaying the received data signal and generating a delayed version. (EX1003; ¶¶115-17; EX1006, Fig. 3, 6:16-63). Thus, Moss discloses both a first pin to receive a first data signal and a first adjustable delay element to delay the received first data signal and generate a first delayed data signal as recited in limitation 1[a].

**c. Element 1[b]: "a second pin to receive a second data signal; a second adjustable delay element to delay the received second data signal and generate a second delayed data signal;"**

Johnson discloses this limitation. (EX1003, ¶119). As described above with reference to Element 1[a], Johnson discloses a "first pin to receive a first data signal" (signal DQ0), a "first adjustable delay element" (ring delay 57a), that generates a "first delayed data signal." (input to latch 59a). In the same manner, Johnson also discloses a "second pin to receive a second data signal" (signal DQ1), a "second adjustable delay element" (ring delay 57b) that generates a "second delayed data signal" (input to latch 59b). (EX1003; ¶199; *See, e.g.* EX1004, 4:36-52, 7:24-60)



(EX1004, Fig. Even if Johnson did not disclose this feature, Moss does. (EX1003; ¶120). Moss's memory controller includes circuitry to receive and process multiple data signals from memory components via a data bus DQ, which comprises multiple data pins. (EX1003, ¶120; EX1006, 1:15-40, 5:25-28, Fig. 3). The controller's delay elements, such as delay line 330, delay the received data signals, effectively generating delayed versions of these signals. (EX1003, ¶120; EX1006, 6:16-23, 6:28-36).

A POSITA would have been motivated to combine Johnson's multiple data pins with adjustable delays and Moss's multi-pin data bus with delay elements, as both address timing control for multiple data signals in memory systems. (EX1003; ¶121).

**d. Element 1[c]: "a pin to receive a strobe signal;"**

Johnson discloses a pin to receive a strobe signal DCLK, which is used to clock data into and out of the memory device. (EX1003, ¶¶122-23; EX1004, Fig. 4, 4:24-5:7). This DCLK strobe signal serves the same purpose as the strobe signal in the challenged patent, timing the sampling of data signals. (EX1003, ¶¶122-23, EX1004, 4:24-5:7, Fig. 5).

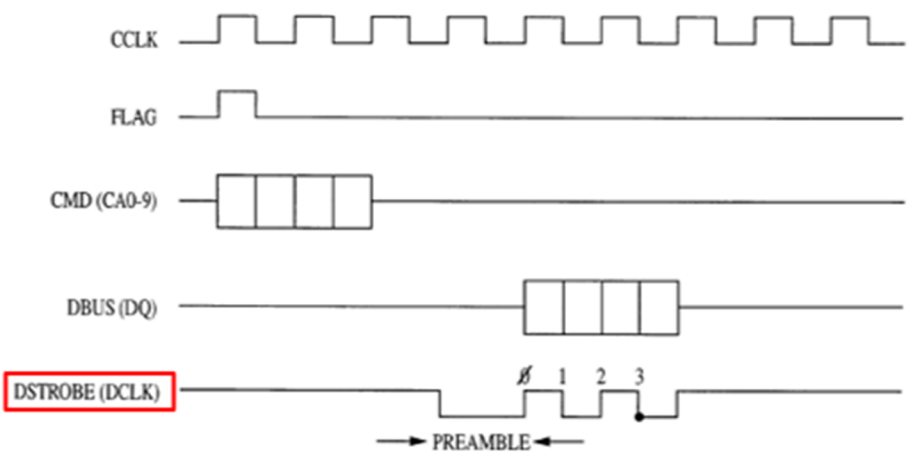



FIG. 5

(EX1004, Fig. 5 (annotated)).

Even if Johnson did not disclose this feature, Moss does. (EX1003, ¶¶124-25). Moss discloses a memory controller with a pin to receive a strobe signal DQS from an associated memory component, which is applied to delay lines within the controller. (EX1003, ¶¶124-25; EX1006, 5:48-60, 6:16-22, Fig. 3). A POSITA would have been motivated to combine Johnson's pin for receiving data signals with Moss's adjustable delay elements for data signal timing, as both address timing control in memory systems to improve data transfer efficiency. (EX1003, ¶126).

**e. Element 1[d]: "a first sampling circuit to sample the first delayed data signal based on the strobe signal; and"**

Johnson discloses this limitation. (EX1003, ¶¶127-28). Referring to Figure 10, the latch 59a serves as a "first sampling circuit to sample the first delayed data signal based on the strobe signal." (EX1003, ¶¶127-28; EX1004, 4:12-26). As shown

in Figure 10, the latch 59a receives two critical inputs: (1) the "first delayed data signal" from ring delay 57a, and (2) the "strobe signal" DCLK.

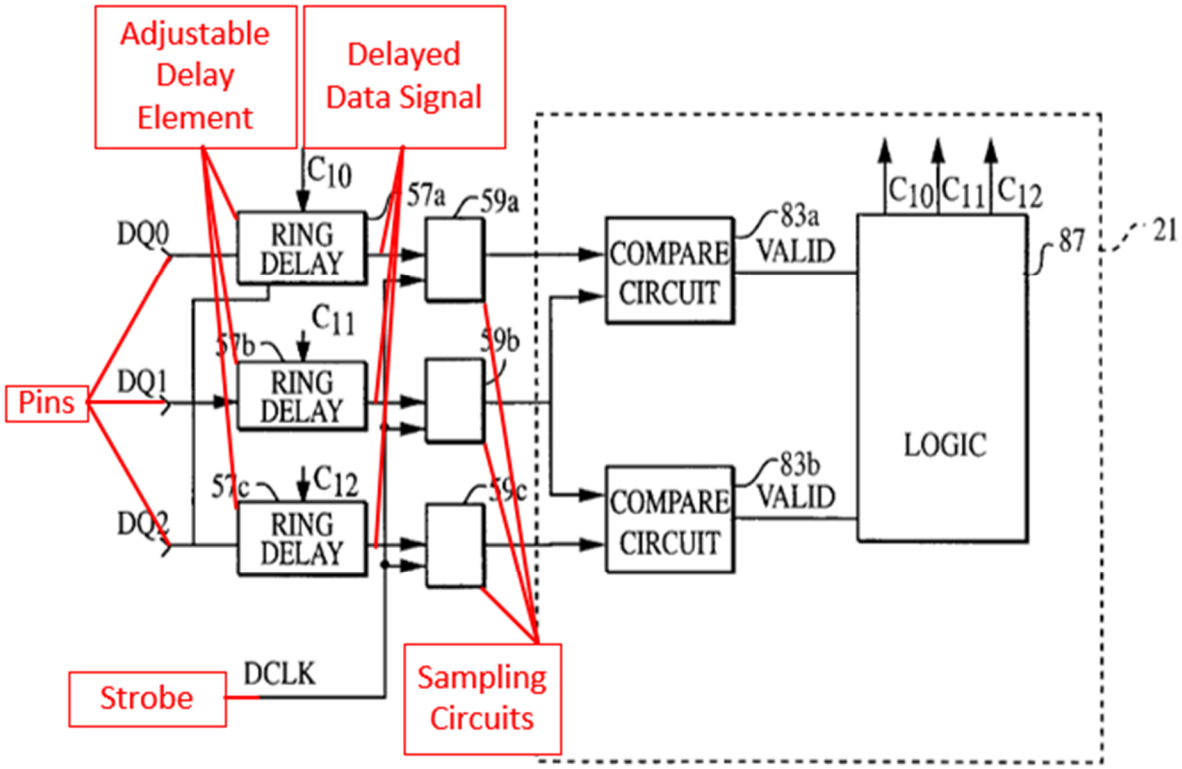



FIG. 10

(EX1004, Fig. 10 (annotated excerpt)).

Johnson states that "DCLK passes through gated buffer 53, delay circuit 55 and is used to control latch 59 to latch in incoming data on the data bus DQ." (EX1003, ¶¶127-28; EX1004, 4:12-26). That is, the DCLK strobe signal directly controls the sampling operation of latch 59a. The use of the word "control" indicates that the latch's operation is fundamentally dependent on and driven by the DCLK signal. (EX1003, ¶¶127-28).

Even if Johnson did not disclose this feature, Moss does. (EX1003, ¶¶127-28). Moss's memory controller interfaces with DDR SDRAM components via a data bus DQ comprising multiple data pins, receiving and processing multiple data signals. (EX1003, ¶¶127-28; EX1006, 1:9-14, 6:16-6:36, Fig. 3). The controller employs delay elements, such as delay line 330, to delay these received data signals, effectively generating delayed versions. (EX1006, 6:16-6:36).

A POSITA would have been motivated to combine Johnson's multiple data pins with adjustable delays and Moss's multi-pin data bus with delay elements, as both address timing control for multiple data signals in memory systems because it would enhance memory controller performance by improving timing control and signal integrity for multiple data signals. (EX1003, ¶130).

**f. Element 1[e]: "a second sampling circuit to sample the second delayed data signal based on the received strobe signal."**

Johnson discloses this limitation. (EX1003, ¶¶131). As described above, Johnson discloses a "first sampling circuit" with respect to the data path originating from DQ0, through ring delay 57a and latch 59a. (*See* supra, § X.A.d). Similarly, Johnson discloses a "second sampling circuit to sample the second delayed data signal based on the strobe signal" with respect to the data path originating from DQ1, through ring delay 57b and latch 59b. (EX1003, ¶ 131).

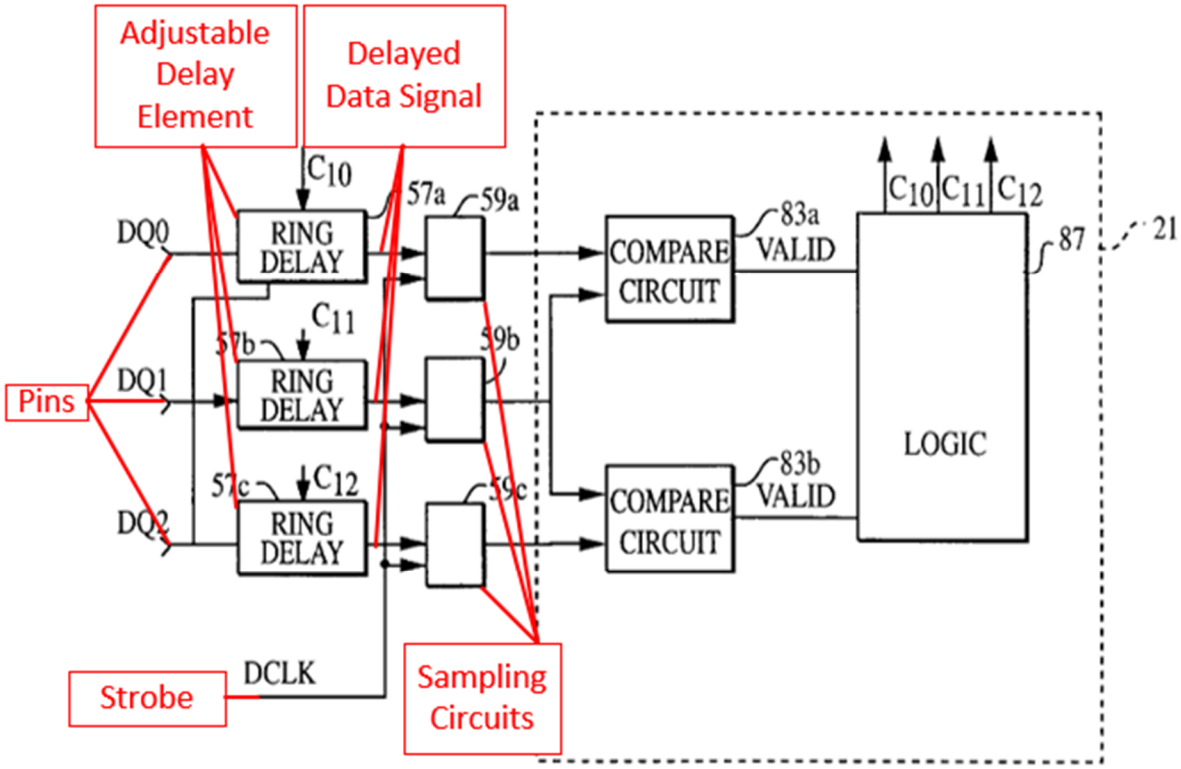
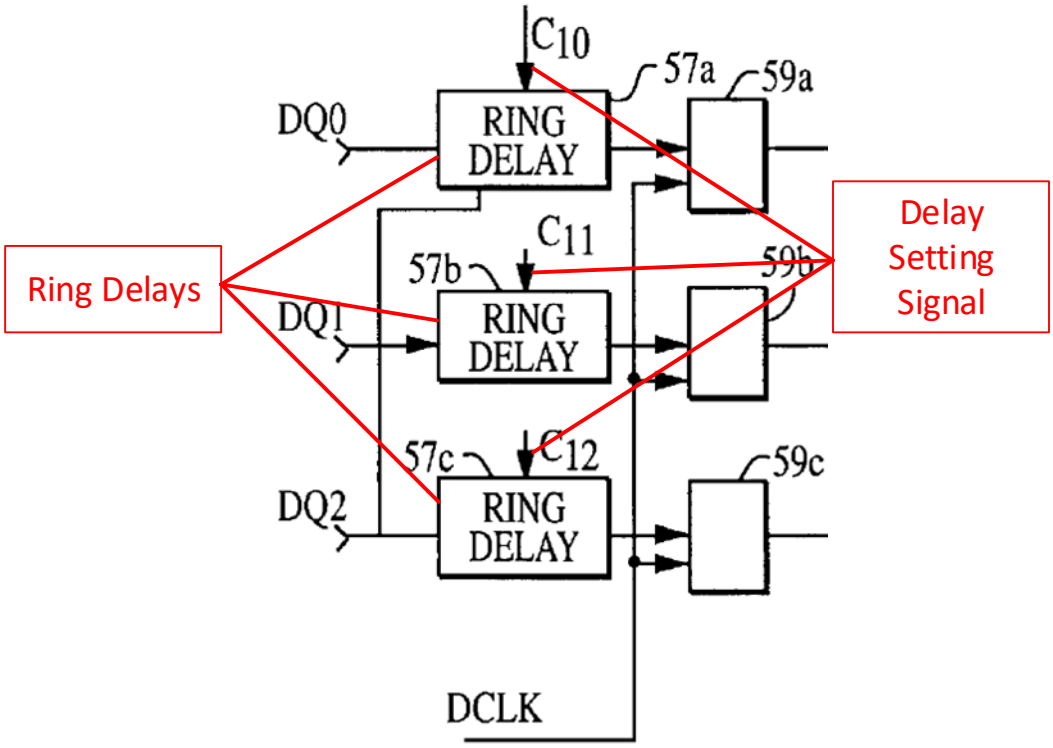



FIG. 10

(EX1004, Fig. 10 (annotated excerpt). Moss also discloses this feature. While Moss shows only one data signal path with register flip-flop 322 in Figure 3, a POSITA would have understood that memory interfaces have multiple data pins for data transfer. (EX1004, ¶132; EX1006, 1:25-31, 5:25-6:25). A POSITA would have been motivated to combine the teachings of Johnson and Moss to arrive at the claimed second sampling circuit because references address timing control in multi-pin memory systems, and the combination would yield predictable results in enhancing memory controller performance. (EX1003, ¶133).

**B. Claim 2: "The IC memory controller according to claim 1, further comprising storage to store each of first and second delay values corresponding to the delays imparted to the first and second data signals."**

Johnson discloses this claim. (EX1003, ¶134). In particular, it describes that control logic can step the ring delays 57a-b through possible delay values, and select a best delay value which is provided to ring delays 57a-b. (EX1003, ¶134; EX1004, 7:25-60). As Johnson describes, "the delay settings of the ring delays 57a, 57b, 57c may be set by logic 87 using signals C10, C11, C12, respectively." (EX1003, ¶134; EX1004, at 7:25-60).




(EX1004, Fig. 10 (annotated excerpt)). A POSITA would have understood that these delay values are necessarily stored in the control logic 21 for application to ring

delays 57, and thus Johnson inherently discloses this feature. (EX1003, ¶134; EX1004, Fig. 10)

Even if Johnson did not disclose this feature, Moss does. (EX1003, ¶135). Moss discloses a memory controller with delay lines that use predetermined, stored delay values to delay the data strobe signal for proper data sampling. (EX1003, ¶135; EX1006, Fig. 3, 6:16-26, 6:55-63).

A POSITA would have been motivated to combine Johnson's storage of delay values for multiple data paths with Moss's use of predetermined stored delays, as both address timing control in memory systems. (EX1003, ¶136).

### C. Claim 4: "The IC memory controller according to claim 1, wherein the first and second data signals are delayed to compensate for timing offset between the received first and second data signals."

Johnson discloses this claim. (EX1003, ¶137). Specifically, Johnson is directed to a calibration system and method of calibrating data paths "to produce serial and parallel bit alignment on all data paths." (EX1003, ¶137; EX1004, at Abstract). The purpose of Johnson is to ensure that any delays between the data signals in various paths (including a first and second data signals) are aligned, thereby compensating for any time offsets. (EX1003, ¶137; EX1004, at 2:24-42).

Even if Johnson did not disclose this feature, Moss does. Moss's memory controller uses delay elements to align received data signals with a strobe signal,

skewing the data strobe signal DQS to capture data at the center of DQS transitions. (EX1003, ¶138; EX1006, 3:9-15, Fig. 3, 6:24-27).

A POSITA would have been motivated to combine Johnson's use of delays for compensating timing differences across multiple data paths with Moss's technique of skewing the data strobe signal relative to the data signal, as both address timing control in memory systems. (EX1003, ¶139).

### D. Claim 5: "The IC memory controller according to claim 4, further comprising: a first timing signal delay element associated with the first pin; and a second timing signal delay element associated with the second pin; wherein each of the first and second timing signal delay elements impart first and second delays to the strobe signal."

Johnson discloses this claim. (EX1003, ¶¶140-42). Johnson's memory controller uses adjustable delay elements to align data signals with a clock signal, featuring a data path with a data pin DQ, delay elements, and a latch controlled by a delayed clock signal. (EX1003, ¶¶140-42; EX1004, Fig. 4, 4:13-27). Johnson teaches that control logic can adjust delays for multiple data paths. (EX1003, ¶¶140-42; EX1004, 7:37-60).

Even if Johnson did not disclose this feature, Moss does. (EX1003, ¶¶143-144). Moss teaches delaying the data strobe signal DQS using a delay line 330, which then clocks register flip-flops to capture data from the memory component. (EX1003, ¶¶143-144; EX1006, Fig. 3, 6:16-35). While Moss shows a single delay line for the strobe signal, implementing separate delay elements for each data pin or

group of pins would have been an obvious extension to allow for more precise timing compensation. (EX1003, ¶¶143-144).

A POSITA would have been motivated to combine Johnson's adjustable delays for multiple data paths with Moss's technique of delaying the strobe signal, as both address timing control in memory systems. (EX1003, ¶145).

### E. Claim 6: "The IC memory controller according to claim 1, wherein: each of the first and second delay elements comprise locked-loop circuits having plural serially connected delay elements."

Johnson discloses this claim. (EX1003, ¶¶146-47). Johnson discloses adjustable delay elements in data paths DQ0-17, implemented as ring delays with plural serially connected delay elements. (EX1003, ¶¶146-47; EX1004, Fig. 4, 7:25-60, Fig. 10). These ring delays, which can be selectively enabled to adjust the overall delay, disclose locked-loop circuits. (EX1003, ¶¶146-47).

Even if Johnson did not explicitly disclose this limitation, Moss's teachings make this feature obvious. (EX1003, ¶¶148-49). Moss describes programmable delay lines for compensating phase offset errors. (EX1006, 6:56-63), and while not explicitly stating they are locked-loop circuits, a POSITA would recognize that such architecture is common in programmable delay lines. (EX1003, ¶¶148-49). Given Moss's discussion on compensating for various sources of delay and phase variance. (EX1006, 6:8-15), a locked-loop circuit with multiple delay elements would have

been an obvious choice to address these challenges, as it could maintain precise timing across different operating conditions. (EX1003, ¶¶148-49).

A POSITA would have been motivated to implement Moss's programmable delay lines using Johnson's locked-loop circuit architecture, as both address timing control in high-speed memory interfaces and aim to improve signal alignment. (EX1003, ¶150).

### F. Claim 7: "The IC memory controller according to claim 6, wherein the first delay value is used to select delay elements of the first delay circuit and the second delay value is used to select delay elements of the second delay circuit."

Johnson discloses this claim. (EX1003, ¶151). Johnson's memory controller employs ring delay circuits with plural serially connected delay elements in data paths, allowing for adjustable delays based on specific delay values. (EX1003, ¶151; EX1004, 4:1-10, Fig. 4, Fig. 10). Johnson teaches selecting delay elements based on delay values, which a POSITA would have understood applies to all ring delays in the system, enabling fine-tuning of each data path's timing independently to compensate for variations and achieve optimal alignment with the clock signal. (EX1003, ¶151; EX1004, 1:38-43, 4:38-50).

Even if Johnson did not disclose this claim, Moss does. (EX1003, ¶152). Moss discloses using delay values to select delay elements in programmable delay lines within its IC memory controller. (EX1003, ¶152; EX1006, Fig. 3, 6:16-23). A POSITA would understand that the Delay DQS Rising 330 and Delay DQS Falling

328 circuits operate in this manner, allowing precise delay adjustments to meet specific timing requirements. (EX1003, ¶152; EX1006, 6:64-7:4).

A POSITA would have been motivated to combine Johnson's explicit teaching of using delay values to select delay elements with Moss's programmable delay lines, because this combination would predictably enhance delay precision and adaptability, offering the known benefits of fine-grained delay adjustment crucial for high-performance memory controllers. (EX1003, ¶153).

### G. Claim 9: "The IC memory controller according to claim 1, further comprising a calibration circuit to, in a calibration mode, determine the first and second delay values."

Johnson discloses this claim. (EX1003, ¶¶154-55, EX1004, 6:35-45, 7:46-53). During calibration, the control logic circuit 21 determines appropriate delay values for each ring delay to align data on different DQ paths. (EX1003, ¶¶154-55; EX1004, at 7:46-53).

Even if Johnson did not disclose this feature, Moss renders it obvious. (EX1003, ¶156; EX1006, at 6:55-7:2). Moss teaches a memory controller that uses predetermined delay values to compensate for phase offset errors. (EX1003, ¶156; EX1006, at 6:55-63). While Moss does not explicitly describe a calibration mode, it suggests that delay values are determined through external methods. (EX1003, ¶156; EX1006, at 6:64-7:2). A POSITA would have recognized that implementing a calibration mode to determine these values is a straightforward extension of Moss's

teachings. (EX1003, ¶156). A POSITA would have been motivated to combine Johnson's explicit calibration mode into Moss's memory controller, because combining them would yield predictable results in enhancing memory controller performance. (EX1003, ¶157).

### H. Claim 10:

Claim 10 is substantially similar to Claim 1, and merely rephrases the apparatus claim of Claim 1 as a method. Thus, Claim 10 is invalid for substantially the same reasons as described above with respect to Claim 1, and for the additional reasons provided below. *See supra*, § X.A.

#### a. Element 10[pre]: "A method of operation in an IC memory controller, the method comprising:"

The preamble is not limiting. To the extent the preamble is limiting, Johnson discloses this limitation. (EX1003, ¶¶158-59). Johnson teaches a method of operation in an IC memory controller that coordinates data flow and timing in the memory system, executing specific steps and procedures to ensure proper functioning. (EX1003, ¶¶158-59; EX1004, at 3:34-41, 4:28-43).

Even if Johnson does not disclose this limitation, Moss does. Moss teaches a method of operation in an IC memory controller for realigning read data returned from memory components to adjust for phase shifts due to propagation delays and other factors. (EX1003, ¶160; EX1006, at Abstract, 1:43-54).

A POSITA would have been motivated to combine the methods of Johnson and Moss to create a comprehensive method of operation for an IC memory controller, as both references address timing control and signal synchronization in memory systems. (EX1003, ¶162).

**b. Element 10[a]: "receiving first and second data signals from a memory device at respective first and second pins;"**

Johnson discloses this limitation. (EX1003, ¶163). Johnson's memory controller receives data signals from a memory module over a bi-directional data bus DQ0-17, which comprises multiple data paths connected to respective pins on the memory controller. (EX1003, ¶163; EX1004, Fig. 3, 3:31-45, Fig. 4, 3:65-4:18).

Even if Johnson did not disclose this limitation, Moss does. (EX1003, ¶ 164). Moss's memory controller receives multiple data signals from a DDR SDRAM memory component at corresponding pins. (EX1003, ¶164; EX1006, Fig. 3, Abstract). For a typical 8-bit wide DDR SDRAM, this corresponds to 8 separate data signals received at 8 respective pins of the memory controller. (EX1003, ¶150; EX1006, 6:39-49).

A POSITA would have been motivated to combine the teachings of Johnson and Moss to achieve the claimed method, as both references address memory systems using multiple data pins, and combining Johnson and Moss would yield predictable results in enhancing memory controller performance, providing the

known benefits of increased data bandwidth in high-speed memory interfaces. (EX1003, ¶165).

**c. Element 10[b]: "aligning the received first and second data signals with a strobe signal, the aligning comprising imparting a first delay to the first data signal, the first delay corresponding to a first delay value, imparting a second delay to the second data signal, the second delay corresponding to a second delay value."**

Johnson discloses this limitation. (EX1003, ¶¶166-67, EX1004, 1:27-31, 4:37-43). Johnson's memory controller aligns first and second data signals received from a memory device with a strobe signal. (EX1003, ¶¶166-67; EX1004, 1:27-31, 4:37-43). This alignment is accomplished using adjustable delay elements to delay the received data signals and generate delayed data signals. (EX1003, ¶¶166-67; EX1004, 4:43-56, Fig. 4). Johnson uses separate adjustable delay elements with individually calibrated delay values for each data signal, compensating for timing variations between different data signals and achieving precise alignment with the strobe signal. (EX1003, ¶¶166-67; EX1004, 1:12-26, 4:37-50).

Even if Johnson did not disclose this feature, Moss does. (EX1003, ¶¶168-69). Moss teaches a memory controller that aligns received data signals (DQ) with a strobe signal (DQS) by imparting delays. (EX 1003, ¶¶168-69; EX1006, Fig. 3, 5:51-61).

A POSITA would have been motivated to combine Johnson's individually calibrated delay elements with Moss's programmable delay lines, because this

combination would yield predictable results in enhancing delay precision and adaptability, providing the known benefits of fine-grained delay adjustment critical in high-performance memory controllers. (EX1003, ¶170).

### I. Claim 11: "The method according to claim 10, further comprising: in a calibration mode, determining the first and second delay values; and storing the first and second delay values."

Johnson discloses this claim. (EX1003, ¶171). During calibration, Johnson's control logic circuit determines and stores first and second delay values for ring delays in each data path. (EX1003, ¶171; EX1004, 5:50-61, 5:67-6:5). Johnson necessarily stores these delay values to track them during calibration and apply them to ring delays in normal operation. (EX1003, ¶171; EX1004, 1:69-2:2, 5:61-6:5). This calibration occurs during initialization, constituting a calibration mode. (EX1003, ¶171; EX1004, 1:40-43).

Even if Johnson did not disclose this claim, Moss does. Moss determines delay values during calibration to compensate for phase offsets between clock and strobe signals, calculating multiple delay values for clock and data signal paths. (EX1003, ¶172; EX1006, 5:58-63, 6:55-59, 7:5-10). Moss stores these calibrated values for quick configuration of programmable delay lines without recalibration. (EX1003, ¶172; EX1006, 7:10-20).

A POSITA would have been motivated to combine Johnson's calibration process with Moss's storage and reuse of delay values to enhance calibration

efficiency and adaptability, providing the known benefits of quick reconfiguration without full recalibration. (EX1003, ¶172).

### J. Claim 12: "The method according to claim 11, wherein: during the receiving mode, the imparting the first and second delays includes retrieving the stored first and second delay values."

Johnson discloses this claim. (EX1003, ¶ 174). During normal operation, Johnson's memory controller retrieves previously determined and stored delay values to set appropriate delays for each data path, which directly corresponds to the claimed "imparting the first and second delays includes retrieving the stored first and second delay values" during a receiving mode. (EX1003, ¶174; EX1004, 1:64-2:2, 7:54-59). By using stored delay values, Johnson's system can quickly configure data paths for proper timing alignment when entering a receiving mode, eliminating the need for recalibration and improving system efficiency. (EX1003, ¶175; EX1004, 1:38-2:9)

Even if Johnson does not disclose this claim, Moss does. (EX1003, ¶ 175). Moss's memory controller uses stored delay values to configure programmable delay lines during read operations, which correspond to a receiving mode. (EX1003, ¶175; EX1006, 6:55-65, 7:10-20). The delay line 306 in Figure 3 uses these stored values to realign clock and data signals, effectively imparting delays based on retrieved delay values. (EX1003, ¶175; EX1006, Fig. 3, 6:55-65).

A POSITA would have been motivated to combine Johnson's explicit teaching of retrieving stored delay values during operation with Moss's use of stored values for quick reconfiguration, as both references address timing control in memory systems and seek to improve signal alignment efficiency. (EX1003, ¶176)

### K. Claim 13: "The method according to claim 12, wherein: the first and second data signals are delayed by the first and second delay values."

To the extent this claim is not indefinite, Johnson discloses this claim. (EX1003, ¶ 177). Johnson's memory controller uses adjustable delay elements in multiple data paths to align data signals with a clock signal. (EX1003, ¶177; EX1004, Abstract, 3:50-67, Fig. 4).

Even if Johnson does not disclose this claim, Moss does. Moss's memory controller uses programmable delay lines to delay data signals based on predetermined delay values. (EX1003, ¶178; *See supra*, §X.H.c).

A POSITA would have been motivated to combine Johnson's individually calibrated delay elements with Moss's programmable delay lines, as both references address timing control in high-speed memory interfaces and seek to improve signal alignment. (EX1003, ¶179).

### L. Claim 14: "The method according to claim 11, further comprising: during the calibration mode, calibrating a timing signal delay value corresponding to a delay for application to the strobe signal."

Johnson discloses this claim. (EX1003, ¶¶180-81). Johnson's SLDRAM device includes a calibration strobe delay element to impart a calibrated delay to the strobe signal during a calibration mode. (EX1003, ¶¶180-81; EX1004, 4:24-27). During calibration, the control logic circuit steps through possible delay values for both data and strobe signals, determining an optimal internal delay for clock signals, including the strobe signal, relative to data signals. (EX1003, ¶¶180-81; EX1004, 5:29-40, 5:60-67).

Even if Johnson did not disclose this claim, Moss does. (EX1003, ¶182). Moss's memory controller generates a delayed clock signal CLK2 from the controller's clock signal CLK using a programmable delay line 306 to compensate for phase offset errors between CLK and the data strobe signal DQS. (EX1003, ¶182; EX1006, Fig. 3, 6:55-63) The delay value is calibrated during what can be considered a calibration mode, based on the accumulated phase variance 308 between CLK and DQS. (EX1003, ¶182; EX1006, Fig. 3, 6:4-15, 6:64-7:4)

A POSITA would have been motivated to combine Johnson's explicit calibration of strobe signal delay with Moss's programmable delay line for clock signal adjustment, as both references address timing control in memory systems and seek to compensate for phase offsets. (EX1003, ¶183)

### M. Claim 15: "The method according to claim 14, further comprising: during the calibration mode, storing the calibrated timing delay value."

Johnson discloses this claim. (EX1003, ¶184). Johnson's control logic circuit 21 determines optimal delay values for both data and strobe signals during calibration. (EX1003, ¶184, EX1004, 1:69-2:2, 5:61-6:5). A POSITA would have understood that these calibrated delay values are necessarily stored for use during normal operation. (EX1003, ¶184; EX1004, 1:69-2:2, 5:61-6:5).

Even if Johnson did not disclose this claim, Moss does. Moss's memory controller stores calibrated delay values for quick configuration of programmable delay lines, including the delay line 306 used for clock signal adjustment. (EX1003, ¶185).

A POSITA would have been motivated to combine Johnson's explicit calibration and storage of delay values with Moss's use of stored values for quick reconfiguration, as both references address timing control in memory systems and seek to improve signal alignment efficiency. (EX1003, ¶186).

## XI. Ground 2: Obvious over Johnson, in view of Moss, in further view of Liou

### A. Claim 8: "The IC memory controller according to claim 1, further comprising a calibration strobe delay element to impart a calibrated delay to the strobe signal."

Johnson discloses this claim. (EX1003, ¶¶187-190). Johnson teaches a delay circuit 55 that delays the data clock signal DCLK, corresponding to the claimed

strobe signal, as part of the calibration circuitry used to align incoming data with the clock signal. (EX1003, ¶¶187-90; EX1004, at 4:20-27, 4:24-27). The delay imparted by delay circuit 55 is calibrated during a calibration mode to determine the optimal delay for properly sampling incoming data. (EX1003, ¶178; EX1004, at 4:27-41).

Even if Johnson does not disclose this claim Liou does. (EX1003, ¶¶191-93). Liou teaches a first delay circuit 110 that delays the data strobe signal DQS by a controlled delay value, functioning as a calibration strobe delay element. (EX1003, ¶¶191-93; EX1007, at [0023]). The controlled delay value is provided by a delay value controller 106, which can dynamically adjust the delay based on feedback from comparison circuits, allowing real-time calibration to account for factors like temperature and voltage variations. (EX1003, ¶¶191-93; EX1007, at [0007], [0011], [0021-0026]). A POSITA would have been motivated to combine the teachings of Johnson and Liou. *See supra*, § IX.B.

## XII. Ground 3: Obvious over Stubbs, in view of Moss

### A. Claim 1

#### a. Element 1[pre]

Stubbs discloses this limitation. (EX1003, ¶194). Stubbs describes a semiconductor memory device with input/output circuitry that functions as an integral component of an IC memory controller. (EX1003, ¶194; EX1005, Abstract, [0007], [0027-0028], [0032]). Even if Stubbs does not disclose this limitation, Moss does. (*See supra*, §X.A.a; EX1003, ¶195). A POSITA would have been motivated to

combine the teachings of Stubbs and Moss to arrive at the claimed IC memory controller, as both references address high-speed memory interfaces and seek to improve data transfer efficiency. (EX1003, ¶196).

**b. Element 1[a]**

Stubbs discloses this limitation (EX1003, ¶197). Stubbs teaches a first pin to receive a first data signal and a first adjustable delay element to delay the received first data signal and generate a first delayed data signal. (EX1003, ¶197; EX1005, Fig. 4, [0028], [0047]).

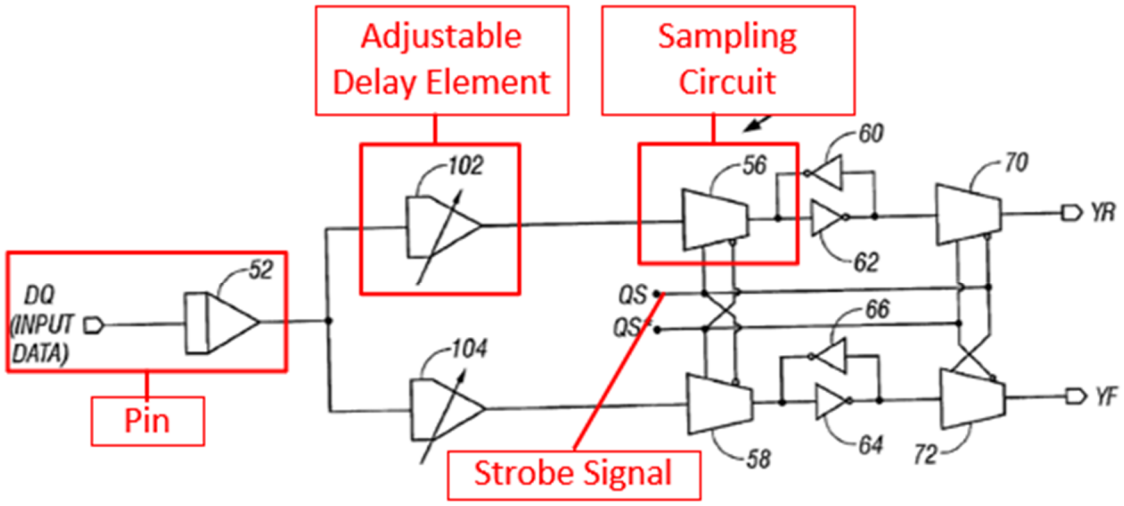



FIGURE 4

(EX1005, Fig. 4 (annotated)). Specifically, Stubbs' write path circuit includes an input buffer that receives data from an external data pin, corresponding to the claimed first pin, and a first delay element coupled to the input buffer's output, which is adjustable and generates a first delayed data signal. (EX1003, ¶197; EX1005, Fig. 4, [0047-0048]). This adjustable delay element allows for independent optimization

of setup and hold times for rising and falling edge data, and can be implemented using various techniques like inverter chains or RC delay circuits, with selectable delay values, enabling fine-tuning for specific system requirements. (EX1003, ¶197; EX1005, [0048], [0050-0053]).

Even if Stubbs does not disclose this limitation, Moss does. (*See supra*, §X.A.b; EX1003, ¶198). A POSITA would have been motivated to combine Stubbs' adjustable delay elements with Moss's memory controller design, as both references address timing control in high-speed memory interfaces, yielding predictable results in enhancing delay precision and adaptability, and providing the known benefits of fine-grained delay adjustment critical in high-performance memory controllers. (EX1003, ¶199).

**c. Element 1[b]**

Stubbs discloses this limitation (EX1003, ¶ 200). Stubbs teaches that the write path circuit shown in Fig. 4 is provided for each input/output (DQ) pin of the memory device, with multiple input/output pins typically present. (EX1003, ¶200; EX1005, [0029], [0047]) For each of these input/output pins, a separate write path circuit is provided, which includes an input buffer and an adjustable delay element, directly corresponding to the claimed second pin and second adjustable delay element. (EX1003, ¶200; EX1005, [0047], [0048])

Even if Stubbs does not disclose this limitation, Moss does. (*See supra*, §X.A.c; EX1003, ¶201)

A POSITA would have been motivated to combine Stubbs' multiple adjustable delay elements with Moss's memory controller design, as both references address timing control in high-speed memory interfaces with multiple data signals. (EX1003, ¶202)

**d. Element 1[c]**

Stubbs discloses this limitation. (EX1003, ¶203-04). Stubbs teaches a pin to receive a strobe signal, where the memory device receives an externally-applied clock signal CLK at an input pin that is used to generate an internal data strobe signal QS/QS for controlling input data sampling. (EX1003, ¶¶203-04; EX1005, at [0005], [0007], [0035-0036]). This dedicated pin allows the memory device to synchronize its internal operations with external system timing, ensuring proper data capture and routing in high-speed memory applications where timing margins are critical. (EX1003, ¶¶194-195; EX1005, at [0004-0007], [0035-0037]).

Even if Stubbs does not disclose this limitation, Moss does. (*See supra*, §X.A.d; EX1003, ¶205).

A POSITA would have been motivated to combine Stubbs' clock signal input pin with Moss's explicit strobe signal pin, as both references address timing control in high-speed memory interfaces, yielding predictable results in enhancing

synchronization precision and providing known benefits of accurate data sampling critical in high-performance memory controllers. (EX1003, ¶206)

**e. Element 1[d]**

Stubbs discloses this limitation. (EX1003, ¶207). Specifically, Stubbs teaches a first pass gate 56 that samples a delayed data signal output from delay element 102 based on a data strobe signal QS/QS*. (EX1003, ¶207; EX1005, Fig. 4, [0037]). The pass gate 56 functions as a sampling circuit by selectively allowing the delayed data signal to pass through to its output under the control of the data strobe signal QS/QS* applied to its control inputs. (EX1003, ¶207; EX1005, [0034], [0036]). This sampling operation is illustrated in Figure 3, which shows the data signal being sampled on the rising edge of the QS strobe signal. (EX1003, ¶207; EX1005, Fig. 3, [0039]).

Even if Stubbs does not disclose this limitation, Moss does. (*See supra*, §X.A.e; EX1003, ¶208)

A POSITA would have been motivated to combine Stubbs' pass gate sampling circuit with Moss's memory controller design, as both references address data sampling in high-speed memory interfaces, and this combination would yield predictable results in enhancing sampling precision, providing the known benefits of accurate data capture critical in high-performance memory controllers. (EX1003, ¶209)

### f. Element 1[e]

Stubbs discloses this limitation. (EX1003, ¶210). Stubbs teaches that the write path circuitry shown in Figure 4, including the sampling circuits, is replicated for each input/output (DQ) pin of the memory device, meaning there is a second sampling circuit for a second data pin. (EX1003, ¶210; EX1005, [0046]). Each data pin has its own pair of sampling circuits (pass gates 56 and 58) to handle the rising-edge and falling-edge data, allowing for parallel processing of multiple data bits and enabling the high data rates required in DDR operation. (EX1003, ¶210; EX1005, [0046], [0029], [0012]).

Even if Stubbs does not disclose this limitation, Moss does. (*See supra*, §X.A.f; EX1003, ¶211).

A POSITA would have been motivated to combine Stubbs' multiple sampling circuits with Moss's memory controller design, as both references address data sampling in high-speed memory interfaces with multiple data signals, yielding predictable results in enhancing sampling precision across multiple data paths. (EX1003, ¶212).

## B. Claim 2

Stubbs discloses this claim. (EX1003, ¶213). Stubbs teaches adjustable delay elements to achieve predetermined timed relationships between delayed data signals and data strobe edges, implying the necessity of storing delay values in non-volatile

storage to maintain these adjusted values across power cycles or resets. (EX1003, ¶213; EX1005, at [0048]). Stubbs also describes a calibration mode for determining delay values, which would require storage for subsequent use during normal operation, and the disclosure of locked-loop circuits with plural serially connected delay elements implies the need for storing delay values to select specific delay elements. (EX1003, ¶213; EX1005, at [0018], [0006-0007]) Storing calibrated delay values allows for quick setup of correct timing relationships without time-consuming recalibration, improving the overall efficiency and reliability of the memory system. (EX1003, ¶213; EX1005, at [0002-0004], [0047-0048])

Even if Stubbs does not disclose this claim, Moss does. (*See supra*, § X.B; EX1003, ¶214)

A POSITA would have been motivated to combine Stubbs' adjustable delay elements with Moss's explicit storage of delay values, as both references address timing control in high-speed memory interfaces, yielding predictable results in enhancing system efficiency by allowing quick reconfiguration of delay values without repeated calibration. (EX1003, ¶215)

### C. Claim 4

Stubbs discloses this claim. (EX1003, ¶216). Stubbs teaches an IC memory controller that delays first and second data signals to compensate for timing offset between the received signals, using separate adjustable delay elements for rising

edge data (first data signal) and falling edge data (second data signal). (EX1003, ¶216; EX1005, Fig. 4). These delay elements allow independent adjustment of setup and hold times for rising and falling edge data, achieving a predetermined timed relationship between the delayed data signals and the rising and falling edges of the data strobe signal, which corresponds to the specified setup and hold window for the device. (EX1003, ¶216; EX1005, [0018], [0047]). This adjustment compensates for timing offsets between the received first and second data signals. (EX1003, ¶216).

Even if Stubbs does not disclose this claim, Moss does. (*See supra*, §X.C; EX1003, ¶217).

A POSITA would have been motivated to combine Stubbs' adjustable delay elements with Moss's timing offset compensation techniques, as both references address timing control in high-speed memory interfaces, yielding predictable results in enhancing signal alignment precision and providing the known benefits of improved timing margins critical in high-performance memory controllers. (EX1003, ¶218).

### D. Claim 5

Stubbs discloses this claim. (EX1003, ¶¶219-20). Stubbs teaches a write path circuit for a memory device with multiple data input pins and associated delay elements that correspond to the claimed first and second timing signal delay elements associated with the first and second pins. (EX1003, ¶¶219-20; EX1005,

Fig. 4, [0046-0047]) While Stubbs primarily discusses delaying data signals, it also teaches that the same delay elements can be used to delay the strobe signal, making it obvious to a POSITA that the delay elements could delay either the data signals or the strobe signal to achieve the desired timing relationship. (EX1003, ¶¶210-20; EX1005, [0047-0048]) This arrangement allows independent optimization of setup and hold times for rising and falling edge data, enabling memory devices to meet more stringent timing specifications by compensating for signal propagation differences. (EX1003, ¶¶219-20; EX1005, [0015-0016], [0047-0048])

Even if Stubbs does not disclose this claim, Moss does. (*See supra*, §X.D; EX1003, ¶221)

A POSITA would have been motivated to combine Stubbs' adjustable delay elements with Moss's explicit timing signal delay elements, as both references address timing control in high-speed memory interfaces, yielding predictable results. (EX1003, ¶222)

### E. Claim 6

Stubbs discloses this claim. (EX1003, ¶223). Stubbs teaches delay elements comprising locked-loop circuits having plural serially connected delay elements, implemented as a network of series-connected delay elements 122, 124, 126, and 128 that form a locked-loop circuit generating precisely timed delayed versions of the input data signal. (EX1003, ¶223; EX1005, [0051-0053], Fig. 5). This

configuration allows for fine-grained control over the delay interval by selecting different tap points along the series, enabling precise timing adjustments to optimize setup and hold times for both rising and falling edge data in a DDR memory controller. (EX1003, ¶223; EX1005, [0053-0054]). The locked-loop circuit with plural serially connected delay elements provides advantages such as independent adjustment of rising and falling edge data timing and flexibility in accommodating various system timing requirements. (EX1003, ¶223; EX1005, [0006], [0015], [0048], [0053]).

Even if Stubbs does not disclose this claim, Moss does. (*See supra*, §X.E; EX1003, ¶224)

A POSITA would have been motivated to combine Stubbs' locked-loop circuits with Moss's delay elements, as both references address timing control in high-speed memory interfaces, and this combination would yield predictable results in enhancing delay precision and adaptability, providing the known benefits of fine-grained delay adjustment critical in high-performance memory controllers. (EX1003, ¶225).

### F. Claim 7

Stubbs discloses this claim. (EX1003, ¶226). Stubbs teaches using first and second delay values to select delay elements of first and second delay circuits in its write data path circuit, which includes adjustable delay elements for independently

controlling the timing of rising and falling edge data. (EX1003, ¶226; EX1005, [0047-0048]). The delay circuit comprises series-connected delay elements with multiple tap points, where selecting different tap points for rising and falling edge data paths corresponds to using first and second delay values to select delay elements. (EX1003, ¶226; EX1005, [0051-0053], Fig. 5). This selective coupling of delay elements based on chosen tap points is equivalent to using delay values to select delay elements of respective delay circuits. (EX1003, ¶226; EX1005, [0053]).

Even if Stubbs does not disclose this claim, Moss does. (*See supra*, §X.F). (EX1003, ¶227)

A POSITA would have been motivated to combine Stubbs' selectable delay elements with Moss's delay value selection technique, as both references address timing control in high-speed memory interfaces, and this combination would yield predictable results in enhancing delay precision and adaptability, providing the known benefits of fine-grained delay adjustment critical in high-performance memory controllers. (EX1003, ¶228)

### G. Claim 9

Stubbs discloses this claim. (EX1003, ¶¶229-30). Stubbs teaches a calibration circuit that operates in a calibration mode to determine first and second delay values for adjusting the timing of data signals in a memory controller. (EX1003, ¶¶229-30; EX1005, at [0018], [0019]). The calibration circuit optimizes setup and hold times

for rising edge and falling edge data relative to the data strobe signal, allowing independent adjustment of timing for rising and falling edge data to achieve proper alignment with the data strobe signal. (EX1003, ¶¶229-30; EX1005, at [0015], [0018-0019]). While Stubbs does not explicitly label the calibration circuit as a separate component, a POSITA would have understood that the described functionality for determining and applying delay values in a calibration mode necessarily requires dedicated calibration circuitry within the memory controller. (EX1003, ¶¶229-30; EX1005, at [0018-0019]).

Even if Stubbs does not disclose this claim, Moss does. (*See supra*, §X.G). (EX1003, ¶232).

A POSITA would have been motivated to combine Stubbs' calibration functionality with Moss's explicit calibration circuit, as both references address timing control in high-speed memory interfaces, yielding predictable results in enhancing delay precision and adaptability. (EX1003, ¶232).

## H. Claim 10

### a. Limitation 10[pre]

Stubbs discloses this limitation. (EX1003, ¶233). Stubbs teaches a method of operation in an IC memory controller, including controller components such as control circuit 12, addressing circuit 40, and input/output circuit 30, which manage data flow to and from memory banks 20. (EX1003, ¶233; EX1005, at [0028], Fig.

1). The method involves receiving data signals, aligning them with a strobe signal, and applying delays to ensure proper timing relationships in a double-data-rate system, addressing critical timing issues in high-speed data transfer and ensuring accurate data capture and processing. (EX1003, ¶223; EX1005, at [0012-0015], [0041-0044]).

Even if Stubbs does not disclose this limitation, Moss does. (*See supra*, §X.H.a; EX1003, ¶234)

A POSITA would have been motivated to combine Stubbs' method of operation with Moss's explicit IC memory controller implementation, as both references address high-speed memory interfaces and seek to improve data transfer efficiency, yielding predictable results in enhancing memory controller performance and providing the known benefits of precise timing control critical in high-speed memory interfaces. (EX1003, ¶235)

**b. Limitation 10[a]**

Stubbs discloses this limitation. (EX1003, ¶¶236-38). Stubbs teaches receiving first and second data signals from a memory device at respective first and second pins, where the memory device contains multiple input/output pins (DQ0-DQ7) for receiving data signals in parallel. (EX1003, ¶¶236-38; EX1005, [0029]). In Stubbs' DDR SDRAM architecture, data is received on both rising and falling clock edges, with one pin receiving data on the rising edge and another on the falling

edge, effectively doubling the data transfer rate. (EX1003, ¶¶236-38; EX1005, [0012], [0029]). The received data signals propagate from input buffers through adjustable delay elements before being captured by pass gates controlled by the data strobe signal, allowing for precise timing adjustments. (EX1003, ¶¶236-38; EX1005, [0037-0041], Fig. 4).

Even if Stubbs does not disclose this limitation, Moss does. (*See supra*, §X.H.b; EX1003, ¶239).

A POSITA would have found it obvious to combine Johnson, Moss, and Stubbs. Combining these features would yield predictable results in enhancing data reception efficiency, providing the known benefits of increased data bandwidth critical in high-performance memory controllers. (EX1003, ¶240; EX1006, at 5:51-55; EX1004, at [0004]).

**c. Limitation 10[b]**

Stubbs discloses this limitation. (EX1003, ¶234). Stubbs teaches aligning received first and second data signals with a strobe signal by imparting delays corresponding to first and second delay values through separate delay elements for rising and falling edge data. (EX1003, ¶233; EX1005, at [0047], Fig. 4). Specifically, Stubbs' write data path circuit includes adjustable delay elements 102 and 104 that impart independently adjustable first and second delays to rising and falling edge data paths respectively, which are then aligned with a strobe signal QS/QS*

controlling pass gates. (EX1003, ¶233; EX1005, at [0047-0048], Fig. 4). This circuitry is replicated for each DQ pin, allowing for multiple instances of first and second delays applied to separate data signals. (EX1003, ¶233; EX1005, at [0046-0047]).

Even if Stubbs does not disclose this limitation, Moss does. (*See supra*, *See supra*, §X.H.c; EX1003, ¶234)

A POSITA would have been motivated to combine Stubbs' adjustable delay elements with Moss's signal alignment techniques, as both references address timing control in high-speed memory interfaces, yielding predictable results in enhancing signal alignment precision and improving timing margins critical in high-performance memory controllers. (EX1003, ¶235)

### I. Claim 11

Stubbs discloses this claim. (EX1003, ¶244). During calibration, Stubbs teaches determining delay values for aligning rising and falling edge data signals with a data strobe signal and storing these values for use during normal operation. (EX1003, ¶244; EX1005, at [0018-0019]). The calibration process optimizes setup and hold times for rising and falling edge data independently by adjusting separate delay elements for each path, and while not explicitly stated, a person of ordinary skill would have understood that this calibration occurs for each DQ pin. (EX1003, ¶244; EX1005, at [0015], [0046-0047]). During normal operation, the stored delay

values adjust the timing of incoming data signals, maintaining proper setup and hold times for both rising and falling edge data across all pins. (EX1003, ¶244; EX1005, at [0019], [0047-0048]).

Even if Stubbs does not disclose this limitation, Moss does. (*See supra*, §X.I; EX1003, ¶245)

A POSITA would have been motivated to combine Stubbs' calibration process with Moss's explicit storage of delay values, as both references address timing control in high-speed memory interfaces, and this combination would yield predictable results in enhancing system efficiency by allowing quick reconfiguration of delay values without repeated calibration. (EX1003, ¶246).

### J. Claim 12

Stubbs discloses this claim. (EX1003, ¶244). Stubbs teaches retrieving stored first and second delay values during a receiving mode to impart first and second delays, using separate adjustable delay elements for rising and falling edge data. (EX1003, ¶244; EX1005, at [0047], Fig. 4). These delay values are determined during calibration, stored, and later retrieved and applied during normal operation to maintain optimized setup and hold times. (EX1003, ¶244; EX1005, at [0018], [0047]). Stubbs' write data path circuit is replicated for each DQ pin, allowing per-pin optimization and ensuring proper alignment of data with the strobe signal for both rising and falling edge data. (EX1003, ¶245; EX1005, at [0015], [0047-0048]).

Even if Stubbs does not disclose this claim, Moss does. (*See supra*, § X.J; EX1003, ¶249).

A POSITA would have been motivated to combine Stubbs' use of stored delay values with Moss's explicit retrieval process, as both references address timing control in high-speed memory interfaces, yielding predictable results in enhancing system efficiency by allowing quick reconfiguration of delay values without repeated calibration. (EX1003, ¶250).

### K. Claim 13

To the extent this claim is not indefinite, Stubbs discloses this claim. (EX1003, ¶251). Stubbs teaches delaying first and second data signals by first and second delay values using separate adjustable delay elements 102 and 104 for each input/output (DQ) pin. (EX1003, ¶251; EX1005, at [0046-0047], Fig. 4). These delay elements introduce adjustable delays into the propagation of data signals, allowing for independent optimization of timing for different data signals. (EX1003, ¶251; EX1005, at [0047-0048]). By providing separate delays for different data paths, Stubbs enables different delay times for data signals arriving at pass gates 56 and 58, with the delay elements adjusted to achieve predetermined timed relationships between the delayed data signals and the data strobe signals, optimizing setup and hold times. (EX1003, ¶251; EX1005, at [0047-0048]).

Even if Stubbs does not disclose this claim, Moss does. (*See supra*, §X.K; EX1003, ¶252).

A POSITA would have been motivated to combine Stubbs' adjustable delay elements with Moss's delay implementation, as both references address timing control in high-speed memory interfaces. (EX1003, ¶250).

### L. Claim 14

Stubbs discloses this claim. (EX1003, ¶254). Stubbs teaches determining and storing delay values for data signals relative to a data strobe signal to achieve proper setup and hold times during a calibration mode. (EX1003, ¶254; EX1005, at [0018-0019]). While Stubbs primarily focuses on delaying data signals, it also discloses using adjustable delay elements for both data and strobe signals to achieve proper timing. (EX1003, ¶254; EX1005, at [0007], [0010]). A POSITA would have found it obvious to apply the same calibration technique to the strobe signal, as this would provide finer control over the relative timing between data and strobe, allowing for more precise optimization of setup and hold times across different operating conditions. (EX1003, ¶254).

Even if Stubbs does not disclose this limitation, Moss does. Moss discloses this limitation. (*See supra*, §X.L; EX1003, ¶255).

A POSITA would have been motivated to combine Stubbs' calibration techniques with Moss's explicit calibration of strobe signal delay, as both references

address timing control in high-speed memory interfaces, and this combination would yield predictable results in enhancing timing precision, providing the known benefits of adaptive timing control critical in high-speed memory interfaces. (EX1003, ¶256).

### M. Claim 15

Stubbs discloses this claim. (EX1003, ¶257). Stubbs teaches storing calibrated delay values during a calibration mode for later use during normal operation of the memory device. (EX1003, ¶257; EX1005, at [0018-0019]). While Stubbs primarily focuses on storing delay values for data signals, the same principle would apply to storing a calibrated timing delay value for the strobe signal. (EX1003, ¶257). This storage allows optimized delay settings to be maintained and quickly applied without needing to recalibrate each time the device is used, and enables adaptive behavior in the memory system. (EX1003, ¶257; EX1005, at [0009], [0018], [0019]).

Even if Stubbs does not disclose this claim, Moss does. (*See supra*, §X.M; EX1003, ¶258).

A POSITA would have been motivated to combine Stubbs' calibration techniques with Moss's explicit storage of calibrated delay values, as both references address timing control in high-speed memory interfaces. (EX1003, ¶259)

## XIII. Ground 4: Obvious over Stubbs, in view of Moss, in further view of Liou.

### A. Claim 8

Stubbs discloses this claim (EX1003, ¶260). Stubbs teaches a synchronous double-data-rate semiconductor memory device with write path circuitry including delay elements for adjusting timing of data and strobe signals. (EX1003, ¶260; EX1005, at Abstract, [0007-0010]). While Stubbs does not explicitly disclose a calibration strobe delay element to impart a calibrated delay to the strobe signal, this feature would have been obvious to a POSITA based on Stubbs' teachings of adjusting timing of both data and strobe signals to achieve proper alignment for sampling data. (EX1003, ¶260; EX1005, at [0007], [0018]). Stubbs' write path circuitry could be readily modified to include a calibration strobe delay element in the path of the DQS strobe signal before it reaches the pass gates 56 and 58, allowing for fine-tuning of the strobe signal timing relative to the delayed data signals. (EX1003, ¶260; EX1005, at Fig. 4, [0047]).

Even if Stubbs does not disclose this claim, Liou does. (*See supra*, § XI.A; EX1003, ¶261).

A POSITA would have been motivated to incorporate Liou's explicit calibration strobe delay element into Stubbs' memory device, as both references address timing control in high-speed memory interfaces, and this combination would

yield predictable results in enhancing timing precision, providing the known benefits of adaptive timing control critical in high-speed memory interfaces. (EX1003, ¶262).

## XIV. Ground 5: Obvious over Stubbs, in view of Moss, in further view of Johnson

### A. Claim 10

#### a. Limitation 10[pre]

Stubbs discloses this limitation. (*See supra*, § XII.A.a; EX1003, ¶263). Even if Stubbs does not disclose this limitation, Moss does. (*See supra*, § X.A.a; EX1003, ¶264). Even if the combination of Stubbs and Moss does not disclose this limitation, Johnson does. (*See supra*, § X.A.a; EX1003, ¶265).

A POSITA would have found it obvious to combine the teachings of Johnson, Stubbs, and Moss to arrive at a method of operation in an IC memory controller as claimed. (EX1003, ¶266). Johnson teaches a memory controller that executes specific procedures to manage data flow and timing in a memory system, including initialization, calibration, and ongoing data transfer operations. (EX1003, ¶266; EX1004, at 3:34-41, 4:28-43). Stubbs teaches a write data path circuit within a memory controller that aligns received data signals with a strobe signal by applying independently adjustable delays, while Moss explicitly describes a method implemented within a memory controller circuit to realign read data returned from memory components, compensating for phase shifts due to propagation delays and other factors. (EX1003, ¶266; EX1005, at [0047-0048], Fig. 4; EX1006, at Abstract,

5:51-55, 6:36-7:46). A POSITA would have been motivated to incorporate the specific alignment techniques of Stubbs and Moss into Johnson's memory controller operations to improve data timing accuracy and system performance across various operating conditions. (EX1003, ¶266; EX1004, at 2:47-53; EX1005, at [0016]; EX1006, at 1:43-54).

**b. Limitation 10[a]**

Stubbs discloses this limitation. (*See supra*, § XII.A.b; EX1003, ¶267). Even if Stubbs does not disclose this limitation, Moss does. (*See supra*, §X.A.b; EX1003, ¶268). Even if the combination of Stubbs and Moss does not disclose this limitation, Johnson does. (*See supra*, §X.A.b; EX1003, ¶269).

A POSITA would have been motivated to combine Johnson and Moss to arrive at this limitation. (EX1003, ¶268; *See supra*, §X.A.b). A POSITA would also be motivated to combine Stubbs and Moss to arrive at this limitation. (EX1003, ¶268; *See supra,* §XII.A.b). Furthermore, a POSITA would have been motivated to combine Stubbs, Moss, and Johnson to arrive at the claimed limitation for substantially the same reasons as discussed with respect to those combinations. (EX1003, ¶268).

**c. Limitation 10[b]**

Stubbs discloses this limitation. (EX1003, ¶269; *See supra*, §XII.A.c). Even if Stubbs does not disclose this limitation, Moss does. (EX1003, ¶270; *See supra*, §

§X.A.c). Even if the combination of Stubbs and Moss does not disclose this limitation, Johnson does. (EX1003, ¶271; *See supra*, §X.A.c).

A POSITA would have been motivated to combine Johnson and Moss to arrive at this limitation. (EX1003, ¶272; *See supra*, § §X.A.c). A POSITA would also be motivated to combine Stubbs and Moss to arrive at this limitation. (EX1003, ¶272; *See supra,* §XII.A.b). Furthermore, a POSITA would have been motivated to combine Stubbs, Moss, and Johnson to arrive at the claimed limitation for substantially the same reasons as discussed with respect to those combinations. (EX1003, ¶272).

**d. Limitation 10[c]**

Stubbs discloses this limitation. (EX1003, ¶273; *See supra*, § §XII.A.d). Even if Stubbs does not disclose this limitation, Moss does. (EX1003, ¶274; *See supra*, §X.A.c). Even if the combination of Stubbs and Moss does not disclose this limitation, Johnson does. (EX1003, ¶275; *See supra*, §X.A.c)

A POSITA would have been motivated to combine Johnson and Moss to arrive at this limitation. (EX1003, ¶276; *See supra*, §X.A.c) A POSITA would also be motivated to combine Stubbs and Moss to arrive at this limitation. (EX1003, ¶276; *See supra,* § XII.A.c) Furthermore, a POSITA would have been motivated to combine Stubbs, Moss, and Johnson to arrive at the claimed limitation for

substantially the same reasons as discussed with respect to those combinations. (EX1003, ¶276)

### B. Claim 11

Stubbs discloses this claim. (EX1003, ¶277; *See supra*, XII.B). Even if Stubbs does not disclose this claim, Moss does. (EX1003, ¶278; *See supra*, §X.B). Even if the combination of Stubbs and Moss does not disclose this claim, Johnson does. (EX1003, ¶279; *See supra*, §X.B)

A POSITA would have been motivated to combine Johnson and Moss to arrive at this claim. (EX1003, ¶280; *See supra*, §X.B) A POSITA would also be motivated to combine Stubbs and Moss to arrive at this claim. (EX1003, ¶280; *See supra,* §XII.B) Furthermore, a POSITA would have been motivated to combine Stubbs, Moss, and Johnson to arrive at the claim for substantially the same reasons as discussed with respect to those combinations. (EX1003, ¶280)

### C. Claim 12

Stubbs discloses this claim. (*See supra*, §XII.C). (EX1003, ¶281). Even if Stubbs does not disclose this claim, Moss does. (*See supra*, §X.C). (EX1003, ¶282). Even if the combination of Stubbs and Moss does not disclose this claim, Johnson does. (*See supra*, §X.C). (EX1003, ¶283)

A POSITA would have been motivated to combine Johnson and Moss to arrive at this claim. (*See supra*, §X.C) A POSITA would also be motivated to combine

Stubbs and Moss to arrive at this limitation. (*See supra,* §XII.C) Furthermore, a POSITA would have been motivated to combine Stubbs, Moss, and Johnson to arrive at the claimed limitation for substantially the same reasons as discussed with respect to those combinations. (EX1003, ¶284)

## XV. PTAB Discretion Should Not Preclude Institution

### A. Board Should Not Exercise Discretion Under 35 U.S.C. § 314(a)

The factors described in *Apple, Inc. v. Fintiv, Inc*, IPR2020-00019, Paper 11 (PTAB March 20, 2020) (Precedential) ("*Fintiv-I*") favor institution.

As of this Petition, discovery has only recently opened in the District Court Litigation and, although a stay motion has not yet been filed, Petitioner intends to promptly file a stay motion in the event of IPR institution. The Board has treated related factors as neutral after declining to speculate on the outcome of a stay motion. *See, e.g., HP Inc. v. Slingshot Printing LLC*, IPR2020-01084, Paper 13 at 9 (PTAB Jan. 14, 2021) ("HP") (instituting IPR after declining to speculate on likelihood of a stay).

Institution is strongly favored where, as here, Petitioner has been "exceptionally diligent" in filing. *Micron Tech., Inc. v. Godo Kaisha IPR Bridge 1*, IPR2020-01007, Paper 15 at 15-16 (PTAB Dec. 7, 2020). The Board has made clear that "it is often reasonable for a Petitioner to wait to file its petition until it learns which claims are being asserted against it in the parallel proceeding," and here,

Petitioner filed its Petition less than eight weeks after receiving infringement contentions. *Fintiv-I* at 11. In light of Petitioner's diligence, any argument comparing the timing of respective milestones between this proceeding and the District Court Litigation would be premature.

If Patent Owner raises §314(a) arguments in a Preliminary Response, Petitioner respectfully requests the opportunity to reply prior to institution, in order to address expected schedules at that time and whether a stipulation limiting arguments to be made in the District Court Litigation would be appropriate.

### B. Board Should Not Exercise Discretion Under 35 U.S.C. § 325(d)

The Board should not deny institution under § 325(d) because none of the primary references relied upon (Johnson and Stubbs) were made of record during prosecution of the '608 Patent. Further, while Moss and Liou were made of record during the prosecution, neither was relied upon or considered relevant by the examiner. Further, none of the arguments presented here appear to have been considered during the prosecution, and thus are not duplicative of any prior proceeding. *See Edwards Lifesciences Corp. v. Boston Scientific SciMed, Inc.,* IPR2017-01295, Paper 9, at 25-27 (PTAB Oct. 25, 2017) (institution not denied when Petition's and Examiner's reliance on a prior art reference was substantially different).

## XVI. Conclusion

Petitioner requests institution of an IPR for the Challenged Claims of the '608 Patent.

Respectfully submitted,

Dated: August 9, 2024

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## CERTIFICATION UNDER 37 C.F.R. § 42.24

Under the provisions of 37 C.F.R. § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,328 words, which is less than the 14,000 allowed under 37 C.F.R § 42.24.

Dated: August 9, 2024

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**CERTIFICATE OF SERVICE UNDER 37 C.F.R. § 42.105**

I hereby certify that on August 09, 2024, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,111,608 and supporting exhibits to be served via FedEx Express® on the Patent Owner at the following correspondence address of record as listed on the USPTO Patent Center:

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