UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES) INC.
Petitioner

v.

INTELLECTUAL VENTURES II LLC
Patent Owner

Case No. IPR2024-01226
Patent No. 7,646,835 B1

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,646,835 B1

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CHALLENGED CLAIMS

Claim 1	
1.P	A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, the method comprising:
1.1	generating command signals to access an integrated circuit component
1.2	accessing data signals to convey data for the integrated circuit component;
1.3	accessing sampling signals to control sampling of the data signals; and
1.4.a	systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device,
1.4.b	wherein the valid operation range includes an optimal operation point for the integrated circuit device.
Claim 2	
2	The method of claim 1, wherein the integrated circuit device comprises a DRAM component.
Claim 3	
3	The method of claim 2, wherein said altering is performed by a memory controller coupled to the DRAM component.
Claim 4	
4	The method of claim 2, wherein the DRAM component comprises a DDR DRAM component.
Claim 5	
5	The method of claim 4, wherein the data signals comprise a plurality of data bus (DQ) signals for the DDR DRAM component.

Claim 6	
6	The method of claim 5, wherein the sampling signals comprise a plurality of sampling bus (DQS) signals for the DDR DRAM component.
Claim 7	
7.P	A system for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, the system comprising:
7.1	a controller configured to generate command signals for accessing an integrated circuit component;
7.2.a	a delay calibrator integrated within the controller and
7.2.b	configured to access data signals conveying data for the integrated circuit device and
7.2.c	to access sampling signals for controlling sampling of the data signals,
7.3.a	wherein the delay calibrator is further configured to systematically alter a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device; and
7.3.b	wherein the valid operation range includes an optimal operation point for the integrated circuit device.
Claim 8	
8	The system of claim 7, wherein the integrated circuit device comprises a DRAM component.
Claim 9	
9	The system of claim 8, wherein the DRAM component comprises a DDR DRAM component.
Claim 10	

10	The system of claim 9, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.
Claim 11	
11	The system of claim 10, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.
Claim 12	
12.P	In a memory controller, a method for finding an operating mode for a DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, the method comprising:
12.1	generating command signals to access a DRAM component;
12.2	accessing data signals to convey data for the DRAM component;
12.3	accessing sampling signals to control sampling of the data signals; and
12.4	systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operating range of the DRAM component.
Claim 13	
13.1	The method of claim 12, further comprising: performing a coarse calibration by altering the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a large step interval to determine if the valid operating range of the DRAM component exists; and
13.2	if the valid operating range exists, then performing a fine calibration by altering the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a small step interval to identify an optimal operating mode of the DRAM component.
Claim 14	

14	The method of claim 13, wherein said performing a coarse calibration comprises simultaneously varying each of the phase shift of the command signal, the phase shift of the data signal, and the phase shift of the sampling signal by a five percent step increase.
Claim 15	
15	The method of claim 13, wherein said performing a fine calibration comprises varying each of the phase shift of the command signal, the phase shift of the data signal, and the phase shift of the sampling signal one at a time by a two percent step increase.
Claim 16	
16	The method of claim 13, further comprising configuring the memory controller to operate the DRAM component in the optimal operating mode.
Claim 17	
17	The method of claim 12, wherein the DRAM component comprises a DDR DRAM component.
Claim 18	
18	The method of claim 17, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.
Claim 19	
19	The method of claim 18, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.
Claim 20	
20.P	A computer readable media having stored thereon, computer-executable instructions that, if executed by a processor, cause the processor to perform a method for finding an operating mode for a DDR DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DDR DRAM component, the method comprising:

20.1	generating command signals to access a DDR DRAM component;
20.2	accessing DQ signals to convey DQ signals for the DDR DRAM component;
20.3	accessing DQS signals to control sampling of the DQ signals; and
20.4	systematically altering a phase shift of the command signals, a phase shift of the DQ signals, and a phase shift of the DQS signals to determine a valid operating range of the DDR DRAM component.
Claim 21	
21.1	The computer readable media of claim 20, wherein the method further comprises: performing a coarse calibration by altering the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a large step interval if the valid operating range of the DDR DRAM component exists; and
21.2	if the valid operating range exists, then performing a fine calibration by altering the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a small step interval to identify an optimal operating mode of the DDR DRAM component.
Claim 22	
22	The computer readable media of claim 21, wherein the method further comprises configuring the memory controller to operate the DRAM component in the optimal operating mode.
Claim 23	
23.P	In a memory controller, a method for finding an operating mode for a DDR DRAM component coupled to a PCB (printed circuit board) by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DDR DRAM component, the method comprising:
23.1	generating command signals to access a DDR DRAM component;

23.2	accessing data signals to convey data for the DDR DRAM component;
23.3	accessing sampling signals to control sampling of the data signals; and
23.4	systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals transmitted via a PCB to determine a valid operating range of the DDR DRAM component.

I. INTRODUCTION

Lenovo (United States), Inc. ("Petitioner") respectfully requests *inter partes* review ("IPR") of claims 1-23 ("Challenged Claims"[1]) of U.S. Patent No. 7,646,835 ("'835 Patent").

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner hereby names Lenovo (United States) Inc. as a real-party-in-interest and, solely because it is named as a defendant in the co-pending district court case listed below, further identifies Lenovo Group Ltd. as a real party-in-interest.

B. Related Matters

Intellectual Ventures I LLC *et al.* has asserted the '835 Patent against Lenovo Group Ltd. in *Intellectual Ventures I LLC et al. v. Lenovo Group Limited*, 6:23-cv-307 (WDTX) ("co-pending litigation").

The '835 Patent is also asserted in the following cases:

- *Intellectual Ventures I LLC et al. v. OnePlus Technology (Shenzen) Co., Ltd*., No. 6-23-cv-00290 (WDTX, filed April 20, 2023);

[1] A subset of the Challenged Claims are being asserted (and at issue) in the co-pending litigation.

- *Intellectual Ventures I LLC et al. v. Zebra Technologies Corporation,* No. 6-23-cv-00292 (WDTX, filed April 20, 2023);
- *Intellectual Ventures II LLC v. Lenovo Group Limited*, No. 6-23-cv-00068 (WDTX, filed February 2, 2023, terminated on April 26, 2023).

C. Counsel and Service Information

Lead counsel is Dinesh Melwani (Reg. No. 60,670). Back-up counsel are Ankit Aggarwal (Reg. No. 67,882) and William Uhr (Reg. No. 71,282). Service information is: Bookoff McAndrews, PLLC, 2000 Pennsylvania Avenue NW Suite 4001, Washington, DC 20006; Tel.: 202.808.3497; Fax.: 202.450.5538; email: docketing@bomcip.com, dmelwani@bomcip.com, aaggarwal@bomcip.com, and wuhr@bomcip.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-5906.

IV. GROUNDS FOR STANDING

Petitioner certifies that the ’835 Patent is available for review and Petitioner is not barred/estopped from requesting review on these grounds. 37 C.F.R. §42.104(a).

V. PRECISE RELIEF REQUESTED AND GROUNDS

A. Identification of Challenge[2]

Petitioner requests the Challenged Claims to be found unpatentable based on the following grounds:

1. *Ground 1:*

Claims 1-23 are unpatentable under 35 U.S.C. §103 as obvious over U.S. Patent No. 6,434,081 ("*Johnson*") in view of U.S. Patent No. 6,629,222 ("*Jeddeloh*").

2. *Ground 2:*

Claims 1, 2, 3, 7, 8, and 12 are unpatentable under 35 U.S.C. §103 as obvious over *Johnson* in view of U.S. Patent No. 6,115,318 ("*Keeth*").

3. *Ground 3:*

Claims 4-6, 9-11, and 13-19 are unpatentable under 35 U.S.C. §103 as obvious over *Johnson* in view of *Jeddeloh* and in view of *Keeth*.

[2] For each Ground, Petitioner does not rely on any reference other than those listed here. Other references are discussed to show the state of the art at the time of the invention. *See Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1365 (Fed. Cir. 2015).

VI. LEVEL OF ORDINARY SKILL

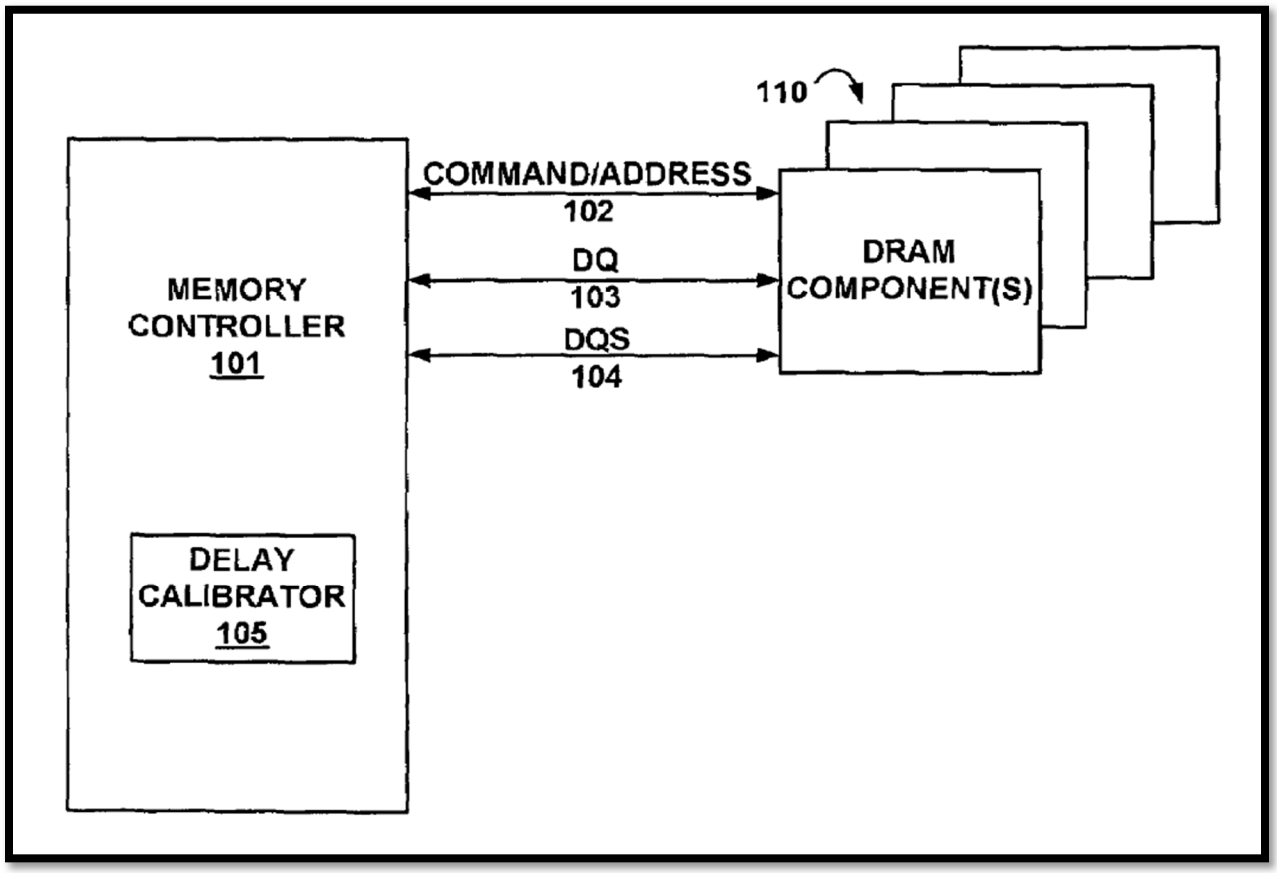
As of November 17, 2003, a person having ordinary skill in the art ("POSITA") would have had a bachelor's degree in electrical engineering, computer engineering, or the equivalent, and two to three years of experience designing high-speed computer memory devices. More practical experience could also substitute for formal education, while a higher level of education could substitute for practical experience. Ex-1002, ¶¶31-35.

VII. SUMMARY OF THE '835 PATENT

A. '835 Patent

The '835 Patent describes calibrating intra-cycle timing relationships for integrated circuit devices. Ex-1001, Abstract. To ensure that critical timing specifications remain within critical specification parameters, automatic calibration of intra-cycle timing relationships for sampling signals of an integrated circuit device are provided. *Id.*, 1:34-37; Ex-1002, ¶55.

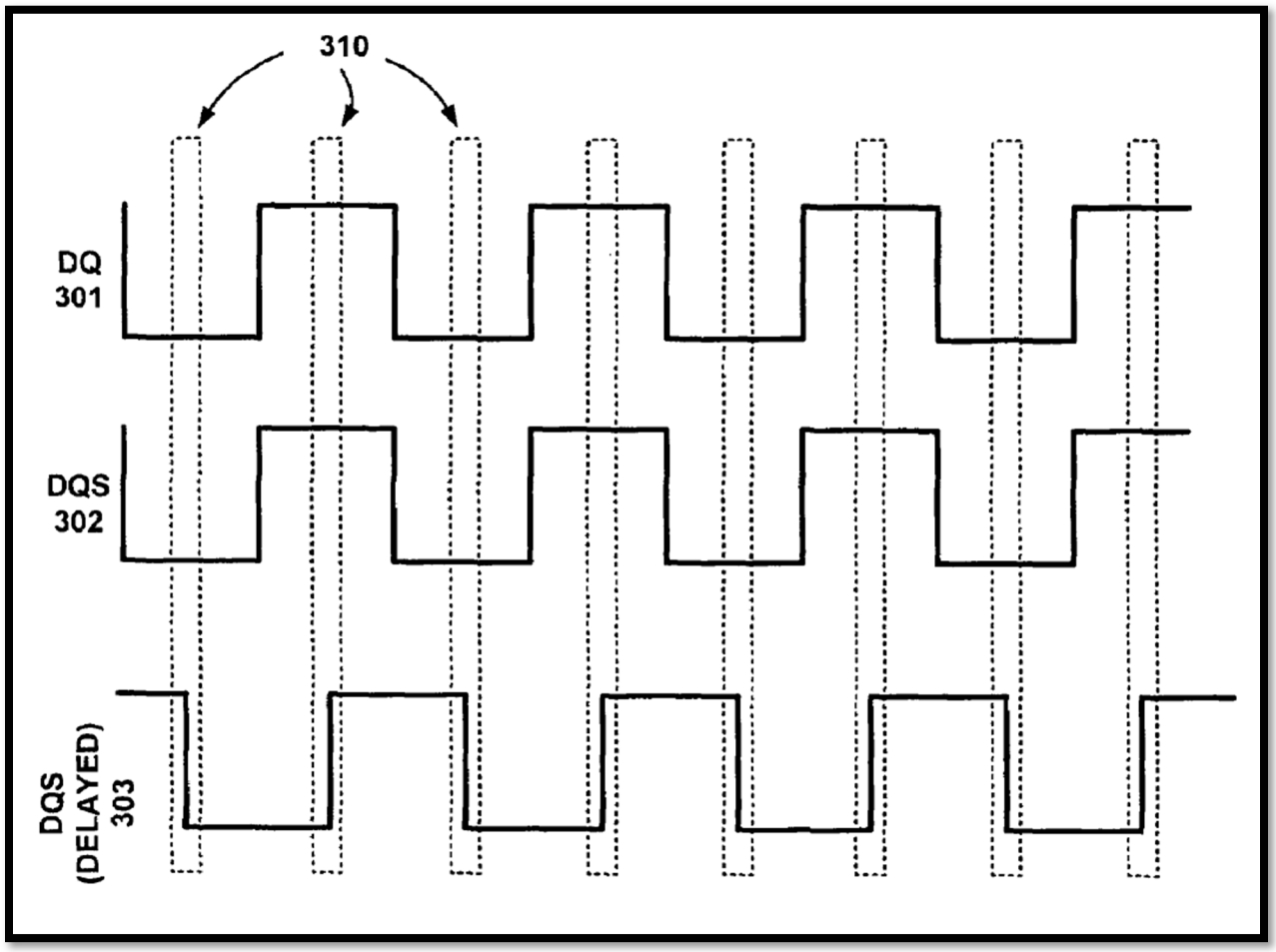
As shown below, memory system 100 of the '835 Patent includes a memory controller 101 with a delay calibrator 105. Ex-1001, 2:63-64. The memory controller 101 is coupled to a plurality of DRAM components 110 via: a) a command/address bus 102; b) a data bus ("DQ"); and c) a sampling signal bus ("DQS"). *Id.*, 2:64-3:2; Ex-1002, ¶¶56-57.



Ex-1001, 2; Ex-1002, ¶¶56-57.

The ’835 Patent states that the memory system “implements a method for automatically calibrating intra-cycle timing relationships between command signals of the command/address bus 102, data signals of the DQ bus 103, and sampling signals of the DQS bus 104.” Ex-1001, 3:3-6. Also, “each of the DRAM components 110 comprise the integrated circuit device for which the calibration adjustments are performed,” and the memory controller 101 performs the adjusting. *Id.*, 3:6-9; Ex-1002, ¶¶57-58.

Figure 3, reproduced below, depicts relative timings of the command/address signals, the DQ signals, and the DQS signals. Ex-1002, ¶59. Timing diagram 300 shows a DQ signal 301 and a DQS signal 302 during a read transaction. Ex-1001, 4:53-54. The rising and falling edges of DQS 302 are aligned with the rising and falling edges of the DQ signal 301. *Id.*, 4:56-58. To align sampling windows with rise-and-hold times of the DQ signal 301, a 90° phase shift is performed to "place the sampling windows 310 at the center of the rise-and-hold times of DQ 301 (e.g., shown as DQS delayed 303)." *Id.*, 4:59-61. DQS 303 is delayed such that rising and falling edges are centered to rise-and-hold times of DQ signal 301:



Id., 4; Ex-1002, ¶60.

The phase-shifted DQS signal 303 is generated by the delay calibrator 105 during an automatic calibration process. Ex-1002, ¶60. During calibration, a phase relationship between signals is automatically adjusted to calibrate the operation of the DRAM components 110. *Id.* The automatic calibration process purportedly increases the reliability rate of computer systems and can be used to increase the maximum obtainable performance of such computer systems. Ex-1001, 3:58-64; Ex-1002, ¶¶61-62.

Optimal operation of DRAM components is allegedly achieved by calibrating intra-cycle timing relationships between command/address signals, DQ signals, and DQS signals. Ex-1001, 3:13-16. The calibration includes "generating command signals and address signals for accessing the DRAM components (e.g., DRAM chips of a memory module) [,] … accessing data signals (e.g., DQ signals) that convey data for the DRAM components… [, and] accessing sampling signals (e.g., DQS signals) for controlling the sampling of the data signals." *Id.*, 3:16-27. A phase relationship between the command, data, and sampling signals is then automatically adjusted. *Id.*, 3:27-29; Ex-1002, ¶¶63-65.

The phase shift of a DQS signal can be adjusted over a minimum to a maximum value (e.g., 0-100% shift). Ex-1001, 5:7-13. Embodiments "search for and find the valid region of operation within the configuration space without requiring knowledge, a-priori, where the valid region is." *Id.*, 4:10-13.

B. Priority Date

The application underlying the '835 Patent (U.S. Application No. 10/716,320) ("'320 application") was filed on November 17, 2003, and issued as the '835 Patent on January 12, 2010. Accordingly, the earliest possible effective filing date of the '835 Patent is November 17, 2003.

C. The '835 Patent's Relevant File History

The '320 application was filed with twenty-two (22) claims. During examination, the Examiner issued multiple Office Actions rejecting all pending claims over U.S. Patent No. 6,553,472 ("Yang") or over Yang in view of U.S. Patent Publication No. 2004/0160833 ("Suzuki"), U.S. Patent No. 6,016,282 ("Keeth '282"), and/or U.S. Patent No. 5,781,766 ("Davis"). Ex-1003, 108-122; 167-180; 216; 257-269; 293-303; Ex-1002, ¶¶66-75. In a June 11, 2007, response, the Applicant argued that Yang does not disclose "automatic calibration" of cycle timing relationships, but instead discloses "programming clock delays, command delays, read command parameter delays, and write command parameter delays of a memory controller." Ex-1003, 286-287 (emphasis in original).

In Office Actions dated September 6, 2007, January 25, 2008, and July 23, 2008, the Examiner applied the same references and U.S. 2003/0122696 ("Johnson") to reject the pending claims. *Id.*, 167-180; 196-202; 259-260. In response to each Office Action, Applicant argued that the claims distinguished the references because "a process requiring user input" allegedly "is not automatically calibrating." *Id.*, 154-155, 204, 248.

A December 12, 2008, Office Action rejected the pending claims based on the same references in combination with U.S. Pub. No. 2002/0078316 ("Nakamura"). *Id.*, 109-122.

On March 12, 2009, Applicant amended all independent claims and argued that the cited art did not teach "systematically altering respective phase shifts of the command, data, and sampling signals to determine a valid operation range of the integrated device," as the amended claims then recited. *Id.*, 89-103 (emphasis in original); Ex-1002, ¶76.

The Office mailed a Notice of Allowance on May 14, 2009. Ex-1003, 65; Ex-1002, ¶77.

Accordingly, during prosecution of the '320 application, Applicant unsuccessfully argued that automatic calibration of cycle timing relationships is not taught by "programming [] delays of a memory controller." Ex-1003, 286-287. The Applicant also unsuccessfully argued that "a process requiring user input" allegedly "is not automatically calibrating." *Id.*, 154-155, 204, 248. The issued claims of the '835 Patent were allowed as a result of amending the independent claims to recite "systematically altering respective phase shifts of the command, data, and sampling signals to determine a valid operation range of the integrated device," or similar limitations. Ex-1003, 65.

VIII. SUMMARY OF THE PRIOR ART

A. ***Johnson***

Johnson was filed on May 12, 2000, issued on August 13, 2002, and is prior art under Sections 102(a), (b), and (e). Ex-1004, 1; Ex-1002, ¶78.

Johnson teaches a "calibration technique which is useful for calibrating the timing of control and data signals in memory devices." Ex-1004, 1:5-8; Ex-1002, ¶79. *Johnson*'s technique calibrates timing relationships between commands on a CA0-9 bus, data on data paths DQ, and a command clock signal (CCLK), and a data clock signal (DCLK) for a memory device. Ex-1004, 3:30-47; Ex-1002, ¶79.

Johnson discloses "a plurality of SLDRAM modules 11*a*...11*n* which are accessed and controlled by a memory controller 13. Memory controller 13 provides a command link to each of the SLDRAM modules 11*a*...11*n* which includes a clock signal CCLK [] and a 10 bit command bus data path CA0-9. [A] bi-directional data bus DQO-17 is provided between memory controller 13 and each of the SLDRAM modules 11*a*...11*n*, as are bi-directional data clocks DCLK0 and DCLK1." Ex-1004, 3:31-44.

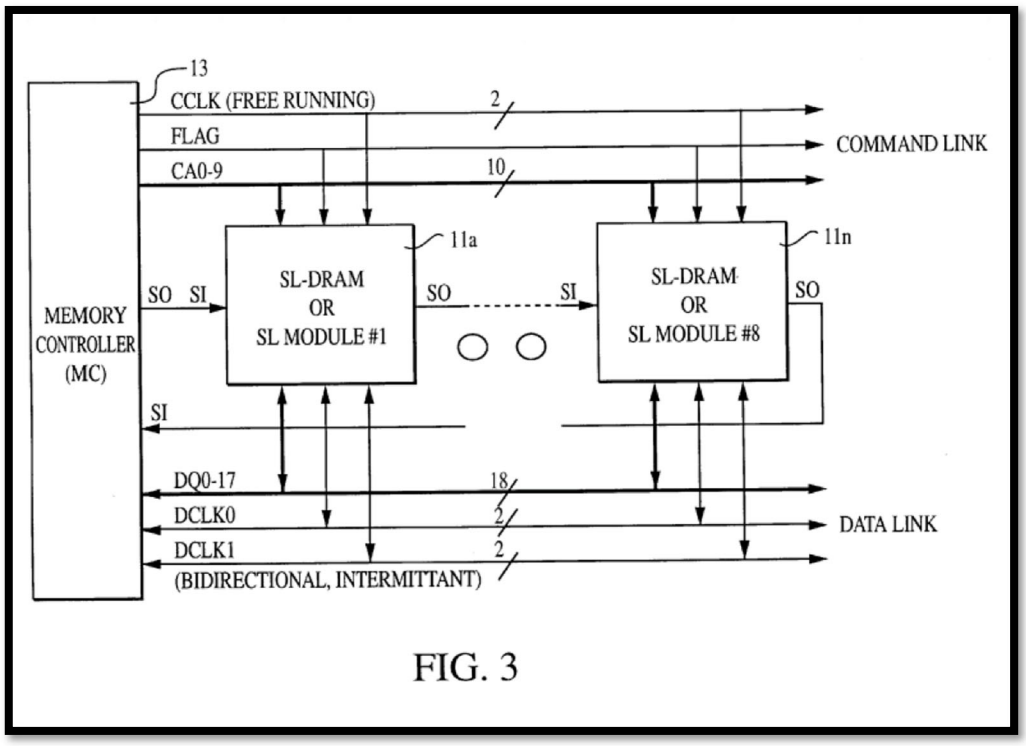


FIG. 3

Id., 4, Ex-1002, ¶80.

Johnson further teaches that "all incoming data can properly be aligned with respect to the clock used to latch in the data by adjusting the data delays relative to the clock (CCLK or DCLK) to position a sampling clock edge at or near the center of the data 'eye' or 'window' where the data is valid on an incoming data path." Ex-1004, 2:3-9. A control logic circuit then "steps through all possible delay positions of ring delays…as the data sampling is performed and stores patterns representing which delay values for the ring delays…provide for a correct sampling." *Id.*, 4:36-41. Ex-1002, ¶¶81-85.

B. *Jeddeloh*

Jeddeloh was filed on July 13, 1999, issued on September 30, 2003, and is prior art under Section 102(e). Ex-1005, 1; Ex-1002, ¶86.

Jeddeloh teaches synchronizing "a data signal and a data strobe signal received from a random access memory." Ex-1005, Abstract. *Jeddeloh* explains that a "data strobe signal is used to clock [] data into [a] memory interface" and that a delay circuit is "configured to delay the data strobe signal so as to synchronize the data strobe signal with the data signal received from the random access memory." *Id.*, 4:28-29; Ex-1002, ¶¶87-90.

Jeddeloh further teaches determining delay values "by performing test read operations using a plurality of different combinations of different first delay values and different second delay values." Ex-1005, Abstract; Ex-1002, ¶¶91-92. "[D]ata strobe signal 206 passes through delay circuit 314 [and] also passes through inverter 318 and delay circuit 316." *Id.*, 5:25-28. The delay circuits 314 and 316 can be "programmed to precisely synchronize data strobe signal 206 with data signal 202." Ex-1005, 5:32-34.

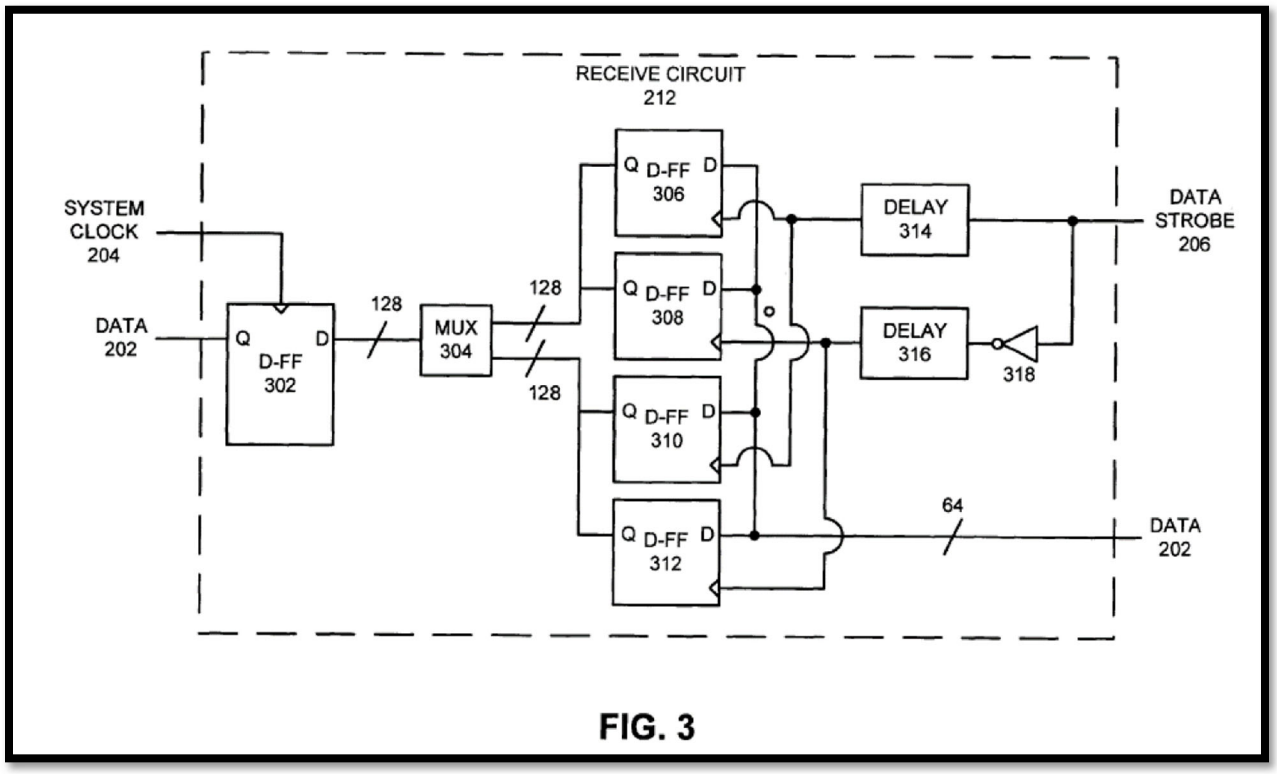


FIG. 3

Id., 4; Ex-1002, ¶92.

C. ***Keeth***

Keeth was filed on December 3, 1996, issued on September 5, 2000, and is prior art under Sections 102(a), (b), and (e). Ex-1006, 1; Ex-1002, ¶93.

Keeth discloses "a memory integrated circuit [that] includes a vernier clock adjustment circuit [] providing a rising-edge clock signal representing the input clock signal delayed by a rising-edge delay and providing a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay." Ex-1006, Abstract; Ex-1002, ¶¶94-99. *Keeth*'s clock adjustments "compensate[] for such effects as duty cycle variation, bus position of a given memory device, timing drift,

loading variations, clock jitter, clock skew, noise, overshoot, and ringing." *Id.*, 1:51-59. *Keeth* further teaches that "command, write, and read vernier clock adjustment circuits are" adjusted for "DRAM module[s.]" Ex-1006, 8:26-32; Ex-1002, ¶¶101-103. Figure 7 shows a block diagram of *Keeth*'s memory system, including vernier clock adjustment circuits 60, 70, and 74, which are discussed in further detail in Ground 2.

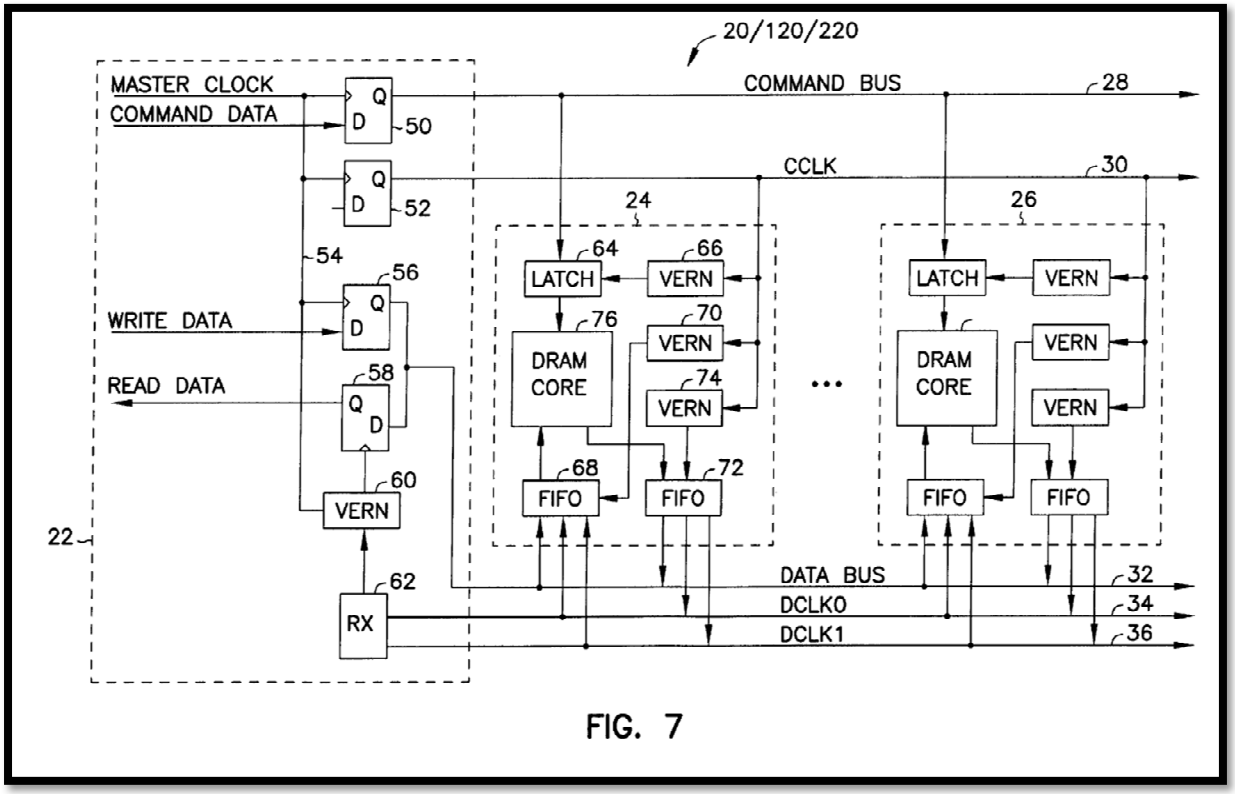


FIG. 7

Ex-1006, 10; Ex-1002, ¶¶100-102; *see infra* Section X(B).

IX. CLAIM CONSTRUCTION

In the co-pending litigation, the Court construed the preambles of claims 1, 7, 12, 20, and 23 as non-limiting. Ex-1007, 8. The Court also construed "the valid

operation range includes an optimal operation point for the integrated circuit device" in claims 1 and 7 according to its plain and ordinary meaning and specified that "this claim element does not require determining the optimal operation point." *Id.*

The claims of the '835 Patent should be construed under the *Phillips* standard. 37 C.F.R. § 42.100(b); *see generally Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). Under *Phillips*, claim terms are typically given their ordinary and customary meanings, as would have been understood by a POSITA, at the time of the invention, having taken into consideration the language of the claims, specification, and prosecution history. *Phillips*, 415 F.3d, 1313; *see also id.*, 1312-16. The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Sys., Inc.*, IPR2015-00633, Paper 11 at 16 (Aug. 14, 2015). As explained in further detail below, the scope of the claims includes the prior art under any reasonable construction, including the Court's constructions in the co-pending litigation. Ex-1002, ¶¶38-39. Petitioner believes that no express constructions of the claims are necessary to assess whether the Challenged Claims read on the prior art.[3]

[3] Petitioner reserves all rights to raise claim construction and other arguments in other proceedings.

X. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Ground 1: Claims 1-23 are obvious over *Johnson* in view of *Jeddeloh*

1. *Claim 1*

Element 1.P

To the extent the preamble is limiting, *Johnson* teaches automatically calibrating intra-cycle timing relationships between commands on a command bus data path CA0-9 (the recited "command signals"), data on a data bus DQ (the recited "data signals"), and command clock signal (CCLK) and data clock signal (DCLK) (the recited "sampling signals") for a memory system (the recited "integrated circuit device"). Ex-1004, 3:33-47; Ex-1002, ¶109. *Johnson* describes an automatic calibration process for use in a memory device where a data path is "calibrated relative to a clock signal." Ex-1004, Abstract; Ex-1002, ¶109. Annotated Figure 3 below illustrates the relevant signals.

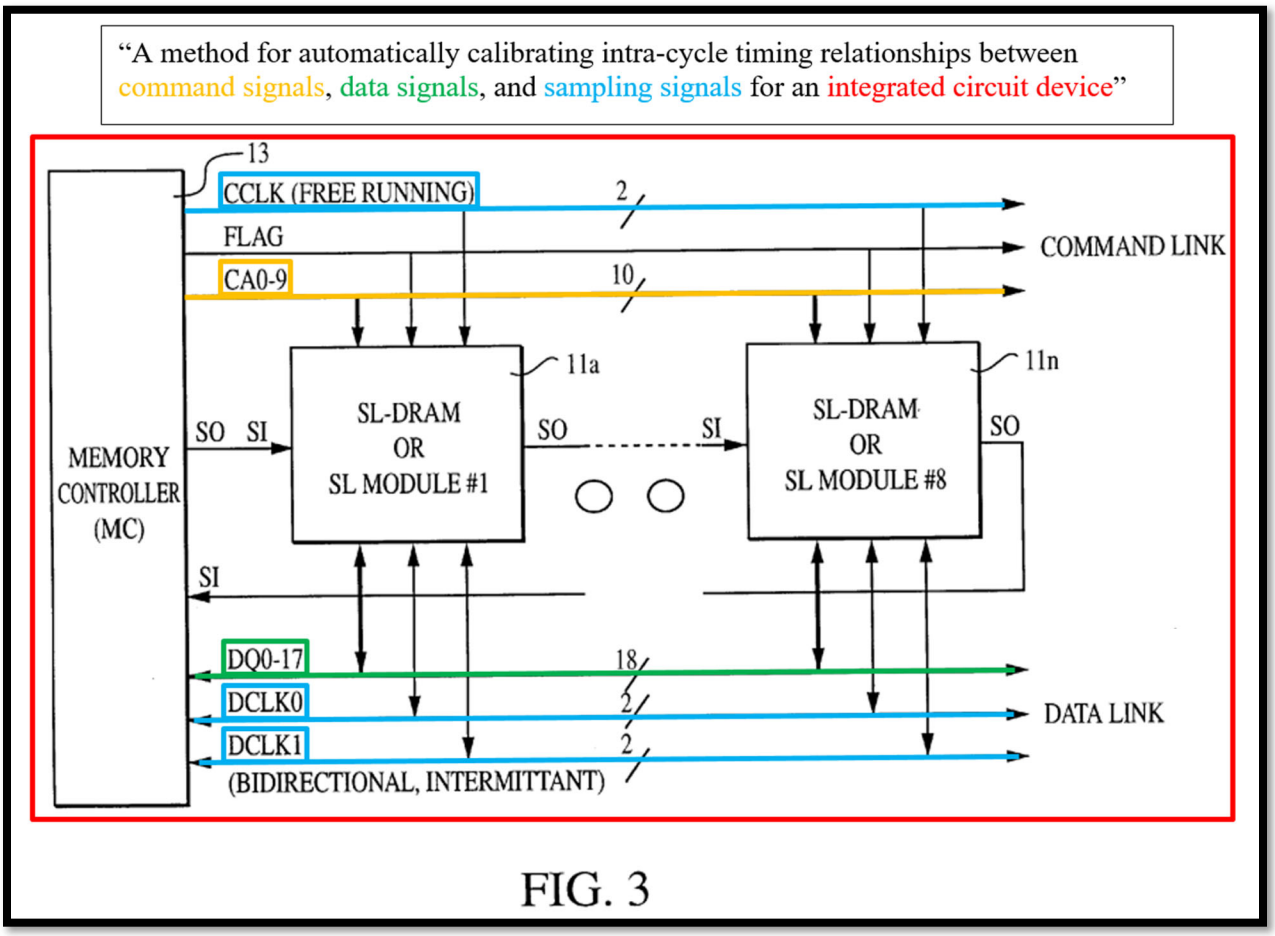


FIG. 3

Ex-1004, 3[4]; Ex-1002, ¶109.

Figure 3 depicts an SLDRAM system that "includes a plurality of SLDRAM modules 11*a*...11*n* which are accessed and controlled by a memory controller 13." Ex-1004, 3:31-33; Ex-1002, ¶110. The memory controller 13 "provides a command link to each of the SLDRAM modules" which includes the command bus data path

[4] All annotations and quoted claim elements in text boxes are added by Petitioner unless otherwise noted.

CA0-9 and a clock signal CCLK. Ex-1004, 3:30-40; Ex-1002, ¶110. A data link that includes bi-directional data bus DQ0-17 as well as bi-directional data clocks DCLK0 and DCLK1 are also "provided between memory controller 13 and each of the SLDRAM modules[.]" Ex-1004, 3:33-47; Ex-1002, ¶110.

Johnson teaches a signal calibration process such that "serial and parallel calibration of all data paths is achieved." Ex-1004, 2:51-52; Ex-1002, ¶111. The calibration process is performed on "the data paths of the command bus CA0-9" and "the receive data paths of the data bus DQ[.]" *Id.*, 4:56-58; Ex-1002, ¶111. As a result, timing relationships between all of the command signals, data signals, and sampling signals are calibrated. Ex-1002, ¶111. *Johnson* further discloses that the calibration process is performed automatically at initialization. Ex-1004, 1:36-40; Ex-1002, ¶112; Ex-1019, 53.

Johnson states that its "memory device [] clocks data (i.e., reads or writes data) twice per clock cycle: on both the rising and falling edges of the clock." Ex-1004, 8:41-44. *Johnson* explains that as a result of calibration, each "data path has its data eye correctly centered on a rising or falling clock edge." *Id.*, 6:30-33. A POSITA would have understood that the data signal having the "data eye" has an "intra-cycle timing relationship" with a clock edge of a cycling clock. Ex-1002, ¶111.

Johnson's calibration technique is for "calibrating the timing of control and data signals in memory devices[.]" Ex-1004, 1:6-7; Ex-1002, ¶111. *Johnson* explains that its "memory device containing the calibration structure and operating as described above may be used in a processor-based system" where the processor "may itself be an integrated processor which utilizes on-chip memory devices containing the calibration structure." *Id.*, 8:29-41. Accordingly, the various signals discussed in *Johnson* (e.g., on data path CA0-9, data bus DQ, CCLK, DCLK0 and DCLK1) are for "an integrated circuit device." Ex-1002, ¶111.

Therefore, *Johnson* discloses Element 1.P. Ex-1002, ¶¶109-112.

Element 1.1

Johnson discloses that a "plurality of SLDRAM modules 11*a*…11*n* [] are accessed and controlled by [] memory controller 13." Ex-1004, 3:31-33. The memory controller 13 "provides a command link to each of the SLDRAM modules 11*a*…11*n* which includes [] a 10 bit command bus data path CA0-9" (the recited "command signals"). *Id.*, 3:33-38; Ex-1002, ¶113. Data on CA0-9 "is clocked in by sequential positive and negative going transitions of the command clock signal CCLK." Ex-1004, 4:67-5:3. Annotated Figure 3 below illustrates this claim element.

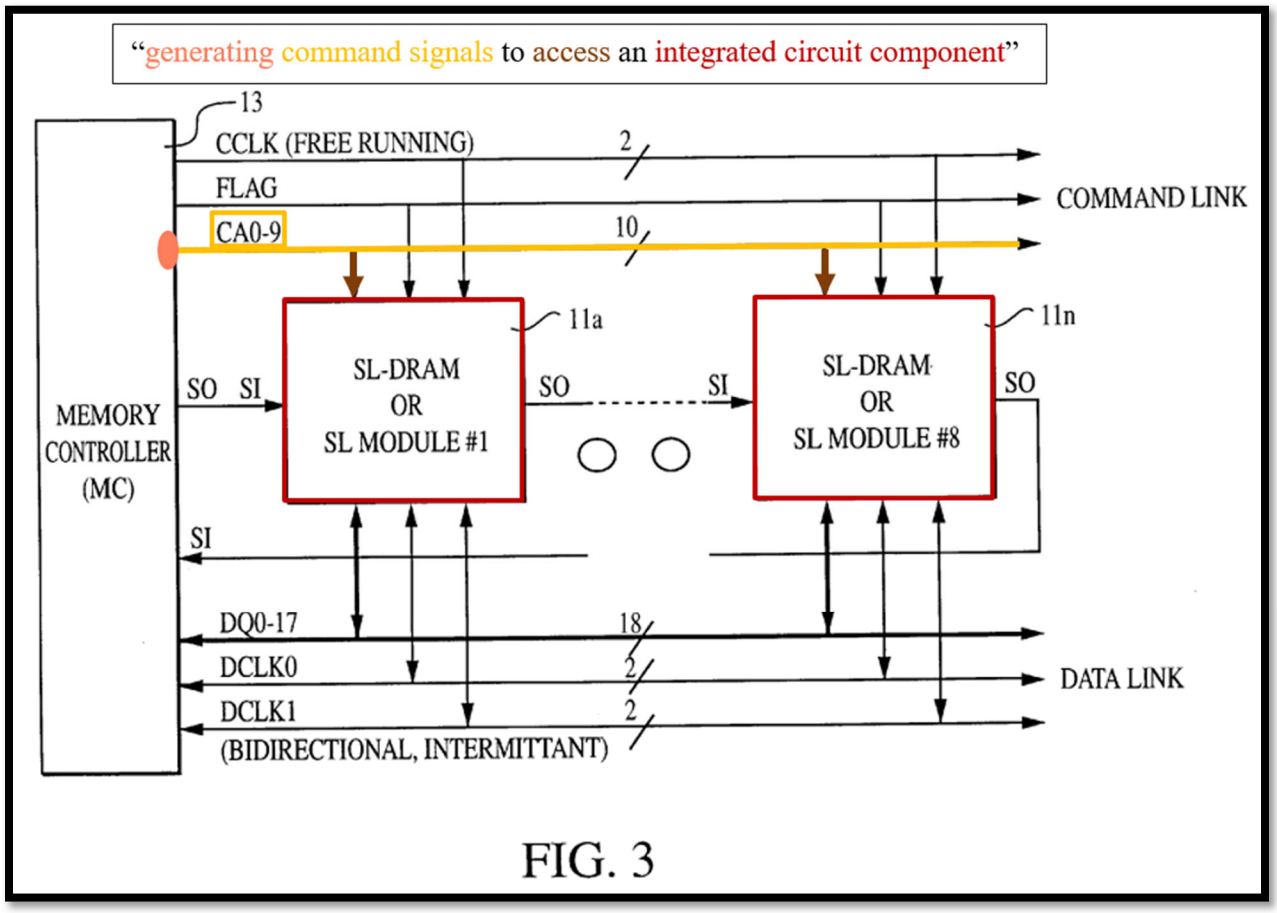
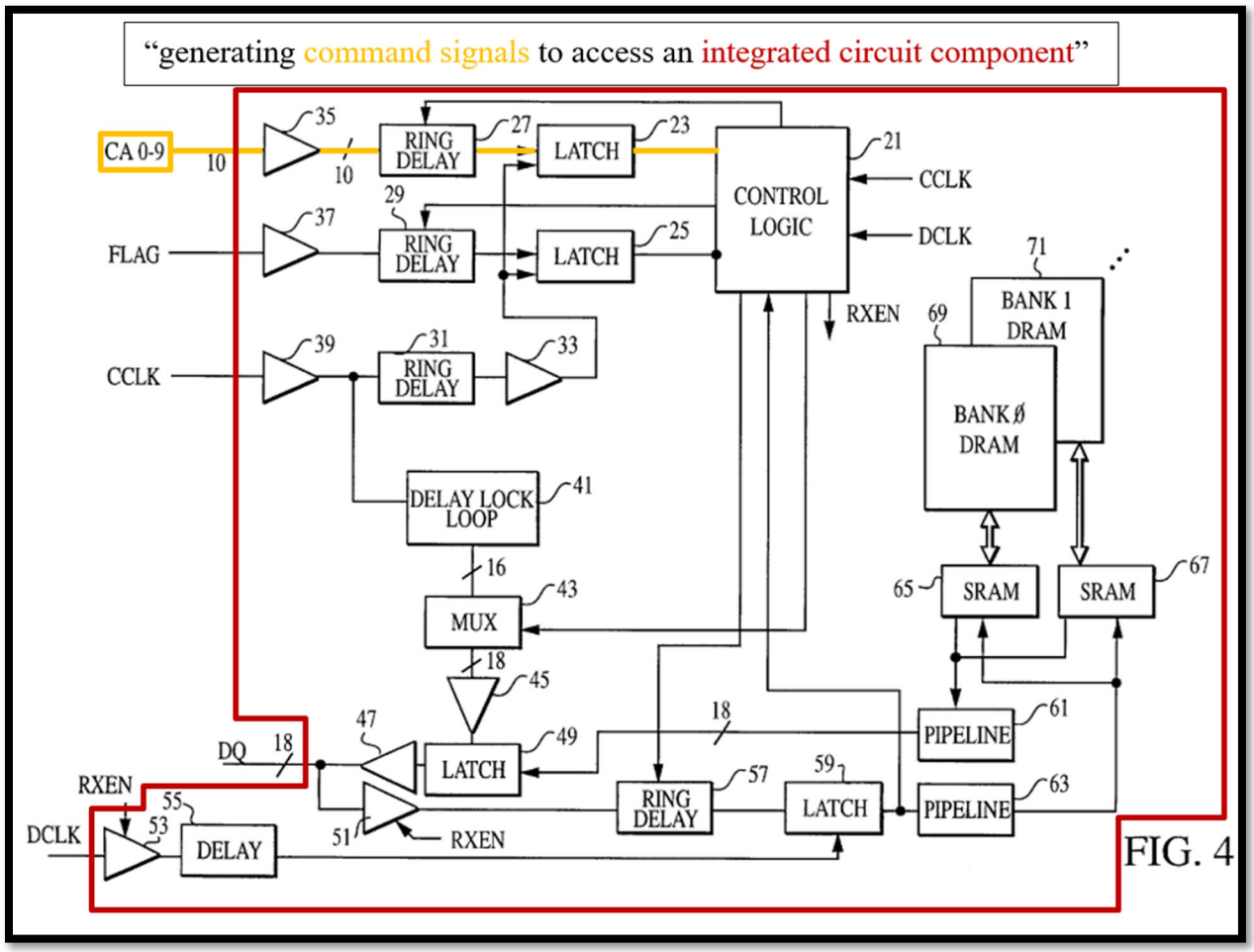


FIG. 3

Id., 3; Ex-1002, ¶114.

As depicted in annotated Figure 4 below, a control logic circuit 21 of an SLDRAM module "receives and analyzes commands on the CA0-9 bus and controls the input/output (I/O) **access operations of the memory banks**[.]"[5] Ex-1004, 3:57-60.

[5] All emphasis added by Petitioner unless otherwise noted.



Id., 4; Ex-1002, ¶115.

Johnson explains that the "memory device containing the calibration structure and operating as described above may be used in a processor-based system" where the processor "may itself be an integrated processor which utilizes on-chip memory devices containing the calibration structure and operates in accordance with the present invention" *Id.*, 8:29-41. Accordingly, a POSITA would have understood that *Johnson*'s SLDRAM modules 11*a*…11*n* are integrated circuit components accessed by command signals generated by the memory controller. Ex-1002, ¶¶113, 117. A

POSITA would have understood that *Johnson*'s memory controller performs the "generating," at least because such controllers were well-known to manage the flow of information between memory and CPUs, and did so by generating and issuing commands to memory modules to execute read or write operations. *Id.*, ¶¶115, 117; Ex-1015, 2; Ex-1016, 4, Ex-1017, 1.

Therefore, *Johnson* discloses Element 1.1. *Id.*, ¶¶113-117.

Element 1.2

Johnson discloses that "a bi-directional data bus DQ0-17 is provided between memory controller 13 and each of the SLDRAM modules 11*a*...11*n*, as are bi-directional data clocks DCLK0 and DCLK1. The clock DCLK0 is used to strobe **input/output data into and out of the SLDRAM modules**[.]" Ex-1004, 3:41-45. *Johnson* explains that data (the recited "data signals to convey") to be input to a memory bank of an SLDRAM module (the recited "integrated circuit component") "is supplied by memory controller 13 (FIG. 3) on the DQ data bus." *Id.*, 4:12-14; Ex-1002, ¶118. Annotated Figure 3 below illustrates this claim element.

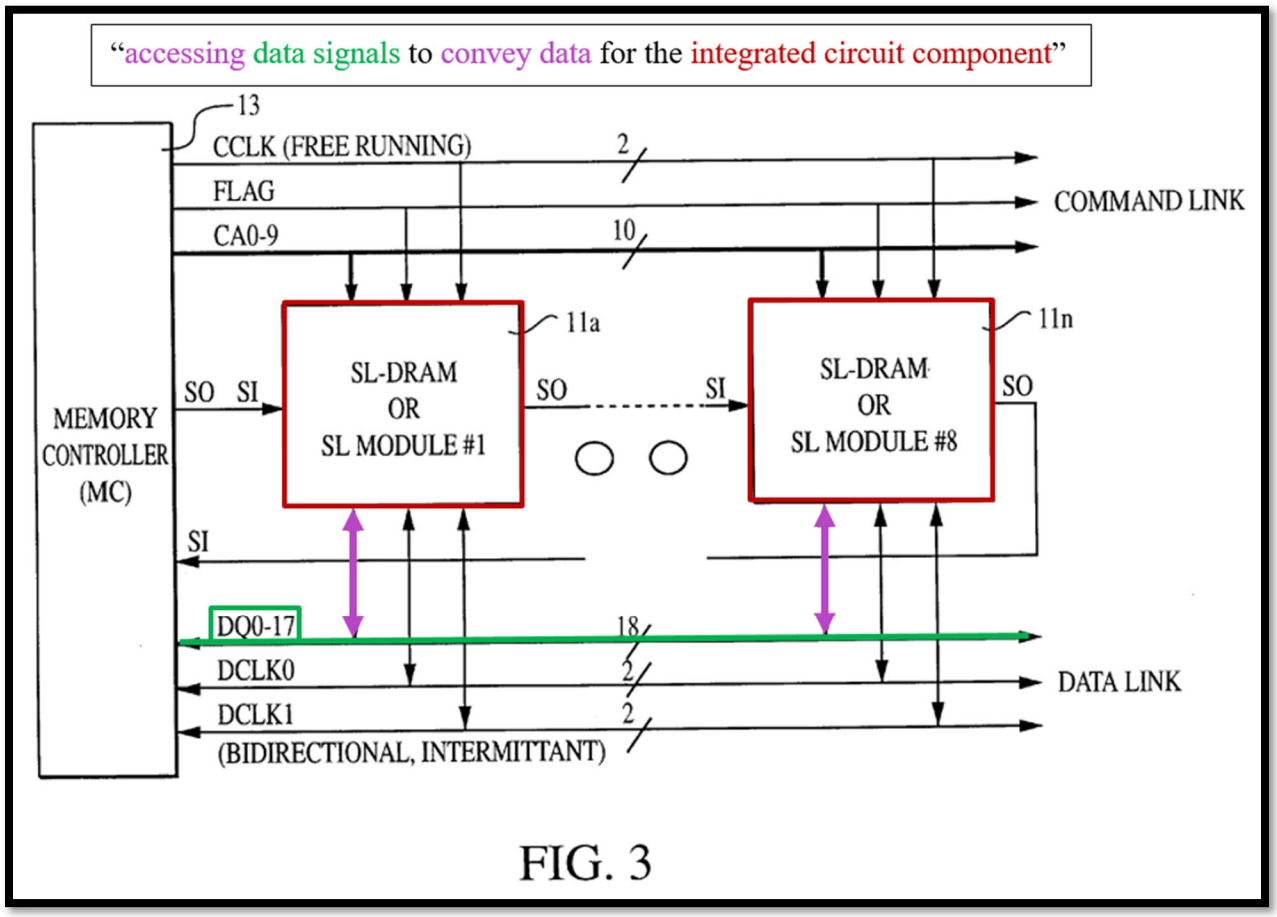
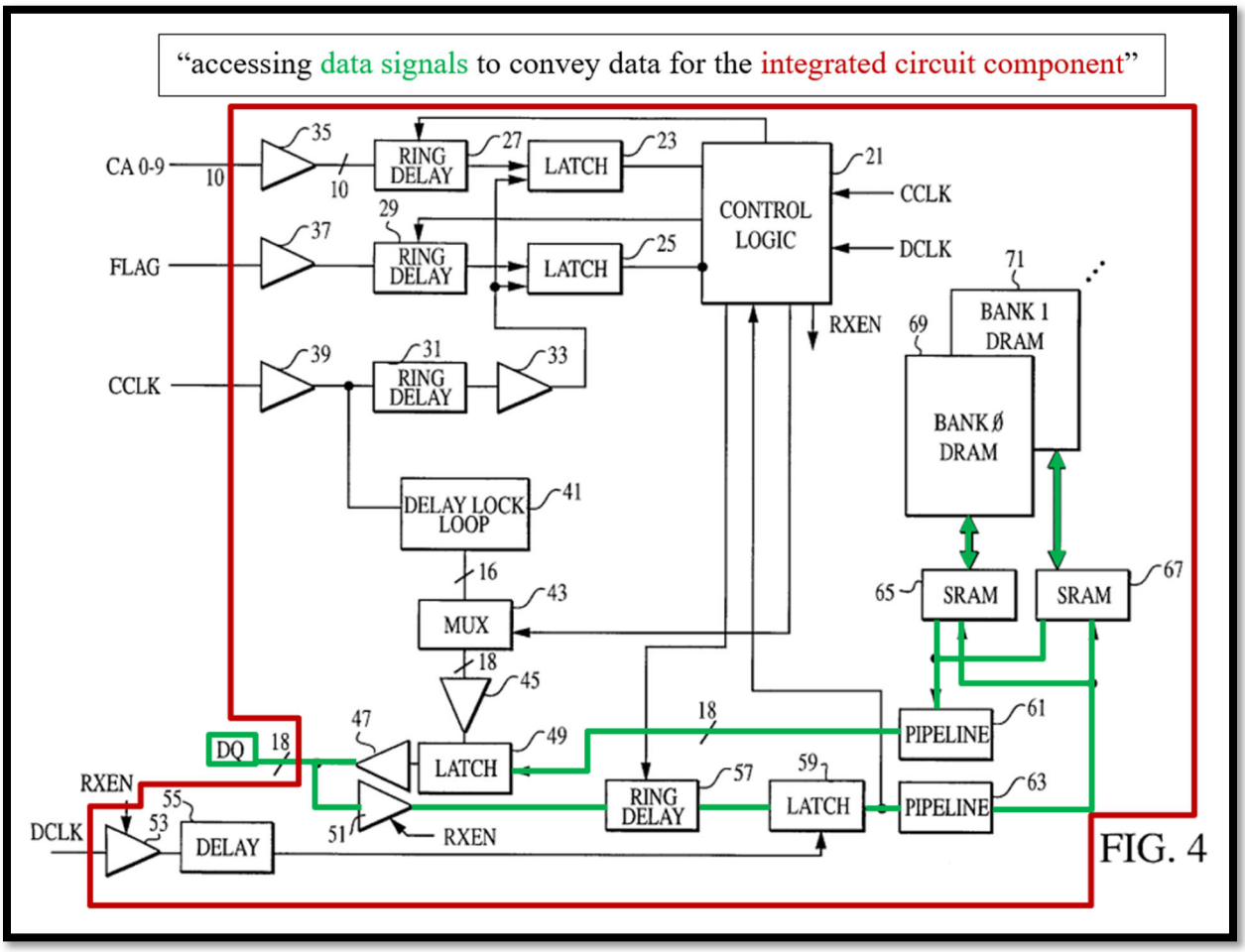


FIG. 3

Ex-1004, 3; Ex-1002, ¶119.

Johnson further teaches that SLDRAM modules include a latch to "latch in incoming data on the data bus DQ." Ex-1004, 4:24-26. During a write operation, "[d]ata which is to be input[ted] to memory banks 69, 71 is supplied by memory controller 13 (FIG. 3) on the DQ data bus[.]" Ex-1004, 4:12-18. During a read operation, data output from memory banks 69 and 71 pass through the circuitry until it is "passed back to memory controller 13 (FIG. 3) via data bus DQ." *Id.*, 4:5-11. An annotated version of Figure 4 provided below illustrates these steps.



Id., 4; Ex-1002, ¶120.

The memory controller 13 accesses data signals output from memory banks of an SLDRAM module and transmitted via data bus DQ during a read operation. Ex-1002, ¶121. The SLDRAM module accesses data signals transmitted from memory controller 13 via data bus DQ during a write operation. Ex-1004, 4:12-18; Ex-1002, ¶121.

Therefore, *Johnson* discloses Element 1.2. Ex-1002, ¶¶118-122.

Element 1.3

Johnson discloses providing clock signals CCLK, DCLK0, and DCLK1 (the recited "sampling signals") to "strobe input/output data into and out of the SLDRAM modules" (the recited "to control sampling of the data signals"). Ex-1004, 3:44-45; Ex-1002, ¶123. Annotated Figure 3 below illustrates the clock signals CCLK, DCLK0, and DCLK1.

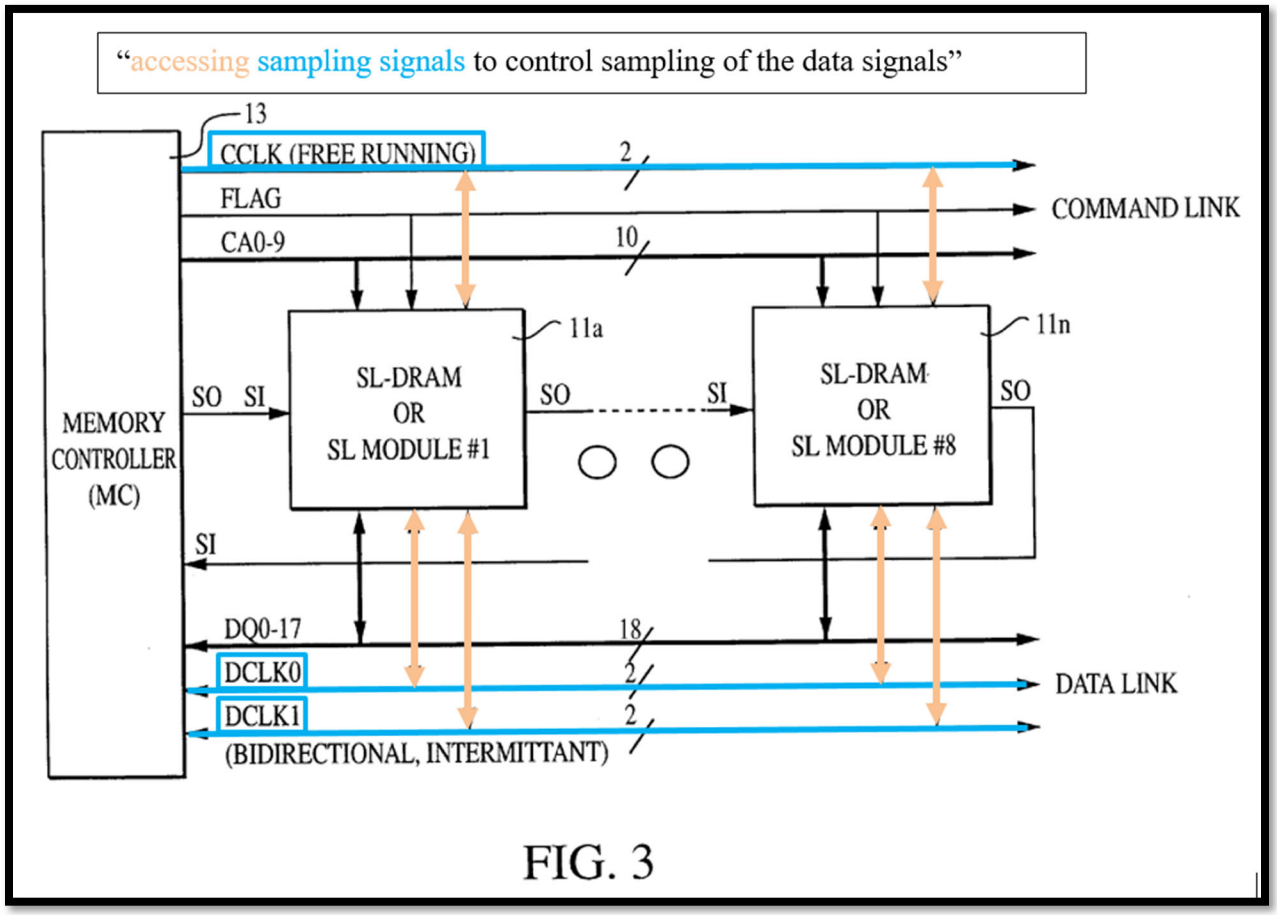


FIG. 3

Ex-1004, 3; Ex-1002, ¶124.

Johnson explains that "[m]emory controller 13 provides a command link to each of the SLDRAM modules 11*a*…11*n* which includes a clock signal CCLK**.**" Ex-1004, 3:33-36. In addition, "bi-directional data clocks DCLK0 and DCLK1" are provided "between memory controller 13 and each of the SLDRAM modules 11*a*...11*n*." *Id.*, 3:42-44. DCLK0 and DCLK1 are used to "strobe input/output data into and out of the SLDRAM modules" *Id.*, 3:44-45; Ex-1002, ¶125. The memory controller 13 therefore accesses data sampling signals when data is read from or written to the SLDRAM modules. Ex-1002, ¶123. Each SLDRAM module also accesses data sampling signals when data is read from or written to the respective SLDRAM module. *Id.* Sampling of data signals is further discussed in reference to annotated Figure 4 below.

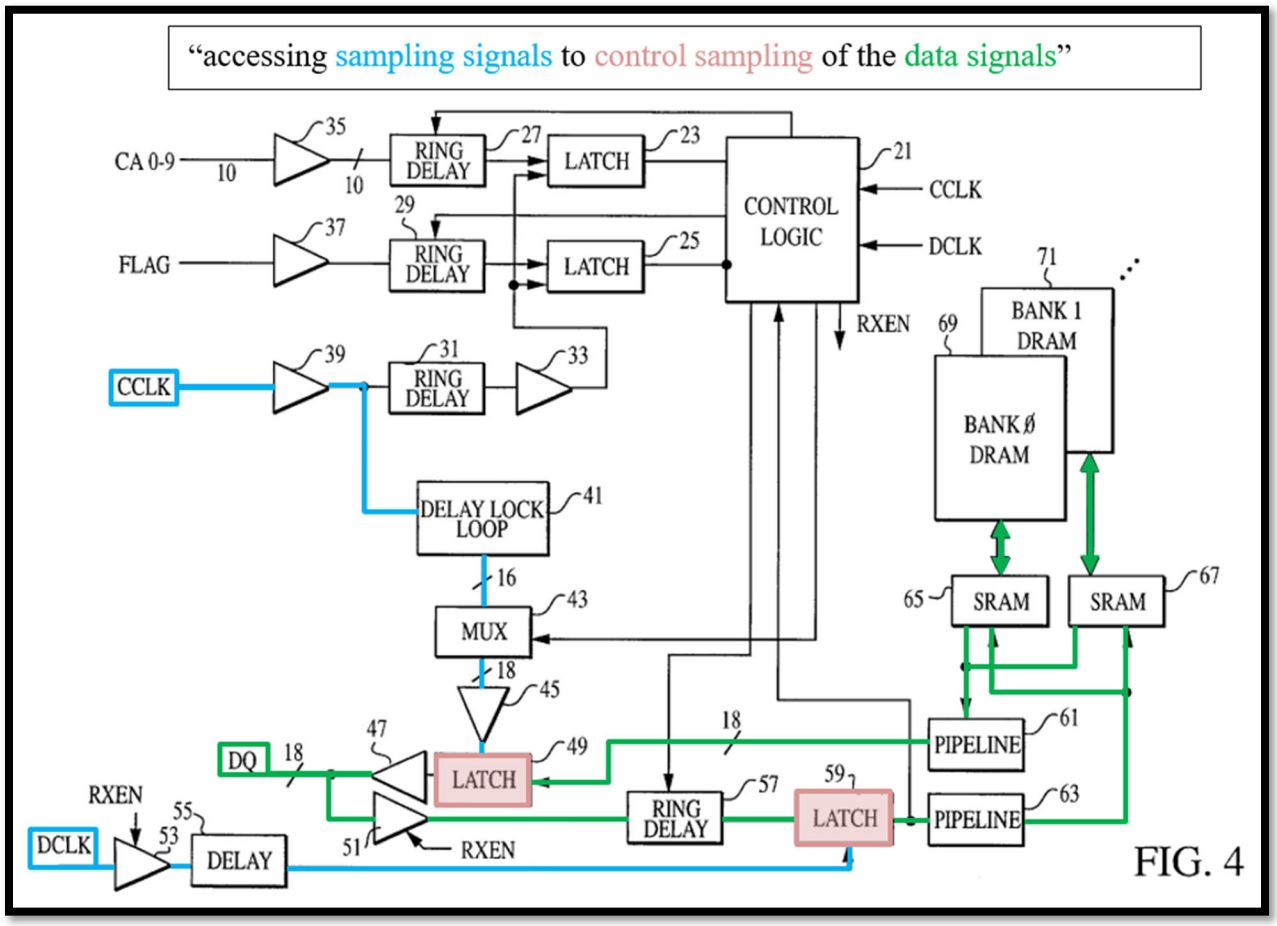


FIG. 4

Ex-1004, 4; Ex-1002, ¶125.

Johnson explains that "[t]he signal CCLK [] passes from buffer 39 into a delay lock loop circuit 41" that provides clock signals into a multiplexer. *Id.*, 4:1:3. The multiplexer provides "clock output signals through respective buffers" to latches 49, which latch the data output from the memory banks. *Id.*, 4:3-5; Ex-1002, ¶126. "The output data latched in latches 49" is passed "to memory controller 13 [] via data bus DQ." Ex-1004, 4:5-11. CCLK therefore controls sampling of data signals at least

when the data signals are output from the memory banks onto the data bus DQ. Ex-1002, ¶126.

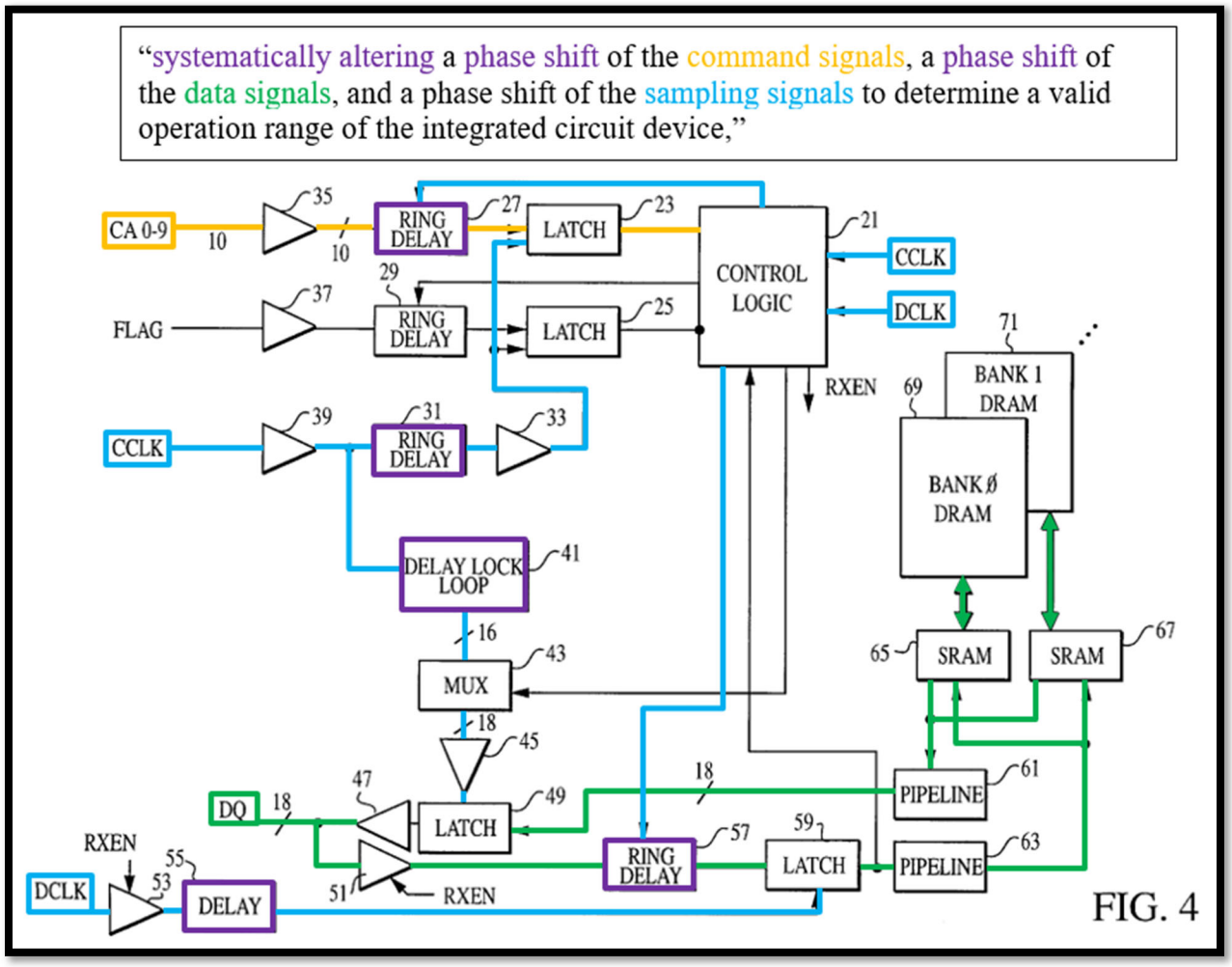
Additionally, the data clock DCLK "passes through gated buffer 53, delay circuit 55 and is used to **control latch 59 to latch in incoming data on the data bus DQ**." Ex-1004, 4:23-26. *Johnson*'s calibration process is implemented such that the circuit of Figure 4 is "synchronized to ensure that the incoming data is properly **clocked in by the clock signals CCLK and DCLK**." *Id.*, 4:29-31. By latching or clocking data, the sampling signals CCLK, DCLK0, and DCLK1 control the sampling of the data signals. Ex-1002, ¶¶126-129.

Thus, *Johnson* discloses Element 1.3. Ex-1002, ¶¶123-129.

Element 1.4.a

Johnson discloses testing delay values of the command signals transmitted via data bus CA0-9 (the recited "a phase shift of the command signals") to determine values that result in alignment with CCLK and testing delay values of the data signals transmitted by data bus DQ0-17 (the recited "a phase shift of the data signals") to determine values that result in alignment with DCLK. Ex-1004, 1:42-48, Ex-1002, ¶130. *Johnson* identifies a range of delay values that result in valid sampling for the memory device (the recited "determine a valid operation range of the integrated circuit device"). Ex-1004, 4:41-43, Ex-1002, ¶130.

Johnson teaches "parallel calibration of all data paths[,]" by "aligning the ring delays of a path under calibration to an immediate previously calibrated data path until all data paths have been calibrated." *Id.*, 2:51-52. Based on the calibration, VALID signals are generated by compare circuits to "signal whether the synchronization pattern is properly recognized to the logic 81" (the recited "to determine a valid operation range of the integrated circuit device"). *Id.*, 6:48-54; Ex-1002, ¶¶135-136. A POSITA would have understood that *Johnson*'s signals are cyclic signals having a phase such that a delay (i.e., shift) in timing of such signals is a phase shift. Ex-1004, 5 (showing cycles of CCLK, FLAG, CMD, DQ, and DCLK signals), 8:41-44; Ex-1002, ¶136. Annotated Figure 4 below illustrates this element.



Ex-1004, 4; Ex-1002, ¶131.

Regarding command signals, *Johnson* discloses that a "synchronizing pattern is applied to" data input paths CA0-9 "while the data pattern is sampled in latches 23 and 25 by the delayed clock signal CCLK" ("systematically altering a phase shift of the command signals"). Ex-1004, 2:33-36; Ex-1002, ¶134. Specifically, "[t]he control logic circuit 21 steps through all possible delay positions of ring delays 27 and 29 [] and stores patterns representing which delay values [] provide for a correct

sampling and recognition" of the synchronization pattern. Ex-1004, 4:36-41. The synchronizing pattern is used to establish "an 'eye' or 'window' of acceptable delays for each of the ring delays 27 for the command data paths CA0-9." *Id.*, 2:41-43; Ex-1002, ¶134.

Regarding data signals, *Johnson* teaches that "[t]he same calibration process may be carried out on [] any one of the receive data paths of the data bus DQ." Ex-1004, 4:55-59. While CA0-9 data paths are aligned to CCLK, "the data paths DQ0-17 are aligned to [DCLK]." *Id.*, 6:46-48. For example, *Johnson* discloses that the calibration discussed above may be used to align data path DQ<0> "until a final delay value is selected" (the recited "systematically altering [] a phase shift of the data signals"). *Id.*, 25-31; Ex-1002, ¶136. "Once a first data path, e.g., DQ0, is serially aligned to DCLK [] the remaining DQ1-17 data paths can then be aligned." Ex-1004, 7:36-42. The control logic 21 "steps through all possible delay values of ring delay 57*b*, and notes those delays which produce a coincidence of the calibration pattern on data paths DQ<0> and DQ<1>, and selects a final delay value for delay 57*b* which is at or near the center of acceptable delays." Ex-1004, 7:52-57. A POSITA would have understood that *Johnson*'s methodical procedure for "step[ping] through" phase shifts to calibrate delays of both command signals and data signals is "systematically altering." Ex-1002, ¶136.

Johnson further teaches that "control logic circuit 21 includes compare circuit 83*a*, which aligns the DQ1 data path including ring delay 57*b* to the previously aligned DQ0 data path which includes ring delay 57*a* by comparing the calibration pattern on aligned data path DQ0 with the calibration pattern on the DQ1 data path to generate an appropriate validity signal on signal lines VALID." Ex-1004, 7:46-52. *Johnson*'s calibration is therefore used to "determine a valid operation range of the integrated circuit device." Ex-1002, ¶135.

Johnson's calibration is intended "to produce serial and parallel bit alignment on all data paths." Ex-1004, Abstract. To the extent Patent Owner argues that *Johnson* does not explicitly describe stepping through delays for its CCLK or DCLK signals (each a "sampling signal"), as shown in annotated Figure 4 above, *Johnson* discloses that the "signal CCLK also passes from buffer 39 into a **delay lock loop circuit 41** which provides 16 clock signals into a multiplexer 43. The **multiplexer provides 18 clock output signals** through respective buffers 45 to 18 latches 49 which latch data output from the memory banks 69, 71." *Id.*, 2:1-8; Ex-1002, ¶133. Figure 4 of *Johnson* shows that the data output from the memory banks 69, 71 does not pass through a delay before it reaches latches 49 where it is latched by CCLK. Ex-1004, 4; Ex-1002, ¶133. A POSITA would have therefore recognized a need for alignment between CCLK and the data signals at least at latches 49. *Id. Johnson* also

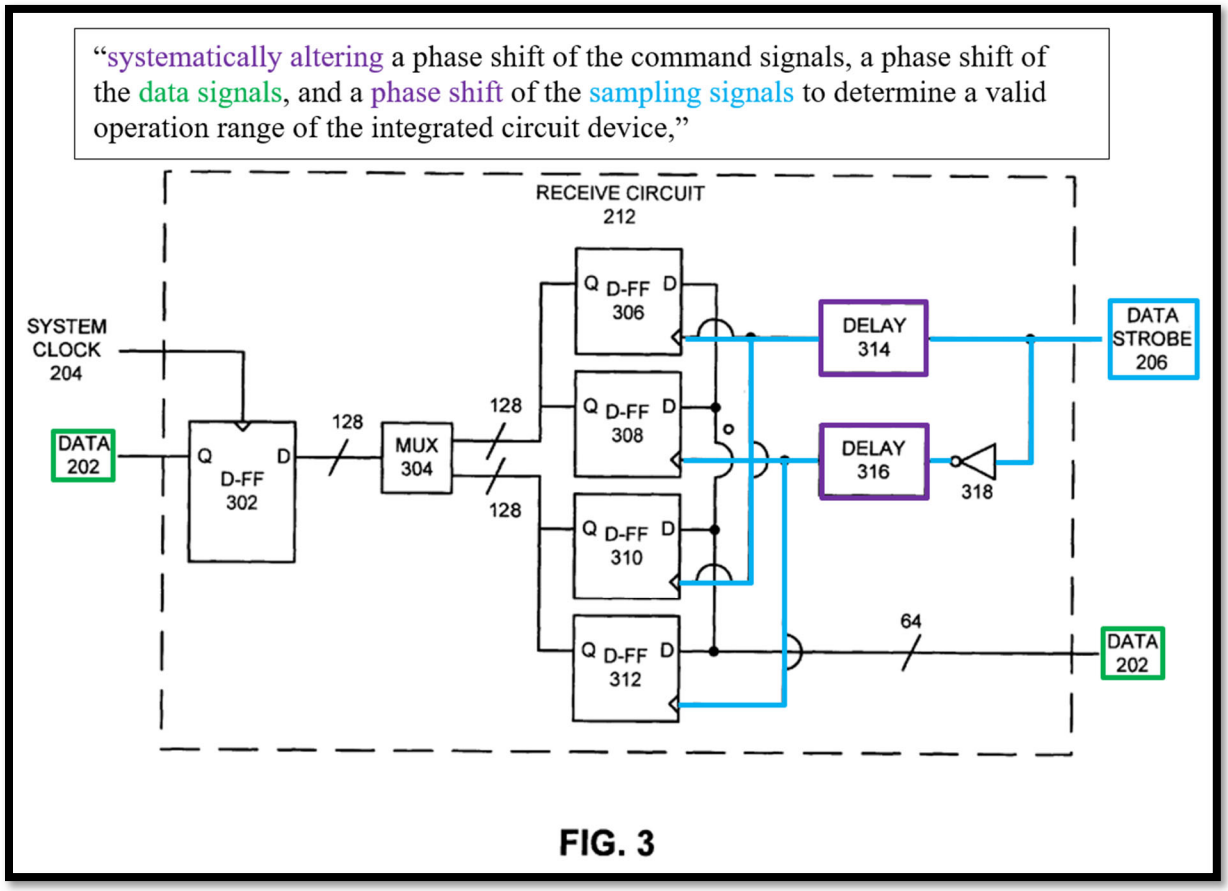
shows that DCLK is delayed as it passes through "delay circuit 55" latching a data signal at latch 59. Ex-1004, 4:24-26.

A POSITA therefore would have been motivated to implement the express teachings of *Johnson* to systematically alter delay values for the signal CCLK and DCLK in order to "establish[] an 'eye' or 'window' of acceptable delays" according to the technique described by *Johnson*. Ex-1004, 4:41-43; Ex-1002, ¶133. Such calibration of the signal CCLK would be nothing more than applying a known technique already disclosed by *Johnson* to known device components (e.g., delay lock loop circuit 41 and/or delay circuit 55) ready for improvement to yield the predictable results of improving alignment of signals in a memory device, as taught by *Johnson*. Ex-1002, ¶133; *see KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 415-421 (2007). Accordingly, it would have been obvious based on the teachings of *Johnson* to apply the calibration technique to the CCLK and DCLK signals (the recited "systematically altering [] a phase shift of the sampling signals."). *Id.*

To the extent Patent Owner argues that *Johnson* does not teach and/or render obvious systematically altering a phase shift of sampling signals, *Jeddeloh* teaches this element. Ex-1002, ¶137. *Jeddeloh* discloses synchronizing "a data signal and a data strobe signal received from a random access memory." Ex-1005, Abstract. A "second programmable delay circuit is configured to delay the data strobe signal so as to synchronize the data strobe signal with the data signal received from the

random access memory." *Id. Jeddeloh*'s data strobe signals are "sampling signals." Ex-1002, ¶137.

Jeddeloh teaches a system that "selects a [] delay value in the middle of a valid range of [] delay values" by "performing test read operations using a plurality of different combinations of different [] delay values." Ex-1005, 7:19-24; Abstract. Annotated Figure 3 below illustrates *Jeddeloh*'s delay of data strobe signals.



Id., 4; Ex-1002, ¶138.

Jeddeloh explains that "data strobe signal 206 passes through delay circuit 314 into clock inputs of D-FFs 306 and 310. Data strobe signal 206 also passes

through inverter 318 and delay circuit 316 into clock inputs of D-FFs 308 and 312." Ex-1005, 5:25-28. The delay circuits 314 and 316 can be "programmed to precisely synchronize data strobe signal 206 with data signal 202." *Id.*, 5:32-34. Specifically, "delay values to be loaded into delay circuits 218, 314 and 316" are determined by the system. *Id.*, 6:27-28. Thereafter, "test read operations using different delay values" are performed (the recited "systematically altering [] a phase shift of the sampling signals") and once "optimal delay values are determined [(the recited "to determine a valid operation range of the integrated circuit device")], the delay values are programmed into" the delay circuits. *Id.*, 6:30-36; Ex-1002, ¶¶139-142.

To the extent that *Johnson* does not explicitly explain or render obvious how CCLK or DCLK are synchronized to the data signals received from and sent to the DRAM banks, a POSITA would have had reason to look to *Jeddeloh* for specificity as to how to synchronize the signals. *Id.*, ¶144. *Johnson* does disclose applying delay circuits to the sampling signals CCLK and DCLK, albeit without intricate detail. Ex-1004, 1:57-59, 4:1-3; 4:24-26; Ex-1002, ¶¶141-142. A POSITA would have recognized the advantages of applying *Jeddeloh*'s defined technique of systematically altering a phase shift of sampling signals to the delays of *Johnson*. Ex-1002, ¶141. A POSITA would have been motivated to make such a modification at least to improve synchronization of data signals and sampling signals when both writing to and reading from DRAM banks. Ex-1002, ¶143.

As an initial matter, both *Johnson* and *Jeddeloh* list Micron Technology, Inc. as Assignee and both were filed about a year apart. Ex-1004; Ex-1006; Ex-1002, ¶144. Modifying the calibration process of *Johnson* to include data strobe signal synchronization of *Jeddeloh* would have been nothing more than using a known technique (e.g., the data signal and a data strobe signal synchronization of *Jeddeloh*) to improve similar devices (e.g., the memory system of *Johnson* and the random access memory of *Jeddeloh*) in the same way to correct alignment of signals in a memory device. *Id.*; *see KSR*, 550 U.S. at 415-421. Accordingly, it would have been obvious to a POSITA to modify the calibration process of *Johnson* to incorporate the data strobe signal synchronization of *Jeddeloh*. *Id.*

Therefore, *Johnson* and *Jeddeloh*, at least in combination, disclose Element 1.4.a. Ex-1002, ¶¶130-144.

Element 1.4.b

Johnson discloses determining an "eye" or "window" of acceptable delays for command signals and data signals (the recited "valid operation range"), as discussed above. Ex-1004, 4:41-44; Ex-1002, ¶145. According to *Johnson*, once a window of acceptable delays is found "the **'best'** delay value" which is "approximately in the middle of the window[,]" is identified. Ex-1004, 4:44-48; Ex-1002, ¶146. These "best" delay values represent an "optimal operation point for an integrated circuit

device." Ex-1002, ¶146; Ex-1007, 8 (this element "does not require determining the optimal operation point.").

Therefore, *Johnson* discloses Element 1.4.b. Ex-1002, ¶¶145-146. *Johnson* in view of *Jeddeloh* thus renders claim 1 obvious. Ex-1002, ¶¶109-146.

2. *Claim 2*

Johnson states that "[a] memory device containing the calibration structure and operating as described above may be used in a processor-based system" and that the memory device may be "any type of **DRAM device** including an SLDRAM." Ex-1004, 8:36-38. The processor "may itself be an integrated processor which utilizes on-chip memory devices containing the calibration structure and operates in accordance with the present invention." *Id.*, 8:38-40. Accordingly, *Johnson* discloses a memory device formed of an integrated circuit device and including DRAM memory, which is a "DRAM component." Ex-1002, ¶147.

Johnson in view of *Jeddeloh* thus renders claim 2 obvious. *Id.*

3. *Claim 3*

Johnson's system includes a "plurality of SLDRAM modules 11*a*...11*n* which are accessed and controlled by a memory controller 13" (the recited "memory controller coupled to the DRAM component"). Ex-1004, 3:30-33. *Johnson* explains that "[m]emory controller 13 provides a command link to each of the SLDRAM modules 11*a*...11*n* which includes a clock signal CCLK," bi-directional data clocks

DCLK0 and DCLK1, command signals on a command bus data path CA0-9, and data signals on a bi-directional data bus DQ0-17. *Id.*, 3:33-44. *Johnson* discloses that a control logic circuit 21 in each SDLRAM module "steps through all possible delay positions of ring delays" to determine delay values for correct sampling and recognition of the synchronization pattern. *Id.*, 3:57-60; 4:55-59; 4:36:41; Ex-1002, ¶148. Moreover, *Johnson* explains that the memory controller "achieves this timing calibration at system initialization[.]" *Id.* at 1:48-50. A POSITA would have recognized that the memory controller in *Johnson* is capable of performing the said altering as is disclosed in *Jeddeloh*. Ex-1002, ¶148.

Specifically, *Jeddeloh* describes a memory interface 122, or memory controller, that receives "data signal 202 and data strobe signal 206 from memory 104." Ex-1005, 4:39-40; Ex-1002, ¶149. As shown in Figure 2 below, the memory interface 122 is coupled to data signal 202 and system clock 204. Ex-1005, 4:41-42.

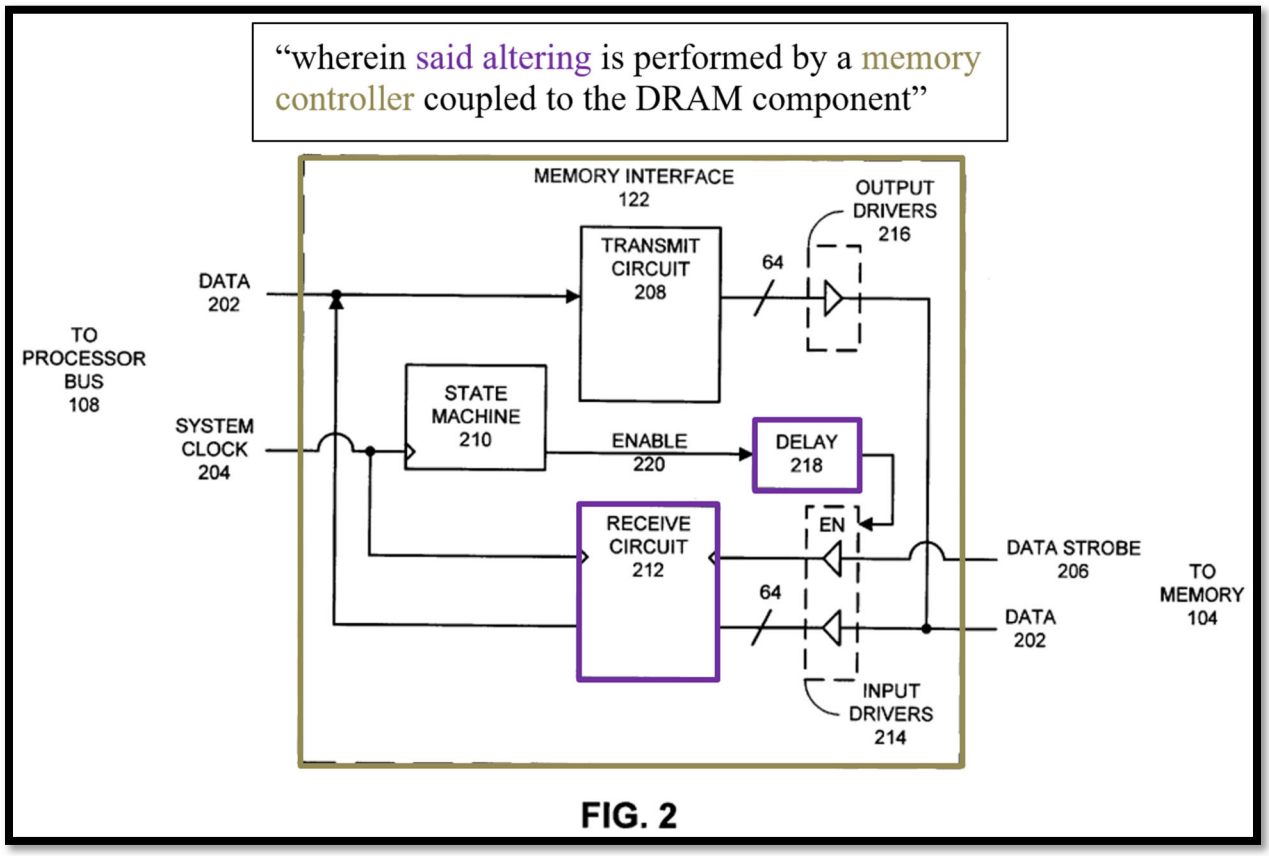


FIG. 2

Id., 3; Ex-1002, ¶149.

Jeddeloh explains that "[f]or alignment purposes, enable signal [220] passes through delay circuit 218, which can be adjusted to compensate for skew between enable signal 220 and data signal 202." Ex-1005, 5:2-6. Delay circuits 314 and 316 in the receive circuit 212 are "programmed to precisely synchronize data strobe signal 206 with data signal 202." *Id.*, 5:32-34; *see supra* Section X(A)(1). Accordingly, *Jeddeloh* teaches that "said altering is performed by a memory controller." Ex-1002, ¶¶149-151.

Johnson provides a substantially similar architecture as *Jeddeloh*, with an SLDRAM module coupled to a memory controller. *Id.*, ¶153. Additionally, a POSITA would have understood that *Johnson*'s memory controller is capable of performing synchronizing functions, such as the delays described by *Jeddeloh*. *Id.* ¶¶50-54, 154.

Moreover, a POSITA would have recognized the advantages of modifying *Johnson* such that the memory controller, instead of the control logic circuits 21 within each memory module, performs the phase shift altering. *Id.*, ¶154. In particular, a POSITA would have recognized that such a modification would consolidate the functions of multiple control logic circuits 21 within a single memory controller, thereby reducing system complexity and cost, while improving power efficiency and compatibility. *Id.* A POSITA therefore would have been motivated to incorporate *Jeddeloh*'s teachings of a memory controller altering phase signals into the memory system described by *Johnson*. *Id.*, ¶¶152-154. This combination would be nothing more than combining prior art elements (*Jeddeloh*'s memory controller with *Johnson*'s memory system) according to known methods to yield predictable results with a reasonable expectation of success. *Id.*, ¶154; *see KSR*, 550 U.S. at 415-421.

Johnson in view of *Jeddeloh* thus renders claim 3 obvious. Ex-1002, ¶¶148-154.

4. *Claim 4*

Johnson states that the "memory device may be any type of DRAM device." Ex-1004, 8:36-38. A POSITA would have understood that "any type of DRAM device" includes DDR DRAM. Ex-1002, ¶155; Ex-1012, 10. *Johnson* further states that an SLDRAM component "is a double data rate device[.]" Ex-1004, 1:26-27; *see also id.*, 2:44-47.

Additionally, to the extent Patent Owner argues that *Johnson* does not explicitly teach that the DRAM component comprises a DDR DRAM component, *Jeddeloh* teaches that its memory implements "a clocked interface that returns data along with a strobe signal for latching the data during read operations" and includes "memory implementing the DDR interface standard." Ex-1005, 3:54-56; Ex-1002, ¶156.

As would have been known by a POSITA and is described in *Johnson*, SLDRAM was a type of innovative DRAM that was comparable to and backwards compatible with DDR DRAM. Ex-1002, ¶155; Ex-1014, 1. *Johnson* describes the SLDRAM module as having similar characteristics as DDR DRAM, such as "a double data rate" data transfer. Ex-1004, 1:26-27; Ex-1002, ¶158. Both *Johnson* and *Jeddeloh* describe a device "which uses both the positive- and negative-going edges of a clock cycle to READ and WRITE data to the memory cells[.]" Ex-1004, 1:27-29; *see also* Ex-1005, 1:49-53; Ex-1002, ¶158. Incorporating *Jeddeloh*'s DDR

DRAM module in lieu of the SLDRAM module of *Johnson* would have been nothing more than simple substitution of one known element for another to obtain predictable results with a reasonable expectation of success. Ex-1002, ¶160; *Uber Techs. Inc. v. X One, Inc.*, 957 F. 3d 1334, 1339 (Fed. Cir. 2020) ("[T]wo of a finite number of known, predictable solutions" represents "a simple design choice" (citations omitted)); *see also KSR*, 550 U.S. at 415-421.

Also, *Jeddeloh* suggests that strobed memory modules, such as DDR DRAM and SLDRAM, can utilize the circuitry of "delay circuits 314 and 316 [which] can be programmed to precisely synchronize data strobe signal 206 with data signal 202." Ex-1005, 5:31-33; Ex-1002, ¶157. A POSITA would have known, and been motivated, to modify *Johnson* to incorporate DDR DRAM based on the teachings of *Jeddeloh*. Ex-1002, ¶156.

Further, a POSITA would have been motivated to incorporate DDR DRAM into the memory system of *Johnson* to realize any of several well-understood advantages. *Id.*, ¶158. For example, a POSITA would have understood that the DDR standard was already widely adopted as of November 2003. *Id.*, ¶¶40-49, ¶159; Ex-1013, 2. Adhering to the DDR standard by incorporating a DDR DRAM component would afford *Johnson*'s memory system better compatibility, availability, support, and cost efficiency. *Id.*

Johnson in view of *Jeddeloh* thus renders claim 4 obvious. Ex-1002, ¶¶155-160.

5. *Claim 5*

Johnson teaches that "a bi-directional **data bus DQ0-17** is provided between memory controller 13 and each of the SLDRAM modules 11*a*...11*n*." Ex-1004, 1:41-43. *Johnson* states that "[d]ata which is to be input to memory banks [] is supplied by memory controller 13 (FIG. 3) on the DQ data bus" (the recited "the data signals comprise a plurality of data bus (DQ) signals"). *Id.*, 2:12-18.

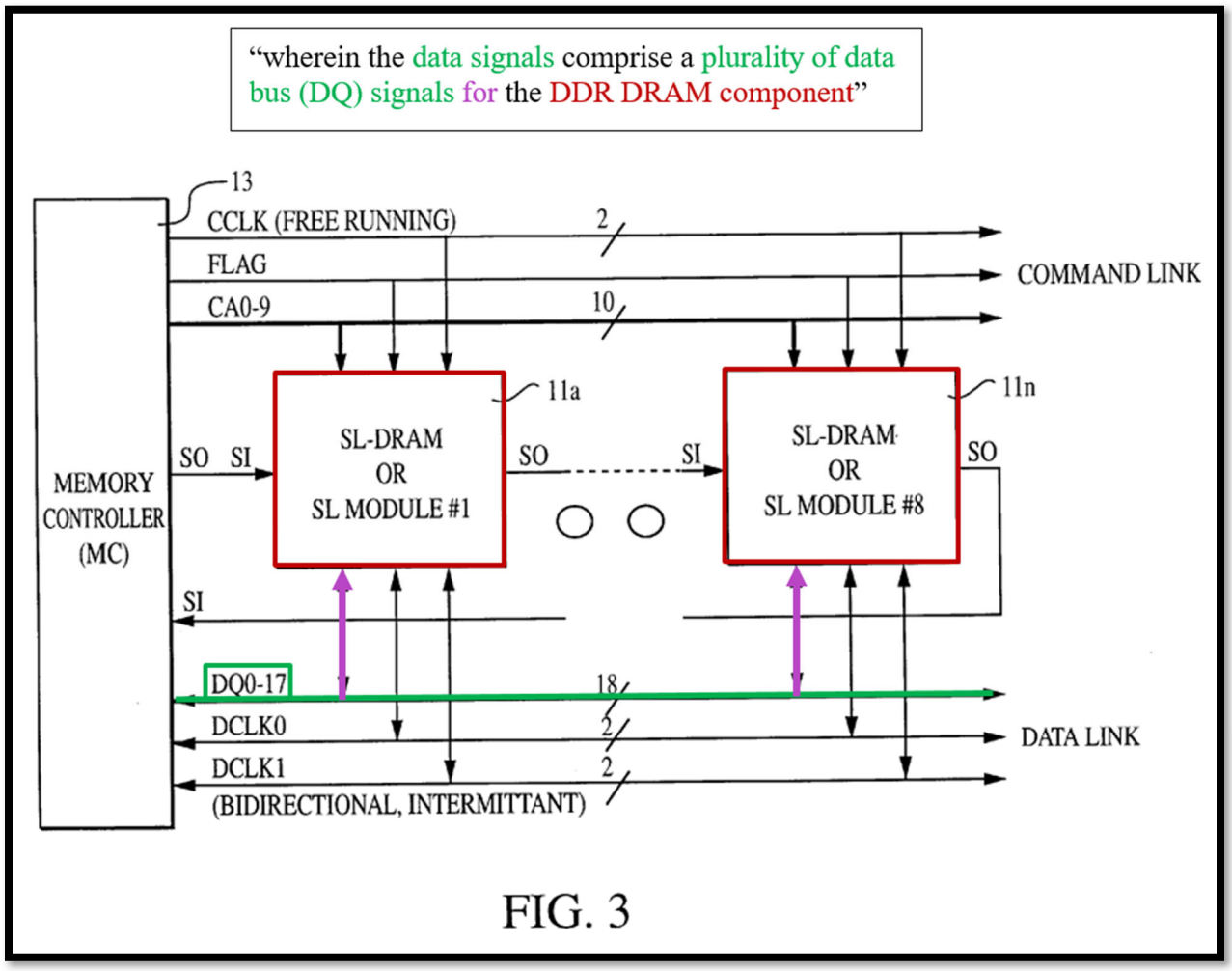


FIG. 3

Id., 3; Ex-1002, ¶162

As explained previously, *Johnson* teaches and/or renders obvious incorporating a DDR DRAM component in the memory system. *See supra* Section X(A)(4). Accordingly, a POSITA would have understood that *Johnson*'s data signals DQ on its data bus DQ0-17 would be "for the DDR DRAM component." Ex-1002, ¶164. Further, a POSITA would have been motivated to ensure that the data signals

transmitted on data bus DQ0-17 adhere to the DDR DRAM standard to ensure proper compatibility with *Jeddeloh*'s DDR DRAM component. *Id.*

Johnson in view of *Jeddeloh* thus renders claim 5 obvious. Ex-1002, ¶¶161-164.

6. *Claim 6*

Johnson discloses "a bi-directional data bus DQ0-17 is provided between memory controller 13 and each of the SLDRAM modules 11*a*…11*n*, as are bi-directional data clocks DCLK0 and DCLKI. **The clock DCLK0 is used to strobe input/output data into and out of the SLDRAM modules, a process for which the DCLK1 signal path is also intermittently used.**" Ex-1004, 3:40-47. Annotated Figure 3 below illustrates such sampling bus signals.

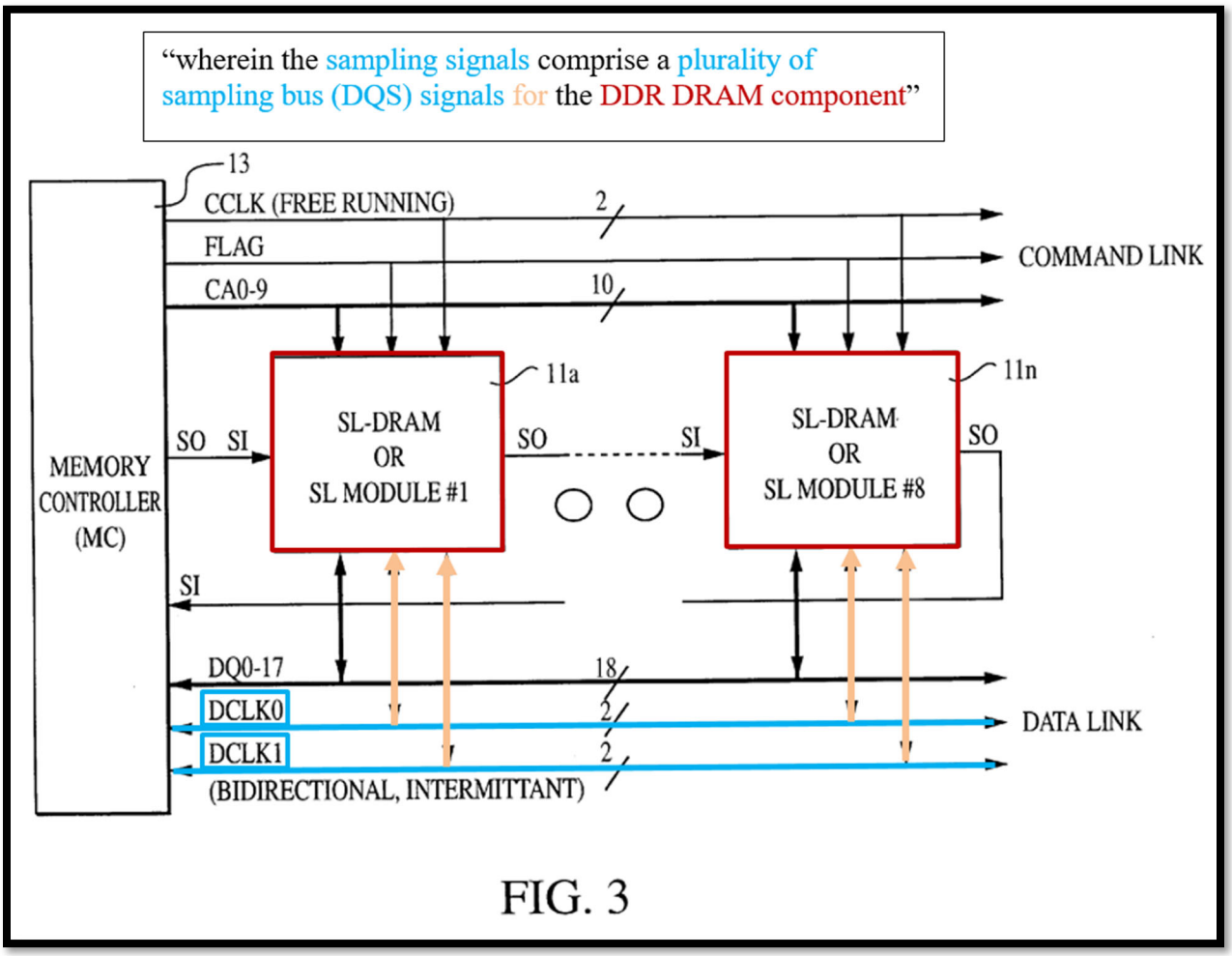


FIG. 3

Id., 3; Ex-1002, ¶166.

Johnson's control logic 21 receives clock signals including the DCLK0 and DCLK1 signals. Ex-1004, 3:60-62; Ex-1002, ¶167. "The data clock DCLK passes through gated buffer 53, delay circuit 55 and is used to control latch 59 to latch in incoming data on the data bus DQ." Ex-1004, 4:30-31. The SLDRAM circuit is "synchronized to ensure that the incoming data is properly clocked in by the clock signals CCLK and DCLK." *Id.*, 4:27-31. As an example, *Johnson* explains that "four

bits of data on a DQ path of the data bus (DBUS) are clocked in on four sequential positive and negative going transitions of the data clock signal DCLK[.]" *Id.*, 4:62-67. Further, using *Johnson*'s calibration technique, "each data path is aligned with the clock such that rising and falling edges [] of the clock are aligned with the center of the respective data eye for each data path." *Id.*, 6:21-24.

Similarly to the DCLK described in *Johnson*, *Jeddeloh* describes a "strobe signal for latching the data" for memory "implementing the DDR interface standard." Ex-1005, 3:53-56; Ex-1002, ¶168. A POSITA would have understood that *Jeddeloh*'s strobe signal for its DDR DRAM modules is a DQS signal. Ex-1002, ¶168; Ex-1021, 5. As explained previously, *Johnson* teaches and/or renders obvious incorporating a DDR DRAM component in the memory system. *See supra* Section X(A)(4). Accordingly, a POSITA would have understood that *Johnson*'s strobe signals would be "for the DDR DRAM component." Ex-1002, ¶168. Further, a POSITA would have been motivated to ensure that at least the strobe signals DCLK0 and DCLK1 are DQS signals that adhere to the DDR DRAM standard to ensure proper compatibility with *Jeddeloh*'s DDR DRAM component. *Id.*; *KSR*, 550 U.S. at 415-421.

Johnson in view of *Jeddeloh* thus renders claim 6 obvious. Ex-1002, ¶¶165-168.

7. *Claim 7*

Element 7.P

As previously explained, *Johnson* discloses a "method or automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device." *See supra* Section X(A)(1)(1.P). Additionally, *Johnson* discloses "[a]n SLDRAM **system** with which the present invention may be used is illustrated in FIG. 3." Ex-1004, 3:30-31. Thus, a POSITA would have readily understood that *Johnson* discloses a corresponding system for the calibration method. Ex-1002, ¶169.

Therefore, to the extent the preamble is limiting, *Johnson* teaches Element 7.P. *Id.*

Element 7.1

Johnson discloses "generating command signals to access an integrated circuit component." *See supra* Section X(A)(1)(1.1). Additionally, *Johnson* describes a memory controller 13 that provides command signals, as depicted in annotated Figure 3 below.

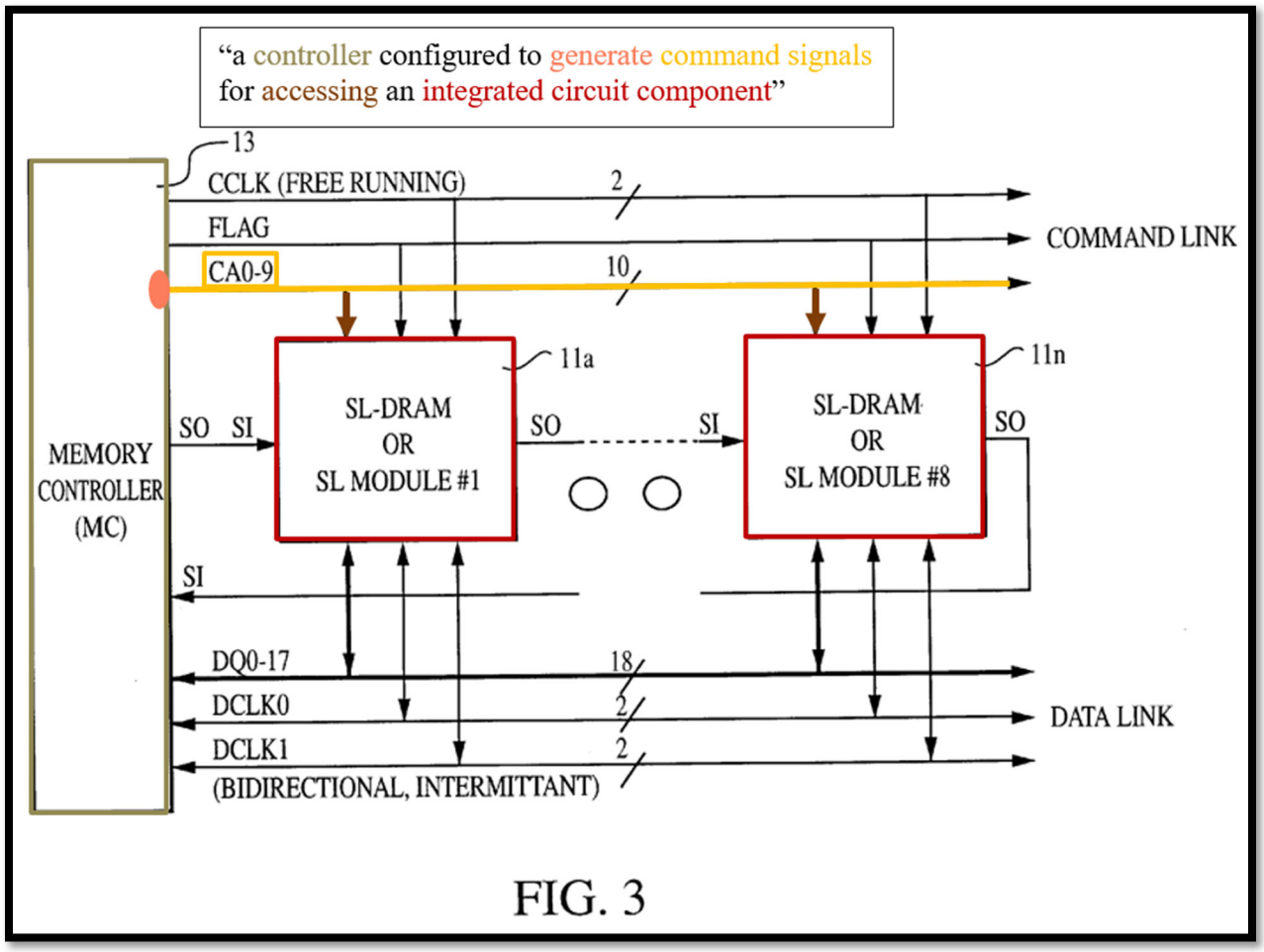


FIG. 3

Ex-1004, 3; Ex-1002, ¶170.

Johnson teaches that clock cycles are used "to READ and WRITE data to the memory cells and **to receive command** and FLAG **data from a memory controller**." Ex-1004, 1:26-30. A POSITA would have understood that *Johnson*'s SLDRAM modules 11*a*…11*n* are integrated circuit components accessed by command signals generated by the memory controller. Ex-1002, ¶¶113, 117.

Therefore, *Johnson* teaches Element 7.1. *Id.*, ¶¶170-171.

Element 7.2.a

Johnson describes a memory controller that achieves "timing calibration at system initialization." Ex-1004 at 1:48-50. To the extent Patent Owner argues that *Johnson* does not explicitly describe the components and/or circuitry of the memory controller, a POSITA would have known that the memory controller in *Johnson* includes a delay calibrator. Ex-1002, ¶172. *Johnson* explains "the data bits on each of the incoming data paths [from the memory controller to the SLDRAM module] is properly serially aligned with an edge of clock signal CCLK[.]" Ex-1004, 2:26-28. To be properly aligned with the clock signal, the data must be phase altered (e.g., delayed) within the memory controller. Ex-1002, ¶172. *Johnson* also states that the synchronization pattern is applied "by memory controller 13[.]" Ex-1004, 5:8-10. Based on *Johnson*'s description of its functionality, a POSITA would have understood that *Johnson*'s memory controller includes a delay calibrator. Ex-1002, ¶172.

Additionally, *Jeddeloh* teaches that its memory controller (e.g., memory interface 122) includes delay circuit 218 and delay circuits 314 and 316. Ex-1005, 5:2-7, 5:16-33; Ex-1002, ¶173. *Jeddeloh* explains that for "alignment purposes, enable signal [220] passes through delay circuit 218, which can be adjusted to compensate for skew between enable signal 220 and data signal 202." Ex-1005, 5:2-5. Receive circuit 212 of memory interface 122 also includes delay circuits 314 and

316. *Id.*, 3-4; Ex-1002, ¶174. The system "determines delay values to be loaded into delay circuits 218, 314 and 316" and, "[o]nce the optimal delay values are determined, the delay values are programmed into first delay circuit 218 (step 504) and a second delay circuit 314 (step 506)." Ex-1005, 6:27-35. Annotated Figure 2 below illustrates the memory interface 122 of *Jeddeloh*.

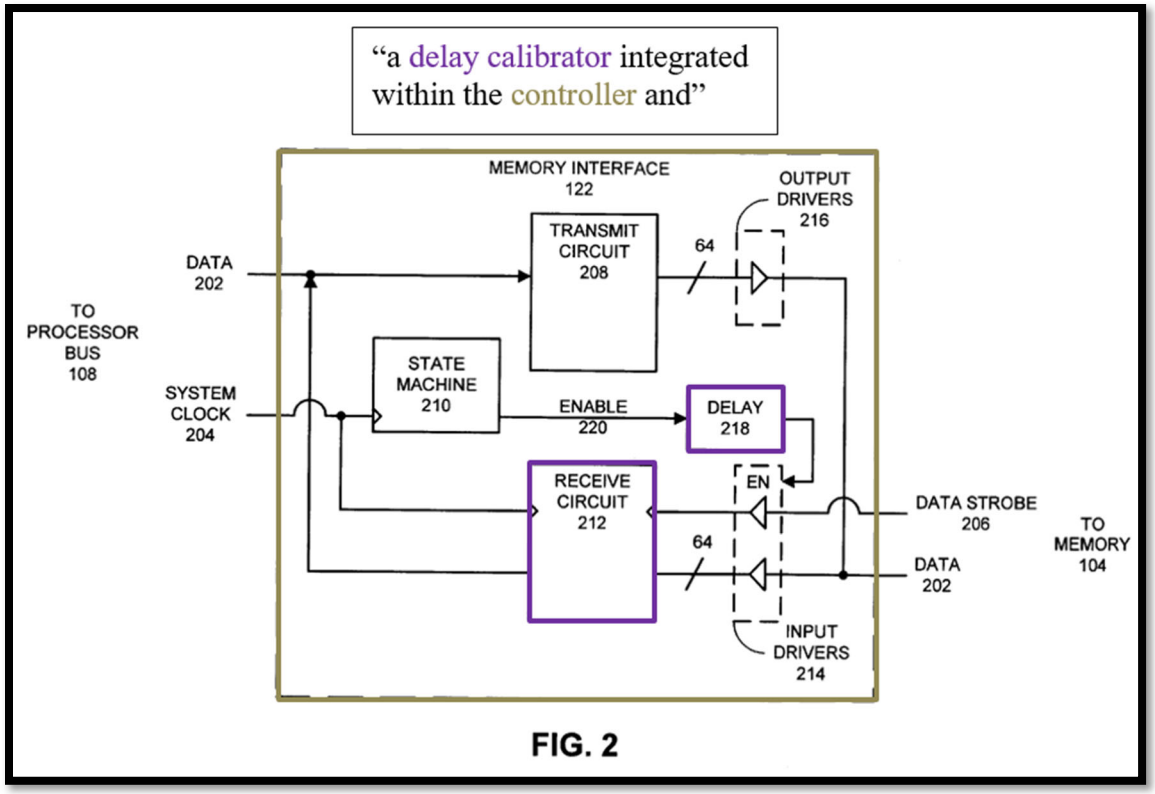


FIG. 2

Id., 3; Ex-1002, ¶174.

A POSITA would have understood that the delay circuit 218 and delay circuits 314 and 316 are delay calibrators. Ex-1002, ¶173; Ex-1020, 197 (defining "calibrate" as "to adjust precisely for a particular function").

A POSITA would have known and would have been motivated to incorporate *Jeddeloh*'s delay calibrator(s) within *Johnson*'s memory controller at least to provide pre-aligned data for transmission to the DRAM modules of *Johnson*. Ex-1002, ¶178. A POSITA would have recognized that by doing so, faster performance rates could be achieved. *Id. Johnson*'s system includes a control logic circuit 21 within the SLDRAM modules which "receives and analyzes commands on the CA0-9 bus[, FLAG signal, and clock signals CCLK and DCLK,] and controls the input/output (I/O) access operations of the memory banks 69, 71." Ex-1004, 3:57-62. A POSITA would have recognized that including a delay circuit within memory controller 13 as well would provide similar benefits at another location within the system. Ex-1002, ¶178.

Modifying *Johnson* according to *Jeddeloh* to incorporate a delay calibrator (e.g., delay circuit) within the memory controller would have been nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. Ex-1002, ¶179; *KSR*, 550 U.S. at 415-421. A POSITA would have recognized the delay circuit of *Jeddeloh* as a common component of a memory controller, and thus would have been motivated to include it within the memory controller of *Johnson*. *Id.* A POSITA would have been motivated to do so at least to provide an additional degree of alignment of signals at the memory controller beyond the alignment achieved at the DRAM

modules. *Id.*, ¶178. A POSITA would have recognized that the enhanced signal alignment would allow the system to handle signals with smaller windows of valid data, thereby enabling faster data rates and improved performance. *Id.*, ¶¶177-179.

Therefore, *Johnson* in view of *Jeddeloh* teaches Element 7.2. *Id.*, ¶¶172-179.

Element 7.2.b

Johnson discloses "accessing data signals to convey data for the integrated circuit component." *See supra* Section X(A)(1)(1.2). A POSITA would have known and would have been motivated to incorporate the delay calibrator of *Jeddeloh* into *Johnson*'s memory controller. *See supra* Section X(A)(7)(7.2.a).

A POSITA would have understood that *Jeddeloh*'s delay calibrator is configured to access data signals. Ex-1002, ¶180. *Jeddeloh* states that "memory interface 122 receives **data signal 202** and data strobe signal 206 from memory 104 (from FIG. 1)." Ex-1005, 4:39-40. *Jeddeloh* further states that "**data signal 202** and data strobe signal 206 from memory 104 passes through input drivers 214 into **receive circuit 212**." *Id.*, 4:55-56 (emphasis added). *Johnson*'s control logic circuit 21 also accesses data signals, as it is "arranged to compare a **next data path** to be calibrated to a just calibrated data path." Ex-1004, 7:25-29; Ex-1002, ¶181. Based on these disclosures, a POSITA would have understood that the memory controller and the delay calibrator of the *Jeddeloh*-modified system of *Johnson* accesses data signals. Ex-1002, ¶181.

Therefore, *Johnson* in view of *Jeddeloh* teaches Element 7.2.b. Ex-1002, ¶¶180-181.

Element 7.2.c

Johnson discloses "accessing sampling signals to control sampling of the data signals." *See supra* Section X(A)(1)(1.3). A POSITA also would have known and would have been motivated to incorporate the delay calibrator of *Jeddeloh* into *Johnson*'s memory controller. *See supra* Section X(A)(7)(7.2.a).

A POSITA would have understood that *Jeddeloh*'s delay calibrator is configured to access sampling signals. Ex-1002, ¶180. *Jeddeloh* states that "memory interface 122 receives data signal 202 and **data strobe signal 206** from memory 104 (from FIG. 1)." Ex-1005, 4:39-40. *Jeddeloh* further states that "data signal 202 and **data strobe signal 206** from memory 104 passes through input drivers 214 into **receive circuit 212**." *Id.*, 4:55-56 (emphasis added). *Johnson*'s control logic circuit 21 also accesses sampling signals, as it "receives … the **clock** [e.g., sampling] **signals CCLK, DCLK.**" Ex-1004, 7:25-29; Ex-1002, ¶183. Based on these disclosures, a POSITA would have understood that the memory controller and the delay calibrator of the *Jeddeloh*-modified system of *Johnson* accesses sampling signals for controlling sampling of the data signals. Ex-1002, ¶183.

Therefore, *Johnson* in view of *Jeddeloh* teaches Element 7.2.b. *Id.*, ¶¶182-183.

Element 7.3.a

Johnson discloses and renders obvious "systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device" *See supra* Section X(A)(1)(1.4.a); Ex-1002, ¶184. A POSITA also would have known and would have been motivated to incorporate the delay calibrator of *Jeddeloh* into *Johnson*'s memory controller. *See supra* Section X(A)(7)(7.2.a); Ex-1002, ¶184.

Jeddeloh states that its "system first determines delay values to be loaded into delay circuits 218, 314 and 316[.]" Ex-1005, 6:27-28. *Jeddeloh* explains that the BIOS code performs "test read operations using **different delay values**[.]" *Id.,* 6:30-31. The "optimal delay values" are then determined and programmed into the delay circuits. *Id.*, 6:32-35. Delay values from the middle of the valid range for the delay circuits are selected by the system. *Id.* at 7:19-24. Based on these disclosures, a POSITA would have understood that *Jeddeloh*'s delay calibrator is configured to systematically alter phase shifts. Ex-1002, ¶¶137-142. Further, a POSITA would have understood that the delay calibrator of the *Jeddeloh*-modified system of *Johnson* would be configured to systematically alter phase shifts of all of the command signals, data signals, and sampling signals. *Id.*, ¶185; *see also* Section X(A)(1)(1.4.a).

Therefore, *Johnson* in view of *Jeddeloh* renders Element 7.3.a obvious. *Id.*, ¶¶184-185.

Element 7.3.b

Johnson discloses Element 7.3.b. *See supra* Section X(A)(1)(1.4.b); Ex-1002, ¶186. *Johnson* in view of *Jeddeloh* thus renders claim 7 obvious. Ex-1002, ¶¶169-186.

8. *Claim 8*

See supra Section X(A)(2); Ex-1002, ¶187.

9. *Claim 9*

See supra Section X(A)(4); Ex-1002, ¶188.

10. *Claim 10*

See supra Section X(A)(5); Ex-1002, ¶189.

11. *Claim 11*

See supra Section X(A)(6); Ex-1002, ¶190.

12. *Claim 12*

Element 12.P

Johnson teaches a "method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device." *See supra* Section X(A)(1)(1.P). *Johnson* in view of *Jeddeloh* also teaches "determin[ing] a valid operation range of the integrated circuit

device," which is an "operating mode." *See supra* Section X(A)(1)(1.4.a); Ex-1002, ¶191. Further, *Johnson* in view of *Jeddeloh* teaches that the "altering is performed by a memory controller coupled to the DRAM component" and that the signals are "for the DRAM component." *See supra* Sections X(A)(2)-(3); Ex-1002, ¶191.

Therefore, *Johnson* in view of *Jeddeloh* teaches Element 12.P. Ex-1002, ¶191.

Element 12.1

See supra Section X(A)(1)(1.1); Ex-1002, ¶192.

Element 12.2

See supra Section X(A)(1)(1.2); Ex-1002, ¶193.

Element 12.3

See supra, Section X(A)(1)(1.3); Ex-1002, ¶194.

Element 12.4

See supra, Section X(A)(1)(1.4.a); Ex-1002, ¶195. *Johnson* in view of *Jeddeloh* therefore renders Claim 12 obvious. Ex-1002, ¶¶191-195.

13. *Claim 13*

Element 13.1

Johnson in view of *Jeddeloh* teaches "systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of" *Johnson*'s DRAM component. *See supra* Section X(A)(1)(1.4.a). *Johnson* discloses a control logic

circuit that "steps through all possible delay positions of ring delays 27 and 29 as the data sampling is performed and stores patterns representing which delay values for the ring delays 27 and 29 provide for a correct sampling." Ex-1004, 4:37-41. By stepping through all possible delay positions and identifying those that yield correct sampling, *Johnson* determines "a valid operation range." Ex-1002, ¶197.

Jeddeloh explicitly describes "a coarse delay adjustment mechanism and a fine delay adjustment mechanism" in the circuitry of the programmable delay circuit. Ex-1005, 2:40-41; Ex-1002, ¶198. *Jeddeloh* states that the input "into programmable delay circuit 400 passes through a chain of coarse delay elements 402, 404, 406 and 408. The outputs of coarse delay elements 402, 404, 406 and 408 feed into MUX 410. MUX 410 selects between the outputs of coarse delay elements 402, 404, 406 and 408 to generate an output[.]" Ex-1005, 5:65-6:4. This multiplexer is controlled by coarse delay component 424, thus the delay circuit has a coarse adjustment through MUX 410. *Id.*, 6:10-14; Ex-1002, ¶198. Annotated FIG. 4 below illustrates the programmable delay circuit 400.

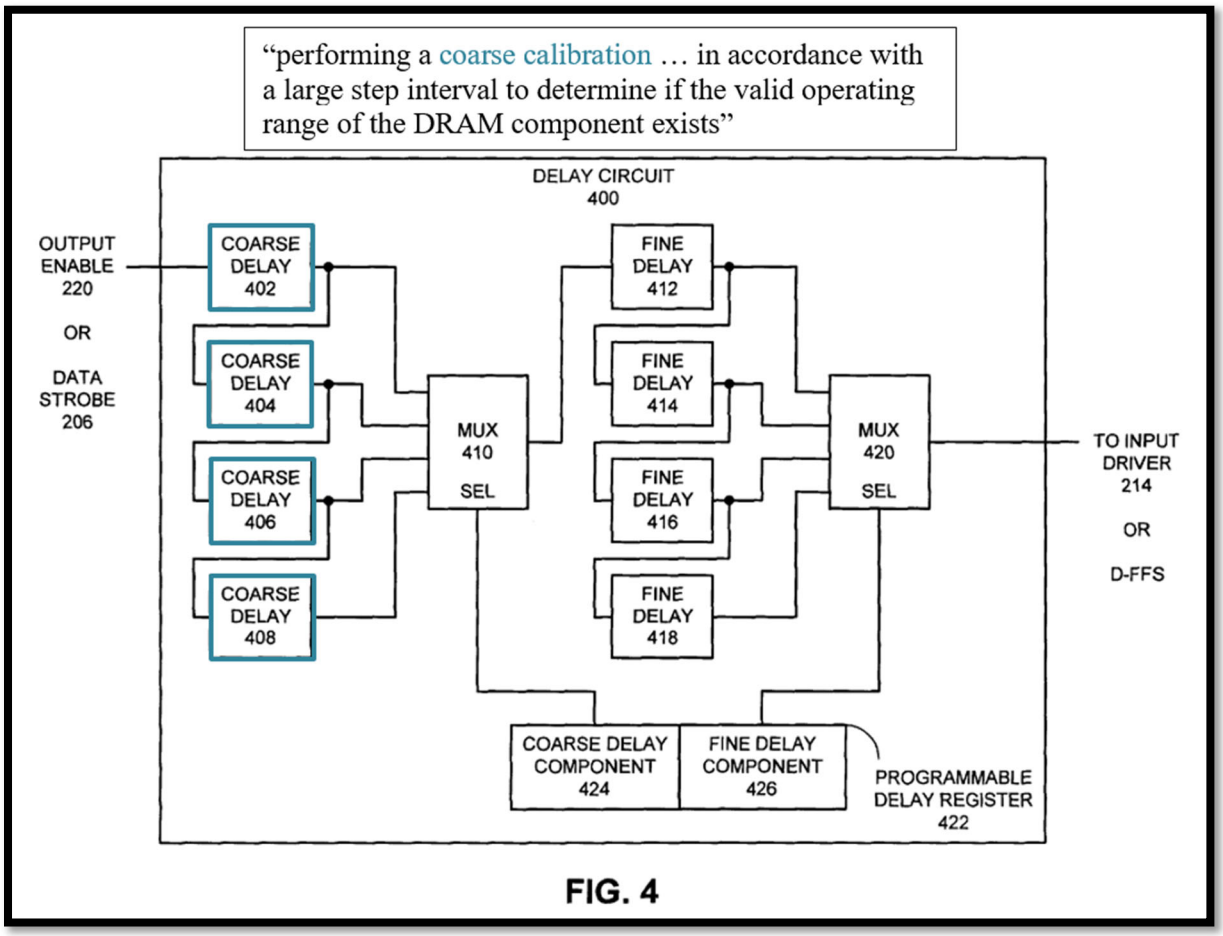


FIG. 4

Ex-1005, 5; Ex-1002, ¶198.

The "[p]rogrammable delay circuit 400 represents the internal structure of delay circuit 218 [] or delay circuits 314 and 316," all of which are in *Jeddeloh*'s memory interface 122. Ex-1005, 5:54-58; *see also id.*, 4:56-60, 5:2-7, 5:16-33; Ex-1002, ¶¶89-91. A POSITA would have understood *Jeddeloh*'s "coarse delay adjustment mechanism" configured to perform coarse adjustments does so with a large step interval. Ex-1002, ¶199.

A POSITA would have known to incorporate the coarse delay circuitry of *Jeddeloh* into the delay elements taught by *Johnson* that are configured to alter the phase shift of the command and data signals. Ex-1002, ¶200. Indeed, a POSITA would have recognized that it was common practice to first perform a coarse adjustment to find an acceptable range of values before a fine adjustment to find a more precise range as this has been widely practiced long before the filing of the '835 Patent. *Id.*, ¶¶201-202; Ex-1018, 1. For example, *Jeddeloh* describes initializing "the first delay value and the second delay value to their lowest possible values[.] Ex-1005, 7:7-9. The system then attempts to read a written value to determine if "the read operation [is] successful." *Id.*, 7:12-14. The values are incremented and, once the system has attempted "all possible combinations of delay values," the system "selects a first [and a second] delay value in the middle of a **valid range of first [and second] delay values** [respectively.]" *Id.*, 7:14-24. A POSITA would have understood that selecting delay values in the "valid range" includes "determin[ing] if the valid operating range of the DRAM component exists." Ex-1002, ¶200.

A POSITA would have also been motivated to incorporate the coarse delay elements of *Jeddeloh* into the system of *Johnson* at least to reduce the total number of incremental adjustments performed, thereby improving the efficiency and speed of *Johnson*'s calibration. *Id.* Including the coarse delay elements of *Jeddeloh* within

the memory controller of *Johnson* to alter a phase shift of the sampling signals, data signals, and command signals would have been nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. *Id.*; *KSR*, 550 U.S. at 415-421.

Therefore, *Johnson* in view of *Jeddeloh* teaches Element 13.1. Ex-1002, ¶¶197-202.

Element 13.2

Johnson teaches that, once a window of acceptable delays is established, "the control logic circuit 21 **determines the 'best' delay value** as that value which is approximately in the middle of the window." Ex-1004, 4:46-48. The circuit "notes those delays which produce a coincidence of the calibration pattern on data paths DQ<0> and DQ<1>, and **selects a final delay value for delay 57b** which is at or near the center of acceptable delays." *Id.* at 7:54-57. A POSITA would have understood that *Johnson*'s "best" delay value is an optimal operating mode. Ex-1002, ¶145.

With reference to Figure 4, *Jeddeloh* explains that "MUX 410 selects between the outputs of coarse delay elements 402, 404, 406 and 408 to generate an output that feeds into a chain of fine delay elements 412, 414, 416 and 418." Ex-1005, 6:2-8. "The outputs of fine delay elements 412, 414, 416 and 418 feed into MUX 420." *Id.* "MUX 420 selects between the outputs of fine delay elements 412, 414, 416 and

418 to generate an output for delay circuit 400." *Id.* Fine delay component 426 controls MUX 420 such that delay circuit 400 has a fine adjustment through MUX 420. *Id.*, 6:10-14. Annotated Figure 4 below shows multiple fine delay elements.

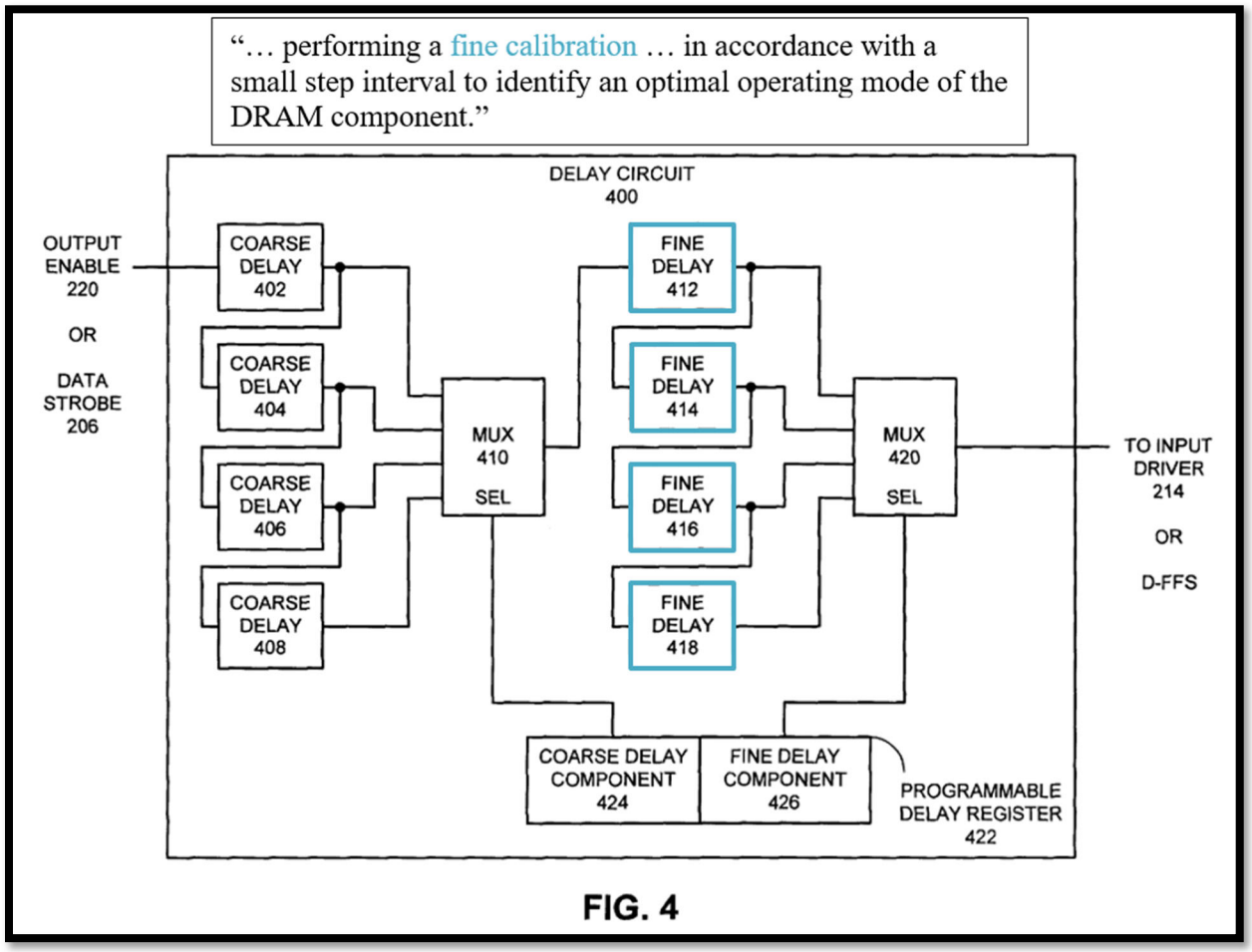


FIG. 4

Id., 5; Ex-1002, ¶203.

As explained previously, a POSITA would have known and would have been motivated to include *Jeddeloh*'s coarse delay circuitry in the system of *Johnson*. *See supra* Section X(A)(13)(13.1). For the same reasons, a POSITA would have appreciated using a coarse calibration with a subsequent fine calibration to find an

optimal mode (i.e., *Johnson*'s "best" delay value). Ex-1002, ¶205. Accordingly, modifying *Johnson* to include the fine delay elements of *Jeddeloh* would have been nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. *Id.*; *KSR*, 550 U.S. at 415-421.

Therefore, *Johnson* in view of *Jeddeloh* teaches Element 13.2. Ex-1002, ¶¶203-205. *Johnson* in view of *Jeddeloh* thus renders claim 13 obvious. *Id.*, ¶¶197-205.

14. *Claim 14*

Johnson teaches that an optimal delay is achieved by "adjusting the temporal position of the received data bits to achieve a desired bit alignment relative to the clock" which is "accomplished by adjusting a delay in the receiving path of the received data until the received data is properly sampled by the clock and recognized internally." Ex-1004, 1:59-64.; Ex-1002, ¶206. The control logic 21 of *Johnson* "establishes an 'eye' or 'window' of acceptable delays for each of the ring delays 27 for the command data paths CA0-9 and for ring delay 29 for the FLAG input path." Ex-1004, 4:41-43.

Similar to calibration with a large (e.g., coarse) step interval, a POSITA would have recognized that identifying a general range of acceptable delay values is a form of coarse calibration. Ex-1002, ¶207. Additionally, *Jeddeloh* explicitly teaches a

plurality of coarse delay elements that provide varying delay values. *See supra* Section X(A)(13)(13.1). A POSITA would have understood to choose a percent step increase for the coarse calibration that allows for rapid calibration while also finding an acceptable range of delay values. Ex-1002, ¶208. In particular, a POSITA would have recognized that "a five percent step increase" is suitable for the coarse calibration at least because such a configuration would test at most 20 delay possibilities per cycle, allowing the system to quickly find the general range of acceptable delay values. *Id.* Selecting a percentage step increase that results in testing a reasonably low integer quantity of delay values would have amounted to a design choice from a finite number of known, predictable solutions with a reasonable expectation of success. *Id.*; *Uber Techs.*, 957 F. 3d at 1339. Selecting a step increase of five percent—to test 20 delay values—would have been obvious to a POSITA to try. *Id.*; *KSR*, 550 U.S. at 415-421.

A POSITA would have also understood that *Johnson*'s phase shift calibration for the respective signals would occur "simultaneously." Ex-1002, ¶209. *Johnson*'s calibration technique is performed at initialization (e.g., start-up or reset). Ex-1004, 1:36-40; Ex-1002, ¶209. Thus, such calibration would occur all at once and before the memory system is utilized to ensure proper functionality of the memory system. Ex-1002, ¶209. A POSITA would therefore have understood that *Johnson*'s system performs calibration of the phase shifts all at initialization, i.e. simultaneously. *Id*.

Johnson in view of *Jeddeloh* thus renders claim 14 obvious. *Id.*, ¶¶206-209.

15. *Claim 15*

The optimal delay in *Johnson* is achieved by "adjusting the temporal position of the received data bits to achieve a desired bit alignment relative to the clock" which is "accomplished by adjusting a delay in the receiving path of the received data until the received data is properly sampled by the clock and recognized internally." Ex-1004, 1:59-64. After a window of acceptable delays is established, the control logic 21, "determines the 'best' delay value as that value which is approximately in the middle of the window." Ex-1004, 4:46-48; Ex-1002, ¶211.

Similar to a calibration with a small (e.g., fine) step interval, a POSITA would have recognized that finding the "best" value is a form of fine calibration. Ex-1002, ¶211. Additionally, *Jeddeloh* explicitly teaches that a plurality of fine delay elements provide varying delay values. *See supra* Section X(A)(13)(13.2). A POSITA would have understood to choose a relatively smaller percentage step increase that allows for a precise calibration process after a range of acceptable values is determined. Ex-1002, ¶211. In particular, a POSITA would have recognized that "a two percent step increase" is suitable for the fine calibration at least because such a configuration would allow for identification of delay values skipped over during the coarse calibration. *Id.*, ¶¶211-212. Selecting a percentage step increase that is smaller than a five percent step increase would have amounted to a design choice from a finite

number of known, predictable solutions with a reasonable expectation of success. *Id.*; *Uber Techs.*, 957 F. 3d at 1339. Selecting a step increase of two percent for fine calibration would have been obvious to a POSITA to try. *Id.*; *KSR*, 550 U.S. at 415-421.

Additionally, a POSITA would have recognized that varying the phase shifts "one at a time" would conserve system resources during the calibration process and would allow the system to test delay values independently of other system changes. *Id.*, ¶212. Varying the delay values one at a time, as opposed to simultaneously, would have amounted to nothing more than choosing from a finite number of identified, predictable solutions, with a reasonably expectation of success. *Id.*; *Uber Techs.*, 957 F. 3d at 1339.

Johnson in view of *Jeddeloh* thus renders claim 15 obvious. *Id.*, ¶¶210-212.

16. *Claim 16*

Johnson discloses determining an "eye" or "window" of acceptable delays for command signals and data signals. Ex-1004, 4:41-44. Once a window of acceptable delays is found, "the **'best'** delay value" which is "approximately in the middle of the window[,]" is identified (the recited "optimal operating mode"). *Id.*, 4:44-48; Ex-1002, ¶213. *Johnson* further discloses that, control logic circuit 21 "**selects as a final delay for ring delay 29** a delay value which is approximately in the center of those delay values, e.g., D4...D7, which produced a proper recognition." Ex-1004, 5:66-

6:3. Additionally, *Jeddeloh* teaches that when "**optimal delay values are determined, the delay values are programmed into first delay circuit 218** (step 504) and a second delay circuit 314 (step 506)." Ex-1005, 6:32-35.

A POSITA therefore would have readily understood that the *Jeddeloh*-modified memory controller of *Johnson* would be configured to "operate the DRAM component in the optimal operating mode." Ex-1002, ¶213. As previously explained, the *Jeddeloh*-modified memory controller of *Johnson* would be nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. *Id.*, ¶213; *KSR*, 550 U.S. at 415-421.

Therefore, *Johnson* in view of *Jeddeloh* renders claim 16 obvious. *Id.*

17. *Claim 17*

See supra Section X(A)(4); Ex-1002, ¶214.

18. *Claim 18*

See supra Section X(A)(5); Ex-1002, ¶215.

19. *Claim 19*

See supra Section X(A)(6) ; Ex-1002, ¶216.

20. *Claim 20*

Element 20.P

As explained previously, *Johnson* in view of *Jeddeloh* teaches "[i]n a memory controller, a method for finding an operating mode for a DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component." *See supra* Section X(A)(12)(12.P). *Johnson* in view of *Jeddeloh* also teaches that the DRAM component is a DDR DRAM component. *See supra* Section X(A)(4).

Johnson further discloses that the "memory device containing the calibration structure [] may be used in a **processor-based system**" that "comprises **a processor 94, a memory device 96 [which contains the calibration structure], and an I/O (input/output) device 92**." *Id.*, 8:29-36. A POSITA would have readily understood that a calibration system as described in *Johnson* and *Jeddeloh* would utilize executable instructions stored on a computer readable media accessible by *Johnson*'s processor. Ex-1002, ¶217. A POSITA in particular would have understood that the executable instructions could be stored on a thumb drive, hard drive, or other similar computer readable media and made accessible to the processor via I/O device 92. *Id.* Such a configuration would have been nothing more than a combination of prior art elements according to known methods to yield predictable results with a reasonable expectation of success. *Id.*; *KSR*, 550 U.S. at 415-421.

Therefore, *Johnson* in view of *Jeddeloh* teaches Element 20.P. *Id.*

Element 20.1

Johnson in view of *Jeddeloh* teaches "generating command signals to access a DRAM component," and that the DRAM component is a "DDR DRAM component." *See supra* Sections X(A)(4), X(A)(12)(12.1). Therefore, *Johnson* in view of *Jeddeloh* teaches Element 20.1. Ex-1002, ¶218.

Element 20.2

Johnson in view of *Jeddeloh* teaches "accessing data signals to convey data for the DRAM component," that the DRAM component is a "DDR DRAM component," and that the data signals comprise "DQ signals." *See supra* Sections X(A)(4), X(A)(5), X(A)(12)(12.2). Therefore, *Johnson* in view of *Jeddeloh* teaches Element 20.2. Ex-1002, ¶219.

Element 20.3

Johnson in view of *Jeddeloh* teaches "accessing sampling signals to control sampling of the data signals," that the data signals comprise "DQ signals," and that sampling signals comprise DQS signals. *See supra* Sections X(A)(1)(1.1), X(A)(5)-(6). Therefore, *Johnson* in view of *Jeddeloh* teaches Element 20.3. Ex-1002, ¶220.

Element 20.4

Johnson in view of *Jeddeloh* teaches "systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the

sampling signals to determine a valid operating range of the DRAM component." *See supra* Section X(A)(12)(12.4). *Johnson* in view of *Jeddeloh* further teaches that the DRAM component is a DDR DRAM component, that the data signals include "DQ signals," and that the sampling signals include "DQS signals." *See supra* Sections X(A)(4)-(6). Therefore, *Johnson* in view of *Jeddeloh* teaches Element 20.4 and renders claim 20 obvious. Ex-1002, ¶¶217-221.

21. *Claim 21*

Element 21.1

See supra Sections X(A)(4), X(A)(13)(13.1); Ex-1002, ¶¶222-224.

Element 21.2

See supra Sections X(A)(4), X(A)(13)(13.2); Ex-1002, ¶¶225-226.

22. *Claim 22*

See supra Section X(A)(16); Ex-1002, ¶227.

23. *Claim 23*

Element 23.P

Johnson in view of *Jeddeloh* teaches "[i]n a memory controller, a method for finding an operating mode for a DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component." *See supra* Section X(A)(12)(12.P). *Johnson* in view of

Jeddeloh also teaches that the DRAM component is a "DDR DRAM component." *See supra* Section X(A)(4).

By the filing of the '835 Patent, using PCBs to connect computer components, such as DDR DRAM components, to other components such as controllers and processors was extremely well known in the art. Ex-1002, ¶¶41-42; 228; Ex-1009, 1; Ex-1010, 15. A POSITA would have been well aware of the practice of using PCBs to connect components of a memory system. *Id.*, ¶¶41-42, 229. Indeed, arranging a DDR DRAM component on a PCB would amount to nothing more than substituting one known element (*Johnson*'s integrated circuit) for another (a PCB connecting multiple components) to obtain predictable results (a functional memory system). *Id.*, ¶¶228-229; *KSR*, 550 U.S. at 415-421.

Therefore, *Johnson* in view of *Jeddeloh* teaches Element 23.P. *Id.*, ¶¶228-229.

Element 23.1

See supra Section X(A)(20)(20.1); Ex-1002, ¶230.

Element 23.2

See supra Section X(A)(20)(20.2); Ex-1002, ¶231.

Element 23.3

See supra Section X(A)(20)(20.3); Ex-1002, ¶232.

Element 23.4

See supra Section X(A)(20)(20.4); Ex-1002, ¶233. Additionally, a POSITA would have readily understood that signals transmitted between a memory controller and DRAM modules in the *Jeddeloh*-modified memory system of *Johnson* would be transmitted via the PCB. Ex-1002, ¶229.

Therefore, *Johnson* in view of *Jeddeloh* teaches Element 23.4 and renders claim 23 obvious. *Id.*, ¶¶228-233.

B. Ground 2: Claims 1-3, 7-8, and 12 are obvious over *Johnson* in view of *Keeth*.

1. *Claim 1*

Element 1.P

See supra Section X(A)(1)(1.P); Ex-1002, ¶¶234-235.

Element 1.1

See supra Section X(A)(1)(1.1); Ex-1002, ¶236.

Element 1.2

See supra Section X(A)(1)(1.2); Ex-1002, ¶237.

Element 1.3

See supra Section X(A)(1)(1.3); Ex-1002, ¶238.

Element 1.4.a

See supra Section X(A)(1)(1.4.a); Ex-1002, ¶239.

To the extent Patent Owner argues that *Johnson* does not explicitly disclose or render obvious the recited "systematically altering [] a phase shift of the sampling signals," *Keeth* teaches this element. Ex-1002, ¶239. *Keeth* discloses a similar memory system, which includes a command bus 28 "for carrying address and control information from memory controller 22 to the DRAM modules," and a bi-directional data bus 32 for "carrying write data from memory controller 22 to the DRAM modules and further carrying read data from the DRAM modules to memory controller 22." Ex-1006, 3:44-56. A "free-running clock (CCLK) [is] provided on a clock line 30 from memory controller 22" (the recited "sampling signals") and two bi-directional data clocks DCLK0 and DCLK1 (the recited "sampling signals") "are respectively provided on clock line 34 and clock line 36." *Id.*; Ex-1002, ¶241. Annotated Figure 1 below illustrates the sampling signals (blue) and the data signals (green).

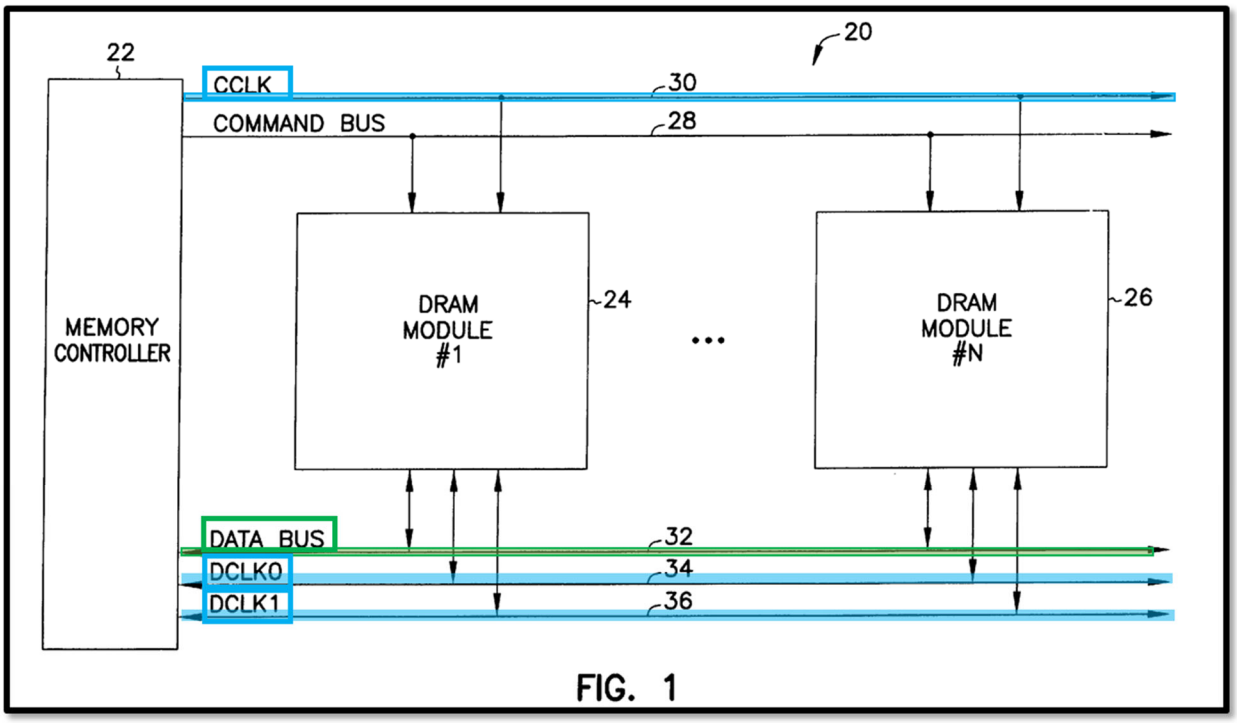


FIG. 1

Ex-1006, 4; Ex-1002, ¶241.

Keeth discloses vernier clock adjustment for memory systems to compensate for "effects of duty cycle variation, bus position of a given memory device, timing drift, loading variations, clock jitter, clock skew, noise, overshoot, and ringing" by individually adjusting "rising-edge and falling-edge timings, either independently or interdependently from each other." Ex-1006, 1:51-59. Specifically, *Keeth* states that "each DRAM includes a variety of vernier adjustment circuits which compensate" for variability in signal timing "to permit read data from all DRAMs to arrive at memory controller 22 within fixed, deterministic timing, and similarly permit write data to arrive with fixed, deterministic timing to the selected DRAM devices." *Id.*, 7:41-46; Ex-1002, ¶242.

Keeth teaches that a vernier clock adjustment circuit 60 is used to adjust the timing of DCLK0 or DCLK1 for a read operation. Ex-1002, ¶247. *Keeth* teaches that the "rising edge and falling edge transitions of the selected DCLK are employed to clock the input latches of the [] memory controller receiving data." Ex-1006, 3:61-63. Vernier clock adjustment circuit 60 is configured as shown in Figure 9 to produce a delayed version of the active DCLK used for rising edge clockings and a delayed version of the active DCLK used for falling edge clockings. *Id.*, 10:6-17; Ex-1002, ¶245. A POSITA would have recognized that delaying the active DCLK signals is "altering a phase shift of…the sampling signals." Ex-1002, ¶248. Annotated Figure 7 below shows the vernier delay 60 (purple) that performs the altering and the sampling signals (blue).

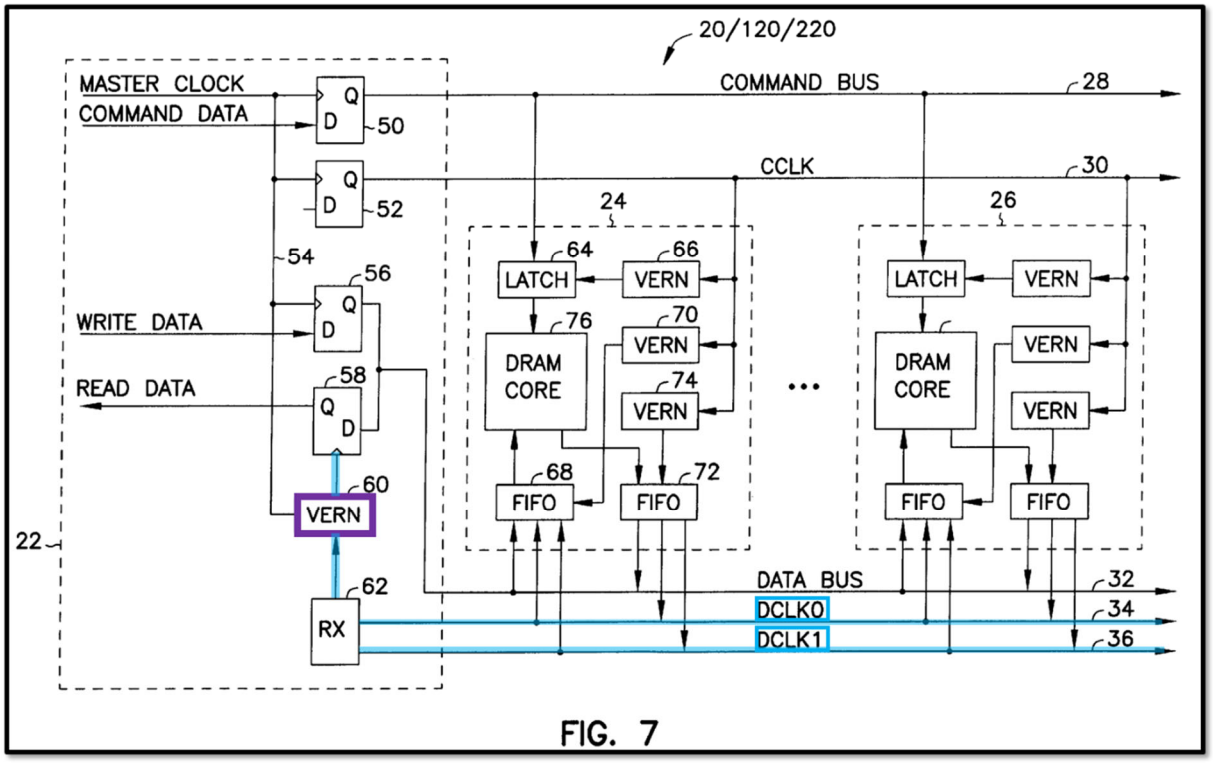


FIG. 7

Ex-1006, 10; Ex-1002, ¶248.

Additionally, vernier clock adjustment circuits 70 and 74 are used in write and read operations, respectively, to adjust the timing of CCLK, which controls sampling of data signals at DRAM module 24. Ex-1002, ¶249. *Keeth* states that a "write first-in, first-out (FIFO) buffer 68 receives the DCLK0 and DCLK1 clock signals from lines 34 and 36 and the write data from data bus 32 and provides write data to a DRAM core 76." Ex-1006, 7:9-12. During write operations, write FIFO buffer 68 samples data signals from data bus 32 before the data is written to DRAM core 76. Ex-1006 at 7:10-12. Similarly, a "read FIFO buffer 72 receives read data from DRAM core 76 and provides the read data to data bus 32 along with the DCLK0 and

DCLK1 clock signals to clock lines 34 and 36." *Id.* at 7:15-18. The read FIFO buffer 72 "receives a delayed CCLK clock from a read vernier clock adjustment circuit 74," which is used to clock read FIFO buffer 72. *Id.*, 7:20-22; 9:15-18. Because write FIFO buffer 68 and read FIFO buffer 72 are both clocked by CCLK, CCLK controls, at least in part, sampling of the data signals read from and written to DRAM core 76. *Id.* at 7:12-20. CCLK is therefore a "sampling signal." Ex-1002, ¶249.

Vernier clock adjustment circuits 70 and 74 are configured to produce delayed versions of CCLK used to clock write FIFO buffer 68 and read FIFO buffer 72. Ex-1006, 10:6-17, Ex-1002, ¶251. The delayed versions of CCLK ensure proper timing of write FIFO buffer 68 and read FIFO buffer 72. *Id.* A POSITA would have recognized that delaying the CCLK signal is "altering a phase shift of…the sampling signals." *Id.* Annotated Figure 7 below shows the vernier clock adjustment circuits 70 and 74 and corresponding CCLK signals.

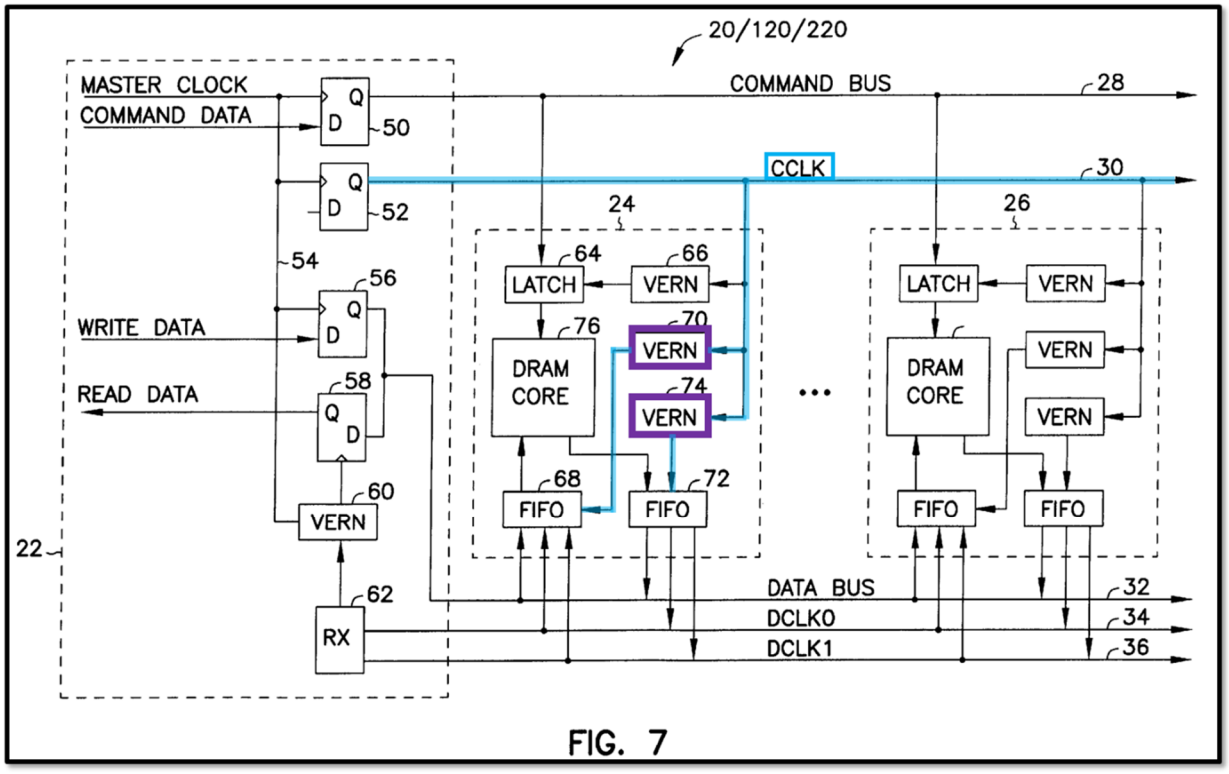


FIG. 7

Ex-1006, 10; Ex-1002, ¶251.

Keeth explains that the memory system adjusts the vernier delays by "run[ning] through all delay steps of the vernier circuit and determin[ing] when data misses on low adjustments and on high adjustments." Ex-1006, 7:66-8:5. The system then "sets the vernier adjustment in an approximated optimal middle setting." *Id.* Alternatively, *Keeth* states that the memory system "includes a feedback controller used to set the vernier settings by first selecting an estimated optimal setting and allowing the controller and feedback circuitry to arrive at the optimal delay setting for the vernier clock adjustment circuit." *Id.*, 8:5-9. A POSITA would have recognized that either manner of adjusting the vernier delays amounts to

"systematically altering." Ex-1002, ¶246; Ex-1020, 1230 (defining "systematic" as "methodical in procedure or plan").

A POSITA would have recognized the advantages of modifying *Johnson* to systematically alter a phase shift of sampling signals, as taught by *Keeth*. Ex-1002, ¶255. As an initial matter, both *Johnson* and *Keeth* list Micron Technology, Inc. as Assignee and both references share Brent Keeth as a common inventor. Ex-1004; Ex-1006; Ex-1002, ¶252. *Johnson* already describes delaying the sampling signals CCLK and DCLK. Ex-1004, 1:57-59, 4:1-3; 4:24-26; Ex-1002, ¶¶141-142. A POSITA would have been motivated to make such a modification at least to improve synchronization of data signals and sampling signals when both writing to and reading from DRAM banks. Ex-1002, ¶255. *Johnson* shows that CCLK passes through a delay lock loop 41. Ex-1004, 4; Ex-1002, ¶1423. To the extent that *Johnson* does not explicitly explain how CCLK is synchronized to the data signals received from the DRAM banks, a POSITA would have had reason to look to *Keeth* for specificity as to how to synchronize data signals received from the DRAM banks to the sampling signals used to latch them. Ex-100, ¶254.

Modifying the calibration process of *Johnson* to include sampling signal vernier delay adjustments of *Keeth* would have been nothing more than using a known technique (e.g., adjusting sampling signals per *Keeth*) to improve similar devices (e.g., the memory system of *Johnson*) in the same way to correct alignment

of signals in a memory device. *Id.,* ¶256; *KSR*, 550 U.S. at 415-421. Accordingly, it would have been obvious to a POSITA to modify the calibration process of *Johnson* to incorporate the sampling signal adjustments of *Keeth*. *Id.*

Therefore, *Johnson* and *Keeth*, at least in combination, disclose Element 1.4.a. Ex-1002, ¶¶239-256.

Element 1.4.b

See supra Section X(A)(1)(1.4.b); Ex-1002, ¶257. *Johnson* in view of *Keeth* therefore renders claim 1 obvious. *Id.*, ¶¶235-257.

2. *Claim 2*

See supra Section X(A)(2); Ex-1002, ¶258.

3. *Claim 3*

See supra Section X(A)(3); Ex-1002, ¶259.

Keeth states that "adjustments to vernier clock adjustment circuit 66, 70, 74 in each DRAM device is made by writing a delay value in a register located in each DRAM device." Ex-1006, 7:47-50. *Keeth* explains that memory controller 22 "writes the vernier delay control register of read vernier clock adjustment circuit 74 or otherwise sets the delay of the read vernier clock adjustment circuit to increase the delay until read delay data can be optimally sampled." *Id.*, 8:49-55. *Keeth* further states that "[m]emory controller 22 correspondingly adjusts the read vernier clock adjustment circuits of each of the DRAM modules through the Nth DRAM module

26." *Id.*, 8:56-58. *Keeth*'s "memory controller 22 adjusts memory controller vernier clock adjustment circuit 60" that is located within the memory controller. *Id.*, 8:40-42. Accordingly, *Keeth*'s vernier clock adjustment circuits are controlled by *Keeth*'s memory controller, which a POSITA would have understood to be "said altering is performed by a memory controller." Ex-1002, ¶¶261-262.

Johnson provides a substantially similar architecture as *Keeth*, with an SLDRAM module coupled to a memory controller. *Id.*, ¶¶260-261. Indeed, combining *Johnson* with *Keeth* in this way would be nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. *Id.*, ¶263. Additionally, a POSITA would have understood that *Johnson*'s memory controller is capable of performing synchronizing functions, such as the delays described by *Keeth*. *Id.*, ¶260.

Moreover, a POSITA would have recognized the advantages of modifying *Johnson* such that the memory controller, instead of the control logic circuits 21 within each memory module, performs the phase shift altering. *Id.*, ¶263. In particular, a POSITA would have recognized that such a modification would consolidate *Johnson*'s the functions of multiple control logic circuits 21 within a single memory controller. *Id.* Such consolidation would reduce system complexity and cost, while improving power efficiency and compatibility. *Id.* A POSITA

therefore would have been motivated to incorporate *Keeth*'s teachings of a memory controller altering signal phases into the memory system described by *Johnson*. *Id.*

Johnson in view of *Keeth* thus renders claim 3 obvious. Ex-1002, ¶¶259-263.

7. *Claim 7*

Element 7.P

See supra Section X(A)(7)(7.P); Ex-1002, ¶264.

Element 7.1

See supra Section X(A)(7)(7.1); Ex-1002, ¶265.

Element 7.2.a

See supra Section X(A)(7)(7.2.a).

As explained previously, *Johnson* and *Keeth* teach that "said altering is performed by a memory controller coupled to the DRAM component." *See supra* Section X(B)(3); Ex-1002, ¶266. As the memory controller of the *Keeth*-modified memory system of *Johnson* calibrates delays of the signals, the memory controller includes a "delay calibrator integrated within the controller." Ex-1002, ¶¶266-267.

Element 7.2.b

The delay calibrator integrated within the *Keeth*-modified memory controller of *Johnson* meets this element for the same reasons that *Johnson*'s memory controller does. *See supra* Section X(A)(1)(1.2); Ex., 1002, ¶268.

Element 7.2.c

The delay calibrator integrated within the *Keeth*-modified memory controller of *Johnson* meets this element for the same reasons that *Johnson*'s memory controller does. *See supra* Section X(A)(1)(1.2); Ex., 1002, ¶269.

Element 7.3.a

The delay calibrator integrated within the *Keeth*-modified memory controller of *Johnson* meets this element for the same reasons that *Johnson*'s memory controller does. *See supra* Sections X(B)(1)(1.4.a), X(B)(3); Ex-1002, ¶¶270-271.

Element 7.3.b

See supra Section X(A)(1)(1.4.b); Ex-1002, ¶272.

8. *Claim 8*

See supra Sections X(A)(2); Ex-1002, ¶273.

9. *Claim 12*

Element 12.P

See supra Sections X(A)(1)(1.P), X(A)(2), X(B)(3); Ex-1002, ¶274.

Element 12.1

See supra Section X(A)(1)(1.1); Ex-1002, ¶275.

Element 12.2

See supra Section X(A)(1)(1.2); Ex-1002, ¶276.

Element 12.3

See supra Section X(A)(1)(1.3); Ex-1002, ¶277.

Element 12.4

See supra Section X(B)(1)(1.4.b); Ex-1002, ¶278. *Johnson* in view of *Keeth* therefore renders Claim 12 obvious. Ex-1002, ¶¶274-278.

C. Ground 3: Claims 4-6, 9-11, and 13-19 are Obvious Over *Johnson* in View of *Keeth* and *Jeddeloh*

As previously explained, *Johnson* in view of *Keeth* renders claims 1-3, 7-8, and 12 obvious. *See supra* Section X(B). As also previously explained, *Johnson* in view of *Jeddeloh* teaches all elements of dependent Claims 4-6, 9-11, and 13-19, and therefore renders those claims obvious. *See supra* Section X(A).

A POSITA would have recognized the benefits of modifying, and would have been motivated to modify, the *Johnson-Keeth* memory system described in Section X(B) to conform to the DDR standard for the same reasons previously explained. *See supra* Sections X(A)(4)-(6). A POSITA would have also recognized the benefits of modifying, and would have been motivated to modify, the *Johnson-Keeth* memory system described in Section X(B) to include *Jeddeloh*'s coarse delay and fine delay circuitry. *See supra* Sections X(A)(13)-(16). For at least these same reasons, the combination of *Johnson*, *Keeth*, and *Jeddeloh* renders dependent claims 4-6, 9-11, and 13-19 obvious. Ex-1002, ¶¶279-281.

XI. ARGUMENTS FOR DISCRETIONARY DENIAL SHOULD BE REJECTED.

A. Section 325(d) Is Inapplicable Because the Asserted Art Was Never Evaluated During Examination.

The Board should not deny institution under § 325(d) because the art asserted here was not identified during prosecution or before the Examiner, and is not cumulative of art that was. As set forth below, the Examiner either (1) was not presented with the same or substantially the same art or arguments as Petitioner's, or (2) materially erred in allowing the Challenged Claims. *Advanced Bionics, LLC v. Med-El Elektromedizinische Gerate GmbH*, IPR2019-01469, Paper 6, 8 (P.T.A.B. Feb. 13, 2020) (citing *Becton, Dickinson, & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017)).

Advanced Bionics Analysis Step 1. Neither "the same [nor] substantially the same" art or arguments were previously presented to the Office during prosecution of the Challenged Claims. *Advanced Bionics*, IPR2019-01469, Paper 6, 8, 10 (*Becton, Dickinson* "factors (a), (b), and (d)" relate to whether "the same or substantially the same art or arguments previously were presented to the Office."). *Johnson, Jeddeloh,* and *Keeth* were never cited during prosecution of the '835 Patent, let alone considered by the Examiner or used in any rejection. *See generally* Ex.-1003. These references are also not substantially the same or cumulative of references considered during examination. To the extent Patent Owner argues that

Keeth is cumulative of US 6,016,282 ("Keeth '282"), Keeth '282 was never considered by the Office for its disclosure of "systematically altering [] a phase shift of the sampling signals." Keeth '282 was only considered for its disclosure of "coarse delay adjustments" and "fine delay adjustments." *See* Ex-1003, 108-122, 154-158, 167-180, 216, 257-269, 293-303.

Advanced Bionics Analysis Step 2. To the extent the Board disagrees and determines that the first step of the *Advanced Bionics* analysis does not favor institution, discretionary denial still is not warranted because the Examiner must have necessarily overlooked invalidating disclosures of the art that was examined, constituting material error. *Advanced Bionics*, IPR2019-01469, Paper 6, 10 (listing silence as evidence of error and stating *Becton, Dickinson "*factors (c), (e), and (f) relate to whether the petitioner has demonstrated a material error by the Office"). As stated above in detail, *Johnson* in combination with *Jeddeloh* and/or *Keeth,* teaches every element of the Challenged Claims and renders the Challenged Claims obvious. To the extent any reference that was examined could be considered cumulative of these prior art references, the Examiner should have rejected the Challenged Claims at least under Section 103 and maintained the rejection(s).

Accordingly, the Board should reach the merits of this petition, and institute review of all Challenged Claims, especially in light of the accompanying expert testimony, which was not before the Office during prosecution.

B. Any Secondary Considerations Cannot Overcome the Strong Evidence of Obviousness.

The Board, at the institution phase, has repeatedly held that evidence of secondary considerations presented by the Patent Owner should be addressed in a trial where the parties may develop, and the Board may consider, a full record. *See*, e.g., *Tristar Products, Inc. v. Choon's Design, LLC*, IPR2015-01883, Paper 6, 26 (P.T.A.B. Mar. 9, 2016). That is the appropriate course here, especially given that "the inventions represent[] no more than 'the predictable use of prior art elements according to their established functions,'" and, thus any "secondary considerations are inadequate to establish nonobviousness as a matter of law." *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1246 (Fed. Cir. 2010) (quoting *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007)).

C. Institution is Proper Under Section 314(a) and *Fintiv*.

The merits of this Petition are strong, which alone warrants institution. Petitioner also hereby stipulates that, if institution is granted, Petitioner will not raise in the co-pending litigation any defense based on the same grounds raised, or that could have been raised, in this Petition. This stipulation precludes discretionary denial under Section 314(a). Director Vidal, Memorandum, "Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court

Litigation," at 4-5, 7-8 (June 21, 2022) ("the PTAB will not discretionarily deny institution if Petitioner presents a *Sotera* stipulation.").

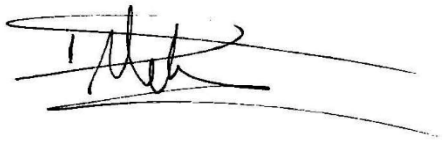
XII. PRESERVATION OF RIGHTS

Petitioner reserves all rights to any benefit of changes resulting from challenges based on the recent Supreme Court decision in *Loper Bright*. *Loper Bright Enters. v. Raimondo*, No. 22-451, slip op. at 35 (U.S. June 28, 2024).

XIII. CONCLUSION

For the reasons above, Petitioner requests institution of IPR of the Challenged Claims based on all grounds.

Respectfully submitted,



Dated: August 2, 2024

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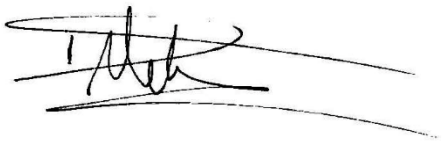
CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,646,835 contains, as measured by the word-processing system used to prepare this paper, 13,974 words. This word count does not include the items excluded by 37 C.F.R. § 42.24.

Dated: August 2, 2024

Respectfully submitted,



By: _____
Dinesh N. Melwani (Reg. No. 60,670)
Counsel for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105(a), I hereby certify that on August 2, 2024, I caused a true and correct copy of the foregoing "PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 7,646,835 B1" and supporting exhibits to be served via Federal Express on the Patent Owner at the following correspondence address of record and/or likely to effect service:

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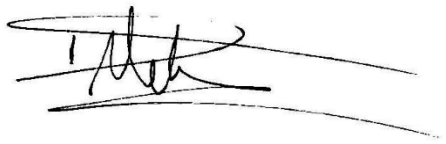
Dated: August 2, 2024

Respectfully submitted,



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