UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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REOLINK DIGITAL TECHNOLOGY CO., LTD.
Petitioner,

v.

KT IMAGING US, LLC
Patent Owner

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Case No. IPR2024-01154
U.S. Patent No. 8,314,481

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**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,314,481**

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# I. INTRODUCTION

Reolink Digital Technology Co., Ltd. ("Petitioner" or "Reolink Digital") requests *inter partes* review of claims 1–3 of U.S. Patent No. 8,314,481 ("the '481 patent") (Ex. 1001) assigned to KT Imaging US, LLC ("Patent Owner" or "PO" or "KTI"). For the reasons below, the Board should find the challenged claims unpatentable.

# II. MANDATORY NOTICES

## A. Real Parties-in-Interest

The real party-in-interest is Reolink Digital Technology, Co., Ltd.

## B. Related Matters

The '481 patent is at issue in *KT Imaging USA, LLC v. Reolink Digital Technology Co., Ltd.*, 6-22-cv-00876 (WDTX), filed August 22, 2022 ("WDTX case"). The '481 patent was also asserted in the following matters:

| Case | Filing Date |
|---|---|
| *KT Imaging USA, LLC v. Panasonic Corporation*, 4-19-cv-00485 (EDTX) | 7/3/2019 |
| *KT Imaging USA, LLC v. Kyocera Corporation*, 4-19-cv-00488 (EDTX) | 7/3/2019 |
| *KT Imaging USA, LLC v. Acer America Corporation*, 6-20-cv-00299 (WDTX) | 4/20/2020 |
| *KT Imaging USA, LLC v. Dynabook, Inc.*, 4-20-cv-00333 (EDTX) | 4/20/2020 |

| | |
|---|---|
| *KT Imaging USA, LLC v. ASUSTek Computer Inc.*,<br>6-20-cv-00300 (WDTX) | 4/20/2020 |
| *KT Imaging USA, LLC v. HP Inc.*,<br>4-20-cv-00337 (EDTX) | 4/20/2020 |
| *KT Imaging USA, LLC v. Samsung Electronics Co., Ltd.*, 4-20-cv-00339 (EDTX) | 4/20/2020 |
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| *KT Imaging USA, LLC v. Shenzhen Wansview Technology Co., Ltd.*,<br>6-22-cv-00877 (WDTX) | 8/22/2022 |
| *KT Imaging USA, LLC v. Axis Communications AB*,<br>1-22-cv-08240 (SDNY) | 9/27/2022 |
| *KT Imaging USA, LLC v. Hangzhou Hikvision Digital Technology Co., Ltd.*,<br>6-22-cv-01026 (WDTX) | 10/3/2022 |
| *KT Imaging USA, LLC v. Zhejiang Dahua Technology Co., Ltd.*,<br>4-22-cv-03440 (SDTX) | 10/6/2022 |

### C. Counsel and Service Information

Lead counsel: Timothy C. Bickham (Reg. No. 41,618); Backup Counsel: (1) Stephen Yang (Reg. No. 70,589); (2) Chris (Zheng) Liu (Reg. No. 67,862); (3) Mark Consilvio (Reg. No. 72,065). Service information: Dentons US, LLP, 1900 K Street NW, Washington, DC 20006; Tel: 202.496.7500; Fax: 202.496.7756; email: ipt.docketchi@dentons.com. Petitioner consents to electronic service.

## III. PAYMENT OF FEES

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 30827.

## IV. GROUNDS FOR STANDING

Petitioner certifies that the '481 patent is available for review and Petitioner is not barred or estopped from requesting review on the grounds identified herein. Petitioner files this request less than a year after it waived service in the WDTX case. *See Motorola Mobility LLC v. Patent of Michael Arnouse*, Case IPR2013-00010, Paper 20 (January 30, 2013) (informative decision) ("[W]here the petitioner waives service of a summons, the one-year time period begins on the date on which such a waiver is filed."). "As the Board has recognized, a complaint *improperly served* does not trigger the § 315(b) time bar." *GoPro, Inc. v. 360Heros, Inc.*, IPR2018-01754, Paper 38 at 14 (PTAB Aug. 23, 2019) (precedential decision) (quoting *IpDatatel, LLC v. ICN Acquisition, LLC*, Case IPR2018-01823, Paper 17 at 10–18

(PTAB Apr. 17, 2019) (interpreting "served" in § 315(b) to require compliance with Rule 4 of the Federal Rules of Civil Procedure ("FRCP")). Indeed, as the Federal Circuit stated in *Click-To-Call*, "the text of § 315(b) clearly and unmistakably considers only the date on which the petitioner, its privy, or a real party in interest was properly served with a complaint." 899 F.3d 1321, 1332 (Fed. Cir. 2018).

Plaintiff KTI filed a complaint on August 22, 2022 in U.S. District Court for the Western District of Texas alleging patent infringement by Petitioner Reolink Digital. KTI then ineffectively attempted to serve Petitioner by mailing a copy of the summons and the complaint to a Hong Kong address that is not registered to Petitioner or any agent of Petitioner. (*See* Ex 1030, 2.) KTI attempted to serve Petitioner at an address where it does not maintain a place of business and has no association to the business located at the Hong Kong address. (*Id*., 2, 4.) The service attempt also did not comply with Rule 4 of the Federal Rules of Civil Procedure. (*Id*.) Notably, KTI did not attempt to serve Petitioner at its principle place of business in Shenzhen, China. KTI was nevertheless able to obtain a judgement of default against Petitioner on June 23, 2023. (*Id*., 2.)

After learning of the default judgement, counsel for Petitioner signed a waiver of the service of summons on July 5, 2023. (*Id*., 4.) On July 14, 2023, Petitioner timely moved to set aside the default judgement. (*Id*., 1.) KTI did not oppose the motion. On July 17, 2023, the district court granted Petitioner's motion and set aside

the default judgement. (Ex. 1031, 1.) The court accepted the waiver of service and ordered Petitioner to file its Answer to the Complaint by August 4, 2023. (*Id*.) The court and the parties have proceeded based on the July 5, 2023 waiver of service date.

## V. PRECISE RELIEF REQUESTED

Petitioner respectfully requests cancellation of claims 1–3 of the ’481 patent based on the following grounds:

**Ground 1**: Claims 1–2 are anticipated under pre-AIA 35 U.S.C. § 102(b) as by U.S. Application Publication No. 2003/0071332 (“Hsu”).

**Ground 2**: Claims 1–3 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 6,262,479 (“Chou”) and Hsu.

**Ground 3**: Claims 1–3 are anticipated under pre-AIA 35 U.S.C. § 102(e) as by U.S. Application Publication No. 2006/0008939 (“Chen”).

The application for the ’481 patent was filed on May 18, 2005. (Ex. 1001, 1.) Hsu was published on April 17, 2003. Chou issued on July 17, 2001. Therefore, Hsu and Chou qualify as prior art at least under pre-AIA 35 U.S.C. § 102(b). Chen was filed on Jul. 8, 2004, was published on Jan. 12, 2006, and has a different inventive entity than the ’481 patent. Therefore, Chen qualifies as prior art under pre-AIA 35 U.S.C. § 102(e).

Hsu and Chou were not considered during prosecution of Application No. 11/131,727 (which led to the ’481 patent). (*See generally* Ex. 1004.)

Although Chen was found by the examiner and the basis of a rejection, the examiner erred in withdrawing that rejection. To overcome the Chen reference, applicant submitted an “Affidavit of Common Ownership” (Hsin Affidavit) from one inventor who is listed as a coinventor for both the Chen publication and ’481 patent.[1] (Ex. 1004, 123.) The total content of Hsin Affidavit is provided below:

I ___HSIN, Chung Hsien _____ being duly sworn, depose and say that I am an inventor of the invention disclosed but not claimed in U.S. Publication No. 2006/0008939. I am also an inventor of the invention disclosed within U.S. Patent Application 11/131,727.

I certify that the information presented in this affidavit and true and correct to the best of my knowledge.

(Ex. 1004, 123.) Based on the bare assertion of being listed as coinventor for both the Chen reference and the ’727 application, the applicant argued that the Chen reference was not “by another” and therefore does not qualify as prior art under (pre-

[1] The Chen patent publication lists four coinventors: (1) Abnet Chen; (2) Tony Wang; (3) Chung Hsien Hsin; and (4) Figo Hsieh. The ’602 Patent also lists four coinventors, three of which are different from Chen: (1) Chung Hsien Hsin; (2) Yves Huang; (3) Kevin Chang; and (4) Chief Lin.

AIA) 35 U.S.C. § 102(e). (Ex. 1004, 118–119.) The examiner then allowed the '727 application to issue.

The examiner clearly erred in withdrawing the Chen reference, presumably because of the Hsin Affidavit. Although a rejection can be overcome by a showing that the reference invention is not by "another," a naked assertion of inventorship and that fails to provide any context, explanation or evidence to support that assertion is insufficient to show that the relied-upon subject matter was the inventor's own work. *See EmeraChem Holdings, LLC v. Volkswagen Grp. of Am., Inc.*, 859 F.3d 1341, 1345 (Fed. Cir. 2017) (finding that inventor declaration insufficient because "[n]othing in the declaration itself, or in addition to the declaration, provides any context, explanation, or evidence to lend credence to the inventor's bare assertion" made many years since the alleged events occurred).

The Hsin Affidavit submitted near eight years after filing of Chen patent application does nothing but invoke what was already apparent from the face of the two applications, namely that Hsien is a coinventor to both. That is not sufficient to provide that the challenged claims were not "by another."

It has been long held that different inventive entities, such as is the case with Chen and the '481 patent, leads to the presumption that the invention is "by another" for the purposes of § 102(e)—the mere listing an inventor in common is not enough. Indeed, the Court of Appeals for the Federal Circuit has stated:

> to decide whether a reference patent is "by another" for the purposes of 35 U.S.C. § 102(e), the Board must (1) determine what portions of the reference patent were relied on as prior art to anticipate the claim limitations at issue, (2) evaluate the degree to which those portions were conceived "by another," and (3) decide whether that other person's contribution is significant enough, when measured against the full anticipating disclosure, to render him a joint inventor of the applied portions of the reference patent.

*Duncan Parking Techs., Inc. v. IPS Grp., Inc.*, 914 F.3d 1347, 1358 (Fed. Cir. 2019). Nothing in the Hsin Affidavit speaks to the requisite analysis. Accordingly, the applicant did not make a showing sufficient to disqualify Chen as prior art and the examiner erred in issuing the '481 patent over Chen.

Petitioner's full statement of the reasons for the relief requested is set forth in detail below, and is supported by the Declaration of R. Jacob Baker, Ph.D., P.E. (Ex. 1002, ¶¶14–83), expert in the field of the '481 Patent (*id*., ¶¶5–13; Ex. 1003).

## VI. THE '481 PATENT

### A. Problem Purportedly Addressed

The '481 patent is directed to a substrate structure for an image sensor package. (Ex. 1001, 1:8–12; *see also* Ex. ¶¶26–30.) The '481 patent purports to improve the reliability of the package as compared to a prior art image sensor arrangement. (*Id*. at 1:13–55.) In essence, the '481 describes filling in gaps between electrodes in an image sensor package with an insulation material that may otherwise

allow "particles and wet air from [the surrounding] atmosphere" to enter the image sensor package. (*See id.*)

The '481 patent illustrates a "prior art" image sensor package, where a lower surface of a frame layer 18 is adhered to an upper surface 22 of a substrate 10. (Ex. 1001, 1:14–33, FIG 1 (below).) A plurality of first electrodes 15 are formed on the substrate 10 and a plurality of second electrodes 16 are formed on a second surface 14. (*Id.*)

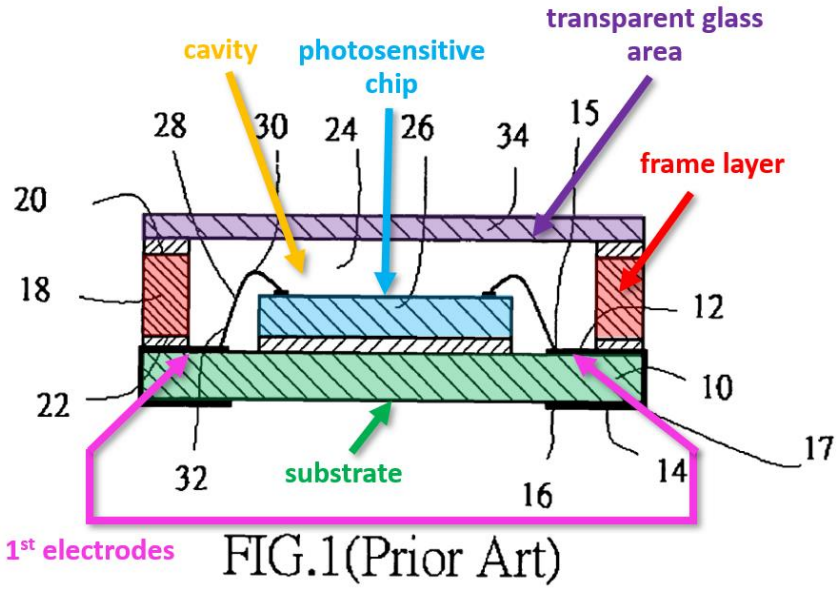


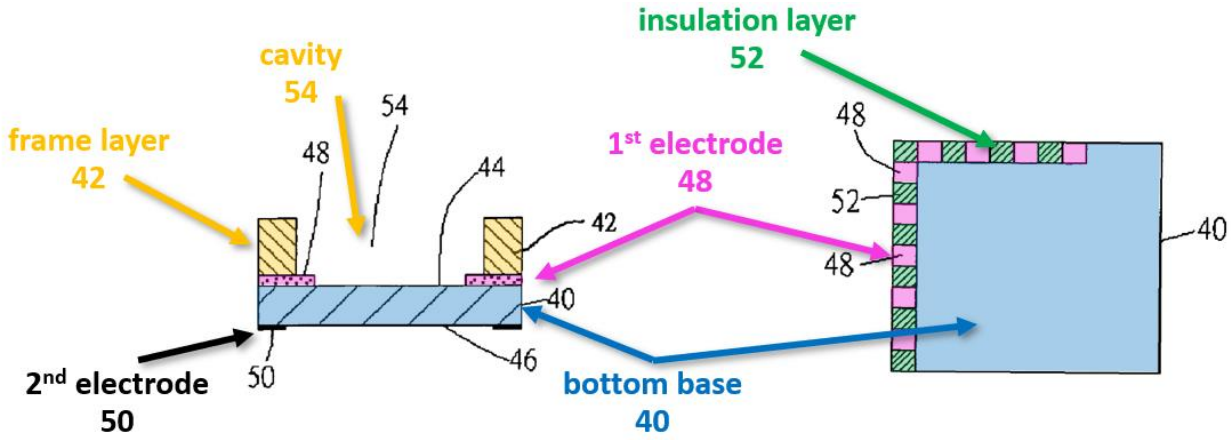
FIG.1(Prior Art)

(Ex. 1001, FIG. 1.)[2]

According to the '481 patent, this "prior art" arrangement undesirably allows particles or wet air to enter through passages between the first electrodes. (Ex. 1001, 1:34–37.) And this purportedly reduces the reliability of the image sensor. (*Id.*) To

[2] All color annotations throughout are added unless noted otherwise.

address this issue, the '481 patent proposes including an insulation layer between the first electrodes. (Ex. 1001, 2:6–24.) As shown below, insulation layer 52 is placed between first electrodes 48. (*Id.*, FIGs. 2–3.)




(Ex. 1001, FIG. 2, 3.)

Yet, notwithstanding the assertions of the '481 patent, all of the features recited in the challenged claims were already known in the art. (Ex. 1002, ¶¶22–30, 33–83) And, as discussed in more detail below, the same techniques presented as novel in the '481 patent had in fact already been disclosed in the prior art. (*Id.*)

### B. Level of Ordinary Skill in the Art

In the corresponding WDTX action between the same parties, KTI alleges that a person having ordinary skill in the art at the time of the alleged invention ("POSA") would have had (1) a Master of Science degree in engineering, with approximately two years of experience with semiconductor or image sensor packaging; or (2) a Bachelor of Science degree in engineering with approximately four years of experience with semiconductor or image sensor packaging. Petitioner and its expert,

Dr. Baker, adopts KTI's definition solely for the purposes of this proceeding. (Ex. 1002 at ¶¶20–21.)

### C. Claim Construction

In the corresponding WDTX action between the same parties, the Court ruled that the preamble of claim 1, *i.e.* "[a] substrate structure for an image sensor package," was not limiting and therefore did not require construction. (Ex. 1032, 20–23.) No other terms of the '481 were construed.

For IPR proceedings, the Board applies the claim construction standard according to *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). See 83 Fed. Reg. 51,340-59 (Oct. 11, 2018). Under *Phillips*, claim terms are typically given their ordinary and customary meanings, as would have been understood by a POSA at the time of the invention. *Phillips*, 415 F.3d at 1313; *see also id*., 1312-16. The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

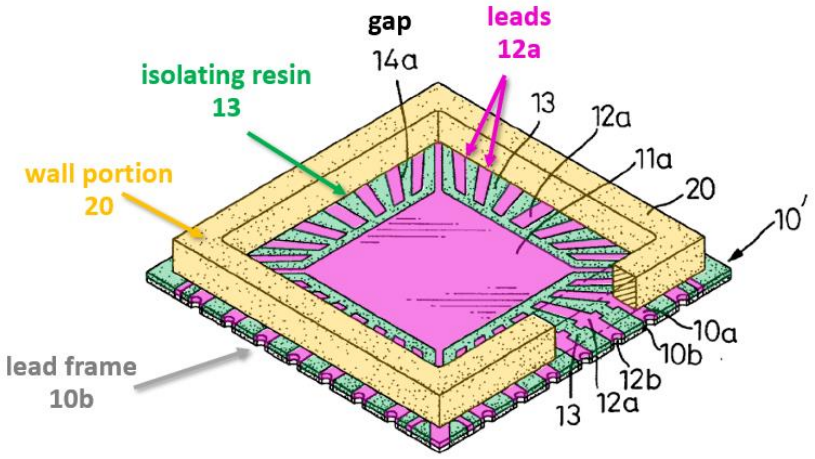
## VII. OVERVIEW OF THE PRIOR ART

### A. Overview of the Prior Art

#### 1. Hsu (Ex. 1005)

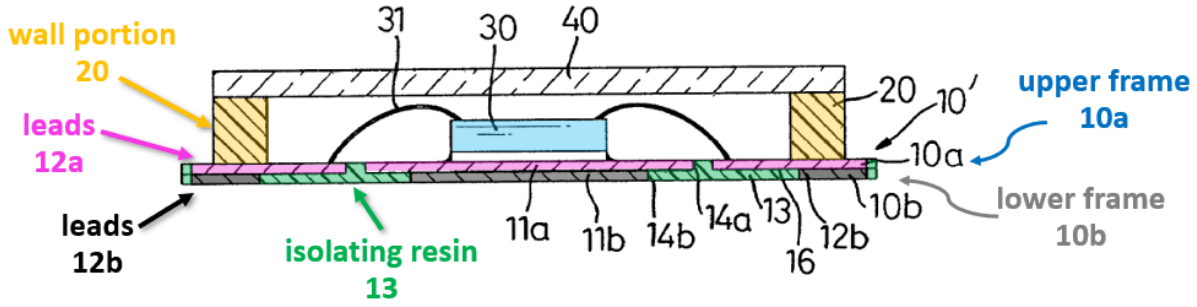
Like the ’481 patent, Hsu is directed to a semiconductor packaging structure, particularly one that is easy to fabricate, incurs a low production cost and has a good heat dissipation. (Ex. 1005, ¶0002; *see also* Ex. 1002, ¶¶33–41.) Hsu’s substrate structure looks to improve upon the prior art substrate structures, nearly identical to the conventional image sensor package described by the ’481 patent. (*Compare* Ex. 1001, ¶¶0004–0006, FIGs. 1 and 2 *with* Ex. 1005, ¶¶0003–0006, FIGs. 13 and 14.) In particular, Hsu recognizes the susceptibility of the prior art image sensor packages to moisture. (*See*, *e.g.*, Ex. 1005, ¶0007 (“Since the substrate is made of epoxy resin, the substrate is easy to absorb moisture, and the chip mounted on the substrate would be affected by the moisture, so that the stability of the chip is reduced.”).)

To address this and other deficiencies, Hsu proposes several embodiments of a semiconductor packaging structure. (Ex. 1005, ¶¶0028–0041.) A fifth embodiment of a semiconductor packaging structure is illustrated below, where a wall portion 20 is arranged on an upper leads 12a and isolation resin 13.




(Ex. 1005, FIG. 8 (a perspective view of the fifth embodiment).)

In the fifth embodiment, a metal frame (10′) is combined by an upper lead frame (10a) and a lower lead frame (10b) through a thermal-compress process. (Ex. 1005, ¶0036.)



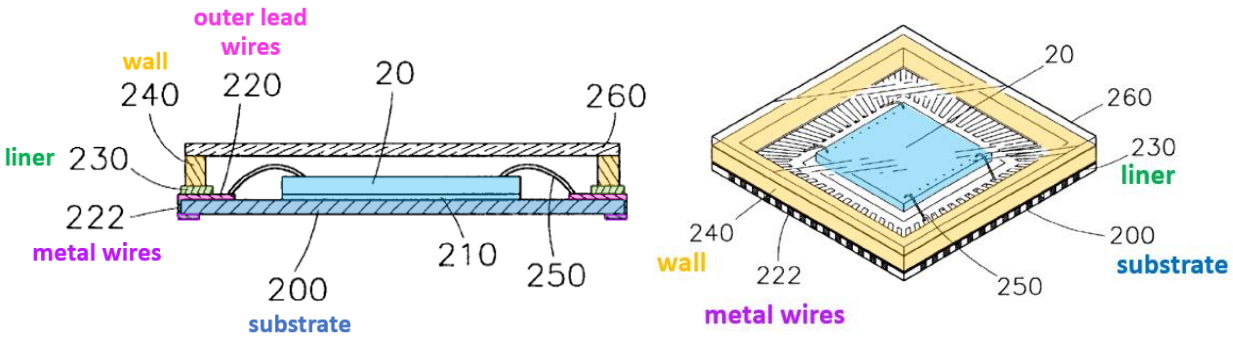

(Ex. 1005, FIG. 11.)

As illustrate above, leads (12b) of the lower lead frame (10b) correspond to the leads (12a) of the upper lead frame (10a). (Ex. 1005, ¶0040.) Because the two die pads (11a)(11b) and sets of leads (12a)(12b) have the different configurations, once the two lead frames (10a)(10b) are compressed together, multiple interstice (16) are

defined for receiving the isolating resin (13). The isolating resin (13) further fills the multiple interstice (16) and the gaps (14a)(14b) between the leads. (*Id.*)

### 2. Chou (Ex. 1006)

Like the '481 patent, Chou is directed to a semiconductor packaging structure, and discloses semiconductor package structures with a simple structural mold and a lower cost. (Ex. 1006, 1:5–49; *see also* Ex. 1002, ¶¶42–44.) Chou recognizes that because the outer lead wires formed on a substrate surface will create an irregular surface, it was therefore desirable to make a flat seat for placing a framing wall. (Ex. 1006, 2:42–47.) To form a flat seat and increase adhesion to the wall, Chou discloses an insulating liner coats the periphery of the substrate. (*Id.*)




(Ex. 1006, FIGs. 4 and 6.)

### 3. Chen (Ex. 1007)

Like the '481 patent, Chen is also directed to an image sensor package, and in particular to an image sensor is capable of increasing reliability. (Ex. 1007, ¶0002; *see also* Ex. 1002, ¶¶45–47.) Chen describes a prior art image sensor package where each first electrode 15 of the substrate 10 is arranged in straight line, and a green

paint 35 is coated between the each first electrode 15. (Ex. 1007, ¶0006.) A frame layer 18 is mounted on the green paint 35. (*Id*.) Chen recognizes that there is a gap between the green paint 35 and first electrode 15, wet-air from the atmosphere will enter the internal of the product through the gap and the reliability of the product may be reduced. (*Id*.)

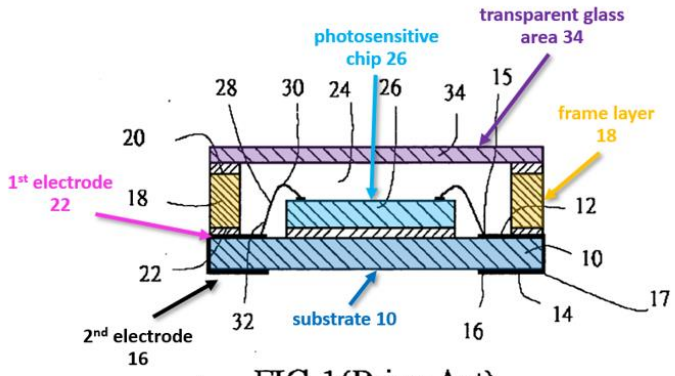



FIG.1(Prior Art)

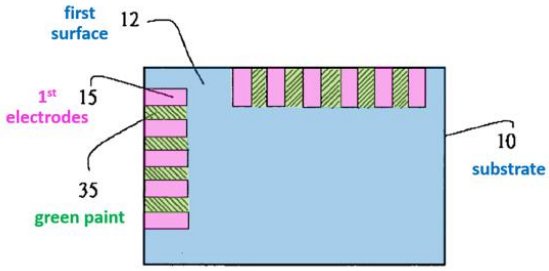



FIG.2(Prior Art)

(Ex. 1007, FIGs. 1 and 2.)

To address this problem, Chen proposes a curved first electrode arrangement with green paint coated between the first electrodes. (Ex. 1007, ¶0015.) According to Chen, this arrangement prevents wet air from entering the image sensor. (Ex. 1007, ¶0020.)

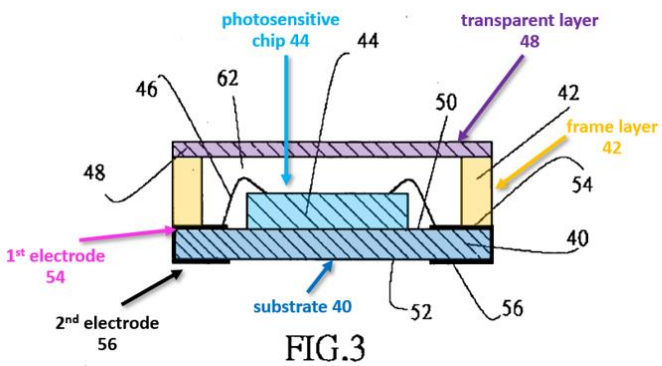



FIG.3

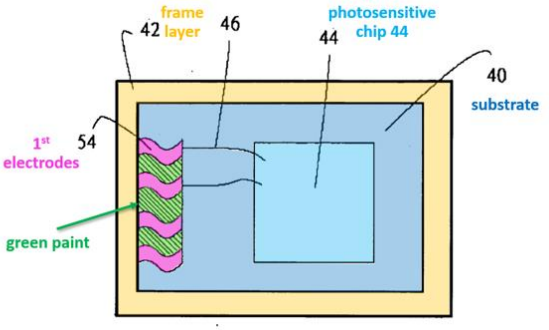



FIG.5

(Ex. 1007, FIGs. 3 and 5.)

## VIII. DETAILED GROUNDS OF UNPATENTABILITY

### A. Ground I – Claims 1–2 are anticipated by Hsu

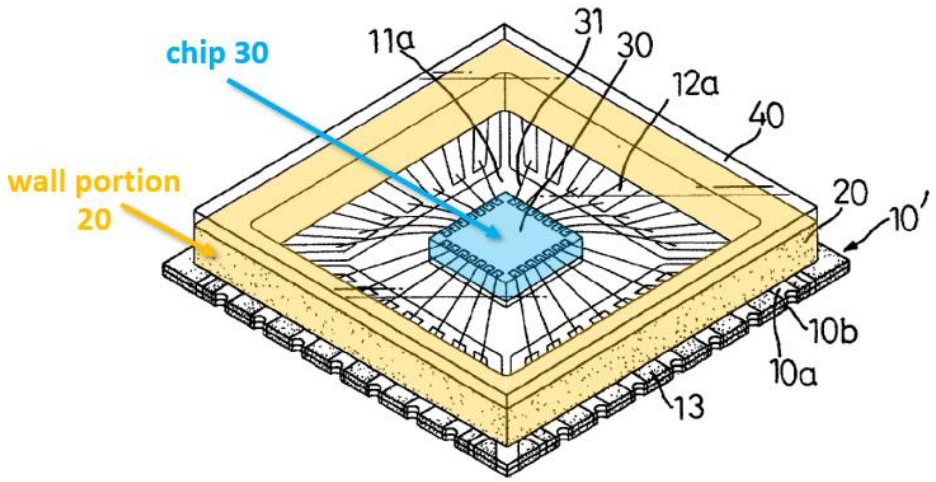
#### 1. Claim 1

Hsu discloses each and every limitation of claim 1 of the ’481 patent under pre-AIA 35 U.S.C. § 102(b) , as set forth in further detail below. (Ex. 1002, ¶¶33–41, 48–60.)

##### a. A substrate structure for an image sensor package, the substrate structure comprising:

As noted above, the district court ruled that the preamble is not limiting. Nevertheless, Hsu discloses a semiconductor substrate structure suitable for an optical sensing package 30. (*See, e.g.*, Ex. 1005, ¶¶0002 (“The present invention relates to a semiconductor packaging structure….”), 0028, 0033 (“Both the transparent cover 40 and the transparent resin are suitable for the optical sensing semiconductor packaging structure.”), 0037–0041, FIG. 7 (reproduced below); Ex. 1002, ¶¶49–50.) Further, Hsu discloses that a conventional semiconductor packaging structure for sensing optical signals may be a charge coupled device (CCD) (*i.e.*, an image sensor). This packaging structure has a substrate defined with a groove in the middle portion of the substrate, wherein a chip is mounted on the substrate. (Ex. 1005, ¶0004.) In light of this disclosure and the structural similarity to well-known components common to image sensor packages (*e.g.*, a chip, a die pad, a wall portion, electrical leads connected by gold wires to the chip, *etc*.), a

POSA would have understood Hsu's substrate structure to be suitable for an image sensor. (Ex. 1002, ¶¶49–50.)[3]



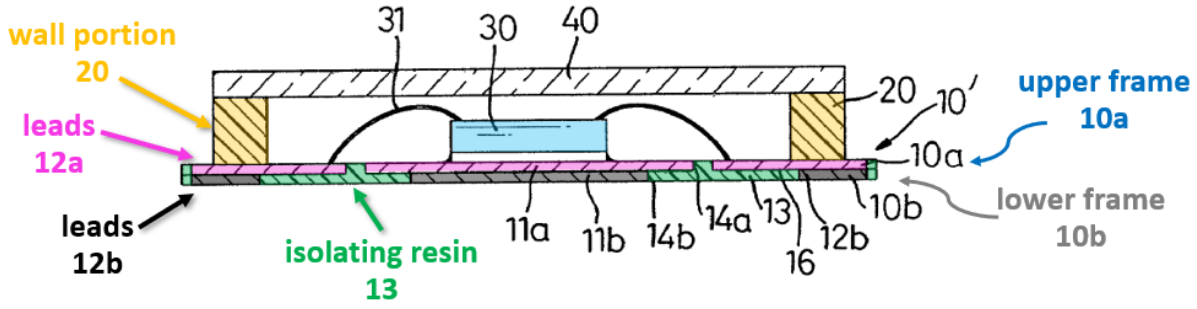

(Ex. 1005, FIG. 7.)

**b. a bottom base having an upper surface formed with a plurality of first electrodes, and a lower surface formed with a plurality of second electrodes,**

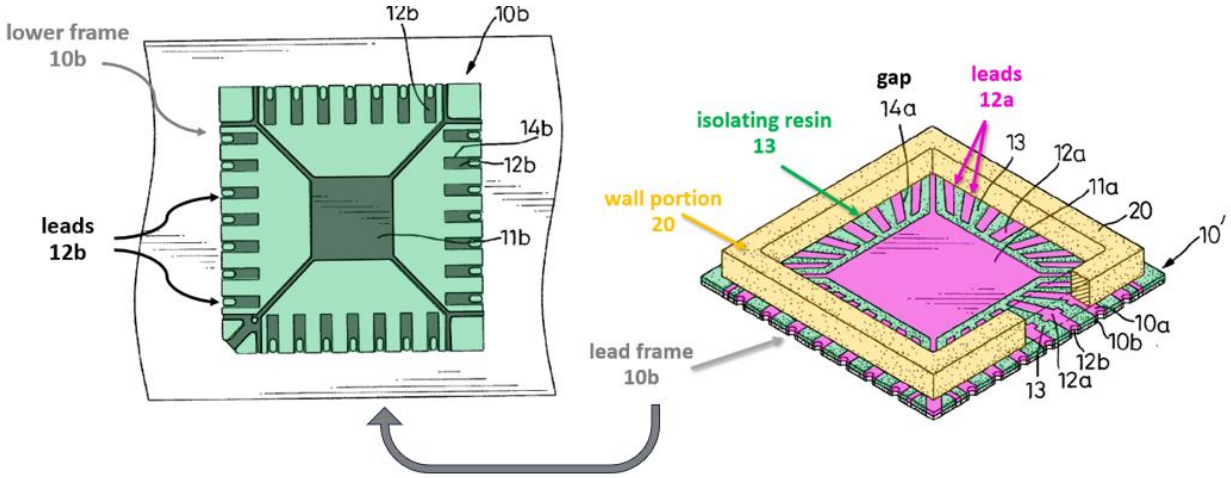
Hsu discloses this limitation. ((Ex. 1002, ¶¶33–41, 51–52.) For instance, Hsu discloses a lower frame 10b (*i.e.*, a bottom base) having an upper surface formed with a plurality of leads 12a (*i.e.*, first electrodes), and a lower surface formed with

[3] Although the analysis here is primarily directed to Hsu's fifth embodiment (FIGs. 7–12), it should be noted that Hsu's description of the fifth embodiment pertains to lead frame 10′ as an alternative to lead frame 10 and thus does not repeat its description of other common components (such as wall portion 20). (Ex. 1005, ¶0037.)

a plurality of leads 12b (*i.e.*, second electrodes). (Ex. 1005, ¶¶0037–0041, FIGs. 7–11.)




(Ex. 1005, FIG. 11.)



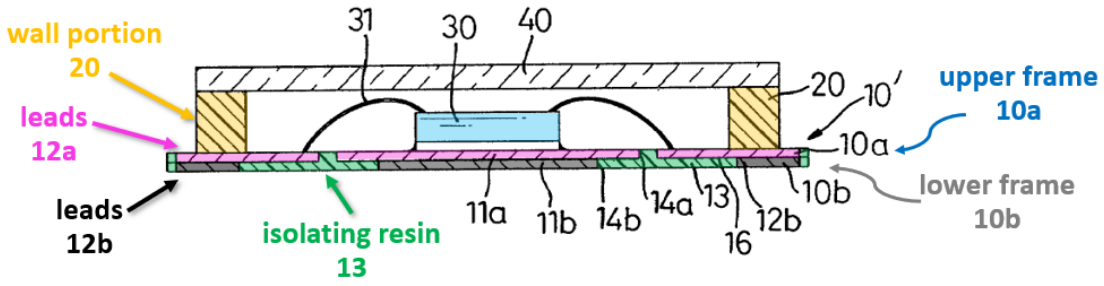

(Ex. 1005, FIGs. 8 and 10.)

Specifically, Hsu discloses lower frame 10b (*i.e.*, a bottom base) has an upper surface adjoining upper frame 10a as shown in Figures 8 and 11. In particular, "the upper lead frame 10a and the lower lead frame 10b are in alignment with each other and compressed together to form the metal frame 10′, and the leads 12b of the lower lead frame 10b are corresponded to the leads 12a of the upper lead frame 10a." (Ex. 1005, ¶0040.) Hence, the plurality of leads 12a are formed on the upper surface of

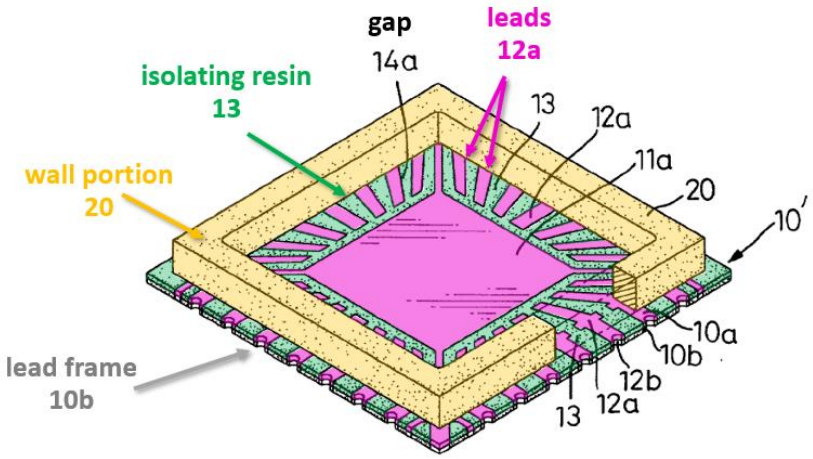
lower lead frame 10b, and the plurality of leads 12b forms at least a part of a lower surface of lower lead frame 10b. (Ex. 1005, ¶¶0037–0041, FIGs. 7–11; Ex. 1002, ¶¶33–41, 51–52.)

**c. wherein an insulation layer is coated between first electrodes and in direct surface contact with the upper surface of the bottom base;**

Hsu discloses this limitation. (Ex. 1002, ¶¶33–41, 53–56.) For instance, Hsu discloses isolating resin layer 13 (*i.e.*, an insulation layer) is coated between leads 12a (*i.e.*, first electrodes) and arranged on (*i.e.*, in direct surface contact with) the upper surface of the bottom base, as shown in Figures 8 and 11 (below). (Ex. 1005, ¶¶0037–0038, 0039 ("An interval is defined between the die pad (11a)(11b) and the plurality of leads (12a)(12b) for filling with the isolating resin (13). Multiple gaps (14a)(14b) are each defined by two adjacent leads (12a)(12b), wherein the multiple gaps (14a)(14b) are communicated with each other."), 0040 ("Since the two die pads (11a)(11b) and the leads (12a)(12b) of the upper lead frame (10a) and the lower lead frame (10b) have the different size, once the two lead frames (10a)(10b) are compressed together, multiple interstice (16) are defined for receiving the isolating resin (13). The isolating resin (13) further fills the multiple interstice (16) and the gaps (14a)(14b) by molding compound."), FIGs. 7–11.) Hence, resin 13 fills the space between upper leads 12a and coats at least their sides and fills the space above and directly adjoining the lower frame 10b.




(Ex. 1005, FIG. 11.)




(Ex. 1005, FIG. 8.)

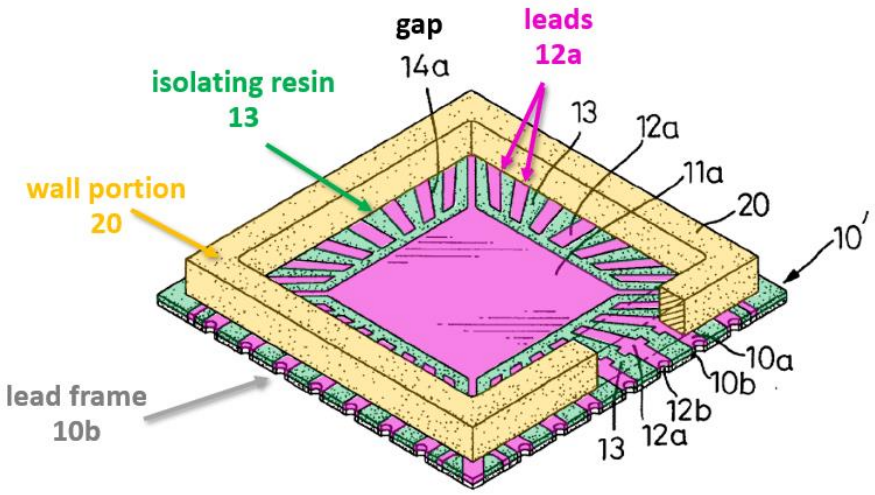
A POSA would have understood that isolating resin 13 is an electrically insulating layer which electrically isolates individual pairs of leads 12a and 12b from the other pairs of leads. (Ex. 1002, ¶¶¶33–41, 54.) A resin material is generally understood to be an electrically insulating material. (*Id.*) Moreover, its described function (*i.e.*, "isolating") and its arrangement in the gaps between the pairs of electrical leads 12a, 12b is indicative of an electrically isolating (*i.e.*, electrically insulating) material. (Ex. 1002, ¶55.) A POSA would have also understood that if isolating resin 13 were conductive, it would create an electrical short between the

leads and the substrate would not function as intended. (*Id.*; *see also* Ex. 1005, ¶0039 ("[E]ach of the plurality of leads 12b of the lower lead frame 10b only has an external portion corresponding to one of the external portions of the leads 12a"); ¶0046 ("Since the chip is directly connected to the leads of the lead frame and the leads are electrically and directly mounted on a circuit board, thus the signal conduction path is very short and the conducting delay is avoid[ed]."), Ex. 1004, 71 (applicant arguing that a POSA would never commonly and electrically connect a plurality of electrodes such that they short circuit).)

Hsu further discloses that "[a]n interval is defined between the die pad 11a, 11b and the plurality of leads 12a, 12b for filling with the isolating resin 13." Also, "[m]ultiple gaps 14a, 14b are each defined by two adjacent leads 12a, 12b." (Ex. 1005, ¶0039.) Thus, "multiple interstice 16 are defined for receiving the isolating resin 13." (Ex. 1005, ¶0040.) Hsu states that "[t]he isolating resin 13 further fills the multiple interstice 16 and the gaps 14a, 14b by molding compound." (Ex. 1005, ¶0040.) Hence, isolating resin 13 is coated between leads 12a in gaps 14a and in direct surface contact with the upper surface of the lower lead frame 10b, as shown in Figures 7–11. (Ex. 1002, ¶56.)

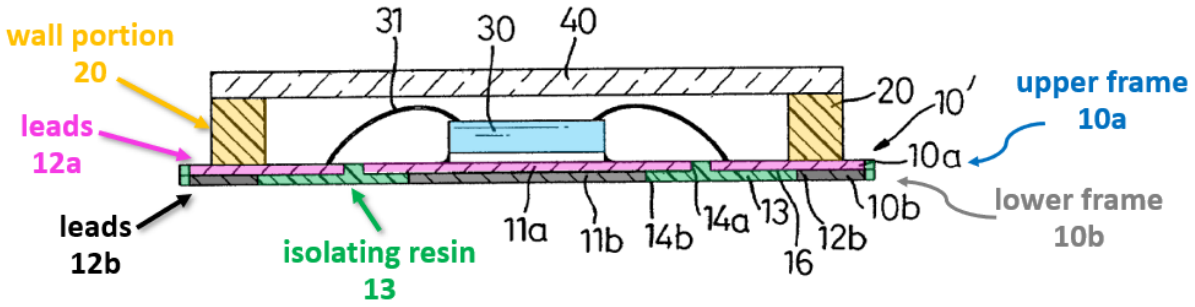
**d. a frame layer arranged on and in direct surface contact with the first electrodes and the insulation layer to form a cavity together with the bottom base,**

Hsu discloses this limitation. (Ex. 1002, ¶¶33–41, 57–59.) For instance, Hsu discloses wall portion 20 (*i.e.*, a frame layer) arranged on and (*i.e.*, in direct surface contact) with the leads 12a (*i.e.*, the first electrodes) and the isolating resin 13 (*i.e.*, the insulation layer). (*See, e.g.*, Ex. 1005, ¶¶0037–0041; FIGs. 7–11.) In particular, as illustrated below in Figure 8, wall portion 20 extends around the periphery of the lead frame (Ex. 1005, FIG. 8; *see also id.*, ¶0030 ("The wall portion 20 is formed by molding compound and is installed at [the] periphery of the lead frame 10.").) A transparent cover 40 can be arranged on the wall portion 20 to enclose a chip 30 inside the wall portion 20 and thus protect the chip 20 from the contaminant. (Ex. 1005, ¶¶0032, 0041, FIGs. 5–7, 11.) Thus, a POSA would have considered wall portion 20 be a "frame layer" as claimed.




(Ex. 1005, FIG. 8.)

As illustrated in Figure 8 (above) and also Figure 11 (below), Hsu wall portion 20 (*i.e.*, a frame layer) and the isolating resin 13 can be formed integrally on the lead frame 10 by molding compound, or the wall portion 20 is formed on the lead frame 10 after the isolating resin 13 is put in the gaps 14. Thus, Hsu discloses wall portion 20 (*i.e.*, a frame layer) on the lead frame is in direct surface contact with the leads 12a (*i.e.*, the first electrodes) and the isolating resin 13 (*i.e.*, the insulation layer). (Ex. 1005, ¶0030; Ex. 1002, ¶58.)

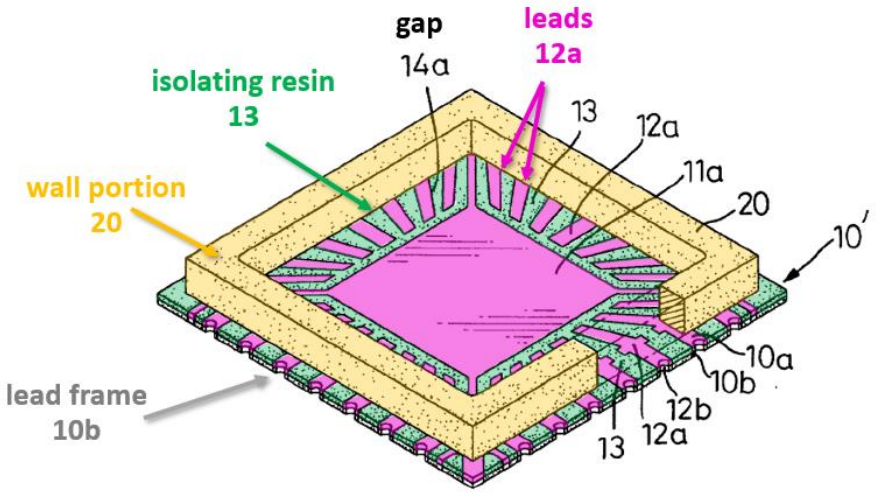



(Ex. 1005, FIG. 11.)

Further, Hsu discloses that the wall portion 20 (*i.e.*, frame layer), leads 12a (*i.e.*, first electrodes), and isolating resin 13 (*i.e.*, insulating layer) form a cavity to enclose the chip 30 (*i.e.*, a cavity) together with the lead frame 10b (*i.e.*, bottom base), as illustrated above in Figure 11. Hsu further discloses a transparent cover 40 can be arranged on the wall portion 20 to enclose a chip 30 inside the wall portion 20 and thus protect the chip 20 from the contaminant. (*See* Ex. 1005, ¶0032, FIGs. 1, 3; Ex. 1002, ¶59.)

**e. wherein the insulation layer is interposed between the bottom base and the frame layer**

Hsu discloses this limitation. (Ex. 1002, ¶¶33–41, 60.) For instance, Hsu discloses isolating resin 13 (*i.e.*, the insulation layer) is interposed between the lead frame 10b (*i.e.*, the bottom base) and wall portion 20 (*i.e.*, the frame layer). (*See, e.g.*, Ex. 1005, ¶¶0037–0041, FIGs. 7–11.) In particular, as illustrated in Figure 8 below, at the outer periphery, the wall portion 20 is arranged over top of the isolating resin 13 and isolating resin 13 is above lower frame 10b. At least in this sense, isolating resin 13 is arranged between the lead frame 10b and wall portion 20. (Ex. 1002, ¶60.)




(Ex. 1005, FIG. 8.)

#### 2. Claim 2 – The substrate structure according to claim 1, wherein the first electrodes are electrically connected to the second electrodes, respectively

Hsu discloses this limitation. (Ex. 1002, ¶¶33–41, 61.) For instance, as noted above, Hsu discloses that "each of the plurality of leads 12b of the lower lead frame 10b only has an external portion corresponding to one of the external portions of the leads 12a." (Ex. 1005, ¶0039.) Hsu further discloses that "the upper lead frames 10a and the lower lead frame 10b are in alignment with each other and compressed together to form the metal frame 10′, and the leads 12 of the lower lead frame 10b are corresponded to the leads 12a of the upper lead frame 10a." (Ex. 1005, ¶0040.) Hence, this direct contact between the leads forms a direct physical connection. (Ex. 1002, ¶61.) A POSA would have therefore understood the upper leads 12a (*i.e.*, the first electrodes) are electrically connected to the lower leads 12b (*i.e.*, the second electrodes), respectively. (Ex. 1002, ¶61.)

### B. Ground II – Claims 1–3 are obvious over Chou and Hsu

#### 1. Claim 1

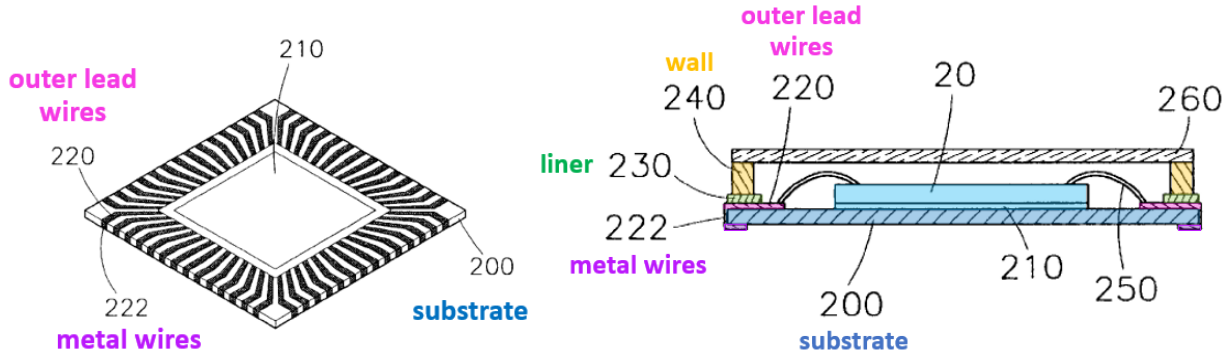
The combination of Chou and Hsu discloses and/or suggests every limitation of claim 1 of the '481 patent under pre-AIA 35 U.S.C. § 103(a), as set forth in further detail below. (Ex. 1002, ¶¶33–44, 62–73.)

**a. A substrate structure for an image sensor package, the substrate structure comprising:**

As noted above, the district court ruled that the preamble is not limiting. Nevertheless, Chou discloses substrate structure for an image sensor package. (*See*, *e.g.*, Ex. 1006, 2:21–29 ("[T]he semiconductor packaging structure serves to package [a] photoelectric element, for example a charge coupling device (CCD), and includes a substrate 200 made of such as epoxy resins (for example, BT, FR3x, FR4xx, R5xx, etc)) or ceramic materials."); Ex. 1002, ¶¶33–44, 62–73; *see also* Section VIII.A.1(a).)

**b. a bottom base having an upper surface formed with a plurality of first electrodes, and a lower surface formed with a plurality of second electrodes,**

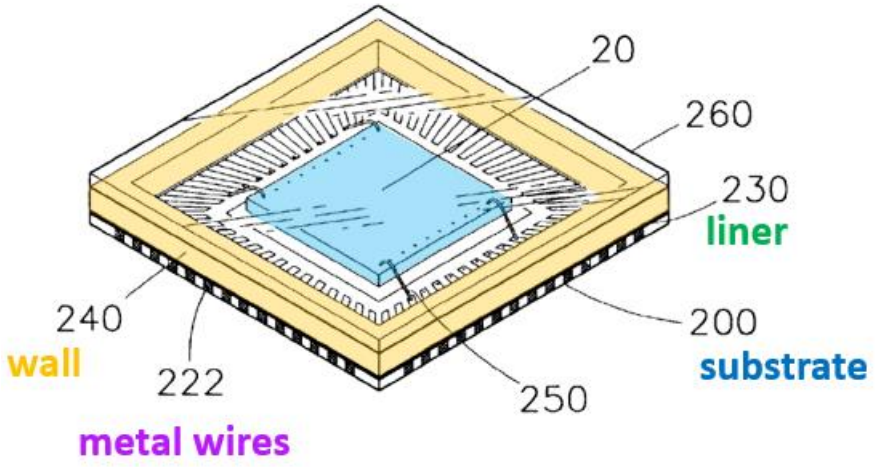
Chou discloses this limitation. (Ex. 1002, ¶¶42–44, 64.) For instance, Chou discloses substrate 200 (*i.e.*, a bottom base) having an upper surface formed with a plurality of outer lead wires 220 (*i.e.*, first electrodes), and a lower surface formed with a plurality of metal wires 222 (*i.e.*, second electrodes). (Ex. 1006, 2:30–37 ("With reference to FIG. 3, a perspective view of the substrate 200 and the related elements are illustrated. A chip seat 210 is installed on the substrate 200. A plurality of outer lead wires 220 and metal wires 222 are installed on the periphery of the chip seat 210. The metal wire 222 extends to pass through the lateral side of the Substrate 200 to the bottom of the substrate 200."), FIGs. 3–6; *see also* Section VIII.A.1(b).)




(Ex. 1006, FIGs. 3–4.)

**c. wherein an insulation layer is coated between first electrodes and in direct surface contact with the upper surface of the bottom base;**

Chou discloses this limitation. (Ex. 1002, ¶¶42–44, 65.) For instance, Chou discloses liner 230 (*i.e.*, an insulation layer) is coated between outer lead wires 220 (*i.e.*, first electrodes) and arranged on (*i.e.*, in direct surface contact with) the upper surface of the substrate 200 (*i.e.*, the bottom base), as illustrated in Figure 6 (below). (Ex. 1006, 2:31–67, FIGs. 3–6.) In particular, Chou discloses the "[s]ince the outer lead wires 220 will form with an undulated surface … a liner (for example, insulating plate) is firstly coated on the periphery of the substrate 200 of the wall 240 for forming a flat seat to install the wall 240 and increase adhesion." (Ex. 1006, 2:42–47; *see also id*., 1:50–61.) Hence, a POSA would have understood that the insulating liner fills in the gaps between the outer lead wires to form a smooth surface. (Ex. 1002, ¶¶42–44, 65; *see also* Section VIII.A.1(c).)



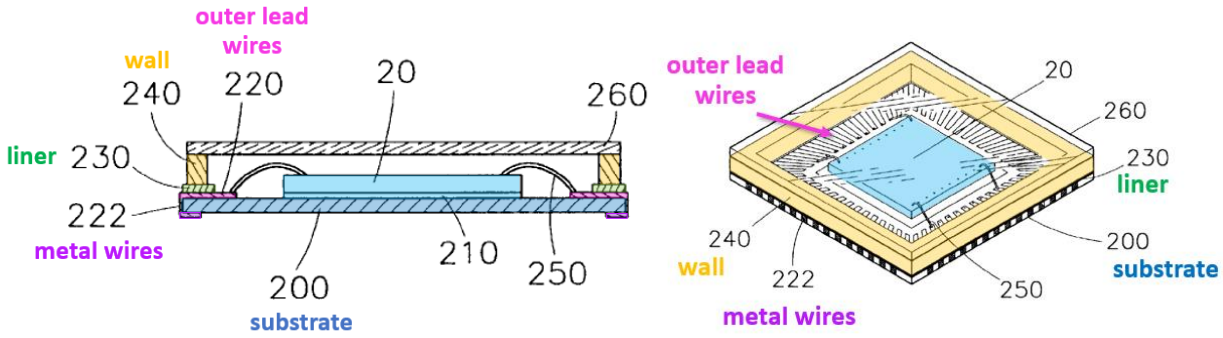

(Ex. 1006, FIG. 6.)

**d. a frame layer arranged on and in direct surface contact with the first electrodes and the insulation layer to form a cavity together with the bottom base,**

The combination of Chou and Hsu suggests this limitation. (Ex. 1002, ¶¶33–44, 66–71.) For instance, Chou discloses a wall 240 (*i.e.*, a frame layer) arranged on and (*i.e.*, in direct surface contact) with liner 230 (*i.e.*, the insulation layer). (*See, e.g.*, Ex. 1006, 2:31–67; FIGs. 3–6.) In particular, Chou discloses "a liner (for example, *insulating* plate) … *form[s] a flat seat to install the wall 240* and increase adhesion." (Ex. 1006, 2:42–47; *see also id*., 1:50–61.)

Further, as illustrated in Figures 4 and 6 (below), wall 240 (*i.e.*, frame layer), outer lead wires 220 (*i.e.*, first electrodes), and liner 230 (*i.e.*, insulating layer) form a cavity together with the substrate 200 (*i.e.*, bottom base) in which to place a semiconductor chip. (Ex. 1006, 2:22–52; FIGs 4, 6.) For example, Chou states that

"[a] wall portion 240 is installed on the substrate [200] for *forming a groove to receive a photoelectric element*." (Ex. 1006, 2:42–47; *see also id*., 1:50–61.)




(Ex. 1006, FIGs. 4, 6.)

Although Chou does not expressly disclose that wall 240 is in direct surface contact with outer lead wires 220, such a feature would have been an obvious alternative to Chou's substrate structure. As exemplified by Chou, there was a known desire to have a flat surface to which to mount a frame layer. (*See*, *e.g.*, Ex. 1006, 2:40–50, 3:6–8; Ex. 1002, ¶68.) Chou describes using a liner to coat the undulating surface of a substrate that is formed by individual lead wires and thereby form a flat surface for install the frame layer. (*See*, *e.g.*, Ex. 1006, 2:42–47.)

A POSA would have appreciated that an obvious way to form such a flat surface is to fill the gaps between the outer lead wires/electrodes with an insulating material. (Ex. 1002, ¶69.) Several examples of such an arrangement exist in the prior art, including the teachings of Hsu discussed above. (Ex. 1002, ¶69; *see also* Section VIII.A.1(c)–VIII.A.1(d) (discussing how Hsu discloses an isolating resin that fills the gaps between electrode leads and thereby forms a flat surface for a wall

portion that acts as a frame layer); Ex. 1007, ¶¶0024–0028, FIGs. 1–3 (having an insulating film 8a flush with internal electrodes 6a); Ex. 1008, 2:3–4:12, FIGs. 1A–1C, 3 (describing an insulating sealant 12 that fills the area between electrical leads 4, 5 properly to seal the perimeter of the image sensor substrate and forms a flat surface for a lid 11).)

Further, a POSA would have appreciated that although Chou illustrates in Figure 4 that the liner 230 extends above outer lead wires 220, such an arrangement is not necessary to form a flat surface for the wall 240, particular in light of these prior art teachings. (Ex. 1002, ¶70.) Furthermore, filling only the gaps between outer lead wires would beneficially minimize the amount of material needed to form a smooth surface for the wall in in Chou's package, thereby reducing material costs while still achieving Chou's aims. (Ex. 1002, ¶70.)

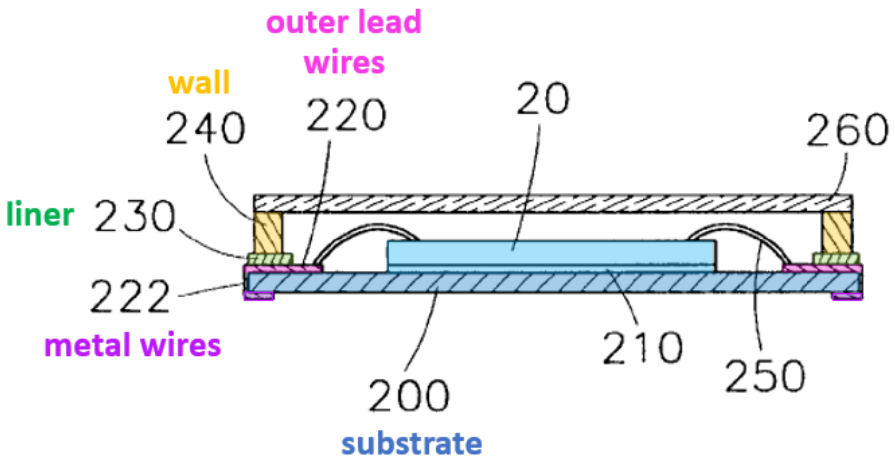
Notably, the original patent application that led to the '481 patent placed no criticality on direct surface contact between the frame layer and first electrodes. (Ex. 1004, 5–11.) In fact, direct surface was never mentioned in original written description. (Ex. 1004, 5–11, 30–36.) The direct-surface-contact language recited in the '481 patent claims and in the '481 patent was added during prosecution. (*Id*.)

In light of the above, it would have been obvious to a POSA to modify Chou's package to include an insulating liner between the outer lead wires (*e.g.*, similar to the arrangement disclosed by Hsu and others and thereby ensure that the bottom

surface of the wall 240 is in direct surface contact with the outer lead wires 220 and the insulating liner 230. (*See* Ex. 1005, FIGs 1–3; Ex. 1002, ¶71.) Such a modification to Chou would have been a predictable combination of known components according to known methods (*e.g.*, applying the teachings of Hsu regarding using filling the gaps between electrical leads to Chou's semiconductor package), and would have been produced the predictable result of forming a flat surface for install a wall. (*Id*.) *See also KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 ("KSR") ("The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.").

**e. wherein the insulation layer is interposed between the bottom base and the frame layer**

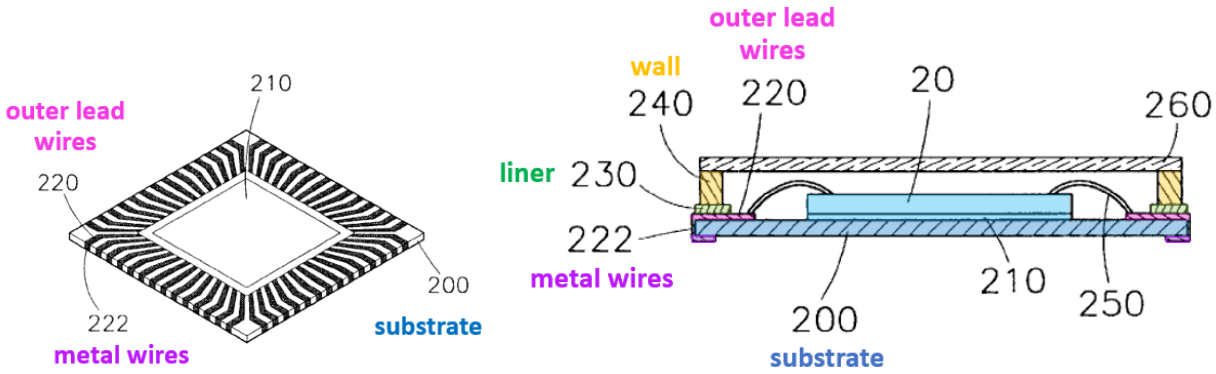
Chou discloses this limitation. (Ex. 1002, ¶¶42–44, 72.) For instance, Chou discloses liner 230 (*i.e.*, the insulation layer) is interposed between substrate 200 (*i.e.*, the bottom base) and wall 240 (*i.e.*, the frame layer). (*See*, *e.g.*, Ex. 1006, 1:50–61, 2:28–47, FIGs. 4, 6.) In particular, Chou discloses that "a liner (for example, insulating plate) is firstly *coated on the periphery of the substrate 200* of the wall 240 for *forming a flat seat to install the wall 240* and increase adhesion." (Ex. 1006, 2:42–47; *see also id*., 1:50–61; *see also* Section VIII.A.1(e).)




(Ex. 1006, FIG. 4.)

**2. Claim 2 – The substrate structure according to claim 1, wherein the first electrodes are electrically connected to the second electrodes, respectively**

Chou discloses this limitation. (Ex. 1002, ¶¶42–44, 73.) For instance, Chou discloses outer lead wires 220 (*i.e.*, the first electrodes) are electrically connected to metal wires 222 (*i.e.*, the second electrodes), respectively. In particular, Chou discloses that "[b]onding wires are connected on the element for electrically connecting the packaging element with outer devices." (Ex. 1006, 1:57–59; *see also id.*, 1:32–34.) To this end, bonding wires 250 are physically connected to outer lead wires 220, which are in turn, physically connected to metal wires 222, respectively, as illustrated in Figures 3 and 4 (below). A POSA would have understood that such a physical respective connection between conductive wires also results in a respective electrical connection. (Ex. 1002, ¶73; *see also* Section VIII.A.2.)




(Ex. 1006, FIGs. 3, 4.)

### 3. Claim 3 – The substrate structure according to claim 1, wherein the insulation layer is composed of green paint

The combination of Chou and Hsu suggests this limitation. (Ex. 1002, ¶¶42–44.) For instance, Although Chou does not expressly disclose the insulation material is composed of green paint, a POSA would have found it obvious to choose a suitable material for the insulation layer and green paint was a well-known suitable material for forming an insulation layer.[4] (*See, e.g.*, Ex. 1011, 4:56–5:3 (describing "an insulating material such as that of the green paint"); Ex. 1012, abstract, ("Electrode trenches are etched, and an insulating layer is formed by using green paint in the electrode trenches to isolate different electrodes on the same surface of the device"); Ex. 1013, ¶¶0007, 0032, 0042; Ex. 1002, ¶¶42–44.)

[4] The '481 patent does not describe the lens material as providing any criticality to the claimed invention. (*See generally* Ex. 1001.)

In light of the known suitable materials, a POSA would have been motivated to select an appropriate material for the liner, such as green paint, for filling the gaps between the outer lead electrodes and forming a flat surface for the wall. As the Supreme Court long ago stated, "reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put into the last opening in a jig-saw puzzle. It is not invention." *Sinclair Co. v. Interchemical Corp.*, 325 U.S. 327, 335 (1944). Furthermore, such a modification would have allowed liner/insulation layer to be formed with known materials using known technologies/techniques leading to a reasonable expectation of success. (Ex. 1011, 4:56–5:3; Ex. 1012, abstract; Ex. 1013, ¶¶0007, 0032, 0042; Ex. 1002, ¶¶42–44)

### C. Ground III – Claims 1–3 are anticipated by Chen

#### 1. Claim 1

Chen discloses each and every limitation of claim 1 of the '481 patent under pre-AIA 35 U.S.C. § 102(e), as set forth in further detail below. (Ex. 1002, ¶¶45–47, 74–81.)

##### a. A substrate structure for an image sensor package, the substrate structure comprising:

As noted above, the district court ruled that the preamble is not limiting. Nevertheless, Chen discloses a substrate structure for an image sensor package. (*See, e.g.*, Ex. 1007, ¶¶0007–0008, 0011–0013, 0014 ("Please refer to FIG. 3, FIG.

4, and FIG. 5, it is an image sensor package of the present invention includes a substrate 40, a frame layer 42, a photosensitive chip 44, wires 46, and a transparent layer 48."), 0015–0020, FIG. 3–5; Ex. 1002, ¶¶45–47, 74–81.)

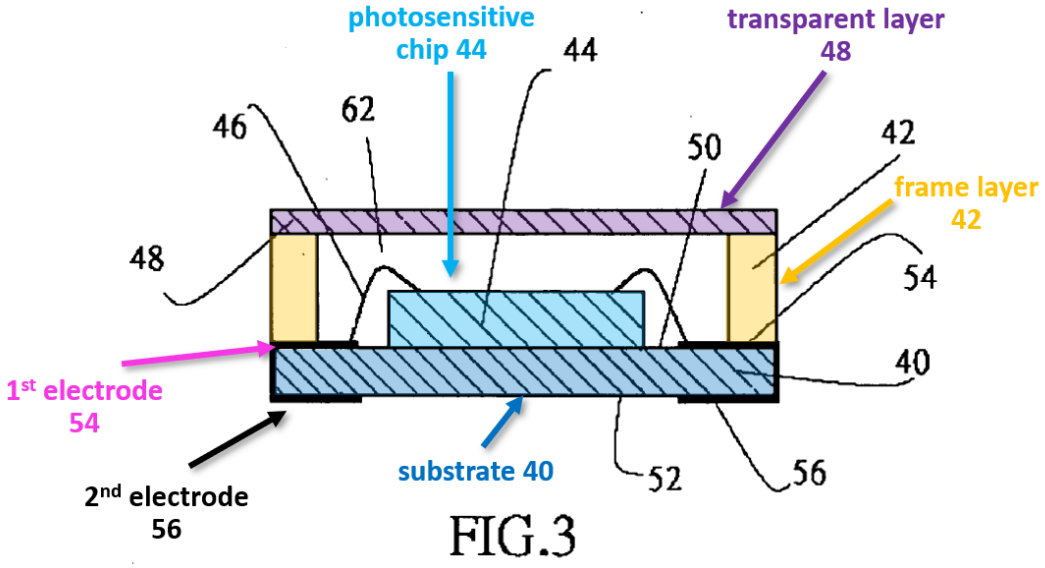


FIG.3

(Ex. 1007, FIG. 3 (a cross-sectional view of the image sensor package).)

**b. a bottom base having an upper surface formed with a plurality of first electrodes, and a lower surface formed with a plurality of second electrodes,**

Chen discloses this limitation. (Ex. 1002, ¶¶45–47, 76.) For instance, Chen discloses substrate 40 (*i.e.*, a bottom base) having an upper surface 50 formed with a plurality of first electrodes 54, and a lower surface 52 formed with a plurality of second electrodes 56. (*See*, *e.g.*, Ex. 1007, ¶¶0007–0008, 0011–0014, 0015 ("The substrate 40 has an upper surface 50 on which first electrodes 54 are formed, and a lower surface 52 on which second electrodes 56 are formed."), 0016–0020, FIG. 3–5; Ex. 1002, ¶¶45–47, 76.)

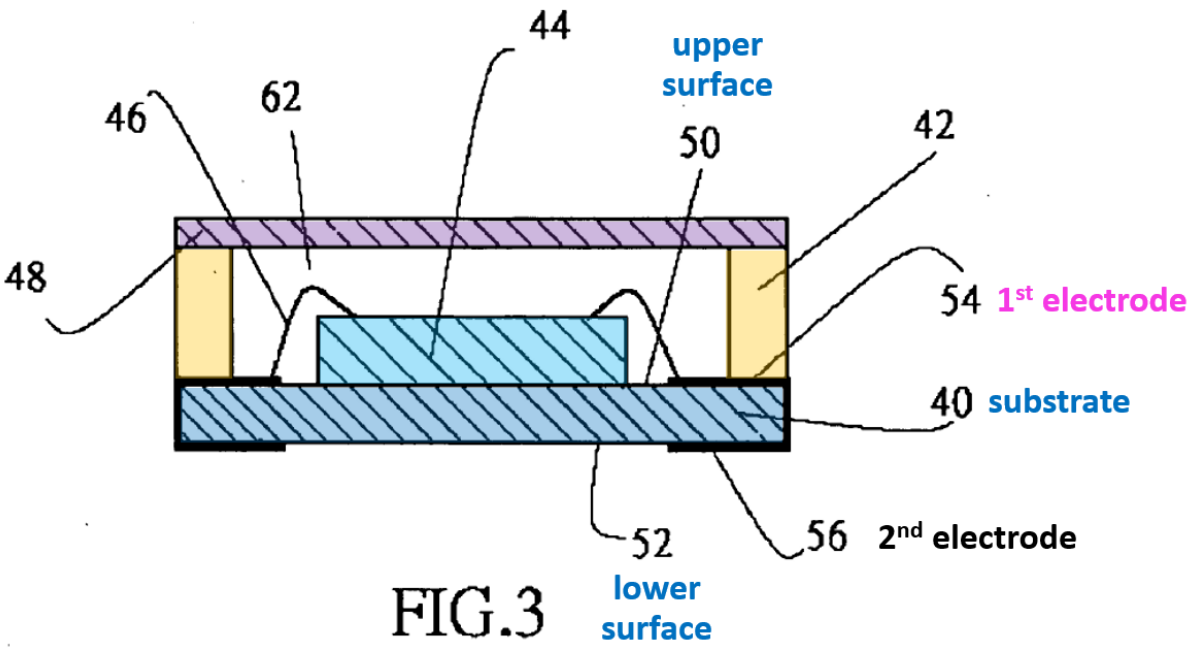



FIG.3

(Ex. 1007, FIG. 3.)

**c. wherein an insulation layer is coated between first electrodes and in direct surface contact with the upper surface of the bottom base;**

Chen discloses this limitation. (Ex. 1002, ¶¶45–47, 77–78.) For instance, Chen discloses green paint 58 (*i.e.*, an insulation layer) is coated between each first electrode 54 and arranged on (*i.e.*, in direct surface contact with) the upper surface 50 of the substrate 40 (*i.e.*, a bottom base), as shown in Figure 5 (below). (*See*, *e.g.*, Ex. 1007, ¶¶0007–0008, 0011–0014, 0015 ("A green-paint 58 is coated between the each first electrode 54 of the substrate 40."), 0016–0020, FIG. 3–5; Ex. 1002, ¶77.)

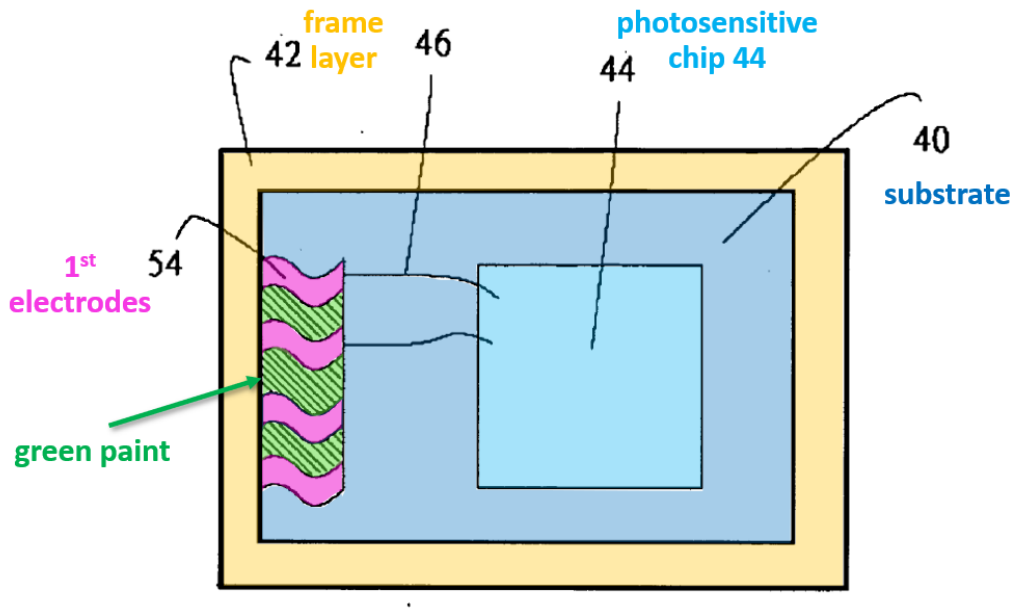



FIG.5

(Ex. 1007, FIG. 5 (a top-view showing the image sensor package).)

Specifically, a POSA would have understood that green paint 58 is an insulating layer which electrically insulates each first electrode 54. (Ex. 1002, ¶78.) A paint is generally understood to be a non-conductive material. (Ex. 1002, ¶78; *see also* Ex. 1011, 4:56–5:3; Ex. 1012, abstract; Ex. 1013, ¶¶0007, 0032, 0042.) Moreover, a POSA would have also understood that if green paint 58 were conductive, it would create an electrical short between the leads and the substrate would not function as intended. (Ex. 1002, ¶78; *see also* Ex. 1007, ¶0018 ("The plurality of wires 46 are electrically connected the photosensitive chip 44 to the first electrode 54 of the substrate 40."); Ex. 1004, 71 (applicant arguing that a POSA would never commonly and electrically connect a plurality of electrodes such that

they short circuit); Ex. 1001, 2:19–21 (listing "green paint" as an insulation layer.) Hence, a POSA would have understood the green paint 58 to be an insulating layer. (Ex. 1002, ¶78; Ex. 1011, 4:56–5:3; Ex. 1012, abstract; Ex. 1013, ¶¶0007, 0032, 0042.)

**d. a frame layer arranged on and in direct surface contact with the first electrodes and the insulation layer to form a cavity together with the bottom base,**

Chen discloses this limitation. (Ex. 1002, ¶¶45–47, 79–80.) For instance, in Figures 3 and 5, Chen illustrates a frame layer 42 arranged on and in direct surface contact with the first electrodes 54 and the green paint 58 (*i.e.*, the insulation layer) to form a cavity 62 together with the substrate 40 (*i.e.*, the bottom base). (*See*, *e.g.*, Ex. 1007, ¶¶0004–0020; FIGs. 1–5.) Chen's disclosure is consistent with the original disclosure of the application that led to the '481 patent. The originally filed disclosure was (*i.e.*, the claims and specification) to recite the requirements of limitation 1(d) and relied on "logic" and Figures 2–4 for alleged support. (*See*, *e.g.*, Ex. 1004, 31–35, 38.) For similar reasons, Chen's identical objective of preventing "wet air" (*i.e.*, moisture) from entering the image sensor package and nearly identical figures, must similarly provide sufficient disclosure of this feature.

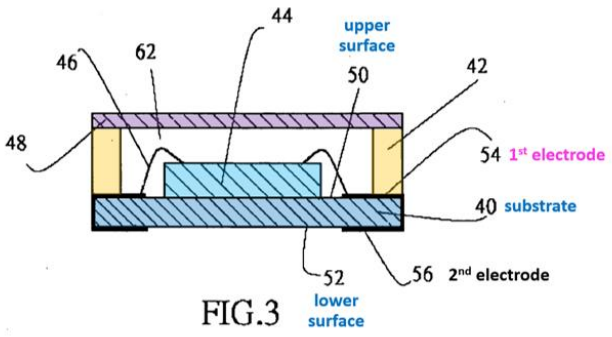



FIG.3

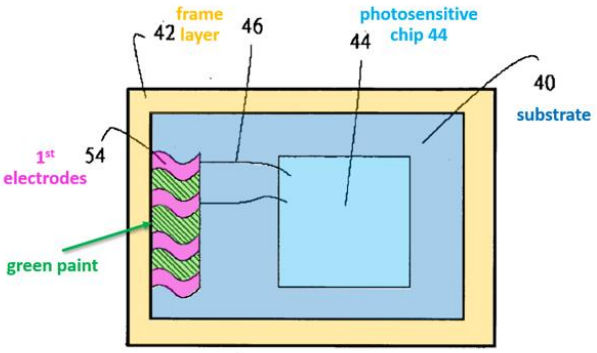



FIG.5

(Ex. 1007, FIGs. 3 and 5.)

Further, Chen discloses that green paint between curved electrodes does not allow air to enter the cavity containing the photosensitive chip, unlike the conventional image sensor package that includes green paint between the electrodes and allows wet air to enter the cavity. (Ex. 1007, ¶¶0006–0007, 0015, 0020.) A POSA would have understood from Chen's disclosure that the change in the shape of electrodes 54 would have allowed the green paint to fill the gap between electrodes and thereby seal hermetically seal the image sensor cavity 62. (Ex. 1002, ¶80) Understandably, if green paint 58 did not completely fill the volume between substrate 40, first electrodes 54, and the frame layer 42, air would be allowed to enter cavity 62 and Chen's curved electrode arrangement would not be any more reliable than the conventional image sensor arrangement. (*See* Ex. 1007, ¶0007 ("An object of the invention is to provide an image sensor package [that] can prevent the wet-air from the atmosphere air [from] inter[ing] the internal [cavity] of the product [so as to] enhance[] the reliability of the product."); Ex. 1002, ¶80.) Further, with the gap

between the electrodes filled, the green paint (*i.e.*, the insulating layer) would be in direct surface contact with the frame layer 42 which extends across the top of the gap between the electrodes. (Ex. 1007, FIGs. 3–5; *see also id*. ¶0006 ("Referring to FIG. 2, it is a top view of the substrate of the FIG. 1. The each electrode 15 of the substrate 10 is arranged in straight line, and a green paint 35 is coated between the each first electrode 15. The frame layer 18 is mounted on the green paint 35."); Ex. 1002, ¶80.)

**e. wherein the insulation layer is interposed between the bottom base and the frame layer**

Chen discloses this limitation. (Ex. 1002, ¶¶45–47, 81.) For instance, Chen discloses green paint 58 (*i.e.*, the insulation layer) is interposed between the substrate 40 (*i.e.*, the bottom base) and frame layer 42. (*See, e.g.*, Ex. 1007, ¶¶0008, 0014–0016, FIGs. 3–5.) In particular, as illustrated in Figure 3 (below), at the outer periphery of the package, the frame layer 42 is arranged over top of electrodes 54 and above substrate 40. Further, the green paint 58 is coated between the electrodes, as shown in Figures 4 and 5. Thus, the green paint is logically arranged between frame layer 42 and substrate 40. (Ex. 1002, ¶81; *see also* Ex. 1004, 68–70 (amending the claims to recite this feature and relying on original Figures 2–4).)

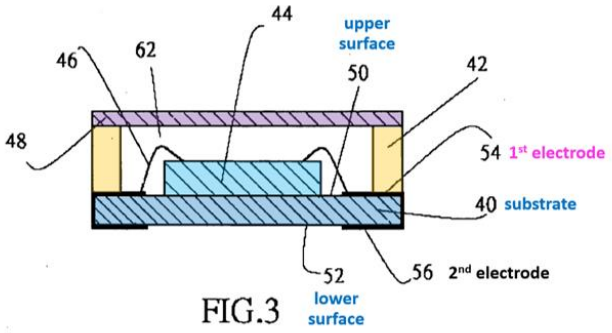



FIG.3

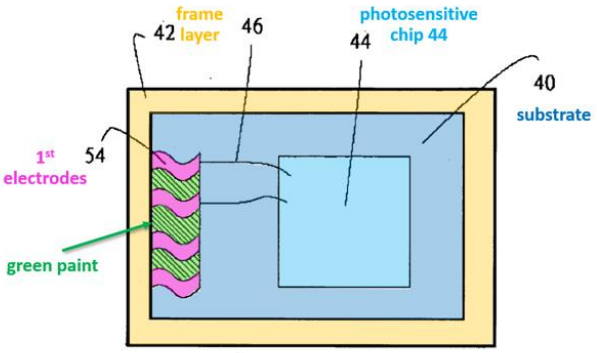



FIG.5

(Ex. 1007, FIGs. 3 and 5.)

**2. Claim 2 – The substrate structure according to claim 1, wherein the first electrodes are electrically connected to the second electrodes, respectively**

Chen discloses this limitation. (Ex. 1002, ¶¶45–47, 82.) For instance, Chen discloses that "[t]he first electrodes 54 are corresponding to electrically connect to the second electrode 56." (Ex. 1007, ¶0015.)

**3. Claim 3 – The substrate structure according to claim 1, wherein the insulation layer is composed of green paint**

Chen discloses this limitation. (Ex. 1002, ¶¶45–47, 83.) For instance, as noted above, Chen discloses that "[a] green-paint 58 is coated between the each first electrode 54 of the substrate 40." (Ex. 1007, ¶0015.)

## VII. SECONDARY CONSIDERATIONS

Patent Owner bears the burden of proof in establishing objective indicia of nonobviousness, but has not come forward with any such evidence. To the extent Patent Owner offers any purported evidence of nonobviousness in this proceeding,

consideration should be delayed until Petitioner has had an opportunity to respond to it.

## VIII. DISCRETIONARY FACTORS

As explained below, the six factors set out in *Fintiv* weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential).

The first factor (stay) is at best neutral because Petitioner has not yet moved to stay the parallel district court case and the PTAB does speculate on how the district court would rule should a stay be requested. *See, e.g., Hulu LLC v. SITO Mobile R&D IP, LLC*, IPR2021-00298, Paper 11 at 10-11 (P.T.A.B. May 19, 2021).

The second factor (proximity of trial dates) is also neutral. While jury selection is currently set for April 2025, "an early trial date" is "non-dispositive" and simply means that "the decision whether to institute will likely implicate other factors," which, as explained, favor institution. *Fintiv*, IPR2020-00019, Paper 11 at 5, 9; *see also Intuitive Surgical, Inc. v. Ethicon LLC*, IPR2018-01703, Paper 7 at 12 (P.T.A.B. Feb. 19, 2019) (recognizing that, even if a trial will come before a final decision, institution is appropriate to "give[] the district court the opportunity, at its discretion, to conserve judicial resources by staying the litigation until the review is complete," which helps "satisfy[] the AIA's objective"); *cf. Unilioc USA, Inc. v. RingCentral, Inc.*, No. 2-17-cv-00354-JRG (E.D. Tex. Feb. 12, 2018), at *1

(observing that staying the case pending IPR will "streamline the scope of th[e] case to an appreciable extent" regardless of the IPR outcome); *NetNut Ltd. v. Bright Data Ltd.*, IPR2021-01492, Paper 12 at 9–16 (P.T.A.B. Mar. 21, 2022) (granting institution even when the co-pending trial date was scheduled six months before the final written decision deadline).

The third factor (investment in parallel proceedings) weighs in favor of institution. The fact discovery is in its early states and the Parties' have only limited investment to date. No depositions have been taken. Fact discovery has not ended. Expert discovery is not yet open. The majority of work still remains ahead. (Ex. 1033.)

Petitioner's reasonable diligence in pursuing this petition prior to receiving the final infringement contentions weighs in favor of institution third *Fintiv* factor. *Facebook, Inc. v. USC IP P'ship, L.P.*, IPR2021-00033, Paper 13 at 13 (P.T.A.B. April 30, 2021) (finding it was reasonable for Petitioner to wait to file the Petition until shortly after receiving infringement contentions). Petitioner has not received infringement contentions for nearly all of the more than 70 accused products. Moreover, the most cost-intensive period in the case will occur after the Board's institution decision, including dispositive motions and trial. *See Precision Planting, LLC. v. Deere & Co.*, IPR2019-01044, Paper 17 at 14-15 (P.T.A.B. Dec. 2, 2019) (where the district court has not issued a claim construction ruling, fact discovery

and expert discovery are not closed, and dispositive motion briefing has not yet occurred, that weighs against finding that case is at "an advanced stage"); *Abbott Vascular, Inc. v. FlexStent, LLC*, IPR2019-00882, Paper 11 at 30 (P.T.A.B. Oct. 7, 2019) (same). Because the investment in the trial has been relatively small and Petitioner acted diligently, this factor favors institution. *See*, *e.g.*, *Hulu*, Paper 11 at 13.

The fourth factor (overlap) also weighs in favor of institution. Petitioner stipulates that it will not maintain the same grounds of invalidity or grounds based on the same prior art in the parallel WDTX case if the Board institutes review as requested. Thus, there will be no overlap. This alleviates any concerns about potentially conflicting outcomes. In the parallel WDTX case, Reolink Digital's preliminary invalidity contentions do not contain any ground presented in this petition nor rely on the references from either ground. Thus, there is currently no overlap between Reolink Digital's invalidity contentions in the parallel district court proceeding and the grounds presented here.

Regarding the fifth factor, the Board should give no weight to the fact that Petitioner and PO are the same parties as in district court. *See Weatherford U.S., L.P., v. Enventure Global Tech., Inc.*, Paper 16 at 11-13 (P.T.A.B. April 14, 2021).

And even if *Fintiv* factors 1–5 had favored a discretionary denial, the sixth factor (other circumstances) weighs in favor of institution, given the compelling

merits here. *Commscope Technologies LLC v. Dali Wireless, Inc.*, IPR2022-01242, Paper 23 (P.T.A.B. Feb. 27, 2023); *see also* Section VIII. There is also a significant public interest against "leaving bad patents enforceable," and institution will further that interest. *Thryv, Inc v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020); *see also OpenSky Indus., LLC v. VLSI Tech. LLC*, IPR2021-01064, Paper 108 at 4–6 (P.T.A.B. Oct. 17, 2022). To Petitioners knowledge, KTI does not manufacture any commercial products and have no market presence. And despite the high likelihood of unpatentability of the challenged claims as demonstrated here, KTI has asserted the '481 patent more than 17 times against diverse commercial entities and accused an equally diverse range of products of infringement. Virtually all of those suits have settled and allowed KTI to continue to assert the '481 patent undeterred. Regardless of the other factors, the circumstances here provide compelling motivation to institute review of patent claims of highly questionable validity.

## IX. CONCLUSION

For the foregoing reasons, Petitioner respectfully requests review and cancellation of claims 1–3 of the '481 patent.

Dated: July 3, 2024

Respectfully submitted,

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## CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing Petition for Inter Partes Review contains 7978 words, excluding those portions identified in 37 C.F.R. § 42.24(a), as counted by the word-processing software used to prepare this paper.

Dated: July 3, 2024

By: /Timothy C. Bickham/
Timothy C. Bickham, Lead Counsel
Reg. No. 41,618

## CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § §42.6(e) and 42.105(a), the undersigned certifies that on July 3, 2024, a copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,314,481, the associated power of attorney, and Exhibits 1001-1013, 1030-1033 were served by FedEx Priority Overnight on the correspondence address of record indicated in the Patent Office's public Patent Center system for U.S. Patent No. 8,314,481B2:

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Dated July 3, 2024

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