UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NXP USA, INC.

Petitioner

v.

BELL SEMICONDUCTOR, LLC

Patent Owner

Patent No. 7,345,245

PETITION FOR *INTER PARTES* REVIEW

OF U.S. PATENT NO. 7,345,245

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I. INTRODUCTION

NXP USA, Inc. ("Petitioner" or "NXP") requests *inter partes* review of claims 1-12 ("the challenged claims") of U.S. Patent No. 7,345,245 ("the '245 patent") (Ex. 1001), which, according to PTO records, is assigned to Bell Semiconductor LLC ("Patent Owner" or "PO"). For the reasons discussed below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. §42.8

Real Parties-in-Interest

Petitioner identifies the following as the real parties-in-interest: NXP USA, Inc. ("Petitioner"), NXP Semiconductors N.V., NXP B.V., and Freescale Semiconductor Holdings V, Inc.

Related Matters

The '245 patent is at issue in *Bell Semiconductor, LLC v. NXP USA, Inc. et al* Case No. 8:22-cv-02133-HDV-ADS, pending in Federal District Court in the Central District of California.

Counsel and Service Information

Lead counsel is Bruce Garlick (Reg. No. 36,520), and Backup counsel are (1) Timothy Taylor (Reg. No. 76,643), (2) Patricia Healy (Reg. No. 73,072) and (3) Timothy Markison (Reg. No. 33,534). Service information is Garlick & Markison, 2025 Guadalupe Street, Suite 260, Austin, TX 78705, Tel.: 512-751-5682, Fax: 888-

456-7824, email: GM-NXP-Bell-IPR@texaspatents.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

Fees under 37 C.F.R. § 42.15(a) will be paid at the time of filing. When necessary to further the proceeding or in the case of overages, the PTO is authorized to charge and deposit funds to and from Deposit Account No. 50-2126.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '245 patent is available for review, and Petitioner is not barred or estopped from requesting review on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

Claims 1-12 should be canceled as unpatentable based on the following grounds:

Ground 1: Claims 7-8 and 10-11 are obvious by Devnani et al. ("Devnani") (Ex. 1005) in view of Applicant's admitted prior art (AAPA) under pre-AIA 35 U.S.C. § 103(a).

Ground 2: Claim 9 is obvious by Devnani in view of AAPA, and further in view of Pillai (Ex. 1007) under pre-AIA 35 U.S.C. § 103(a).

Ground 3: Claim 12 is obvious by Devnani in view of AAPA, and further in view of US Pat. No. 6,172,305 to Tanahashi (Ex. 1009) under pre-AIA 35 U.S.C. § 103(a).

Ground 4: Claims 1-2 and 4-5 are obvious by Devnani in view of AAPA under pre-AIA 35 U.S.C. § 103(a).

Ground 5: Claim 3 is obvious by Devnani in view of AAPA, and further in view of Pillai under pre-AIA 35 U.S.C. § 103(a).

Ground 6: Claim 6 is obvious by Devnani in view of AAPA, and in further view of Tanahashi under pre-AIA 35 U.S.C. § 103(a).

Ground 7: Claims 1, 2 and 5 are obvious by US Patent Pub. 2003/0003705 to Chung, *et al.* ("Chung") (Ex. 1006) in view of *Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages*, April 2003 ("Celeron") (Ex. 1008) under pre-AIA 35 U.S.C. § 103(a).

Ground 8: Claim 3 is obvious by Chung in view of Celeron, and further in view of Pillai under pre-AIA 35 U.S.C. § 103(a).

Ground 9: Claim 4 is obvious by Chung in view of Celeron, and further in view of AAPA under pre-AIA 35 U.S.C. § 103(a).

Ground 10: Claim 6 is obvious by Chung in view of Celeron, and further in view of Tanahashi under pre-AIA 35 U.S.C. § 103(a).

Ground 11: Claims 1, 2 and 5 are obvious by Devnani in view of Celeron under pre-AIA 35 U.S.C. § 103(a).

Ground 12: Claim 6 is obvious by Devnani in view of Celeron, and further in view of Tanahashi under pre-AIA 35 U.S.C. § 103(a).

Ground 13: Claim 7 is obvious by Review of BGAs (Ex. 1018) in view of Devnani, and further in view of CRTA (Ex. 1016) under pre-AIA 35 U.S.C. § 103(a).

VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art ("POSITA") at the time of the alleged invention of the '245 patent would have had a bachelor's degree in a field relating to the semiconductor manufacturing process, such as materials science, physics, electrical engineering, and/or other related subjects, and at least two to three years of experience with fabrication of integrated circuits. (Ex. 1002, ¶0020)[1] More education can supplement practical experience and vice versa. (*Id.*)

VII. OVERVIEW OF THE '245 PATENT

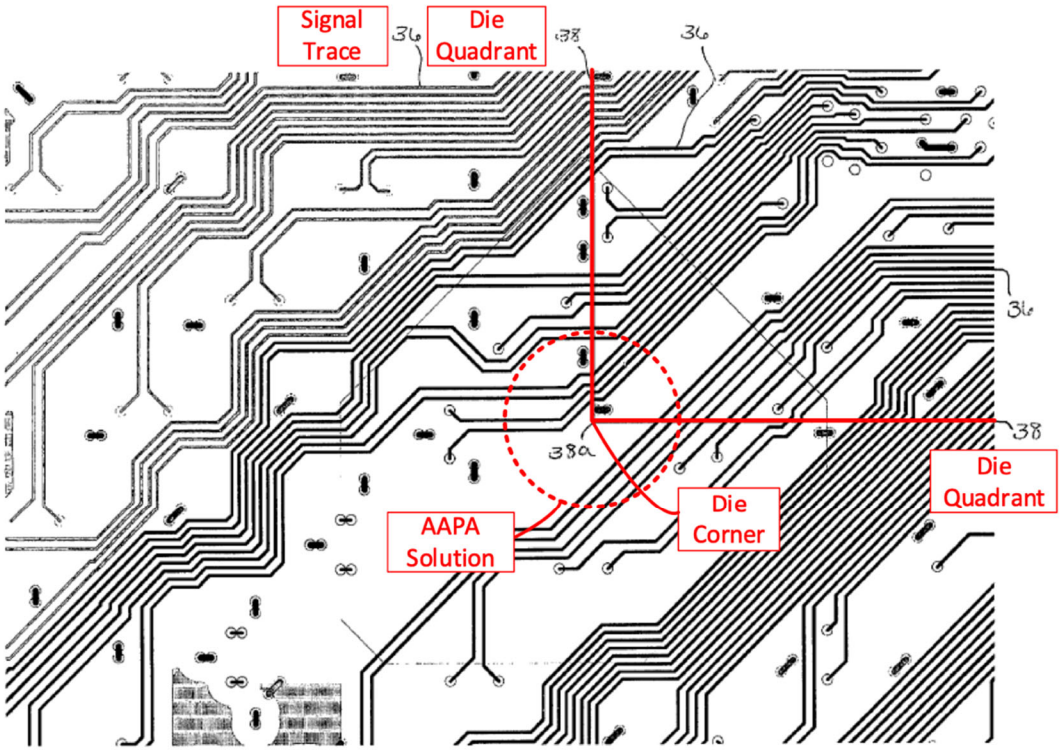
The '245 patent is entitled "Robust High Density Substrate Design For Thermal Cycling Reliability." (Ex. 1001, Title) The '245 patent discloses a semiconductor package upon which an IC die (die) mounts and which may be mounted upon a Printed Circuit Board (PCB). The '245 patent purports to improve

[1] Petitioner submits the declaration of Dr. Baker (Ex. 1002), an expert in the field of the '245 patent.

thermal cycling reliability for the semiconductor package by routing signal traces away from a high stress area, which is defined by a corner of an attached die. (*Id*., Abstract) (Ex. 1002, ¶0026) According to the '245 patent, the improvement is in the definition of the high stress area, which is different from prior art solutions that define the high stress area to be a "circular shaped area with a one (1) millimeter radius using placement of the die corner 38a as the center of the circle". (Ex. 1001, 2:6-15; 2:32-36)

The '245 patent discloses as prior art that "areas of high stress are associated with the die corner 38a and in particular the ball pads which are positioned under the area surrounding the die corner 38a. The edges of the ball pads 34, which are associated with the die corner 38a act as stress concentration points and under thermal cycling conditions, cracks are initiated from the edges of the ball pads 34 and extend into the dielectric layer above layer L9. If traces 36 are routed or other metal structures are provided on layer L8 over the ball pads 34 associated with the die corner 38a, the cracks can extend through the traces 36 and cause failures due to trace cracks under cycled stress conditions." (*Id.*, 1:51-2:2) (Ex. 1002, ¶0031)

Thus, it was well known as admitted by the Applicant's Admitted Prior Art (AAPA) that during thermal cycling, stress points of the die corner and the ball pads associated with the die corner caused cracks that would extend into other layers and would crack traces routed near the stress points. The AAPA solution of defining a circular stress zone is annotated onto the prior art Figure 3 of the '245 patent below, which shows layer 8 (L8) of a prior art substrate.



(Ex. 1001, Fig. 3 annotated)

To reiterate, the '245 patent states that the 1 mm radius circle (AAPA Solution) used to define the area of stress is not large enough. "A disadvantage of having a one (1) millimeter radius region under the die corner 38a is that it is not sufficient to avoid trace cracks in the layer L8 under thermal cycling conditions for all packaging

technolgies." (Ex. 1001, 2:11-15, [sic]) Thus, the '245 patent purports to solve this problem by defining a high stress zone 58 (red) for a smaller IC die and high stress zone 60 (blue) for a larger IC die. (*Id*., 3:17-26) (Ex. 1002, ¶0033)

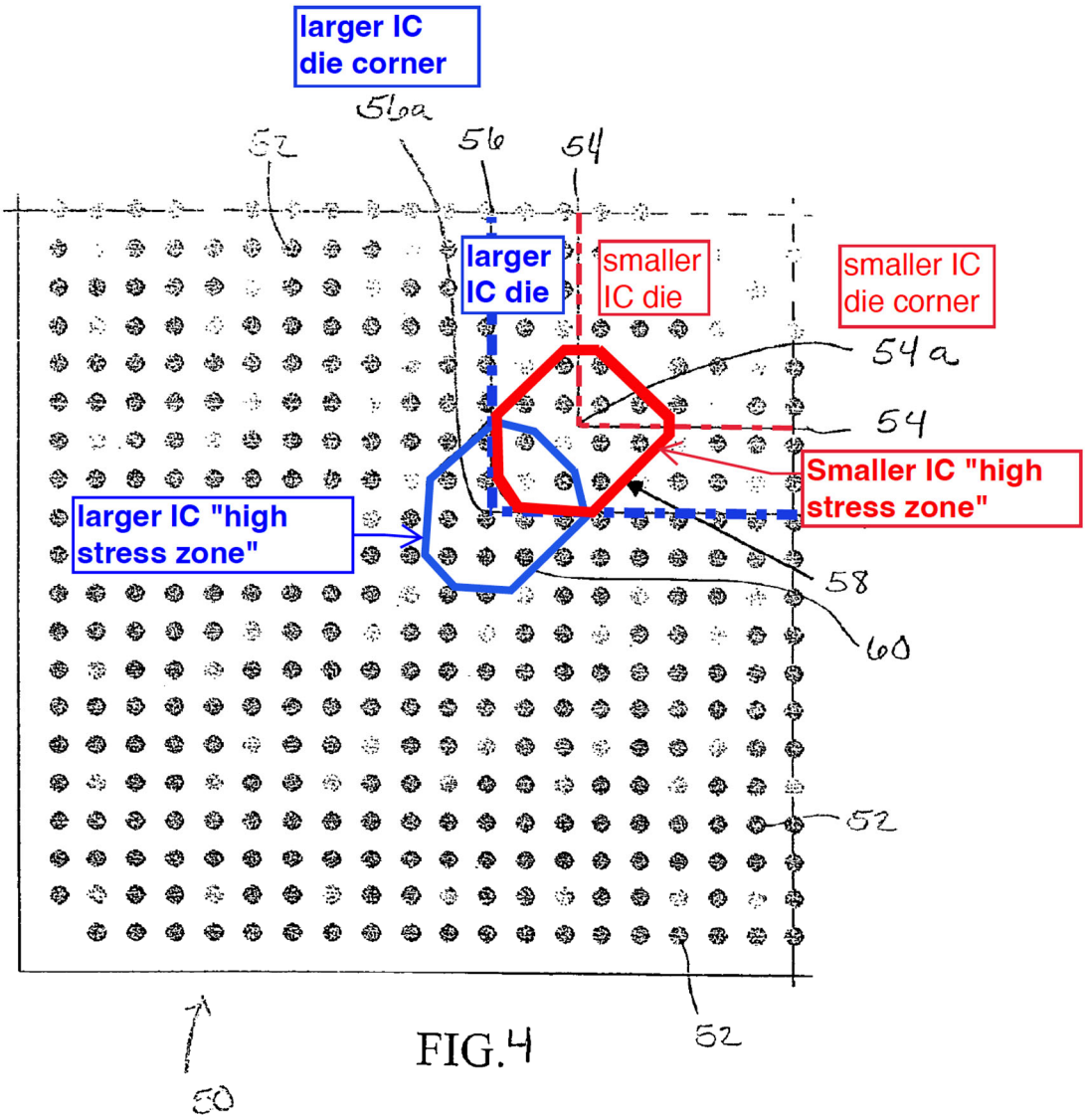


FIG.4

(Ex. 1001, Fig. 4 annotated)

More specifically, rather than defining the area of stress as the circular area having a 1 mm radius (of the AAPA Solution), the '245 patent defines the area of

stress as a high stress zone that is associated with the die corner that "extends approximately two ball pitches away from the die corner" in each direction. (*Id.*, 3:20-26) Notably, this "two ball pad pitch" distance is the same for each high stress zone 58, 60 shown above in Figure 4 and "each high stress zone 58, 60 is similarly shaped." (*Id*., 3:22-23) (Ex. 1002, ¶0035)

Further, the '245 patent does not disclose any specific reason, advantage, or unexpected result for a distance of "two ball pad pitches" or for the size or shape of the "high stress area" around the corner of a die. (Ex. 1002, ¶0037) Thus, the '245 patent is purporting an invention by merely changing the size and/or shape of a high stress area without any recitation of a new function, an unexpected result, or a significance of the high stress area's configuration not known in the art at the time of filing the '245 patent.

MPEP §§ 2144.04.IV.A states:

A. Changes in Size/Proportion

In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955) (Claims directed to a lumber package "of appreciable size and weight requiring handling by a lift truck" were held unpatentable over prior art lumber packages which could be lifted by hand because limitations relating to the size of the package were not sufficient to patentably distinguish over the prior art.); *In re Rinehart,* 531 F.2d 1048, 189 USPQ 143 (CCPA 1976) ("**mere scaling up** of a prior art process capable of being scaled

up, if such were the case, **would not establish patentability in a claim to an old process so scaled**." 531 F.2d at 1053, 189 USPQ at 148.).

In *Gardnerv.TEC Syst., Inc.,* 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), *cert. denied,* 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device **was not patentably distinct** from the prior art device. [emphasis added]

MPEP §§ 2144.04.IV.B states:

B. Changes in Shape

In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966) (The court held that the configuration of the claimed disposable plastic nursing container was a matter of choice which a person of ordinary skill in the art would have found obvious **absent persuasive evidence that the particular configuration of the claimed container was significant**.). [emphasis added]

However, as explained below (*infra* Section IX), the above purported features of a high stress area were either all known in the prior art or are obvious variants thereof. (Ex. 1002, ¶0038)

VIII. CLAIM CONSTRUCTION

For IPR proceedings, the Board applies the claim construction standard according to Phillips v. AWH Corp., 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 83 Fed. Reg. 51,340-59 (Oct. 11, 2018). Under *Phillips*, claim terms are typically given their ordinary and customary meanings, as would have been understood by a POSITA at the time of the invention. *Phillips*, 415 F.3d at 1313; *see also Id.*, 1312-16. The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). Petitioner believes that no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims. (Ex. 1002, ¶0039)

IX. DETAILED EXPLANATION OF UNPATENTABILITY

A. Qualification of cited references as prior art

Earliest effective filing date of the '245 patent

The '245 patent issued March 18, 2008, from U.S. App. No. 10/681,554 ("the '554 application"), was filed October 8, 2003. The earliest effective filing date for the '245 patent is October 8, 2003[2].

US Patent Pub. 2003/0183919 to Devnani *et al.* ("Devnani")

Devnani (Ex. 1005) was filed April 2, 2002, and published on October 2, 2003. Because both the filing and publication dates of Devnani are prior to the earliest effective filing date of the '245 patent, namely October 8, 2003, Devnani qualifies as prior art to the '245 patent under at least pre-AIA 35 U.S.C. §§ 102(a) and 102(e).

US Patent Pub. 2003/0003705 to Chung, *et al.* ("Chung")

Chung (Ex. 1006) was filed July 2, 2001, and published on January 2, 2003. Because both the filing and publication dates of Chung are prior to the earliest effective filing date of the '245 patent, namely October 8, 2003, Chung qualifies as prior art to the '245 patent under at least pre-AIA 35 U.S.C. §§ 102(a) and 102(e).

US Patent No. 6,680,530 to Pillai *et al.*, ("Pillai")

Pillai (Ex. 1007) was filed August 12, 2002, and issued on January 20, 2004. Because the filing date of Pillai is prior to the earliest effective filing date of the '245 patent, namely October 8, 2003, Pillai qualifies as prior art to the '245 patent under at least pre-AIA 35 U.S.C. §102(e).

[2] Because the '245 patent has an earliest-effective filing date of October 8, 2003, it is not subject to the provisions of the Leahy-Smith America Invents Act (AIA).

Mobile Intel® Celeron® Processor (0.13 µ) in Micro-FCBGA and Micro-FCPGA Packages Datasheet ("Celeron")

Celeron (Ex. 1008) was published in April of 2003, which is prior to the earliest effective filing date of the '245 patent. Celeron, therefore, qualifies as prior art to the '245 patent under at least pre-AIA 35 U.S.C. §§ 102(a).

US Patent No. 6,172,305 to Tanahashi ("Tanahashi")

Tanahashi (Ex. 1009) was filed July 29, 1998, and issued on January 9, 2001. Because Tanahashi issued more than 1 year before the earliest effective filing date of the '245 patent, namely October 8, 2003, Tanahashi qualifies as prior art to the '245 patent under pre-AIA 35 U.S.C. §102(b).

Thomas D. Moore and John L. Jarvis, The effects of in-plane orthotropic properties in a multi-chip ball grid array assembly, Microelectronics Reliability, Volume 42, Issue 6, June 2002, pages 943-949 ("Moore & Jarvis")

Thomas & Moore (Ex. 1009) was published in June of 2002, which is prior to the earliest effective filing date of the '245 patent. Thomas & Moore, therefore, qualifies as prior art to the '245 patent under at least pre-AIA 35 U.S.C. §§ 102(b).

D.J. Xie and Z.P. Wang, Process capability study and thermal fatigue life prediction of ceramic BGA solder joints, Finite Elements in Analysis and Design, Volume 30, Issues 1-2, July 15, 1998, pages 31-45 ("Xie and Wang")

Xie and Wang (Ex. 1011) was published" in July of 1998, which is prior to the earliest effective filing date of the '245 patent. Xie and Wang, therefore, qualifies as prior art to the '245 patent under at least pre-AIA 35 U.S.C. §§ 102(b).

Critical Review and Technology Assessments '91-'92, Reliability Analysis Center, AD-A278 419; April 21, 1994, 452 pages ("CRTA")

CRTA (Ex. 1016) was published in April of 1994, which is prior to the earliest effective filing date of the '245 patent. CRTA, therefore, qualifies as prior art to the '245 patent under at least pre-AIA 35 U.S.C. §§ 102(b).

2000 Packaging Handbook, Chapter 4: Performance Characteristics of IC Packages; pages 1-66, 2000 ("PCIP")

PCIP (Ex. 1017) was published in 2000, which is prior to the earliest effective filing date of the '245 patent. PCIP, therefore, qualifies as prior art to the '245 patent under at least pre-AIA 35 U.S.C. §§ 102(b).

A Review of Ball Grid Arrays For Electronic Assembly, S B Dunkerton and J M Goward, Presented at ICAWT '98, The 1998 International Conference on Advances in Welding Technology - 'Joining applications in electronics and medical devices', Columbus, Ohio, USA, 30 September - 2 October 1998 ("Review of BGAs")

Review of BGAs (Ex. 1018) was published in 1998, which is prior to the earliest effective filing date of the '245 patent. PCIP, therefore, qualifies as prior art to the '245 patent under at least pre-AIA 35 U.S.C. §§ 102(b).

Other than Pillai and Tanahashi, none of these references were cited during prosecution. (*See generally* Ex. 1004). Pillai was cited by the Examiner in allowing the claims during prosecution. However, as discussed below in Section X, inclusion of Pillai in Grounds 2 and 9 does not warrant discretionary denial because Petition presents Pillai in a new light in combination with each of Devnani, Chung and Celeron, which are references not previously considered by the Patent Office. Tanahashi was not cited as a primary reference during prosecution and is not cited as a primary reference herein.

Pillai was relied upon during the prosecution of the '245 patent (the '554 application). In a Final Office Action dated April 23, 2007, pending claims 14-16, 18, 20-22 and 24 were rejected under pre-AIA 35 U.S.C. § 102(e) as being anticipated by Pillai, claims 17 and 23 were rejected under 35 U.S.C. 103(a) as being

unpatentable over Pillai, and claims 19-25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Pillai in view of Tanahashi. (Ex 1004, pp. 271-274; then pending claims 14-25 correspond exactly to issued claims 1-12.)

In response to the Final Office action dated April 23, 2007, Applicant filed a Notice of Appeal and submitted, on July 23, 2007, Reasons for Review. In this filing, Applicant argued that the "independent claims specifically recite that the bottom routing layer has signal traces (plural) thereon, and that none of the signal traces (plural) of the bottom routing layer are located either: 1) over ball pads of the ball pad layer which are disposed in an area within two ball pads of the corner of the die (claim 14); or within the area of increased stress defined by the corner of the die (claim 20)."

Applicant went on to state that "[i]n contrast, Figure 1 of Pillai only shows the bottom routing layer having a single signal trace This is because Figure 1 of Pillai is simplified and only shows connection to one via/ball pad. Pillai does not disclose where the other signal traces on the bottom routing layer would be with regard to the other vias/ball pads, and fails to disclose that none of these other, non-shown, signal traces would be either: 1) over ball pads of the ball pad layer which are disposed in an area within two ball pads of the corner of the die (claim 14); or within the area of increased stress defined by the corner of the die (claim 20)." (Ex. 1004, pp. 263-266

[emphasis added]). In response to the Reasons for Review, the Examiner withdrew the 102(e) rejection to Pillai and allowed all claims.

The newly cited prior art references overcome the shortcomings of Pillai by showing multiple signal traces on the bottom routing layer routed outside of a high stress zone. During prosecution, AAPA of the ’245 patent was not cited in combination with Pillai or any other reference under an obviousness rejection. As will be described below, AAPA provides strong basis for a POSITA to arrive at the solution of independent claims 1 and 7 when used as a secondary reference. Had the Examiner considered the combination of Pillai and AAPA, the ’245 patent would likely not have issued. Thus, the ’245 patent is a bad patent. There is a significant public interest against “leaving bad patents enforceable,” and institution will further that interest. *Thryv, Inc v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020).

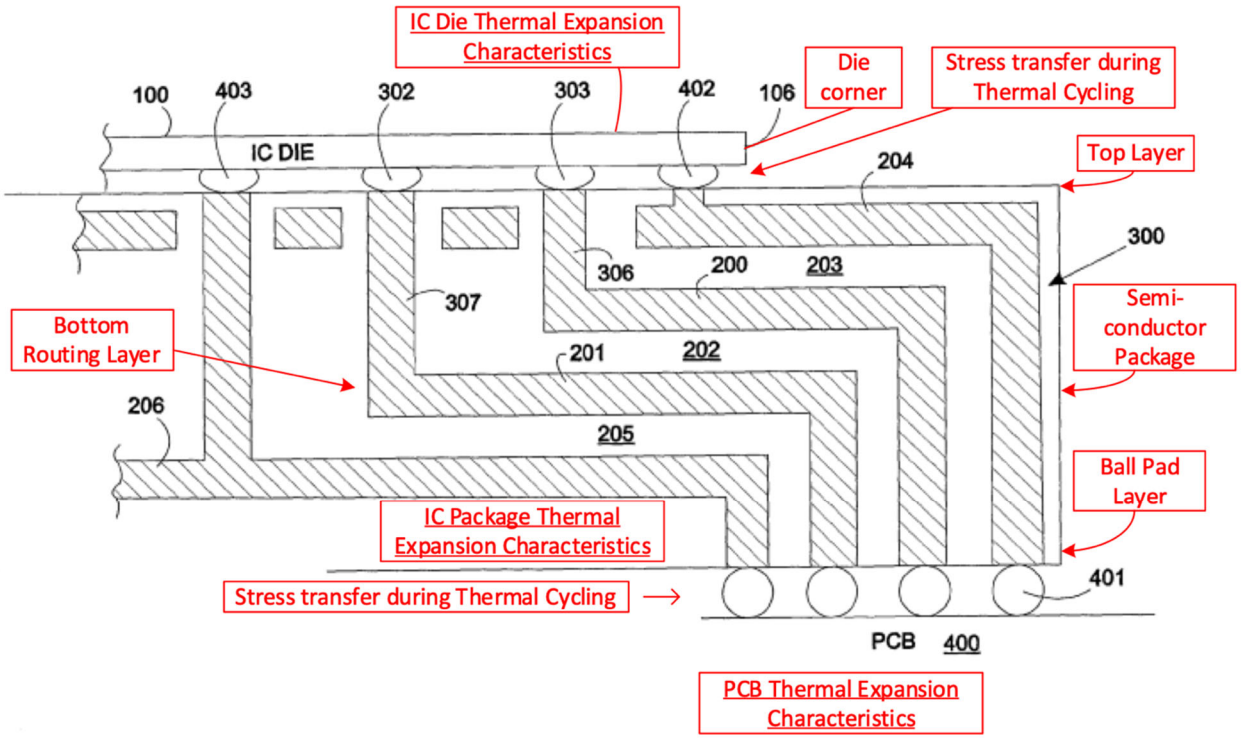
B. Ground 1 – Claims 7-8, and 10-11 are obvious by Devnani in view of Applicant’s Admitted Prior Art (AAPA)

As shown in detail below, Devnani in combination with AAPA discloses or suggest all features recited in claims 7, 8 and 10-11. (Ex. 1002, ¶¶0063-0091)

1. Claim 7

a) "A semi-conductor package comprising:"

To the extent that the preamble is limiting, Devnani discloses a semi-conductor package 300 as shown below in Figure 4. (Ex. 1005, ¶0023) (Ex. 1002, ¶¶0060-0061)



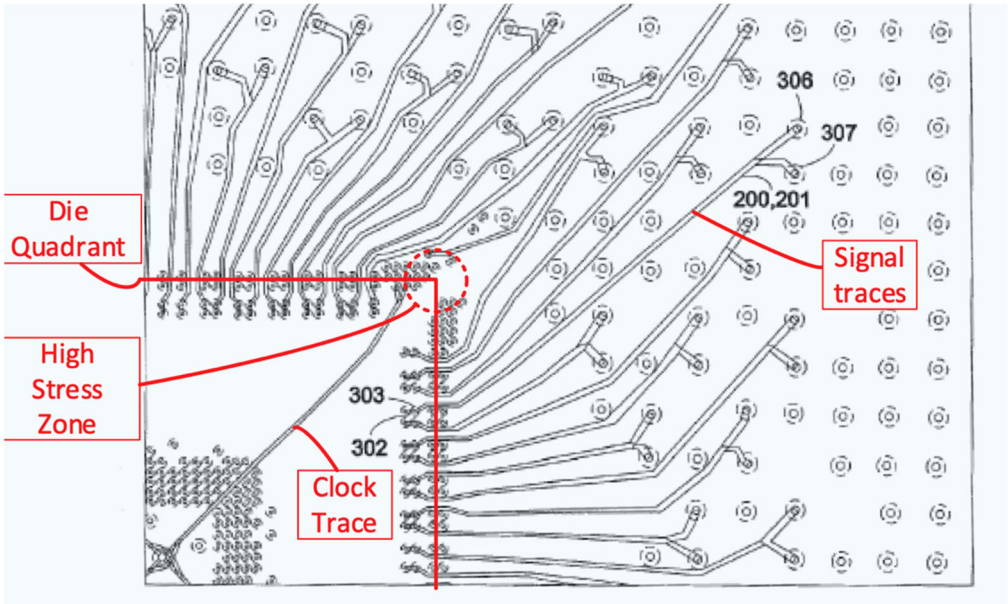
(Ex. 1001, Fig. 4 annotated)

AAPA also discloses a semi-conductor package. (Ex. 1001, 1:7-12) (Ex. 1002, ¶0062)

b) "a top layer having a die mounted thereon, said die having a corner defining a surrounding area of increased stress; and"

As shown above in Figure 4, Devnani discloses the die 100 mounted upon a top layer of the semi-conductor package 300 and the die 100 has a die edge 106 that would be understood by a POSITA to include a die corner (Ex. 1005, ¶0020) (Ex. 1002, ¶0063) Figure 4 has also been annotated to show stresses from thermal cycling based on differing thermal expansion characteristics for the various materials of the IC die, the semiconductor package, and the printed circuit board (PCB). (*Id.*)

Figure 3, shown below, has been annotated to show the area of increased stress ("high stress zone") near the die corner and how Devnani implicitly discloses routing signal traces away from such stress. However, Devnani does not explicitly state that the "corner defines a surrounding area of increased stress". (*Id.*)

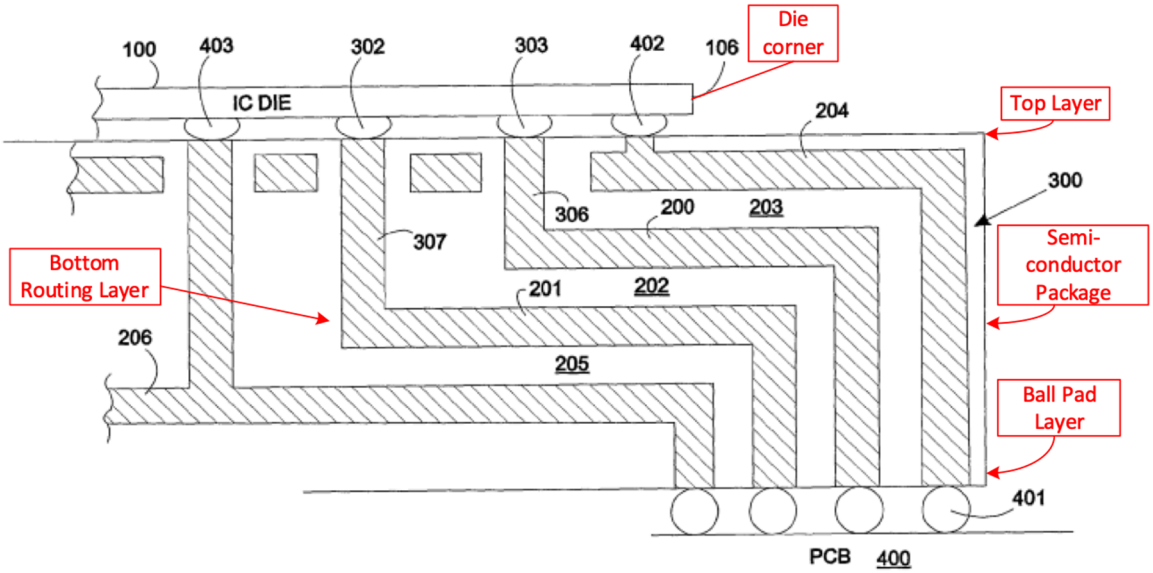


(*Id.*, Fig. 3 annotated)

However, these high stress areas were well known by a POSITA before the date of invention of the '245 patent as is shown by numerous references. (Ex. 1002, ¶¶0052-0058) This die corner stress is also supported by the Applicant's Admitted Prior Art (AAPA) of the '245 patent, which states "areas of high stress are associated with the die corner 38a and in particular the ball pads which are positioned under the area surrounding the die corner 38a." (Ex. 1001, 1:58-60). Thus, this element of claim 7 was well known prior to the invention of '245 patent. (Ex. 1002, ¶0064)

c) "a plurality of layers under the top layer, said plurality of layers comprising a bottom routing layer having signal traces thereon,"

Devnani discloses a plurality of layers in an IC package (Ex. 1005, ¶0005) and also shows in Figure 4 below, a layer for routing signals (e.g., signal 201) that is lower than other layers of the IC package. (*Id.*, ¶¶0005, 0025; Claim 1)



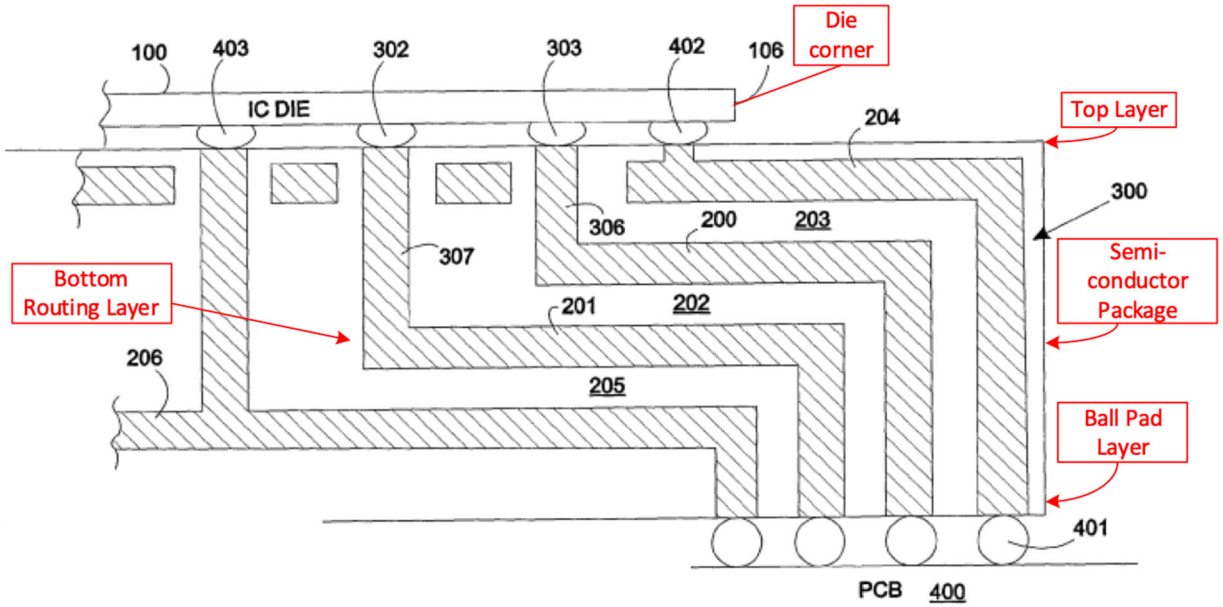
(Ex. 1005, Fig. 4 annotated)

A POSITA would understand that a "bottom routing layer" would be a routing layer beneath another layer of the IC package. (Ex. 1002, ¶0065) In the event the Patent Owner argues Devnani does not disclose this limitation, AAPA also discloses this limitation. (Ex. 1002, ¶0066)

AAPA discloses "signals are typically routed directly over the ball pads under the die corner on **the bottom routing layer**" (Ex. 1001, 1:24-26 [emphasis added]) and further discloses "a typical multi-layer organic BGA flip chip substrate that uses a 9-layer stackup". (*Id*., 1:27-29). As such, AAPA discloses a plurality of layers under a top layer (e.g., layers 2-9 of the 9-layers) and that signal traces are on a bottom routing layer. As such, both Devnani and AAPA teach this claim limitation. (Ex. 1002, ¶0070)

d) "and a ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads dispersed thereon,"

Figure 4 of Devnani, shown below, and related text discloses a ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads 401 dispersed thereon. (Ex. 1005, ¶0023) (Ex. 1002, ¶0071)

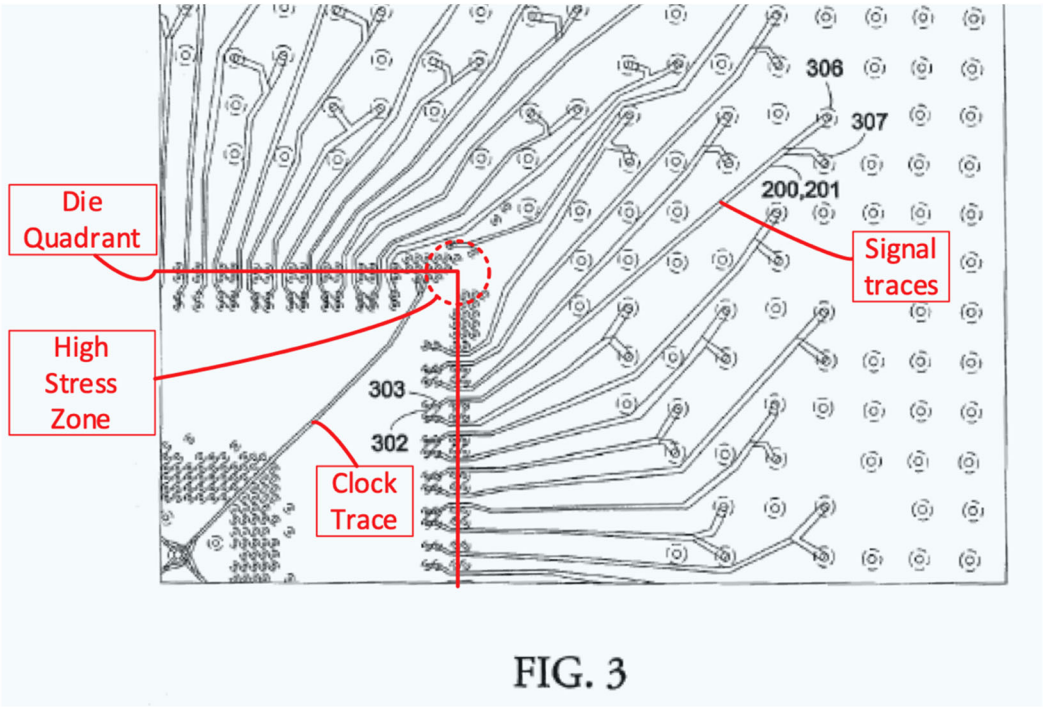


(Ex. 1005, Fig. 4 annotated)

In the event that the Patent Owner argues Devnani does not disclose this claim limitation, AAPA discloses this limitation. (Ex. 1002, ¶0068) For example, AAPA discloses a "9-layer stackup" (Ex. 1001, 1:28-35) and further discloses that "A plurality of ball pads 30 (one of which is shown) are provided on Layer L9." AAPA further discloses that "ball pads 34 of layer L9". (*Id.*, 1:57-58) As such, AAPA is disclosing a ball pad layer (L9) is under the bottom routing layer (L8) and that a plurality of ball pads (ball pads 34) are dispersed thereon. (Ex. 1002, ¶0069)

e) "wherein none of the signal traces of the bottom routing layer are located within the area of increased stress defined by the corner of the die."

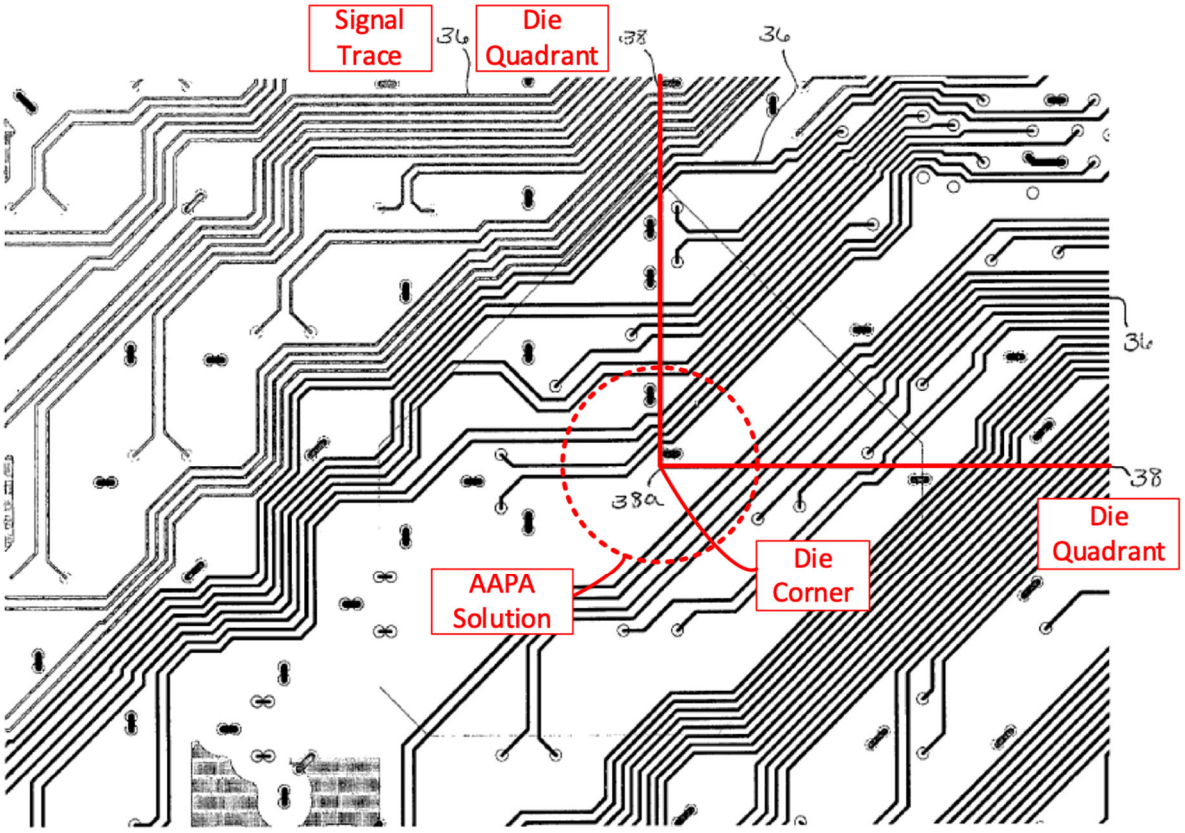
Figure 3 (below) of Devnani is annotated to show where a die quadrant resides when the IC die is mounted upon the package 300 and to identify the high stress zone associated with the corner of the die as disclosed by AAPA. (Ex. 1002, ¶0070)



(Ex. 1005, Fig. 3 annotated)

As is shown above in Figure 3 of Devnani, all of the signal traces are routed away from edges of the die and outside an area (e.g., AAPA's high stress zone) associated with the die corner. (Ex. 1002, ¶0071) In the event the Patent Owner argues Devnani does not disclose the claim limitation, AAPA also discloses this claim limitation. (*Id.*)

AAPA in Figure 3 (shown below) of the ’245 patent and its accompanying description discloses an existing, *i.e.*, prior art, solution (AAPA Solution) used to prevent stress cracks in traces is by routing the traces on the bottom routing layer outside a high stress zone associated with the corner of the die. The AAPA Solution defines the high stress zone as being a circular area having a radius of 1 mm around the corner of the die. In particular, AAPA states that “Another existing solution to overcoming this problem is to define a circular shaped area with a one (1) millimeter radius using placement of the die corner 38a as the center of the circle. **When routing traces on layer L8, traces are not routed within this circular region**.”) (Ex. 1001., 2:6-11, emphasis added)



(*Id.*, Fig. 3 annotated)

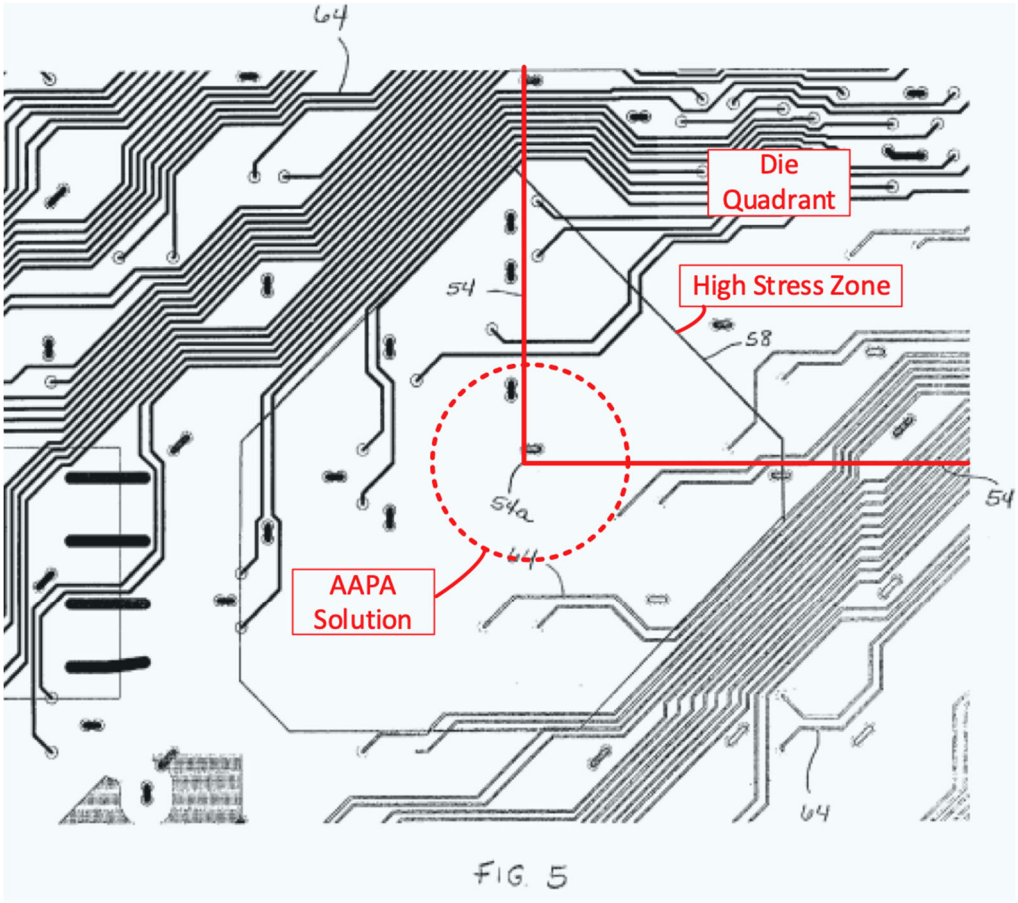
A POSITA implementing the semiconductor package of Devnani would have good reason to look to AAPA to route signal traces away from a high stress area associated with the corner of a die as they both are in the same field of semiconductor packages. As was well known years prior to the date of the '245 patent, the corner of the die and the ball pads near the corner of the die experience the most stress during thermal cycling. Thus, a POSITA would have been motivated to move traces away from high stress areas to prevent trace cracking. (Ex. 1002, ¶0073)

Further, the modification of Devnani with the AAPA would have amounted to nothing more than the use of a known technique to improve a similar device, and the

results of the modification would have been predictable. This is because at the time of the invention, a POSITA would have had the requisite skill level to readily modify the IC package disclosed by Devnani to implement the teachings of routing traces away from an area of high stress as disclosed by AAPA of the ’245 patent and numerous contemporaneous references. Moreover, such modification of Devnani would have been routine for the POSITA as they would be using well-known elements with no change in their respective functions. (Ex. 1002, ¶0074)

Notably, the only difference between the AAPA solution and the purported invention of the ’245 patent is the increased area of the high stress zone as shown below in Fig. 5 of the ’245 patent and which is annotated with a rough estimate of the high stress area of the AAPA solution. The AAPA Solution defines the area of increased stress as a circle centered on the corner of the die. (Ex. 1002, ¶0075)

The AAPA Solution, as shown in Figure 5 of the ’245 patent, discloses that “none of the signal traces of the bottom routing layer are located within the area of increased stress defined by the corner of the die the circle centered at the corner of the die” as required by the last element of claim 7 of the ’245 patent. (Ex. 1002, ¶0076)



(*Id.*, Fig. 5 annotated)

A POSITA would have been motivated to combine the teachings of Devnani with the AAPA Solution to select a high stress zone that is larger than the AAPA Solution to reduce potential damage to signal traces of a package during thermal cycling. A POSITA would have been motivated to select dimensions of such a high stress zone based upon an analysis of thermal expansion characteristics of die 100, the package 300, and a PCB upon which the package mounts as these characteristics were all well known as evidenced by the AAPA the numerous contemporaneous

references discussed above. Thus, claim 7 is rendered obvious by the combination of Devnani and AAPA. (Ex. 1002, ¶0077)

2. Claim 8

a) "A package as recited in claim 7, wherein none of the signal traces of the bottom routing layer are located within two ball pad pitches of the corner of the die."

Devnani in combination with AAPA discloses a package with signal traces on a bottom routing layer and discloses a corner of a die as discussed above in Section IX.B.1 regarding claim 7. However, Devnani does not explicitly state the signal traces that are not near the corner of the die are farther than "two ball pad pitches". However, this distance would be obvious for a POSITA implementing the IC package of Devnani-AAPA. (Ex. 1002, ¶0078)

The '245 patent discloses as AAPA that an existing solution to overcoming the problem of trace cracks near a die corner "is to define a circular shaped area with a one (1) millimeter radius using placement of the die corner 38a as the center of the circle. **When routing traces on layer L8, traces are not routed within this circular region**." (Ex. 1001, 2:7-11, emphasis added). The '245 patent states, "[a] disadvantage of having a one (1) millimeter radius region under the die corner 38a is that it is not sufficient to avoid trace cracks in the layer L8 under thermal cycling conditions for all packaging technlogies [sic]." (*Id.*, 2:11-15) (Ex. 1002, ¶0079)

Thus, a POSITA would have been motivated to use a larger area than the AAPA solution--e.g., an area with a diameter 2 ball pad pitches from the corner of the die, rather than a smaller circle with a 1 mm radius, to decrease the risk of cracks in signal traces during thermal cycling of the semiconductor package. Simply using a larger area (high stress zone) within which to exclude signal traces uses an admittedly known technique to achieve an admittedly known result, namely a reduction in failures due to trace cracks under thermal cycling. (*Id*., ¶0080)

A POSITA would take note that in the '245 patent, there is no specific disclosure regarding any advantages, criticality, or unexpected results related to the specific selection of a high stress zone defined by 2 ball pad pitches from the corner of the die. A POSITA would have anticipated success in reducing the number of stress cracks in signal traces by routing those signal traces outside of an area larger than 1 mm from the corner of the die, which would include an area defined by 2 ball pad pitches from the corner of the die. (*Id*., ¶0081)

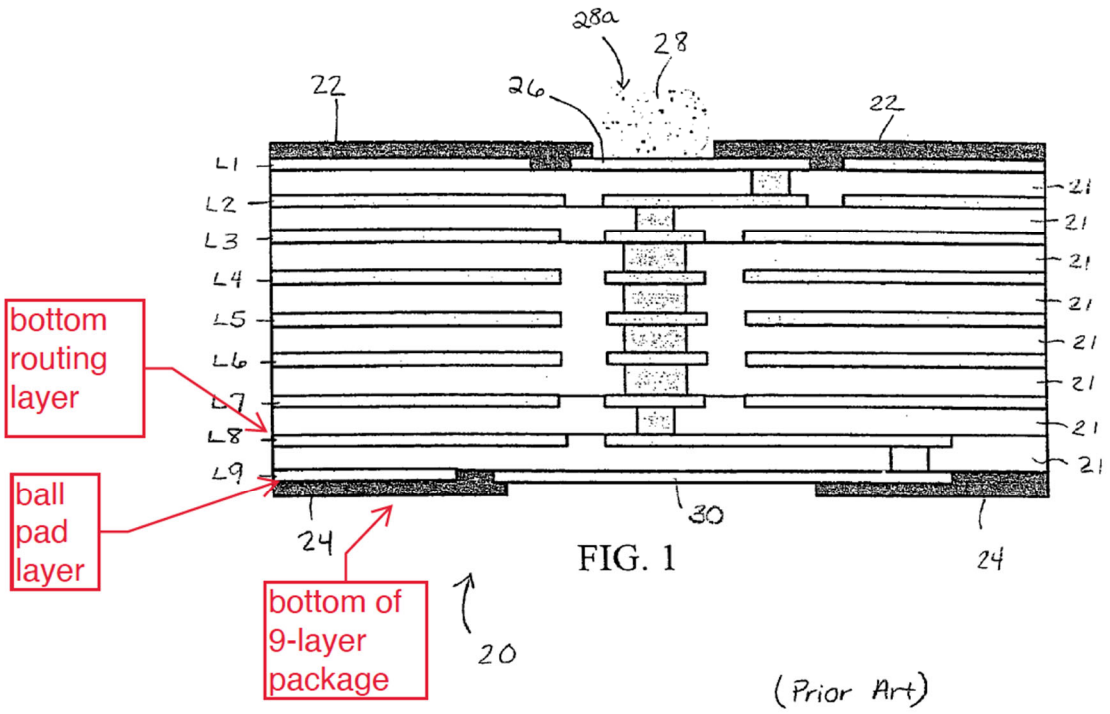
This is further evidence by AAPA, which states that "under cycled thermal excursions, cracks can initiate from the ball pad edges and spread into the layers above the ball pad layer" (Ex. 1001, 1:19-21) and "areas of high stress are associated with the die corner 38a **and in particular the ball pads** which are positioned under the area surrounding the die corner" (*Id*., 1:58-60 [emphasis added]). Thus, a POSITA would have good reason to include these areas of high stress under the ball

pads near the corner of the die when determining the size of the high stress area. Thus, claim 8 is rendered obvious by the combination of Devnani and AAPA. (Ex. 1002, ¶0082)

3. Claim 10

a) "A package as recited in claim 7, wherein the package comprises nine layers with the routing layer being the eighth layer, and the ball pad layer being the ninth layer, on a bottom of the package."

Devnani in combination with AAPA discloses a package with nine layers with a routing layer on layer 8 and a ball pad layer on layer 9 as discussed above in Section IX.B.1(d) regarding claim 7 (Ex. 1002, ¶0083)



(Ex. 1001, Fig. 1)

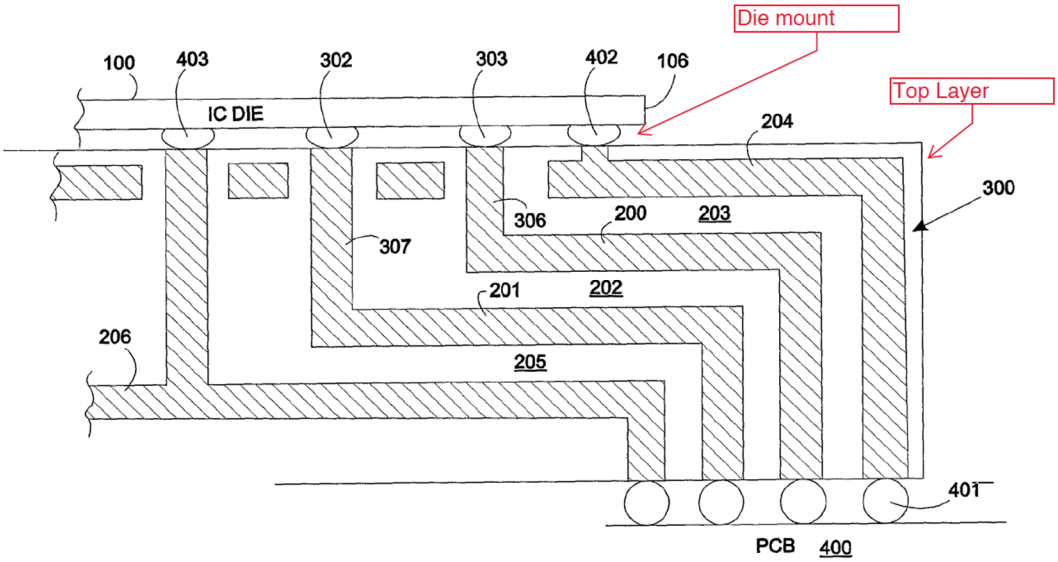
This is further evidenced by Figure 1 of the ’245 patent, which shows a prior art IC package with 9 layers, with a bottom routing layer on layer 8 and a ball pad layer on layer 9. A POSITA would have been motivated to combine the AAPA 9-layer stackup with a ball pad layer and routing layer with the IC package of Devnani to route signals, power, and ground between a die and a PCB as was widely known in the art. Thus, the combination of Devnani and AAPA renders claim 10 obvious. (Ex. 1002, ¶0084)

4. Claim 11

a) “A package as recited in claim 7, wherein the die is mounted to the top layer in an arrangement other than a pin connection.”

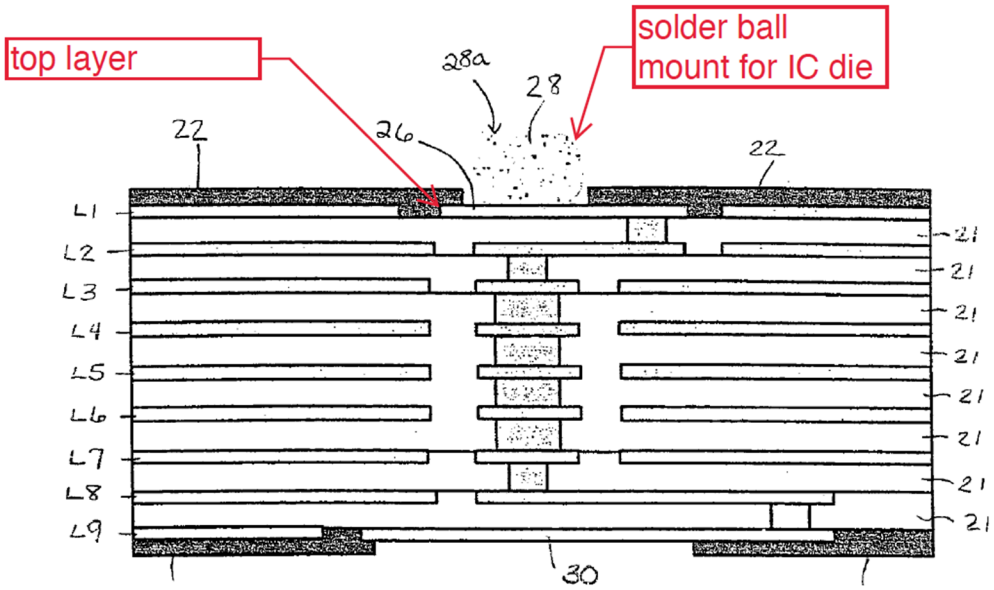
Devnani discloses the additional element of claim 11, “wherein the die is mounted to the top layer in an arrangement other than a pin connection.” (*Id*., ¶0085)

Referring to Figure 4 of Devnani (below) and related text, Devnani discloses a die 100 mounted upon a top layer of the semi-conductor package 300 via balls 302, 303, 402 and 403. (Ex. 1005, ¶0023) Devnani further discloses that the balls may be “balls of a conventional ball grid array package”. (*Id*., ¶0027)(Ex. 1002, ¶0086)



(Ex. 1005, Fig. 4 annotated)

In the event the Patent Owner argues that Devnani does not teach this claim limitation, AAPA teaches this limitation. (Ex. 1002, ¶0087) AAPA discloses "As an example, FIG. 1 (below) of the '245 patent discloses as prior art a typical multi-layer organic **BGA flip chip substrate** that uses a 9-layer stackup 20 with a thin core." (Ex. 1001., 1:26-28 [emphasis added]) (Ex. 1002, ¶0087)



(*Id.*, Fig 1 annotated)

A POSITA would understand that in BGA packages, the die is mounted to a top layer of the package using solder balls, which is "an arrangement other than a pin connection". (*Id*.)

C. Ground 2 – Claim 9 is obvious by Devnani in view of AAPA, and further in view of Pillai

1. Claim 9

a) "A package as recited in claim 7, wherein said ball pad layer has a plurality of ball pads dispersed thereon and no metal traces on the ball pad layer which are connected to the ball pads."

As shown in detail below, the combination of Devnani, AAPA, and Pillai discloses all features of claim 9. Devnani-AAPA discloses a package with a ball pad layer that has a plurality of ball pads dispersed thereon as discussed above in Section IX.B.1(d) regarding claim 7. (Ex. 1002, ¶0089)

Pillai discloses that the ball pad layer does not include metal traces connected to the ball pads as shown in a zoomed in portion of Figure 1 of Pillai below. (*Id*.)

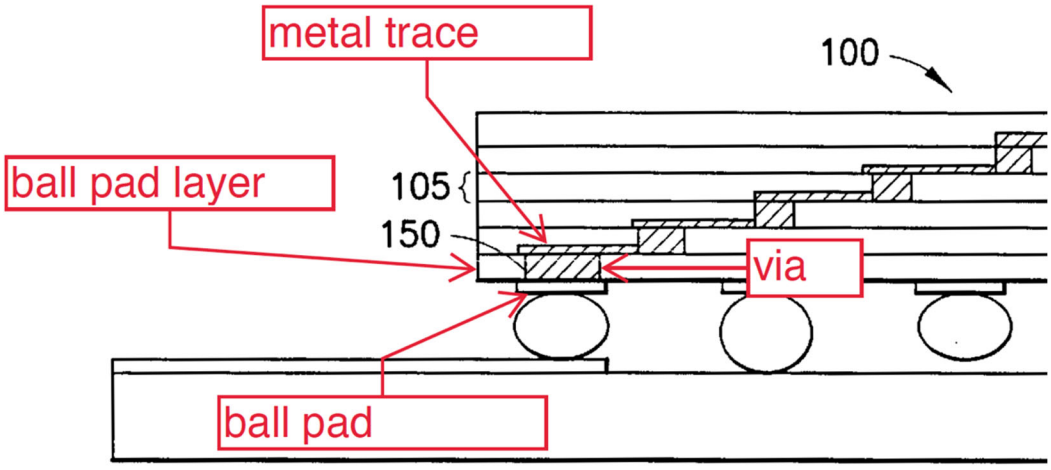


FIG. 1

(Ex. 1007, Fig. 1 annotated)

A POSITA implementing the semiconductor package of Devnani-AAPA would have had good reason to look to Pillai as they are all in the same field of IC packages. Moreover, a POSITA would have been motivated to combine the teachings of Pillai with the combination of Devnani and AAPA to use vias to connect the balls of the ball pad layer to metal traces of routing layers and NOT have metal traces on the ball pad layer. (Ex. 1002, ¶0090)

The use of vias was in widespread use at the time of the '245 patent, and a POSITA would have been motivated to combine Pillai via's to connect traces with ball pads with Devnani-AAPA semiconductor package as this would reduce potential damage to metal traces of the package during thermal cycling. (*Id.*)

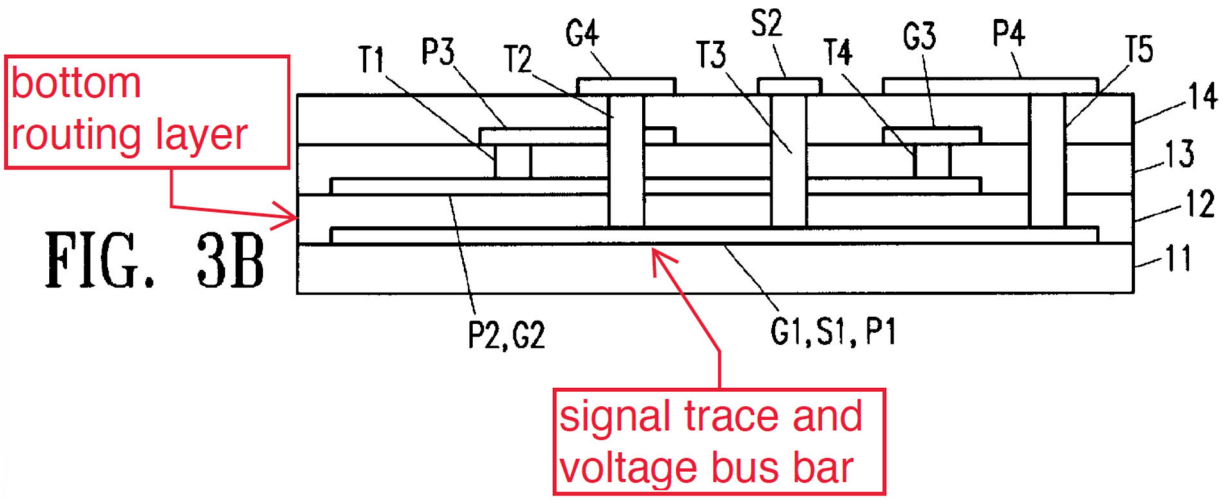
D. Ground 3 – Claim 12 is obvious by Devnani in view of AAPA, and further in view of Tanahashi

1. Claim 12

a) "A package as recited in claim 7 wherein the signal traces on the bottom routing layer comprise at least one voltage bus bar."

Devnani, AAPA and Tanahashi disclose or suggest all features recited in claim 12. (Ex. 1002, ¶¶0092-0095) The Devnani-AAPA combination discloses a package wherein the signal traces are on a bottom routing layer as discussed above in Sections IX.B.1(a)-(c) regarding claim 7 (*Id.*, ¶0092)

Tanahashi discloses a routing layer including both a signal trace (signal wiring conductor S1) and a voltage bus bar (power wiring conductor P1) on the same layer. (Ex. 1009, 13:28-33) (Ex. 1002, ¶0093)



(Ex. 1009, Fig. 3B annotated)

Tanahashi does not explicitly state that the routing layer, which includes the signal trace and the voltage bus bar, is the "bottom routing layer." However, as is shown in Figure 3B of Tanahashi, signal trace S1 and a voltage bar P1 are routed on the layer immediately above layer 11 (lowest layer). A POSITA would understand that the lower layer that included signal traces would be the "bottom routing layer." (Ex. 1002, ¶0094)

Further, a POSITA implementing the semiconductor package of Devnani-AAPA would have had good reason to look to Tanahashi as they are all directed to multilayer structures on which semiconductor devices are mounted. Such a person would have been motivated to combine Tanahashi's teaching of combining voltage conductors and signal conductors on a single layer with the Devnani-AAPA semiconductor package to provide additional routing flexibility and/or to decrease the number of layers of a semiconductor package. (*Id*., ¶0095)

E. Ground 4 – Claims 1-2 and 4-5 are obvious by Devnani in view of AAPA

As shown in detail below, Devnani and AAPA disclose or suggest all features recited in claims 1-2 and 4-5. (*Id*., ¶¶0096-0120) Independent claim 1 is very similar to independent claim 7 and similar arguments are made herein in Ground 4 as were made in Ground 1 as discussed above in Section IX.B.1 through Section IX.B.4 above.

1. Claim 1

a) "A semi-conductor package comprising: a top layer having a die mounted thereon, said die having a corner;"

b) "a plurality of layers under the top layer, said plurality of layers comprising a bottom routing layer having signal traces thereon,"

c) "and a ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads,"

Devnani-AAPA teaches these limitations. (See Sections IX.B.1(a)-(d)) (Ex. 1002, ¶¶0097-0103)

d) "wherein none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die."

Figure 3 of Devnani (shown below) is annotated to illustrate where a die quadrant resides when the IC die is mounted upon the package 300 and to identify the AAPA high stress zone associated with the corner of the die. As is shown in Figure 3 of Devnani, signal traces 200 of the bottom routing layer are routed from edges of the die and around an area (e.g., the AAPA high stress zone) associated with the die corner. (Ex. 1002, ¶0104)

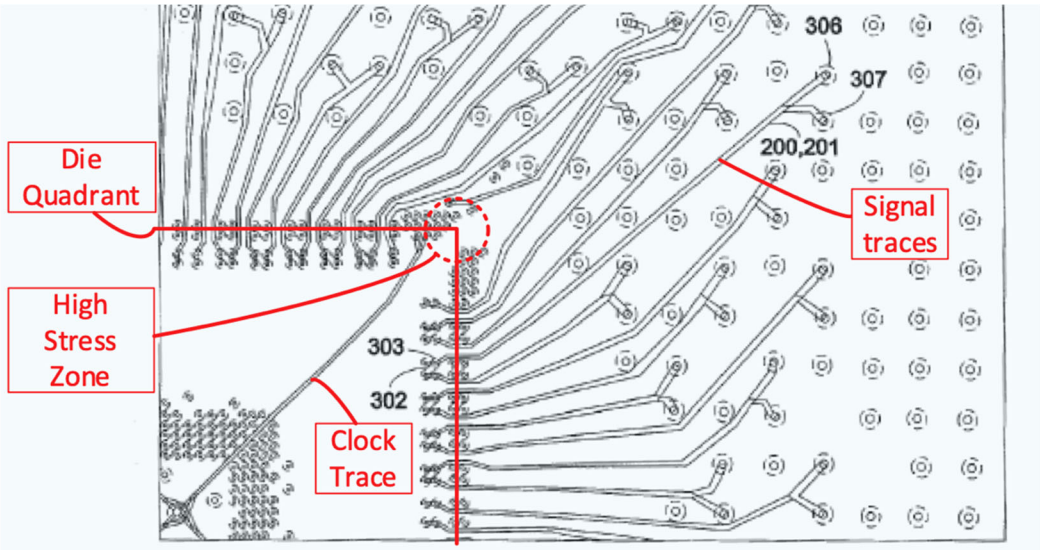


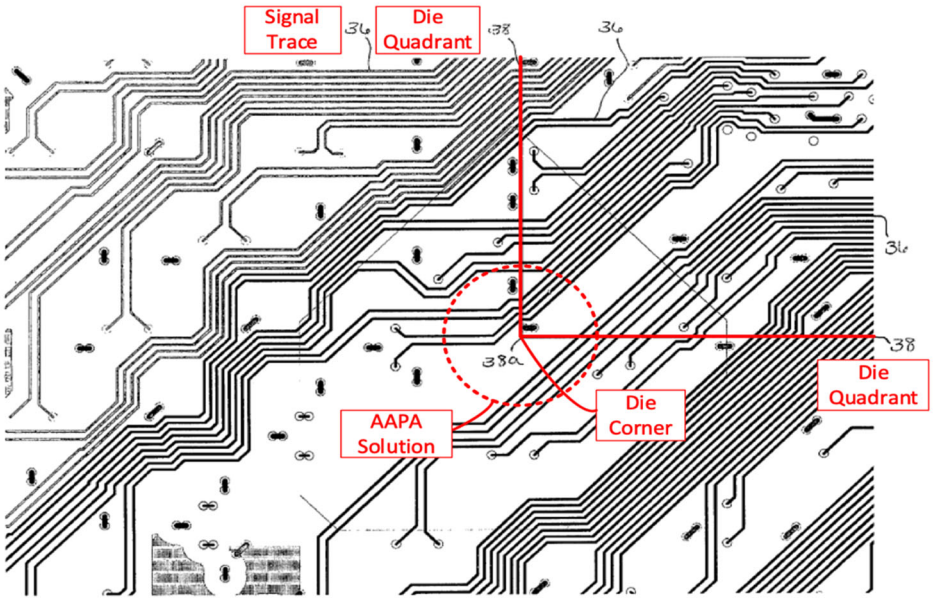
FIG. 3

(Ex. 1005, Fig. 3 annotated)

This inherent feature of Devnani shows all signal traces 200 of the bottom routing layer being routed away from the high stress zone. With all signal traces of Devnani routed away from the high stress zone, "none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer" in the high stress area. (Ex. 1002, ¶0105)

However, Devnani does not explicitly disclose that high stress area is defined by "two ball pad pitches of the corner of the die." However, AAPA renders this claim element obvious. (*Id.*)

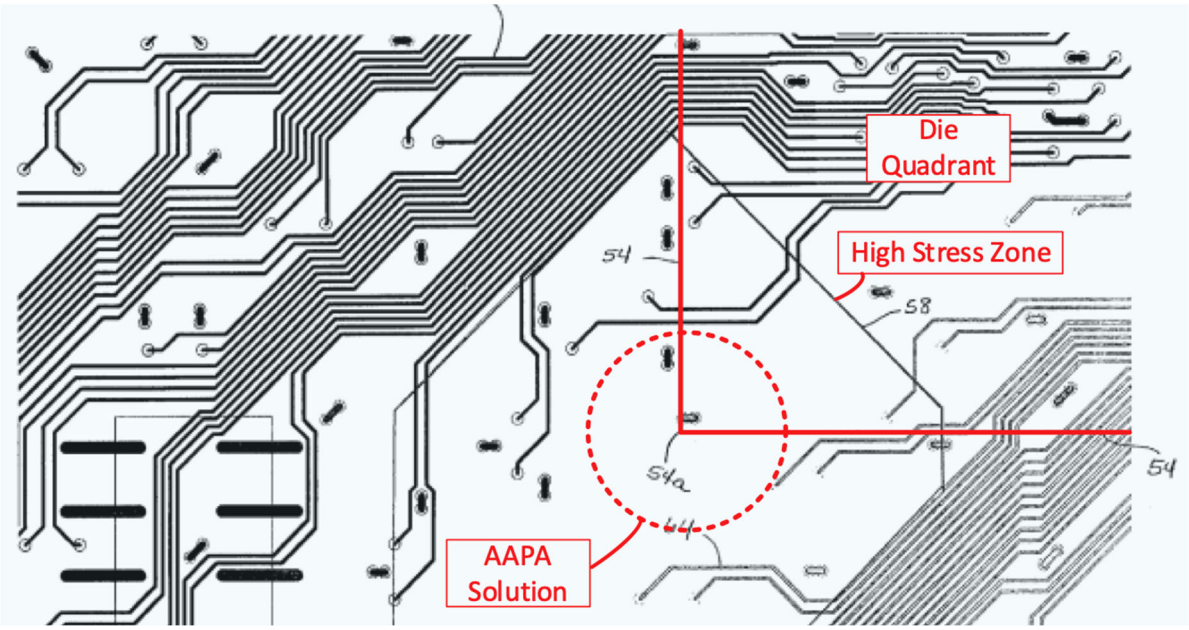
AAPA in Figure 3 of the '245 patent and its accompanying description discloses an existing, *i.e.*, prior art, solution (AAPA Solution) used to prevent stress cracks in traces is by routing the traces on the bottom routing layer outside a high stress zone associated with the corner of the die. Specifically, the AAPA of the '245 patent states "Another existing solution to overcoming this problem is to define a circular shaped area with a one (1) millimeter radius using placement of the die corner 38a as the center of the circle. **When routing traces on layer L8, traces are not** routed **within this circular region**.") (*Id.,* 2:6-11) (Ex. 1002, ¶0107)



(Ex. 1001, Fig. 3 annotated)

Figure 5 of the '245 patent (AAPA annotated), presented below, includes the AAPA Solution overlaid on the high stress zone solution purported by the '245 patent. The AAPA Solution defines the area of increased stress as a circle centered on the corner of the die. The only differences in the areas between the AAPA

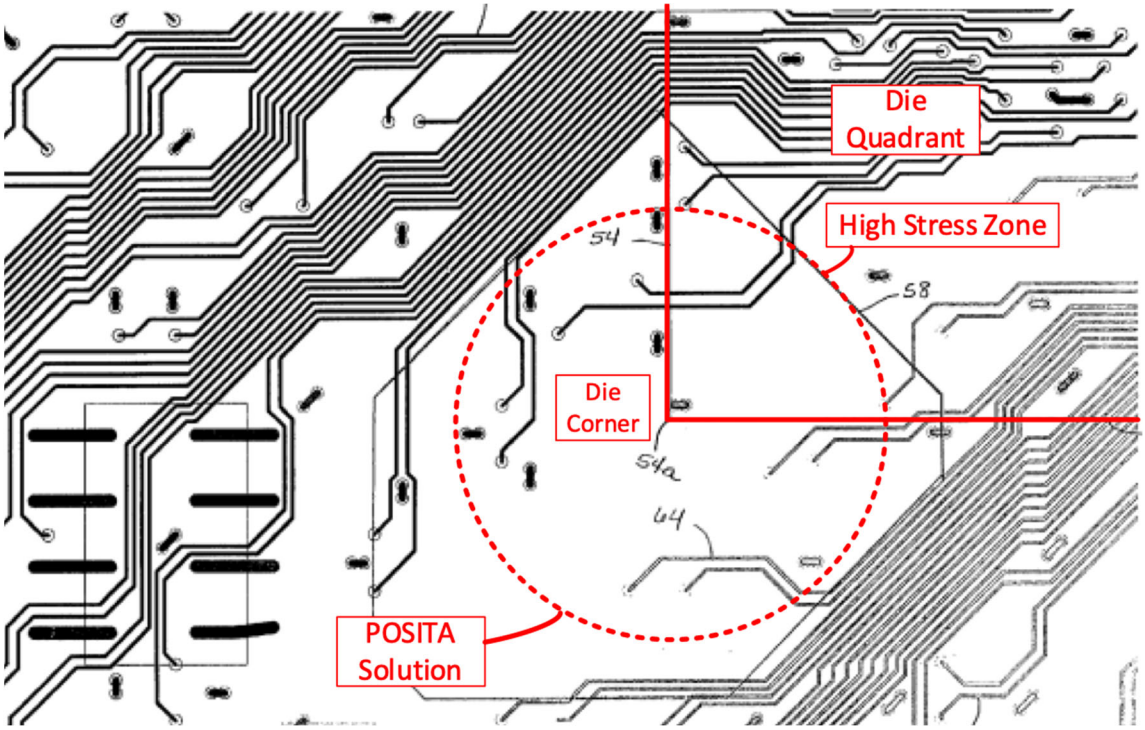
Solution and the high stress zone solution of the '245 patent illustrated in Figure 5 of the '245 patent are differing respective sizes and shapes--the shape and size of the circle of the AAPA Solution as compared to the shape and size of the die high stress zone 58. (Ex. 1002, ¶0108)



(Ex. 1001, Fig. 5 annotated)

Further, a POSITA would have known that the die corner and the underlying solder balls near the die corner would be high stress points as shown by numerous references. (Ex. 1002, ¶¶46-47, 52-57) Thus, a POSITA would have been motivated to define an area sufficient in size such that traces would not crack due to thermal cycling and would have been motivated to move traces from under ball pads (great stress areas) for the same reason the AAPA moved traces from a 1mm circular radius from the corner of the die (great stress area). (Ex. 1002, ¶0108)

This POSITA solution is illustrated in Figure 5 (below) of the '245 patent. The POSITA solution overlays the purported solution of the '245 patents' high stress zone. The only difference between the AAPA Solution and the POSITA Solution is the size of the circle, both of which are centered on the die corner 54a, and routing traces from high stress points (corner of die and underlying solder balls). This POSITA Solution is nearly identical to the high stress zone solution of Figure 5. The shape of the area of increased stress presented in Figure 5 of '245 patent differs from the circular POSITA Solution only in its shape. (Ex. 1002, ¶0109)



(Ex. 1001., Fig. 5 annotated)

Claim 1 of the '245 patent does not require a particular shape of a high stress zone, only that "none of the signal traces of the bottom routing layer are located over

ball pads of the ball pad layer which are disposed **in an area within two ball pad pitches of the corner of the die.**" (Ex. 1001, Claim 1 emphasis added) (Ex. 1002, ¶0110)

A POSITA implementing the Devnani-AAPA semiconductor package substrate, would have been motivated to use a larger area--e.g., an area with **a diameter 2 ball pad pitches from the corner of the die**, rather than a smaller circle with a 1 mm radius, to decrease risk of cracks in signal traces during thermal cycling of the semiconductor package and further would have been motivated to move traces from under ball pads near corner of die (high stress points) for the same reason the AAPA solution moved traces from the corner of a die (high stress area). Simply using a larger area (high stress zone) within which to exclude signal traces uses an admittedly known technique to achieve an admittedly known result, namely a reduction in failures due to trace cracks under thermal cycling. (Ex. 1002, ¶0111)

A POSITA would take note that there is no specific disclosure in the '245 patent regarding any advantages, criticality, or unexpected results related to the specific selection of the **shape** or **size** of the high stress zone. Thus, a POSITA would naturally select an any size or shaped area they believed would result in reducing failures due to trace cracks. As such, a POSITA would have anticipated success in reducing the number of stress cracks in signal traces by routing signal traces around a larger area than 1 mm from the corner of the die, such area defined by 2 ball pad

pitches from the corner of the die, and around other stress points such as ball pads near the die corner. (Ex. 1002, ¶0112)

Further, courts typically find shape modifications without clear significance to be obvious. *See In re Dailey,* 357 F.2d 669, 149 USPQ 47 (CCPA 1966) (holding that **the configuration** of the claimed disposable plastic nursing container **was a matter of choice** which a person of ordinary skill in the art would have found obvious **absent persuasive evidence** that **the particular configuration** of the claimed container **was significant**. [emphasis added]) Thus, simply changing the size or shape of an area (e.g., AAPA high stress area) to a different area (e.g., POSITA high stress area and the '245 patents' high stress zone) would have been obvious to a POSITA as there is no articulated reason, much less persuasive evidence, for the particular configuration of the high stress zone being "two ball pad pitches" in the '245 patent.

2. Claim 2

a) "A package as recited in claim 1, wherein none of the signal traces of the bottom routing layer are located within two ball pad pitches of the corner of the die."

The combination of Devnani-AAPA discloses this claim limitation as discussed above in Section IX.D.1(d) regarding claim 1. As discussed above, Devnani-AAPA would lead a POSITA to route traces of a bottom routing layer away from a high stress area (e.g., corner of a die). (Ex. 1002, ¶0113). Further, numerous

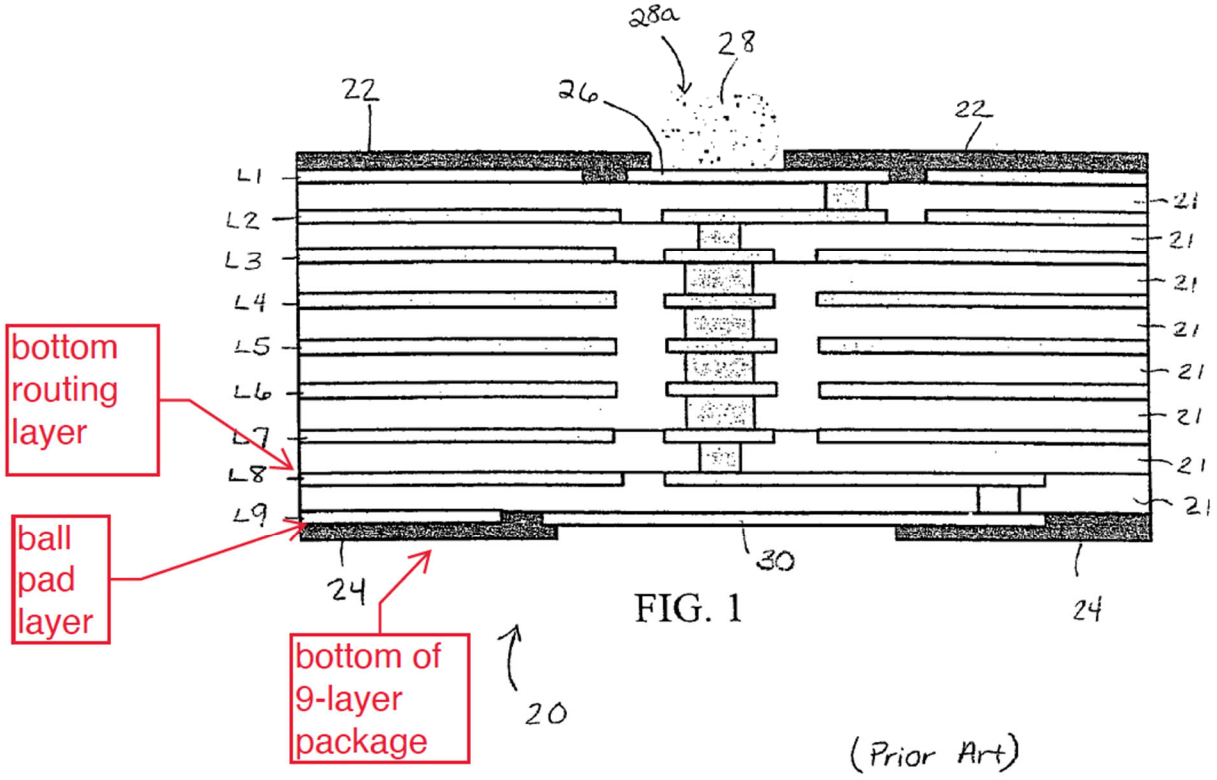
references disclose that stresses (e.g., from the edges or corner of the die, and from ball pad areas near the die corner) could cause cracking. (see generally Ex. 1010, Ex. 1011, Ex. 1016, Ex. 1017, Ex. 1018, AAPA of Ex. 1001) As such, a POSITA would be motivated to define the contours of the AAPA's high stress area to route Devnani's traces away from this area to reduce track cracking and this area would include a distance of two ball pad pitches. (Ex. 1002, ¶0114)

3. Claim 4

a) "A package as recited in claim 1, wherein the package comprises nine layers with the routing layer being the eighth layer and the ball pad layer being the ninth layer, on a bottom of the package"

The combination of Devnani-AAPA teaches this claim limitation as discussed above in Section IX.B.3(a) regarding claim 10. (*Id*., ¶0115) However, for further evidence, see Figure 1 of the '245 patent (below), which shows a prior art IC package with 9 layers, with a bottom routing layer on layer 8 and a ball pad layer on layer 9. A POSITA would have been motivated to combine the AAPA 9-layer stackup 20

with the package 30 of Devnani to route signals, power, and ground between a die and a PCB as was widely known in the art. (Ex. 1002, ¶0116)



(Ex. 1001, Fig. 1 annotated)

4. Claim 5

a) "A package as recited in claim 1, wherein the die is mounted to the top layer in an arrangement other than a pin connection."

Devnani-AAPA discloses this limitation as discussed above in Section IX.B.4 regarding claim 11. The same rationale applies to claim 5 as applied to claim 11. (Ex. 1002, ¶¶0117-0120)

F. Ground 5 – Claim 3 is obvious by Devnani in view of AAPA, and further in view of Pillai

a) "A package as recited in claim 1, wherein said ball pad layer has a plurality of ball pads dispersed thereon and no metal traces on the ball pad layer which are connected to the ball pads."

Devnani-AAPA discloses this limitation as discussed above in Section IX.C.1 regarding claim 9. The same rationale applies to claim 3 as applied in claim 9. (Ex. 1002, ¶¶0121-0123)

G. Ground 6 – Claim 6 is obvious by Devnani in view of AAPA, and further in view of Tanahashi

a) "A package as recited in claim 1, wherein the signal traces on the bottom routing layer comprise at least one voltage bus bar."

Devnani-AAPA discloses this limitation as discussed above in Section IX.D.1 regarding claim 12. The same rationale applies to claim 6 as applied in claim 12. (Ex. 1002, ¶¶0124-0128)

H. Ground 7 – Claims 1, 2 and 5 are obvious by Chung in view of Celeron

As shown in detail below, Chung and Celeron disclose or suggest all features recited in claims 1 and 5. (Ex. 1002, ¶¶0129-0149)

1. Claim 1

a) "A semi-conductor package comprising a top layer having a die mounted thereon, said die having a corner;"

Chung discloses a semi-conductor package having a top layer having a die mounted thereon, where the die has a corner as shown below in Figure 3. Figure 3 also shows (below) a top layer, which is made up of multiple vertically arranged portions. "FIG. 3 illustrates a three-dimensional view of an electrical assembly in accordance with one embodiment of the present invention. The electrical assembly includes an integrated circuit 302 (IC) and an IC package consisting of a vertical package section 304 and a horizontal package section 306." (Ex. 1006, ¶0027) (Ex. 1002, ¶0130)

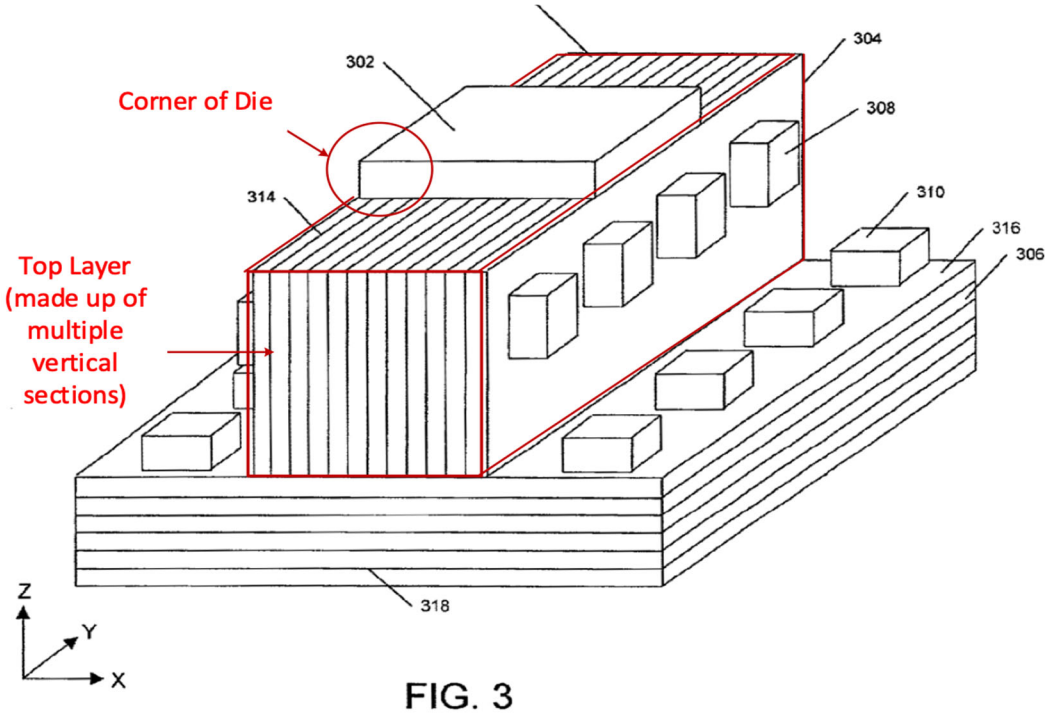


FIG. 3

(Ex. 1006, Fig. 3 annotated)

b) "a plurality of layers under the top layer, said plurality of layers comprising a bottom routing layer having signal traces thereon"

Chung in Figure 3 (above) illustrates a plurality of layers under the top layer. "Horizontal section 306 includes multiple layers of conductive materials separated by multiple layers of dielectric materials." (*Id.,* ¶0037)

Figure 5 of Chung, reproduced below in an annotated form below, illustrates that the plurality of layers includes a bottom routing layer 544, which can include traces used to route signals, power, and ground. "Each of these conductive layers 540, 542, 544 could include planar conductive areas and/or traces." (*Id.,* ¶0050) "The function of the horizontal section 306 is to carry I/O signals, power, and ground between the next level of interconnect and vertical section 304." (*Id.,* ¶0038)

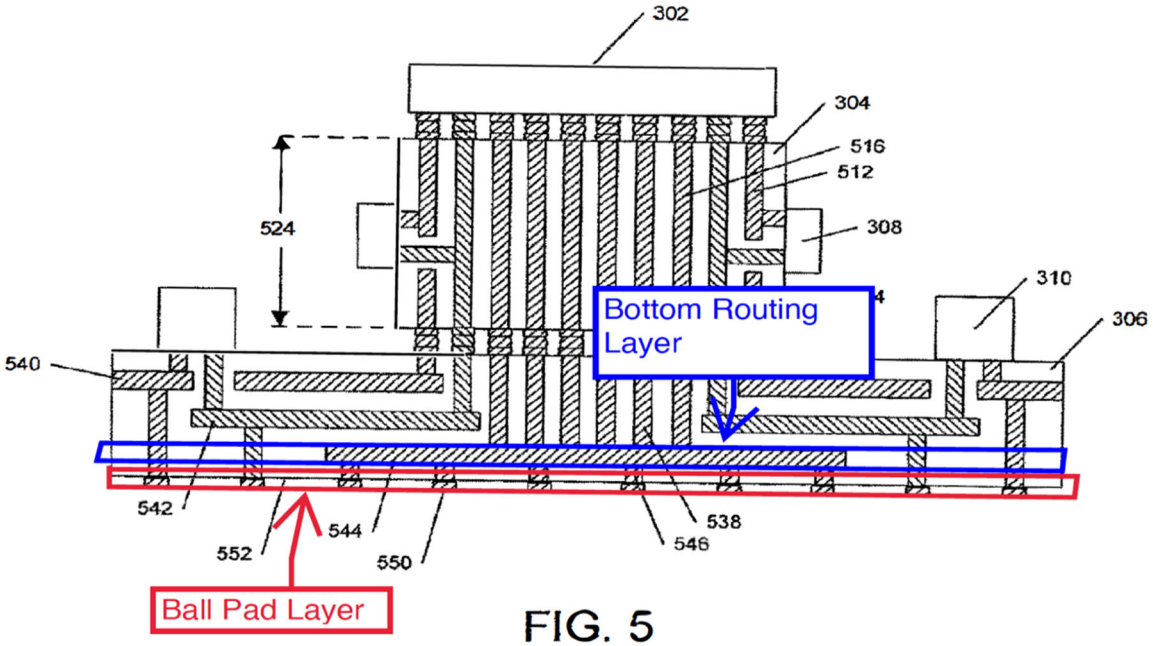


FIG. 5

(*Id*., Fig. 5 annotated)

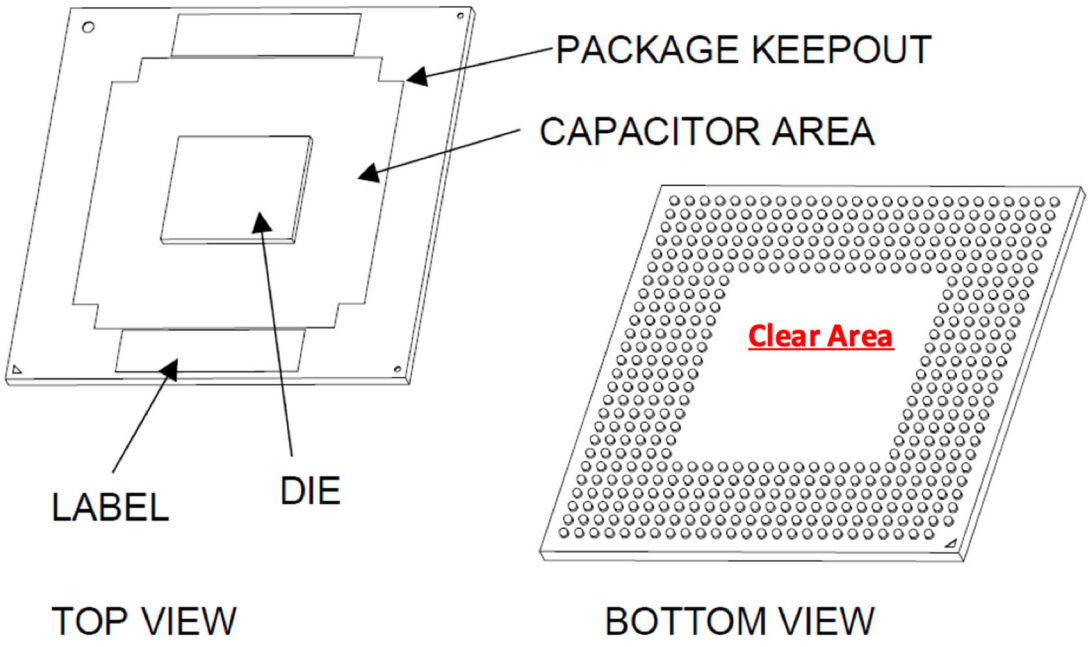
c) "a ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads"

Chung includes a ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads as shown by bond pads 550 in Figure 5 above being on the ball pad layer. Chung further discloses that "along with vias 538, 546, conductive layers 540, 542, 544 electrically connect the set of top surface bond pads with a set of connectors (e.g., bond pads 550 or pins) on the bottom surface 552 of horizontal section 306". (Ex. 1006, ¶0050) As such, a POSITA would have understood Chung's bond pads on the bottom surface of the horizontal section correspond to the ball pad layer of claim 1. (Ex. 1002, ¶0133)

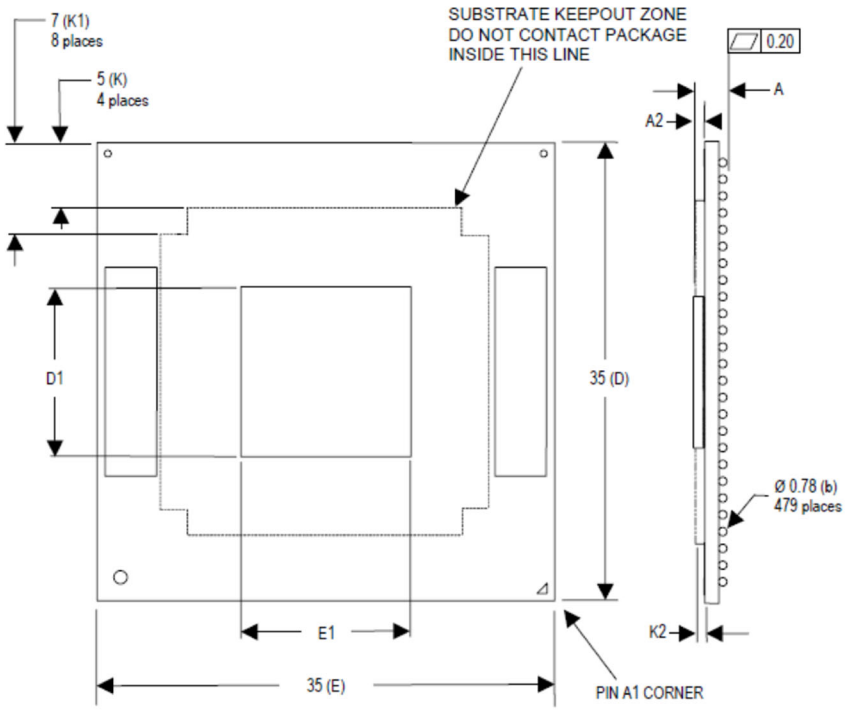
d) "wherein none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die."

Chung does not explicitly show that "none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die" required by the last element of claim 1. (Ex. 1002, ¶0134)

However, Celeron, in the same field of endeavor, discloses a clear area (shown in Figure 28 below) that is devoid of ball pads on the bottom of the semiconductor package. (Ex. 1008, p. 69-72) (Ex. 1002, ¶0135)



(Ex. 1008, Fig. 28 annotated)



(*Id.*, Fig. 29)

Celeron further discloses dimensions for the ball pad pitch, die size, package size, and other elements along with specific values given in Table 44 (below) that can be mapped to Figures 29 and 30 shown above. (Ex. 1008, p. 69) (Ex. 1002, ¶0136)

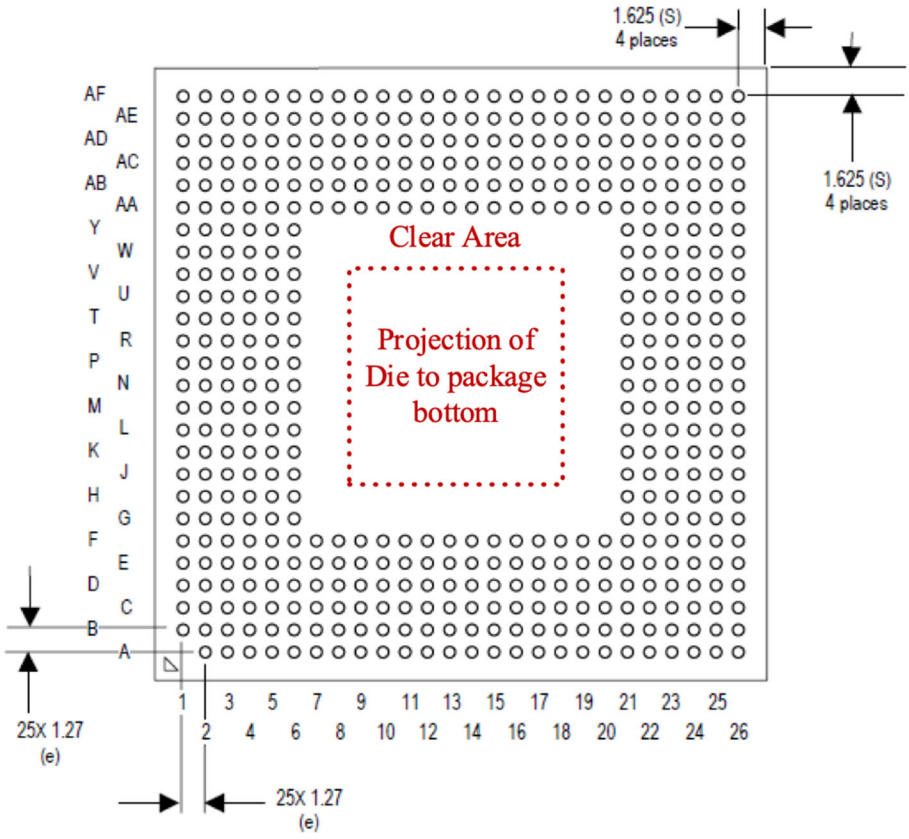
Table 44. Micro-FCBGA Package Mechanical Specifications

Symbol	Parameter	Min	Max	Unit
A	Overall height, as delivered (1)	2.27	2.77	mm
A2	Die height	0.854		mm
b	Ball diameter	0.78		mm
D	Package substrate length	34.9	35.1	mm
E	Package substrate width	34.9	35.1	mm
D1	Die length	11.18[3] 10.82[4]		mm
E1	Die width	7.20[3] 6.85[4]		mm
e	Ball pitch	1.27		mm
N	Ball count	479		each
K	Keep-out outline from edge of package	5		mm
K1	Keep-out outline at corner of package	7		mm
K2	Capacitor keep-out height	-	0.7	mm
S	Package edge to first ball center	1.625		mm
--	Solder ball coplanarity	0.2		mm
Pdie	Allowable pressure on the die for thermal solution	-	689	kPa
W	Package weight	4.5		g

(Ex. 1008, Table 44)

As illustrated by Celeron in Figure 30 below, the ball pad pitch is approximately 1.27 mm. (Ex. 1008, Fig. 30 (dimension e), Table 44 (dimension e)). Celeron discloses that the largest edge of the largest die is 11.18 mm long and the die is centered in the semiconductor package, which has a minimum length of 34.9 mm. (Ex. 1008, Table 44 (dimensions D, E, D1, E1)). The closest that any of the four corners of the die is located in relation to the edge of the clear zone, which is

clear of ball pads, is 3.10 mm, which is greater than two ball pad pitches. (Ex. 1002, ¶0137)



(Ex. 1008, Fig. 30 annotated)

The edge of the clear zone (the area devoid of ball pads) is 8.76 mm from each package edge. (*Id.,* Fig. 30 (dimensions S, e, and b), Table 44 (dimensions S, e, and b) (dimensions S (1.625) + 5 X e (1.27) + b (.78)) Celeron discloses that the largest die is 11.18 mm long. (Ex. 1008, Fig. 29 (dimension D1), Table 44 (dimension D1)). Celeron further discloses that the die is centered on top of the semiconductor package. (Ex. 1008, Figs. 28, 29) The nominal distance from the center of the

minimum length package to its edge is 17.45 mm. (*Id.*, (dimension D/2)). (*Id.*, (dimension D/2)) (Ex. 1002, ¶0138)

Celeron further discloses that the distance from the center of the package to the edge of the largest die positioned at the center of the package is 5.59 mm. (*Id.,* (dimension D1/2)). Thus, the distance from the edge of the package to the edge of the largest die is 11.86 mm. (*Id*., (D/2 – D1/2)). The edge of the clear zone is 8.76 mm, making the distance from the edge of the die going to the edge of the clear zone being 3.10 mm, which is greater than 2.54 mm (two ball pad pitches). (Ex. 1002, ¶0139)

Thus, *Celeron*, discloses that there are no ball pads on the ball pad layer "disposed in an area within two ball pad pitches of the corner of the die." Because there are no ball pads "disposed in an area within two ball pad pitches of the corner of the die, there can be no "signal traces of the bottom routing layer [that] are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die," as recited by claim 1. (Ex. 1002, ¶0140)

A POSITA implementing the IC package of Chung would have had good reasons to look to Celeron as they both are in the same field of IC packages. Moreover, it would be straightforward for such a person to implement the clear area of Celeron in Chung's IC package as Celeron clear area would not change function when implemented in Chung's package. A POSITA would have been motivated to

combine the multiple routing layers of Chung with the clear area of Celeron to prevent damage to signal traces of the bottom routing layer during thermal cycling. (Ex. 1002, ¶0141) Thus, the combination of Chung and Celeron renders obvious claim 1.

2. Claim 2

a) "A package as recited in claim 1, wherein none of the signal traces of the bottom routing layer are located within two ball pad pitches of the corner of the die."

The Celeron-Chung combination discloses a semiconductor package with a bottom routing layer and no ball pads within two ball pad pitches of the corner of the die as discussed above in Section IX.H.1 regarding claim 1. The additional negative element of removing ball pads within the area two ball pad pitches from the corner of the die is disclosed as discussed above because the Chung-Celeron combination discloses no solder balls within two ball pad pitches from the corner of the die. (Ex. 1002, ¶0142) As such, the combination of Devnani and AAPA renders claim 2 obvious.

3. Claim 5

a) A package as recited in claim 1, wherein the die is mounted to the top layer in an arrangement other than a pin

Chung in Figure 3 "illustrates a three-dimensional view of an electrical assembly in accordance with one embodiment of the present invention. The electrical assembly includes an integrated circuit 302 (IC) and an IC package consisting of a vertical package section 304 and a horizontal package section 306." (Ex. 1006, ¶0027) (Ex. 1002, ¶0143)

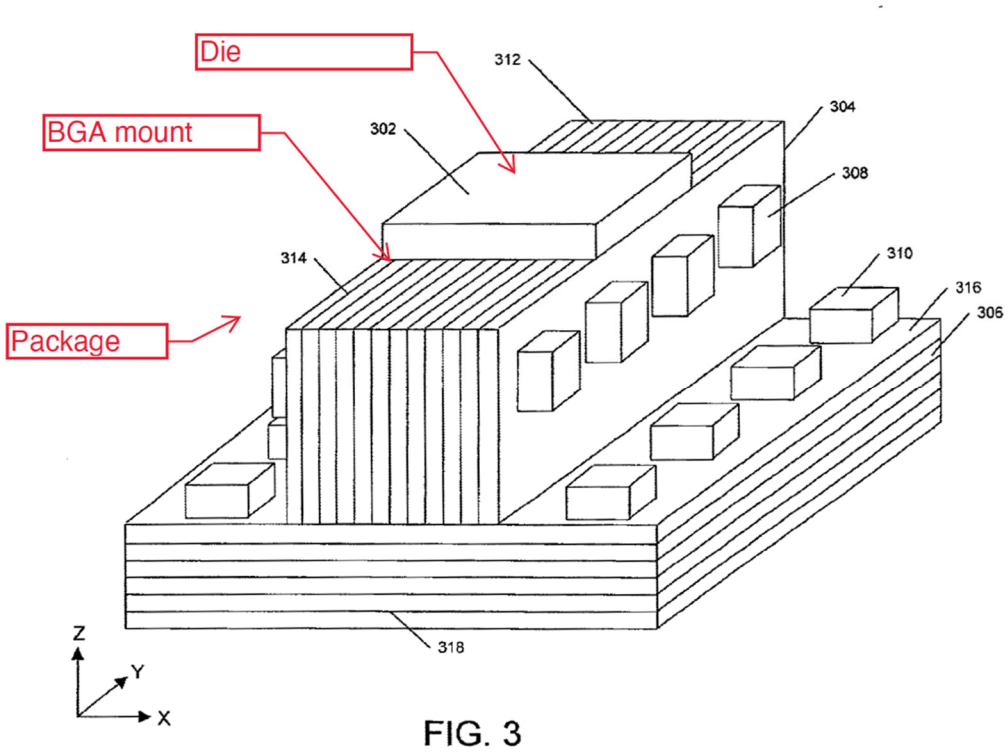


FIG. 3

(Ex. 1006, Fig. 3 annotated)

Chung further discloses, "a die mounted to the top layer of a semiconductor package in an arrangement other than a pin connection." "[T]he chip is flipped over

and attached, via solder bumps or balls to matching pads on the top surface 312 of the vertical section 304." (*Id.*, ¶0028) Solder bumps or balls are used with Ball grid array (BGA) packages, which were in widespread use prior to the invention of the '245 patent. (Ex. 1002, ¶0144).

I. Ground 8 – Claim 3 is obvious by Chung in view of Celeron, and further in view of Pillai

a) "A package as recited in claim 1, wherein said ball pad layer has a plurality of ball pads dispersed thereon and no metal traces on the ball pad layer which are connected to the ball pads."

As shown in detail below, the combination of Chung, Celeron and Pillai disclose all features of claim 3. (Ex. 1002, ¶¶0145-0148) The Chung-Celeron combination discloses an IC package with a ball pad layer having a plurality of ball pads as discussed above in Section IX.H.1 regarding claim 7. Pillai discloses no metal traces being on the ball pad layer as discussed above in Section IX.B.1

For convenience, Figure 1 of Pillai is reproduced below and illustrates that the ball pad layer does not include metal traces connected to the ball pads.

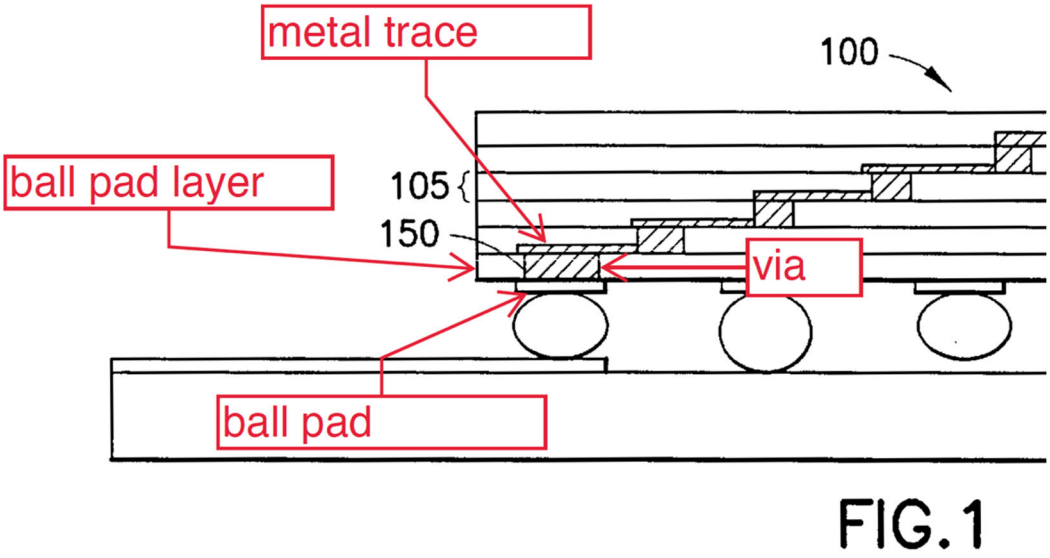


FIG. 1

(Ex. 1007, Fig. 1 annotated)

A POSITA implementing the IC package of Chung-Celeron would have had good reason to look to Pillai has they are all in the same field of IC packaging. A POSITA would have been motivated to combine the teachings of Pillai with the combination of Chung and Celeron to use vias to connect the balls of the ball pad layer to metal traces of routing layers and NOT have metal traces on the ball pad layer. The motivation to combine would be due to reduced potential damage to metal traces of the package during thermal cycling. (Ex. 1002, ¶0148)

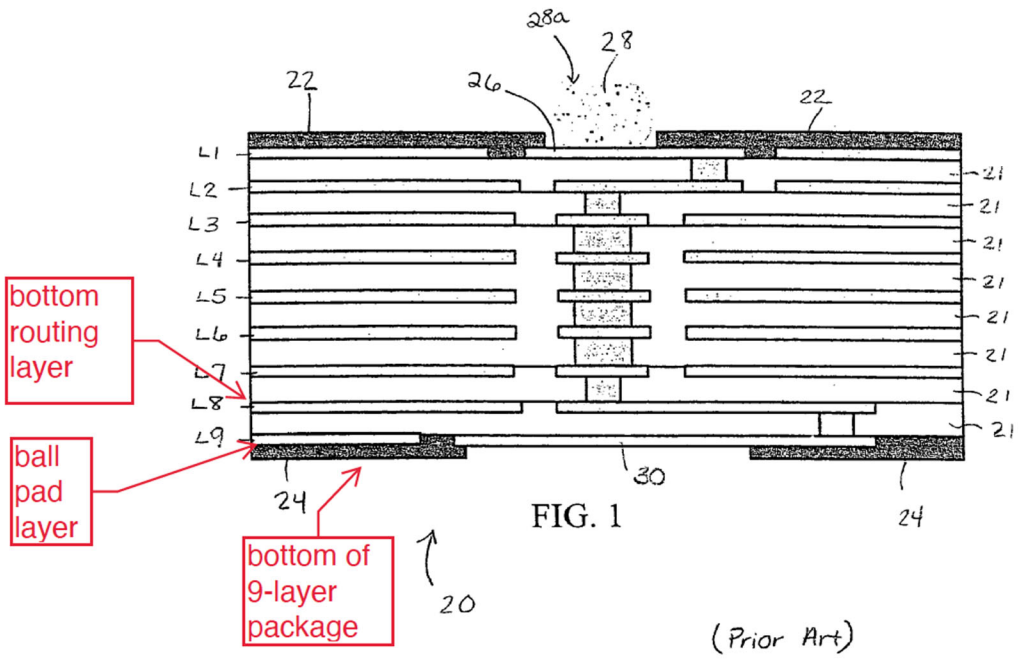
J. Ground 9 – Claim 4 is obvious by Chung in view of Celeron, and further in view of AAPA

As shown in detail below, the combination of Chung, Celeron and AAPA disclose all features of claim 4. (Ex. 1002, ¶0149)

a) "A package as recited in claim 1, wherein the package comprises nine layers with the routing layer being the eighth layer and the ball pad layer being the ninth layer, on a bottom of the package."

The Chung-Celeron combination discloses a multiple layered IC package as discussed above in Section IX.G.1. Applicant's Admitted Prior Art (AAPA) discloses the specific layers limitation as discussed above in Section IX.B.3 regarding claim 10. (Ex. 1002, ¶0150)

For example, AAPA discloses in Fig. 1, shown below, and related text that "a **plurality of ball pads 30** (one of which is shown) **are provided on Layer L9**." (Ex. 1001, 1:41-42, emphasis added) (Ex. 1002, ¶0151) AAPA also discloses "Layer L8 provides the bottom routing layer….Signal traces 36 are dispersed throughout layer L8." (Ex. 1001, 1:51-54) (Ex. 1002, ¶0152)



(*Id.*, Fig. 1 annotated)

A POSITA implementing the packages of Chung and Celeron would have been motivated to look to the AAPA 9-layer stackup 20 to route signals, power, and ground between a die and a PCB. Such a person would have had good reason to look to AAPA as Chung, Celeron and AAPA are all in the same field of IC packaging. (Ex. 1002, ¶0153)

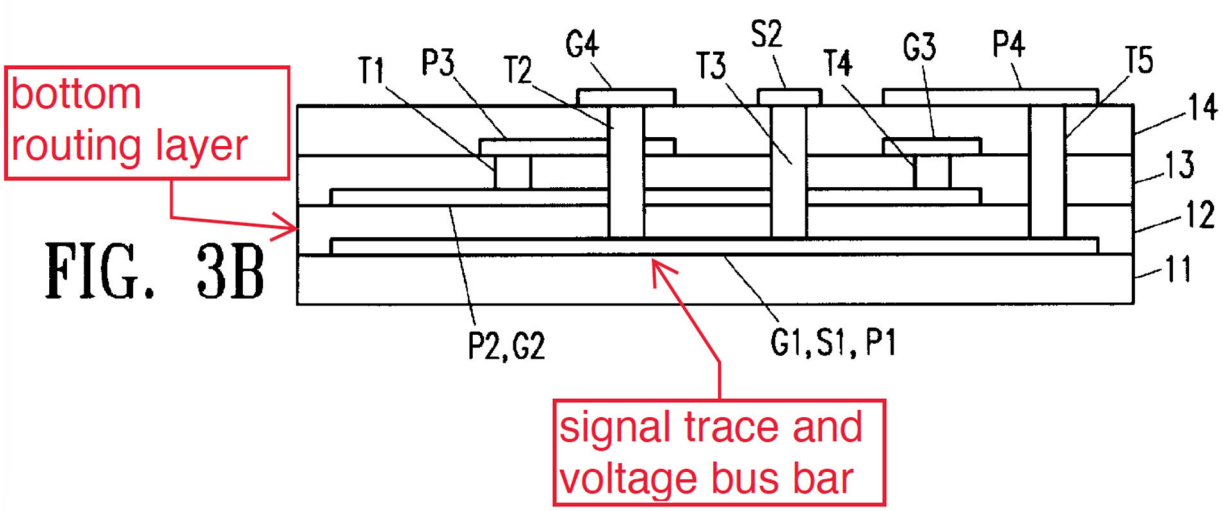
K. Ground 10 – Claim 6 is obvious by Chung in view of Celeron, and further in view of Tanahashi

a) "A package as recited in claim 1 wherein the signal traces on the bottom routing layer comprise at least one voltage bus bar."

As shown in detail below, Chung, Celeron and Tanahashi disclose or suggest all features recited in claim 6. (Ex. 1002, ¶0155) The Chung-Celeron combination

discloses an IC package with signal traces on a bottom routing layer as discussed above in Section IX.H.1 regarding claim 7.

Tanahashi discloses in Figure 3B (below) that signal traces and a voltage bus bar can be on the same layer. (*Id.*)



(Ex. 1009, Fig. 3B annotated)

Tanahashi does not explicitly state that the routing layer, which includes the signal trace and the voltage bus bar, is the "bottom routing layer." However, as is shown in Figure 3B (above) of Tanahashi, signal trace S1 and a voltage bar P1 are routed on the layer immediately above layer 11 (lowest layer). A POSITA would understand that the lower layer that included signal traces would be on the "bottom routing layer." (Ex. 1002, ¶0156)

A POSITA implementing the IC package of Chung-Celeron would have had good reason to look to Tanahashi as they are all directed to multilayer structures on which semiconductor devices are mounted. A POSITA would have been motivated

to combine Tanahashi's teaching of combining voltage conductors and signal conductors on a single layer with the Chung-Celeron semiconductor package to provide additional routing flexibility and/or to decrease the number of layers of a semiconductor package. (Ex. 1002, ¶0157)

L. Ground 11 – Claims 1 and 5 are obvious by Devnani in view of Celeron

As shown in detail below, Devnani and Celeron disclose or suggest all features recited in claims 1, 2 and 5. (Ex. 1002, ¶¶0158-0167)

1. Claim 1

a) "A semi-conductor package comprising: a top layer having a die mounted thereon, said die having a corner;"

Devnani discloses this limitation as discussed above in Section IX.A.1(a).

b) "a plurality of layers under the top layer, said plurality of layers comprising a bottom routing layer having signal traces thereon,"

Devnani discloses this limitation as discussed above in Section IX.A.1(b).

c) "and a ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads,"

Devnani discloses this limitation as discussed above in Section IX.A.1(c).

d) "wherein none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die."

Celeron discloses this limitation as discussed above in Section IX.H.1(d) regarding claim 1. A POSITA implementing the IC package of Devnani would have had good reason to look to Celeron as they are both in the same field of IC packaging. A POSITA would have been motivated to combine the routing layer of Devnani that routed traces away from high stress areas with the clear area of Celeron to prevent damage to signal traces of the bottom routing layer during thermal cycling. (Ex. 1002, ¶0162)

2. Claim 5

a) "A package as recited in claim 1, wherein the die is mounted to the top layer in an arrangement other than a pin connection."

Celeron discloses this limitation as discussed above in Section IX.H.3(a). Further, Devnani discloses that a conventional ball grid array (BGA) package could be used. (Ex. 1005, ¶0027) As stated by Devnani and numerous contemporaneous references, BGA packages were in widespread use prior to the invention of the '245 patent. A POSITA would have been motivated to use the BGA package of Devnani to mount a die upon a semiconductor package of Celeron, which "is an arrangement other than a pin connection." (Ex. 1002, ¶0163).

M. Ground 12 – Claim 6 is obvious by Devnani in view of Celeron, and further in view of Tanahashi

a) "A package as recited in claim 1, wherein the signal traces on the bottom routing layer comprise at least one voltage bus bar."

Devnani, Celeron and Tanahashi disclose or suggest all features recited in claim 6. (Ex. 1002, ¶0164-0166) The Devnani-Celeron combination discloses an IC package with as discussed above in Section IX.L.1 regarding claim 1. Tanahashi discloses in Figure 3B (below) that signal traces and a voltage bus bar can be on the same layer.

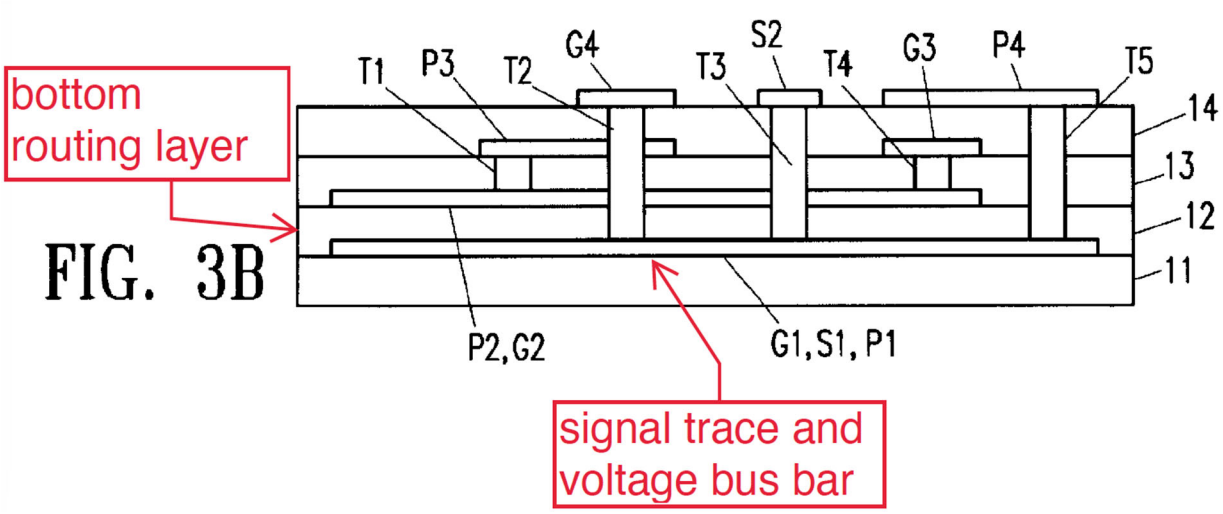


FIG. 3B

(Ex. 1009, Fig. 3B annotated)

Tanahashi does not explicitly state that the routing layer, which includes the signal trace and the voltage bus bar, is the "bottom routing layer." However, as is shown in Figure 3B (above) of Tanahashi, signal trace S1 and a voltage bar P1 are routed on the layer immediately above layer 11 (lowest layer). A POSITA would

understand that the lower layer that included signal traces would be the "bottom routing layer." (Ex. 1002, ¶0165)

A POSITA implementing the IC package of Devnani-Celeron would have had good reason to look to Tanahashi as they are all directed to multilayer structures on which semiconductor devices are mounted. A POSITA would have been motivated to combine Tanahashi's teaching of combining voltage conductors and signal conductors on a single layer with the Devnani-Celeron semiconductor package to provide additional routing flexibility and/or to decrease the number of layers of a semiconductor package. (Ex. 1002, ¶0166)

N. Ground 13 – Claim 7 is obvious by Review of BGAs, in view of Devnani and CRTA.

1. Claim 7

a) "A semi-conductor package comprising:"

To the extent the preamble is limiting, the combination of Review of BGAs, Devnani and CRTA discloses this claim feature. (Ex. 1002, ¶0167) Figure 3 of Review of BGAs, as shown and annotated below, discloses a semi-conductor package. (Ex. 1018, p. 6) (Ex. 1002, ¶0167)

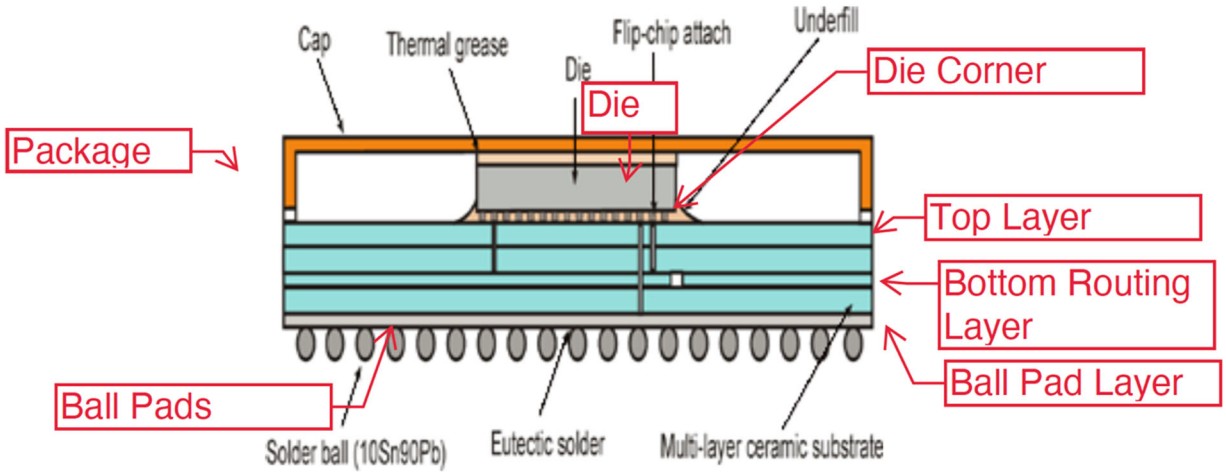


Fig. 3. Ceramic ball grid array (CBGA) [3]

(*Id.*, Fig. 3 annotated)

b) "a top layer having a die mounted thereon, said die having a corner defining a surrounding area of increased stress; and"

The combination of Review of BGAs, Devnani and CRTA discloses this claim limitation. (Ex. 1002, ¶0168) Review of BGAs shows in Figure 3 above, a die mounted upon a top layer of the semi-conductor package, where the die has a die corner. Review of BGAs further discloses "the greatest strains are found beneath the edges of the silicon die" (Ex. 1018, p. 17)

Review of BGAs does not explicitly use the term "corner". However, CRTA discloses "that thermal coefficient of expansion (TCE) mismatch have been identified by major manufacturers that cause cracking during temperature cycling". (Ex. 1016, p. 32) CRTA further discloses that the "cracking generally occurs **near the corners of the chip**". (*Id.* [emphasis added]) Further, CRTA states that "package

stress increases exponentially from the package center along a radius line to the **die corner**." (*Id.*, p. 34 [emphasis added])

A POSITA implementing the IC package of Review of BGAs would have had good reason to look to CRTA as they both are in the same field of IC packages and deal with thermal cycling stresses. Further, such a person would have been motivated to include the high stress of a die corner of CRTA in implementing a change to the BGA package of Review of BGAs to reduce package failure. Such a modification would have been straightforward for such a person as it would be a simple substitution of including the high stress of at a die corner with Review of BGAs stress along a die edge in a package design. (Ex. 1002, ¶0169)

c) "a plurality of layers under the top layer, said plurality of layers comprising a bottom routing layer having signal traces thereon,"

d) "and a ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads dispersed thereon,"

The combination of Review of BGAs, Devnani and CRTA discloses these claim limitations. (Ex. 1002, ¶0170)

Review of BGAs shows in Figure 3, below, the package has a plurality of layers, that include a top layer, a bottom routing layer, and a ball pad layer under the bottom routing layer having a plurality of ball pads.

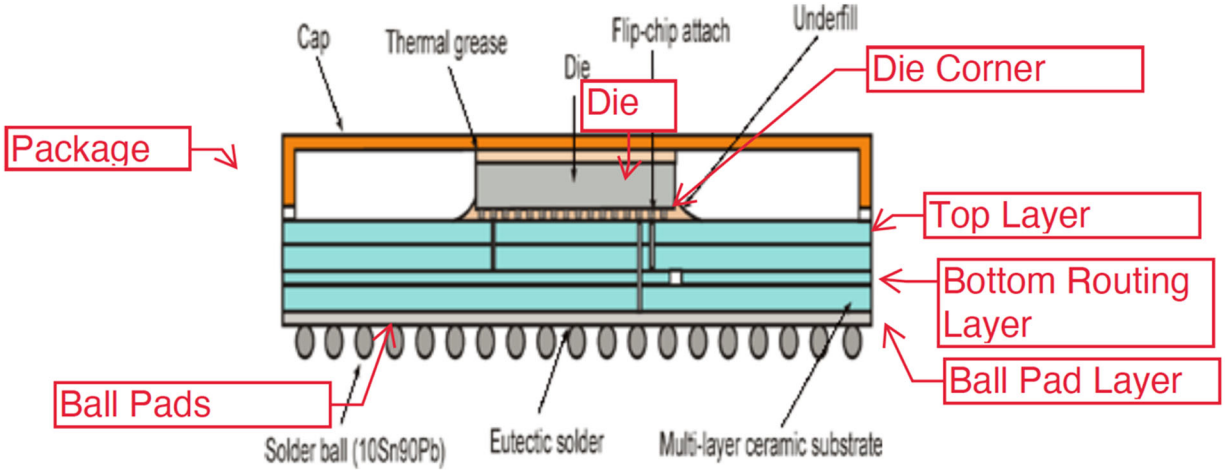
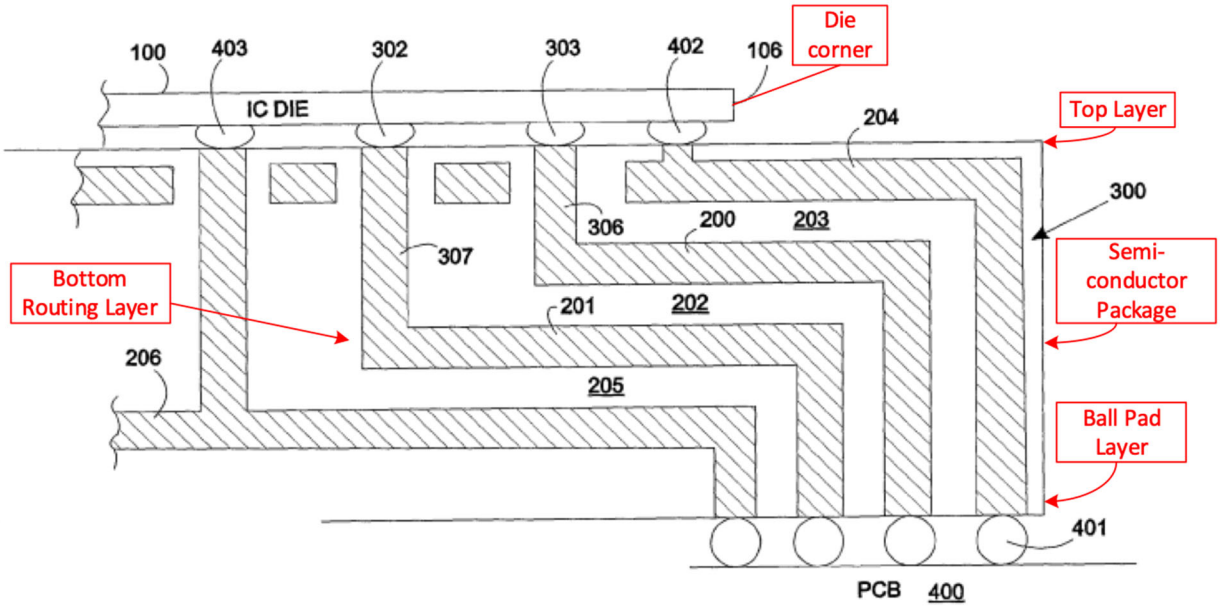


Fig. 3. Ceramic ball grid array (CBGA) [3]

(*Id.*, Fig. 3 annotated)

In the event the Patent Owner argues that Review of BGAs does not disclose this limitation, Devnani also discloses this limitation. (Ex. 1002, ¶0172)

Devnani discloses layers in an IC package (Ex. 1005, ¶0005) and also shows in Figure 4, below, a layer for routing signals (e.g., signal 201) that is lower than other layers of the IC package. (*Id.*, ¶¶0005, 0025; Claim 1) A POSITA would understand that a "bottom routing layer" would be a routing layer beneath another layer of the IC package. (Ex. 1002, ¶0173)



(Ex. 1005, Fig. 4 annotated)

e) "wherein none of the signal traces of the bottom routing layer are located within the area of increased stress defined by the corner of the die."

In my opinion, the combination of Review of BGAs, Devnani and CRTA discloses this claim feature. Figure 3 (below) of Devnani is annotated to show where a die quadrant resides when the IC die is mounted upon the package 300 and to identify the high stress zone of CRTA associated with the corner of the die. Devnani implicitly shows routing traces 201 away from the edges of the die and NOT routing any traces directly under the corner of the die. (Ex. 1002, ¶0174)

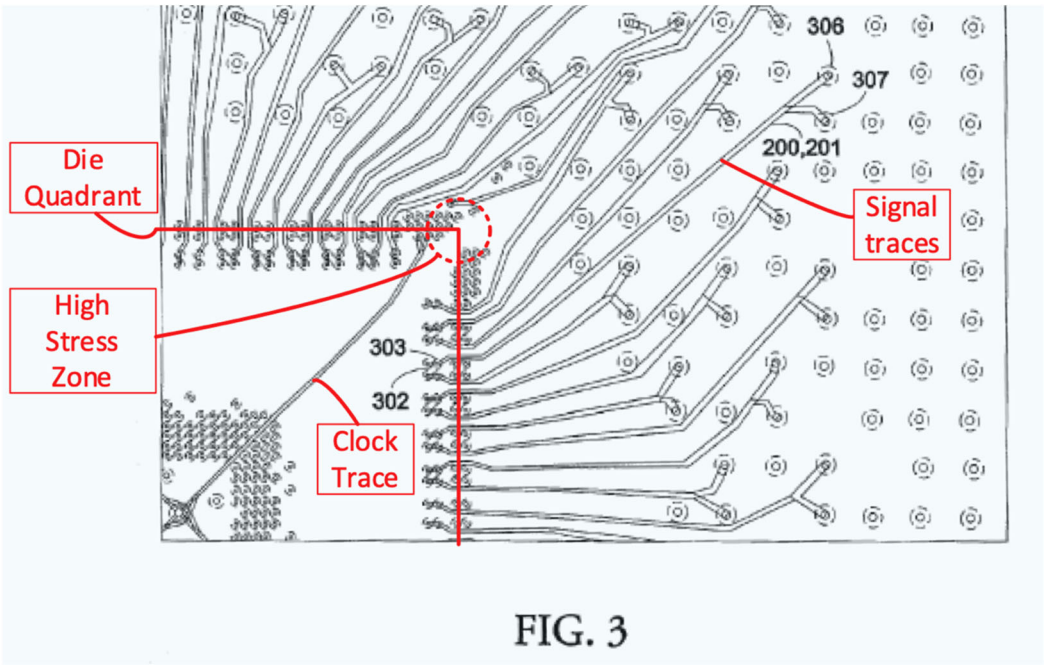


FIG. 3

(Ex. 1005, Fig. 3 annotated)

This inherent feature of Devnani discloses signal traces being routed away from the high stress areas and NOT routing any traces within the highest stress area near the die corner. (Ex. 1002, ¶0175)

A POSITA implementing the semiconductor package of Review of BGAs and Devnani would have good reason to look to CRTA to NOT route any signal traces inside the highest stress area associated with the corner of a die as they both are in the same field of semiconductor packages. Such a POSITA would have been motivated to implement CRTA's highest stress die corner to move Devnani's traces away from such high stress areas to prevent trace cracking with the IC package of Review of BGAs-Devnani. (Ex. 1002, ¶0176)

Further, the modification of Review of BGAs-Devnani with CRTA would have amounted to nothing more than the use of a known technique to improve a similar device, and the results of the modification would have been predictable. This is because at the time of the invention, a POSITA would have had the requisite skill level to readily modify the IC package disclosed by Review of BGAs-Devnani to route traces of a bottom layer based on CRTA teaching a highest stress being in a die corner. Moreover, such modification of Devnani would have been routine for the POSITA as they would be using well-known elements with no change in their respective functions. (Ex. 1002, ¶0177)

X. DISCRETIONARY DENIAL IS NOT APPROPRIATE

A. The Board Should Not Deny Institution Under *Fintiv*

The merits of Petitioner's arguments are compelling and the evidence in support is substantial. That "alone demonstrates that the PTAB should not discretionarily deny institution under *Fintiv*." (Ex. 1012 at 4-5; Memorandum from Director Vidal (dated June 21, 2022)) The six *Fintiv* factors do not justify denying institution.

The **first factor** is neutral because NXP has not yet moved to stay the district court proceeding. *See, e.g., Hulu LLC v. SITO Mobile R&D IP, LLC et al.*, IPR2021-00298, Paper 11 at 10-11 (PTAB May 19, 2021).

The **second factor** weighs against denial. Jury Trial is set for August 20, 2024 (Ex. 1013). However, on June 23, 2023, the co-pending Central District of California lawsuit was reassigned to the Honorable Hernan D. Vera, which more than likely will result in delay of the Jury trial (Ex. 1014). Therefore, it is likely that the trial will occur after the FWD in this IPR, which is expected prior to the end of November 2024. And even if the trial proceeds in August 2024, which it likely will not, the above timing does not tip in favor of denying the petition in this case. *See also, e.g., Apple Inc. v. Aire Tech. Ltd.*, IPR2022-01135, Paper 11 at 5-6 (PTAB Jan. 4, 2023).

The **third factor** weighs strongly against denial. Defendant served its initial infringement contentions on May 17, 2023. Petitioner's diligence in pursuing this petition less than 6 months after receiving the infringement contentions weighs in favor of institution. *Facebook, Inc. v. USC IP P'ship, L.P.*, IPR2021-00033, Paper 13 at 13 (PTAB April 30, 2021) (finding it was reasonable for Petitioner to wait to file the Petition until shortly after receiving infringement contentions).

The **fourth factor** weighs strongly against denial. This Petition challenges claims 1-12 of the '245 patent. Only claims 1, 5, and 6 of the '245 patent are asserted against Petitioner in district court. (Ex. 1015). This IPR petition is thus the only venue in which invalidity challenges of claims 2-4 and 7-12 of the '245 patent will be adjudicated, which promotes system efficiency. See *Fintiv*, Paper 11 at 4.

Accordingly, this factor weighs against denial. *See, e.g., Vudu, Inc. v. Ideahub, Inc.*, IPR2020-01688, Paper 16 at 14-15 (PTAB April 19, 2021).

Regarding the **fifth factor**, the Board should give no weight to the fact that Petitioner and PO are the same parties as in district court. *See Weatherford U.S., L.P., v. Enventure Global Tech., Inc.*, Paper 16 at 11-13 (April 14, 2021).

The **sixth factor** (other circumstances) weighs heavily against denial. Pillai was cited as an anticipatory reference during prosecution of the '245 patent. Applicant made very distinct and specific arguments regarding the shortcomings of Pillai to obtain allowance. Had the Examiner considered the combination of Pillai and AAPA, the '245 patent would likely have not issued—thus the '245 is a bad patent. *See Align Technology, Inc. v. 3Shape A/S*, IPR2020-01087, Paper 15 at 42-43 (PTAB Jan 20, 2021); see also Section IX. There is a significant public interest against "leaving bad patents enforceable," and institution will further that interest. *Thryv, Inc v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020).

B. The Board Should Not Deny Institution Under § 325(d)

Other than Pillai and Tanahashi, none of the prior art cited herein was explicitly considered as prior art by the Patent Office during prosecution of the '245 patent. (Ex. 1001, Cover ("References Cited" section)

Both Pillai and Tanahashi were considered during prosecution. Pillai was considered as the primary reference (anticipatory) during prosecution[3], but inclusion of Pillai as a secondary reference applied in Grounds 2 and 9 does not warrant discretionary denial. Petitioner presents Pillai in combination with multiple differing prior art references including Devnani, Chung, and Celeron. These references combined with Pillai were not previously considered by the Patent Office. Thus, although the Examiner relied on Pillai, the Examiner did not rely on any of the *combinations* of the prior art presented in this Petition with Pillai. *See, e.g.*, *Halliburton Energy Services, Inc. v. US Well Services, LLC*, IPR2021-01036, Paper 12 at 20 (PTAB Jan. 19, 2022) (granting institution when the Examiner cited a reference in a rejection during prosecution, but the Petition set forth "obviousness grounds based on combinations of [the reference] with other prior art not considered by the Examiner").

Although Tanahashi was considered during prosecution, inclusion of Tanahashi as a reference applied in Grounds 6 and 10 does not warrant discretionary denial, because Petitioner presents in a new light as a secondary reference in

[3] "Claims 14-16, 18, 20-22 and 24 were rejected under 35 U.S.C. §102(e) as being anticipated by United States Patent No. 6,680,530 (Pillai)." (Ex. 1004, pp. 269-278, corresponding to issued claims 1-3, 5, 7-10 and 12 of the '245 patent)

combination with references not cited during prosecution of the ’245 patent. The references combined with Tanahashi were not previously considered by the Patent Office.

Additionally, during prosecution, the examiner’s assertion that Tanahashi disclosed the subject matter added by claims 6 and 12[4], which are the subjects of grounds 6 and 10, was not disputed by the Applicant. Instead, the Applicant challenged only the portions of the rejection directed to the independent claims.

Furthermore, Petitioner is not asking the Office to reconsider any arguments, but merely to make determinations consistent with the Examiner’s previous and uncontested finding that Pillai discloses certain features included in the challenged claims and with Applicant’s arguments regarding Pillai. Petitioner also presents additional evidence and analysis in the petition that were not before the Examiner, including the declaration of Dr. Baker. (Ex. 1002)

Under these circumstances, Petitioner respectfully submits that denial of institution under § 325(d) would not be appropriate.

[4] Claims 19 and 25 were re-numbered as claims 6 and 12 upon issuance of the ’245 patent. (Ex. 1004)

XI. CONCLUSION

For the foregoing reasons, Petitioner requests IPR and cancellation of claims 1-12 of the ’245 patent.

Respectfully Submitted,

Dated: November 9, 2023 By: /Bruce E. Garlick/

Bruce E. Garlick (Reg. No. 36,520)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,345,245 contains, as measured by the word processing system used to prepare this paper, 12,576 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully Submitted,

Dated: November 9, 2023

By: /Bruce E. Garlick/
Bruce E. Garlick (Reg. No. 36,520)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on November 9, 2023, I caused a true and correct copy of the Petition for *Inter Partes* Review of U.S. Patent No. 7,345,245 and supporting exhibits filed November 9, 2023 to be served via Priority Mail Express on the Patent Owner at the following correspondence addresses of record:

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Respectfully Submitted,

Dated: November 9, 2023 By: /Bruce E. Garlick/

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