IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

***In re* Patent of:**	Othieno et al.	§	**Docket No.:**	M76459389-091X
		§		
U.S. Patent No.:	7,646,091	§	**Customer No.:**	196553
		§		
Issue Date:	January 12, 2010	§	**Group Art Unit:**	2826
		§		
Filing Date:	April 6, 2006	§	**Examiner:**	--
		§		

Patent Title: SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION

REQUEST FOR *EX PARTE* REEXAMINATION OF U.S. PATENT 7,646,091

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United States Patent and Trademark Office
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TABLE OF CONTENTS

I. INTRODUCTION 1

II. THE ’091 PATENT 3

A. Priority Date of the ’091 Patent 3

B. Overview of the ’091 Patent 3

C. Prosecution History of the ’091 Patent 5

D. Level of Ordinary Skill in the Art 7

III. TECHNICAL REQUIREMENTS FOR *EX PARTE* REEXAMINATION UNDER 37 C.F.R. § 1.510 8

A. 37 C.F.R. § 1.510(b)(1): Statement Pointing Out Each Substantial New Question of Patentability 8

B. 37 C.F.R. § 1.510(b)(2): Identification of Every Claim for Which Reexamination Is Requested 9

C. 37 C.F.R. § 1.510(b)(2): Detailed Explanation of the Pertinency and Manner of Applying the Prior-Art 9

D. 37 C.F.R. § 1.510(b)(3): Copy of Every Patent or Printed Publication Relied upon or Referred to 9

E. 37 C.F.R. § 1.510(b)(4): Copy of the Entire Patent 9

F. 37 C.F.R. § 1.510(b)(5): Certification of Service 9

G. 37 C.F.R. § 1.510(b)(6): Certification by the Third-Party Requester 10

H. 37 C.F.R. § 1.510(a): Fee for Requesting Reexamination 10

I. Broadest Reasonable Interpretation 10

J. Identification of Related Matters 11

IV. THE PRIOR ART 11

A. The Prior Art 11

1. Okabe (Ex. 1005) 11

2. Hashemi (Ex. 1006) 13

3. Kramer (Ex. 1007) 14

4. Miller (Ex. 1008) 15

5. Rozenblit (Ex. 1014) 16

6. Taggart (Ex. 1009) 16

7. High-Speed Digital Design (hereinafter "Digital Design") (Ex. 1010) 17

8. Choi (Ex. 1011) 18

9. Sutardja (Ex. 1012) 19

10. Conn (Ex. 1013) 20

B. Summary of the Grounds Presented 20

V. THE PRIOR ART RAISES A SUBSTANTIAL NEW QUESTION OF PATENTABILITY 22

VI. CLAIM CONSTRUCTION 24

VII. DETAILED EXPLANATION OF UNPATENTABILITY 25

A. Miller in view of Hashemi discloses or suggests all the features of Claim 1 25

1. Claim 1 25

B. Hashemi in view of Okabe and Rozenblit discloses all the features of Claim 1 50

1. Claim 1 50

C. Okabe in combination with AAPA and Rozenblit discloses or suggests all of the features of claims 1 and 12 of the '091 Patent 67

1. Claim 1 67

2. Claim 12 91

D. Okabe in Combination with AAPA, Rozenblit and Sutardja Discloses or Suggests all the features of Claims 2, 5, 6, and 9..................................95

1. Claim 2 95

2. Claim 5 98

3. Claim 6 100

4. Claim 9 102

E. Okabe in Combination with AAPA, Rozenblit, Sutardja and Taggart Discloses or Suggests all the features of Claims 3, 4 and 7......................104

1. Claim 3 104

2. Claim 4 106

3. Claim 7 107

F. Okabe in Combination with Applicant's Admitted Prior Art (AAPA), Rozenblit, Sutardja, and Choi Discloses or Suggests all the features of Claims 8 and 11..111

1. Claim 8 111

2. Claim 11 113

G. Okabe in Combination with AAPA, Rozenblit, Sutardja, Choi, and Digital Design Discloses or Suggests all the features of Claim 10...........116

1. Claim 10 116

H. Okabe in Combination with AAPA, Rozenblit, Kramer and Sutardja Disclose or Suggest all the features of Claim 13 121

1. Claim 13 121

I. Okabe in Combination with AAPA, Rozenblit Conn, Kramer and Sutardja Disclose or Suggest all the features of Claim 14 126

1. Claim 14 126

VIII. THIS REQUEST IS NOT REDUNDANT AND SHOULD NOT BE DENIED UNDER 35 U.S.C. §325(D) 131

IX. CONCLUSION 132

LIST OF EXHIBITS

Ex. 1001	U.S. Patent No. 7,646,091
Ex. 1002	Declaration of R. Jacob Baker, Ph.D., P.E.
Ex. 1003	Curriculum Vitae of R. Jacob Baker, Ph.D., P.E.
Ex. 1004	File History of U.S. Patent No. 7,646,091
Ex. 1005	U.S. Patent No. 7,515,879 to Okabe et al ("Okabe")
Ex. 1006	U.S. Patent No. 6,377,464 to Hashemi et al ("Hashemi")
Ex. 1007	U.S. Patent No. 7,420,286 to Kramer ("Kramer")
Ex. 1008	U.S. Patent No. 6,744,130 to Miller ("Miller")
Ex. 1009	U.S. Patent Publication No. 2006/0001180 to Taggart et al ("Taggart")
Ex. 1010	Johnson, H. W., & Graham, M. (1993). *High Speed Digital Design: A Handbook of Black Magic*; PTR Prentice Hall., IBSN:0-13-395724-1 ("Digital Design")
Ex. 1011	Jinwoo Choi, Sung-Hwan Min, Joong-Ho Kim, Madhavan Swaminathan, Wendemagegnehu (Wendem) Beyene, and Xingchao (Chuck) Yuan, *Modeling and Analysis of Power Distribution Networks for Gigabit Applications*, IEEE Transactions on Mobile Computing, Vol. 2, No. 4, October-December 2003, pages 299-313 ("Choi")
Ex. 1012	U.S. Patent Publication No. 2007/0018292 to Sutardja ("Sutardja")
Ex. 1013	U.S. Patent No. 7,084,487 to Conn ("Conn")
Ex. 1014	U.S. Patent No. 6,658,237 to Rozenblit ("Rozenblit")
Ex. 1015	Patent Owner's Preliminary Response, NXP USA, Inc. v. Bell Semiconductor, LLC, IPR2024-00167, February 20, 2024

I. INTRODUCTION

Pursuant to 35 U.S.C. §§ 302-307 and 37 C.F.R. § 1.510, the undersigned, on behalf of NXP USA, Inc., NXP Semiconductors N.V., NXP B.V., and Freescale Semiconductor Holdings V, Inc. (hereinafter "NXP"), hereby requests *ex parte* reexamination of claims 1-14 (“challenged claims”) of U.S. Patent No. 7,646,091 (“the ’091 Patent”), a copy of which is attached as Ex. 1001. The ’091 Patent was issued on January 12, 2010, to Othieno *et al* and was originally assigned to LSI Logic Corporation and is now assigned to Bell Semiconductor, LLC (“Patent Owner” or “Bell”). The ’091 Patent issued from Application No. 11/399,723, which was filed on April 6, 2006, and has no priority claim.

This Request presents substantial new questions of patentability as to each of the challenged claims. The claims challenged in this Request were the subject of a recent *inter partes* review petition. The present Request raises substantial new questions of patentability, applying prior-art references that were not previously considered during any examination of the ’091 Patent and which clearly disclose elements that the PTAB found were not adequately disclosed in the *inter partes* review petition.

Indeed, the PTAB declined to institute IPR2024-00167 on the basis that the cited references allegedly did not render obvious split ground planes that were independently connected to low speed circuitry and high speed circuitry, because

"high speed" and "low speed" were not explicitly supported by Petitioner's arguments. However, the prior art references raised in this Request confirm that baseband signals were considered low speed and radio frequency (RF) signals were considered high speed circuitry as would have been well known to a person of ordinary skill in the art (POSITA) by the priority date of the '091 Patent (Apr. 6, 2006). The prior art references raised in the Request further raise other substantial new questions of patentability as will be discussed below. This Request includes three new 35 U.S.C. § 103 grounds for unpatentability in view of two new prior art references (Miller and Rozenblit) and in view of Hashemi, Okabe and/or Applicant's Admitted Prior Art (AAPA).

Thus, the prior art presented herein in this Request discloses that separate grounds were well known to separate high speed signals from low speed signals to reduce noise and provide signal isolation in integrated circuit packages and further that certain frequencies (e.g., baseband) were known to be low speed and other frequencies were known to be high speed (e.g., RF).

Because this Request presents new prior art references that have not been previously considered and they raise substantial new questions (SNQ) of patentability, *ex parte* reexamination should be granted and each of the challenged claims should be canceled as unpatentable.

II. THE ’091 PATENT

A. Priority Date of the ’091 Patent

The ’091 Patent was filed April 6, 2006. (Ex. 1001.) Solely for the purpose of this Request, the undersigned Requester assumes that the ’091 Patent is entitled to this filing date. In the IPR Petition related to the ’091 Patent (IPR2024-00167), neither the Petitioner nor the Patent Owner challenged April 6, 2006, as the appropriate priority date for the ’091 Patent for the purposes of that proceeding.

B. Overview of the ’091 Patent

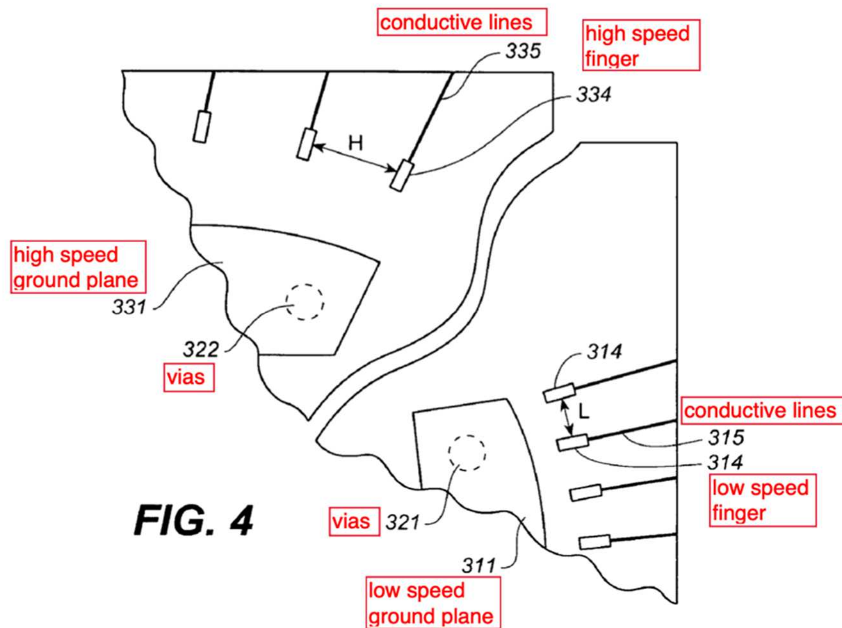
The ’091 Patent discloses a semiconductor integrated circuit (IC) package that includes a substrate and an IC die attached to the substrate. (Ex. 1001, Abstract.)

According to the ’091 Patent, prior art IC “packages generally include[d] a signal ground plane for all IC systems and grounds. When all systems operated at low frequencies or low serial data transfer rates, this situation was not much of a problem.” (*Id.*, 2:6-9.) The ’091 Patent further discloses that when high speed portions and low speed portions of the IC are electrically connected to the same ground plane 111, excessive noise generated by the high speed circuitry interferes with the operation of the low-speed circuitry. (*Id.*, 1:64-2:13; Ex. 1002, ¶¶27, 29-30.)

The ’091 Patent admits that the prior art had already tried to address this interference issue *by using individual pins for separately grounding* each high-speed connection. (Ex. 1001, 2:23-31; Ex. 1002, ¶30.)

Thus, the ’091 Patent purports to solve the interference resulting from having high and low speed circuitry sharing the same ground plane by utilizing a separate ground plane for the high speed circuitry. (Ex. 1001, 2:45-48; Ex. 1002, ¶31.) This is shown below in Figure 4 of the ’091 Patent as high speed ground plane 331 and low speed ground plane 311.

The ’091 Patent also purports to address interconnection crosstalk issues by increasing the spacing (H) between high speed conductive lines. (Ex. 1001, ¶¶33-34) This spacing is shown below in Figure 4 as “H” between high speed fingers 334.



(*Id.*, FIG. 4 (annotated).)

Notably, the ’091 Patent does not disclose *any* physical or otherwise structural difference (e.g., size, materials, shape, etc.) in a ground plane enabled for use with high speed circuitry as opposed to a ground plane enabled for use with low speed

circuitry. The separation of the ground planes and the spacing between interconnects are the purported advancements over the prior art (Ex. 1002, ¶31.)

However, as explained below in Section VII, separate ground planes to reduce interference between signals and spacing between interconnections to reduce cross-talk were all well known in the prior art. (Ex. 1002, ¶¶37-289) Further, the Office when examining the claims, gave no weight to the intended use of a ground plane for use with high speed circuitry nor the intended use of a second ground plane for use with low speed circuitry. (Ex. 1004, pp. 391-392.)

C. Prosecution History of the ’091 Patent

The ’091 Patent issues from U.S. Application No. 11/399,723, which was filed on April 6, 2006. During examination, the Examiner rejected the claims over prior art reference Wu, which taught separate ground nets for two separate power nets disposed on a multi-power IC chip mounted in the package (Ex. 1004, p. 352.)

The Examiner further stated that Wu taught the separate ground returns “can be useful in applications needing high isolation between noisy digital or RF functions, and highly sensitive analog functions, e.g., low noise, broad-band amplifiers and the like.” (Ex. 1004, p. 352.)

The Examiner further stated “it is well known in the art for variables such as speeds, numbers of signals, the timing of signals, dielectric constants of dielectric

layer isolating contacts, etc., are used to adjust the desired impedances/reduce cross-talk performance between the contacts." (Ex. 1004, p. 352.)

Throughout prosecution, the Examiner did not give any patentable weight to the function/intended use portions of claim 1. (*See generally* Ex. 1004.)

For example, the Examiner stated "Note that a recitation of the function/intended use such as '**the first ground plane is configured for electrical connection with low speed electronic circuitry** or **the second ground plane is configured for electrical connection with high speed electronic circuitry**' of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, and then it meets the claim. >While features of an apparatus may be recited either structurally or functionally, claims< directed to >an< apparatus must be distinguished from the prior art in terms of structure rather than function. >*In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997). See also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< *In re Danly*, 263 F.2d 844,847, 120 USPQ 528,531 (CCPA 1959). A claim containing a 'recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus' if the prior art apparatus teaches all the <u>structural</u> limitations of the claim. *Ex parte*

Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). See MPEP § 2114." (Ex. 1004, pp. 391-392 [emphasis added].)

The claims were deemed allegedly allowable because "the prior art does not provide a semiconductor integrated circuit (IC) which comprises: a fourth ground plane that is spatially separated and electrically isolated from the third ground plane and at least one reference plane associated with each layer of the substrate and the ground planes included thereon." (Ex. 1004, p. 304.)

But these aspects of claim 1 (as well as the rest of the Challenged Claims) were not new and are taught by the prior art discussed herein.

D. Level of Ordinary Skill in the Art

A POSITA at the time of the '091 Patent would have had a bachelor's degree in a field relating to the semiconductor manufacturing process like materials science, physics, electrical engineering, or other related subjects, and at least two to three years of experience with fabrication and packaging of integrated circuits. More education can supplement practical experience and vice versa. Depending on the engineering background and level of education of a person, it would have taken a few years for the person to become familiar with the problems encountered in the art

and to become familiar with the prior and current solutions to those problems. (Ex. 1002, ¶20-21.)[1]

III. TECHNICAL REQUIREMENTS FOR *EX PARTE* REEXAMINATION UNDER 37 C.F.R. § 1.510

This *ex parte* reexamination request satisfies each requirement for *ex parte* reexamination of the ’091 for the reasons set forth below.

A. 37 C.F.R. § 1.510(b)(1): Statement Pointing Out Each Substantial New Question of Patentability

The present *ex parte* reexamination request raises substantial new questions of patentability, applying prior-art references that were not previously considered during any examination of the ’091 Patent and which clearly disclose elements that the PTAB found were not adequately explained in the *inter partes* review petition. A statement pointing out each new SNQ based on the cited patents and printed publications in accordance with 37 C.F.R. § 1.510(b)(1) is provided below in Section V.

[1] Petitioner submits the declaration of Dr. Jacob Baker (Ex. 1002), an expert in the field of the ’091 patent. (*See generally* Ex. 1003.)

B. 37 C.F.R. § 1.510(b)(2): Identification of Every Claim for Which Reexamination Is Requested

Reexamination is requested for Claims 1-14 of the '091 Patent in view of the prior-art references discussed below.

C. 37 C.F.R. § 1.510(b)(2): Detailed Explanation of the Pertinency and Manner of Applying the Prior-Art

A detailed explanation of the pertinency and matter of applying the prior art to every claim for which reexamination is requested in accordance with 37 C.F.R. §1.510(b)(2) is provided below in Section VII. The material and analysis in the Request are fully supported by the expert testimony of Dr. Baker.

D. 37 C.F.R. § 1.510(b)(3): Copy of Every Patent or Printed Publication Relied upon or Referred to

Requester has provided a copy of every patent or printed publication relied upon or referred to in this *ex parte* reexamination request as Exhibits 1001-1016. For convenience, the cited patents and printed publications are listed on a Form PTO-1449, which is attached.

E. 37 C.F.R. § 1.510(b)(4): Copy of the Entire Patent

Third-Party Requester has provided a full copy of the '091 Patent, including its Certificate of Correction as Ex. 1001 in accordance with 37 C.F.R. §1.510(b)(4).

F. 37 C.F.R. § 1.510(b)(5): Certification of Service

In accordance with 37 C.F.R. § l.510(b)(5), Third-Party Requester has provided below in the last page of this Request a certification that a copy of the

request has been served in its entirety on the Patent Owner at the address as provided for in § 1.33(c). The name and address of the party served has been indicated.

G. 37 C.F.R. § 1.510(b)(6): Certification by the Third-Party Requester

In accordance with 37 C.F.R. § l.510(b)(6), Third Party Requester certifies that the statutory estoppel provisions of 35 U.S.C. § 315(e)(l) or 35 U.S.C. § 325(e)(l) do not prohibit Third Party Requester from filing this *ex parte* reexamination request.

H. 37 C.F.R. § 1.510(a): Fee for Requesting Reexamination

All fees set forth in 37 C.F.R. §1.510(a) have been paid simultaneously with filing this request. Authorization to charge any underpayment of fees to Deposit Account No. 50-2126.

I. Broadest Reasonable Interpretation

In reexamination, the U.S. Patent and Trademark Office applies the broadest reasonable interpretation (BRI) when construing claim terms. *In re Yamamoto*, 740 F.2d 1569, 1571 (Fed. Cir. 1984). When applying the BRI, words of the claim must be given their plain meaning, unless such meaning is inconsistent with the specification. *In re Zietz*, 893 F.2d 319,321 (Fed. Cir. 1989). The presumption that a term is given its ordinary and customary meaning may be rebutted by the Applicant by clearly setting forth a different definition of the term in the specification (*i.e.*, by acting as a lexicographer). *In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997).

J. Identification of Related Matters

The ’091 Patent is at issue in *Bell Semiconductor, LLC v. NXP USA, Inc. et al* Case No. 8:22-cv-02133-HDV-ADS, pending in Federal District Court in the Central District of California. On May 13, 2024, the PTAB declined to institute IPR2024-00167 regarding the ’091 Patent as discussed above. The ’091 Patent is also at issue in *Bell Semiconductor, LLC v. Texas Instruments, Incorporated.* Case No. 4:23-cv-069S, pending in Federal District Court in the Eastern District of Texas. Because this patent is involved in concurrent litigation, the USPTO should accord it priority. MPEP § 2261 (“Any cases involved in litigation, whether they are reexamination proceedings or reissue applications, will have priority over all other cases.”).

IV. THE PRIOR ART

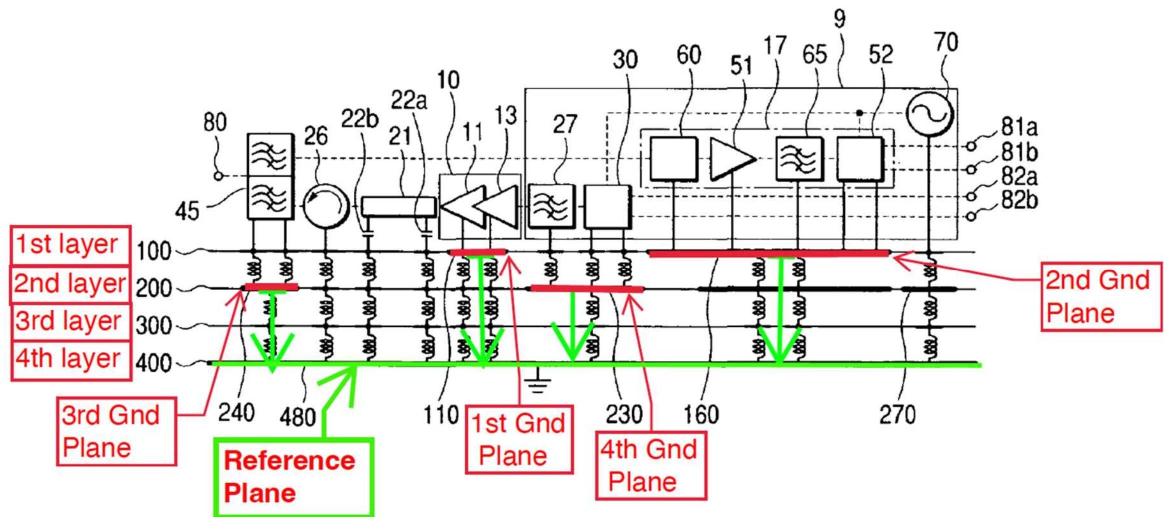
A. The Prior Art

1. Okabe (Ex. 1005)

Okabe is analogous to the ’091 Patent as they are both in the same field of integrated circuit packages. Okabe discloses a radio frequency (RF) module comprising a module substrate that has reduced interference between its electronic circuit blocks, where the electronic circuits operate at different speeds (e.g., frequencies of 3.8 megahertz (MHz), 1.9 gigahertz (GHz), 2.1 GHz, 200 kilohertz (kHz)). (Ex. 1005, 2:66-3:3, 3:10-18, 7:36-43, 14:5-13.)

Okabe discloses separate ground planes that are separated and electronically isolated in order to reduce interference. (*Id.*, 5:39-46; Abstract.) Okabe also discloses it was well known in the art to separate ground planes to reduce interference between a first and second active circuit chip on a single interconnect substrate. (*Id.*, 2:24-41.) Okabe discloses that the separate ground planes can be extended to individual circuits. (Ex. 1005, 2:42-49.)

Okabe further discloses in Figure 14, shown below, a substrate that includes four layers 100-400, where a first layer of the substrate includes separate and electrically isolated first and second ground planes and a second layer of the substrate includes separate and electrically isolated third and fourth ground planes. (*Id.*, 14:26-15:3.)



(*Id.*, FIG. 14 (annotated).)

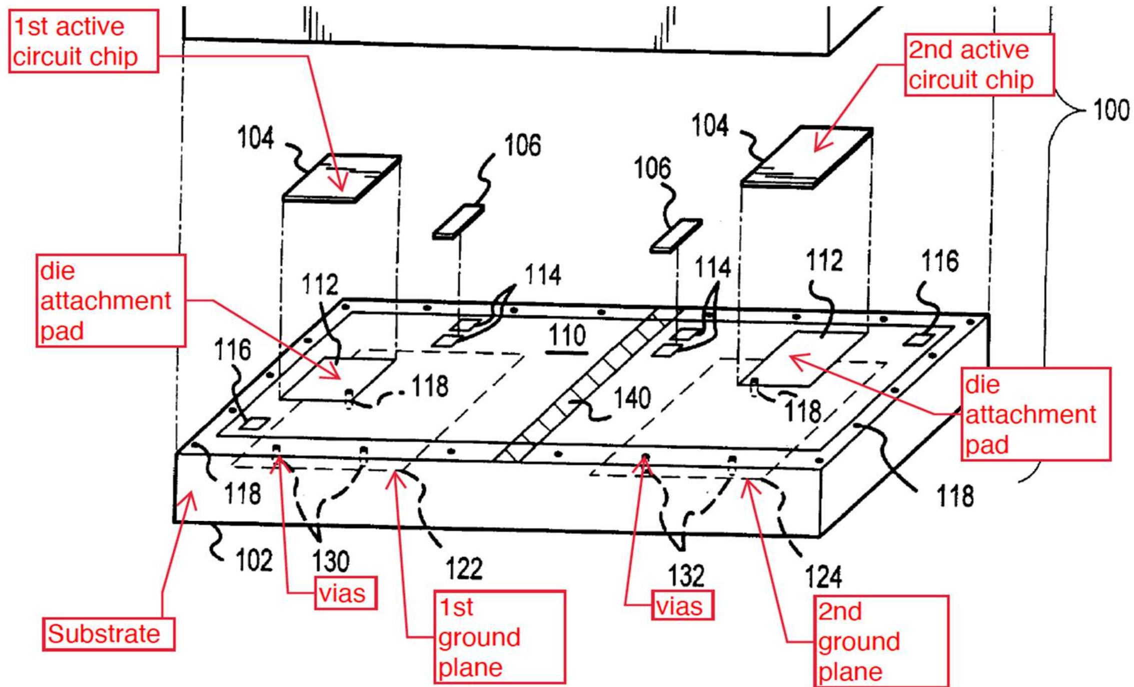
Okabe further discloses that "these separate ground planes *are electrically isolated from each other* as they are and function as the ground only by termination to the common ground plane 480." (*Id.*, 14:22-25 (emphasis added).)

2. Hashemi (Ex. 1006)

Hashemi is analogous to the '091 Patent as they are both in the same field of integrated circuit packages. Hashemi discloses "a multiple chip module (MCM) for use with baseband, RF or IF applications" that includes a number of active circuit chips mounted on a substrate. (Ex. 1006, Abstract.) Hashemi teaches the MCM is capable of concurrent operation at different speeds, with examples ranging from 45 Megahertz (MHz) to 2.4 Gigahertz (GHz). (*Id.*; Ex. 1006, 3:5-10, 43-51.)

Hashemi teaches that the MCM can include physically separated split ground planes to achieve electronic isolation between different active circuit chips (e.g., RF and baseband (*i.e.*, high and low speed)) and the physically separated or split ground planes can reside at different metal layers or at the same metal layer. (Ex. 1006, Abstract, Claims 15-16, 7:9-26.)

Hashemi teaches in Figure 1, shown below, a first ground plane 122 being used for a first active chip 104, and a second ground plane 124 being used for a second active chip 104, which reduces unwanted interference (e.g., noise). (Ex. 1006, 7:16-21.)

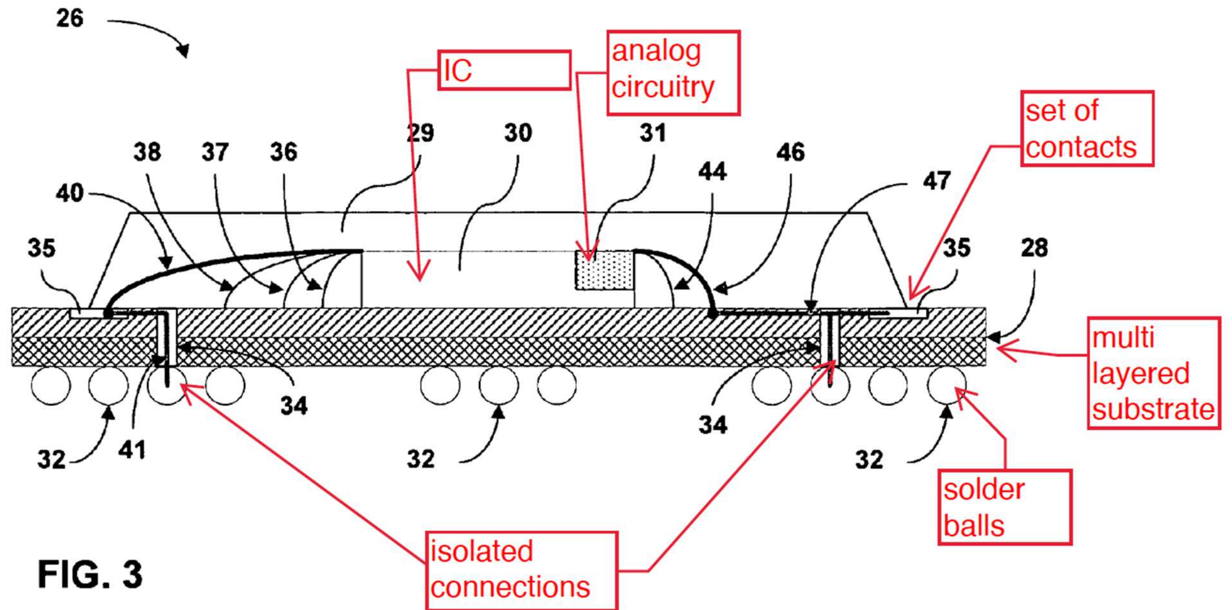


(Ex. 1006, FIG. 1 (annotated).)

3. Kramer (Ex. 1007)

Kramer is analogous to the '091 Patent as they are both in the same field of integrated circuit packages. Kramer discloses isolating grounds for separate portions of an integrated circuit. (Ex. 1007, 5:38-41.) As shown in Figure 3 below, Kramer discloses an integrated circuit 30 attached to BGA package 28 includes an analog circuit 31. Kramer states that "IC 30 comprises an analog circuit 31, such as a serial

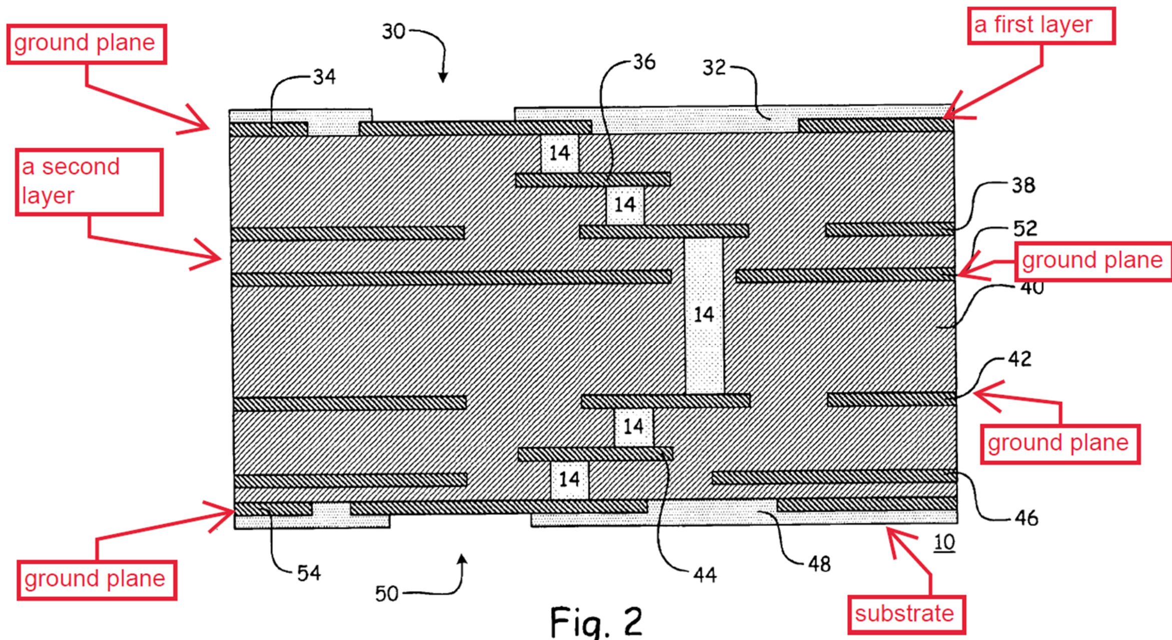
transceiver, that requires isolated power and ground connections to reduce noise on analog circuit 31 from other circuits of IC 30." (*Id.*)



(Ex. 1007, FIG. 3 (annotated).)

4. Miller (Ex. 1008)

Miller discloses multiple ground planes on different layers of a substrate that is cross-talk tolerant to very high speed core devices. Miller also discloses the substrate includes one or more references layers (power or ground) associated with each layer of the substrate.



(Ex. 1008, FIG. 2 (annotated).)

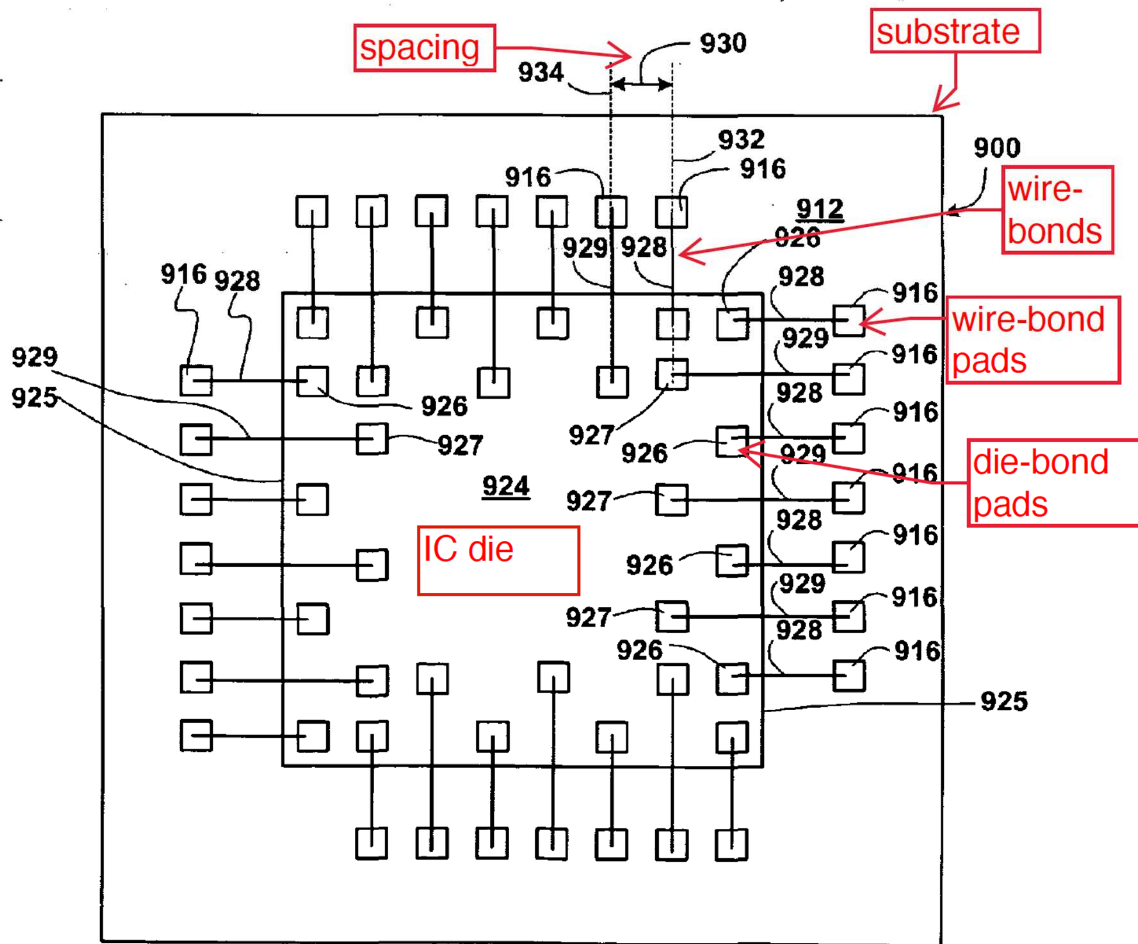
5. Rozenblit (Ex. 1014)

Rozenblit discloses it was well known that baseband was considered low frequency and RF was considered high frequency. (Ex. 1014, 15:2-7; 21:44-51; 5:46-54.) Rozenblit further discloses it was known to shield, physically separate, and otherwise isolate RF signals from lower speed signals to reduce interference, and thus Rozenblit set out to develop a multi-band transceiver *(Id.*, 5:46-62.)

6. Taggart (Ex. 1009)

Taggart is analogous to the ’091 Patent as they are both in the same field of integrated circuit packages. Taggart discloses a spacing or “pitch” for aligning bond fingers with die pads in as shown below in Figure 9. (Ex. 1009, ¶27.) Taggart discloses specific values for the spacing ranging from “about 10 um [micrometers]

to about 200 um", with specific examples of the pitch being 135 um and 200 um. (*Id.*, ¶27.)



(Ex. 1009, FIG. 9, (annotated).)

7. High-Speed Digital Design (hereinafter "Digital Design") (Ex. 1010)

Digital Design discloses design guidelines for various circuits to control crosstalk for high and low speed signals by determining how far to separate traces. (Ex. 1010, p. 189.) Digital Design shows in Figure 5.4, shown below, that crosstalk

for signal traces is based on in part on the distance, D, between signal traces (Ex. 1010, p. 192.). As one example, Digital Design discloses that "more closely spaced traces yield more crosstalk". (Ex. 1010, p. 215.)

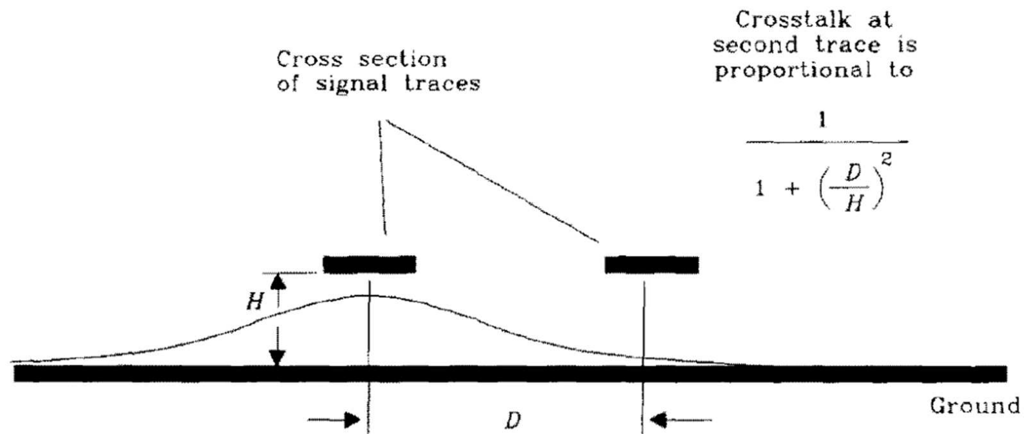


Figure 5.4 Cross section of two traces showing crosstalk.

(*Id.*, FIG 5.4)

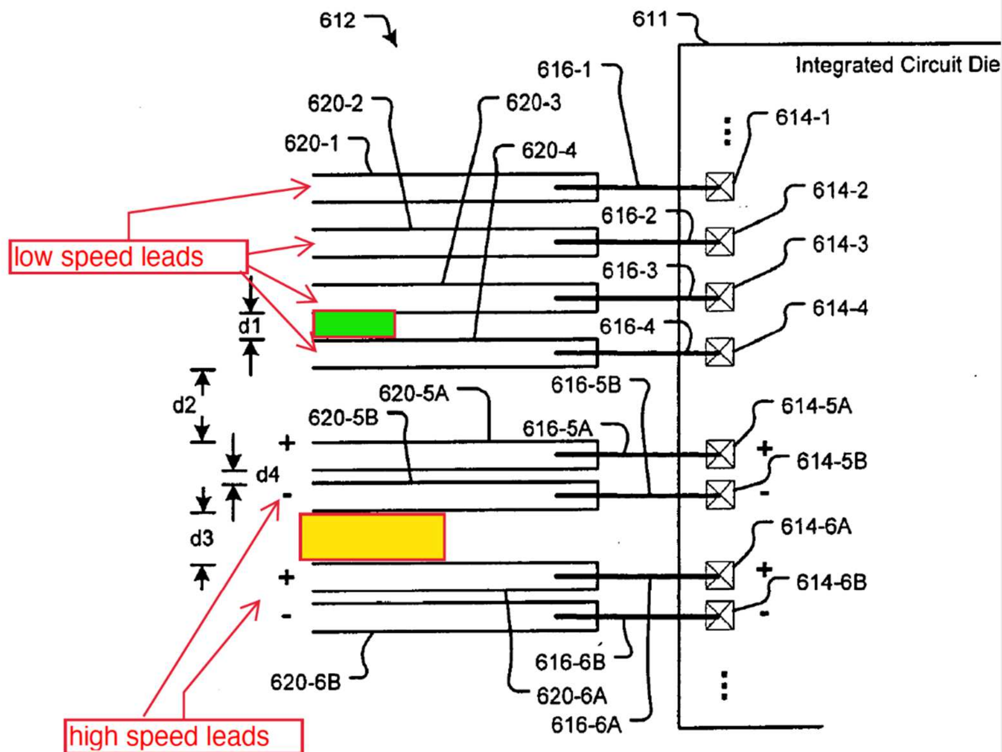
8. Choi (Ex. 1011)

Choi teaches in Figure 6, shown below, a multi-layered PCB that has low-speed interconnects on layer 1 and high-speed interconnects on layer 6. (Ex. 1011, p. 304.) Choi further teaches that the low-speed signal transmission lines have characteristic impedances designed for 50 Ω (Ohms) and the high-speed signal transmission lines are designed to provide 100 Ohm differential impedance. (*Id.*)

(Ex. 1011, FIG. 6.)

9. Sutardja (Ex. 1012)

Sutardja teaches in Figure 10A, shown below, that the spacing between the low speed leads (d1, annotated in green) is different from the spacing between the pairs of high speed leads (d4, annotated in yellow), and further that the spacing (d1, d2, d3, and d4) "may be irregular to increase or decrease coupling." (Ex. 1012, ¶0139.)



(Ex. 1012, FIG. 10A, (annotated).)

10. Conn (Ex. 1013)

Conn discloses a stacked die arrangement for different IC die. (Ex. 1013, Abstract.) In an example, one die can be operable at frequencies much higher than another die. (*Id.*, 6:40-50.)

B. Summary of the Grounds Presented

<u>Ground 1</u>: Claim 1 is unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Miller (Ex. 1008) and in view of Hashemi (Ex. 1006).

<u>Ground 2</u>: Claim 1 is unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Hashemi (Ex. 1006) and in view of Okabe (Ex. 1005) and Rozenblit (Ex. 1014).

<u>Ground 3</u>: Claims 1 and 12 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Okabe (Ex. 1005) in view of AAPA from within the '091 Patent (Ex. 1001) and Rozenblit (Ex. 1014).

<u>Ground 4</u>: Claims 2, 5, 6, and 9 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Okabe, AAPA, Rozenblit, and Sutardja (Ex. 1012).

<u>Ground 5</u>: Claims 3, 4, and 7 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Okabe, AAPA, Rozenblit, Sutardja, and Taggart (Ex. 1009).

<u>Ground 6</u>: Claims 8 and 11 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Okabe, AAPA, Rozenblit, Sutardja, and Choi (Ex. 1011).

<u>Ground 7</u>: Claim 10 is unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Okabe, AAPA, Rozenblit, Sutardja, Choi, and Digital Design (Ex. 1010).

<u>Ground 8</u>: Claim 13 is unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Okabe, in view of AAPA, Rozenblit, Kramer (Ex. 1007), and Sutardja.

<u>Ground 9</u>: Claim 14 is unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Okabe, AAPA, Rozenblit, Conn (Ex. 1013), Kramer, and Sutardja.

None of the above references were considered by the Examiner during prosecution.

V. THE PRIOR ART RAISES A SUBSTANTIAL NEW QUESTION OF PATENTABILITY

This Request presents substantial new questions of patentability as to each of the challenged claims. The claims challenged in this Request were the subject of a recent *inter partes* review petition, IPR2024-00167, that the Board declined to institute review based on a perceived lack of disclosure of high and low speed circuitry being connected to separate ground planes. (Ex. 1004, pages 20-21.) While the Third-Party Requester disagrees with the Board's conclusion, the present Request raises substantial new questions of patentability regarding this element – low speed signals being connected to a separate ground plane than high speed signals, and raises other substantial new questions of patentability.

For example, Rozenblit raises a substantial new question of patentability because Rozenblit discloses that RF signals were known to be defined as "high frequency" and baseband signals were known to be "low frequency."

Miller raises a substantial new question of patentability because Miller discloses the allegedly allowable features of claim 1 indicated during the prosecution and was not considered during prosecution. Specifically, Miller discloses multiple ground planes and a reference plane, which was stated by the Examiner in the Notice of Allowability as allegedly novel over the prior art.

Okabe raises a SNQ of patentability because Okabe discloses the allegedly allowable features of claim 1 indicated during the prosecution and was not

considered during prosecution. Specifically, Okabe teaches a second layer with third and fourth ground planes that are electrically isolated and spatially separated on the second layer, and teaches a reference plane, which was cited by the Examiner in the Notice of Allowability as allegedly novel over the prior art.

Hashemi raises a SNQ of patentability because Hashemi teaches split ground planes that are electrically isolated and spatially separated on a layer to reduce interference from high speed (RF) signals.

Further, the combinations of prior-art references presented below were not previously considered by the PTAB in IPR2024-00167, nor by the Examiner during the original examination of the ’091 Patent. In particular, references Hashemi, Okabe, Miller, AAPA, Conn, Kramer, Taggart, Choi, Sutardja, Digital Design, and Rozenblit, were not made of record during prosecution of the ’091 Patent and raise further SNQs as laid out in the Grounds below.

As detailed below, each of the prior-art references and/or combinations applied in this Request teaches separate ground planes for signals that could cause interference to other signals, like high and low speed signals. Each of the grounds presented below provides noncumulative technological teachings that were not previously considered and discussed on the record during prosecution of the application (or at the PTAB) that resulted in the patent for which reexamination is requested.

Further, as detailed below, each of the prior-art references and/or combinations applied in this Request teach separate ground planes that "**enable**" or are "**configured for**" electrical connection with low speed circuitry and high speed circuitry. Even though the Examiner did not give weight to these "functional" uses of high and low speed in the apparatus claim throughout prosecution (*See generally* Ex. 1004), the prior art renders these functional uses obvious as shown below.

Because this Request presents new grounds that have not previously been substantively considered in relation to the claims, *ex parte* reexamination should be granted and each of the challenged claims should be cancelled as unpatentable.

VI. CLAIM CONSTRUCTION

The '091 Patent is not expired. Thus, this Request analyzes the Challenged Claims according to their broadest reasonable interpretation in light of the specification. MPEP 2258 § I.G. For purposes of this Request, all terms should be interpreted in accordance with their broadest reasonable interpretation and a specific construction is not necessary for any claim term. No express construction is necessary to show the unpatentability of the claims. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (construing terms "only to the extent necessary to resolve the controversy"); MPEP 2111.01.

VII. DETAILED EXPLANATION OF UNPATENTABILITY

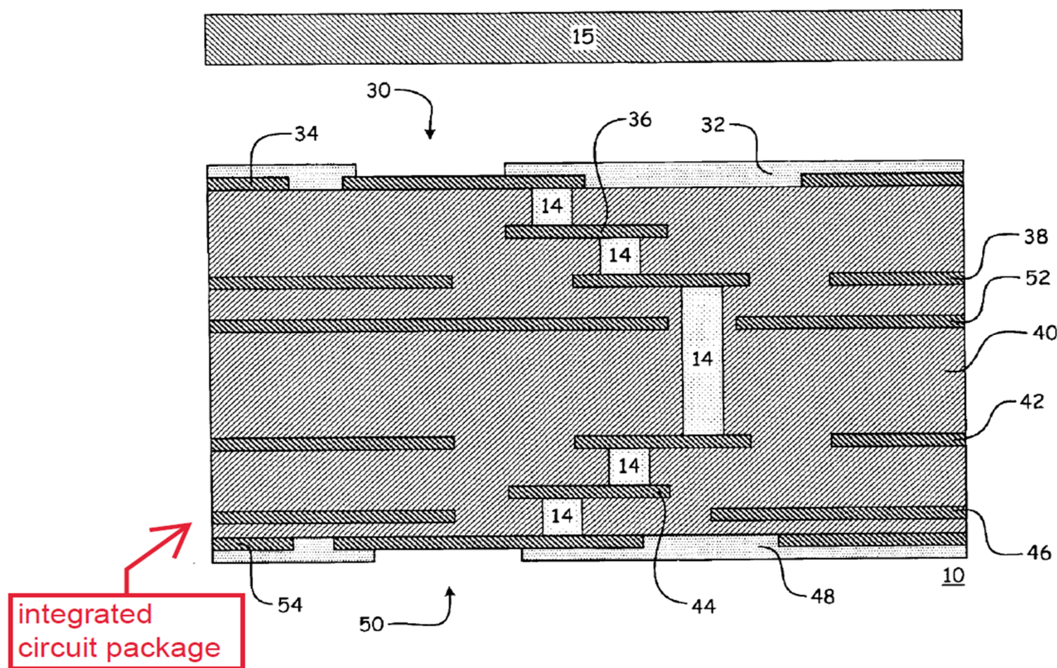
A. Miller in view of Hashemi discloses or suggests all the features of Claim 1

The combination of Miller and Hashemi discloses all of the features of claim 1 of the ’091 Patent.

1. Claim 1

a) “A semiconductor integrated circuit (IC) package which comprises:”

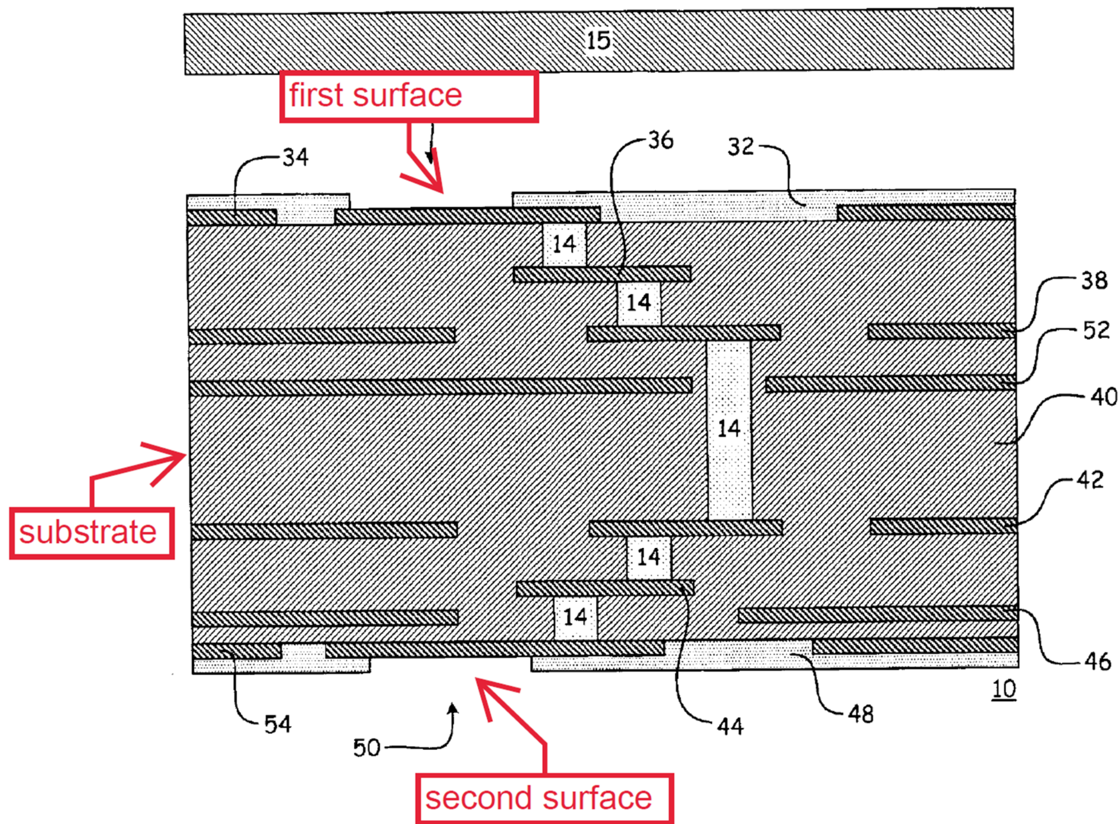
Miller discloses or at least renders obvious limitation (1a). (Ex. 1002, ¶37.) Miller discloses in Figure 2, shown below, “a cross sectional view of a portion of a packaged integrated circuit, including an integrated circuit 15 and a package substrate 10.” (Ex. 1008, 4:55-58.) (Ex. 1002, ¶38.)



(Ex. 1008, FIG. 2 (annotated).)

b) “a substrate having a first surface and a second surface wherein;”

Miller discloses or at least renders obvious limitation (1b). As shown in Figure 2 below, substrate 10 has a first “top surface” and a second “lower” surface. (Ex. 1008, 4:3-12; 5:47-53.) (Ex. 1002, ¶39.)

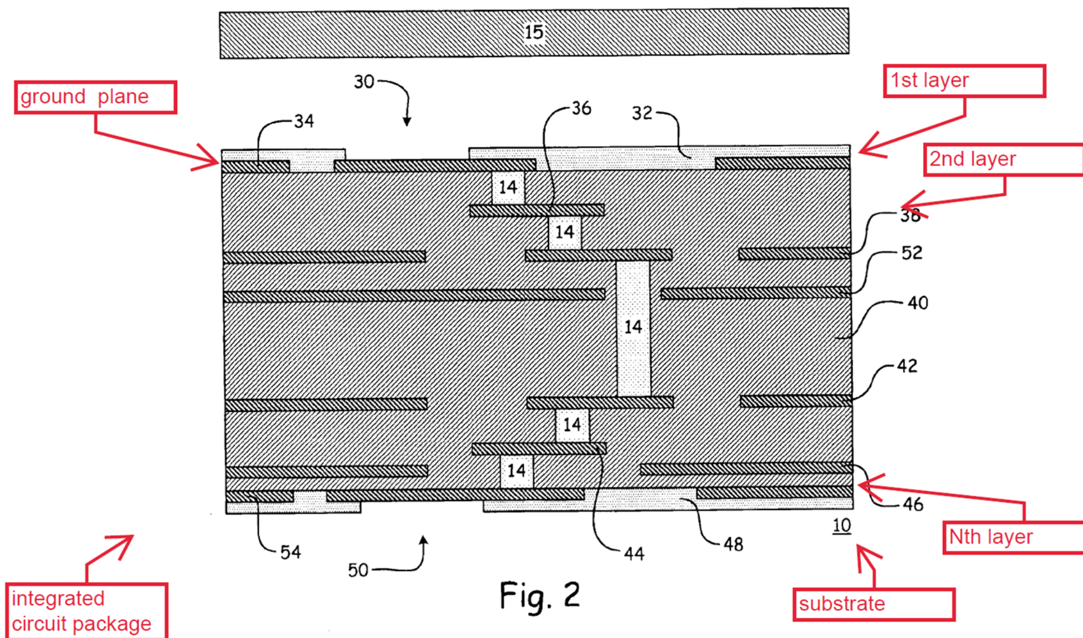


(*Id*., FIG. 2 (annotated).)

c) “a first layer of the substrate includes,”

Miller discloses or at least renders obvious limitation (1c). Miller discloses “[a]s used herein, references to layers being ‘upper’ layers or ‘above’ another layer have reference to layers that are closer to the integrated circuit 15 side of the package substrate 10, while references to layers being ‘lower’ layers or ‘below’ another layer

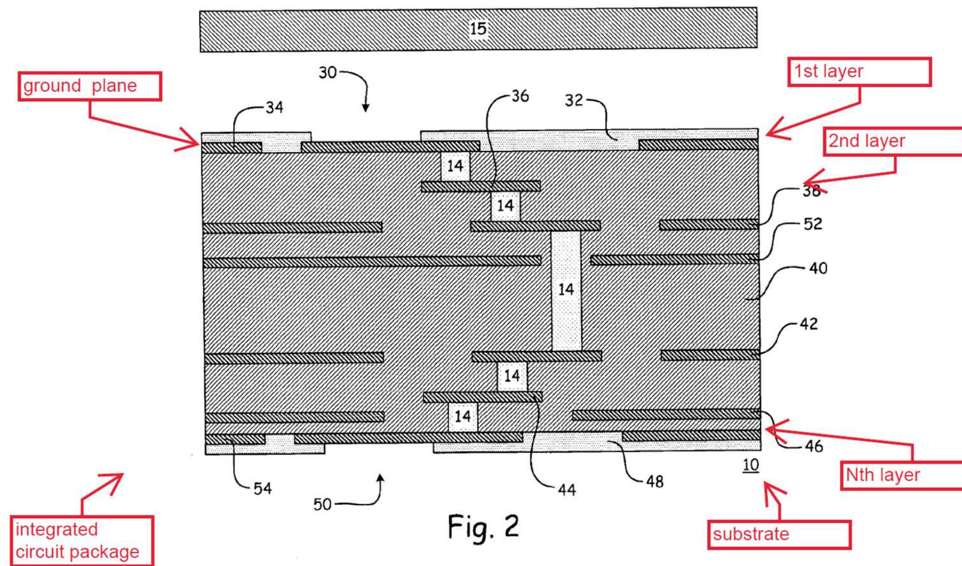
have reference to layers that are farther from the integrated circuit 15 side of the package substrate 10." (Ex. 1008, 4:63-5:2.) Miller also shows these layers, including a first layer, in Figure 2, shown below. (Ex. 1002, ¶40.)



(Ex. 1008, FIG. 2 (annotated).)

d) "a first ground plane enabling electrical connection with low speed electronic circuitry, and"

Miller and Hashemi disclose or at least render limitation (1d) obvious. Miller discloses a first ground plane 34 on a first layer of a substrate 10 as shown below in Figure 2. (Ex. 1002, ¶41.)



(Ex. 1008, FIG. 2 (annotated).)

Hashemi shows in Figure 1 below, a multichip module (MCM) 100 that includes a substrate 102 that includes *a first ground plane* 122 connected to a first active chip 104. Hashemi further discloses "*split ground planes on the same* or different metal *layers* of a substrate are preferably utilized *to obtain RF isolation between a plurality of active circuit chips and/or between different functional sections* on a single active circuit chip. As shown in FIG. 1, MCM 100 may include two functionally distinct portions (each portion being associated with one of the two active chips 104) contained on a single substrate 102. To reduce the amount of unwanted RF interference between the two portions, MCM 100 preferably includes *a first ground plane 122 and a separate second ground plane 124*. In the context of

FIG. 1, first and second ground planes 122 and 124 are formed upon the same internal metal layer." (Ex. 1006, 7:9-21 (emphasis added).) (Ex. 1002, ¶42.)

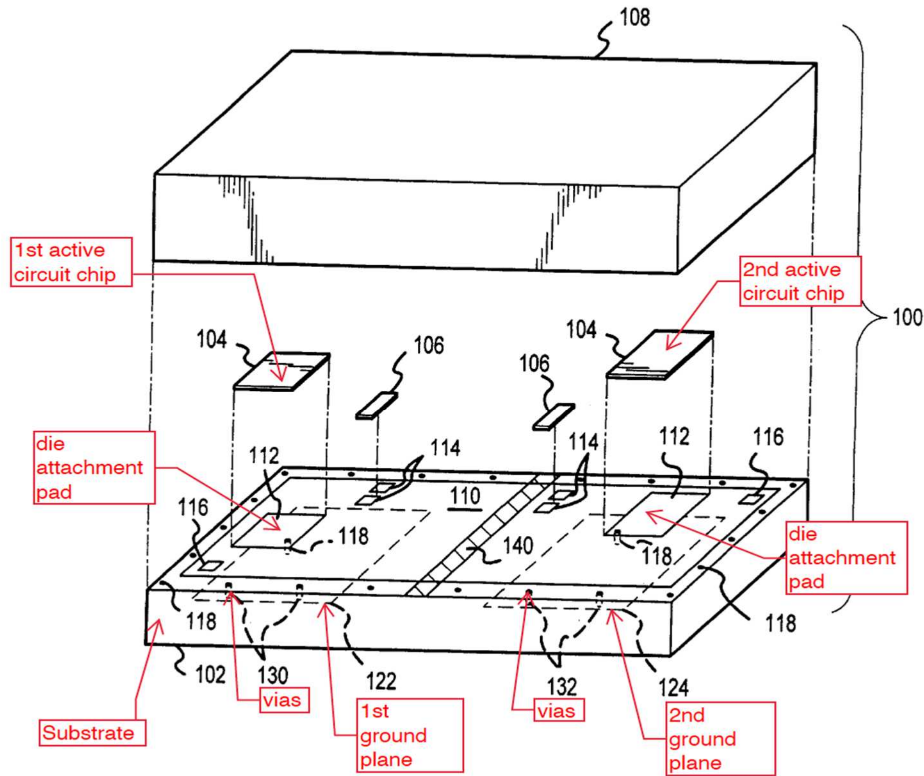


FIG.1

(Ex. 1006, FIG. 1 (annotated).)

Hashemi further teaches that "MCM 100 may be integrated to include, e.g., *a 45 MHz baseband section*." (*Id.*, 3:44-48, (emphasis added).) Thus, Hashemi teaches a first ground plane (ground plane 122), and that the first ground plane enables connection with low speed circuitry (e.g., a 45MHz baseband section). (Ex. 1002, ¶43.)

A POSITA would have understood that the baseband section would be "low speed circuitry." Further, Hashemi discloses that the baseband section is 45MHz and

the RF section is above 800MHz (Ex. 1006, 1:38-44), which a POSITA would have understood meant the baseband section was low speed. In fact, Patent Owner admits that baseband components are understood by a POSITA to be low speed circuitry and RF components are understood to be high speed circuitry. (Ex. 1015, pg. 23.) (Ex. 1002, ¶44.)

Notably, the ’091 Patent does not claim or disclose any structural difference from a typical ground plane for “enabling electrical connection with low speed circuitry.” In fact, the Examiner in prosecution of the ’091 Patent gave **no** weight to this limitation. (Ex. 1002, ¶45.)

For example, the Examiner stated “a recitation of the function/intended use such as ‘the first ground plane is configured for electrical connection with low speed electronic circuitry or the second ground plane is configured for electrical connection with high speed electronic circuitry’ of the claimed invention *must result in a structural difference between the claimed invention and the prior art* in order *to patentably distinguish the claimed invention* from the prior art. If the prior art structure is capable of performing the intended use, and then it meets the claim.” (Ex. 1004, pp 391-392 (Emphasis added).) (Ex. 1002, ¶46.)

The MPEP states in part in §2114:

> **“II. MANNER OF OPERATING THE DEVICE DOES NOT DIFFERENTIATE APPARATUS CLAIM FROM THE PRIOR ART**

"[A]pparatus claims cover what a device *is,* not what a device *does*." *Hewlett-Packard Co. v. Bausch & Lomb Inc.,* 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original). A claim containing a "recitation with respect to the manner in which **a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim**. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987) (The preamble of claim 1 recited that the apparatus was "for mixing flowing developer material" and the body of the claim recited "means for mixing ..., said mixing means being stationary and completely submerged in the developer material." The claim was rejected over a reference which taught all the structural limitations of the claim for the intended use of mixing flowing developer. However, the mixer was only partially submerged in the developer material. The Board held that the amount of submersion is immaterial to the structure of the mixer and thus the claim was properly rejected.)." (emphasis added)

As such, Hashemi and Miller teach structural components for all the limitations of claim 1 and render the claims obvious regardless of any intended use recitation. (Ex. 1002, ¶47.)

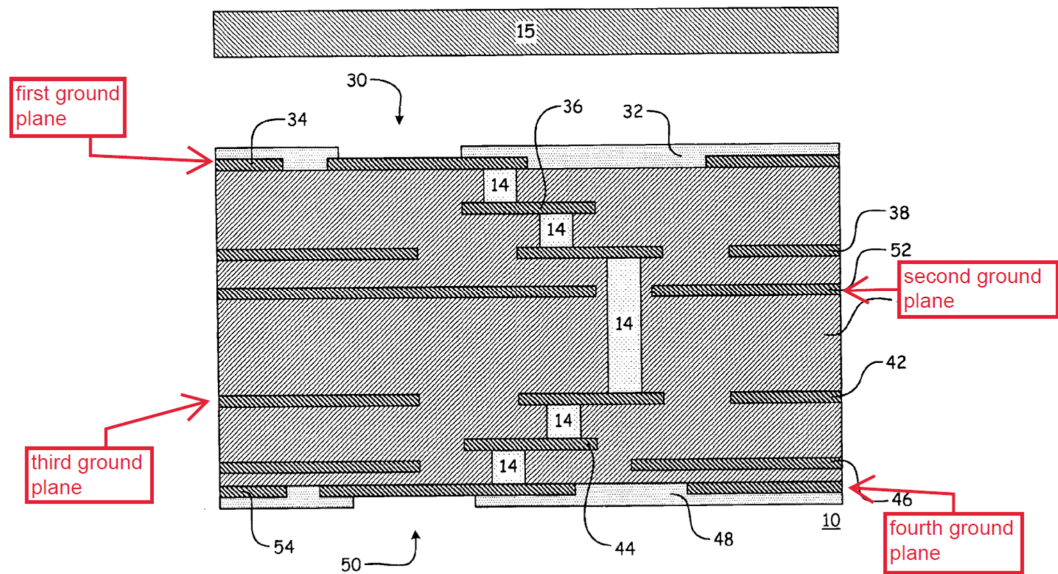
Based on the foregoing, a POSITA would have found it obvious that Hashemi and Miller's ground planes were capable of performing the intended use of being configured for electrical connection with circuitry. (Ex. 1002, ¶48.)

This is further evidenced by Hashemi, who explicitly discloses that a first ground plane is configured for electrical connection with baseband section (low speed circuitry) and a second ground plane is configured for electrical connection with an RF section (high speed circuitry). As such, any ground plane would render this limitation obvious. However, because the combination of Miller and Hashemi explicitly discloses this limitation, this limitation would be obvious to a POSITA. (Ex. 1002, ¶49.)

e) "a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane enabling electrical connection with high speed electronic circuitry;"

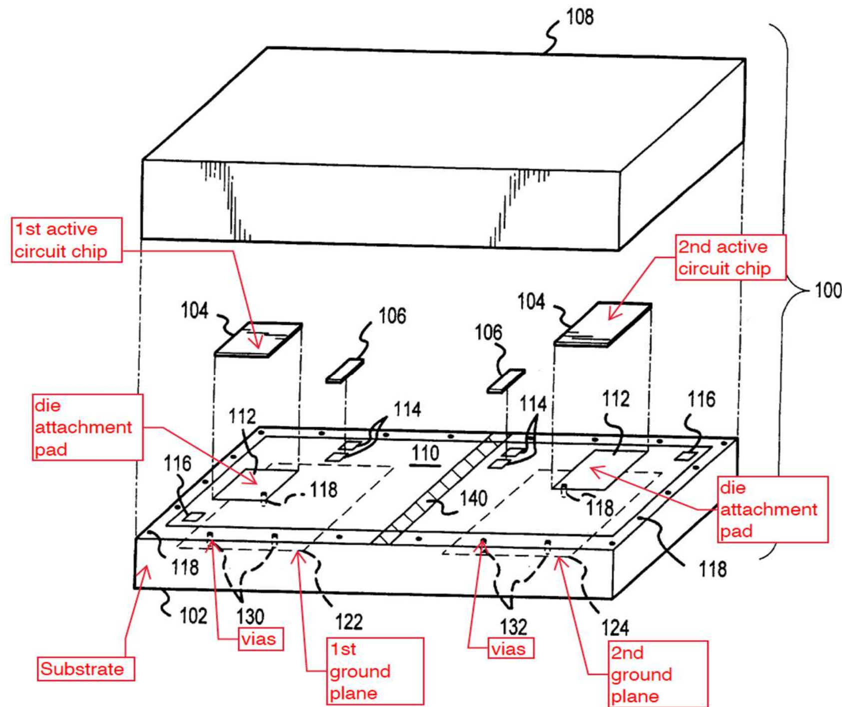
The combination of Miller and Hashemi discloses this limitation or render it obvious. Miller discloses a second ground plane, but places it on a second layer. Hashemi teaches a second ground plane can be on the *same* layer as the first ground plane. A POSITA would have combined the teaching of Hashemi and understood how to implement it in Miller. (Ex. 1002, ¶50.)

Miller discloses multiple ground planes on different layers of a substrate, as shown below in Figure 2. As discussed supra, the second of Miller's ground planes would be configured for electrical connection with electronic circuitry, which would include "high speed" circuitry. (Ex. 1002, ¶51.)



(Ex. 1008, FIG. 2 (annotated).)

Hashemi shows in Figure 1 below, a multichip module (MCM) 100 that includes a substrate 102 that includes a *second* ground plane 124 connected to a second active chip 104. (Ex. 1002, ¶52.)



(Ex. 1006, FIG. 1 (annotated).)

Hashemi further discloses "*split ground planes on the same* or different *metal layers* of a substrate are preferably utilized *to obtain RF isolation* between a plurality of active circuit chips and/or between *different functional sections* on a single active circuit chip. As shown in FIG. 1, MCM 100 may include two functionally distinct portions (each portion being associated with one of the two active chips 104) contained on a single substrate 102. To reduce the amount of unwanted RF interference between the two portions, MCM 100 preferably includes a *first ground plane 122* and a *separate second ground plane 124*. In the context of FIG. 1, first and second ground planes 122 and 124 are formed upon the *same internal metal layer*." (Ex. 1006, 7:9-21 (Emphasis added).) (Ex. 1002, ¶53.)

Hashemi further teaches that "Unlike prior art systems that may require separate RF and baseband packages, MCM 100 may be integrated to include, e.g., a 45 MHz baseband section and a 900 MHz RF section." (*Id.,* 3:44-48 (Emphasis added).) (Ex. 1002, ¶54.)

Hashemi also explicitly teaches electrical isolation using the separate ground planes. For example, Hashemi teaches "the relative separation of vias 906–916 from vias 918-922 *may reflect a desire to electrically or thermally isolate the two portions of circuit chip 902*. RF isolation of active circuitry enables the MCM to integrate a plurality of RF functions onto a single dielectric substrate. *The electrical isolation may be further enhanced through the use of divided ground planes* respectively coupled to the different groups of vias." (Ex. 1006, 9:64-10:4.) (Ex. 1002, ¶55.)

Thus, Hashemi teaches a separate second ground plane (ground plane 124) that is *separate and electrically isolated* from a first ground plane 122. Hashemi further discloses that the separate second ground plane enables connection with high speed circuitry (e.g., the 900 MHz RF section), as the baseband section can be thought of as low speed circuitry and the RF section can be thought of as high-speed circuitry. A POSITA would have understood that 900 MHz is a much higher frequency than baseband and would be considered "high speed," whereas baseband would be considered low speed. This is further evidenced by Patent Owner, which

stated that “RF/IF components may be thought of as high speed circuitry.” (Ex. 1015, pg. 23.) (Ex. 1002, ¶56.)

Notably, the ’091 Patent does not claim or disclose any structural difference from a typical ground plane for “enabling electrical connection with high speed circuitry.” In fact, the Examiner in prosecution of the ’091 Patent gave no weight to this limitation regarding high and low speeds. (Ex. 1004, pp 391-392.) (Ex. 1002, ¶57.)

For example, the Examiner stated “a recitation of the function/intended use such as ‘the first ground plane is configured for electrical connection with low speed electronic circuitry or the second ground plane is configured for electrical connection with high speed electronic circuitry’ of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, and then it meets the claim.” (Ex. 1004, pp 391-392.) (Ex. 1002, ¶58.)

As discussed above, MPEP §2114 discloses in part “A claim containing a ‘recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus’ if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987).” Thus, a POSITA would

have understood that any second separate ground plane would render this limitation obvious, whether or not it was connected to high speed circuitry. However, the combination of Miller and Hashemi explicitly disclose this limitation and thus this limitation would be obvious to a person of ordinary skill in the art.

A POSITA implementing the integrated circuit package of Miller would have had good reason to look to Hashemi as they both are in the same field of integrated circuit packaging and more specifically, directed to multilayered substrates. (Ex. 1002, ¶59.)

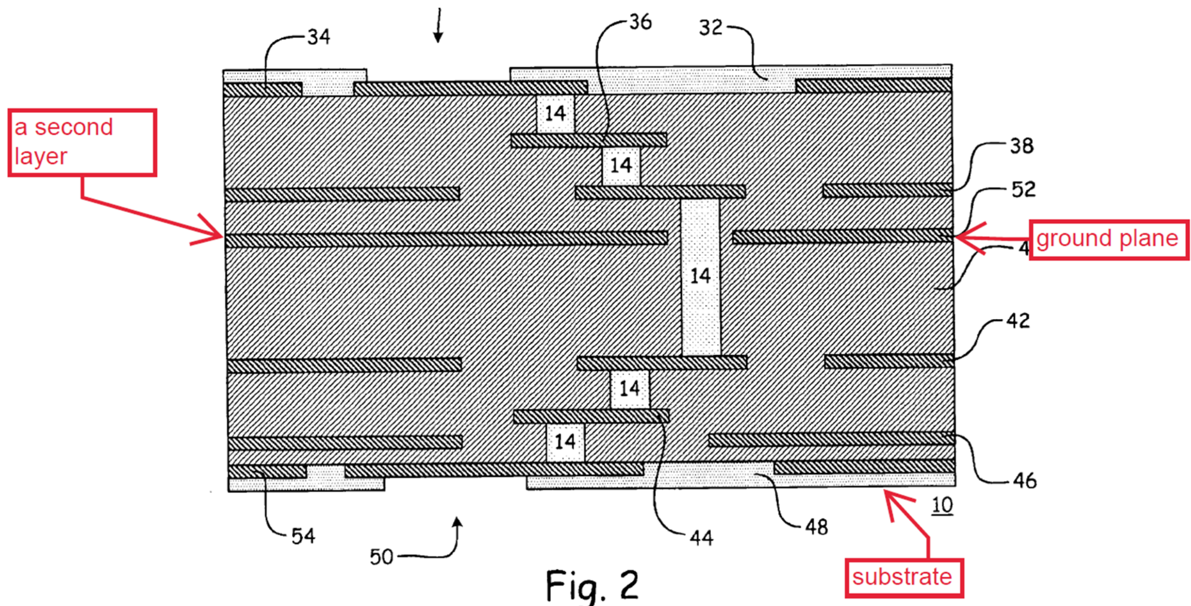
Further, a POSITA implementing the IC of Miller would have been motivated to use Hashemi's split ground planes to further reduce cross talk for high speed systems. (Ex. 1008, 3:16-18.) Furthermore, it would have been a simple substitution to implement the split ground plane of Hashemi in the substrate of Miller, with predictable results of reducing crosstalk by isolating first signals (e.g., RF or high speed signals) from second signals (e.g., baseband or low speed signals) as taught by Hashemi (Ex. 1006, 2:25-29; 5:29-63; 7:9-13; 10:2-5.) (Ex. 1002, ¶60.)

Notably, the claim further does not preclude electricity (e.g., moving electrons) that passed through the second ground plane from never interacting with electrons that passed through the first ground plane. In fact, claim 1 later states a reference plane is associated with each layer and the ground planes included thereon, demonstrating that a reference plane where current would flow is associated with

each ground plane and thus the split ground planes are only electrically isolated on a specific layer of a substrate. Further, claim 1 states that the first ground plane is not electrically connected to the second ground plane *on the first layer*. There is no teaching in the claim that all electricity that passed through a first ground plane never interacts with electricity that at some point passed through a second ground plane. As such, the combination of Miller and Hashemi renders limitation (1e) obvious. (Ex. 1002, ¶61.)

f) "a second layer of the substrate includes,"

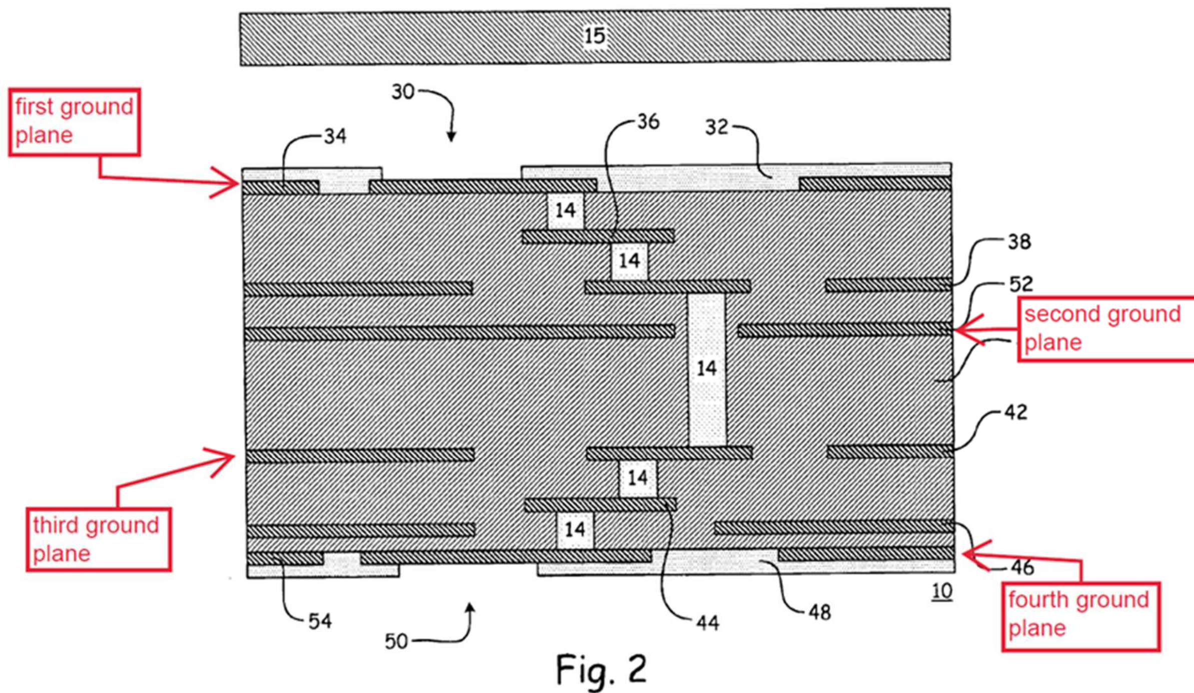
Miller and Hashemi disclose or at least render this limitation (1f) obvious. As shown below in Figure 2, Miller discloses the substrate 10 includes a second layer. For example, Miller discloses that the substrate could include 6 or 8 layers. (Ex. 1008, 5:23-28) A person of ordinary skill in the art would have understood that any non-first layer of the multiple layers would be "a second layer." (Ex. 1002, ¶62.)



(Ex. 1008, FIG. 2 (annotated).)

Hashemi discloses a preferred embodiment where the substrate includes 2-4 metal layers (Ex. 1006, 4:28-34) A POSITA would have understood that one of the 2-4 metal layers would be a second layer. (Ex. 1002, ¶63.)

g) "a third ground plane configured for electrical connection with low speed electronic circuitry, and"



(Ex. 1008, FIG. 2 (annotated).)

Miller and Hashemi disclose or at least render this limitation (1g) obvious. Miller discloses multiple ground planes on different layers of a substrate, as shown above in Figure 2. As discussed supra regarding limitation (1d), a ground plane (e.g., a third ground plane) of Miller's ground planes would be configured for electrical connection with electronic circuitry, which would include "low speed" circuitry. (Ex. 1002, ¶64.)

As discussed *supra* regarding limitation (1d), Hashemi discloses separate ground planes on the *same internal metal layer*. Hashemi further discloses the separate ground planes can be "located at indeterminate metal layers or at the lower exposed metal layer." (Ex. 1006, 11:11-14.) Thus, it would have been obvious to a

POSITA that Miller's third ground plane could be split as taught by Hashemi and further that the split ground planes could be at any layer (e.g., a second layer) of a substrate as taught by Miller. (Ex. 1002, ¶65.)

The split ground planes could be at any layer, as Hashemi explicitly discloses that the split planes can be located at intermediate levels. One of ordinary skill in the art would recognize that a split ground plane on one layer would be electrically isolated from the split ground plane for the ground plane on another level, even if they are coupled together via a common reference plane. (*See,* e.g., Ex. 1006, 9:58-10:5 (stating portions of chip coupled to die attach pad 904 through vias 906-16 are "electrically or thermally isolate[d]" from portions of chip coupled to the same die attach pad 904 through vias 918-22, and "electrical isolation may be further enhanced through the use of divided ground planes"); 8:40-44 (describing Fig. 1 as coupling the divided ground planes 122 and 124 to a common conductive ring 200 depicted in Fig. 2)) (Ex. 1002, ¶66.)

In such case in this alternatively suggested embodiment of Hashemi at column 11, each layer would include at least two ground planes that are isolated from each such that one layer would include a ground plane isolated from a ground plane of the second layer, and a third layer would include a ground plane isolated from a ground plane of the fourth layer. Or in alternative, Hashemi would suggest to one

of skill that the layers of Miller would be implemented with split ground planes isolated from ground planes of the other layers. (Ex. 1002, ¶67.)

Hashemi further teaches that "Unlike prior art systems that may require separate RF and baseband packages, MCM 100 may be integrated to include, e.g., a 45 MHz baseband section and a 900 MHz RF section**.**" (*Id.,* 3:44-48 (Emphasis added).) (Ex. 1002, ¶68.)

Thus, Hashemi teaches a second ground plane (ground plane 124), and that the second ground plane enables connection with low speed circuitry (e.g., a 45MHz baseband section). A POSITA would have understood that the baseband section would be "low speed circuitry." In fact, Patent Owner admits that baseband components are understood by a POSITA to be low speed circuitry and RF components are understood to be high speed circuitry. (Ex. 1015, pg. 23) (Ex. 1002, ¶69.)

Notably, the '091 Patent does not claim or disclose any structural difference from a typical ground plane for "enabling electrical connection with low speed circuitry." In fact, the Examiner in prosecution of the '091 Patent gave no weight to this limitation. (Ex. 1002, ¶70.)

For example, the Examiner stated "a recitation of the function/intended use such as "the first ground plane is configured for electrical connection with low speed electronic circuitry or the second ground plane is configured for electrical

connection with high speed electronic circuitry" of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, and then it meets the claim." (Ex. 1004, pp 391-392.) (Ex. 1002, ¶71.)

Further, as discussed above, MPEP §2114 discloses in part "A claim containing a 'recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus' if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987)."

Thus, the Third-Party Requester believes any ground plane would render this limitation obvious. However, the combination of Miller and Hashemi explicitly disclose this limitation and thus this limitation would be obvious to a person of ordinary skill in the art. (Ex. 1002, ¶72.)

h) "a fourth ground plane that is spatially separated and electrically isolated from the third ground plane, the fourth ground plane configured for electrical connection with high speed electronic circuitry, and"

Miller and Hashemi disclose or at least render this limitation (1h) obvious. As discussed *supra* regarding limitation (1e), Miller discloses multiple ground planes on different layers of a substrate, which could include a fourth ground plane as shown in Figure 2. As also discussed *supra* regarding limitation (1e), the fourth

ground plane of Miller's ground planes would be configured for electrical connection with electronic circuitry, which would include "high speed" circuitry. (Ex. 1002, ¶73.)

Hashemi discloses "the split ground plane feature is not limited to internal metal layers, indicating the split grounds could be located on multiple layers. (Ex. 1006, 7:43-44.) Hashemi further discloses "*split ground planes on the same* or different *metal layers* of a substrate." (Ex. 1006, 7:9-10 (emphasis added).) As such, Hashemi is clearly stating that split ground planes could be on different metal layers and thus it would have been clear to a POSITA that the split ground planes feature could be implemented at more than one metal layer, and thus would include a third and fourth ground plane on a second layer of a multi-layered substrate. (*Id.*) Further, Miller shows ground planes on different layers of a substrate. A POSITA would take note that the '091 Patent does not disclose any difference between a third and fourth ground plane on a second layer versus a first and second ground plane on a first layer. (*Id.*) (Ex. 1002, ¶74.)

In fact, the Patent Owner admitted this by stating "the third and fourth ground planes *are analogous to* the first and second ground planes recited in claim 1." (Ex. 1004, p. 276 (emphasis added).) (Ex. 1002, ¶75.)

As such, it would have been obvious to a POSITA to utilize Hashemi's split ground planes on two different layers of Miller's substrate to produce predictable

results of enhancing electronic isolation between devices as taught by Hashemi. (Ex. 1008, 3:16-18; Ex. 1006, 7:9-13.) (Ex. 1002, ¶76.)

i) "a plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate"

Miller and Hashemi disclose or at least render this limitation (1i) obvious. Miller teaches "electrically conductive transmitter ground vias electrically connecting the transmitter ground layer with the ground contacts." (Ex. 1008, 8:15-17.) (Ex. 1002, ¶77.)

Miller discloses that "Any electrical connection technology can work with the present invention, including ball grid array and chip scale package connections." (Ex. 1008, 4:13-15.) (Ex. 1002, ¶78.)

Hashemi also teaches that MCMs may employ a ball grid array and that solder balls may be used as a termination device at the bottom of the MCM. (Ex. 1006, 12:21-25.) Hashemi further discloses in the description of Figure 7, shown below, an internal ground plane may be "connected to a suitable ground termination." (*Id*., 6:61-63.) (Ex. 1002, ¶79.)

A POSITA would have understood that being "connected to" solder balls would include a plurality of electrical connections and that the bottom of the MCM would be the second surface of the substrate. (Ex. 1002, ¶80.)

j) "a plurality of electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate"

Miller and Hashemi disclose or at least renders this limitation (1j) obvious. Miller teaches "electrically conductive receiver ground vias electrically connecting the receiver ground layer with the ground contacts." (Ex. 1008, 8:38-41.) (Ex. 1002, ¶81.)

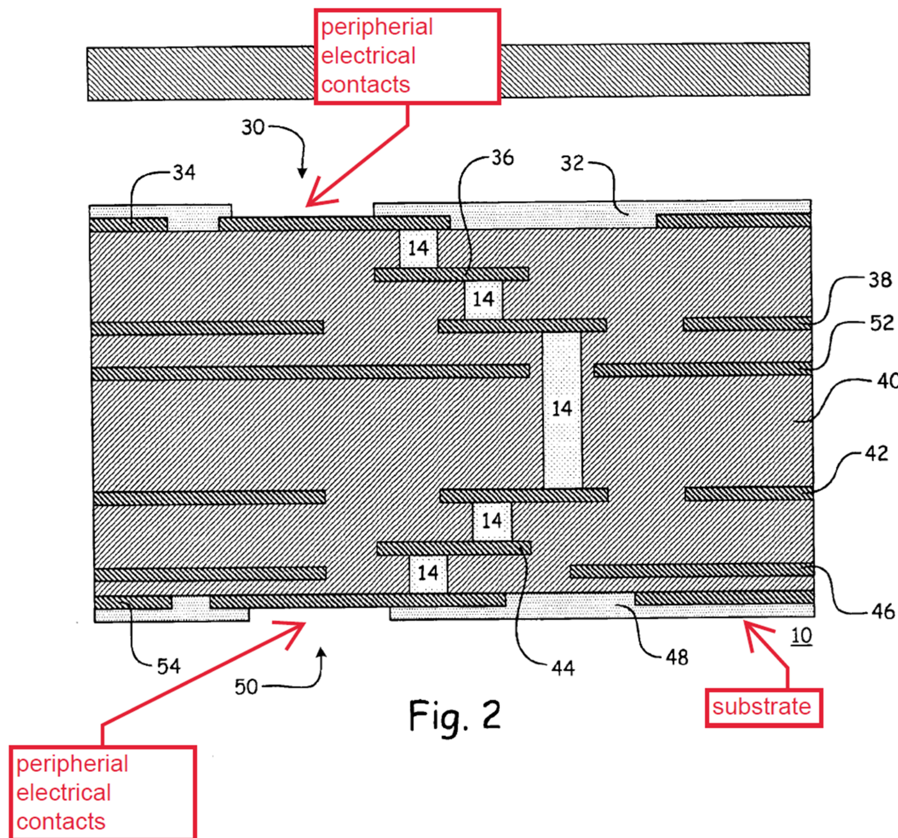
Miller further discloses that "[a]ny electrical connection technology can work… including ball grid array and chip scale package connections." (*Id.*, 4:13-15.) (Ex. 1002, ¶82.)

Hashemi discloses that solder balls may be used as a termination device at the bottom of the MCM. (Ex. 1006, 12:21-25.) Hashemi further discloses that an internal ground plane may be "connected to a suitable ground termination" (*Id.*, 6:61-63), and discloses any of the split ground planes may be electrically connected using vias to die attach pads. (*Id.* 7:13-27.) (Ex. 1002, ¶83.)

k) "peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry external to the package; and"

Miller discloses or at least renders this limitation (1k) obvious. Miller discloses "FIG. 2 also depicts contacts openings 30 in the upper solder mask layer 32, where connections are made to the integrated circuit". (Ex. 1008, 5:47-49.) Miller also discloses "contact openings 50 in the lower solder mask layer 48 provide

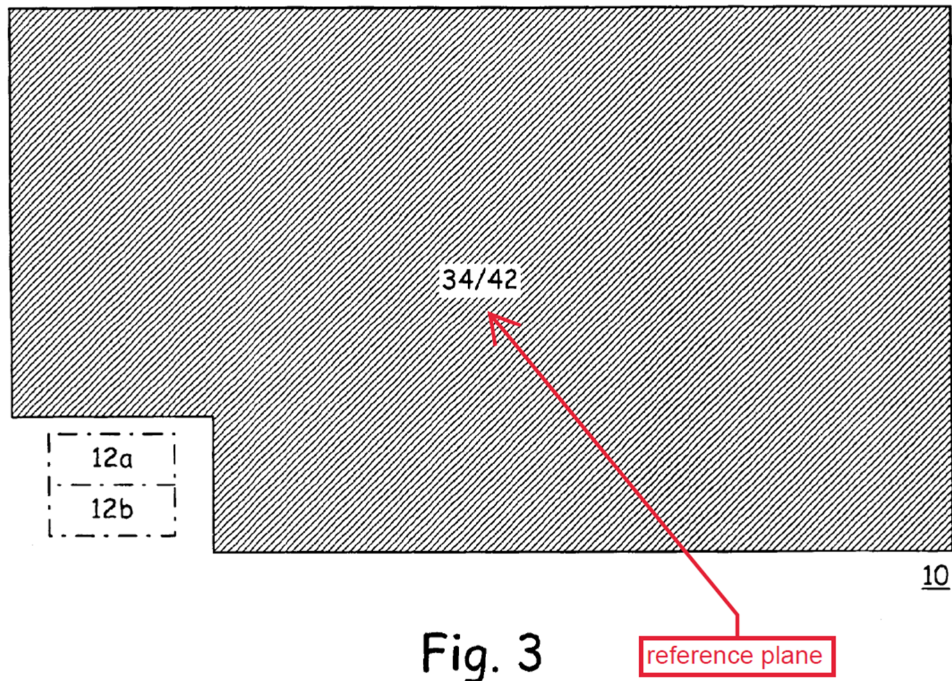
connections to external circuitry. This comprises a lower contact layer ….” (*Id.*, 5:51-53.) A POSITA would have understood these connections to external circuitry would be on the “peripheral” or exterior of the substrate. (Ex. 1002, ¶84.)



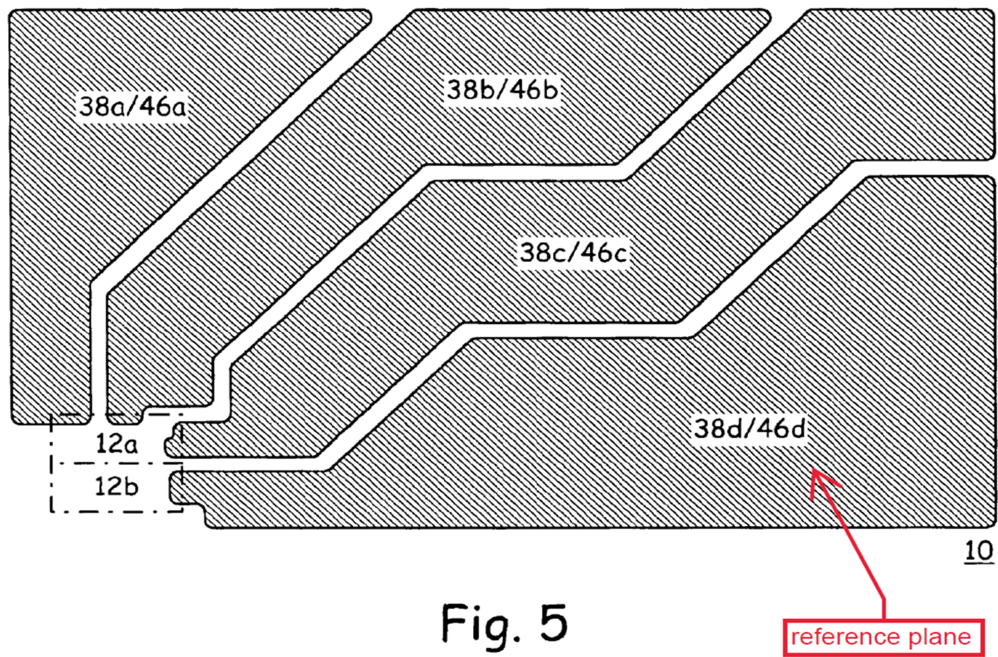
(Ex. 1008, FIG. 2 (annotated).)

l) “At least one reference plane associated with each layer of the substrate and the ground planes included thereon”

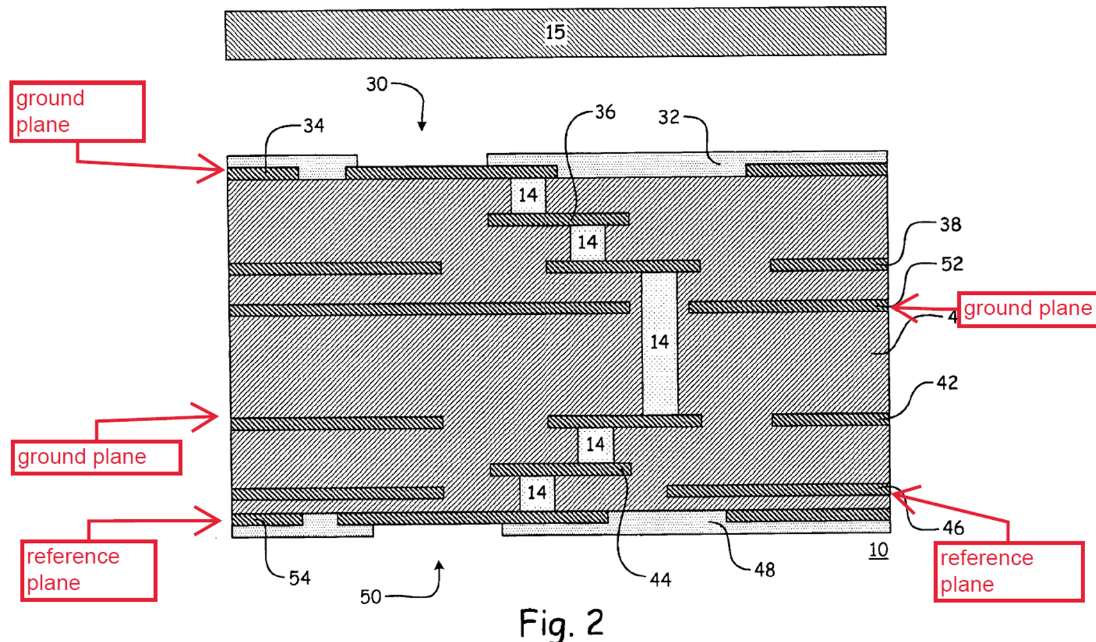
Miller discloses or at least renders this limitation (11) obvious. Miller discloses a reference plane can be “a ground reference layer” as shown below in Figure 3 or a “power reference layer” as shown below in Figure 5. (Ex. 1008, 3:52-60.) (Ex. 1002, ¶85.)



(Ex. 1008, FIG. 3 (annotated).)



(*Id.*, FIG. 5 (annotated).)



(*Id.*, FIG. 2 (annotated).)

Figure 2 of Miller is annotated above to show the examples of a reference plane from Figures 3 and 5 on the substrate 10. As shown, the reference plane is associated with each layer of the substrate 10 and the ground planes thereon. (Ex. 1002, ¶86.)

Notably, the claim further does not preclude electricity (e.g., moving electrons) that passed through a first ground plane on a particular layer from never interacting with electrons that passed through a separate second ground plane on the particular layer. This is evidenced by limitation (1l) which states a reference plane is associated with each layer and the ground planes included thereon, demonstrating that a reference plane where current would flow is associated with each ground plane

and thus the split ground planes are only electrically isolated on a specific layer of a substrate. Further, the only preclusion of claim 1 is that the first ground plane is not electrically connected to the second ground plane *on the first layer*. There is no teaching in the claim that all electricity that passed through a first ground plane never interacts with electricity that at some point passed through a second ground plane. (Ex. 1002, ¶87.)

B. Hashemi in view of Okabe and Rozenblit discloses all the features of Claim 1

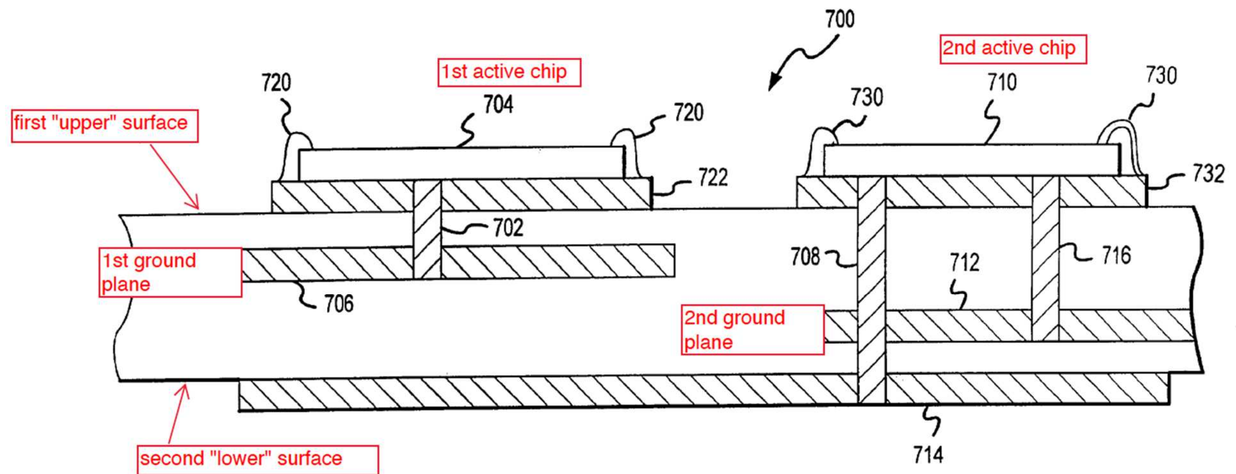
1. Claim 1

a) "A semiconductor integrated circuit (IC) package which comprises:"

Hashemi discloses multiple chip modules (MCMs) as integrated circuit packages that may contain a number of bare and/or packaged integrated circuit (IC) chips and a number of discrete components coupled to an interconnecting substrate. (Ex. 1006, 1:14-18; 12:9-12) (Ex. 1002, ¶88.)

b) "a substrate having a first surface and a second surface wherein;"

Hashemi discloses or at least renders obvious limitation (1b). Hashemi shows in Figure 7, shown below, a substrate with an upper surface and a lower surface. (Ex. 1006, 4:35-40; 6:27; Claim 35) (Ex. 1002, ¶89.)



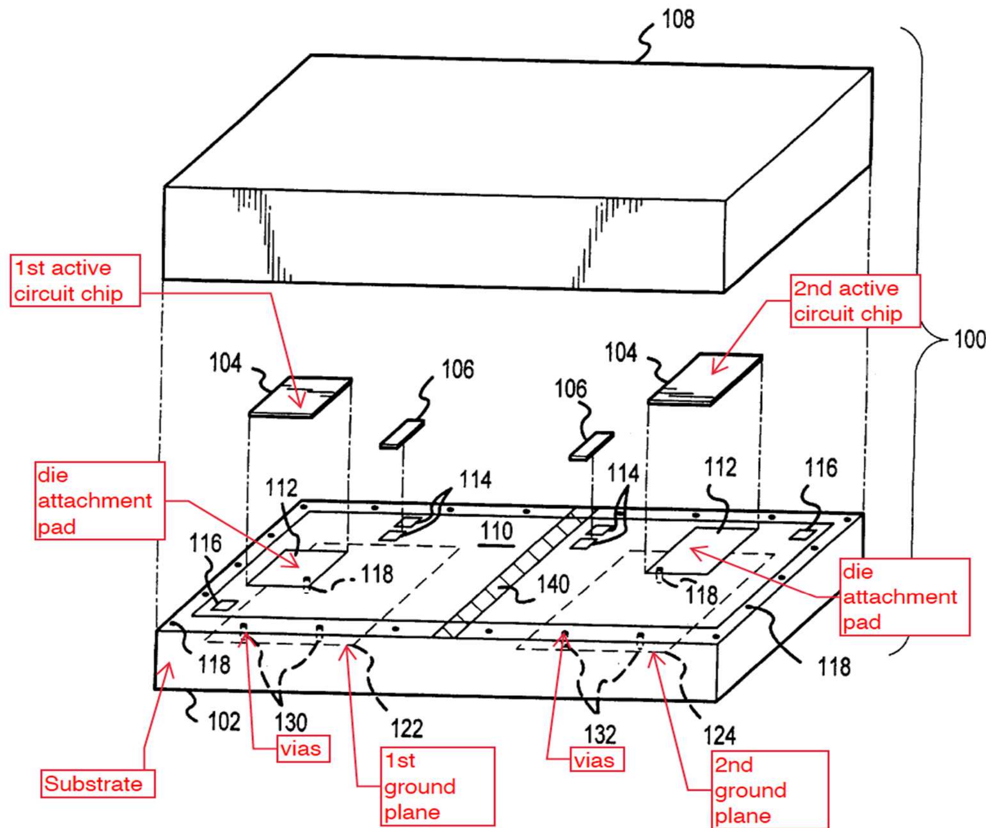
(Ex. 1006, FIG. 7 (annotated).)

c) "a first layer of the substrate includes,"

Hashemi discloses or at least renders obvious limitation (1c). Hashemi discloses the substrate may include any number of metal layers with alternating dielectric layers. (*Id.*, 4:21-34; 7:9-13.) (Ex. 1002, ¶90.)

d) "a first ground plane enabling electrical connection with low speed electronic circuitry, and"

Hashemi discloses or at least renders obvious limitation (1d). Hashemi discloses in Figure 1, shown below, a first ground plane 122 connected by way of vias 130 to a first active chip 104. (Ex. 1006, 7:17-23) (Ex. 1002, ¶91.)



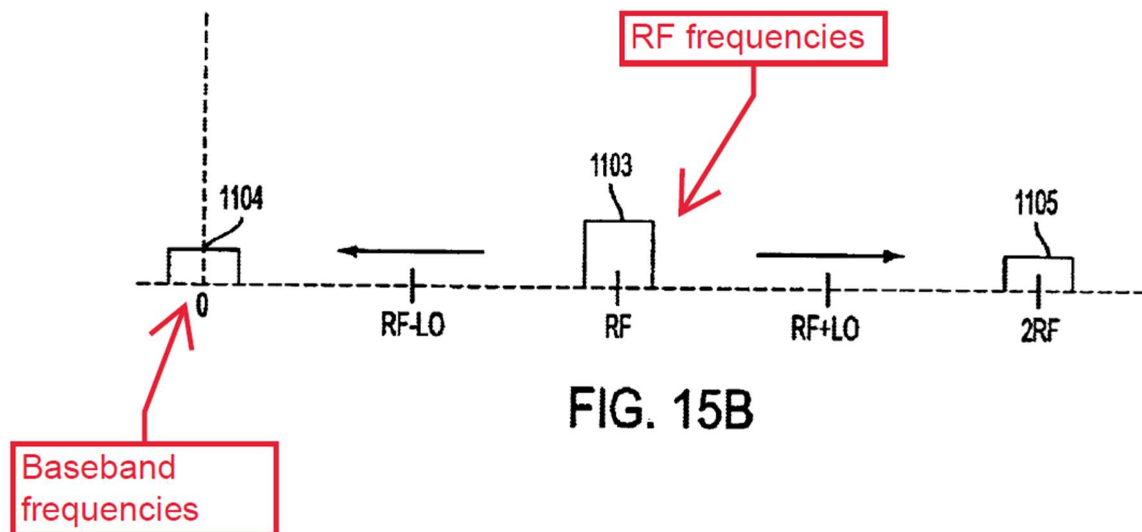
(Ex. 1006, FIG. 1 (annotated).)

Hashemi further teaches that "Unlike prior art systems that may require separate RF and baseband packages, MCM 100 may be integrated to include, e.g., a 45 MHz baseband section and a 900 MHz RF section." (*Id.,* 3:44-48 (emphasis added).) (Ex. 1002, ¶92.)

Thus, Hashemi teaches a first ground plane (ground plane 122), and that the first ground plane enables connection with low speed circuitry (e.g., a 45MHz baseband section). (Ex. 1002, ¶93.)

Rozenblit discloses "baseband frequencies, that is, low frequencies centered **about** 0 Hz". (Ex. 1014, 15:5-7) Rozenblit further discloses "a component 1104 at baseband frequencies." (Ex. 1002, ¶94.)

Thus, Rozenblit teaches that baseband is considered low speed. Thus, a POSITA would have understood that the baseband section of Hashemi would be "low speed circuitry." (Ex. 1002, ¶95.)



(Ex. 1014, FIG. 15B (annotated).)

A POSITA implementing the MCM of Hashemi would have had good reason to look to Rozenblit, as they both are directed to the use of RF transceivers for multi-

function or multi-band for wireless communication implementations. (Ex. 1006, 3:31-51; Ex. 1014, 1:12-14, 4:29-30.) Further, such a POSITA would have been motivated to implement the MCM of Hashemi to adequately protect the MCM against certain frequencies of Rozenblit. (Ex. 1006, 8:24-26.) Furthermore, it would have been a simple substitution to implement the MCM with split ground planes to isolate signals between RF and baseband components on a substrate where the base band frequencies are at the frequencies of Rozenblit, with the predictable results of reducing interference. (Ex. 1006, 7:16-19; 15:14-16; 16:20-22.) (Ex. 1002, ¶96.)

Further, Patent Owner admits that baseband components are understood by a POSITA to be low speed circuitry and RF components are understood to be high speed circuitry. (Ex. 1015, pg. 23.) (Ex. 1002, ¶97.)

Notably, the ’091 Patent does not claim or disclose any structural difference from a typical ground plane for “enabling electrical connection with low speed circuitry”. In fact, the Examiner in prosecution of the ’091 Patent gave no weight to this limitation. (Ex. 1002, ¶98.)

For example, the Examiner stated “a recitation of the function/intended use such as “the first ground plane is configured for electrical connection with low speed electronic circuitry or the second ground plane is configured for electrical connection with high speed electronic circuitry” of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to

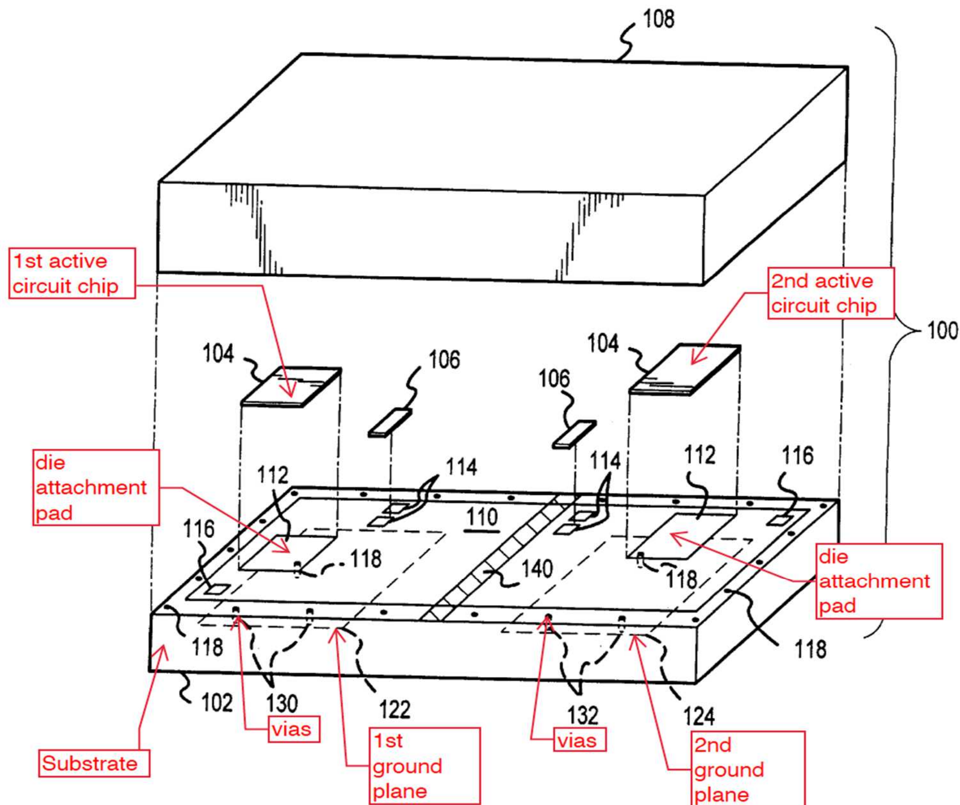
patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, and then it meets the claim." (Ex. 1004, pp 391-392) (Ex. 1002, ¶99.)

As discussed above, MPEP §2114 discloses in part "A claim containing a 'recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus' if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987)." (Ex. 1002, ¶100.)

Thus, a POSITA would have understood that any ground plane would render this limitation obvious. However, the combination of Hashemi and Rozenblit explicitly discloses this limitation and thus this limitation would be obvious to a POSITA.

e) "a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane enabling electrical connection with high speed electronic circuitry;"

Hashemi shows in Figure 1 below, a multichip module (MCM) 100 that includes a substrate 102 that includes *a second ground plane* 124 connected to a second active chip 104. (Ex. 1002, ¶102.)



(*Id.*, FIG. 1 (annotated).)

Hashemi further discloses that these split ground planes can be on the same or different metal layers of a substrate are "preferably utilized to obtain RF isolation between a plurality of active circuit chips and/or between different functional sections on a single active circuit chip. As shown in FIG. 1, MCM 100 may include two functionally distinct portions (each portion being associated with one of the two active chips 104) contained on a single substrate 102. To reduce the amount of unwanted RF interference between the two portions, MCM 100 preferably includes a first ground plane 122 and a separate second ground plane 124. In the context of

FIG. 1, first and second ground planes 122 and 124 are formed upon the same internal metal layer." (Ex. 1006, 7:9-21 (emphasis added).) (Ex. 1002, ¶103.)

Hashemi further teaches that "[u]nlike prior art systems that may require *separate RF and baseband packages*, *MCM 100 may be integrated to include*, e.g., *a 45 MHz baseband section and a 900 MHz RF section*." (Ex. 1006, 3:44-48 (emphasis added).) (Ex. 1002, ¶104.)

Hashemi also explicitly teaches electrical isolation using the separate ground planes. For example, Hashemi teaches "the relative separation of vias 906–916 from vias 918-922 *may reflect a desire to electrically or thermally isolate the two portions of circuit chip 902*. RF isolation of active circuitry enables the MCM to integrate a plurality of RF functions onto a single dielectric substrate. *The electrical isolation may be further enhanced through the use of divided ground planes* respectively coupled to the different groups of vias." (Ex. 1006, 9:64-10:4.) (Ex. 1002, ¶105.)

Thus, Hashemi teaches a separate second ground plane (ground plane 124) that is *separate and electrically isolated* from a first ground plane 122. (Ex. 1002, ¶106.)

Rozenblit discloses that baseband frequencies are low frequencies and that high frequencies can be typically 900Mhz or more. (Ex. 1014, 5:48-50, 15:5-7.) Thus, a POSITA would have understood that separate second ground plane enabling

connection with an RF section that operates at 900 MHz would be high speed circuitry. (Ex. 1002, ¶107.)

That an RF section was known to be high speed is further evidenced by Patent Owner, which stated that “RF/IF components may be thought of as high speed circuitry.” (Ex. 1015, pg. 23.) (Ex. 1002, ¶108.)

Notably, the ’091 Patent does not claim or disclose any structural difference from a typical ground plane for “enabling electrical connection with high speed circuitry”. In fact, the Examiner in prosecution of the ’091 Patent gave no weight to this limitation. (Ex. 1002, ¶109.)

For example, the Examiner stated “a recitation of the function/intended use such as “the first ground plane is configured for electrical connection with low speed electronic circuitry or the second ground plane is configured for electrical connection with high speed electronic circuitry” of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, and then it meets the claim.” (Ex. 1004, pp 391-392.) (Ex. 1002, ¶110.)

As discussed above, MPEP §2114 discloses in part “[a] claim containing a ‘recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus’ if

the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987)." Thus, a POSITA would have understood that any second separate ground plane could be configured for electrical connection with high speed circuitry.

However, the combination of Hashemi and Rozenblit explicitly disclose this limitation and thus this limitation would be obvious to a POSITA. (Ex. 1002, ¶111.)

A POSITA implementing the multiple chip module of Hashemi would have been motivated to enable ground planes to work with low and high speeds as taught by Rozenblit. (Ex. 1002, ¶112.)

A POSITA implementing the MCM of Hashemi would have had good reason to look to Rozenblit, as they both are directed to the use of RF transceivers for multi-function or multi-band for wireless communication implementations. (Ex. 1006, 3:31-51; Ex. 1014, 1:12-14, 4:29-30.) Further, such a POSITA would have been motivated to implement the MCM of Hashemi to adequately protect the MCM against certain frequencies of Rozenblit. (Ex. 1006, 8:24-26.) Furthermore, it would have been a simple substitution to implement the MCM with split ground planes to isolate signals between RF and baseband components on a substrate at the frequencies of Rozenblit, with the predictable results of reducing interference between those signals. (Ex. 1006, 7:16-19; 15:14-16; 16:20-22.) (Ex. 1002, ¶113.)

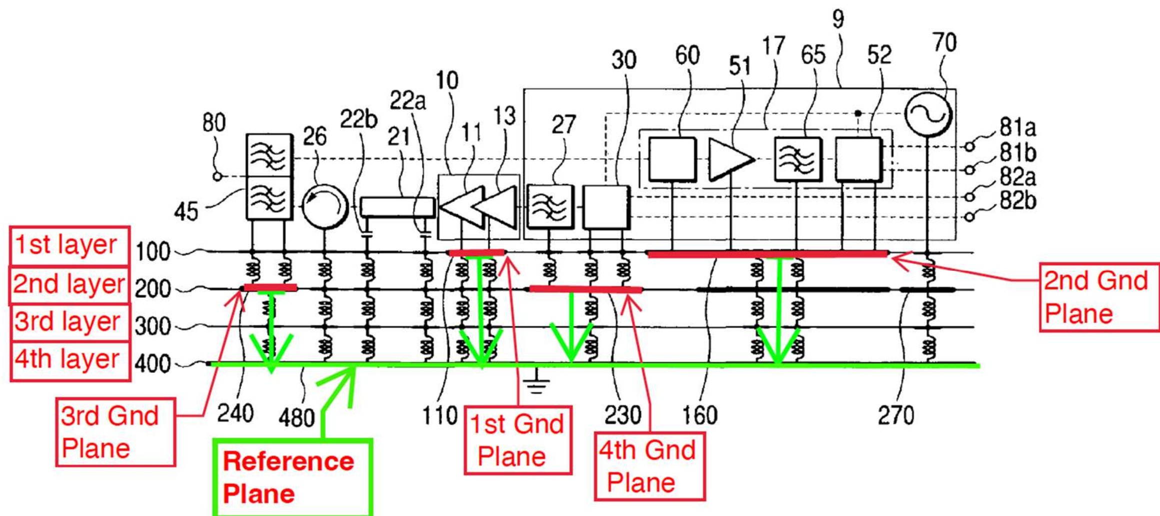
f) "a second layer of the substrate includes,"

Hashemi discloses or at least renders obvious limitation (1f). Hashemi discloses the substrate includes any number of layers and preferred embodiment includes two to four metal layers. (Ex. 1006, 2:21-34.) (Ex. 1002, ¶114.)

g) "a third ground plane configured for electrical connection with low speed electronic circuitry, and"

Hashemi and Okabe disclose or at least render obvious limitation (1g). Hashemi discloses "the MCM may employ split RF ground planes, located at indeterminate metal *layers* or at the lower exposed metal layer to promote effective RF grounding and isolation between different RF chips." (Ex. 1006, 11:11-14.) (Ex. 1002, ¶115.)

Additionally, Okabe discloses in Figure 14, shown below, a third ground plane 240 on the second layer 200 of the substrate 4. (Ex. 1005, 8:27-35.) (Ex. 1002, ¶116.)



(Ex. 1005, FIG. 14 (annotated).)

A POSITA implementing the MCM substrate of Hashemi would have had good reason to look to Okabe as they are in the same field of endeavor, that is, utilizing isolating signals via split ground planes. (Ex. 1006, 7:9-21; Ex. 1005, 14:22-25; 7:61-66.) (Ex. 1002, ¶117.)

Further, such a POSITA would have been motivated to combine the split ground planes of Hashemi on a second layer as explicitly taught by Okabe to reduce interference between different signals. (Ex. 1005, 3:64-66; 5:39-46; Ex. 1006, 7:16-21.) Furthermore, it would have been a simple substitution to implement the split ground planes of Hashemi with the second layer of Okabe with predictable results of reducing interference between signals on the separate ground planes. (Ex. 1005, 3:64-66; 5:39-46; Ex. 1006, 7:16-21.) Still further, Okabe discloses split ground planes on a second layer, and thus a POSITA would have realized that Hashemi's split ground planes could also be on a second layer. (Ex. 1002, ¶118.)

h) "a fourth ground plane that is spatially separated and electrically isolated from the third ground plane, the fourth ground plane configured for electrical connection with high speed electronic circuitry, and"

Hashemi and Okabe disclose or at least render obvious limitation (1h). As discussed above regarding limitation (1d), Hashemi teaches the split ground planes are not limited to one layer. (Ex. 1006, 11:11-14.) Further, as discussed above regarding limitation (1e), Hashemi teaches the split ground planes are electrically isolated and physically distinct. (Ex. 1002, ¶119.)

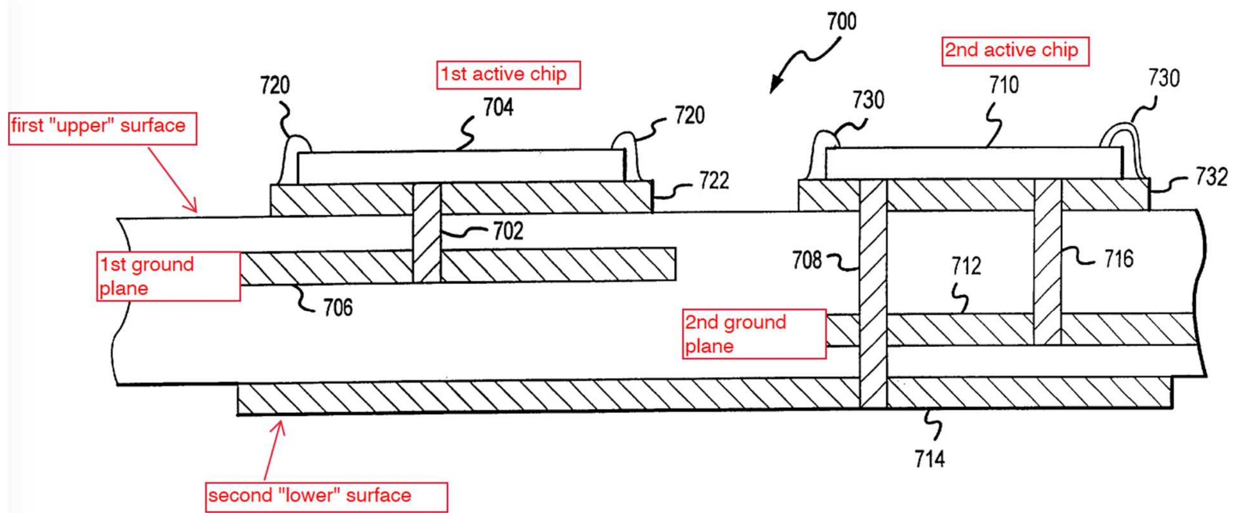
It would have been obvious to a POSITA, that the split ground planes feature of Hashemi could be implemented at a different layer as taught by Okabe, and thus would include a third and fourth ground plane on a second layer of a multi-layered substrate as explicitly taught by Okabe. A POSITA would take note that '091 Patent does not disclose any difference between a third and fourth ground plane on a second layer versus a first and second ground plane on a first layer. (Ex. 1002, ¶120.)

Okabe shows in Figure 14, shown above, a fourth ground plane 270 separated and "electrically isolated" from the third ground plane 240 on the same layer 200 of the substrate 4. (*Id.* 14:13-33.) (Ex. 1002, ¶121.)

i) "a plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate"

Hashemi discloses or at least renders obvious limitation (1i). Hashemi discloses that MCMs may employ a ball grid array and that solder balls may be used as a termination device at the bottom of the MCM. (Ex. 1006, 12:21-25.) Hashemi further discloses in the description of Figure 7, shown below, an internal ground plane may be "connected to a suitable ground termination." (*Id.*, 6:61-63.) (Ex. 1002, ¶122.)

A POSITA would have understood that being "connected to" solder balls would include a plurality of electrical connections and that the bottom of the MCM would be the second surface of the substrate. (Ex. 1002, ¶123.)



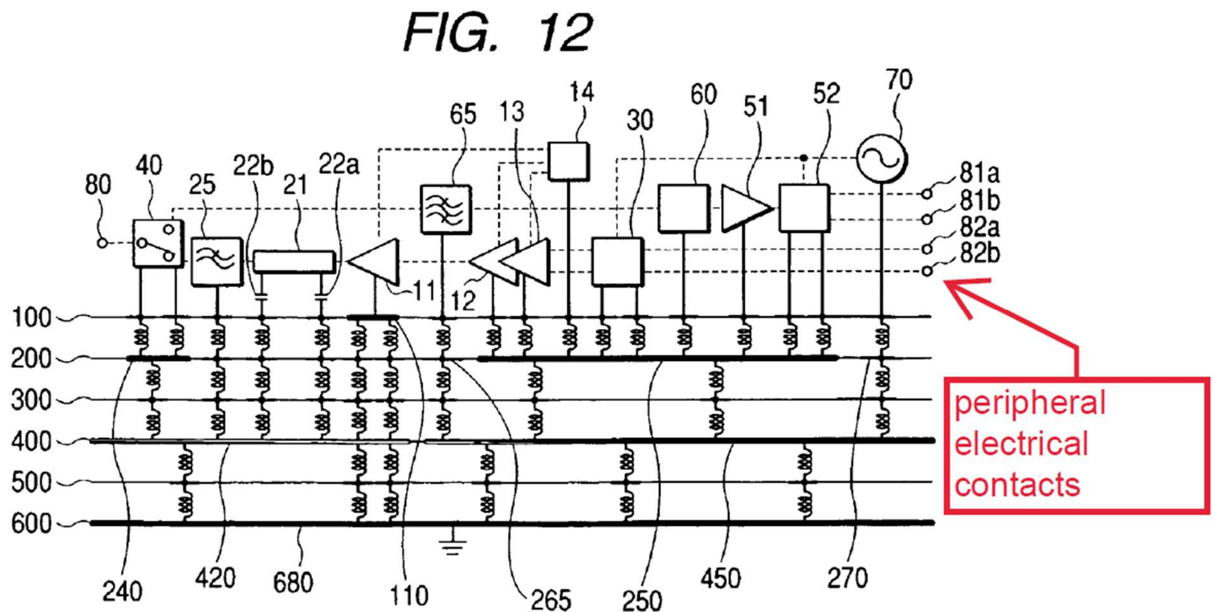
(Ex. 1006, FIG. 7 (annotated).)

j) "a plurality of electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate"

Hashemi discloses or at least renders obvious limitation (1j). Hashemi discloses that MCMs may employ a ball grid array and that solder balls may be used as a termination device at the bottom of the MCM. (*Id.*, 12:21-25.) Hashemi further discloses that an internal ground plane may be "connected to a suitable ground termination" (*Id.*, 6:61-63) and that any of the split ground planes may be electrically connected using vias to die attach pads and/or to a ground provided by a motherboard assembly. (*Id.* 7:13-27.)

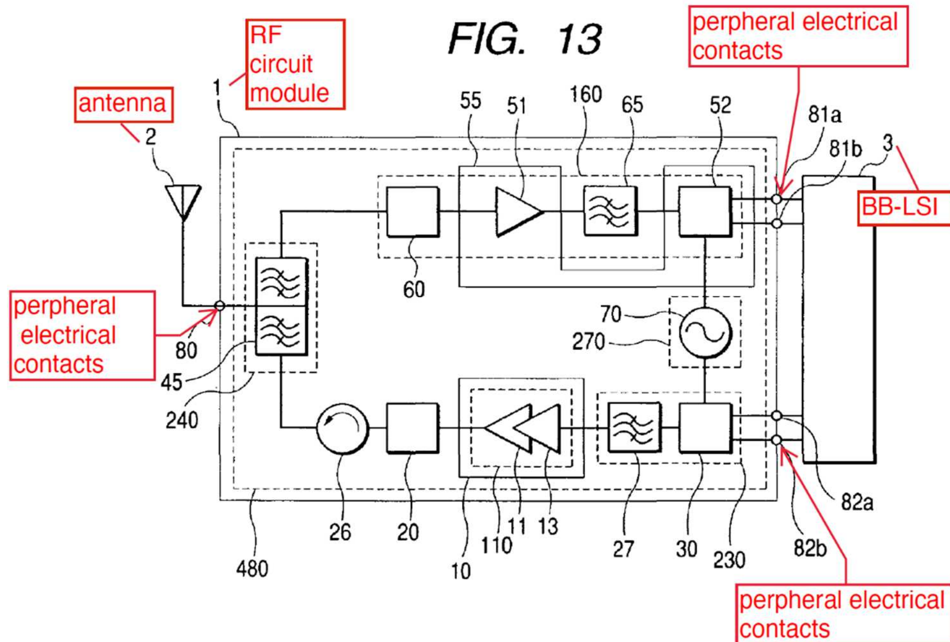
k) "peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry external to the package; and"

Hashemi discloses or at least renders obvious limitation (1k). Hashemi discloses solder balls as a termination device (Ex. 1006, 12:21-25), which a POSITA would have understood as peripheral electrical contacts used to connect with circuitry external to the package. (Ex. 1001, 1:15-29.) (Ex. 1002, ¶125.)



(Ex. 1005, FIG. 12 (annotated).)

Okabe also discloses peripheral electrical contacts as shown above in Figure 12. Further, Okabe discloses in Figure 13, shown below, an antenna 2 and a BB-LSI 3 external to RF circuit module 1. A peripheral connection 80 connects switch 40 with the external antenna 2 and peripheral connections 81a-82b connect the RF module 1 with the external BB-LSI 3. (*Id.*, 7:23-35; 13:40-45). (Ex. 1002, ¶126.)

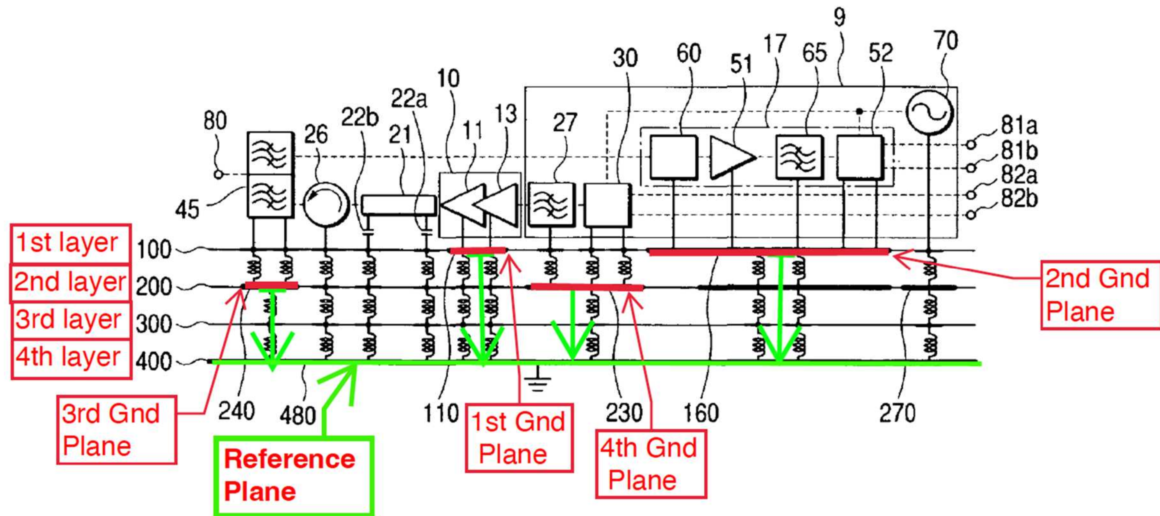


(Ex. 1005, FIG. 13 (annotated).)

l) "At least one reference plane associated with each layer of the substrate and the ground planes included thereon"

Okabe discloses or at least renders obvious limitation (1l). Okabe discloses in Figure 14, shown below, a common ground plane 480 associated with a first layer 100, a second layer 200, a third layer 300, and a fourth layer 400 (e.g., each layer of substrate 4) and each ground plane included on each of the four layers 100-400 (Ex. 1005, 14:13-25). Okabe further discloses that "by providing the module with the common ground plane 480 to which all ground planes are connected, *reference potential* for all RF circuits can be fixed, not dependent on the ground land on the motherboard. As such, a POSITA would have understood the common ground plane

would be "a reference plane" as the circuits would have a common reference to ensure stable performance. (Ex. 1005, 4:7-13.) (Ex. 1002, ¶127.)



(*Id.*, FIG. 14 (annotated).)

The fact that a POSITA would know a ground plane could serve as a reference plane is evidenced further by the background section of the '091 Patent, which discloses that a ground plane is "also referred to herein as a 'Vss plane'" and subsequently refers to a "Vss reference layer," which illustrates that it was well known that a ground layer or plane could serve as a reference layer or plane. (Ex. 1001, 1:25-27; 8:1.) Thus, it would have been obvious to a POSITA that Okabe's common ground plane would be a reference plane associated with each layer of a substrate and the ground planes included thereon. (Ex. 1002, ¶128.)

C. Okabe in combination with AAPA and Rozenblit discloses or suggests all of the features of claims 1 and 12 of the '091 Patent

1. Claim 1

a) "A semiconductor integrated circuit (IC) package which comprises:"

Okabe discloses various "circuits and chips are mounted onto a substrate of the module 1." (Ex. 1005, 13:66-67.) Okabe further discloses prior art multi-chip modules that include integrated circuit chips bonded to a single interconnect substrate. (*Id.*, 2:24-36.) (Ex. 1002, ¶129.)

The '091 Patent discloses limitation (1a) as prior art. (Ex. 1001, 1:15-17 ("The semiconductor industry makes wide use of packaging substrates to hold and electrically interconnect integrated circuit (IC) die mounted within the packaging substrate.").) (Ex. 1002, ¶130.)

The '091 Patent states that Figure 1, shown below, "is a simplified schematic plan view of a portion of a standard [(*i.e.*, prior art)] PBGA (plastic ball grid array) package 100" that includes integrated circuit 101. (Ex. 1001, 1:45-47.) The ball grid array is not depicted in Fig. 1, as it would be on the other side of the substrate. (Ex. 1002, ¶131.)

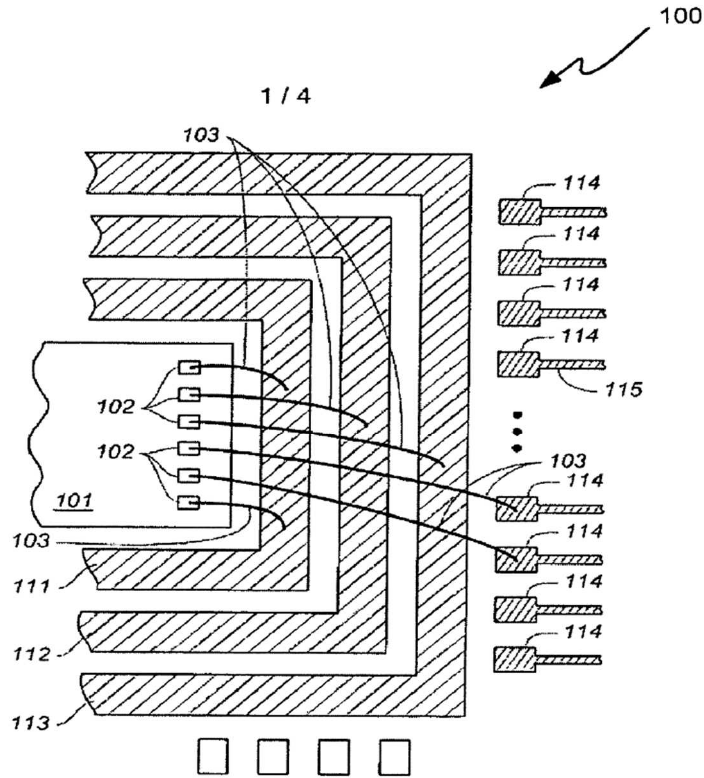
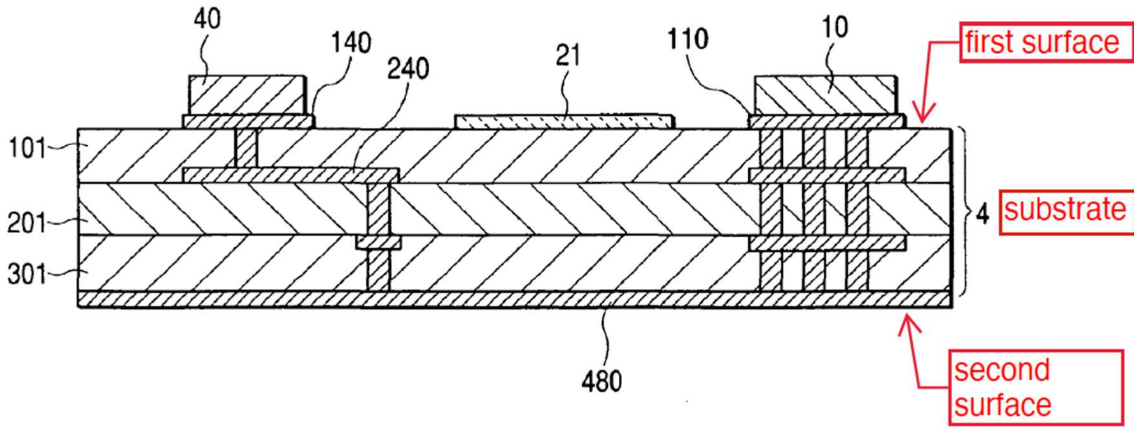


FIG. 1 (PRIOR ART)

(Ex. 1001, FIG. 1.)

b) "a substrate having a first surface and a second surface wherein;"

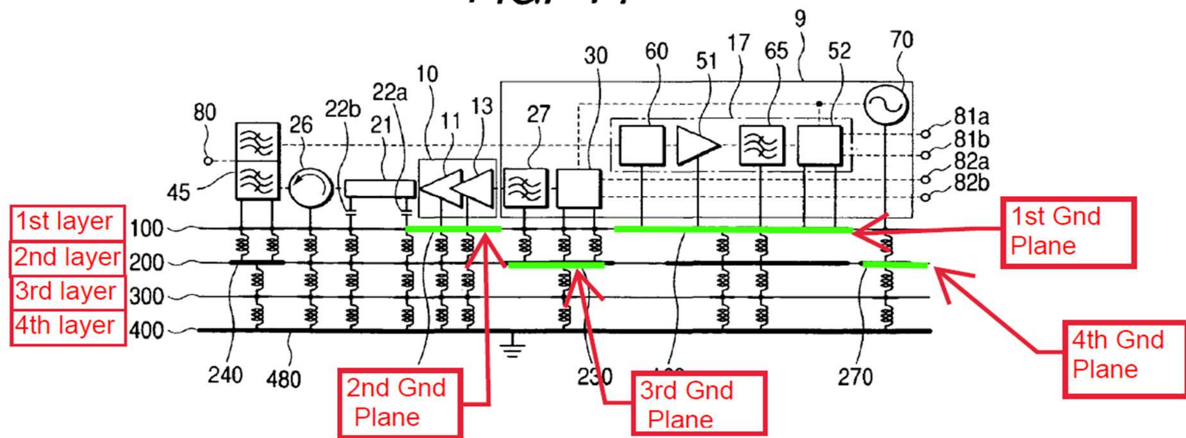
Okabe and AAPA disclose or at least render obvious limitation (1b). As shown in the annotated Figure 10 below, Okabe discloses a substrate 4 having a first surface and a second surface. Further, Okabe discusses a "formation side (top face) of the module substrate." (Ex. 1005, 10:64-65.) A POSITA would have understood that a side or a face of a substrate would be equivalent to a surface, and would also understand that the substrate having a top face or side would indicate the substrate also has a bottom or second side. (Ex. 1002, ¶132.)



(Ex. 1005, FIG. 10 (annotated).)

The ’091 Patent also discloses as AAPA that it was widely known to use packaging substrates. (Ex. 1001, 1:16-20.) A POSITA would have understood a substrate would inherently include a first and second surface. (Ex. 1002, ¶133.)

c) “a first layer of the substrate includes,”



(Ex. 1005, FIG. 14 (annotated).)

Okabe and AAPA both disclose or at least render obvious limitation (1c). Okabe discloses in Figure 14, shown above, a first layer 100 of the substrate 4. (*Id.* 8:18-20, 9:20-22.) The ’091 Patent discloses as AAPA an IC package includes layers. (Ex. 1004, 1:30-32; 5:1-2.) (Ex. 1002, ¶134.)

d) “a first ground plane enabling electrical connection with low speed electronic circuitry, and”

The combination of Okabe, AAPA, and Rozenblit discloses or at least renders obvious limitation (1d). As shown in Figure 14 above, Okabe discloses a first ground plane 110 on the first layer 100 of the substrate 4. (Ex. 1005, 8:8-28.) (Ex. 1002, ¶135.)

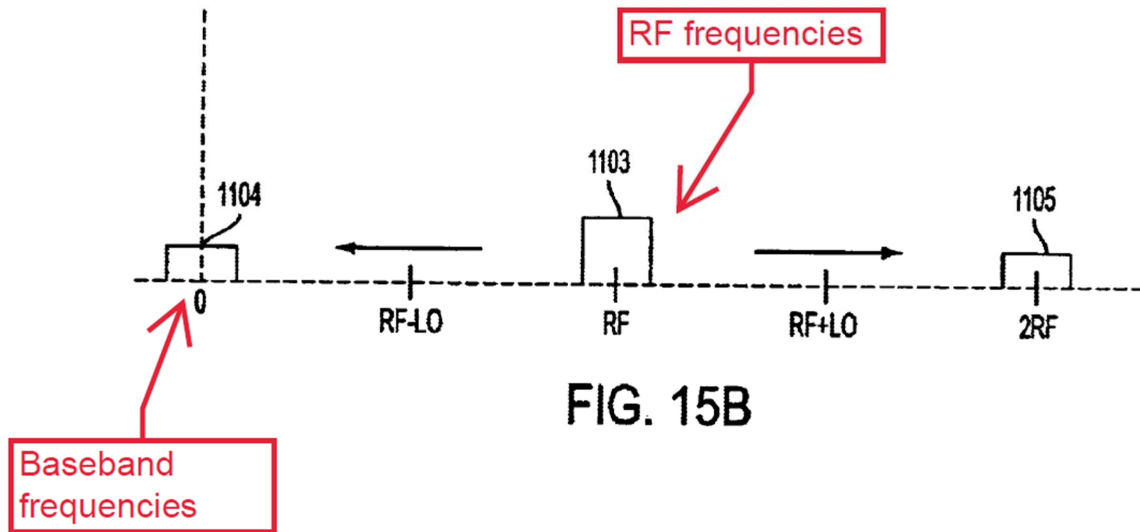
Okabe also discloses that circuits are connected to the ground terminals. (Ex. 1005, 7:52-55; 8:25-27.) A POSITA would have understood that connection of a circuit to a ground plane would be an “electrical connection.” (Ex. 1002, ¶136.)

Okabe further discloses “a radio frequency circuit module comprising a module substrate; first circuit (e.g., a transceiver) to which a first signal (e.g., *transmit signal*) is input and which outputs a second signal (e.g., RF transmit signal) with a higher frequency than the first signal” (Ex. 1005, 3:27-31 (emphasis added)) and a “second circuit (e.g., a power amplifier) which amplifies the second signal.” (Ex. 1005, 3:34-35.) (Ex. 1002, ¶137.)

Okabe further discloses that the BB-LSI 3 (Base Band Large Scale Integrated Circuit) outputs the transmit signal (e.g., the first signal that is a lower frequency than the RF transmit signal). (Ex. 1005, 14:5-6.) (Ex. 1002, ¶138.)

Further, the '091 Patent discloses as AAPA that high and low speed circuitry were commonly known in the art and could be electrically connected to a ground plane (Ex. 1001, 1:64-67 ("in the depicted die 101 the *high speed portions* of the die and *low speed portions* of the die are electrically connected to the same ground plane Vss 111.") (emphasis added).) (Ex. 1002, ¶139.)

Rozenblit discloses "baseband frequencies, that is, low frequencies centered about 0Hz." (Ex. 1014, 15:6-7.)Thus, Rozenblit teaches that baseband frequencies are considered low speed. Thus, a POSITA would understand that the first circuit of Okabe that received the output from Base Band LSI, would be "low speed circuitry." (Ex. 1002, ¶140.)



(Ex. 1014, FIG. 15B (annotated).)

A POSITA implementing the RF circuit module of Okabe would have had good reason to look to Rozenblit, as they both are directed to the use of RF transceivers for multi-function or multi-band for wireless communication implementations. (Ex. 1005, 3:31-51; Ex. 1014, 1:12-14, 4:29-30.) (Ex. 1002, ¶141.)

Further, such a POSITA would have been motivated to use the circuit module of Okabe to adequately protect the circuit module against certain frequencies of Rozenblit interfering with one another as taught by Okabe. (Ex. 1005, 8:24-26.) Furthermore, it would have been a simple substitution to implement the circuit module of Okabe with split ground planes to isolate signals between RF and baseband components on a substrate at the frequencies of Rozenblit, with the predictable results of reducing interference between the RF and baseband

components. (Ex. 1014, 4:46-49, 5:40-62; Ex. 1005, 2:27-29, 3:20-21, 3:58-66.) (Ex. 1002, ¶142.)

Further, there is nothing in the claim precluding an electrical connection with "other" speeds. The only requirement of the claim is that the ground plane **enables** an electrical connection with a certain speed of electronic circuitry. The AAPA discloses that it was known that ground planes were enabled for connection to high speed and low speed electronic circuitry. As such, any ground plane would have rendered limitation (1d) obvious to a POSITA. (Ex. 1002, ¶143.)

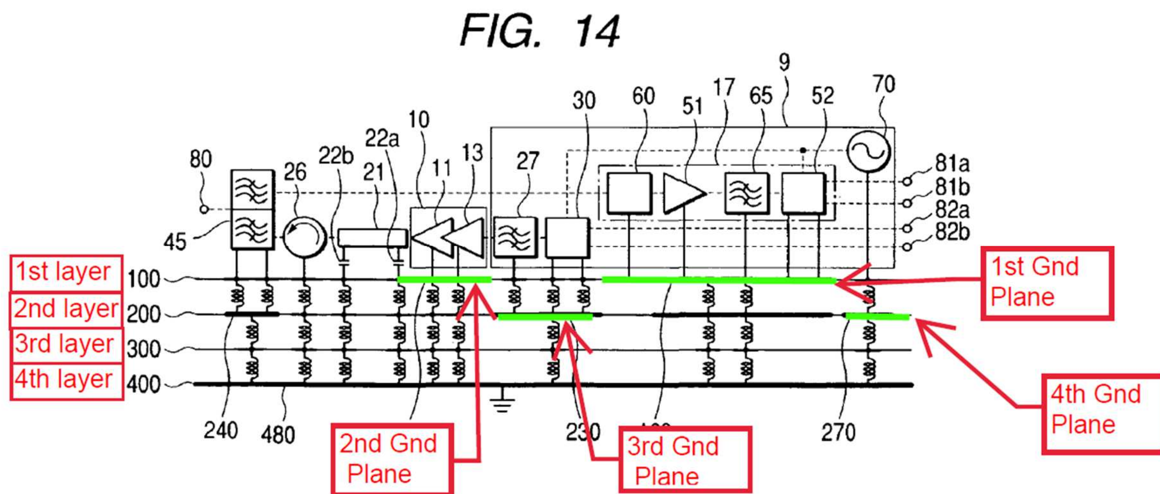
Still further, the '091 Patent does not claim or disclose any structural difference from a typical ground plane for "enabling electrical connection with low speed circuitry." In fact, the Examiner in prosecution of the '091 Patent gave no weight to this limitation. (Ex. 1002, ¶144.)

For example, the Examiner stated "a recitation of the function/intended use such as 'the first ground plane *is configured for electrical connection with low speed electronic circuitry* or the second ground plane *is configured for electrical connection with high speed electronic circuitry*' of the claimed invention *must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art*. If the prior art structure is capable of performing the intended use, and then it meets the claim." (Ex. 1004, pp 391-392 (emphasis added).) (Ex. 1002, ¶145.)

Thus, it would have been obvious to a POSITA that any ground plane would enable electrical connections of low speed circuity, and as such would render this limitation obvious. However, the combination of Okabe, AAPA and Rozenblit explicitly disclose this limitation and thus this limitation would be obvious to a POSITA. (Ex. 1002, ¶146.)

e) "a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane enabling electrical connection with high speed electronic circuitry;"

The combination of Okabe, AAPA, and Rozenblit discloses or at least renders obvious limitation (1e). As shown in Figure 14, shown below, Okabe discloses a second ground plane 160 on the first layer 100 that is separated from and electrically isolated from the first ground plane 110 on the first layer 100. (Ex. 1005, 14:13-25; 14:64-15:3.) (Ex. 1002, ¶147.)



(Ex. 1005, FIG. 14 (annotated).)

Okabe teaches the receiver is "connected to the receive circuits ground plane 160 by bonding wires or solder bumping." (*Id.*, 14:65-67.) A POSITA would have understood that bonding wires or solder bumping would be an electrical connection from the second ground plane that would enable connection with circuitry. (Ex. 1002, ¶148.)

Okabe further discloses "a radio frequency circuit module comprising a module substrate; first circuit (e.g., a transceiver) to which a first signal (e.g., transmit signal) is input and which outputs a *second signal* (e.g., *RF transmit signal*) with a higher frequency than the first signal" (Ex. 1005, 3:27-31 (emphasis added)) and a "*second circuit* (e.g., a power amplifier) which amplifies the ." (Ex. 1005, 3:34-35 (emphasis added).) Okabe further discloses "*a first ground plane for the first circuit*; and *a second ground plane for the second circuit*, electrically isolated from the first ground plane." (Ex. 1005, 3:36-38 (emphasis added).) (Ex. 1002, ¶149.)

Okabe further discloses that "In the RF circuit module … the first circuit and the second circuit, e.g., the transceiver and the power amplifier, *the ground plane for the power amplifier which generates the greatest electric power, thus produces a large current flow* and a great amount of heat, *is isolated from the other ground planes*; *consequently, signal interference* caused by a part of the large current flowing into the other circuits *is reduced*. (Ex. 1005, 3:58-66 (emphasis added).) (Ex. 1002, ¶150.)

Further, the ’091 Patent discloses as AAPA that high and low speed circuitry were commonly known in the art and could be electrically connected to a ground plane (Ex. 1001, 1:64-67 (“in the depicted die 101 the *high speed portions* of the die and *low speed portions* of the die are electrically connected to the same ground plane Vss 111.”).) (Ex. 1002, ¶151.)

Rozenblit discloses RF signals include “high frequencies” such as frequencies of 900 MHz or more. (Ex. 1014, 35-50.) (Ex. 1002, ¶152.)

Thus, Rozenblit teaches that RF signals are considered high speed. As such, a POSITA would understand that the second circuit of Okabe that amplifies the RF transmit signal would be “high speed circuitry.” Furthermore, a POSITA would have been motivated to use separate ground planes for high and low speed circuitry to reduce signal interference as taught by Okabe (Ex. 1005, 15:13-22.), as high and low speed signals of Rozenblit were known to interfere with each other as taught by AAPA. (Ex. 1002, ¶153.)

Notably, the ’091 Patent does not claim or disclose any structural difference between a typical ground plane and a ground plane for “enabling electrical connection with high speed circuitry.” In fact, the Examiner in prosecution of the ’091 Patent gave no weight to this limitation. (Ex. 1002, ¶154.)

For example, the Examiner stated “a recitation of the function/intended use such as “the first ground plane is configured for electrical connection with low speed

electronic circuitry or the second ground plane is configured for electrical connection with high speed electronic circuitry" of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, and then it meets the claim." (Ex. 1004, pp 391-392.) (Ex. 1002, ¶155.)

As discussed above, MPEP §2114 discloses in part "[a] claim containing a 'recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus' if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987)."

Thus, a POSITA would have understood that any separate second ground plane would be enabled for electrical connection with circuitry, which would include high and/or low speeds as taught by the AAPA as discussed above. However, the combination of Okabe, AAPA, and Rozenblit explicitly discloses this limitation and thus this limitation would be obvious to a POSITA. (Ex. 1002, ¶156.)

Notably, the claim further does not preclude electricity (e.g., moving electrons) that passed through the second ground plane from never interacting with electrons that passed through the first ground plane. In fact, claim 1 later states a reference plane is associated with each layer and the ground planes included thereon,

demonstrating that a reference plane where current would flow is associated with each ground plane and thus the split ground planes are only electrically isolated on a specific layer of a substrate. Further, the only preclusion of claim 1 is that the first ground plane is not electrically connected to the second ground plane *on the first layer*. There is no teaching in the claim that all electricity that passed through a first ground plane never interacts with electricity that at some point passed through a second ground plane. As such, the combination of Okabe, AAPA, and Rozenblit explicitly renders limitations (1e) obvious. (Ex. 1002, ¶157.)

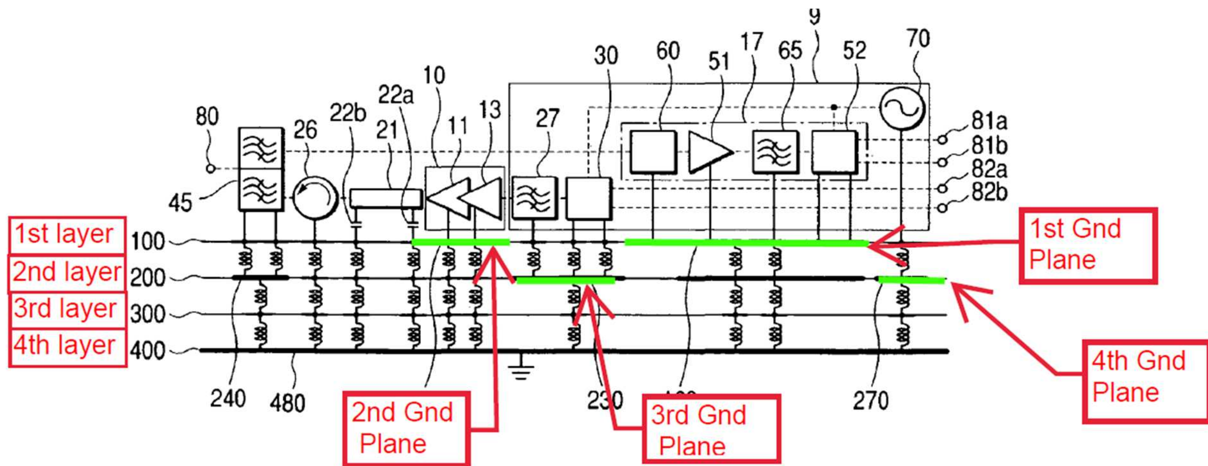
f) "a second layer of the substrate includes,"

Okabe and AAPA both disclose or at least renders obvious limitation (1f). As shown in Figure 14 above, Okabe discloses a second layer 200 of the substrate 4. (Ex. 1005, 8:18-21, 9:28-31.) Further, the '091 Patent discloses as AAPA an IC package includes *layers*. (Ex. 1001, 1:30-32, 5:1-2.) (Ex. 1002, ¶158.)

g) "a third ground plane configured for electrical connection with low speed electronic circuitry, and"

The combination of Okabe, AAPA, and Rozenblit disclose at least renders obvious limitation (1g). (Ex. 1002, ¶159.)

Okabe, as shown below, also discloses a third ground plane 230 on the second layer 200 of the substrate 4. (Ex. 1005, 8:27-35.) (Ex. 1002, ¶160.)



(Ex. 1005, FIG. 14 (annotated).)

Further, as discussed above with reference to limitation (1d) the combination of Okabe, AAPA, and Rozenblit teaches that a first layer includes a first ground plane configured for electrical connection with low speed electronic circuitry. A POSITA would also have understood that any layer (e.g., a second layer) of Okabe could be used for separate ground planes. In fact, the Patent Owner explicitly admitted this by stating "the third and fourth ground planes **are analogous to** the first and second ground planes recited in claim 1." (Ex. 1004, p. 276 (emphasis added).)The '091 Patent discloses as AAPA that high and low speed circuitry were commonly known in the art and could be electrically connected to a ground plane (Ex. 1001, 1:64-67 ("in the depicted die 101 the *high speed portions* of the die and *low speed portions* of the die are electrically connected to the same ground plane Vss 111.") (emphasis added).) (Ex. 1002, ¶161.)

Further, there is nothing in the claim *precluding* an electrical connection with "other" speeds, only that the ground plane enables an electrical connection with a

certain speed. The AAPA discloses that it was known that ground planes enabled connection to high speed and low speed electronic circuitry. As such, limitation (1g) would have been obvious to a POSITA. (Ex. 1002, ¶162.)

Further, the ’091 Patent does not claim or disclose any structural difference from a typical ground plane for “electrical connection with low speed circuitry.” In fact, the Examiner in prosecution of the ’091 Patent gave no weight to this limitation. (Ex. 1002, ¶163.)

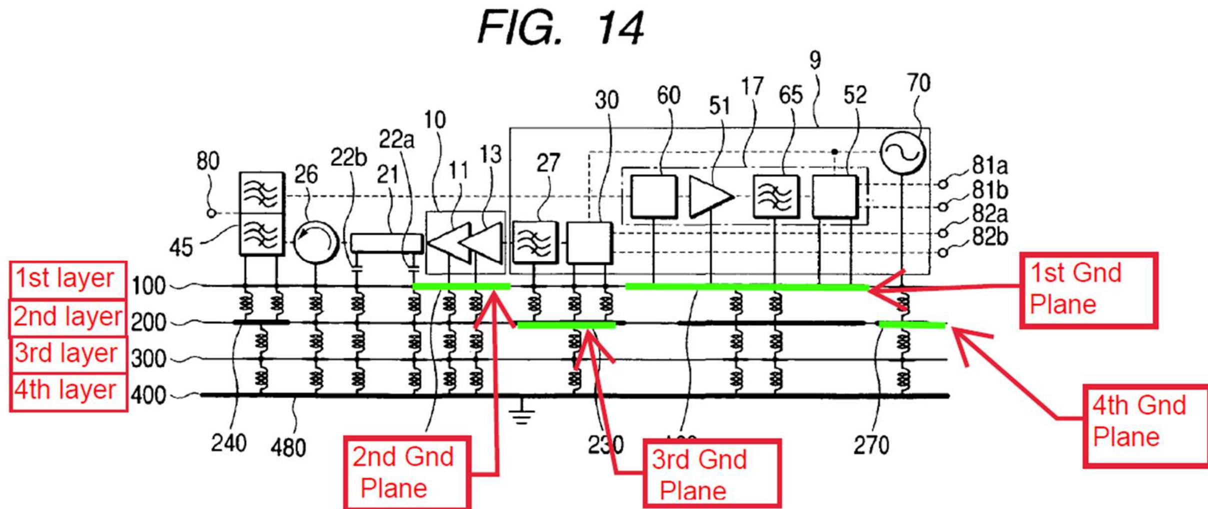
For example, the Examiner stated “a recitation of the function/intended use such as ‘the first ground plane is configured for electrical connection with low speed electronic circuitry or the second ground plane is configured for electrical connection with high speed electronic circuitry’ of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, and then it meets the claim.” (Ex. 1004, pp 391-392.) (Ex. 1002, ¶164.)

Thus, a POSITA would have understood that any ground plane would render this limitation obvious. However, the combination of Okabe, AAPA, and Rozenblit explicitly disclose this limitation and thus this limitation would be obvious to a POSITA. (Ex. 1002, ¶165.)

h) "a fourth ground plane that is spatially separated and electrically isolated from the third ground plane, the fourth ground plane configured for electrical connection with high speed electronic circuitry, and"

The combination of Okabe, AAPA, and Rozenblit discloses or at least renders obvious limitation (1h). As discussed above with reference to limitation (1e) the combination of Okabe, AAPA, and Rozenblit teaches that a first layer includes a second ground plane, separated and electrically isolated from a first ground plane, that is configured for electrical connection with high speed electronic circuitry. A POSITA would have understood that more than one layer (e.g., a second layer) of Okabe could be used for additional separate ground planes. This would have been a straightforward implementation with predictable results of reducing interface between planes on a second layer. In fact, the Patent Owner explicitly admitted this would be obvious by stating "the third and fourth ground planes *are analogous to* the first and second ground planes recited in claim 1." (Ex. 1004, p. 267 (emphasis added).) (Ex. 1002, ¶166.)

Nevertheless, Okabe shows in Figure 14, shown below, a fourth ground plane 270 separated and electrically isolated from the third ground plane 230 on the second layer 200 of the substrate. (Ex. 1005, 14:13-33.) (Ex. 1002, ¶167.)



(Ex. 1005, FIG. 14 (annotated).)

Okabe further discloses "a radio frequency circuit module comprising a module substrate; first circuit (e.g., a transceiver) to which a first signal (e.g., transmit signal) is input and which outputs a *second signal* (e.g., *RF transmit signal*) with a higher frequency than the first signal" (Ex. 1005, 3:27-31 (emphasis added)) and a "*second circuit* (e.g., a power amplifier) which amplifies the *second signal*" (Ex. 1005, 3:34-35 (emphasis added)). Okabe further discloses *a first ground plane for the first circuit*, and *a second ground plane for the second circuit*, where the second ground plane is electrically isolated from the first ground plane. (Ex. 1005, 3:36-38, 4:1-3(emphasis added).) (Ex. 1002, ¶168.)

Okabe further discloses that "[i]n the RF circuit module … the first circuit and the second circuit, e.g., the transceiver and the power amplifier, *the ground plane for the power amplifier which generates the greatest electric power, thus produces a large current flow* and a great amount of heat, *is isolated from the other ground planes*; *consequently, signal interference* caused by a part of the large current flowing into the other circuits *is reduced*." (Ex. 1005, 3:58-66 (emphasis added).) (Ex. 1002, ¶169.)

Thus, Okabe is teaching that separate ground planes reduce signal inference. (Ex. 1002, ¶170.)

Further, the '091 Patent discloses as AAPA that high and low speed circuitry were commonly known in the art and could be electrically connected to a ground plane (Ex. 1001, 1:64-67 ("in the depicted die 101 the *high speed portions* of the die and *low speed portions* of the die are electrically connected to the same ground plane Vss 111.") (emphasis added).) Further, the '091 Patent also discloses as AAPA that the high and low speed were known to affect one another and a prior art solution was "*using individual pins for separately grounding* each high-speed connection." (Ex. 1001, 2:23-27 (emphasis added).) (Ex. 1002, ¶171.)

Rozenblit discloses RF signals include "high frequencies" such as frequencies of 900 MHz or more. (Ex. 1014, 35-50.) Thus, Rozenblit teaches that RF signals are considered high speed. (Ex. 1002, ¶172.)

As such, a POSITA would have been motivated to use the separate ground planes that reduce signal interference as taught by Okabe for the high and low speed signals of Rozenblit, as the high and low speed signals were known to interfere with each other as taught by AAPA. (Ex. 1002, ¶173.)

A POSITA implementing the RF circuit module of Okabe would have looked to AAPA to reduce signal interference between signals that were known to interfere with each other like high and low speed signals. Such a person would then have looked to Rozenblit to separate low speed or baseband signals from high speed or RF signals to achieve predictable results of reducing interference between the RF and baseband signals. (Ex. 1002, ¶174.)

Notably, the ’091 Patent does not claim or disclose any structural difference from a typical ground plane for "enabling electrical connection with high speed circuitry." In fact, the Examiner in prosecution of the ’091 Patent gave no weight to this limitation. (Ex. 1002, ¶175.)

For example, the Examiner stated "a recitation of the function/intended use such as 'the first ground plane is configured for electrical connection with low speed electronic circuitry or the second ground plane is configured for electrical connection with high speed electronic circuitry' of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art

structure is capable of performing the intended use, and then it meets the claim." (Ex. 1004, pp 391-392.) (Ex. 1002, ¶176.)

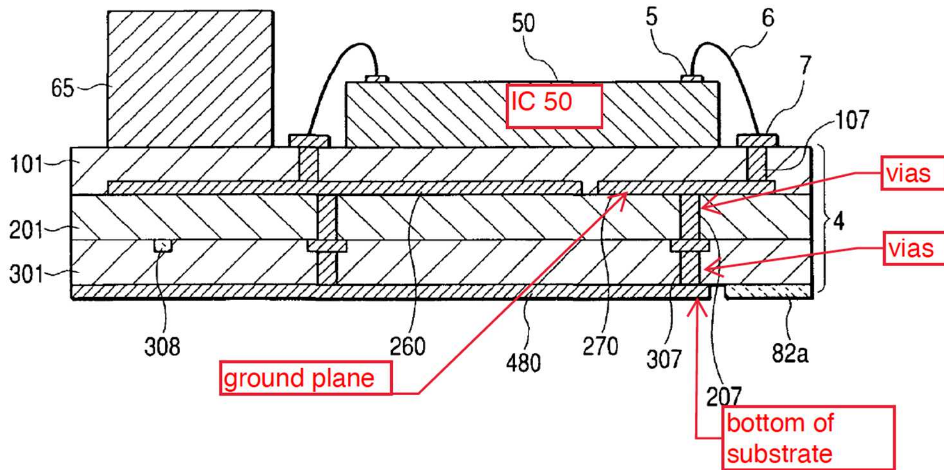
Thus, a POSITA would have understood that any separate fourth ground plane from a third ground plane would render this limitation obvious. However, the combination of Okabe, AAPA and Rozenblit explicitly disclose this limitation and thus this limitation would be obvious to a POSITA. (Ex. 1002, ¶177.)

Notably, the claim further does not preclude electricity (e.g., moving electrons) that passed through the third ground plane from never interacting with electrons that passed through the fourth ground plane. The only preclusion of claim 1 is that the fourth ground plane is not electrically connected to the third ground plane *on the second layer*. There is no teaching in the claim that all electricity that passed through a third ground plane never interacts with electricity that at some point passed through a fourth ground plane. As such, Okabe and AAPA explicitly renders limitations (1h) obvious. (Ex. 1002, ¶178.)

i) "a plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate"

Okabe and AAPA disclose or at least render obvious limitation (1i). Okabe in Figure 9, shown below, discloses a first ground plane 270 electrically connected to a bottom of a substrate 4 by way of vias 207 and 307. (Ex. 1005, 8:38-44.) A POSITA would have understood that "vias" would be a plurality of electrical connections as

was well known as discussed below in paragraph 109. Okabe also discloses solder bumping may be used in a flip chip connection process. (*Id.*, 9:32-38.) (Ex. 1002, ¶179.)



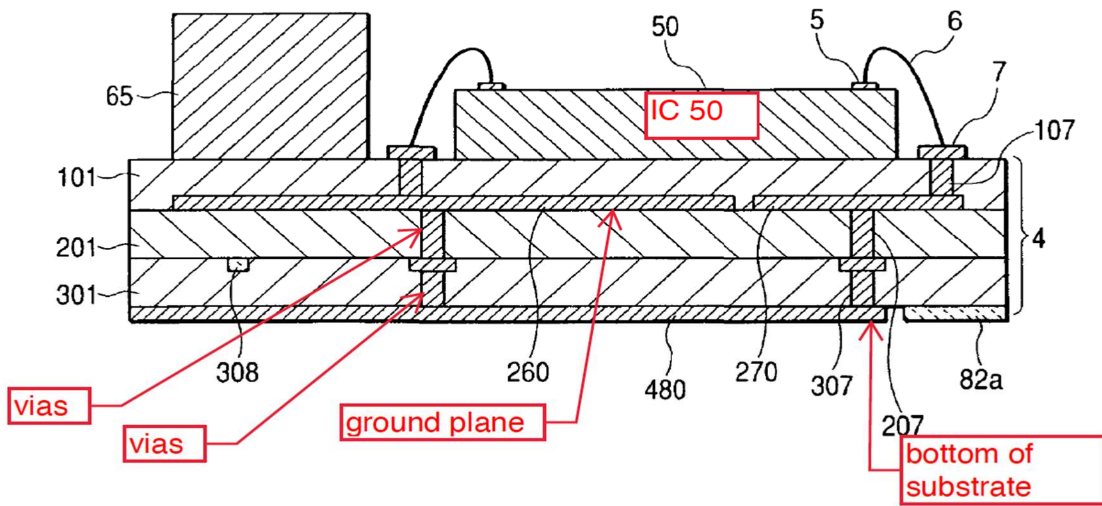
(Ex. 1005, FIG. 9 (annotated).)

The ’091 Patent also discloses that the prior art teaches solder balls on a bottom of a substrate are electrically connected to a ground layer, either via fingers to vias or directly via interlayer vias. (Ex. 1001, 1:51-67; 4:37-42 (“when the principles are applied to ball grid array (BGA) type packages, these contacts are typically facilitate[d] by conductive vias that pass through the substrate and are electrically connected to both, a ground plane and an underlying solder pad. Solder balls are then used to make the external ground connections to other grounds”.)) The ’091 Patent further discloses as AAPA that the packaging substrate 600 can be “an ordinary multi-layer BGA substrate 600.” (*Id.*, 7:34-35.) (Ex. 1002, ¶180.)

As such, a POSITA would have understood that a normal (ordinary) BGA substrate would provide a plurality of electrical connections to connect a ground plane with solder balls mounted on a second surface (e.g., bottom) of the BGA substrate. As such, a POSITA would have understood that solder balls could be mounted on the bottom of Okabe's substrate 4 and that Okabe's vias 207 and 307 would be a "plurality of electrical connections" to electrically connect Okabe's ground plane 270 with the solder balls. (Ex. 1002, ¶181.)

j) "a plurality of electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate"

Okabe and AAPA disclose or at least render obvious limitation (1j). Okabe teaches a second ground plane 260 (e.g., ground plane 260 that is different from ground plane 270) is electrically connected to a second (e.g., bottom) surface of a substrate 4 by way of vias shown in Figure 9, shown below. (Ex. 1002, ¶182.)



(Ex. 1005, FIG. 9 (annotated).)

As discussed in Section VII.C.1(i) above, the ’091 Patent discloses as AAPA that the prior art taught solder balls mounted on a bottom surface of a BGA package. The ’091 Patent further discloses that “typically, metallization lines 115 electrically connects the fingers to vias (not shown) that connect with solder balls on the bottom of the substrate. In some configurations the fingers 114 are typically connected to the ground plane.” (Ex. 1001, 1:50-61.) (Ex. 1002, ¶183.)

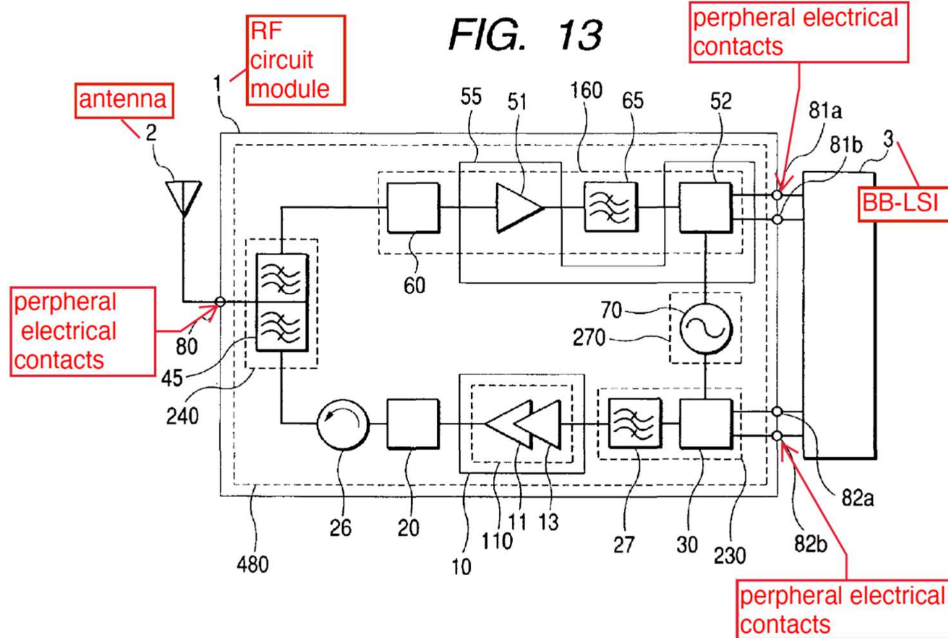
Thus, a person of ordinary skill in the art would have understood the vias would be a plurality of electrical connections that would eletrically connect a second ground plane 260 to commonly used solder balls. (Ex. 1002, ¶184.)

k) “peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry external to the package; and”

Okabe and AAPA disclose or at least renders obvious limitation (1k). Okabe discloses in Figure 13, shown below, an antenna 2 and a BB-LSI 3 external to RF circuit module 1. A peripheral connection 80 connects switch 40 with the external antenna 2 and peripheral connections 81a-82b connect the RF module 1 with the external BB-LSI 3. (*Id.*, 7:23-35; 13:40-45.) (Ex. 1002, ¶185.)

The ’091 Patent discloses as AAPA that “the semiconductor industry makes wide use of packaging substrates to hold and electrically interconnect integrated circuit (IC) die mounted within the packaging substrate. In some implementations the packaging substrates are configured to protect and secure the delicate IC die

while enabling electrical connections with known *external* electrical interconnection socket formats." (Ex. 1001, 1:16-22 (emphasis added).) A POSITA would have understood that external electrical interconnection socket formats would include "peripheral electrical contacts arranged on the substrate" and that the external interconection socket formats would include being configured for connection with circuitry external to an IC package. (Ex. 1002, ¶186.)

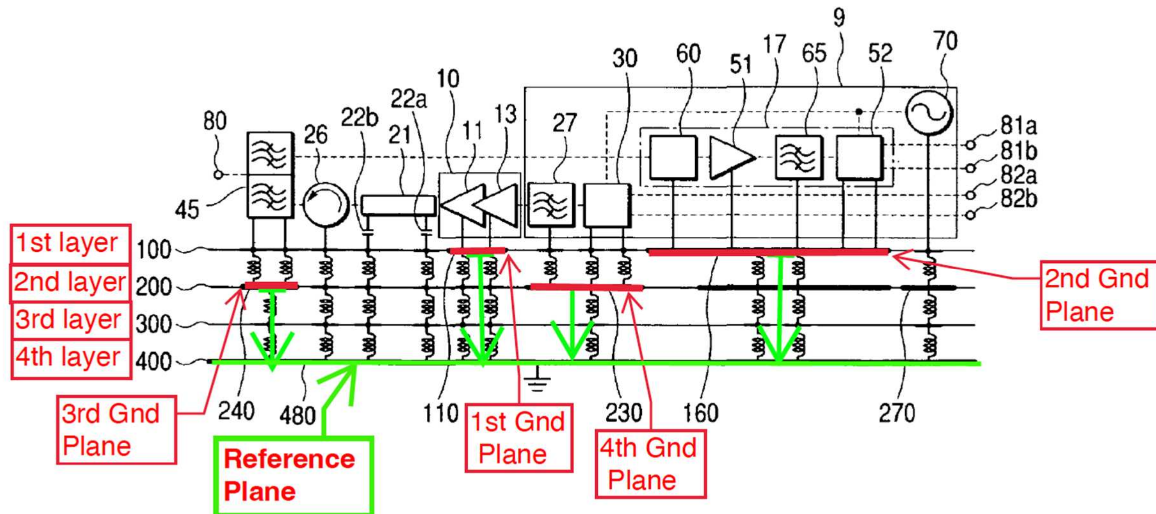


(Ex. 1005, FIG. 13 (annotated).)

l) "At least one reference plane associated with each layer of the substrate and the ground planes included thereon"

Okabe discloses or at least renders obvious limitation (11). Okabe discloses in Figure 14, shown below, a common ground plane 480 associated with a first layer 100, a second layer 200, a third layer 300, and a fourth layer 400 (e.g., each layer of substrate 4) and each ground plane included on each of the four layers 100-400 (Ex.

1005, 14:13-25). Okabe further discloses that "by providing the module with the common ground plane 480 to which all ground planes are connected, *reference potential* for all RF circuits can be fixed, not dependent on the ground land on the motherboard. As such, a POSITA would have understood the common ground plane would be able to be "a reference plane." (Ex. 1002, ¶187.)



(Ex. 1005, FIG. 14 (annotated).)

The fact that a POSITA would know a ground plane could serve as a reference plane is evidenced further by the background section of the '091 Patent, which discloses that a ground plane is "also referred to herein as a 'Vss plane'" and subsequently refers to a "Vss reference layer," which illustrates that it was well known that a ground layer or plane could serve as a reference layer or plane. (Ex. 1001, 1:25-27; 8:1.) Thus, it would have been obvious to a POSITA that Okabe's common ground plane would be a reference plane associated with each layer of a substrate and the ground planes included thereon. (Ex. 1002, ¶188.)

Notably, the claim further does not preclude electricity (e.g., moving electrons) that passed through a ground plane on a layer from never interacting with electrons that passed through a separate ground plane on the layer. In fact, limitation 1l explicitly states "a reference plane associated with each layer and the ground planes included thereon," demonstrating that a reference plane where current would flow is associated with each ground plane and thus the split ground planes are only electrically isolated on a specific layer of a substrate. (Ex. 1002, ¶189.)

Further, the only preclusion of claim 1 is that a ground plane is not electrically connected to a separate ground plane *on the particular layer*. There is no teaching in the claim that all electricity that passed through a first ground plane never interacts with electricity that at some point passed through a second ground plane on the layer. As such, the combination of Okabe, AAPA, and Rozenblit explicitly renders limitations (1l) obvious. (Ex. 1002, ¶190.)

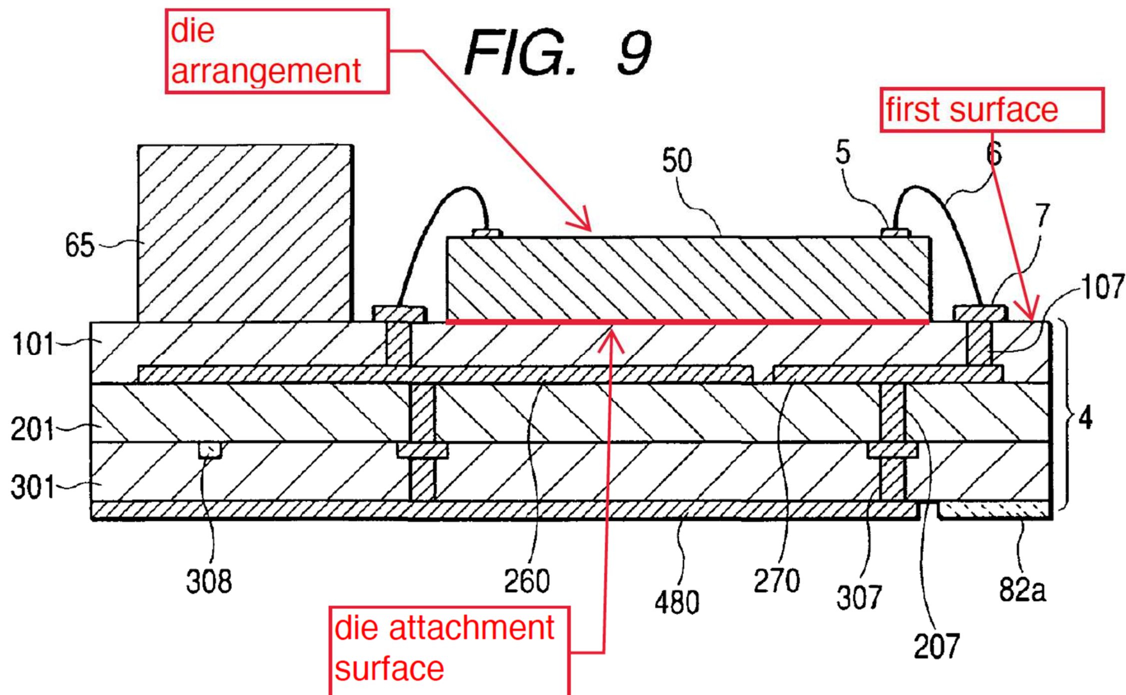
2. Claim 12

Okabe in view of AAPA and Rozenblit discloses or suggests each and every element of dependent claim 12. (Ex. 1002, ¶191.)

a) "An IC package as recited in claim 1, wherein the first surface includes a die attachment surface with a die arrangement attached thereto"

The Okabe-AAPA-Rozenblit combination discloses or suggests this feature. Okabe discloses in Figure 9, shown below, an IC 50 is mounted (attached) to a first

surface (e.g., top) of substrate 4 at a particular area of the substrate (die attachment surface). (Ex. 1005, 9:9-14.) (Ex. 1002, ¶192.)



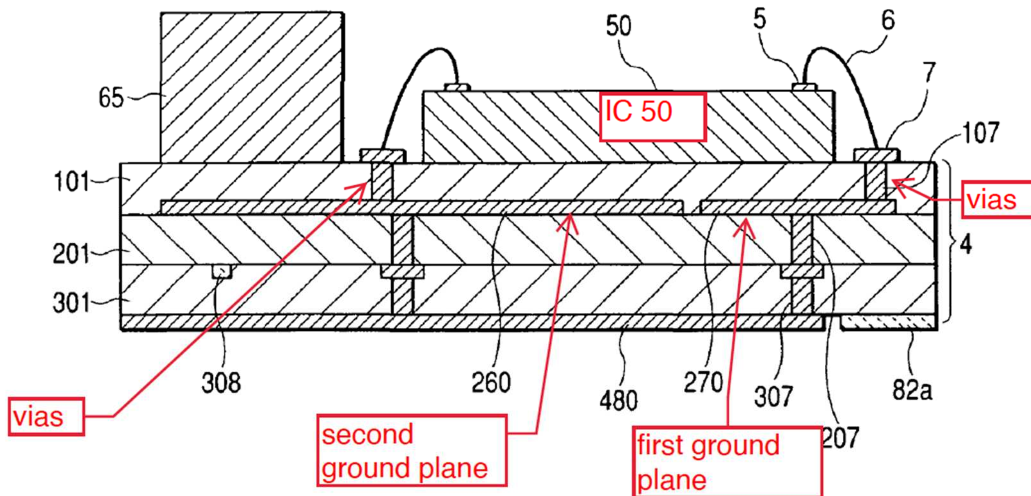
(*E*x. 1005, FIG 9 (annotated).)

The ’091 Patent discloses as AAPA “in one common implementation semiconductor die is attached to the substrate and electrically connected to various electrical connections of the substrate using, for example, wire-bonding techniques. The wire bonds and the die are typically encapsulated with a protective layer of encapsulant. Such packages and the methods of their construction are well known to persons having ordinary skill in the semiconductor packaging arts.” (Ex. 1001, 1:35-42.) As such, a POSITA would have known that the top of Okabe’s substrate where

the IC is mounted, would be a "die attachment surface" for mounting an integrated circuit on the first surface of the substrate. (Ex. 1002, ¶193.)

b) "the die arrangement being electrically connected to the first ground plane, the second ground plane, and the peripheral electrical contacts of the substrate"

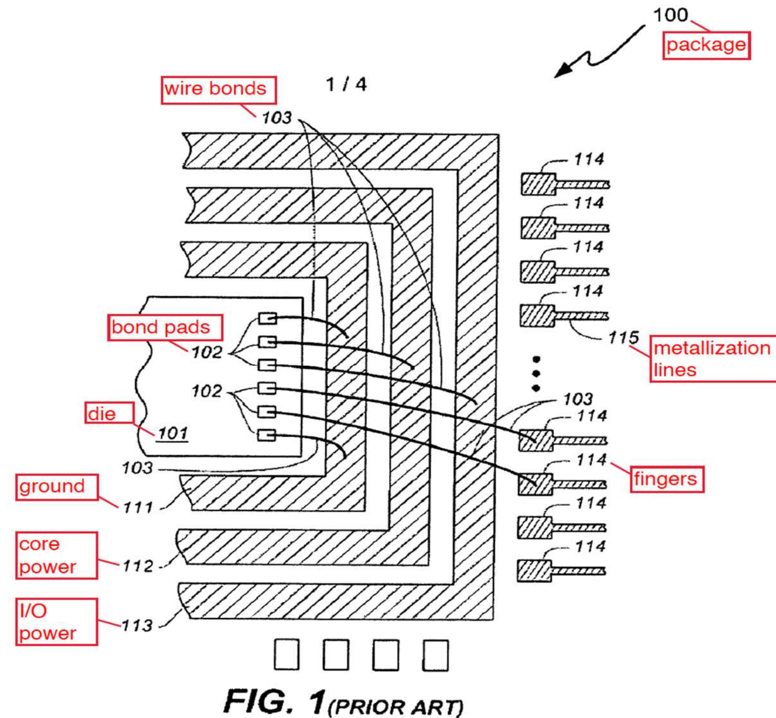
Both Okabe alone and the Okabe-AAPA combination disclose or suggest this feature. Okabe discloses an IC being electrically connected to a first ground plane and a second ground plane on a substrate. For example, Figure 9, shown below, shows an integrated circuit 50 connected (e.g., by way of ground pad 5, bond wire 6, bonding pad 7, and via 107) to a first ground plane 270 and a second ground plane 260. (Ex. 1005, 9:24-31.) As can be seen on Figure 9, shown below, electrical connections 5, 6, 7, and 107, connect the IC die 50 to the ground plane 270 and on the other side of the IC die 50, similar electrical connections (with no reference numerals) connect IC die 50 to a separate ground plane 260. (Ex. 1002, ¶194.)



(Ex. 1005, FIG. 9 (annotated).)

Okabe further discloses the IC being electrically connected to terminals 81a-82b, which are on the peripheral of the substrate module. (*Id.*, 7:4-15, 23-35; 8:29-40.) (Ex. 1002, ¶195.)

The '091 Patent discloses as AAPA that "packaging substrates are configured to protect and secure the delicate IC die while enabling electrical connections with known external electrical interconnection socket formats." (Ex. 1001, 1:19-22.) The peripheral contacts are clearly shown in the '091 Patents prior art Figure 1, shown below, as fingers 114 and metallization lines 115 that are electrically connected to die 101 via bond pads 102 and wires 103. (Ex. 1002, ¶196.)



(Ex. 1001, FIG. 1 (annotated).)

D. Okabe in Combination with AAPA, Rozenblit and Sutardja Discloses or Suggests all the features of Claims 2, 5, 6, and 9

1. Claim 2

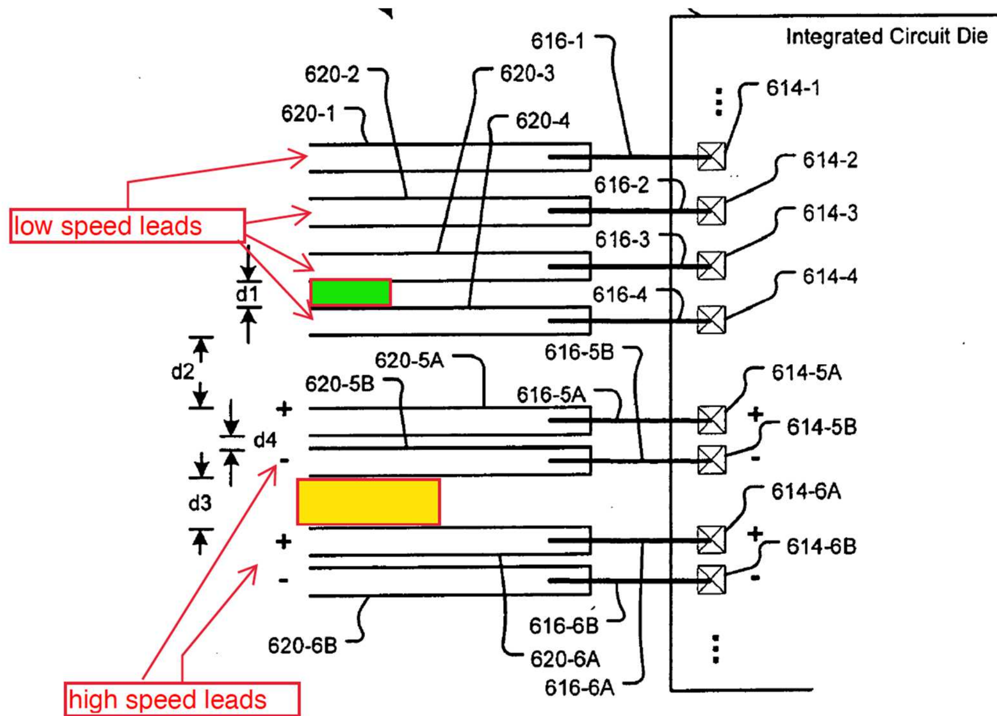
Okabe in view of AAPA, Rozenblit, and Sutardja discloses or suggests each and every element of dependent claim 2. (Ex. 1002, ¶197.)

a) "An IC package as recited in claim 1, wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with low speed circuitry, and"

b) "a second set of electrical contacts for electrical connection with high speed electronic circuitry; and"

The Okabe-AAPA-Rozenblit-Sutardja combination discloses these claim features. The Okabe-AAPA-Rozenblit combination teaches an IC package with

peripheral electrical contacts for electrical connection with low speed and high speed circuitry. (*See supra* Section VII.C.1(a)-(f) regarding claim 1.) As shown below in Figure 10A below, Sutardja also discloses this claim feature by disclosing an integrated circuit (IC) package that includes an IC die having die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶138) and that the leads 620-1 through 620-4 "operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B." (*Id.* ¶139.) (Ex. 1002, ¶198.)



(Ex. 1012, FIG. 10A (annotated).)

A POSITA would have understood that the leads operating at a lower speed would qualify as a first set of electrical contacts for electrical connection with low

speed circuitry and the leads operating at a higher speed would qualify a second set of electrical contacts for electrical connection with high speed circuitry. (Ex. 1002, ¶199.)

c) "wherein the second set of electrical contacts are spaced apart at a distance that is at least twice as far apart as the spacing for the first set of electrical contacts."

Sutardja shows in Figure 10A above, that the second set of leads appear to be twice as far apart as the first set of leads. Further, Sutardja explicitly states that the distances between the high and low speed leads "may be irregular to increase or decrease coupling." (Ex. 1012, ¶139.) (Ex. 1002, ¶200.)

It would have been obvious to a POSITA to modify the distances of a first and second set of electrical contacts to "increase or decrease coupling" as disclosed by Sutardja and a spacing for the second set of at least twice as far apart as the first set, as inherently disclosed by Sutardja, would be obvious to try for a POSITA. (Ex. 1002, ¶201.)

A POSITA would have known that the spacing between the leads (electrical contacts) affects the coupling. Thus, such a person would have been motivated to modify the spacing of the leads to minimize cross talk and/or maintain impedance accuracy of such low and high speed leads. (Ex. 1002, ¶202.)

A POSITA implementing an IC package like that of the Okabe-AAPA-Rozenblit combination would have had good reason to look to Sutardja, particularly

because all of these references are in the same field of integrated circuit packages, include both high speed and low speed circuitry and/or include definitions of what a POSITA would have understood to be high and low speed. Having looked to Sutardja, such a POSITA would have been motivated to utilize spacing of the electrical contacts with characteristics suitable for connection with low speed circuitry as disclosed by Sutardja for the peripheral electrical contacts of the IC package of Okabe-AAPA-Rozenblit to ensure impedance accuracy and minimize cross-talk (increase or decrease coupling). (Ex. 1002, ¶203.)

Moreover, a POSITA would have found it straightforward to space the high and low speed leads as disclosed by Sutardja. Such an implementation would have simply been the application of a known device (IC with low speed contacts) to a similar device (IC) and would have produced predictable results (increase or decrease coupling). Therefore, the Okabe-AAPA-Rozenblit-Sutardja combination discloses or suggests this claim feature. (Ex. 1002, ¶204.)

2. Claim 5

Okabe in view of Applicant's Admitted Prior Art (AAPA), Rozenblit, and Sutardja discloses or suggests each and every element of dependent claim 5. (Ex. 1002, ¶205.)

a) "An IC package as recited in claim 1, wherein the low speed electronic circuitry is defined as circuity having serial transfer rates of less than about 1 Gigabits per second (Gb/s); and"

As discussed above in Section VII.C., the Okabe-AAPA-Rozenblit combination discloses an IC package with low speed electronic circuitry. Sutardja further discloses an integrated circuit die connected to low speed leads and high speed leads. (Ex. 1012, ¶[0139].) Sutardja further discloses that the high speed leads are operable to for high speed signals that are "greater than or equal to 1 Gigabit per second." (*Id.*, ¶[0075].) A POSITA would have understood that if high speed is greater than or equal to 1 Gb/s, than low speed would be "less than about 1 Gb/s." (Ex. 1002, ¶206.)

b) "wherein the high speed electronic circuitry is defined as circuity having serial transfer rates of greater than about 1 Gb/s."

As discussed above, Sutardja discloses an integrated circuit die connected to low speed leads and high speed leads. (Ex. 1012, ¶[0139].) Sutardja further discloses that the high speed leads are operable to for high speed signals that are "greater than or equal to 1 Gigabit per second." (*Id.*, ¶[0075].) (Ex. 1002, ¶207.)

However, a POSITA would take note that the '091 Patent does not provide any specific disclosure regarding any advantages, criticality, or unexpected results related to the specific speed of "greater than about 1 Gb/s [gigabits per second]" recited in claim 5. As has been shown in numerous contemporaneous references mentioned above, speeds of 1 Gb/s were well known in the art. (Ex. 1002, ¶208.)

Further, the Examiner did not give weight to these limitations as they were interpreted as "a recitation of the function/intended use" which "does not differentiate the claimed apparatus from a prior art apparatus." (Ex. 1004, pg. 369.) As such, any electronic circuitry would render this claim obvious to a POSITA. (Ex. 1002, ¶209.)

As discussed above, MPEP §2114 discloses in part "A claim containing a 'recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus' if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987)."

Thus, a POSITA would have understood that the apparatus of Okabe-AAPA-Rozenblit-Sutardja teaches all the structural limitations of claim 5, and thus claim 5 would have been obvious to a POSITA. (Ex. 1002, ¶210.)

3. Claim 6

Okabe in view of AAPA, Rozenblit, and Sutardja discloses or suggests each and every element of dependent claim 6. (Ex. 1002, ¶211.)

a) "An IC package as recited in claim 1 wherein the high speed electronic circuitry is defined as circuity having serial transfer rates of greater than about 8.5 Gb/s."

As discussed above in Section VII.C.1(e), the Okabe-AAPA-Rozenblit combination teaches an IC package with high speed circuitry. Further, Sutardja discloses an integrated circuit die connected to low speed leads and high speed leads.

(Ex. 1012, 0139.) The high speed leads are operable for high speed signals that are "greater than or equal to 1 Gigabit per second." (*Id.*, ¶[0075].) A POSITA would have understood that if high speed is greater than or equal to 1 Gb/s, that would include speeds of 8.5 Gb/s. (Ex. 1002, ¶212.)

A POSITA would take note that the '091 Patent does not provide any specific disclosure regarding any advantages, criticality, or unexpected results related to the specific speed of "greater than about 8.5 Gb/s" recited in claim 6. A POSITA would also take note that the '091 Patent does not provide any structural difference to the IC package or the high speed electronic circuitry in claims 5 and 6 when differentiating between purported high speed thresholds of 1 Gb/s in claim 5 and 8.5 Gb/s in claim 6. As has been shown in numerous contemporaneous references mentioned above, speeds of 1 Gb/s and 8.5 Gb/s were well known in the art. (Ex. 1002, ¶213.)

Further, the Examiner did not give weight to these limitations as they were interpreted as "a recitation of the function/intended use" which "does not differentiate the claimed apparatus from a prior art apparatus." (Ex. 1004, pg. 395.) As such, any electronic circuitry would render this claim obvious to a POSITA. (Ex. 1002, ¶214.)

As discussed above, MPEP §2114 discloses in part "[a] claim containing a 'recitation with respect to the manner in which a claimed apparatus is intended to be

employed does not differentiate the claimed apparatus from a prior art apparatus' if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987)."

Thus, a POSITA would have understood that the apparatus of Okabe-AAPA-Rozenblit-Sutardja teaches all the structural limitations of claim 6, and thus claim 6 would have been obvious to a POSITA. (Ex. 1002, ¶215.)

4. Claim 9

Okabe in view of AAPA, Rozenblit, and Sutardja discloses or suggests each and every element of dependent claim 9. (Ex. 1002, ¶216.)

a) "An IC package as recited in claim 1 wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with low speed circuitry, and"

b) "a second set of electrical contacts for electrical connection with high speed circuitry; and"

As discussed above, Sutardja discloses an integrated circuit (IC) package that includes an IC die having die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶ [0138]) and that the leads 620-1 through 620-4 "operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B." (*Id.* ¶ [0139].) (Ex. 1002, ¶217.)

A POSITA would have understood that "low speed leads" 620-1 through 620-4 would be "a first set of electrical contacts for electrical connection with low speed circuitry" and that "high speed leads" 620-5A through 620-6B would be "a second

set of electrical contacts for electrical connection with high speed circuitry." (Ex. 1002, ¶218.)

c) "wherein the electrical contacts are arranged such that, the first spacing between the contacts of the first set of electrical contacts is smaller than a second spacing between the contact of the second set of electrical contacts, thereby enabling greater contact density for the first set of electrical contacts."

Sutardja discloses various spacing between the low speed leads, the high speed leads, and between the low and high speed leads. This spacing "may be irregular to increase or decrease coupling." (*Id.*, ¶[0139].) Sutardja shows in Figure 10A that the spacing (d1) between the first set of electrical contacts is smaller than the spacing (d3) between the second set of electrical contacts. Thus, this inherent feature of Sutardja renders this limitation obvious. Further, it would have been obvious to a POSITA that the smaller spacing of the first set of electrical contacts (low speed leads) would be "enabling greater contact density for the first set of electrical contacts." (Ex. 1002, ¶219.)

A POSITA implementing an IC package that of Okabe-AAPA-Rozenblit would have had good reason to look to Sutardja as these references are in the same field of IC packages with circuit having different speeds. Having looked to Sutardja, such a POSITA would have been motivated to use the decreased spacing of Sutardja in order to enable more contacts for the Okabe-AAPA-Rozenblit IC package. (Ex. 1002, ¶220.)

Moreover, a POSITA would have found it straightforward to decrease spacing to enable more contact density for the low speed signals where spacing is generally not an issue due to less crosstalk issues with low speed signals. (Ex. 1002, ¶221.)

E. Okabe in Combination with AAPA, Rozenblit, Sutardja and Taggart Discloses or Suggests all the features of Claims 3, 4 and 7

1. Claim 3

Okabe in view of AAPA, Rozenblit, Sutardja, and Taggart discloses or suggests each and every element of dependent claim 3. (Ex. 1002, ¶222.)

a) "An IC package as recited in claim 2, wherein the first set of electrical contacts are spaced apart a distance of at least 70 um (micrometers)"

The Okabe-AAPA-Rozenblit-Sutardja-Taggart combination discloses or suggests this limitation. As discussed above in Section VII.D.1(a), the Okabe-AAPA-Rozenblit-Sutardja combination teaches an IC package with a first set of electrical contacts spaced to minimize cross talk and/or maintain impedance accuracy (increase or decrease coupling). (Ex. 1002, ¶223.)

Further, *Taggart* discloses a distance (pitch) between wire-bond pads, wire-bonds, and die bond pads within a range from about 10 micrometers to about 200 micrometers. (Ex., 1009, ¶[0027].) A POSITA working with the Okabe-AAPA-Sutardja IC package would look to Taggart as they are all in the integrated circuit packaging field. Moreover, a POSITA would have understood that any sets of Taggarts' wire-bond pads, wire-bonds, and die bond pads would be "electrical

contacts" and the 70 micrometers would be in the range of about 10-200 micrometers. Such a person would have been motivated to space electrical contacts of the IC package of Okabe-AAPA-Rozenblit-Sutardja with the ranges of Taggart to increase or decrease coupling which would minimize cross talk and/or maintain impedance accuracy for the electrical contacts as was very well known in the art. (Ex. 1002, ¶224.)

b) "and wherein the second set of electrical contacts are spaced apart a distance of at least 140 um (micrometers)"

As discussed above in Section VII.D.1(b), the Okabe-AAPA-Sutardja combination teaches an IC package with a second set of electrical contacts spaced to increase or decrease coupling. (Ex. 1002, ¶225.)

Further, *Taggart* discloses a distance (pitch) between wire-bond pads, wire-bonds, and die bond pads within a range from about 10 micrometers to about 200 micrometers (*Id.*, ¶[0027]), with a specific embodiment where the pitch is about 135 micrometers. (*Id.*, Claim 13.) A POSITA would have understood that any other of the sets of wire-bond pads, wire-bonds, and die bond pads would be second "electrical contacts" and the 140 micrometers would be in the range of about 10-200 micrometers and specifically "about 135 micrometers" as disclosed by Taggart. (Ex. 1002, ¶226.)

2. Claim 4

Okabe in view of AAPA, Rozenblit, Sutardja, and Taggart discloses or suggests each and every element of dependent claim 4. (Ex. 1002, ¶227.)

a) "An IC package as recited in claim 2, wherein the first set of electrical contacts are spaced apart a distance of at least 70 um (micrometers)"

The Okabe-AAPA-Rozenblit-Sutardja-Taggart combination discloses this claim feature. As discussed in Section VII.D.1 above, the Okabe-AAPA-Rozenblit-Sutardja combination discloses this claim feature. (Ex. 1002, ¶228.)

Taggart discloses a distance (pitch) between wire-bond pads, wire-bonds, and die bond pads within a range from about 10 micrometers to about 200 micrometers. (*Id.*, ¶[0027].) A POSITA would have understood that any sets of wire-bond pads, wire-bonds, and die bond pads would be "electrical contacts" and the 70 micrometers would be in the range of about 10-200 micrometers. Such a person would have been motivated to space electrical contacts to increase or decrease coupling to minimize cross talk and/or maintain impedance accuracy as was very well known in the art. (Ex. 1002, ¶229.)

b) "and wherein the second set of electrical contacts are spaced apart a distance of at least 200 um (micrometers)"

The Okabe-AAPA-Rozenblit-Sutardja-Taggart combination discloses this claim feature. Taggart discloses a distance (pitch) between wire-bond pads, wire-bonds, and die bond pads within a range from about 10 micrometers to about 200 micrometers (um), and gives a specific example of the wire-bond pads, the die bond pads, and the wire-bonds "spaced on 200 um centers." (*Id.*, 0027.) (Ex. 1002, ¶230.)

3. Claim 7

Okabe in view of AAPA, Rozenblit, Sutardja, and Taggart discloses or suggests each and every element of dependent claim 7. (Ex. 1002, ¶231.)

a) "An IC package as recited in claim 1 wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with low speed circuitry, and"

The Okabe-AAPA-Rozenblit-Sutardja-Taggart combination discloses or suggests this feature. As discussed above in Section VII.C.1. (a)-(d), the Okabe-AAPA combination teaches an IC package with peripheral electrical contacts for electrical connection with low speed circuitry. As shown below in Figure 10A, Sutardja discloses an integrated circuit (IC) package that includes an IC die having die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶ [0138].) and that the leads 620-1 through 620-4 "operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B". (*Id.* ¶[0139].) (Ex. 1002, ¶232.)

A POSITA would have understood that the leads operating at a lower speed would be a first set of electrical contacts for electrical connection with low speed circuitry. (Ex. 1002, ¶233.)

b) "a second set of electrical contacts for electrical connection with high speed circuitry, and"

The Okabe-AAPA-Rozenblit-Sutardja-Taggart combination discloses or suggests this feature. As shown below in Figure 10A, Sutardja discloses die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶ [0138]) and that the leads 620-1 through 620-4 "operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B." (*Id.* ¶[0139].) A POSITA would have understood that die pads 614-5A through 614-6B, bondwires 616-5A through 616-6B, and "high speed leads" 620-5A through 620-6B would be equivalent to "a second set of electrical contacts for electrical connection with high speed circuitry." A POSITA would have understood that die pads 614-1 through 614-4, bondwires 616-1 through 616-4, and "low speed leads" 620-1 through 620-4 would be equivalent to "a first set of electrical contacts for electrical connection with low speed circuitry." (Ex. 1002, ¶234.)

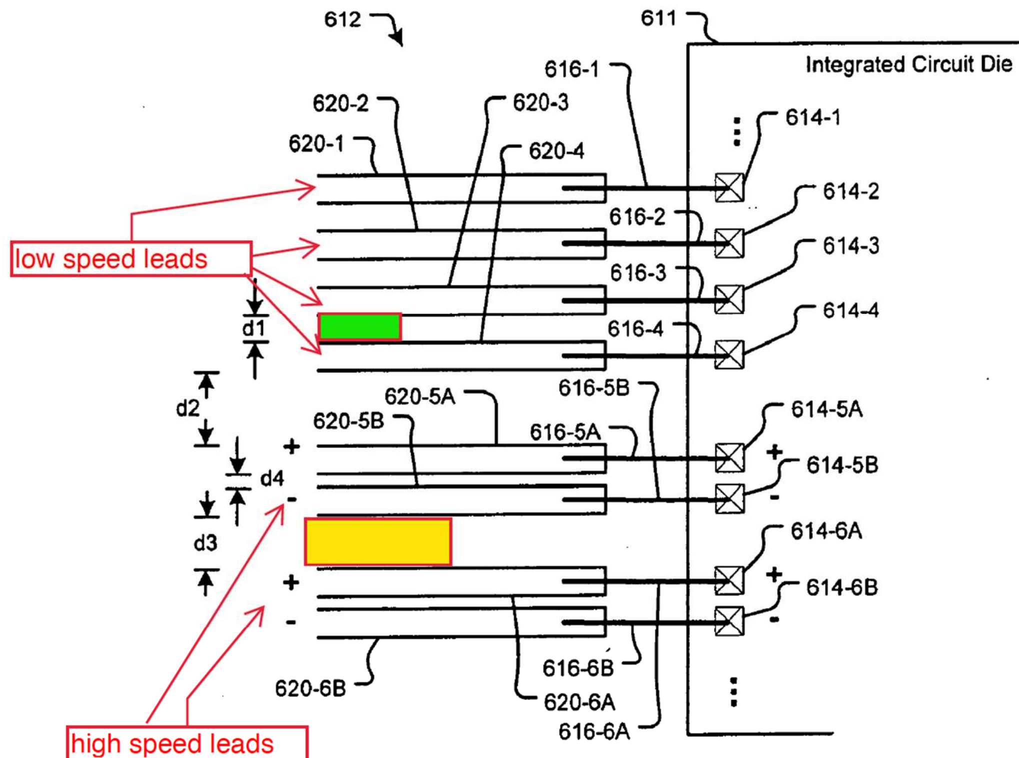


FIG. 10A

(Ex. 1012, FIG. 10A (annotated).)

c) “wherein the second set of electrical contacts are spaced apart at a distance that is at least three times as far apart as the spacing for the first set of electrical contacts.”

The Okabe-AAPA-Rozenblit-Sutardja-Taggart combination discloses or suggests this feature. Sutardja discloses various spacing between the low speed leads, the high speed leads, and between the low and high speed leads. Sutardja explicitly states that “this spacing “may be irregular to increase or decrease coupling.” (*Id.*, ¶[0139].) Sutardja implicitly shows in Figure 10A the spacing (d3)

between the second set of electrical contacts is larger than the spacing (d1) between the first set of electrical contacts. (Ex. 1002, ¶235.)

Taggart discloses an integrated circuit (IC) package that includes an IC die having die bond pads connected to wire-bond pads via bond wires. Taggart further discloses spacing any of the die bond pads, wire-bond pads, and bond wires in accordance with a pitch that ranges from "about 10 um [micrometers] to 200 um." (Ex. 1009, ¶27.) A POSITA would have understood that this range would include many pitch values that would be 3x greater than other pitch values in the ranges. For example, a first pitch value of 10um would leave 30 um-200 um values that would all be at least three times greater than 10 um. (Ex. 1002, ¶236.)

A POSITA would have good reason to look to Taggart to modify Sutardja to select values within 10 um-200 um to increase or decrease coupling between the high or low speed leads as needed. Because Taggart and Sutardja both disclose integrated circuit packages very similar to the Okabe-AAPA-Rozenblit combination, a POSITA implementing the IC package of Okabe-AAPA-Rozenblit would have good reason to look to Taggart and Sutardja. (Ex. 1002, ¶237.)

A POSITA would have understood that particular spacing between the leads for high speed and low speed would modify the coupling of signals as disclosed by Sutardja. Such a person would have a reasonable expectation of success in

implementing spacing as they were well-known and widely-implemented features of signal traces in integrated circuit packages. (Ex. 1002, ¶238.)

F. Okabe in Combination with Applicant's Admitted Prior Art (AAPA), Rozenblit, Sutardja, and Choi Discloses or Suggests all the features of Claims 8 and 11

1. Claim 8

Okabe in view of Applicant's Admitted Prior Art, Rozenblit, Sutardja, and Choi discloses or suggests each and every element of dependent claim 8. (Ex. 1002, ¶239.)

a) "An IC package as recited in claim 1, wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with low speed circuitry, and"

Under this presumption, as discussed above in Section VII.E.1(a), Sutardja discloses an integrated circuit (IC) package that includes an IC die having die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶ [0138]) and that the leads 620-1 through 620-4 "operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B" (*Id.* ¶ [0139].) A POSITA would have understood that any of die pads 614-1 through 614-4, bondwires 616-1 through 616-4, and "low speed leads" 620-1 through 620-4 would be "a first set of electrical contacts for electrical connection with low speed circuitry." (Ex. 1002, ¶240.)

b) "a second set of electrical contacts for electrical connection with high speed circuitry"

As discussed above in Section VII.E.1(b), Sutardja discloses die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶[0138].) and that the leads 620-1 through 620-4 "operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B" (*Id.* ¶ [0139]). A POSITA would have understood that die pads 614-5A through 614-6B, bondwires 616-5A through 616-6B, and "high speed leads" 620-5A through 620-6B would be "a second set of electrical contacts for electrical connection with high speed circuitry." (Ex. 1002, ¶241.)

c) "wherein the second set of electrical contacts are spaced apart at a distance sufficient to establish a differential impedance of at least 100 ohms between the contacts of the second set of electrical contacts."

Sutardja discloses spacing d4 between the high speed leads (second set of electrical contacts), and that the spacing can be changed to "increase or decrease coupling." (*Id.*, ¶ [0139].) (Ex. 1002, ¶242.)

Choi discloses a PBGA package having high speed differential traces designed to provide a 100 ohm differential impedance (Ex. 1011, p. 304). A POSITA would have been motivated to modify the IC package of Okabe-AAPA-Rozenblit with the spacing of Sutardja to achieve the 100 ohm differential impedance as taught by Choi. Such a person implementing the IC package of Okabe-AAPA-Rozenblit would have

looked to Sutardja and Choi as they are all in the same field of IC packages and/or wireless communication. Further, such a person would have known that such impedances are standard and thus would be an obvious design choice in accordance with MPEP §2144. (Ex. 1002, ¶243.)

2. Claim 11

Okabe in view of AAPA, Rozenblit, Sutardja, and Choi discloses or suggests each and every element of dependent claim 11. (Ex. 1002, ¶244.)

a) "An IC package as recited in claim 1 wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with low speed circuitry; and"

As discussed above in Section VII.E.1(a), Sutardja discloses an integrated circuit (IC) package that includes an IC die having die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶[0138].) and that the leads 620-1 through 620-4 "operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B" (*Id.*, ¶ [0139]). A POSITA would have understood that die pads 614-1 through 614-4, bondwires 616-1 through 616-4, and "low speed leads" 620-1 through 620-4 would be equivalent to "a first set of electrical contacts for electrical connection with low speed circuitry." (Ex. 1002, ¶245.)

b) "a second set of electrical contacts for electrical connection with high speed circuitry; and"

As discussed above in Section VII.E.1(b), Sutardja discloses die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶ [0138].) and that the leads 620-1 through 620-4 "operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B." (*Id.*, ¶ [0139].) A POSITA would have understood that die pads 614-5A through 614-6B, bondwires 616-5A through 616-6B, and "high speed leads" 620-5A through 620-6B would be equivalent to a second set of electrical contacts for electrical connection with high speed circuitry. (Ex. 1002, ¶246.)

c) "wherein the electrical contacts are arranged as part of I/O lines such that,"

Sutardja discloses die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶ [0138]) and that the leads 620-1 through 620-4 "operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B." (*Id.*, ¶ [0139].) (Ex. 1002, ¶247.)

d) "a first spacing between the contacts of the first set of electrical contacts is sufficient to establish a control differential impedance of at least 50Ω between the contacts of the first set of electrical contacts; and"

Sutardja discloses spacing d4 between the high speed leads (second set of electrical contacts), and that the spacing can be changed to "increase or decrease coupling." (*Id.*, ¶ [0139].) (Ex. 1002, ¶248.)

Further, Choi discloses, a multi-layered PCB that has a low-speed interconnects on layer 1 and that the low-speed signal transmission lines have characteristic impedances designed for 50 Ω (Ohms). (Ex. 1011, p. 304.) A POSITA implementing the Okabe-AAPA-Rozenblit-Sutardja IC package would have had good reason to look to Choi as they are all dealing with multilayered substrates and/or signaling from an integrated circuit. A POSITA implementing the Okabe-AAPA-Rozenblit-Sutardja IC package with spacing of a first set of electrical contacts would have good reason to Choi's low-speed transmission lines having characteristic impedances of 50 Ohms to avoid impedance mismatch, which was known to cause degradation of a signal. (Ex. 1002, ¶249.)

e) "a second spacing between the contacts of the second set of electrical contacts is sufficient to establish a control differential impedance of at least 100Ω between the contacts of the second set of electrical contacts"

Sutardja discloses spacing d4 between the high speed leads (second set of electrical contacts), and that the spacing can be changed to "increase or decrease coupling." (*Id.*, ¶ [0139].) (Ex. 1002, ¶250.)

Further, Choi discloses a multi-layered PCB that has a high-speed interconnects on layer 6 and that the high-speed signal transmission lines have characteristic impedances designed for 100 Ω (Ohms). (Ex. 1011, p. 304.) (Ex. 1002, ¶251.)

A POSITA would have good reason to modify the IC package of Okabe-AAPA-Rozenblit with the spacing of Sutardja and the characteristic impedance of Choi. Such a person would have been motivated to set the spacing to decrease or increase coupling as needed to maintain a specific impedance. (Ex. 1002, ¶252.)

G. Okabe in Combination with AAPA, Rozenblit, Sutardja, Choi, and Digital Design Discloses or Suggests all the features of Claim 10

1. Claim 10

Okabe in view of AAPA, Rozenblit, Sutardja, Choi, and Digital Design discloses or suggests each and every element of dependent claim 10. (Ex. 1002, ¶253.)

a) "An IC package as recited in claim 1 wherein the peripheral electrical contacts include "a first set of electrical contacts for electrical connection with low speed circuitry, and"

As discussed above in Section VII.D.1(a), Sutardja discloses an integrated circuit (IC) package that includes an IC die having die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶ [0138]) and that the leads 620-1 through 620-4 "operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B." (*Id.* ¶ [0139].) A POSITA would have understood that die pads 614-1 through 614-4, bondwires 616-1 through 616-4, and "low speed leads" 620-1 through 620-4 would be a first set of electrical contacts for electrical connection with low speed circuitry. (Ex. 1002, ¶254.)

b) "a second set of electrical contacts for electrical connection with high speed circuitry, and"

As discussed above in Section VII.D.1(b), Sutardja discloses die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶ [0138]) and that the leads 620-1 through 620-4 "operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B." (*Id.* ¶ [0139].) A POSITA would have understood that die pads 614-5A through 614-6B, bondwires 616-5A through 616-6B, and "high speed leads" 620-5A through 620-6B would be "a second set of electrical contacts for electrical connection with high speed circuitry." (Ex. 1002, ¶255.)

c) "wherein the electrical contacts are arranged as part of I/O lines such that,"

Sutardja discloses die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B for transmitting and receiving signals. (Ex. 1012, ¶¶ [0004], [0138].) (Ex. 1002, ¶256.)

d) "a first spacing between the contacts of the first set of electrical contacts is sufficient to establish a control differential impedance of at least 50Ω between the contacts of the first set of electrical contacts to substantially eliminate cross-talk between I/O lines for the low speed electronic circuitry; and"

Sutardja discloses spacing d1 between the low speed leads (first set of electrical contacts), and that the spacing can be changed to "increase or decrease coupling." (*Id.*, ¶ [0139].) (Ex. 1002, ¶257.)

Choi discloses, a multi-layered PCB that has a low-speed interconnects on layer 1 and that the low-speed signal transmission lines have characteristic impedances designed for 50 Ω (Ohms). (Ex. 1011, p. 304.) (Ex. 1002, ¶258.)

Digital Design discloses in Figure 5.4, shown below, that the spacing of signal traces affects crosstalk. (Ex. 1010, p. 192.) (Ex. 1002, ¶259.)

$$\text{Crosstalk} \approx \frac{K}{1+(D/H)^2} \qquad [5.2]$$

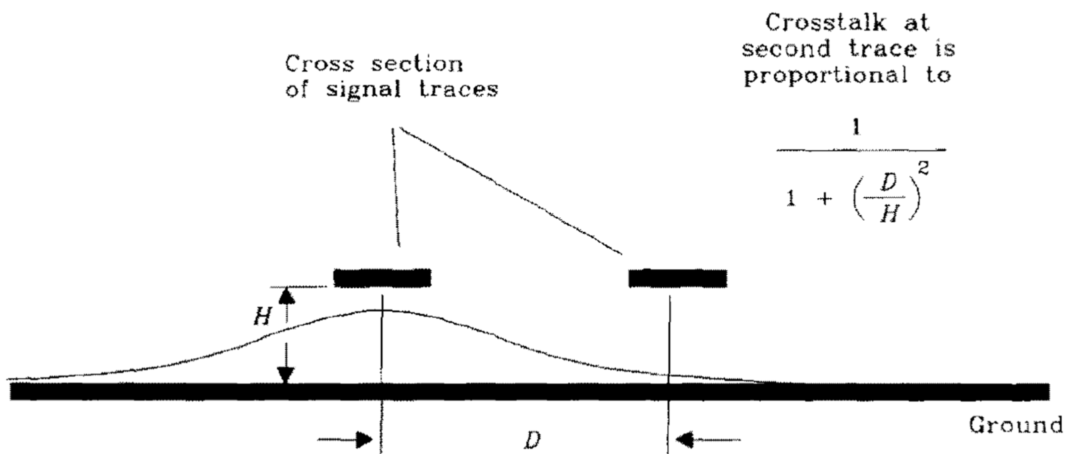


Figure 5.4 Cross section of two traces showing crosstalk.

(*Id.*, FIG. 5.4.)

Digital Design further shows in Figure 5.20, shown below, measuring cross talk for lines having a 50 Ohm characteristic impedance. (Ex. 1002, ¶260.)

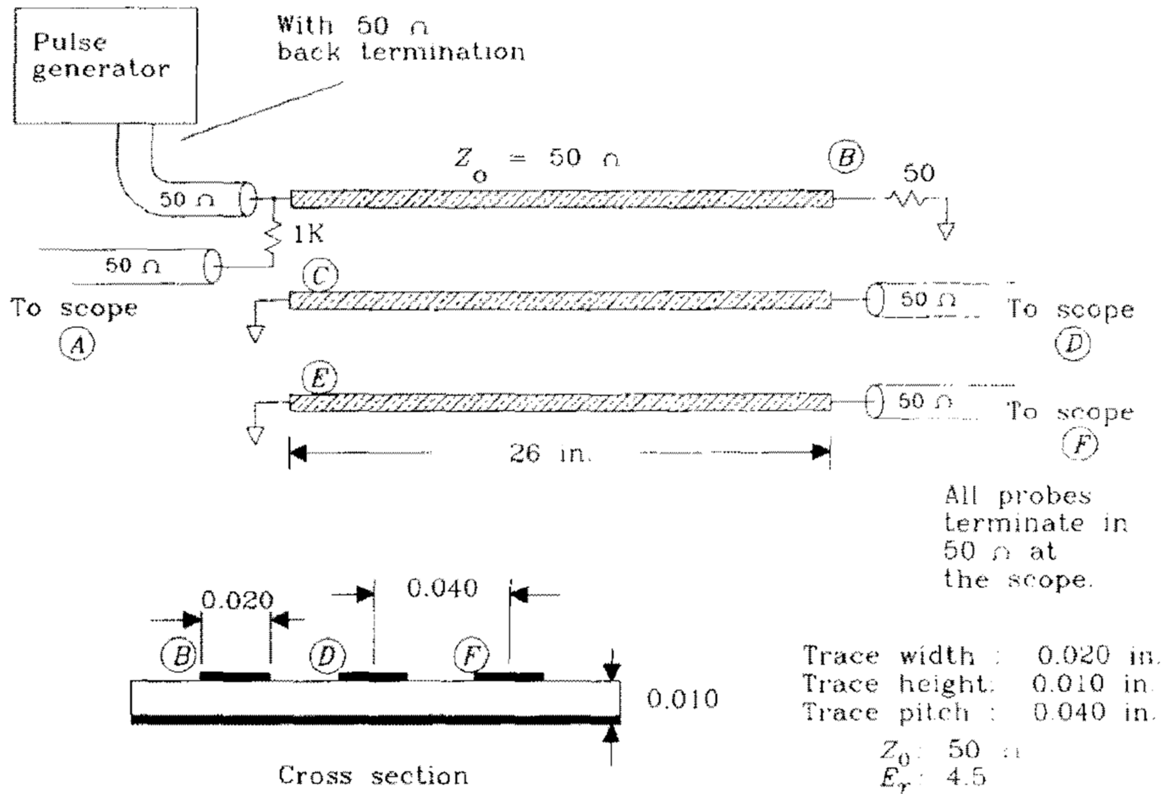


Figure 5.20 Setup for reflected reverse crosstalk measurement.

(*Id.*, FIG. 5.20.)

A POSITA implementing the IC package of Okabe-AAPA-Rozenblit would have good reason to look at Choi, Digital Design, and Sutardja to modifying the spacing of signal lines of Sutardja to achieve a 50 Ohm impedance as taught by Choi and Digital Design as they are all related to IC packages and/or signal characteristics. Such a person would have been motivated to optimize the spacing as it was widely known in the art that spacing would affect the cross talk as disclosed by Digital Design. (Ex. 1002, ¶261.)

e) "a second spacing between the contacts of the second set of electrical contacts is sufficient to establish a control differential impedance of at least 100Ω between the contacts of the second set of electrical contacts to substantially eliminate cross-talk between I/O lines for the high speed electronic circuitry."

Sutardja discloses spacing d4 between the high speed leads (second set of electrical contacts), and that the spacing can be changed to "increase or decrease coupling." (*Id.*, ¶ [0139].) (Ex. 1002, ¶262.)

Choi discloses, a multi-layered PCB that has a high-speed interconnects on layer 6 and that the high-speed signal transmission lines have characteristic impedances designed for 100 Ω (Ohms). (Ex. 1011, p. 304.) (Ex. 1002, ¶263.)

As discussed above with reference to Section VII.I.1(d), Digital Design discloses it was well known that spacing of signal traces affects crosstalk. (Ex. 1010, p. 192.) As such, a POSITA would have been motivated to implement Choi's 100 Ohm characteristic impedance for high speed transmission lines, and the spacing of Digital Design and Sutardja to optimize coupling in order to substantially eliminate cross-talk as was widely known in the art. Such a person implementing the IC package of Okabe-AAPA-Rozenblit would have good reason to look to Sutardja, Choi, and Digital Design as they all relate to IC packaging, wireless communication and/or signal trace spacing optimization. (Ex. 1002, ¶264.)

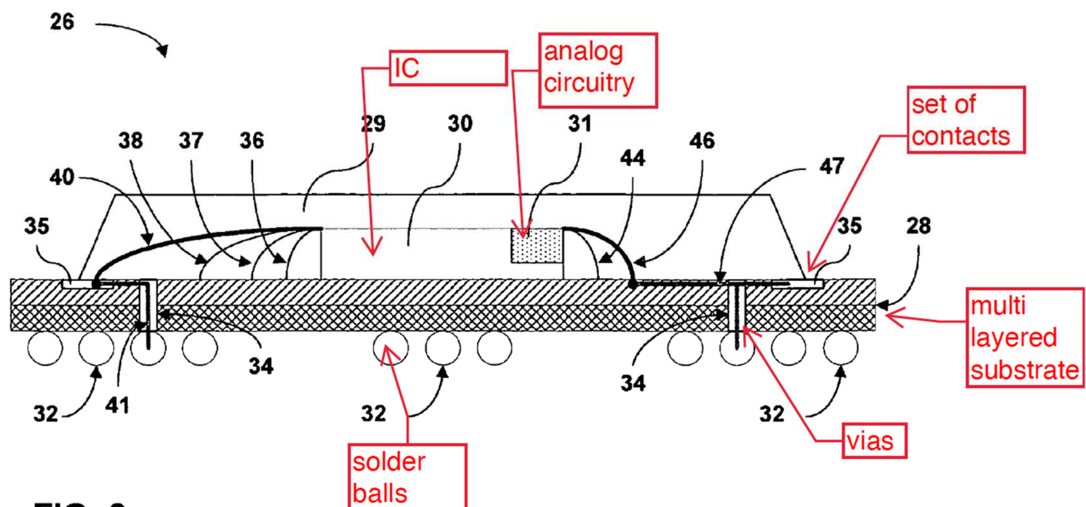
H. Okabe in Combination with AAPA, Rozenblit, Kramer and Sutardja Disclose or Suggest all the features of Claim 13

Okabe in view of AAPA, Rozenblit, Kramer, and Sutardja, discloses or suggests each and every element of dependent claim 13. (Ex. 1002, ¶265.)

1. Claim 13

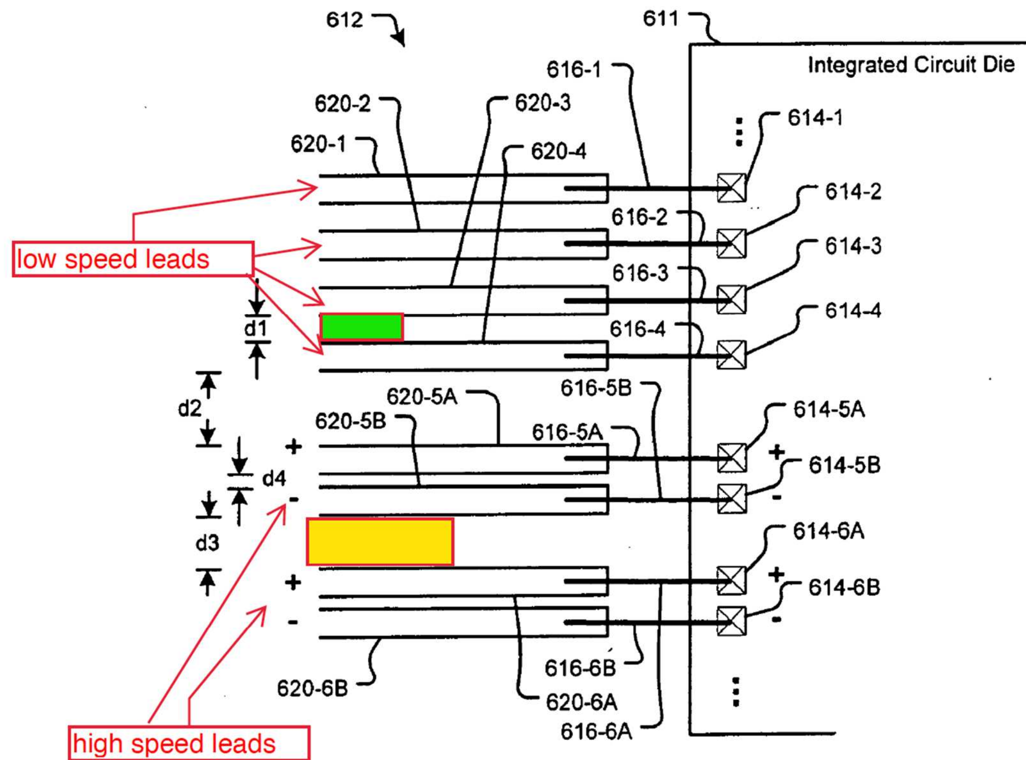
a) "An IC package as recited in claim 12, wherein the die arrangement comprises a die having both high-speed electronic circuitry and low-speed electronic circuitry; and"

Kramer shows in Figure 3, below, an integrated circuit 30 having a portion of the IC being analog circuitry 31. (Ex. 1007, 2:47-57.) The analog circuitry transmits high-speed differential signals, with speeds over 4.25 Gb/s, via a shortened wire bond 46, while wire bond 40 transmits input/output signals from the other portions of the IC 30. (*Id.*, 11:14-23.) (Ex. 1002, ¶266.)



(Ex. 1007, FIG. 3 (annotated).)

A POSITA would have understood that analog circuitry operating at speeds of 4.25 Gb/s and above with specific isolated routing of these signals via separate wirebonds, would indicate that the other portions of the IC would not operate at those speeds and thus either the analog or the other portions (whichever has lower speeds), would include "low speed circuitry." (Ex. 1002, ¶267.)



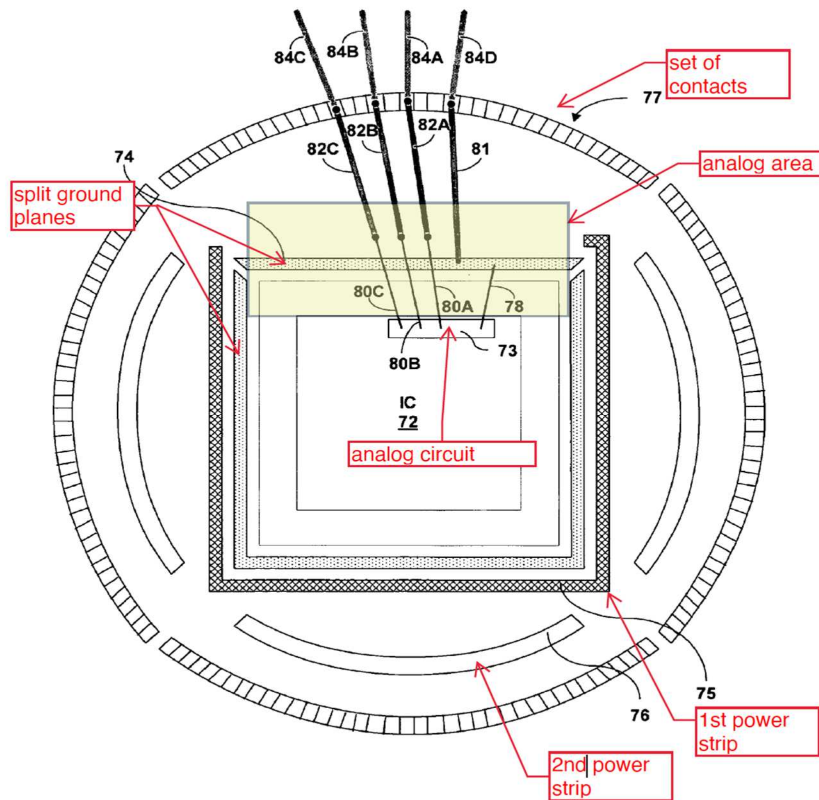
(Ex. 1012, FIG. 10A (annotated).)

b) "wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with low speed circuitry; and a second set of electrical contacts for electrical connection with high speed circuitry; and"

Sutardja discloses peripheral electrical contacts including high speed leads and low speed leads, shown above, where a first set of electrical contacts (620-1 to 620-4) are utilized for electrical connection with low speed circuitry, and a second set of electrical contacts (620-5A to 620-6B) are utilized for electrical connection with high speed circuitry. (Ex. 1012, ¶ [0139].) (Ex. 1002, ¶268.)

c) "wherein the low-speed electronic circuitry is connected with the first ground plane and is electrically connected with the first set of electrical contacts that are spaced for connection with the low speed electronic circuitry; and"

Kramer discloses in Figure 6, shown below, that an IC circuit 72 includes an analog circuit 73 that is connected with a first portion of ground plane 74 that is separated from the remaining portion of ground plane 74 outside the analog area. Kramer discloses the analog circuitry operates at higher speeds (e.g., 4.25 Gb/s and above). (Ex. 1007, 1:38-41.) Kramer also discloses the IC 72 (the non-analog portions) is connected to electrical contacts 77 outside the analog area and discloses wire bonds outside of the analog area of the BGA package couple IC 72 to ground 74, power stripes 75 and 76, and the set of contacts 77. (*Id.*, 8:33-63.) Analog circuit 73 of IC 72 requires isolated power and ground connections to avoid introducing noise from other circuits on IC 72 into analog circuit 73. (Ex. 1007, 8:60-66.) (Ex. 1002, ¶269.)



(Ex. 1007, FIG. 6 (annotated).)

A POSITA would have understood the IC operating at lower speeds than the analog circuit 73 would be low speed circuity, and that the IC 72 being connected to the portion of the ground plane 74 outside the analog area would be a first ground plane. (Ex. 1002, ¶270.)

Sutardja clearly shows in Figure 10A that low speed leads are spaced closer together than high speed leads. Sutardja further discloses that spacing between the leads may be changed to “increase or decrease coupling. (Ex. 1012, ¶ [0139].) (Ex. 1002, ¶271.)

As such, a POSITA would have understood spacing of lines and contacts affects coupling, and would have been motivated to space such low speed leads in order to minimize cross-talk and/or maintain impedance accuracy of the contacts as taught by Sutardja. (Ex. 1002, ¶272.)

d) "wherein the high-speed electronic circuitry is connected with the second ground plane and is electrically connected with the second set of electrical contacts that are spaced for connection with the high speed electronic circuitry."

Kramer discloses in Figure 6, shown above, analog circuitry 73 connected with a first portion of ground plane 74 that is separated from the remaining ground plane 74 outside the analog area. (Ex.1007, FIG. 6.) Kramer discloses the analog circuitry 73 operates at higher speeds (e.g., 4.25 Gb/s and above). (*Id.*, 1:35-42.) (Ex. 1002, ¶273.)

Further, Sutardja shows in Figure 10A, shown above, that the spacing for the high speed leads (second set of electrical contacts) is greater than spacing for low speed leads (first set of electrical contacts). Sutardja further discloses spacing may be irregular to "increase or decrease coupling." (Ex. 1012, ¶ 0139.) (Ex. 1002, ¶274.)

As such, a POSITA implementing the IC package of Okabe-AAPA-Rozenblit would have good reason to look to Kramer and Sutardja as they are all in the field of IC packaging. Moreover, a POSITA would have understood that a particular spacing for Kramer's high speed contacts would affect a particular impedance and

minimize cross talk, and thus it would have been straightforward to modify spacing of the high speed contacts as taught by Sutardja. (Ex. 1002, ¶275.)

I. Okabe in Combination with AAPA, Rozenblit Conn, Kramer and Sutardja Disclose or Suggest all the features of Claim 14

Okabe in view of AAPA, Rozenblit, Conn, Kramer, and Sutardja disclose or suggest each and every element of dependent claim 14. (Ex. 1002, ¶276.)

1. Claim 14

a) "An IC package as recited in claim 12, wherein the die arrangement comprises a stacked die arrangement"

As discussed in Section VII.C.2(a) above, Okabe-AAPA-Rozenblit discloses an IC package with an IC die. (Ex. 1002, ¶277.)

Further, Conn illustrates a stacked die arrangement in Figure 2 shown below. For example, analog power regulator die 73 is stacked on FPGA die 49. (Ex. 1013, 1:35-54.) (Ex. 1002, ¶278.)

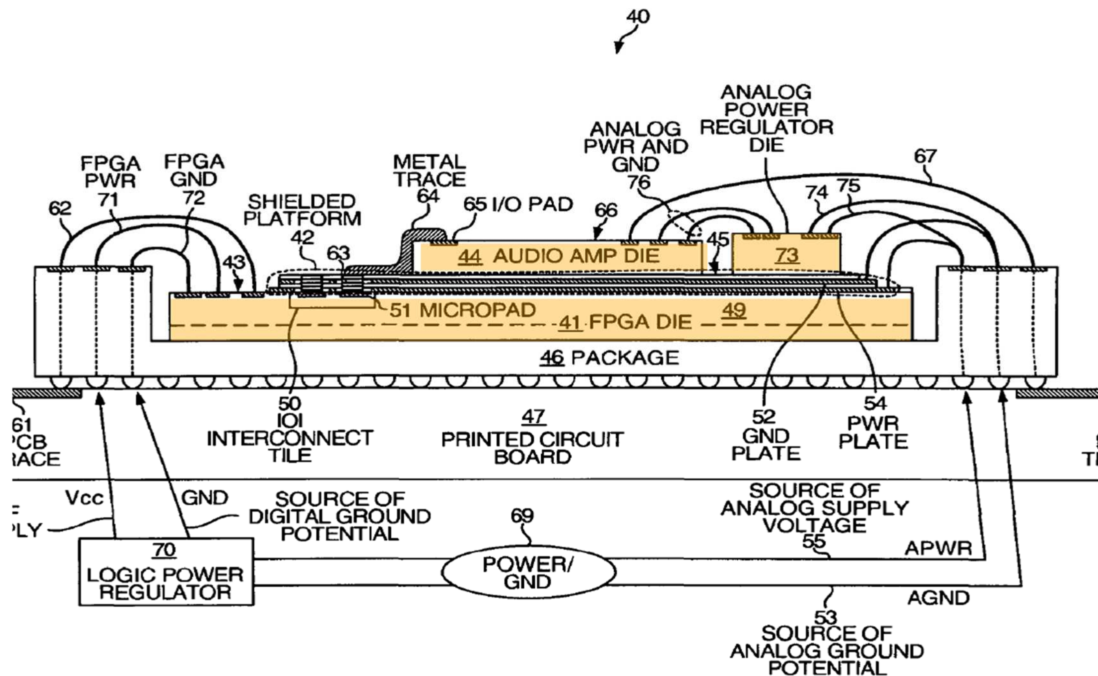


FIG. 2

(Ex. 1013, FIG. 2 (annotated).)

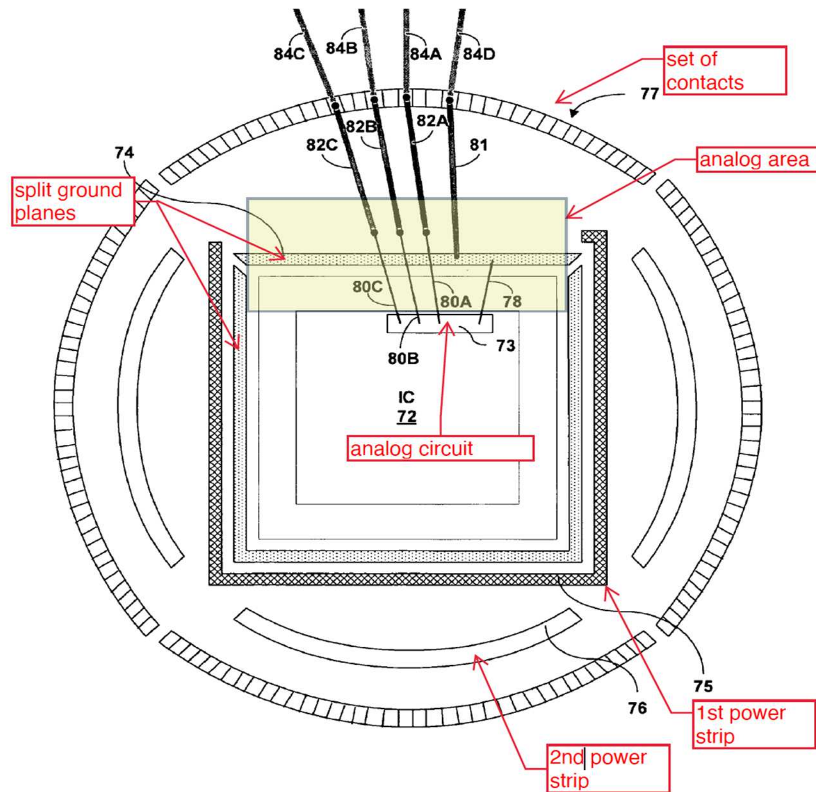
b) “wherein at least one die has high-speed electronic circuitry and wherein at least one die has low-speed electronic circuitry;”

Conn discloses in an example that the analog power regulator die 73 operates at a lower frequency than the underlying FPGA die 49. (*Id.*, 6:30-50.) As such, a POSITA would have understood that a die being capable of operating at a higher frequency than the other would indicate one die having high-speed electronic circuitry and the other die having low speed electronic circuitry. (Ex. 1002, ¶279.)

c) "wherein the low-speed electronic circuitry is connected with the first ground plane and is electrically connected with the first set of electrical contacts that are spaced for connection with the low-speed connection with the low speed electronic circuitry; and"

Kramer discloses in Figure 6, shown below, an IC 72 is connected with a first portion of ground plane 74 that is separated from the remaining ground plane 74 outside the analog area. Kramer further discloses the analog circuitry operates at higher speeds (e.g., 4.25 Gb/s and above). (Ex. 1007, 1:35-42.) Kramer also discloses the IC 72 is connected to electrical contacts 77 outside the analog area. (Ex. 1002, ¶280.)

A POSITA would have understood the IC operating at lower speeds than the analog circuit 73 would be low speed circuity, and that the IC 72 being connected to the portion of the ground plane 74 outside the analog area would be a first ground plane. (Ex. 1002, ¶281.)



(Ex. 1007, FIG. 6 (annotated).)

However, Sutardja clearly shows in Figure 10A that low speed leads are spaced closer together than high speed leads. Sutardja further discloses that spacing between the leads may be changed to "increase or decrease coupling. (Ex. 1012, ¶ [0139].) (Ex. 1002, ¶282.)

As such, a POSITA would have understood spacing of lines and contacts affects coupling, and would have been motivated to space such low speed leads in order to minimize cross-talk and/or maintain impedance accuracy of the contacts. (Ex. 1002, ¶283.)

d) "wherein the high-speed electronic circuitry is electronic connected with the second ground plane and is electrically connected with the second set of electrical contacts that are spaced for connection with the high speed electronic circuitry."

Kramer discloses in Figure 6, shown above, analog circuitry 73 connected with a first portion of ground plane 74 that is separated from the remaining ground plane 74 outside the analog area. Kramer discloses the analog circuitry 73 operates at higher speeds (e.g., 4.25 Gb/s and above). (Ex. 1002, ¶284.)

Further, Sutardja shows in Figure 10A above, that the spacing for the high speed leads (second set of electrical contacts) is greater than spacing for low speed leads (first set of electrical contacts). Sutardja further discloses spacing may be irregular to "increase or decrease coupling." (Ex. 1012, ¶ 0139.) (Ex. 1002, ¶285.)

As such, a POSITA implementing the IC package of Okabe-AAPA-Rozenblit would have good reason to look to Conn, Kramer and Sutardja as they are all in the field of IC packaging. Moreover, a POSITA would have understood that a particular spacing for Kramer's high speed contacts would affect a particular impedance and minimize cross talk, and thus it would have been straightforward to modify spacing of the high speed contacts as taught by Sutardja. (Ex. 1002, ¶286.)

A POSITA implementing the IC package of Okabe-AAPA-Rozenblit, would have good reason to look at Conn, Sutardja, and Kramer as they all are in the similar

fields of IC packaging, having multi-layered substrates and/or spacing of signal lines. (Ex. 1002, ¶287.)

Such an implementation would have simply been the application of a known device (IC package with multiple IC dies) to a similar device (stacked IC dies) and would have produce predictable results of saving space on the package as taught by Conn. (Ex. 1013, 4:28.) Therefore, the Okabe-AAPA-Rozenblit-Conn-Sutardja-Kramer combination discloses or suggests this claim feature. (Ex. 1002, ¶288.)

Further, as discussed above, MPEP §2114 discloses in part "A claim containing a 'recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus' if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987)."

Thus, a POSITA would have understood that the apparatus of Okabe-AAPA-Rozenblit-Conn-Sutardja-Kramer teaches all the structural limitations of claim 14 and thus claim 14 would have been obvious to a POSITA. (Ex. 1002, ¶289.)

VIII. THIS REQUEST IS NOT REDUNDANT AND SHOULD NOT BE DENIED UNDER 35 U.S.C. § 325(D)

As discussed in Sections I, III, IV and V above, the Office has never considered any of the grounds or arguments that are advanced in this request, either during original examination, or in the NXP IPR against the '091 Patent. In particular, the Office has never considered the combination of Miller and Hashemi; or the

combination of Okabe, Hashemi, and Rozenblit; or the combination of Okabe, AAPA, and Rozenblit; and as well as the other Grounds as set forth in this Request.

As such, the prior art grounds presented in this Request have not been considered by the Office and are not unduly cumulative to references that have been considered. Thus, denial under 35 U.S.C. §325(d) is not warranted.

For at least the reasons discussed above, the Office should provide Third-Party Requester with an opportunity to challenge the ’091 Patent.

IX. CONCLUSION

For the foregoing reasons, substantial new questions of patentability are raised in connection with the Challenged Claims, by the Request for *ex parte* Reexamination, because the Challenged Claims are rendered obvious in view of the above-listed prior art references. Therefore, Requester asks that this Request for Reexamination be granted and that the Challenged Claims be canceled. As identified in the attached Certificate of Service and in accordance with 37 C.F.R. §§ 1.33(c) and 1.510(b)(5), a copy of the present Request, in its entirety, is being served to the address of the attorney or agent of record.

Please direct all correspondence in this matter to the undersigned.

RESPECTFULLY SUBMITTED,

Dated: August 6, 2024 By: /Timothy D. Taylor/Reg. No. 76,643
Timothy D. Taylor

Attorney for Third Party Requester NXP

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CERTIFICATE OF SERVICE

The undersigned certifies that copies of the following:

1. Request for *Ex Parte* Reexamination Transmittal Form for U.S. Patent No. 7,646,091;
2. Request for *Ex Parte* Reexamination of U.S. Patent No. 7,646,091;
3. Information Disclosure Statement by Requester; and
4. Exhibits 1001-1015, which includes a copy of the patent to be reexamined and any certificate of correction;

in their entirety were served on the attorney of record for the assignee of U.S. Patent No. 7,646,091, in accordance with 37 C.F.R. § 1.510(b)(5), on August 6, 2024, by the U.S. Postal Service Priority Express Mail.

Mendelsohn Dunleavy, P.C.
1500 John F. Kennedy Blvd., Ste. 910
Philadelphia, PA 19102

Respectfully Submitted,

Dated: August 6, 2024 By: /Timothy D. Taylor/Reg. No. 76,643

Timothy D. Taylor
Attorney for Third Party Requester NXP