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UNITED STATES DISTRICT COURT  
CENTRAL DISTRICT OF CALIFORNIA

POLARIS POWERLED  
TECHNOLOGIES, LLC,

Plaintiff,

v.

WESTERN DIGITAL CORPORATION,  
WESTERN DIGITAL TECHNOLOGIES,  
INC., NEWEGG, INC., ZONES, LLC, and  
PRIVATE LABEL PC, LLC,

Defendants.

Case No. 2:24-cv-02864-ODW-MAR

**FIRST AMENDED COMPLAINT  
FOR PATENT INFRINGEMENT**

**DEMAND FOR JURY TRIAL**

1 Plaintiff Polaris PowerLED Technologies, LLC (“Plaintiff” or “Polaris”)  
2 brings this patent infringement action against Defendants Western Digital  
3 Corporation; Western Digital Technologies, Inc.; Newegg, Inc.; Zones, LLC; and  
4 Private Label PC, LLC (collectively, “Defendants”) as follows:

5 **NATURE OF THE ACTION**

6 1. This is a civil action for infringement of U.S. Patent Nos. 8,554,968  
7 (“the ’968 Patent”), 9,183,085 (“the ’085 Patent”), and 8,601,346 (“the ’346 Patent”),  
8 (collectively, “Asserted Patents”), and under the patent laws of the United States, 35  
9 U.S.C. § 1 *et seq.*

10 2. The technology in this case involves flash memory. Flash memory is  
11 used in, among other things, computing, gaming, data storage, and e-commerce. The  
12 ability of solid-state flash memory to hold electric charges without moving parts has  
13 revolutionized how information is stored and has resulted in great improvements over  
14 older memory technologies. These electrical charges, held in miniscule transistors,  
15 are used to read, store, and write enormous amounts of information in small,  
16 lightweight memory products that have transformed the daily lives of consumers.

17 3. Defendants’ infringing devices are its solid-state drive (“SSD”)  
18 products (“the Accused Products” or “the infringing devices”).

19 4. Western Digital is among the largest manufacturers of memory products  
20 in the United States.

21 5. Plaintiff brings this patent infringement action to protect its valuable  
22 patented technology specifically relating to (1) nonvolatile memory controllers  
23 (NVMCs) and SSDs; (2) interrupt techniques used in NVMCs and SSDs; (3) how  
24 NVMCs and SSDs adaptively select among error correction coding (ECC) schemes;  
25 and (4) how NVMCs and SSDs generate parity data using a distributed processing  
26 technique.

27 6. The Defendants control, participate in the commission of, and have a  
28 direct financial interest in the infringing acts set forth herein.

**THE PARTIES**

**Polaris**

7. Polaris is a California limited liability company having its address at 5150 E. Pacific Coast Highway, Suite 200, Long Beach, California 90804.

**Western Digital**

8. As used in this Complaint, Defendants Western Digital Corporation and Western Digital Technologies, Inc. are collectively referred to as “Western Digital.”

9. On information and belief, Defendant Western Digital Corporation is a Delaware corporation having offices in this District at 3355 Michelson Drive, Suite 100, Irvine, California 92612. Western Digital Corporation is registered with the California Secretary of State to do business in California and can be served through its registered agent, CSC - Lawyers Incorporating Service, 2710 Gateway Oaks Drive, Sacramento, California 95833.

10. On information and belief, Defendant Western Digital Technologies, Inc. is a subsidiary of Western Digital Corporation. Western Digital Technologies, Inc. is a Delaware corporation having offices in this District at 3355 Michelson Drive, Suite 100, Irvine, California 92612. Western Digital Technologies, Inc. is registered with the California Secretary of State to do business in California and can be served through its registered agent, CSC - Lawyers Incorporating Service, 2710 Gateway Oaks Drive, Sacramento, California 95833.

**Newegg**

11. On information and belief, Defendant Newegg, Inc. (“Newegg”) is a corporation formed under the laws of Delaware, with its principal place of business at 17560 Rowland Street, City of Industry, California 91748, which is located in this District.

12. Western Digital advertises Newegg as a “preferred Western Digital authorized partner.” See <https://www.westerndigital.com/company/distributors>.

13. On information and belief, Newegg sells and offers for sale the Accused

1 Products. On information and belief, Newegg provides services that help customers  
 2 in this District build computers that contain the Accused Products, including  
 3 providing a service called “PC Builder” on its website. See  
 4 <https://www.newegg.com/tools/custom-pc-builder>.

### 5 Zones

6 14. On information and belief, Defendant Zones, LLC (“Zones”) is a  
 7 corporation formed under the laws of the State of Washington, with offices at 13915  
 8 Cerritos Corporate Drive, Cerritos, California 90703, which is located in this District.  
 9 Zones is registered with the California Secretary of State to do business in California  
 10 and can be served through its registered agent, CSC - Lawyers Incorporating Service,  
 11 2710 Gateway Oaks Drive, Sacramento, California 95833.

12 15. Western Digital advertises Zones as a “preferred Western Digital  
 13 authorized partner.” See <https://www.westerndigital.com/company/distributors>.

14 16. On information and belief, Zones sells and offers for sale the Accused  
 15 Products. On information and belief, Zones provides services that help customers in  
 16 this District implement infringing functionality in the Accused Products. For  
 17 instance, Zones describes itself as follows: “We’re a global provider of  
 18 comprehensive IT services and solutions, reaching 100-plus countries and employing  
 19 2,000-plus people worldwide. ... We help organizations of all sizes succeed with  
 20 custom IT services and solutions for business, healthcare, government, and  
 21 education, plus market verticals like retail, utilities, and financial services, to name a  
 22 few. ... We architect solutions that simplify the complex and meet your individual  
 23 business needs and goals.” See  
 24 [https://www.zones.com/site/statics/static\\_page.html?name=about-us](https://www.zones.com/site/statics/static_page.html?name=about-us).

### 25 PLPC

26 17. On information and belief, Defendant Private Label PC, LLC (“PLPC”)  
 27 is a corporation formed under the laws of the State of California with its principal  
 28 place of business at 748 Epperson Drive, City of Industry, California 91748, which

1 is located in this District. PLPC is registered with the California Secretary of State  
2 to do business in California and can be served through its registered agent, Jonathan  
3 Wang, 748 Epperson Drive, City of Industry, California 91748.

4 18. Western Digital advertises PLPC as a “preferred Western Digital  
5 authorized partner.” See <https://www.westerndigital.com/company/distributors>.

6 19. On information and belief, PLPC sells and offers for sale the Accused  
7 Products. On information and belief, PLPC provides services that help customers in  
8 this District implement infringing functionality in the Accused Products. For  
9 instance, PLPC describes itself as follows: “PLPC delivers the most efficient  
10 technology solutions to the Gaming, Cloud, HPC, Security & Surveillance, and  
11 Consumer Electronics markets. PLPC distributes technology products from many of  
12 the world’s leading manufacturers and provides solutions to value-added resellers,  
13 DMR, retailers, and thousands of integrators for PC, surveillance, platform enterprise  
14 in the U.S., and Latin America. PLPC has successfully penetrated 18 countries in  
15 Latin America with in-country sales support. *As part of their value-added services,*  
16 *PLPC provides a variety of integration, including product lifecycle support, contract*  
17 *design, and assembly.* In addition, PLPC provides a wide range of financial options  
18 to ensure that our partners always have the resources in place to win business.” See  
19 <https://www.plpc.com/company> (emphasis added).

## 20 **JURISDICTION AND VENUE**

21 20. Plaintiff incorporates by reference and re-alleges the foregoing  
22 paragraphs as fully set forth herein.

23 21. This action arises under the patent laws of the United States, Title 35 of  
24 the United States Code. Accordingly, this Court has subject matter jurisdiction under  
25 28 U.S.C. §§ 1331 and 1338(a).

## 26 **Western Digital**

27 22. On information and belief, Western Digital transacts and conducts  
28 business in this District and the State of California and is subject to the personal

1 jurisdiction of this Court. On information and belief, Western Digital has minimum  
2 contacts within the State of California and this District and has purposefully availed  
3 itself of the privileges of conducting business in the State of California and in this  
4 District. Polaris' causes of action arise directly from Western Digital's business  
5 contacts and other activities in the State of California and in this District.

6 23. On information and belief, Western Digital has committed acts of  
7 infringement within this District and the State of California by, *inter alia*, making,  
8 importing, using, selling, and/or offering for sale Accused Products that infringe one  
9 or more claims of the Asserted Patents. More specifically, Western Digital, directly  
10 and/or through intermediaries or agents, makes, imports, uses, sells, ships,  
11 distributes, offers for sale, advertises, and/or otherwise promotes infringing Accused  
12 Products in the United States, the State of California, and this District.

13 24. Venue is proper in this District under 28 U.S.C. §§ 1391(b), (c) and  
14 1400(b), including based on Western Digital's physical presence in this District  
15 and/or Western Digital's transaction of business in this District directly and/or  
16 through its affiliates and customers and/or acts of patent infringement in this District.

17 **Newegg**

18 25. On information and belief, Newegg, Inc. ("Newegg") transacts and  
19 conducts business in this District and the State of California and is subject to the  
20 personal jurisdiction of this Court. On information and belief, Newegg has minimum  
21 contacts within the State of California and this District and has purposefully availed  
22 itself of the privileges of conducting business in the State of California and in this  
23 District. Polaris' causes of action arise directly from Newegg's business contacts and  
24 other activities in the State of California and in this District.

25 26. On information and belief, Newegg has committed acts of infringement  
26 within this District and the State of California by, *inter alia*, making, importing,  
27 using, selling, and/or offering for sale Accused Products that infringe one or more  
28 claims of the Asserted Patents. More specifically, on information and belief, Newegg,

1 directly and/or through intermediaries or agents, makes, imports, uses, sells, ships,  
2 distributes, offers for sale, advertises, and/or otherwise promotes infringing Accused  
3 Products in the United States, the State of California, and this District.

4 27. Venue is proper in this District under 28 U.S.C. §§ 1391(b), (c) and  
5 1400(b), including based on Newegg's physical presence and the location of its  
6 offices and headquarters in this District and/or Newegg's transaction of business in  
7 this District directly and/or through its affiliates and customers and/or acts of patent  
8 infringement in this District.

9 **Zones**

10 28. On information and belief, Zones transacts and conducts business in this  
11 District and the State of California and is subject to the personal jurisdiction of this  
12 Court. On information and belief, Zones has minimum contacts within the State of  
13 California and this District and has purposefully availed itself of the privileges of  
14 conducting business in the State of California and in this District. Polaris' causes of  
15 action arise directly from Zones' business contacts and other activities in the State of  
16 California and in this District.

17 29. On information and belief, Zones has committed acts of infringement  
18 within this District and the State of California by, *inter alia*, making, importing,  
19 using, selling, and/or offering for sale Accused Products that infringe one or more  
20 claims of the Asserted Patents. More specifically, on information and belief, Zones,  
21 directly and/or through intermediaries or agents, makes, imports, uses, sells, ships,  
22 distributes, offers for sale, advertises, and/or otherwise promotes infringing Accused  
23 Products in the United States, the State of California, and this District.

24 30. Venue is proper in this District under 28 U.S.C. §§ 1391(b), (c) and  
25 1400(b), including based on Zones' physical presence in this District and/or Zones'  
26 transaction of business in this District directly and/or through its affiliates and  
27 customers and/or acts of patent infringement in this District.

**PLPC**

31. On information and belief, PLPC transacts and conducts business in this District and the State of California and is subject to the personal jurisdiction of this Court. On information and belief, PLPC has minimum contacts within the State of California and this District and has purposefully availed itself of the privileges of conducting business in the State of California and in this District. Polaris' causes of action arise directly from PLPC's business contacts and other activities in the State of California and in this District.

32. On information and belief, PLPC has committed acts of infringement within this District and the State of California by, *inter alia*, making, importing, using, selling, and/or offering for sale Accused Products that infringe one or more claims of the Asserted Patents. More specifically, on information and belief, PLPC, directly and/or through intermediaries or agents, makes, imports, uses, sells, ships, distributes, offers for sale, advertises, and/or otherwise promotes infringing Accused Products in the United States, the State of California, and this District.

33. Venue is proper in this District under 28 U.S.C. §§ 1391(b), (c) and 1400(b), including based on PLPC's physical presence and the location of its headquarters in this District and/or PLPC's transaction of business in this District directly and/or through its affiliates and customers and/or acts of patent infringement in this District.

**PATENTS-IN-SUIT**

34. Plaintiff owns the entire right, title, and interest in U.S. Patent No. 8,554,968 titled "Interrupt Technique for a Nonvolatile Memory Controller," including the right to assert all causes of action arising under said patent and to seek damages and all other remedies for the infringement thereof. The '968 Patent issued on October 8, 2013 to inventors Peter Z. Onufryk, Jayesh Patel and Ihab Jaser from the U.S. Patent Application No. 13/052,388 filed on March 21, 2011. A true and correct copy of the '968 Patent is attached as **Exhibit A** to this Complaint.

1           35. Plaintiff owns the entire right, title, and interest in U.S. Patent No.  
2 9,183,085 titled “Systems and Methods for Adaptively Selecting from among a  
3 Plurality of Error Correction Coding Schemes in a Flash Drive for Robustness and  
4 Low Latency,” including the right to assert all causes of action arising under said  
5 patent and to seek damages and all other remedies for the infringement thereof. The  
6 ’085 Patent issued on November 10, 2015, to inventor Philip L. Northcott from the  
7 U.S. Patent Application No. 13/477,600, filed on May 22, 2012. A true and correct  
8 copy of the ’085 Patent is attached as **Exhibit B** to this Complaint.

9           36. Plaintiff owns the entire right, title, and interest in U.S. Patent No.  
10 8,601,346 titled “System and Method for Generating Parity Data in a Nonvolatile  
11 Memory Controller by Using a Distributed Processing Technique,” including the  
12 right to assert all causes of action arising under said patent and to seek damages and  
13 all other remedies for the infringement thereof. The ’346 Patent issued on December  
14 3, 2013, to inventors Peter Z. Onufryk and Inna Levit from the U.S. Patent  
15 Application 13/052,835, filed on March 21, 2011. A true and correct copy of the ’346  
16 Patent is attached as **Exhibit C** to this Complaint.

17           **’968 PATENT BACKGROUND AND PATENTED TECHNOLOGY**

18           37. The ’968 Patent relates generally to improvements to nonvolatile  
19 memory controllers, including the processing of memory commands and the  
20 generation of a completion status for such commands. The inventive nonvolatile  
21 memory controller transmits the completion status to a host processing unit for  
22 storage in a completion queue of the host processing unit. An interrupt manager in  
23 the nonvolatile memory controller determines whether the completion queue contains  
24 an unprocessed completion status and generates an interrupt message packet. The  
25 nonvolatile memory controller transmits the interrupt message packet to the host  
26 processing unit for triggering an interrupt in the host processing unit and alerting the  
27 host processing unit to the unprocessed completion status.

28           38. The claims of the ’968 patent are directed to improvements to computer

1 memory technology, specifically nonvolatile memory controllers.

2 39. Conventional nonvolatile memory controllers did not implement  
3 interrupt managers. Instead, prior art host processors (e.g., CPUs) were required to  
4 continuously monitor the completion status of read/write tasks sent to memory  
5 controllers, requiring excess computing resources on the part of the CPU and the  
6 memory controller. '968 Patent, col. 16:28-42. For example, the CPU was required  
7 to maintain a completion queue. This requires the CPU to set aside cache memory  
8 and clock cycles, adding overhead and reducing overall CPU performance. In  
9 addition, the memory controller also had to set aside clock cycles to monitor the  
10 CPU's completion queue and alert the CPU of unprocessed completion statuses,  
11 thereby reducing the availability of the memory controller and increasing latency.  
12 Continuous monitoring of the completion queue also requires bandwidth on the  
13 communication bus between the CPU and the memory controller. The bus may be  
14 shared with other devices, e.g., a graphics processor, whose performance may be  
15 bottlenecked by effectively reducing the bus bandwidth.

16 40. The implementation of an interrupt manager within nonvolatile memory  
17 units boosts the performance for both the CPU and memory controller by allowing  
18 them to use their resources on tasks other than managing and monitoring the  
19 completion queue. *Id.* The interrupt manager provides periodic reminders of which  
20 tasks, if any, are still incomplete. Thus, a memory system that implements an  
21 interrupt manager enables greater performance of the host CPU, memory controller  
22 and host computer. The structure of the memory system is unconventional compared  
23 to prior art nonvolatile memory systems that did not incorporate an interrupt  
24 manager, and required the CPU and memory controller to mutually communicate  
25 with respect to incomplete tasks. The system addresses a technical problem in  
26 computer systems, improving the responsiveness, efficiency and reliability of how  
27 memory controllers communicate status information to the host processing unit. By  
28 managing interrupts and completion queue states, the invention enhances the overall

1 system performance and responsiveness, e.g., speed and latency. The integration and  
2 arrangement of hardware components recited in the claims underscores the technical  
3 nature of the invention, as it involves concrete hardware-based operations to achieve  
4 the desired improvements in system communication and memory management.

5 41. In addition, claim 8 recites a specific, unconventional architecture for  
6 the memory controller comprising separate memories for completion queue state and  
7 interrupt vector state. The interrupt manager controller is coupled to both the  
8 completion queue state memory and interrupt vector state memory, and maps at least  
9 one completion queue state of the plurality of completion queue states to an interrupt  
10 vector state of the plurality of interrupt vector states. This arrangement allows the  
11 interrupt manager controller to generate the interrupt vector state, determine a  
12 completion status queue, and generate an interrupt packet state to alert the host CPU  
13 of the unprocessed completion status in the completion queue. Claim 8 recites an  
14 unconventional arrangement of elements that implements the interrupt manager  
15 controller whose adoption improves the performance of the memory controller, host  
16 CPU, and host computer, as discussed above.

#### 17 **'085 PATENT BACKGROUND AND PATENTED TECHNOLOGY**

18 42. The '085 Patent relates generally to disclosed techniques providing  
19 relatively low uncorrectable bit error rates (BER) for flash memory; low write  
20 amplification; long life, fast and efficient retrieval; and efficient storage density such  
21 that a solid-state drive (SSD) or flash drive can be implemented using relatively  
22 inexpensive MLC flash for enterprise storage application.

23 43. The claims of the '085 patent are directed to improvements to memory  
24 technology, specifically an improved implementation of error correction coding for  
25 Flash memory.

26 44. Error correction coding (ECC) is used to detect and correct errors that  
27 inevitably occur as a result of memory cell degradation in flash memory, such as  
28 solid state drives. FIG. 1A illustrates a standard layout for a page of flash memory in

1 which a region is provided for user data 101 or information data in the main area of  
2 the flash page, and a spare area 102 is provided to provide room for ECC parity and  
3 other data. '085 Patent, col. 2:3-7. FIG. 1B illustrates how user data 103, metadata  
4 104, such as data integrity feature (DIF) and Journaling Engine management data,  
5 and the manufacturer's recommended amount of ECC parity data 105 may be  
6 interleaved within the page. *Id.* at col. 2:4-11.

7 45. Conventionally, redundant information is stored or transmitted  
8 alongside the regular information bearing data to allow an ECC decoder to deduce  
9 the originally transmitted or stored information even in the presence of errors, for  
10 example, when the signal-to-noise ratio is too low for the cell to be accurately read.  
11 Errors can arise when a memory cell is repeatedly programmed and erased. *Id.* at  
12 col. 1:58-62. The flash memory chip manufacturer conventionally specifies a  
13 particular strength of ECC code, typically a one-dimensional BCH code, capable of  
14 correcting a certain number of bits per certain size of sector, for example 24 bits per  
15 1024 bytes. *Id.* at cols. 1:63-2:1. "So long as the specified error correction is  
16 provided by the flash controller, the flash memory chip manufacturer guarantees a  
17 certain number of Program/Erase (P/E) cycles over which the flash memory chips  
18 will store and retain data, with no more errors than the ECC can correct, with a  
19 probability of uncorrectable errors occurring less than some acceptable risk for the  
20 end user." *Id.* at col. 2:12-18.

21 46. But such "conventional approaches of applying ECC to flash memory  
22 can be inefficient at achieving relatively low uncorrectable error rates over the total  
23 service life and traffic loads that can be required in an enterprise storage environment,  
24 such as in a server. *Id.* at col. 2:23-27.

25 47. As a result, the '085 Patent discloses improvements over the prior art,  
26 including the use of "three-dimensional turbo code, built out of three partially  
27 orthogonal ECC components." *Id.*, col. 2:37-38. The first dimension consists of  
28 "primary" error correction code that provide error correction for a page in the flash

1 memory. *Id.*, col. 2:39-41. The second dimension consists of “secondary” error  
2 correction codes, which are at least partly orthogonal to the primary codes, and  
3 provide error correction for a “page stripe,” which can be a group of flash memory  
4 data pages that are associated by secondary error correction codes. *Id.*, col. 2:41-55.

5 48. Likewise, the ’085 Patent improves on existing approaches by  
6 disclosing a system consisting of a first circuit configured to determine a bit error  
7 rate associated with a region associated with a plurality of flash memory pages or  
8 integer fractions thereof and to compare the determined bit error rate to one or more  
9 predetermined thresholds corresponding to a set of predefined gears comprising at  
10 least a first gear and a second gear, wherein the predefined gears correspond to  
11 different error correction coding (ECC) schemes, wherein the first gear has a different  
12 data payload size and correction capability than the second gear; and a second circuit  
13 configured to select a gear from the set for the region based at least partly on the  
14 comparisons to the one or more predetermined thresholds. *Id.*, col. 4:37-49.

15 49. In another example of an improvement over existing approaches, the  
16 ’085 Patent discloses an apparatus that includes a first circuit configured to run a  
17 memory test to determine raw bit error rates among regions of a flash drive; and a  
18 second circuit configured to: retire regions having a raw bit error rate (RBER) above  
19 a selected threshold; and allocate one or more remaining regions to one of at least a  
20 first gear or a second gear based at least partly on the RBER for the region, wherein  
21 the first gear and the second gear vary by data payload size and correction capability,  
22 wherein different gears correspond to different error correction coding (ECC)  
23 schemes for regions of the flash drive; wherein the first circuit is configured to run  
24 the memory test concurrently with initialization operations for an end user. *Id.*, col.  
25 5:12-24.

26 50. The ’085 claims enable a more granular application of ECC schemes for  
27 particular regions of a flash memory device, providing a number of performance and  
28 lifespan benefits to the flash memory device.

1           51. First, a scheme that requires less redundancy can be used where there is  
2 less likely to be error to allow for fewer regions of the flash memory to be dedicated  
3 to ECC data, whereas a scheme requiring higher redundancy can be used to ensure  
4 that the flash memory will not lose data. As a result, the flash memory is more  
5 efficient in performing error control. In other words, more data can be stored on a  
6 Flash memory that implements multiple schemes or gears, which can lead to cost  
7 savings for customers. Also, performing read/write operations to data stored using a  
8 lower redundancy scheme results in overall faster operation of the flash memory  
9 device.

10           52. Second, each region can be dynamically re-gearred depending on the  
11 data being stored thereon, providing a flexible approach that does not require  
12 partitioning the memory into fixed regions using different gears. Such an approach  
13 can extend the lifespan of the flash device by gradually migrating data from a scheme  
14 with lower redundancy to a scheme requiring higher redundancy, while maintaining  
15 a relatively low uncorrectable error rate. This approach also optimizes the speed and  
16 responsiveness of the flash memory because it is faster to perform read/write  
17 operations when less redundancy is used. This would not be possible in a flash drive  
18 incorporating only a single gear of error correction coding.

19           53. The systems and methods claimed in the '085 patent provide solutions  
20 to technical problems specific to the field of digital memory systems, particularly  
21 flash memory. By dynamically selecting an ECC scheme based on the bit error rate,  
22 the method improves the reliability and efficiency of data storage and retrieval in  
23 flash memory devices. This represents a technical improvement over prior art  
24 systems that may use static ECC schemes without regard to the actual error  
25 conditions. Furthermore, the problem of managing bit error rates in flash memory is  
26 a specific technical challenge. The claimed system and methods address this by  
27 providing a tailored solution that varies the amount of memory space allocated for  
28 data payload and parity symbols based on real-time error conditions. This adaptive

1 approach is technical in nature and directly related to the functioning of computer  
2 memory systems.

3 54. Claim 15 further defines first and second circuits – two physical  
4 arrangements of electronic components connected by leads or wires – that perform  
5 distinct tasks with respect to implementing the dynamic selection of ECC schemes  
6 disclosed in the '085 patent. The specialized integrated circuits that are recited in the  
7 claim underscore the technical nature of the solution, which is designed to work  
8 within the constraints and capabilities of specific hardware components. As the  
9 underlying improvement of using and selecting multiple ECC schemes is already an  
10 improvement to flash memory, claim 8 provides a physical implementation of such  
11 improvement.

12 55. As a result, the '085 claims are directed to unconventional  
13 improvements to flash memory that allow for more efficient storage and relatively  
14 low uncorrectable error rates for both consumer and enterprise applications.

### 15 **'346 PATENT BACKGROUND AND PATENTED TECHNOLOGY**

16 56. The '346 Patent relates generally to a nonvolatile memory controller  
17 performing a data-stripe operation by processing a collection of commands. The  
18 collection of commands includes data update commands and a parity write command.  
19 The nonvolatile memory controller includes a number of command processing units,  
20 each of which receives a command in the collection of commands. Each of the  
21 command processing units receiving a data update command requests a data block  
22 from a controller memory; receives the data block from the controller memory  
23 through a data path in response to the request; and writes the data block to a  
24 nonvolatile memory device.

25 57. The claims of the '346 patent are directed to improvements to memory  
26 technology, specifically an improved nonvolatile memory controller architecture.

27 58. Conventionally, a disk drive controller for a RAID array of disk drives  
28 is required to perform a data stripe operation to distribute data blocks and parity data

1 among the drives in the array. The conventional controller includes a dedicated  
2 processor to generate parity data, which is a computationally intense task. Typically,  
3 the dedicated processor stores data blocks into individual data buffers of the disk  
4 drive controller, executes computing instructions to generate parity data, and stores  
5 the parity data into yet another data buffer.

6 59. The '346 Patent observes that “[a]lthough use of a dedicated processor  
7 for generating parity data generally improves throughput of a disk drive controller,  
8 generation of parity data is still a performance bottleneck in many disk drive  
9 controllers. Moreover, the data buffers consume a considerable amount of area and  
10 power in integrated circuit implementations of the disk drive controller.” ’346 Patent,  
11 col. 1:40-46.

12 60. The '346 Patent introduces an improved architecture for the memory  
13 controller, an embodiment of which is shown in FIG. 4. This architecture comprises  
14 a command processing module 400 having three command processing units 415,  
15 although more or fewer units may be used. *Id.* at col. 7:39-46. The command  
16 processing units process commands for managing data in the nonvolatile memory  
17 device. *Id.* As shown in FIG. 4, the improved architecture also includes parity  
18 calculator 420. The parity calculator includes page frames and generates parity  
19 blocks in the page frames. *Id.* at col. 7:47-49. The parity blocks are generated by  
20 storing a first data block of the sequence of data blocks into the page frame and  
21 updating the data block stored in the page frame with each data block following the  
22 first data block in the sequence of data blocks, without storing each data block in a  
23 data buffer. *Id.* at col. 1:66-2:3, 2:9-14. The parity write command is distributed to  
24 one of the command processing units, which then writes the block to the nonvolatile  
25 memory device. *Id.* at col. 3:10-14.

26 61. The '346 Patent improves over conventional approaches by disclosing  
27 a nonvolatile memory controller that “performs a data stripe operation by using a  
28 plurality of command processing units, the nonvolatile memory controller performs

1 a data stripe operation more quickly than other methods using only a single dedicated  
2 processor to perform a data stripe operation.” *Id.* at col. 2:4-9.

3 62. In addition, the ’346 Patent proposes a parity bit calculator that  
4 “generates the parity block in the page frame as the parity calculator is receiving the  
5 data blocks for the data stripe operation, the parity calculator need not store all the  
6 data blocks of the data stripe at the same time when generating a parity block.” *Id.*  
7 at col. 2:9-13.

8 63. In another example of an improvement over existing approaches, the  
9 ’346 Patent discloses a nonvolatile memory controller that “performs a data stripe  
10 operation on block blocks. The nonvolatile memory controller includes command  
11 processing units and a parity calculator. The parity calculator is coupled to the  
12 command processing units. Each of the command processing units is configured to  
13 receive a command of a plurality of commands for performing the data stripe  
14 operation. The commands include data update commands and a parity write  
15 command. Each command processing unit receiving a data update command is  
16 configured to request a data block of the data blocks based on the data update  
17 command, receive the data block in response to the request, and write the data block  
18 to a nonvolatile memory device. The parity calculator is configured to receive the  
19 data blocks and generate a parity block based on the data blocks. The command  
20 processing unit receiving the parity write command is configured to write the parity  
21 block to a nonvolatile memory based on the parity write command.” *Id.* at col. 2:18-  
22 35.

23 64. The improved nonvolatile memory controller architecture that  
24 implements a plurality of command processing units and the parity bit calculator  
25 leads to performance benefits for the nonvolatile memory controller. Specifically,  
26 “the nonvolatile memory controller consumes less power and area than other  
27 nonvolatile memory controllers in which data blocks of a data stripe operation are  
28 stored in individual data buffers when computing a parity block.” *Id.* at col. 2:14-17.

1 In this approach, the parity buffer need not buffer the entire data block in a buffer,  
2 nor store the parity data in another buffer. It provides an efficient and streamlined  
3 approach whereby the parity calculator works with the plurality of command  
4 processing units in parallel to enable the controller to achieve faster and more  
5 efficient data striping operations.

6 65. As a result of consuming less power, a host device can enjoy extended  
7 battery life, or utilize a smaller and/or less expensive battery or power supply. As a  
8 result of requiring less area, the nonvolatile memory can be smaller and cheaper to  
9 manufacture, as it requires a smaller silicon footprint. Conversely, the nonvolatile  
10 memory capacity can be increased over conventional memory having the same stated  
11 capacity.

12 66. The claims recite nonvolatile memory controllers and methods designed  
13 to perform data stripe operations on multiple data blocks. This is a technical solution  
14 aimed at improving the efficiency and reliability of data storage in nonvolatile  
15 memory devices. By detailing how data blocks are handled and parity blocks are  
16 generated and written, the claim addresses specific technical challenges in memory  
17 management, such as reducing latency and improving data integrity during write  
18 operations. The claims further recite specific hardware arrangements including a  
19 plurality of command processing units and a parity calculator, each with specific  
20 functionalities. This novel integration and arrangement of hardware components  
21 underscores the technical nature of the invention, as it involves concrete hardware-  
22 based operations to achieve the desired improvements in memory management.

### 23 **COUNT I**

24 (INFRINGEMENT OF U.S. PATENT NO. 8,554,968)

25 67. Plaintiff incorporates by reference and re-alleges the foregoing  
26 paragraphs as fully set forth herein.

27 68. Defendants have directly infringed, and continue to directly infringe,  
28 one or more claims of the '968 Patent, including at least claim 1 of the '968 Patent,

1 literally and/or under the doctrine of equivalents, by or through making, using,  
2 offering for sale, selling within the United States and/or importing into the United  
3 States its SSD products that support NVMe.

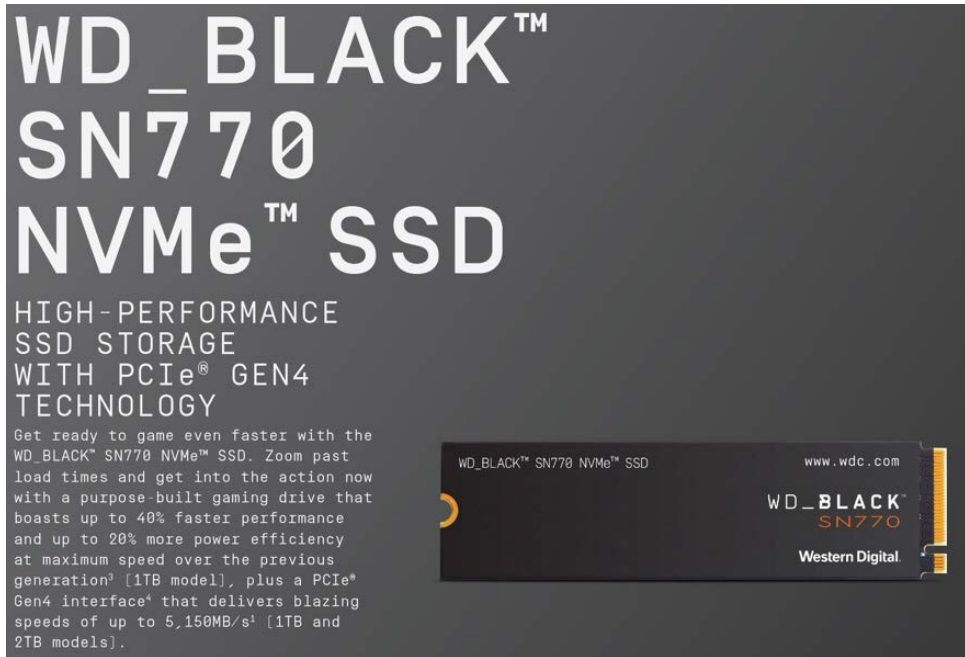
4 69. **Exhibit D** is an exemplary claim chart, demonstrating on an element-  
5 by-element basis, how the Accused Products infringe claims of the '968 patent.

6 70. Claim 1 of the '968 Patent, for example, reads as follows:

7 1. A nonvolatile memory controller for alerting a host  
8 processing unit to an unprocessed completion status  
9 contained in a completion queue of the host processing  
unit, the nonvolatile memory controller comprising:

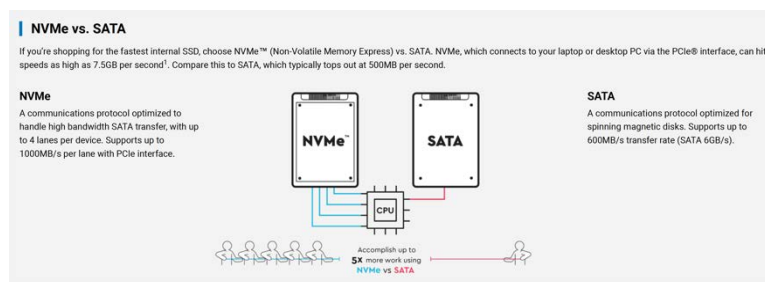
10 an interrupt manager configured to generate a completion  
queue state for indicating the occurrence of a completion  
11 queue event associated with the completion queue,  
generate an interrupt vector state based on the completion  
12 queue state, determine the completion queue of the host  
processing unit contains an unprocessed completion status  
13 based on the interrupt vector state, and generate an  
interrupt message packet for triggering an interrupt in the  
14 host processing unit to alert the host processing unit of the  
unprocessed completion status in the completion queue,  
15 and wherein the completion queue state includes a doorbell  
update status indicating whether the host processing unit  
16 has performed a doorbell update event in which the host  
processing unit updates a head pointer stored in the  
17 nonvolatile memory controller for the completion queue.

18 71. Defendants make, use, sell, offer for sale and import SSD products that  
19 support the NVMe standard and that include a nonvolatile memory controller  
20 configured for alerting a host processing unit to an unprocessed completion status  
21 contained in a completion queue of the host processing unit. For example, as shown  
22 below, WD Black-branded SSDs, which are used for gaming consoles and gaming  
23 PCs, Blue- and Green-branded SSDs, which are used for everyday PCs, Red-branded  
24 SSDs, which are used for Network Attached Storage (NAS), and Gold- and Ultrastar  
25 SSDs , which are used for data centers, all support NVMe:  
26  
27  
28



WD\_BLACK SN770 NVMe SSD, Western Digital (Jan. 2022), [https://documents.westerndigital.com/content/dam/doc-library/en\\_us/assets/public/western-digital/product/internal-drives/wd-black-ssd/product-brief-wd-black-sn770-nvme-ssd.pdf](https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/internal-drives/wd-black-ssd/product-brief-wd-black-sn770-nvme-ssd.pdf) [hereinafter “WD\_BLACK SN770 NVMe SSD”].

72. The image below shows the benefits and improvements of NVMe over SATA:



Internal SSD, Western Digital, <https://www.westerndigital.com/solutions/internal-ssd> (last visited Jan. 2, 2024) [hereinafter “Internal SSD”].

73. The following describes how NVMe functions:

1.4 Theory of Operation

The NVM Express scalable interface is designed to address the needs of Enterprise and Client systems that utilize PCI Express based solid state drives or fabric connected devices. The interface provides optimized command submission and completion paths. It includes support for parallel operation by supporting up to 65,535 I/O Queues with up to 64 Ki - 1 outstanding commands per I/O Queue. Additionally, support has been added for many Enterprise capabilities like end-to-end data protection (compatible with SCSI Protection Information, commonly known as T10 DIF, and SNIA DIX standards), enhanced error reporting, and virtualization.

The interface has the following key attributes:

- Does not require uncachable / MMIO register reads in the command submission or completion path;
- A maximum of one MMIO register write is necessary in the command submission path;
- Support for up to 65,535 I/O Queues, with each I/O Queue supporting up to 65,535 outstanding commands;
- Priority associated with each I/O Queue with well-defined arbitration mechanism;
- All information to complete a 4 KiB read request is included in the 64B command itself, ensuring efficient small I/O operation;
- Efficient and streamlined command set;
- Support for MSI/MSI-X and interrupt aggregation;
- Support for multiple namespaces;
- Efficient support for I/O virtualization architectures like SR-IOV;
- Robust error reporting and management capabilities; and
- Support for multi-path I/O and namespace sharing.

This specification defines a streamlined set of registers whose functionality includes:

- Indication of controller capabilities;
- Status for controller failures (command status is processed via CQ directly);
- Admin Queue configuration (I/O Queue configuration processed via Admin commands); and
- Doorbell registers for scalable number of Submission and Completion Queues.

The NVM Express interface is based on a paired Submission and Completion Queue mechanism. Commands are placed by host software into a Submission Queue. Completions are placed into the associated Completion Queue by the controller. Multiple Submission Queues may utilize the same Completion Queue. Submission and Completion Queues are allocated in memory.

An Admin Submission and associated Completion Queue exist for the purpose of controller management and control (e.g., creation and deletion of I/O Submission and Completion Queues, aborting commands, etc.). Only commands that are part of the Admin Command Set may be submitted to the Admin Submission Queue.

NVM Express, Inc., *NVM Express Base Specification, Revision 1.4*, (June 10, 2019), [https://nvmexpress.org/wp-content/uploads/NVM-Express-1\\_4-2019.06.10-Ratified.pdf](https://nvmexpress.org/wp-content/uploads/NVM-Express-1_4-2019.06.10-Ratified.pdf) [hereinafter “NVM Express Specification”].

Host software submits commands to a controller through pre-allocated Submission Queues. A controller is alerted to newly submitted commands through SQ Tail Doorbell register writes. The difference between the previous doorbell register value and the current register write indicates the number of commands that were submitted.

Upon completion of the command execution by the NVM subsystem, the controller presents completion queue entries to the host through the appropriate Completion Queues. If MSI-X or multiple message MSI is in use, then the interrupt vector indicates the Completion Queue(s) with possible new command completions for the host to process. If pin-based interrupts or single message MSI interrupts are used, host software interrogates the Completion Queue(s) for new completion queue entries. The host updates the CQ Head doorbell register to release Completion Queue entries to the controller and to clear the associated interrupt.

[Express Specification](#) at 274.

74. Defendants' SSD products with NVMe support include an interrupt manager configured to generate a complete queue state for indicating occurrence of a completion queue event associated with the completion queue, as shown below:

#### 1.6.9 controller

A controller is the interface between a host and an NVM subsystem. There are three types of controllers:

- a) I/O controllers;
- b) discovery controllers; and
- c) administrative controllers.

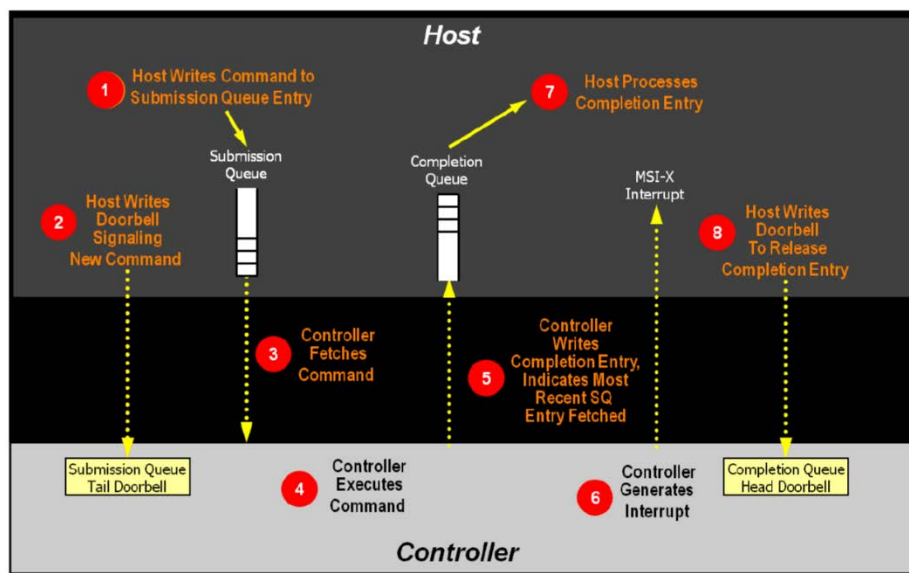
A controller executes commands submitted by a host on a Submission Queue and posts a completion on a Completion Queue. All controllers implement one Admin Submission Queue and one Admin Completion Queue.

[NVM Express Specification](#) at 14.

5. After a command has completed execution, the controller places a completion queue entry in the next free slot in the associated Completion Queue. As part of the completion queue entry, the controller indicates the most recent Submission Queue entry that has been consumed by advancing the Submission Queue Head pointer in the completion entry. Each new completion queue entry has a Phase Tag inverted from the previous entry to indicate to the host that this completion queue entry is a new entry;
6. The controller optionally generates an interrupt to the host to indicate that there is a new completion queue entry to consume and process. In the figure, this is shown as an MSI-X interrupt, however, it could also be a pin-based or MSI interrupt. Note that based on interrupt coalescing settings, an interrupt may or may not be generated for each new completion queue entry;
7. The host consumes and then processes the new completion queue entries in the Completion Queue. This includes taking any actions based on error conditions indicated. The host continues consuming and processing completion queue entries until a previously consumed entry with a Phase Tag inverted from the value of the current completion queue entries is encountered; and
8. The host writes the Completion Queue Head Doorbell register to indicate that the completion queue entry has been consumed. The host may consume many entries before updating the associated Completion Queue Head Doorbell register.

[NVM Express Specification](#) at 283.

Figure 432: Command Processing



[NVM Express Specification](#) at 284.

75. Defendants’ SSD products with NVMe support include an interrupt manager configured to generate an interrupt vector state based on the complete queue state, which is shown below:

Figure 151: Create I/O Completion Queue – Command Dword 11

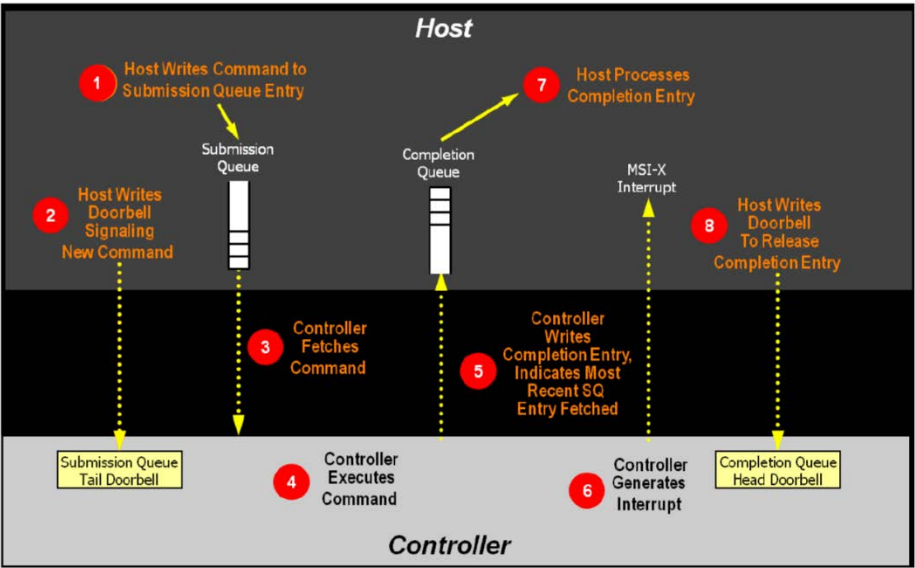
| Bits  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | <b>Interrupt Vector (IV):</b> This field indicates interrupt vector to use for this Completion Queue. This corresponds to the MSI-X or multiple message MSI vector to use. If using single message MSI or pin-based interrupts, then this field shall be cleared to 0h. In MSI-X, a maximum of 2,048 vectors are used. This value shall not be set to a value greater than the number of messages the controller supports (refer to MSICAP.MC.MME or MSIXCAP.MXC.TS). If the value is greater than the number of messages the controller supports, the controller should return an error of Invalid Interrupt Vector. |

[NVM Express Specification](#) at 102.

- After a command has completed execution, the controller places a completion queue entry in the next free slot in the associated Completion Queue. As part of the completion queue entry, the controller indicates the most recent Submission Queue entry that has been consumed by advancing the Submission Queue Head pointer in the completion entry. Each new completion queue entry has a Phase Tag inverted from the previous entry to indicate to the host that this completion queue entry is a new entry;
- The controller optionally generates an interrupt to the host to indicate that there is a new completion queue entry to consume and process. In the figure, this is shown as an MSI-X interrupt, however, it could also be a pin-based or MSI interrupt. Note that based on interrupt coalescing settings, an interrupt may or may not be generated for each new completion queue entry;
- The host consumes and then processes the new completion queue entries in the Completion Queue. This includes taking any actions based on error conditions indicated. The host continues consuming and processing completion queue entries until a previously consumed entry with a Phase Tag inverted from the value of the current completion queue entries is encountered; and
- The host writes the Completion Queue Head Doorbell register to indicate that the completion queue entry has been consumed. The host may consume many entries before updating the associated Completion Queue Head Doorbell register.

[NVM Express Specification](#) at 283.

Figure 432: Command Processing

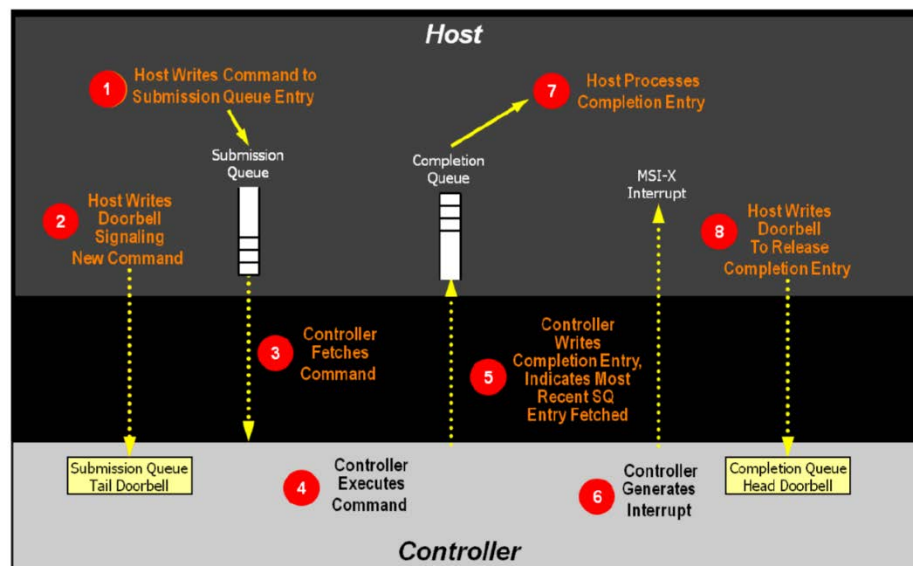


[NVM Express Specification](#) at 284.

76. The Accused Products with NVMe support include an interrupt manager configured to determine whether the completion queue of the host processing unit contains an unprocessed completion state based on the interrupt vector state. The interrupt manager is further configured to generate an interrupt message packet for triggering an interrupt in the host processing unit to alert the host processing unit of the unprocessed completion status in the completion queue. This is shown in the images below:

6. The controller optionally generates an interrupt to the host to indicate that there is a new completion queue entry to consume and process. In the figure, this is shown as an MSI-X interrupt, however, it could also be a pin-based or MSI interrupt. Note that based on interrupt coalescing settings, an interrupt may or may not be generated for each new completion queue entry;
7. The host consumes and then processes the new completion queue entries in the Completion Queue. This includes taking any actions based on error conditions indicated. The host continues consuming and processing completion queue entries until a previously consumed entry with a Phase Tag inverted from the value of the current completion queue entries is encountered; and
8. The host writes the Completion Queue Head Doorbell register to indicate that the completion queue entry has been consumed. The host may consume many entries before updating the associated Completion Queue Head Doorbell register.

Figure 432: Command Processing



[NVM Express Specification](#) at 283-284.

77. The nonvolatile memory controller, which generates an MSI-X interrupt, is transmitted as a PCIe message packet. This is demonstrated in the quote below:

NVMe, which connects to your laptop or desktop PC via the PCIe® interface, can hit speeds as high as 7.5GB per second. Compare this to SATA, which typically tops out at 500MB per second.

### Internal SSD.

*PCI Express Base Specification Revision 2.1* (March 4, 2009), [hereinafter “PCIe v2.1”].

|                                        |                                                                                                                                                                                                                                                                                                                    |
|----------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Message Signaled Interrupt (MSI/MSI-X) | Two similar but separate mechanisms that enable a Function to request service by writing a system-specified DWORD of data to a system-specified address using a Memory Write Request. Compared to MSI, MSI-X supports a larger maximum number of vectors and independent message address and data for each vector. |
| Packet                                 | A fundamental unit of information transfer consisting of a header that, in some cases, is followed by a data payload.                                                                                                                                                                                              |

PCIe v2.1 at 31.

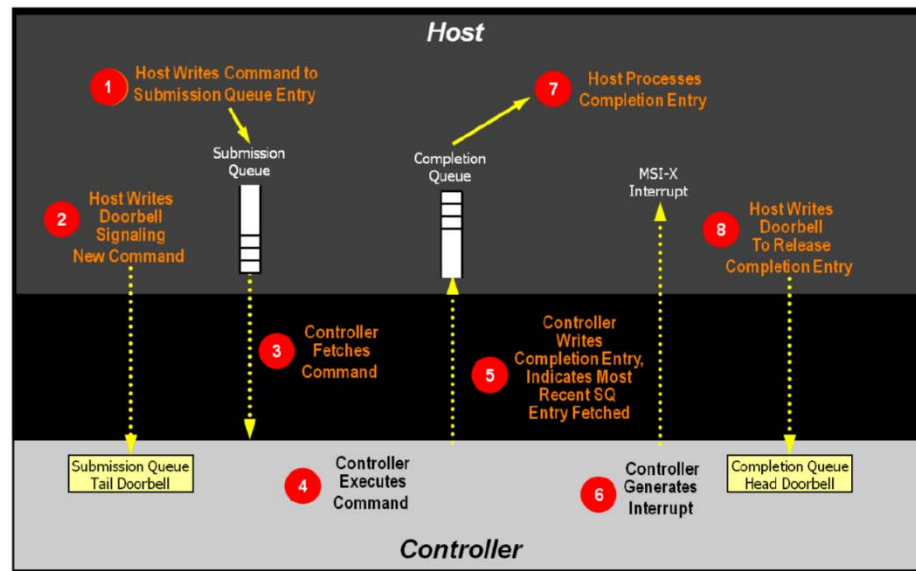
|                               |                                                                                  |
|-------------------------------|----------------------------------------------------------------------------------|
| Transaction Layer             | The Layer that operates at the level of transactions (for example, read, write). |
| Transaction Layer Packet, TLP | A Packet generated in the Transaction Layer to convey a Request or Completion.   |

PCIe v2.1 at 33.

78. The image below shows a completion queue state includes a doorbell update status indicating whether the host processing unit has performed a doorbell update event in which the host processing unit updates a head pointer stored in the nonvolatile memory controller for the completion queue.

6. The controller optionally generates an interrupt to the host to indicate that there is a new completion queue entry to consume and process. In the figure, this is shown as an MSI-X interrupt, however, it could also be a pin-based or MSI interrupt. Note that based on interrupt coalescing settings, an interrupt may or may not be generated for each new completion queue entry;
7. The host consumes and then processes the new completion queue entries in the Completion Queue. This includes taking any actions based on error conditions indicated. The host continues consuming and processing completion queue entries until a previously consumed entry with a Phase Tag inverted from the value of the current completion queue entries is encountered; and
8. The host writes the Completion Queue Head Doorbell register to indicate that the completion queue entry has been consumed. The host may consume many entries before updating the associated Completion Queue Head Doorbell register.

Figure 432: Command Processing



[NVM Express Specification](#) at 283-284.

79. Defendants have directly infringed, and continue to infringe, the claims of the '968 Patent in the United States, by making, using, offering for sale, selling, and/or importing the Accused Products in violation of 35 U.S.C. § 271(a). For example, Defendants provide SSD products configured with the hardware and software that satisfy the limitations of at least claim 1. Defendants further directly infringe the '968 Patent when its SSD products with NVMe are installed and operated by its employees in a computer system, such as for gaming, personal computing, or data centers. Direct infringement further occurs when Defendants' employees use and test the hardware and software.

80. Defendants also have infringed, and continue to infringe the claims of the '968 Patent by actively inducing others to use the Accused Products. Defendants' users, customers, agents or other third parties who use the Accused Products in accordance with Defendants' instructions infringe the claims of the '968 Patent, in violation of 35 U.S.C. § 271(a). Defendants induce its customers to use its SSD products with NVMe for the benefits of higher performance, reduced size and power, and increased reliability compared to SSD products with other interfaces, such as

1 SATA. Defendants are thereby liable for infringement of the '968 Patent under 35  
2 U.S.C. § 271(b).

3 81. Defendants' users, customers, agents or other third parties who use the  
4 Accused Products in accordance with Defendants' instructions infringe the claims of  
5 the '968 Patent, in violation of 35 U.S.C. § 271(b). Defendants intentionally instruct  
6 its customers to infringe through support information, demonstrations, brochures,  
7 videos, and user guides, such as those located at:

8 <https://www.westerndigital.com/support;>

9 <https://support.wdc.com/contact.aspx?lang=en;>

10 <https://www.westerndigital.com/support/category-selection;>

11 [https://www.youtube.com/channel/UC\\_M0BlntDVSblWg6ggUa7UQ;](https://www.youtube.com/channel/UC_M0BlntDVSblWg6ggUa7UQ;)

12 <https://www.youtube.com/watch?v=L0zZtwRFj0E;>

13 <https://www.youtube.com/westerndigital>; and

14 <https://www.youtube.com/c/westerndigitalcorporation>.

15 82. Defendants are on notice of its infringement by no later than the filing  
16 and service of this Complaint. By the time of trial, Defendants will have known and  
17 intended (since receiving such notice) that its continued actions would actively  
18 induce to the infringement of the '968 Patent. Defendants were further aware of the  
19 '968 Patent because it was cited as prior art by Western Digital in U.S. Patent Nos.  
20 10,725,835, 10,296,249, 10,452,278, 10,466,903, and 10,509,569, which are all  
21 assigned to Western Digital.

22 83. On January 23, 2024, Plaintiff sent a notice letter to Western Digital,  
23 notifying them that they were infringing the Asserted Patents. Western Digital's  
24 infringement of the '968 Patent has been willful and intentional under the standard  
25 announced in *Halo Elecs., Inc. v. Pulse Elecs., Inc.*, 579 U.S. 93 (2016). Western  
26 Digital has not replied to this letter.

27 84. Western Digital has willfully infringed the '968 Patent by refusing to  
28

1 take a license and continuing to make, use, test, sell, license, and/or offer for  
2 sale/license the '968 Patent Accused Products. Instead of taking a license, Western  
3 Digital has opted to make the business decision to "efficiently infringe" the '968  
4 Patent. In doing so, Western Digital willfully infringes the '968 Patent.

5 85. Defendants are liable as contributory infringers of the '968 Patent under  
6 35 U.S.C. § 271(c) by having offered to sell, sold and imported and continuing to  
7 offer to sell, selling, and importing into the United States its SSD products that  
8 support NVMe, to be especially made or adapted for use in an infringement of the  
9 '968 Patent. Defendants' SSD products are key components in gaming consoles and  
10 gaming PCs, computers, everyday PCs, Network Attached Storage (NAS) devices,  
11 servers and data centers. These SSD products are material components for use in  
12 practicing the '968 Patent and are specifically made and are not a staple article of  
13 commerce suitable for substantial noninfringing use. Defendants supplied these  
14 components with knowledge of the '968 Patent and with knowledge that these  
15 components constitute material parts of the claimed inventions of the '968 Patent.

16 86. As a result of Defendants' infringement of the '968 Patent, Plaintiff has  
17 suffered monetary damages and is entitled to no less than a reasonable royalty for  
18 Defendants' use of the claimed inventions of the '968 Patent, together with interest  
19 and costs as determined by the Court. Plaintiff will continue to suffer damages in the  
20 future.

21 87. Defendants' acts of direct and indirect infringement have caused and  
22 continue to cause damage to Plaintiff. Plaintiff is entitled to damages in accordance  
23 with 35 U.S.C. §§ 271 and 281 sustained as a result of Defendants' wrongful acts in  
24 an amount to be proven at trial.

## 25 **COUNT II**

26 (INFRINGEMENT OF U.S. PATENT NO. 9,183,085)

27 88. Plaintiff incorporates by reference and re-alleges the foregoing  
28 paragraphs as fully set forth herein.

1           89. Defendants have directly infringed and continue to directly infringe the  
2 '085 Patent, literally and/or under the doctrine of equivalents, by making, using,  
3 offering for sale, selling, and/or importing into the United States its SSD products.  
4 Defendants directly infringe claim 1 of the '085 Patent when its SSD products are  
5 installed and operated by its employees in a computer system, such as for gaming,  
6 personal computing, or data centers. Defendants directly infringe claim 1 when  
7 Defendants' employees use and test its SSD products.

8           90. **Exhibit E** is an exemplary claim chart, demonstrating on an element-  
9 by-element basis, how the Accused Products infringe claims of the '085 patent.

10          91. Claim 1 of the '085 Patent reads as follows:

11           1. A method of selecting an error correction coding (ECC)  
12 scheme, the method comprising:

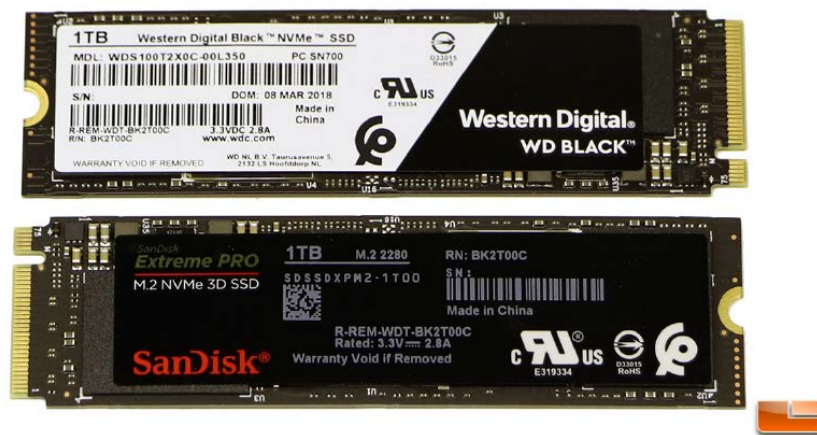
13           determining a bit error rate associated with a region  
14 comprising a fixed number of two or more flash memory  
15 pages or integer fractions thereof, wherein the two or more  
16 flash memory pages of a region can be read  
simultaneously, wherein the region stores at least data  
payload and primary and secondary ECC parity symbols  
corresponding to the data payload of the region;

17           comparing the determined bit error rate to one or more  
18 predetermined thresholds corresponding to a set of  
19 predefined gears comprising at least a first gear and a  
20 second gear, wherein the predefined gears correspond to  
21 different predefined ECC schemes, wherein the first gear  
22 has a different data payload size and correction capability  
than the second gear, wherein the amount of memory space  
allocated for the storage of data payload within the region  
varies between the first gear and the second gear to  
accommodate a varying number of parity symbols between  
the first gear and the second gear; and

23           selecting a gear from the set for the region based at least  
24 partly on the comparisons to the one or more  
predetermined thresholds;

25           wherein determining, comparing, and selecting are  
26 performed by an integrated circuit.  
27  
28

92. Defendants' SSD products perform a method of selecting an error correction coding (ECC) scheme. For example, WD Black-branded SSDs, which are used for gaming consoles and gaming PCs, Blue- and Green-branded SSDs, which are used for everyday PCs, Red-branded SSDs, which are used for Network Attached Storage (NAS), and Gold- and Ultrastar SSDs, which are used for data centers, all perform a method of selecting an error correction coding (ECC) scheme, as shown below:



Western Digital's new controller architecture means that the company has in-house development from the controller to the NAND. This gives WD tremendous design flexibility and they believe this new PCIe Gen 3 x4 controller is scalable and future-ready (think QLC NAND). Since WD designed everything they were able to design for low power and low latency as well as general performance. WD's new controller has three cores, is built on the 28nm process, features nCache 3.0 (marketing term for SLC Cache) for enhanced burst speeds, multi-gear LDPC (low-density parity-check) and hardware ECC to provide full SRAM and DRAM bit correction.

### [WD Black and SanDisk Review.](#)

The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read

[ECC/DSP White Paper](#) at 5.

93. The Accused Products determine a bit error rate (BER) associated with a region comprising a fixed number of two or more flash memory pages or integer fractions thereof, as demonstrated in the images below:

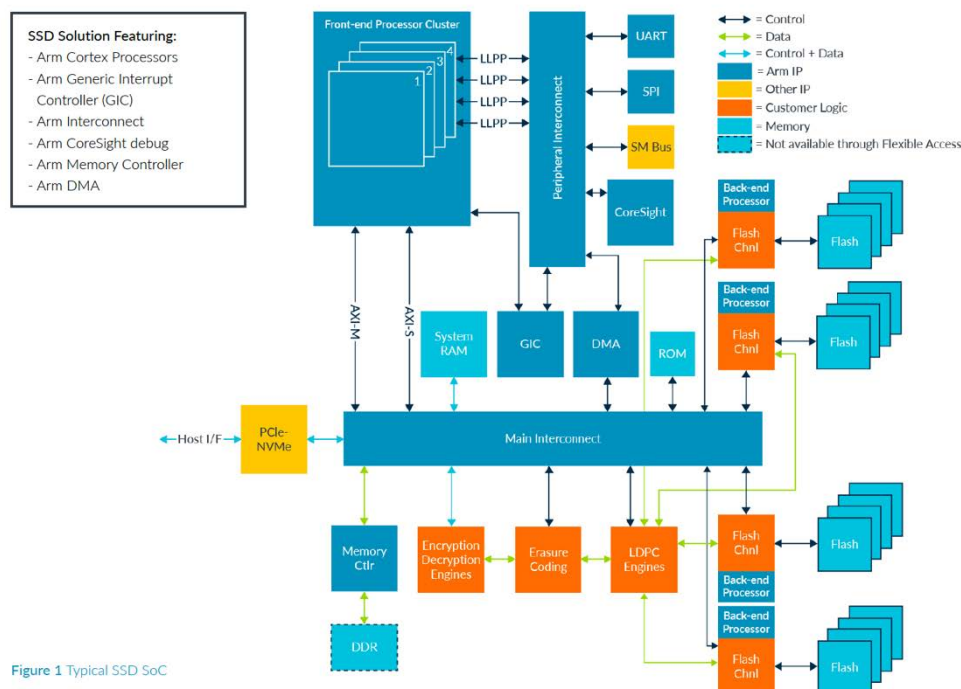
The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read

Idan Alrod et al., *The Application of ECC/DSP to Flash Memory* (Mar. 2021), Western Digital, [https://documents.westerndigital.com/content/dam/doc-library/en\\_us/assets/public/western-digital/collateral/white-paper/white-paper-the-application-of-ecc-dsp-to-flash-memory.pdf](https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-the-application-of-ecc-dsp-to-flash-memory.pdf) [hereinafter “ECC/DSP White Paper”].

To power the SSD, Western Digital uses a proprietary Arm-based multi-core eight-channel PCIe 4.0 x4 NVMe SSD controller that leverages a Micron DDR4 DRAM chip to deliver responsive performance. Western Digital references the controller as its WD BLACK G2. Outfitting the WD Black SN850 with a faster Gen4 PHY is great for performance, but with such fast bandwidth, power draw and heat output were a concern at 28 nm. Thus, WD BLACK G2 on a newer process node to better control those variables with TSMC’s 16nm FinFET technology.

[WD Black SN850 Review.](#)

## Solution Block Diagram



Front-end processors are usually Cortex-R processors but can sometimes be Cortex-A processors to support more intensive wear-leveilling algorithms.

Wear-leveilling is the process of systematically erasing and writing all NAND flash locations to ensure all locations wear out at about the same time. It may require moving unchanging data (cold data) already stored so a block can be erased and rewritten with rapidly changing data (hot data).

### Flash Translation Layer (FTL)

The **front-end processors** are responsible for maintaining the FTL tables that map logical addresses to physical addresses. As part of the FTL, the front-end processors also handle wear-leveilling algorithms to determine where the data should be written, which data should move, and which locations require garbage collection.

### Read Requests and Write Requests

Read and write requests arrive from the host over the **PCIe/NVMe** interface. The requests arrive in the form of descriptors that describe the parameters of a transfer. Write requests also carry the data to be written. These descriptors are written to either the **DDR** memory or a system RAM using a **DMA** operation from the host. For write requests, the user data is transferred to the controller DDR using a separate DMA operation.

## Arm Storage Solution for SSD Controllers at 4.

1  
2 A front-end processor is notified about the arrival of this descriptor. It then parses the  
3 descriptor to modify some of the parameters. In particular, the Logical Block Address (LBA)  
4 provided by the host must be modified to the physical address in the NAND where the  
5 read data is stored. With the correct physical address, the descriptor can be dispatched  
6 to the appropriate **flash channel** using a DMA.

7  
8 For read requests, the flash channel issues a read operation to the appropriate NAND  
9 die. When the data is available, it is moved from the NAND die buffer to the flash channel  
10 and then to the LDPC engines, as space is available. The **LDPC engines** perform ECC  
11 correction and data recovery from the media. If necessary, erasure coding operations  
12 are performed to recover data lost due to a block or page failure. Encrypted data is  
13 decrypted and stored in controller DDR. Finally, the user data is moved to host memory  
14 using a DMA operation to write into the DDR of the host, and then the host is notified  
15 that the data transfer completed.

16 For write requests, the user data in DDR is sent to the SSD data path of encryption,  
17 erasure coding, and LDPC encoding. When the encoded user data reaches the flash channel,  
18 the flash channel issues an operation to write the data to the NAND buffers. When all  
19 the data is in the NAND buffer, a program operation is issued to program the NAND. A  
20 completion response is generated by the flash channel that is sent back to the host.

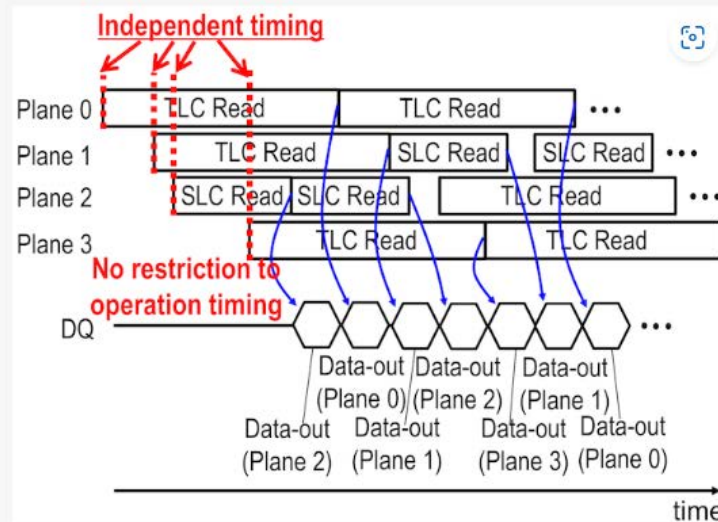
## 21 Arm Storage Solution for SSD Controllers at 5.

22 94. The highlighted text below shows The Accused Products support  
23 reading two or more memory pages of a region simultaneously.

24 Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This  
25 means that the delay of providing the host with response for any command falls under tight profile of probabilities  
26 it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears  
27 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single  
28 command requires higher latency gear-3 decoding, a different command can be attended simultaneously with  
29 Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel  
30 ECC&DSP technology is tailored to serve QoS in near optimal manner.

## 31 ECC/DSP White Paper at 7.

Now, another restriction on multi-plane operations is being relaxed: the timing of read operations in different planes doesn't need to line up. This makes it possible for one plane to perform multiple reads from SLC pages while another plane is performing a single slower read from TLC or QLC pages. This capability is called Asynchronous Independent (Multi-)Plane Read. The practical effect is that for read operations, a large 4-plane die can now match the performance of four smaller 1-plane dies. This mitigates many of the performance downsides that higher per-die capacity brings to SSDs that only have one or two dies per channel.



Billy Tallis, *2021 NAND Flash Updates from ISSCC: The Leaning Towers of TLC and QLC*, AnandTech (Feb. 19, 2021), <https://www.anandtech.com/show/16491/flash-memory-at-isscc-2021>.

95. The Accused Products can store in a region at least data payload and primary and secondary ECC parity symbols corresponding to the data payload of the region, as shown in the highlighted text below:

### Error Detection and Correction

One of the key factors to increase flash reliability as well as write endurance is the implementation of an Error Detection and Correction mechanism. The three most popular Error Correction algorithms used with NAND flash technology today are:

- BCH (Bose, Ray-Chaudhuri, Hocquenghem): BCH codes were invented in 1959 by Hocquenghem, and independently in 1960 by Bose and Ray Chaudhuri.
- LDPC (Low Density Parity Codes) invented by Gallager in 1961.

The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same:

1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature.
2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area.
3. When reading the data back, both data and stored ECC signature are read into the controller. A new ECC signature is generated, based upon the read-back data.
4. The newly created ECC signature is then compared to the original stored ECC signature. If both signatures are the same, no errors have occurred, and the data will be provided to the host. If the two signatures differ, the data will be corrected by the controller before being provided to the host.

Some flash controllers will write the corrected data back to the flash to optimize reliability, while others will not, since there is no guarantee that the data will not show errors again in the future. For 4KB page flash, typically 8 ECC signatures are created when writing data to the flash; one for each 512 bytes of data, as shown in Figure 10.

Western Digital, *Flash 101 and Flash Management* (Sep. 2023), [https://documents.westerndigital.com/content/dam/doc-library/en\\_us/assets/public/western-digital/collateral/white-paper/white-paper-sandisk-flash101-management.pdf](https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-sandisk-flash101-management.pdf) [hereinafter "Flash 101 White Paper"].

The figure shows a 4KB page with data payload of 4096 data payload and an associated spare area of 128 bytes of ECC bytes containing both primary and

secondary ECC bits.

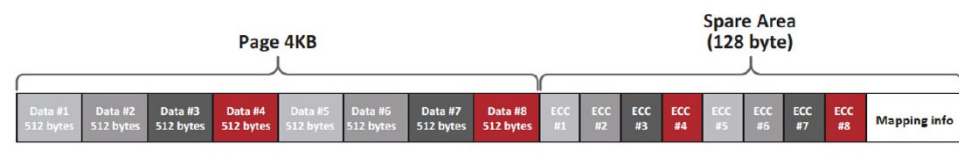


Figure 10: Four ECC signatures for 4KB page

[Flash 101 White Paper](#) at 7.

96. The image below shows how The Accused Products compare the determined bit error rate (BER) to one or more predetermined thresholds corresponding to a set of predefined gears comprising at least a first gear and a second gear, wherein the predefined gears correspond to different predefined ECC schemes.

In this example, three decoding gears are used. The color-coding is used to show the BER regions where each gear is likely to succeed the decoding.

Gear 1 (the green region in Figure 5 below) is based on the bit-flipping decoder mentioned above. Said Gear-1 is characterized by high-energy efficiency (low J/GB/sec). However, as the BER goes up, it fails at some point to decode with high probability. At that point, the higher resolution decoding gears kick in.

The blue curve in Figure 5 indicates the throughput of the system. Naturally, once NAND approaches the BER point where the 2nd gear kicks in, the throughput declines rapidly assuming constant power consumption is maintained.

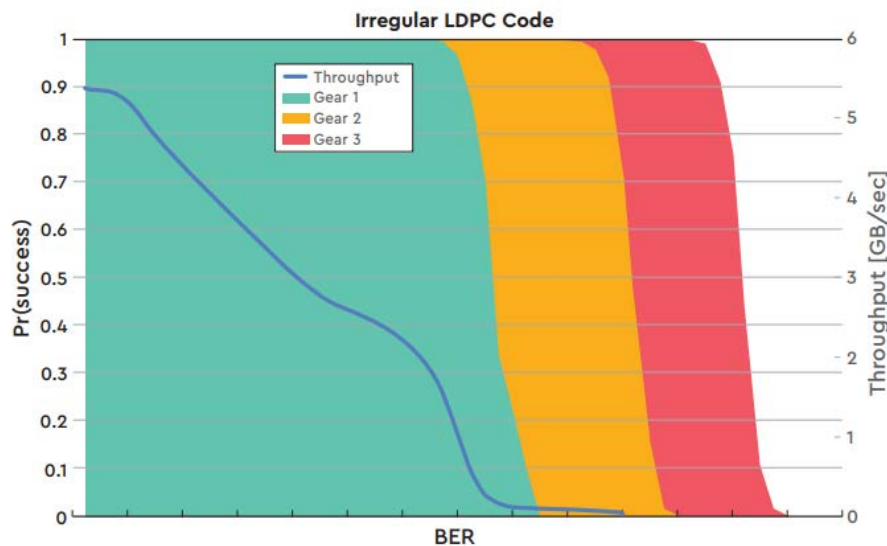
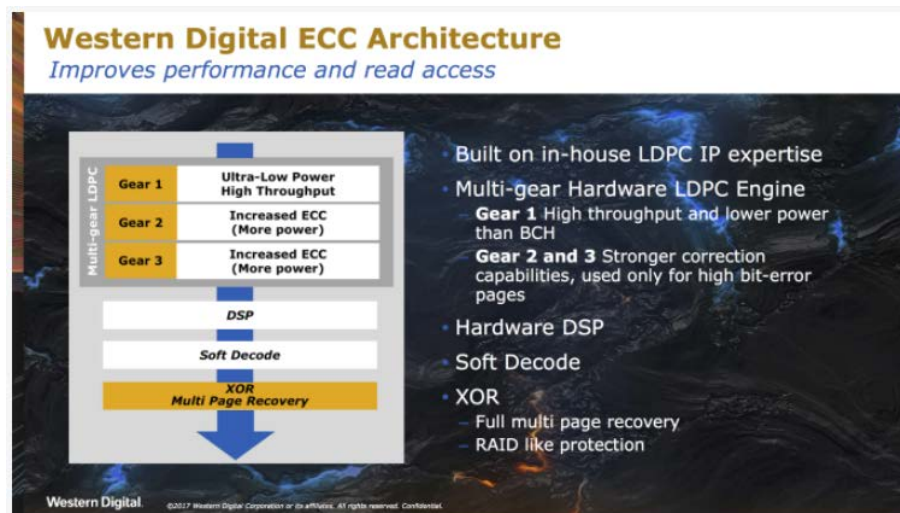


Figure 5: Example of various decoding gears correction capability and overall performance

When the BER is high, there is no point in spending decoder time trying to decode with lower gears, as this would only degrade performance by adding unnecessary latency to the decoding sequence. Consequently, the LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses the appropriate decoding gear.

[ECC/DSP White Paper](#) at 6.

97. The Accused Products include a first gear with a different data payload size and correction capability than a second gear. For example, Gear 1 corresponds to a high throughput and a ECC level while Gear 2 corresponds to a lower throughput and an increased ECC level (i.e., different payload size and correction capability), as shown in the image below:



Ganesh T S & Billy Tallis, The Western Digital NVMe Architecture - NAND & Controller, *The Western Digital WD Black 3D NAND SSD Review: EVO Meets Its Match*, AnandTech (Apr. 5, 2018), <https://www.anandtech.com/show/12543/the-western-digital-wd-black-3d-nand-ssd-review/2> [hereinafter “WD Black 3D Review”].

See also U.S. Patent No. 11,527,300, *Level Dependent Error Correction Code Protection in Multi-Level Non-Volatile Memory*, by Yang et al., assigned to Western Digital [hereinafter “Yang”], describing the adjustment of payload size and ECC parity size (correction capability) based on BER, corresponding to the criteria for selecting the “gear”.

FIG. 12 illustrates an ECC codeword 1200 and a dynamic or variable size of Components of the ECC codeword in accordance with one embodiment. The ECC codeword 1200 may comprise a payload and a parity section as introduced in FIG. 6A through FIG. 6C. The payload size 1202 and parity size 1204 of the ECC codeword 1200 may vary as indicated by the dotted lines. “Payload size” refers to a size measured in data storage units for a payload of an

1 ECC codeword. In one embodiment, a data storage unit is  
2 equal in size to a data sector. "Parity size" refers to a size  
3 measured in bits or bytes, or some other data storage  
4 measurement unit, for a parity section. The unit of measure  
5 for a parity size may depend on the ECC method being used  
6 to encode and decode the ECC codewords.

7 Yang at 33:12-39.

8 Determining the coding rate may comprise increasing the  
9 payload size 1202 in response to an attribute indicating a  
10 greater data integrity for data stored on the multi-level page  
11 that is assigned to the ECC codeword 1200. In particular,  
12 the payload size 1202 may be increased, and the parity size  
13 1204 decreased, based on the data integrity of the ECC  
14 codeword 1200 being higher in relation to other multi-level  
15 pages that will be stored on the same multi-level storage  
16 cells. Alternatively, or in addition, the payload size 1202  
17 may be decreased, and the parity size 1204 increased, based  
18 on the data integrity of the ECC codeword 1200 being  
19 lower in relation to other multi-level pages that will be  
20 stored on the same multi-level storage cells.

21 Yang at 34:4-16.

22 98. The image below shows how The Accused Products allocate memory  
23 space for the storage of data payload within the region varies between the first gear  
24 and the second gear to accommodate a varying number of parity symbols between  
25 the first gear and the second gear. The memory space allocated for the storage of data  
26 payload is reduced as the flash controller transitions into a higher gear. The reduction  
27 of storage for data payload is caused by the increased of parity bits required by a  
28 more complex ECC used in higher gears.

The blue curve in Figure 5 indicates the throughput of the system. Naturally, once NAND approaches the BER point where the 2nd gear kicks in, the throughput declines rapidly assuming constant power consumption is maintained.

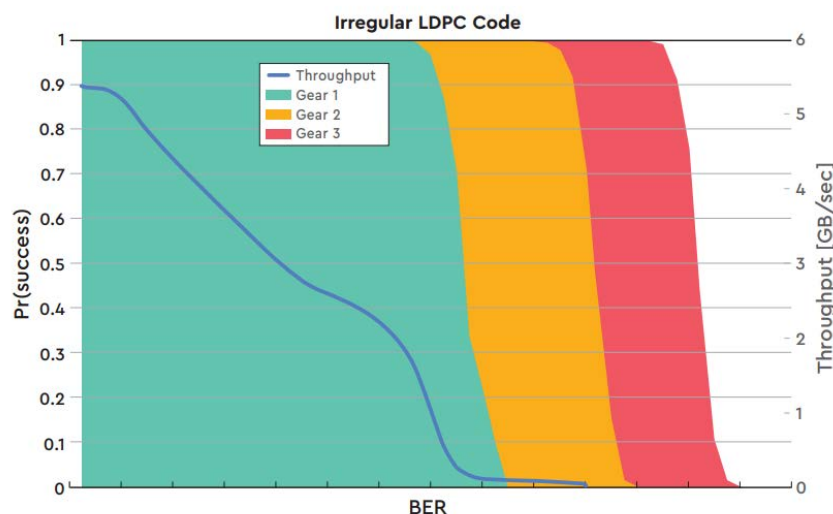
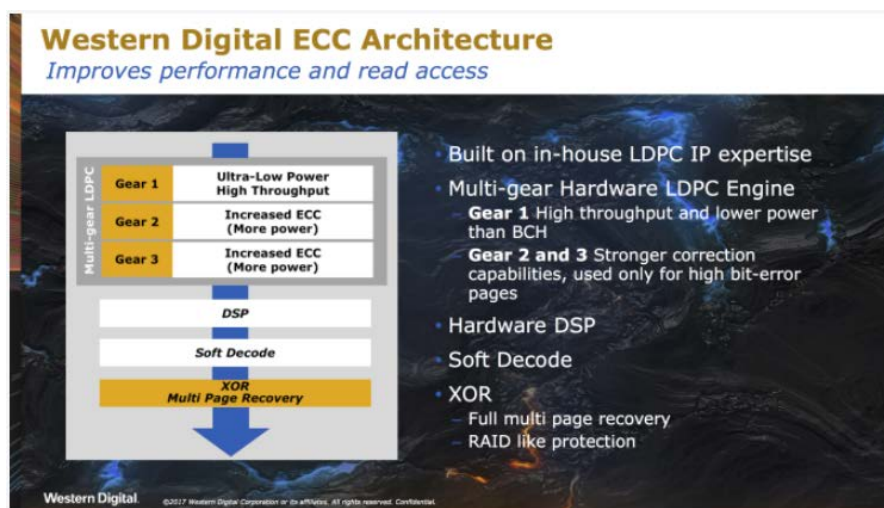


Figure 5: Example of various decoding gears correction capability and overall performance

When the BER is high, there is no point in spending decoder time trying to decode with lower gears, as this would only degrade performance by adding unnecessary latency to the decoding sequence. Consequently, the LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses the appropriate decoding gear.

[ECC/DSP White Paper](#) at 6.



[WD Black 3D Review](#).

See also [ECC/DSP White Paper](#) at 11 (“This feature is set to accommodate full usage of the available NAND cells in the physical page while enabling flexibility in code rate for numerous applications / scenarios.”).

See also [Yang](#), assigned to Western Digital.

1 In certain embodiments, the payload size 1202 and parity  
2 size 1204 may be adjusted based on a data integrity  
3 attribute for a particular non-volatile storage media, storage  
4 cell, set of storage cells or the like. "Data integrity" refers  
5 to an attribute or measure of data, or a data sample,  
6 indicating whether the data is accurate, not erroneous, and  
7 unchanged from a prior transmission or recording of the  
8 data. In certain embodiments, data integrity is an objective  
9 characteristic. In other embodiments, data integrity may be  
10 expressed in relation to a spectrum in which one end  
11 represents no, or very low data integrity and the opposite  
12 end represents perfect, or very high data integrity.

13 [Yang](#) at 33:45-56.

14 The receiver 1304 may coordinate with the address  
15 allocator 1306 to determine where the write data 1312 will  
16 be stored. The address allocator 1306 may determine a  
17 multilevel page to store a set of data blocks associated with  
18 a set of write commands 1310. "Address allocator" refers  
19 to any circuit, sub-circuit, electronic component, hardware,  
20 software, firmware, module, logic, device, or apparatus  
21 configured, programmed, designed, arranged, or  
22 engineered to determine, assign and/or allocate a physical  
23 block address for a particular logical block address.

24 The packetizer 1308 may coordinate with the receiver 1304  
25 and address allocator 1306 to prepare the write data 1312  
26 for storage on the non-volatile storage media. "Packetizer"  
27 refers to any hardware, software, firmware, circuit,  
28 component, module, logic, device, or apparatus  
configured, programmed, designed, arranged, or  
engineered to organize a set of source data into one or more  
data packets. In one embodiment, the source data may  
comprise user data for one or more storage operations. The  
packetizer may be configured to include a header, footer  
and/or redundancy data in each data packet. The packetizer  
may be configured to include padding data or filler data to  
combine with a remainder of the source data that does not  
completely fill a data packet.

The packetizer 1308 may combine the write data 1312 for  
the set of data blocks into a payload for an ECC codeword.  
The packetizer 1308 may coordinate with the address  
allocator 1306 to determine which multi-level page a  
particular ECC codeword is assigned to be stored on. Based  
on a determined multi-level page for the particular ECC  
codeword, the packetizer 1308 may change a payload size  
for the payload of the particular ECC codeword in response  
to a reliability attribute of the determined multi-level page  
satisfying a threshold.

27 [Yang](#) at 34:62-35:28.

99. The Accused Products select a gear from the set for the region based at least partly on the comparisons to the one or more predetermined thresholds, as shown in the image and highlighted text below:

In this example, three decoding gears are used. The color-coding is used to show the BER regions where each gear is likely to succeed the decoding.

Gear 1 (the green region in Figure 5 below) is based on the bit-flipping decoder mentioned above. Said Gear-1 is characterized by high-energy efficiency (low J/GB/sec). However, as the BER goes up, it fails at some point to decode with high probability. At that point, the higher resolution decoding gears kicks in.

The blue curve in Figure 5 indicates the throughput of the system. Naturally, once NAND approaches the BER point where the 2nd gear kicks in, the throughput declines rapidly assuming constant power consumption is maintained.

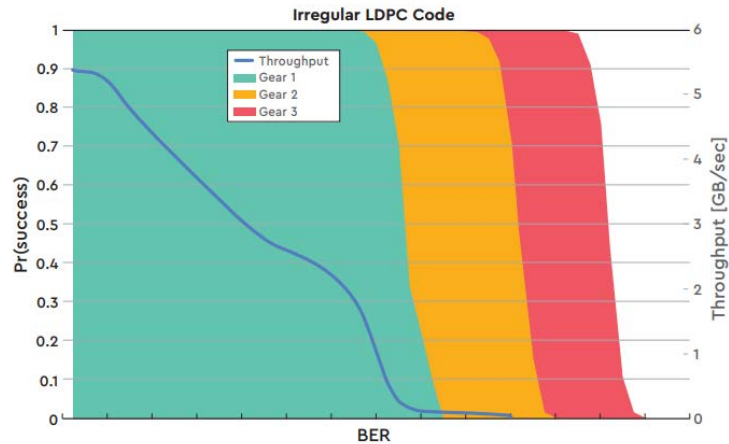


Figure 5: Example of various decoding gears correction capability and overall performance

When the BER is high, there is no point in spending decoder time trying to decode with lower gears, as this would only degrade performance by adding unnecessary latency to the decoding sequence. Consequently, the LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses the appropriate decoding gear.

[ECC/DSP White Paper](#) at 6.

100. The Accused Products determine, compare and select using an integrated circuit.

Furthermore, the parallelism of each decoding gear is dimensioned according to its usage probability (given the memory BER distribution) and the overall required decoding throughput. Thus, the number of costly high-resolution processing units instantiated for the full resolution BP decoder, which is rarely used ("safety net"), could be much lower than the number of simple BF processing units. This approach significantly reduces the ASIC footprint with a negligible impact on overall sustained decoding throughput.

[ECC/DSP White Paper](#) at 7.

101. Defendants have infringed, and continue to infringe, the claims of the '085 Patent in the United States, by making, using, offering for sale, selling, and/or importing the Accused Products in violation of 35 U.S.C. § 271(a). For example, Defendants directly infringe at least claim 1 of the '085 Patent when its SSD products are installed and operated by its employees in a computer system, such

1 as for gaming, personal computing, or data centers, and when Defendants' employees  
2 use and test its SSD products.

3 102. On January 23, 2024, Plaintiff sent a notice letter to Western Digital,  
4 notifying them that they were infringing the Asserted Patents. Western Digital's  
5 infringement of the '085 Patent has been willful and intentional under the standard  
6 announced in *Halo Elecs., Inc. v. Pulse Elecs., Inc.*, 579 U.S. 93 (2016). Western  
7 Digital did not reply to that letter.

8 103. Western Digital has willfully infringed the '085 Patent by refusing to  
9 take a license and continuing to make, use, test, sell, license, and/or offer for  
10 sale/license the '085 Patent Accused Products. Instead of taking a license, Western  
11 Digital has opted to make the business decision to "efficiently infringe" the '085  
12 Patent. In doing so, Western Digital willfully infringes the '085 Patent.

13 104. Defendants also have infringed, and continue to infringe the claims of  
14 the '085 Patent by actively inducing others to use the Accused Products. Defendants'  
15 users, customers, agents or other third parties who use the Accused Products in  
16 accordance with Defendants' instructions infringe the claims of the '085 Patent, in  
17 violation of 35 U.S.C. § 271(a). Defendants induce its customers to use its SSD  
18 products for the benefits of higher performance, reduced size and power, and  
19 increased reliability compared to other SSD products. Defendants are thereby liable  
20 for infringement of the '085 Patent under 35 U.S.C. § 271(b).

21 105. Defendants' users, customers, agents or other third parties who use the  
22 Accused Products in accordance with Defendants' instructions infringe the claims of  
23 the '085 Patent, in violation of 35 U.S.C. § 271(b). Defendants intentionally instruct  
24 its customers to infringe through support information, demonstrations, brochures,  
25 videos, and user guides, such as those located at:

26 <https://www.westerndigital.com/support>;

27 <https://support.wdc.com/contact.aspx?lang=en>;

28 <https://www.westerndigital.com/support/category-selection>;

1 [https://www.youtube.com/channel/UC\\_M0BlntDVSblWg6ggUa7UQ](https://www.youtube.com/channel/UC_M0BlntDVSblWg6ggUa7UQ;);  
2 [https://www.youtube.com/watch?v=L0zZtwRFj0E](https://www.youtube.com/watch?v=L0zZtwRFj0E;);  
3 <https://www.youtube.com/westerndigital>; and  
4 <https://www.youtube.com/c/westerndigitalcorporation>.

5 106. Defendants are liable as contributory infringers of the '085 Patent under  
6 35 U.S.C. 271(c) by having offered to sell, sold and imported and continuing to offer  
7 to sell, selling, and importing into the United States its SSD products, to be especially  
8 made or adapted for use in an infringement of the '085 Patent. Defendants' SSD  
9 products are key components in gaming consoles and gaming PCs, computers,  
10 everyday PCs, Network Attached Storage (NAS) devices, servers and data centers.  
11 These SSD products are material components for use in practicing the '085 Patent  
12 and are specifically made and are not a staple article of commerce suitable for  
13 substantial noninfringing use. Defendants supplied these components with  
14 knowledge of the '085 Patent and with knowledge that these components constitute  
15 material parts of the claimed inventions of the '085 Patent.

16 107. As a result of Defendants' infringement of the '085 Patent, Plaintiff has  
17 suffered monetary damages and is entitled to no less than a reasonable royalty for  
18 Defendants' use of the claimed inventions of the '085 Patent, together with interest  
19 and costs as determined by the Court. Plaintiff will continue to suffer damages in the  
20 future.

21 108. Defendants are on notice of its infringement by no later than the filing  
22 and service of this Complaint. By the time of trial, Defendants will have known and  
23 intended (since receiving such notice) that their continued actions would actively  
24 induce the infringement of the '085 Patent.

25 109. Defendants' acts of direct and indirect infringement have caused and  
26 continue to cause damage to Plaintiff. Plaintiff is entitled to damages in accordance  
27 with 35 U.S.C. §§ 271 and 281 sustained as a result of Defendants' wrongful acts in  
28 an amount to be proven at trial.

**COUNT III**

(INFRINGEMENT OF U.S. PATENT NO. 8,601,346)

110. Plaintiff incorporates by reference and re-alleges the foregoing paragraphs as fully set forth herein.

111. Defendants have directly infringed, and continue to directly infringe, one or more claims of the '346 Patent, including at least claim 1 of the '346 Patent, literally and/or under the doctrine of equivalents, by or through making, using, offering for sale, selling within the United States and/or importing into the United States its SSD products.

112. **Exhibit F** is an exemplary claim chart, demonstrating on an element-by-element basis, how the Accused Products infringe claims of the '346 patent.

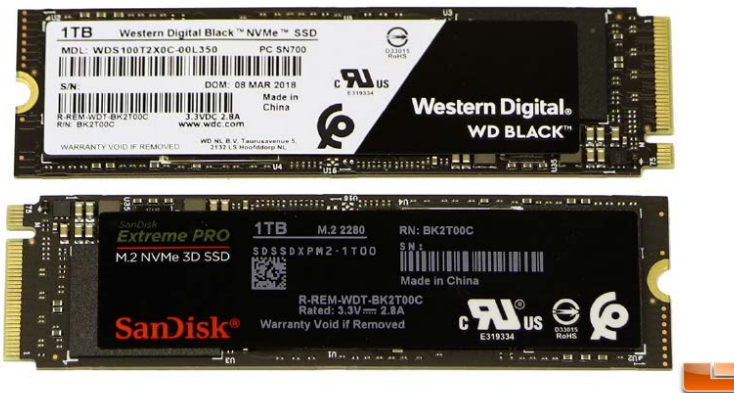
113. Claim 1 of the '346 Patent reads as follows:

1. A nonvolatile memory controller for performing a data stripe operation on a plurality of data blocks, the nonvolatile memory controller comprising:

a plurality of command processing units, each command processing unit of the plurality of command processing units configured to receive a command of a plurality of commands for performing the data stripe operation, the plurality of commands including a plurality of data update commands and a parity write command, each command processing unit of the plurality of command processing units receiving a data update command of the plurality of data update commands configured to request a data block of the plurality of data blocks based on the data update command, receive the data block in response to the request, and write the data block to a nonvolatile memory device; and

a parity calculator coupled to the plurality of command processing units, the parity calculator further comprising a context memory including a page frame, the parity calculator configured to receive the plurality of data blocks as a sequence of data blocks, to generate a parity block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks, without storing each data block in a data buffer, the command processing unit receiving the parity write command configured to write the parity block to a nonvolatile memory based on the parity write command.

114. Defendants make, use, sell, offer for sale and import SSD products that include a nonvolatile memory controller for performing a data stripe operation on a plurality of data blocks. For example, WD Black-branded SSDs, which are used for gaming consoles and gaming PCs, Blue- and Green-branded SSDs, which are used for everyday PCs, Red-branded SSDs, which are used for Network Attached Storage (NAS), and Gold- and Ultrastar SSDs, which are used for data centers, all include a nonvolatile memory controller for performing a data stripe operation on a plurality of data blocks, as shown below:



Western Digital's new controller architecture means that the company has in-house development from the controller to the NAND. This gives WD tremendous design flexibility and they believe this new PCIe Gen 3 x4 controller is scalable and future-ready (think QLC NAND). Since WD designed everything they were able to design for low power and low latency as well as general performance. WD's new controller has three cores, is built on the 28nm process, features nCache 3.0 (marketing term for SLC Cache) for enhanced burst speeds, multi-gear LDPC (low-density parity-check) and hardware ECC to provide full SRAM and DRAM bit correction.



Nathan Kirsch, *WD Black NVMe 3D and SanDisk Extreme PRO NVMe 3D 1TB*

1 SSD Review, Legit Reviews (Apr. 5, 2018), [https://www.legitreviews.com/wd-](https://www.legitreviews.com/wd-black-nvme-3d-sandisk-extreme-pro-nvme-3d-1tb-ssd-review_204268)  
 2 [black-nvme-3d-sandisk-extreme-pro-nvme-3d-1tb-ssd-review\\_204268](https://www.legitreviews.com/wd-black-nvme-3d-sandisk-extreme-pro-nvme-3d-1tb-ssd-review_204268) [hereinafter  
 3 “WD Black and SanDisk Review”].

4 115. The images and quotes below show how The Accused Products include  
 5 command processing units, such as ARM processor cores. The processing units  
 6 receive commands, including a command to perform a data stripe operation. For  
 7 example:

8 The new controller has a tri-core architecture (probably  
 9 using Arm Cortex-cores Fabricated in a 28nm process. It is  
 10 designed to be scalable – the current controller can  
 11 interface with the host using a PCIe 3.0 x4 link, or an x2  
 12 link as in the Western Digital SN520. The architecture of  
 13 the controller also allows future products using variants to  
 14 come to market faster and with newer features. It also  
 15 allows Western Digital to segment their NVMe product  
 stack. The controller in the Western Digital Black 3D  
 NAND SSD is optimized for client workloads including  
 PC gaming and high-performance commercial  
 applications. Western Digital expects this new controller  
 architecture to last at least until NVMe SSDs move beyond  
 PCIe 3 x4 interfaces.

16 [WD Black 3D Review.](#)

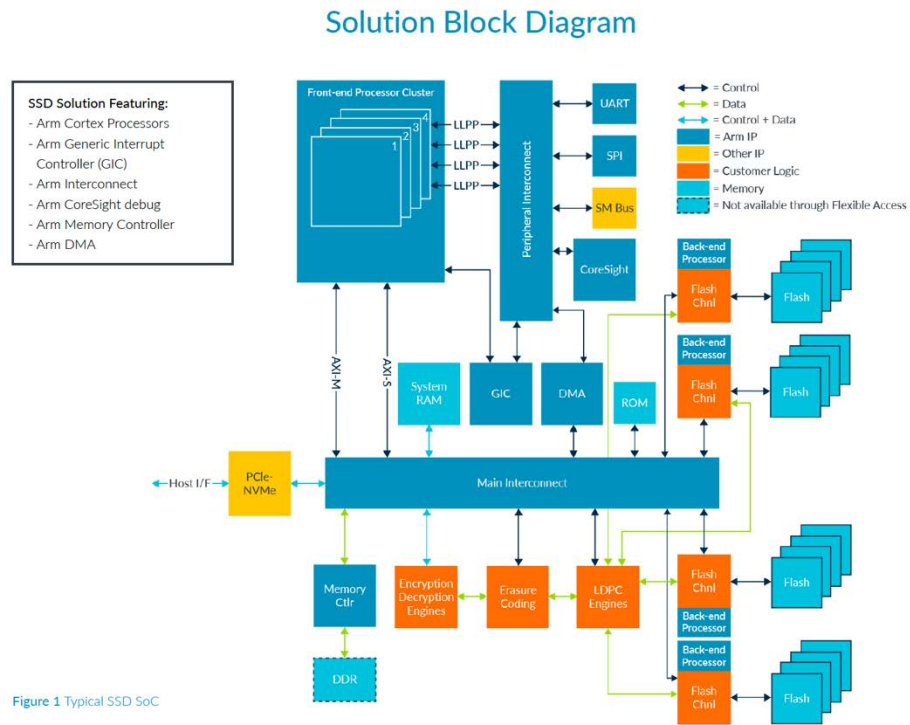
17 WD’s new controller has three cores, is built on the 28nm  
 18 process, ...

19 [WD Black and SanDisk Review.](#)

20 To power the SSD, WD uses a proprietary Arm-based  
 21 multi-core eight-channel PCIe 4.0 x4 NVMe SSD  
 22 controller that leverages a Micron DDR4 DRAM chip to  
 23 deliver responsive performance. Western Digital  
 24 references the controller as its WD BLACK G2. Outfitting  
 25 the Western Digital Black SN850 with a faster Gen4 PHY  
 is great for performance, but with such fast bandwidth,  
 power draw and heat output were a concern at 28nm. Thus,  
 like the controllers from competing manufacturers,  
 Western Digital opted to build the WD BLACK G2 on a  
 newer process node to better control those variables with  
 TSMC’s 16nm FinFET technology.

26 Sean Webster, *WD Black SN850 M.2 NVMe SSD Review: Top-Tier Storage for*  
 27 *Gamers and Pros (Updated)*, Tom’s Hardware (Apr. 1, 2021),  
 28 <https://www.tomshardware.com/reviews/wd-black-sn850-m-2-nvme-ssd-review>

[hereinafter “WD Black SN850 Review”].



Front-end processors are usually Cortex-R processors but can sometimes be Cortex-A processors to support more intensive wear-levelling algorithms.

Wear-levelling is the process of systematically erasing and writing all NAND flash locations to ensure all locations wear out at about the same time. It may require moving unchanging data (cold data) already stored so a block can be erased and rewritten with rapidly changing data (hot data).

#### Flash Translation Layer (FTL)

The front-end processors are responsible for maintaining the FTL tables that map logical addresses to physical addresses. As part of the FTL, the front-end processors also handle wear-levelling algorithms to determine where the data should be written, which data should move, and which locations require garbage collection.

#### Read Requests and Write Requests

Read and write requests arrive from the host over the PCIe/NVMe interface. The requests arrive in the form of descriptors that describe the parameters of a transfer. Write requests also carry the data to be written. These descriptors are written to either the DDR memory or a system RAM using a DMA operation from the host. For write requests, the user data is transferred to the controller DDR using a separate DMA operation.

Arm Ltd., *Arm Storage Solution for SSD Controllers* at 4 (Sept. 2020), <https://www.arm.com/-/media/global/solutions/storage/arm-storage-solution-for-ssd-solutions-brief.pdf?rev=3530e7536aae437aa2d7acf1704fe25b&revision=3530e753-6aae-437a-a2d7-acf1704fe25b> [hereinafter “Arm Storage Solution for SSD Controllers”].

A front-end processor is notified about the arrival of this descriptor. It then parses the descriptor to modify some of the parameters. In particular, the Logical Block Address (LBA) provided by the host must be modified to the physical address in the NAND where the read data is stored. With the correct physical address, the descriptor can be dispatched to the appropriate **flash channel** using a DMA.

For read requests, the flash channel issues a read operation to the appropriate NAND die. When the data is available, it is moved from the NAND die buffer to the flash channel and then to the LDPC engines, as space is available. The LDPC engines perform ECC correction and data recovery from the media. If necessary, erasure coding operations are performed to recover data lost due to a block or page failure. Encrypted data is decrypted and stored in controller DDR. Finally, the user data is moved to host memory using a DMA operation to write into the DDR of the host, and then the host is notified that the data transfer completed.

For write requests, the user data in DDR is sent to the SSD data path of encryption, erasure coding, and LDPC encoding. When the encoded user data reaches the flash channel, the flash channel issues an operation to write the data to the NAND buffers. When all the data is in the NAND buffer, a program operation is issued to program the NAND. A completion response is generated by the flash channel that is sent back to the host.

#### Arm Storage Solution for SSD Controllers at 5.

Defendants' nonvolatile memory controllers include RAID scheme support, which inherently includes stripe operations.

The Sentinel ECC&DSP error correction is based on state-of-the-art Low Density Parity Check (LDPC) coding and provides a full suite of NAND DSP (Digital Signal Processing) services, including data randomization or shaping, NAND health metering via Bit Error Rate (BER) estimation, ECC-based read thresholds calibration, and NAND defect protection and recovery via XOR based RAID scheme support.

Idan Alrod et al., *The Application of ECC/DSP to Flash Memory* (Mar. 2021), Western Digital, [https://documents.westerndigital.com/content/dam/doc-library/en\\_us/assets/public/western-digital/collateral/white-paper/white-paper-the-application-of-ecc-dsp-to-flash-memory.pdf](https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-the-application-of-ecc-dsp-to-flash-memory.pdf) [hereinafter "ECC/DSP White Paper"] at 5.

## Joint LDPC and RAID Decoding for Enterprise SSD

Certain flash applications, such as enterprise SSD, require an exceptionally high level of data reliability. In these applications, the probability of losing data – no matter what caused it – must be exceptionally low. More specifically, the system must be able to cope with flash failure modes that do not only include random errors, but failures of entire pages. These might include word line failures of various sorts, block failures, or even die-level faults.

One existing strategy is to use RAID parity. This method has many variants depending on reliability requirements (how many failed sectors can the system recover from), locality of recovery (how many read and transfer operations required for a single recovery), and other system tradeoffs. The simplest of such schemes is the plain-vanilla variant, where recovery from a single sector failure is possible. This requires one parity sector, which holds the RAID parity of all other sectors. Upon failure of one of the sectors, reconstruction is possible by performing RAID recovery on all the non-failing sectors. Of course, this simple scheme is equally effective if the failing sector is due to a large number of random errors, which is not correctable by the ECC. The following two are simple observations on this scheme:

[ECC/DSP White Paper](#) at 11.

### Appendix – Case Study [FMS 2016, Patent Application US20170255518A1]

Let's assume a standard RAID stripe of length 32. This means that 31 sectors are protected by an additional parity sector. The over-provisioning used by this RAID scheme is around 3%. Next, let's assume an LDPC-based ECC solution that has approximately 10% over-provisioning.

If the LDPC and RAID layers were to be combined, one could observe that the result is a code with extra 3% overprovisioning and a code word size that is x32 larger than the original. A Tanner graph representing a unified LDPC-RAID code is shown in Figure 13 below. It shows a Tanner graph of a combined LDPC-RAID scheme. The smaller graphs  $G_0, G_1, \dots, G_{30}$  represent the information sectors and  $G_{31}$  is the parity sector.

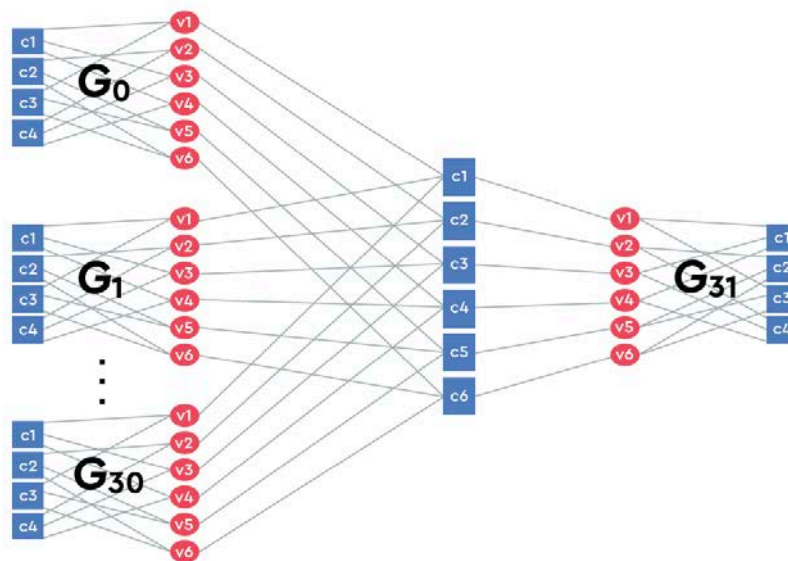


Figure 13: Tanner graph of a combined LDPC-RAID scheme

[ECC/DSP White Paper](#) at 12.

**What are RAID 50 and 60? I see you have a product that supports them. —**

RAID 50 and 60 are very similar to RAID 10, as they are all "nested" RAIDs. The first number in the type — 5 and 6, respectively — represents what subset they are built with, either RAID 5 arrays or RAID 6 arrays. The second number represents the RAID type the first one is "nested" into; in this case, it's RAID 0.

Let's dive a bit deeper.

So, with RAID 50:

- Two RAID 5 subsets **stripe** across each other in RAID 0.
- With eight drives, four drives act as RAID 5 with their own parity. Another four do the same with data split between two sets.
- Any one of the four drives in each set could fail. That's one to two drives — two if they're not within the same subset.

So, with RAID 60:

- Two RAID 6 subsets stripe across each other in RAID 0.
- With eight drives, any one of the four drives in each set could fail. That's two to four drives — four if two are from one subset and two are from the other subset.

RAID 50 vs. RAID 60:

- RAID 50 will have faster performance than RAID 60.
- RAID 60, like RAID 6, has parity for all data written twice. That's why you "lose" two disks of capacity per RAID 6 subset.
- With RAID 50, it's one disk per subset.

Western Digital, *What is RAID Storage?*,  
<https://www.westerndigital.com/solutions/raid> [hereinafter "RAID Storage Guide"].

116. The Accused Products include a plurality of data update commands, which write data to a nonvolatile controller to update the contents of nonvolatile memory, and a parity write command, as shown below:

### **6.15 Write command**

The Write command writes data and metadata, if applicable, to the I/O controller for the logical blocks indicated.

[NVMe Express Specification](#) v1.4 at 268.

The Sentinel ECC&DSP error correction is based on state-of-the-art Low Density Parity Check (LDPC) coding and provides a full suite of NAND DSP (Digital Signal Processing) services, including data randomization or shaping, NAND health metering via Bit Error Rate (BER) estimation, ECC-based read thresholds calibration, and NAND defect protection and recovery via XOR based RAID scheme support.

[ECC/DSP White Paper](#) at 5.

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Certain flash applications, such as enterprise SSD, require an exceptionally high level of data reliability. In these applications, the probability of losing data – no matter what caused it – must be exceptionally low. More specifically, the system must be able to cope with flash failure modes that do not only include random errors, but failures of entire pages. These might include word line failures of various sorts, block failures, or even die-level faults.

One existing strategy is to use RAID parity. This method has many variants depending on reliability requirements (how many failed sectors can the system recover from), locality of recovery (how many read and transfer operations required for a single recovery), and other system tradeoffs. The simplest of such schemes is the plain-vanilla variant, where recovery from a single sector failure is possible. This requires one parity sector, which holds the RAID parity of all other sectors. Upon failure of one of the sectors, reconstruction is possible by performing RAID recovery on all the non-failing sectors. Of course, this simple scheme is equally effective if the failing sector is due to a large number of random errors, which is not correctable by the ECC. The following two are simple observations on this scheme:

[ECC/DSP White Paper](#) at 11.

### Appendix – Case Study [FMS 2016, Patent Application US20170255518A1]

Let's assume a standard RAID stripe of length 32. This means that 31 sectors are protected by an additional parity sector. The over-provisioning used by this RAID scheme is around 3%. Next, let's assume an LDPC-based ECC solution that has approximately 10% over-provisioning.

If the LDPC and RAID layers were to be combined, one could observe that the result is a code with extra 3% overprovisioning and a code word size that is x32 larger than the original. A Tanner graph representing a unified LDPC-RAID code is shown in Figure 13 below. It shows a Tanner graph of a combined LDPC-RAID scheme. The smaller graphs  $G_0, G_1, \dots, G_{30}$  represent the information sectors and  $G_{31}$  is the parity sector.

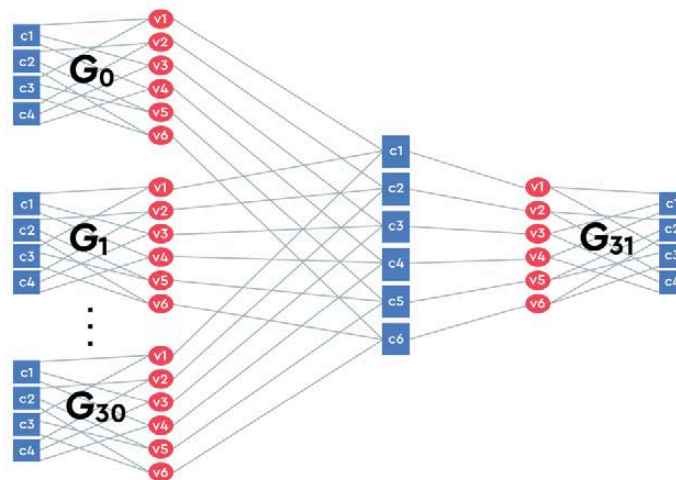


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[ECC/DSP White Paper](#) at 12.

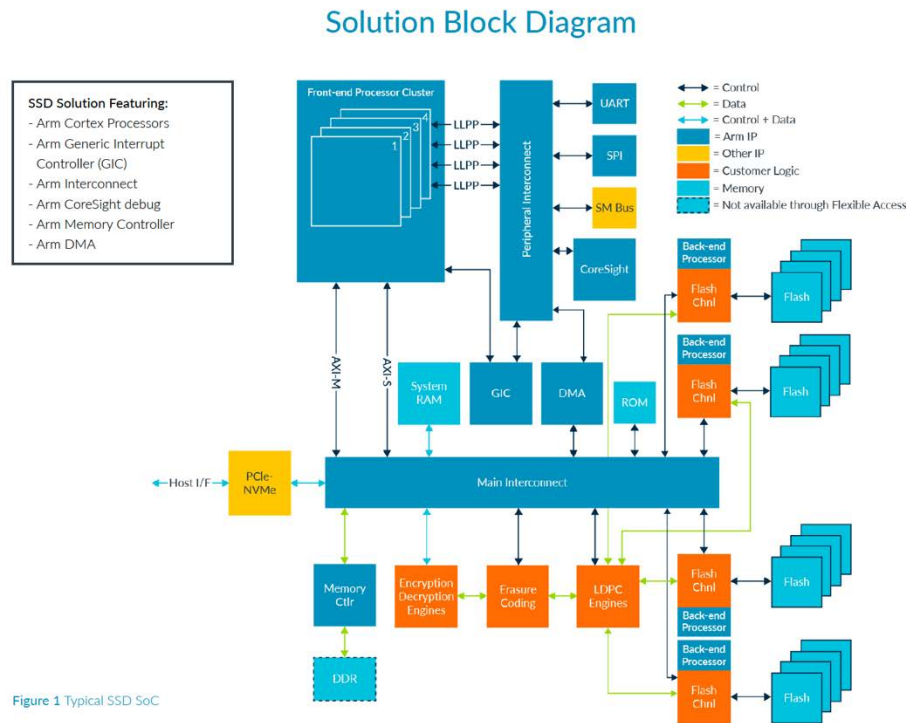
117. For The Accused Products, each command processing unit of the plurality of command processing units receiving a data update command of the plurality of data update commands configured to request a data block of the plurality of data blocks based on the data update command, receive the data block in response to the request, and write the data block to a nonvolatile memory device, as shown in

the quotes and pictures below:

## 6.15 Write command

The Write command writes data and metadata, if applicable, to the I/O controller for the logical blocks indicated.

[NVMe Express Specification](#) at 268.



Front-end processors are usually Cortex-R processors but can sometimes be Cortex-A processors to support more intensive wear-leveling algorithms.

Wear-leveling is the process of systematically erasing and writing all NAND flash locations to ensure all locations wear out at about the same time. It may require moving unchanging data (cold data) already stored so a block can be erased and rewritten with rapidly changing data (hot data).

### Flash Translation Layer (FTL)

The **front-end processors** are responsible for maintaining the FTL tables that map logical addresses to physical addresses. As part of the FTL, the front-end processors also handle wear-leveling algorithms to determine where the data should be written, which data should move, and which locations require garbage collection.

### Read Requests and Write Requests

Read and write requests arrive from the host over the **PCIe/NVMe** interface. The requests arrive in the form of descriptors that describe the parameters of a transfer. Write requests also carry the data to be written. These descriptors are written to either the **DDR** memory or a system RAM using a **DMA** operation from the host. For write requests, the user data is transferred to the controller DDR using a separate DMA operation.

[Arm Storage Solution for SSD Controllers](#) at 4.

1 A front-end processor is notified about the arrival of this descriptor. It then parses the  
2 descriptor to modify some of the parameters. In particular, the Logical Block Address (LBA)  
3 provided by the host must be modified to the physical address in the NAND where the  
4 read data is stored. With the correct physical address, the descriptor can be dispatched  
to the appropriate **flash channel** using a DMA.

5 For read requests, the flash channel issues a read operation to the appropriate NAND  
6 die. When the data is available, it is moved from the NAND die buffer to the flash channel  
7 and then to the LDPC engines, as space is available. The **LDPC engines** perform ECC  
8 correction and data recovery from the media. If necessary, erasure coding operations  
9 are performed to recover data lost due to a block or page failure. Encrypted data is  
decrypted and stored in controller DDR. Finally, the user data is moved to host memory  
using a DMA operation to write into the DDR of the host, and then the host is notified  
that the data transfer completed.

10 For write requests, the user data in DDR is sent to the SSD data path of encryption,  
11 erasure coding, and LDPC encoding. When the encoded user data reaches the flash channel,  
12 the flash channel issues an operation to write the data to the NAND buffers. When all  
13 the data is in the NAND buffer, a program operation is issued to program the NAND. A  
completion response is generated by the flash channel that is sent back to the host.

14 [Arm Storage Solution for SSD Controllers](#) at 5.

15 118. The Accused Products include a parity calculator coupled to the  
16 plurality of command processing units. The Accused Products rely on LDPC (Low  
17 Density Parity Calculation) Error Correcting Code (ECC) to quickly correct a limited  
18 number of random bit errors within an SSD. A RAID scheme is additionally used to  
19 recover more slowly when ECC does not allow data to be read reliably (for example,  
20 NAND defect protection or a sector or drive failure) by storing redundant data for a  
21 stripe. As shown in the text below, a parity calculator is used to create one or more  
22 redundant data blocks for RAID storage.

23 The Sentinel ECC&DSP error correction is based on state-of-the-art Low Density Parity Check (LDPC) coding and  
24 provides a full suite of NAND DSP (Digital Signal Processing) services, including data randomization or shaping,  
25 NAND health metering via Bit Error Rate (BER) estimation, ECC-based read thresholds calibration, and NAND defect  
protection and recovery via XOR based RAID scheme support.

26 [ECC/DSP White Paper](#) at 5.

## Joint LDPC and RAID Decoding for Enterprise SSD

Certain flash applications, such as enterprise SSD, require an exceptionally high level of data reliability. In these applications, the probability of losing data – no matter what caused it – must be exceptionally low. More specifically, the system must be able to cope with flash failure modes that do not only include random errors, but failures of entire pages. These might include word line failures of various sorts, block failures, or even die-level faults.

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[ECC/DSP White Paper](#) at 11.

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Let's assume a standard RAID stripe of length 32. This means that 31 sectors are protected by an additional parity sector. The over-provisioning used by this RAID scheme is around 3%. Next, let's assume an LDPC-based ECC solution that has approximately 10% over-provisioning.

If the LDPC and RAID layers were to be combined, one could observe that the result is a code with extra 3% overprovisioning and a code word size that is x32 larger than the original. A Tanner graph representing a unified LDPC-RAID code is shown in Figure 13 below. It shows a Tanner graph of a combined LDPC-RAID scheme. The smaller graphs  $G_0, G_1, \dots, G_{30}$  represent the information sectors and  $G_{31}$  is the parity sector.

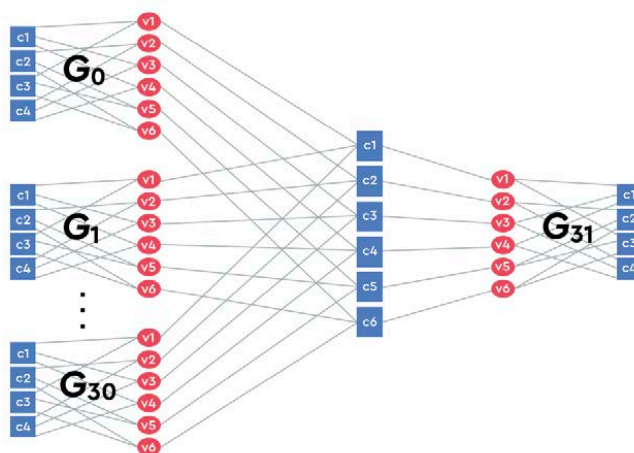


Figure 13: Tanner graph of a combined LDPC-RAID scheme

[ECC/DSP White Paper](#) at 12.

119. As Western Digital (WD) describes in a patent issued from the patent application cited in the ECC/DSP white paper:

Error correction coding (ECC) is often used to correct errors that occur in data read from a memory device. Prior to storage, data may be encoded by an ECC encoder to generate redundant information (e.g., “parity bits”) that may be stored with the data as an ECC codeword. As more parity bits are used, an error correction capacity of the ECC

1 increases and a number of bits required to store the encoded  
2 data also increases. Using a sufficient number of parity bits  
3 to provide “worst-case” error correction capability for all  
4 data stored in a memory device reduces the storage density  
of the memory device in order to protect against an amount  
of data corruption that is statistically unlikely to occur  
before the memory device reaches the end of its useful life.

5 SSD devices may also incorporate a redundant array of  
6 independent dies (RAID)- type storage scheme that may  
7 use parity bits to enable data recovery in case of memory  
8 defects and device failures, which cannot be recovered by  
9 the ECC which is aimed at handling random errors (e.g.,  
10 due to program disturb, read disturb, charge loss due to data  
retention, etc.). ECC may not be able to recover the data in  
case of memory defects or complete failure, which may  
result in very high error rates that exceed the ECC  
capability. Hence, additional RAID-type protection may be  
required for protecting against such memory defects.

11 U.S. Patent No. 9,940,194 of Achtenberg et al. at 1:32-55, *ECC Decoding Using*  
12 *RAID-Type Parity* available at [https://patentimag-](https://patentimages.storage.googleapis.com/bf/90/8b/dec1bb4115b581/US9940194.pdf)  
13 [es.storage.googleapis.com/bf/90/8b/dec1bb4115b581/US9940194.pdf](https://patentimages.storage.googleapis.com/bf/90/8b/dec1bb4115b581/US9940194.pdf) [hereinafter  
“Achtenberg”].

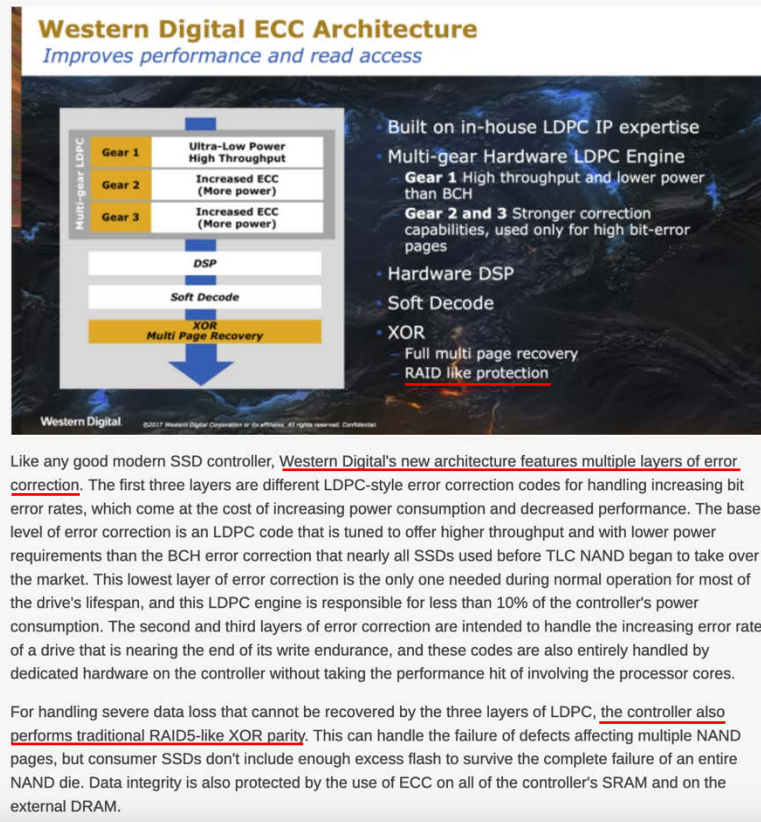
14 The two protection levels, ECC for random errors and  
15 RAID for memory defects and failures, may require  
16 memory overprovisioning for storing the ECC and RAID  
parity.

17 [Achtenberg](#) at 2:8-10.

18 In a particular implementation, the stripe correction  
19 scheme corresponds to a redundant array of independent  
20 disks (RAID)-type exclusive-OR (XOR) scheme, and the  
first correction scheme corresponds to a low density parity  
check (LDPC) scheme.

21 [Achtenberg](#) at 14:47-51.

22 See also [WD Black 3D Review](#).



### WD Black 3D Review.

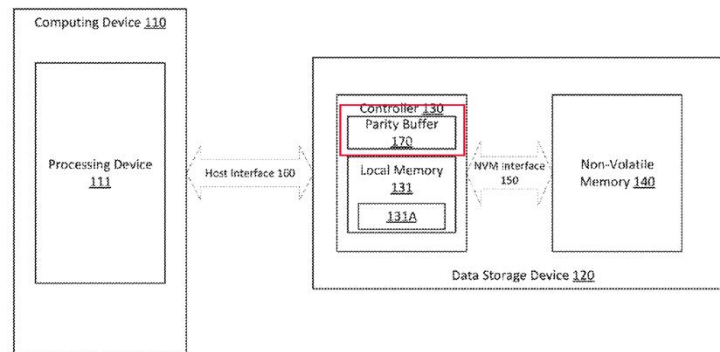
120. Furthermore, other Defendants' patent filings indicate that its RAID parity calculations are performed by a parity calculator that performs a partial parity calculation on blocks received for writing to a stripe. The following image is from U.S. Patent No. 11,106,534:

(57)

#### **ABSTRACT**

An apparatus is disclosed having a parity buffer having a plurality of parity pages and one or more dies, each die having a plurality of layers in which data may be written. The apparatus also includes a storage controller configured to write a stripe of data across two or more layers of the one or more dies, the stripe having one or more data values and a parity value. When a first data value of the stripe is written, it is stored as a current value in a parity page of the parity buffer, the parity page corresponding to the stripe. For each subsequent data value that is written, an XOR operation is performed with the subsequent data value and the current value of the corresponding parity page and the result of the XOR operation is stored as the current value of the corresponding parity page.

U.S. Patent No. 11,106,534, Sun et al., *3-Dimensional Nand Flash Layer Variation Aware SSD RAID*,  
<https://patentimages.storage.googleapis.com/0a/c7/53/8923ad3f4269e8/US11106534.pdf> [hereinafter “Sun”].



Sun at Fig. 1, annotation added.

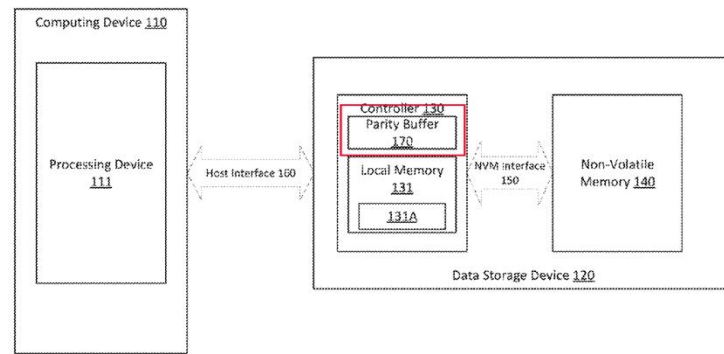
121. The Accused Products include a context memory including a page frame. For example, Defendants’ patent filings, such as Sun, describes a memory system for storing its partial parity RAID data calculation and associated metadata. This system includes features for indicating updated blocks within a data stripe and for converting logical pages to their physical counterparts.

(57)

#### ABSTRACT

An apparatus is disclosed having a parity buffer having a plurality of parity pages and one or more dies, each die having a plurality of layers in which data may be written. The apparatus also includes a storage controller configured to write a stripe of data across two or more layers of the one or more dies, the stripe having one or more data values and a parity value. When a first data value of the stripe is written, it is stored as a current value in a parity page of the parity buffer, the parity page corresponding to the stripe. For each subsequent data value that is written, an XOR operation is performed with the subsequent data value and the current value of the corresponding parity page and the result of the XOR operation is stored as the current value of the corresponding parity page.

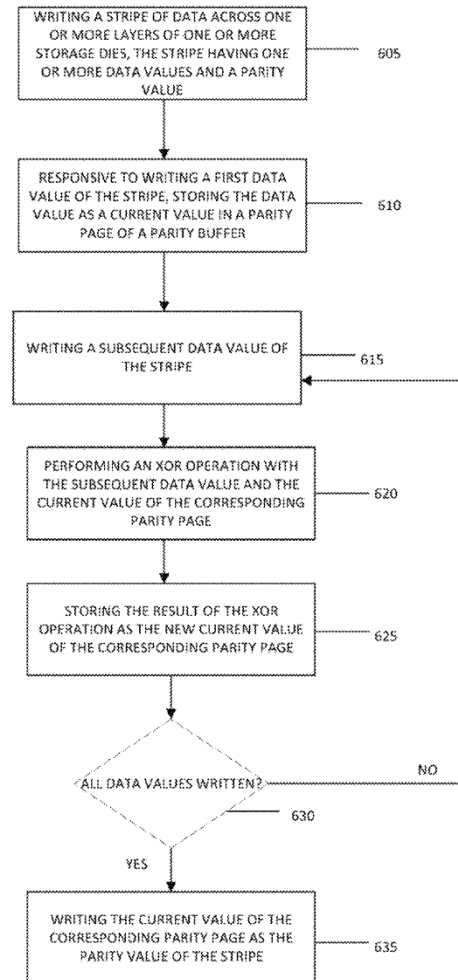
Sun at Abstract.



[Sun](#) at Fig. 1, annotation added.

The logical interface may present to the computing device memory a set of logical addresses (e.g., sequential/contiguous addresses) where data may be stored. Internally, the controller 130 may map logical addresses to various physical memory addresses in the non volatile memory arrays and or other memory module(s).

[Sun](#) at 5:21-26.



[Sun](#) Fig. 6.

At block 630, the controller may determine whether all the data values are written. If there are still data values to be written, the controller returns to block 615. If all data values are written, then at block 635 the controller writes the current value of the corresponding parity page to the parity value of the stripe.

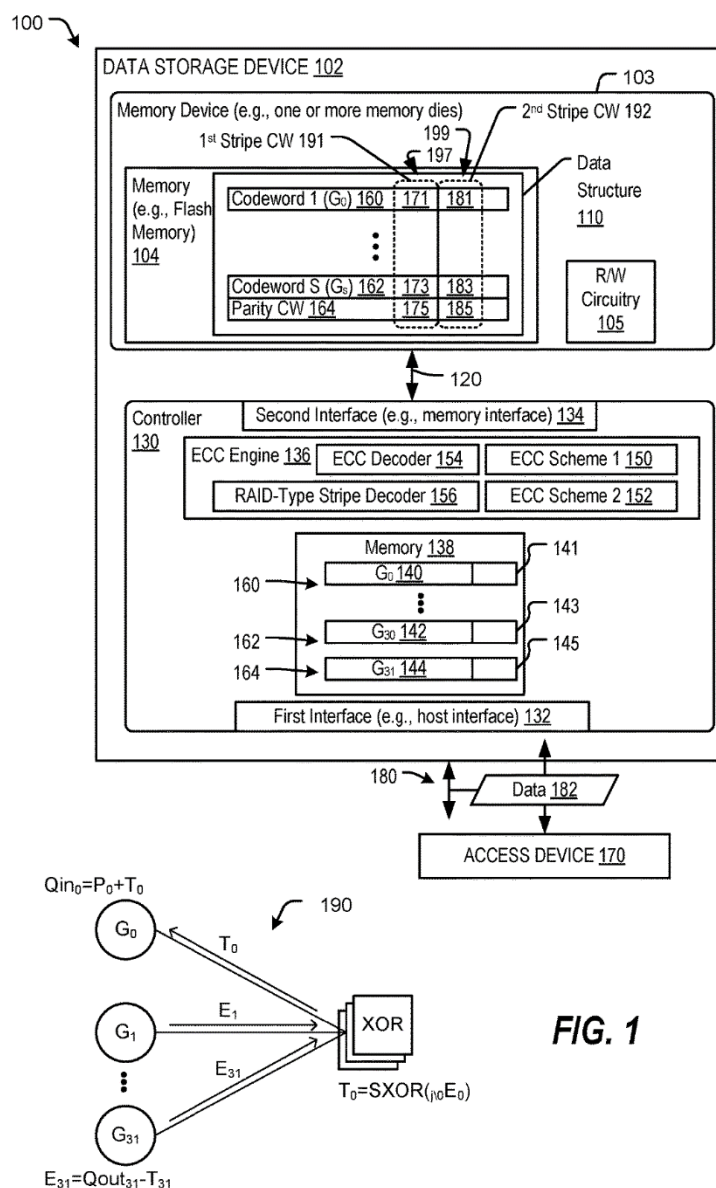
[Sun](#) at 9:52-58.

122. The Accused Products include a parity calculator configured to receive the plurality of data blocks as a sequence of data blocks. For example, U.S. Patent No. 9,940,194, assigned to WD and cited in WD's White Paper, The Application of ECC/DSP to Flash Memory, describes writing a sequence of data blocks for RAID

parity calculation, as shown in the quote and image below:

The controller 130 may be configured to transfer the codewords 160-164 from the Memory 138 for storage into the memory 104 of the memory device 103 to form the data structure 110 in the memory 104. For example, the controller 130 may be configured to sequentially write the codewords 160-164 to consecutively-addressed pages of the memory 104 so that the data structure 110 is aligned in a row-and-column format as depicted in FIG. 1, with the codewords 160-164 forming rows and the stripes 197-199 forming columns in the memory 104.

[Achtenberg](#) at 8:31-40.



[Achtenberg](#) at Fig. 1.

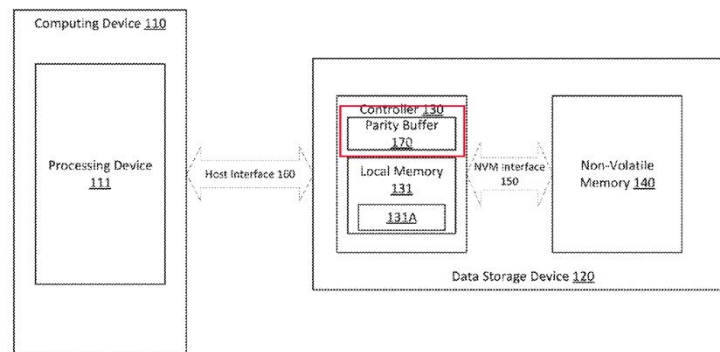
123. Furthermore, Sun describes a buffer for storing parity information, e.g., parity cache or “partial parity Cache (PPC)”, which stores a parity block for a stripe that is updated for each data block written for the stripe.

(57)

#### ABSTRACT

An apparatus is disclosed having a parity buffer having a plurality of parity pages and one or more dies, each die having a plurality of layers in which data may be written. The apparatus also includes a storage controller configured to write a stripe of data across two or more layers of the one or more dies, the stripe having one or more data values and a parity value. When a first data value of the stripe is written, it is stored as a current value in a parity page of the parity buffer, the parity page corresponding to the stripe. For each subsequent data value that is written, an XOR operation is performed with the subsequent data value and the current value of the corresponding parity page and the result of the XOR operation is stored as the current value of the corresponding parity page.

[Sun](#) at Abstract.



[Sun](#) at Fig. 1, annotation added; *see also* Fig. 6.

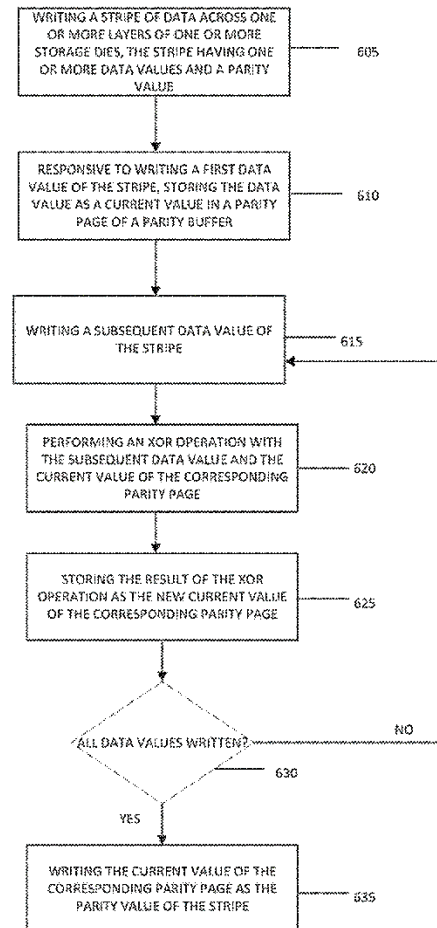
124. The Accused Products generate a parity block storing the first data block of the sequence of data blocks into the page frame and update the parity buffer with the first block written to the stripe. For example, in Sun, WD describes generating and updating the parity block.

(57)

**ABSTRACT**

An apparatus is disclosed having a parity buffer having a plurality of parity pages and one or more dies, each die having a plurality of layers in which data may be written. The apparatus also includes a storage controller configured to write a stripe of data across two or more layers of the one or more dies, the stripe having one or more data values and a parity value. When a first data value of the stripe is written, it is stored as a current value in a parity page of the parity buffer, the parity page corresponding to the stripe. For each subsequent data value that is written, an XOR operation is performed with the subsequent data value and the current value of the corresponding parity page and the result of the XOR operation is stored as the current value of the corresponding parity page.

[Sun](#) at Abstract.

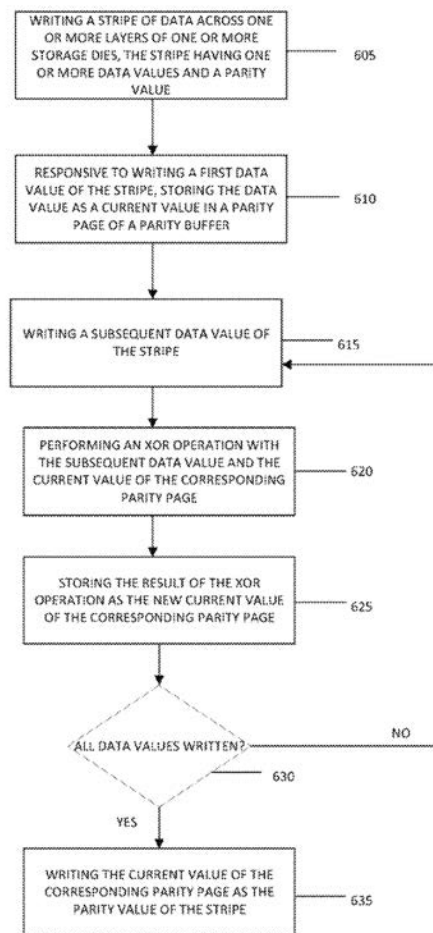


[Sun](#) at Fig. 6.

At block 610, responsive to writing a first data value of the stripe, the controller may store the first data value as a current value in a parity page of a parity buffer. The parity page may correspond to the stripe being written. At block 615, the controller may write a subsequent data value. At block 620, the controller may perform an XOR operation with the subsequent data value and the current value of the corresponding parity page. At block 625, the controller may store the result of the XOR operation as the new current value of the corresponding parity page.

[Sun](#) at 9:43-52.

125. In The Accused Products, the command processing unit that receives the parity write command is configured to write the parity block to a nonvolatile memory based on the parity write command. For example, in Sun, WD describes writing the parity to nonvolatile memory.



[Sun](#) at Fig. 6.

At block 630, the controller may determine whether all the data values are written. If there are still data values to be

1 written, the controller returns to block 615. If all data  
2 values are written, then at block 635 the controller writes  
3 the current value of the corresponding parity page to the  
4 parity value of the stripe.

[Sun](#) at 9:52-58.

5 126. For example, Defendants provide SSD products configured with the  
6 hardware and software that satisfy the limitations of at least claim 1. Defendants  
7 further directly infringe the '346 Patent when its SSD products with NVMe are  
8 installed and operated by its employees in a computer system, such as for gaming,  
9 personal computing, or data centers. Direct infringement further occurs when  
10 Defendants' employees use and test the hardware and software.

11 127. On January 23, 2024, Plaintiff sent a notice letter to Western Digital,  
12 notifying them that they were infringing the Asserted Patents. Western Digital's  
13 infringement of the '346 Patent has been willful and intentional under the standard  
14 announced in *Halo Elecs., Inc. v. Pulse Elecs., Inc.*, 579 U.S. 93 (2016). Western  
15 Digital did not reply to that letter.

16 128. Western Digital has willfully infringed the '346 Patent by refusing to  
17 take a license and continuing to make, use, test, sell, license, and/or offer for  
18 sale/license the '346 Patent Accused Products. Instead of taking a license, Western  
19 Digital has opted to make the business decision to "efficiently infringe" the '346  
20 Patent. In doing so, Western Digital willfully infringes the '346 Patent.

21 129. Defendants also have infringed, and continue to infringe the claims of  
22 the '346 Patent by actively inducing others to use the Accused Products. Defendants'  
23 users, customers, agents or other third parties who use the Accused Products in  
24 accordance with Defendants' instructions infringe the claims of the '346 Patent, in  
25 violation of 35 U.S.C. § 271(a). Defendants induce its customers to use its SSD  
26 products for the benefits of higher performance, reduced size and power, and  
27 increased reliability compared to other SSD products. Defendants are thereby liable  
28 for infringement of the '346 Patent under 35 U.S.C. § 271(b).

130. Defendants' users, customers, agents or other third parties who use the Accused Products in accordance with Defendants' instructions infringe the claims of the '346 Patent, in violation of 35 U.S.C. § 271(b). Defendants intentionally instruct its customers to infringe through support information, demonstrations, brochures, videos, and user guides, such as those located at:

<https://www.westerndigital.com/support;>

<https://support.wdc.com/contact.aspx?lang=en;>

<https://www.westerndigital.com/support/category-selection;>

[https://www.youtube.com/channel/UC\\_M0BlntDVSblWg6ggUa7UQ;](https://www.youtube.com/channel/UC_M0BlntDVSblWg6ggUa7UQ;)

<https://www.youtube.com/watch?v=L0zZtwRFj0E;>

<https://www.youtube.com/westerndigital>; and

<https://www.youtube.com/c/westerndigitalcorporation>.

131. Defendants are liable as contributory infringers of the '346 Patent under 35 U.S.C. § 271(c) by having offered to sell, sold and imported and continuing to offer to sell, selling, and importing into the United States its SSD products, to be especially made or adapted for use in an infringement of the '346 Patent. Defendants' SSD products are key components in gaming consoles and gaming PCs, computers, everyday PCs, Network Attached Storage (NAS) devices, servers and data centers. These SSD products are material components for use in practicing the '346 Patent and are specifically made and are not a staple article of commerce suitable for substantial noninfringing use. Defendants supplied these components with knowledge of the '346 Patent and with knowledge that these components constitute material parts of the claimed inventions of the '346 Patent.

132. As a result of Defendants' infringement of the '346 Patent, Plaintiff has suffered monetary damages and is entitled to no less than a reasonable royalty for Defendants' use of the claimed inventions of the '346 Patent, together with interest and costs as determined by the Court. Plaintiff will continue to suffer damages in the future.

133. Defendants are on notice of their infringement by no later than the filing and service of this Complaint. By the time of trial, Defendants will have known and intended (since receiving such notice) that its continued actions would actively induce to the infringement of the '346 Patent.

134. Defendants' acts of direct and indirect infringement have caused and continue to cause damage to Plaintiff. Plaintiff is entitled to damages in accordance with 35 U.S.C. §§ 271 and 281 sustained as a result of Defendants' wrongful acts in an amount to be proven at trial.

#### **PRAYER FOR RELIEF**

WHEREFORE, Plaintiff requests the following relief from this Court:

A. A judgment that each defendant is liable for infringement of one or more claims of the '968 Patent, the '346 Patent, and the '085 Patent;

B. Compensatory damages in an amount according to proof, and in any event no less than a reasonable royalty, including all pre-judgment and post-judgment interest at the maximum rate allowed by law;

C. A judgment granting Plaintiff such further relief as the Court may deem just and proper; and

D. That the Court declare this an exceptional case and award Plaintiff its attorneys' fees, as provided by 35 U.S.C. § 285 and that Plaintiff be awarded enhanced damages up to treble damages for willful infringement as provided by 35 U.S.C. § 284.

#### **DEMAND FOR JURY TRIAL**

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, Plaintiff demands a trial by jury for all issues so triable.

1 Dated: June 21, 2024

By: /s/ Robert F. Kramer

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