UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner

v.

LONGITUDE LICENSING LTD.,
Patent Owner.

IPR2023-01200
U.S. Patent No. 7,697,369

PETITION FOR *INTER PARTES* REVIEW UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104

TABLE OF CONTENTS

PETITIONER'S EXHIBIT LIST

EX1001	U.S. 7,697,369
EX1002	Prosecution History of U.S. 7,697,369
EX1003	Declaration of R. Jacob Baker under 37 C.F.R. § 1.68
EX1004	*Curriculum Vitae* of R. Jacob Baker
EX1005	U.S. Patent Publication No. 2004/0022095 to Lee et al. ("Lee")
EX1006	*High Performance Memories: New Architecture DRAMs and SRAMs Evolution and Function*, Betty Prince (1999) ("Prince")
EX1007	JEDEC Standard: Double Data Rate (DDR) SDRAM Specification, JESD79C (March 2003) ("JEDEC")
EX1008	U.S. Patent No. 6,026,465 to Mills et al. ("Mills")
EX1009	U.S. Patent No. 6,956,409 to Streif et al. ("Streif")
EX1010	U.S. Patent Publication No. 2006/0064561 to Simeral et al. ("Simeral")
EX1011	Order Granting Motion to Stay (Lenovo) (05-16-23)
EX1012	Order Granting Western Digital's Motion to Intervene (Amazon) (05-16-23)
EX1013	Director Vidal Memorandum re: Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, June 22, 2022

I. INTRODUCTION

Pursuant to 35 U.S.C. §§ 311, 314(a), and 37 C.F.R. § 42.100, Western Digital Technologies, Inc. ("Petitioner") respectfully requests that the Board review and cancel as unpatentable under (pre-AIA) 35 U.S.C. §103(a) claims 1, 2, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 25, 26, and 27 (hereinafter, the "Challenged Claims") of U.S. 7,697,369 (the "'369 patent," EX1001).

The '369 patent describes and claims nothing more than well-known concepts related to data transfer techniques in memory systems. The '369 patent generally "relates to a system having a controller and a memory and, more particularly, to a data sending/receiving operation between the controller and the memory." EX1001, 1:6-8. As explained in the background section of the '369 patent, "[i]n a conventional data sending/receiving operation between the controller and the memory, either the controller or the memory who serves as a sender generates a data strobe." EX1001, 1:9-12. In other words, during the write operation—where the controller transmits data to the memory—the controller generates the strobe signal. During the read operation—where the memory transmits data to the controller—the memory generates the strobe signal. This operation is discussed in further detail in the Background section below.

The purported novelty of the '369 patent is that for the read operation, the memory generates its strobe signal *in response* to a strobe signal from the

controller. *See* EX1002, 8, 17-31. The memory then transmits its strobe signal along with the data signal. However, as will be shown below—and confirmed in the Declaration of R. Jacob Baker (EX1003)—it was already well-known to have the memory send a data strobe signal that is generated in response to a strobe signal from the controller, as evidenced by Lee. Indeed, Lee refers to this concept as "conventional." EX1005, Lee, [0025]. Therefore, the references presented in this Petition anticipate and render obvious the Challenged Claims.

II. GROUNDS FOR STANDING

Petitioner certifies that the '369 patent is eligible for IPR and that Petitioner is not barred or estopped from requesting IPR challenging the patent claims. 37 C.F.R. § 42.104(a).

III. NOTE

Petitioner cites to exhibits' original page numbers. Emphasis in quoted material has been added.

IV. BACKGROUND

The '369 patent relates to data transfer techniques that were well-known as of the earliest claimed priority date. This section provides a brief summary of memory systems and the strobe signals they use to transfer data.

A. Memory Systems

Memory systems typically include a memory controller and the memory

itself. "In a conventional mobile processing system, the memory and the memory controller are, typically, interconnected in a point-to-point fashion." EX1005, Lee, [0006]. Memory systems perform both read and write operations. For a write operation, the memory controller receives data from an external source and then transmits that data to the memory for storage. During a read operation, the memory transmits data to the memory controller, which then passes that data to an external device that is requesting that data. EX1003, ¶ 25.

B. Strobe Signals

When transmitting data between the memory controller and the memory, strobe signals are used to inform the receiving system when to sample the incoming data. For example, during a write operation, the memory controller sends the write data signal along with a write data strobe signal. It takes some time for the data and the strobe signal to reach the memory. The memory—which receives both the data signal and the strobe signal at the same time—then uses the strobe signal to know when to sample the data from the data signal. During a read operation, the controller receives both a data signal and a strobe signal from the memory. The controller then uses the strobe signal to accurately sample data from the data signal. EX1003, ¶¶ 26-27.

C. Synchronous and Asynchronous Memory

Strobe signals are used in both synchronous and asynchronous memory

systems. In synchronous memory systems, transfer of data between the controller and memory is synchronized with an external clock signal. *See* EX1005, Lee, [0005]. For example, when the controller writes to memory, it sends a data signal to the memory along with a strobe signal that is synchronized with the external system clock. Similarly, during a read operation, the memory transmits data along with a strobe signal synchronized with the system clock. An example of synchronous memory is Synchronous Dynamic Random-Access Memory (SDRAM). *See* EX1006, Prince, 23; EX1003, ¶¶ 28-29.

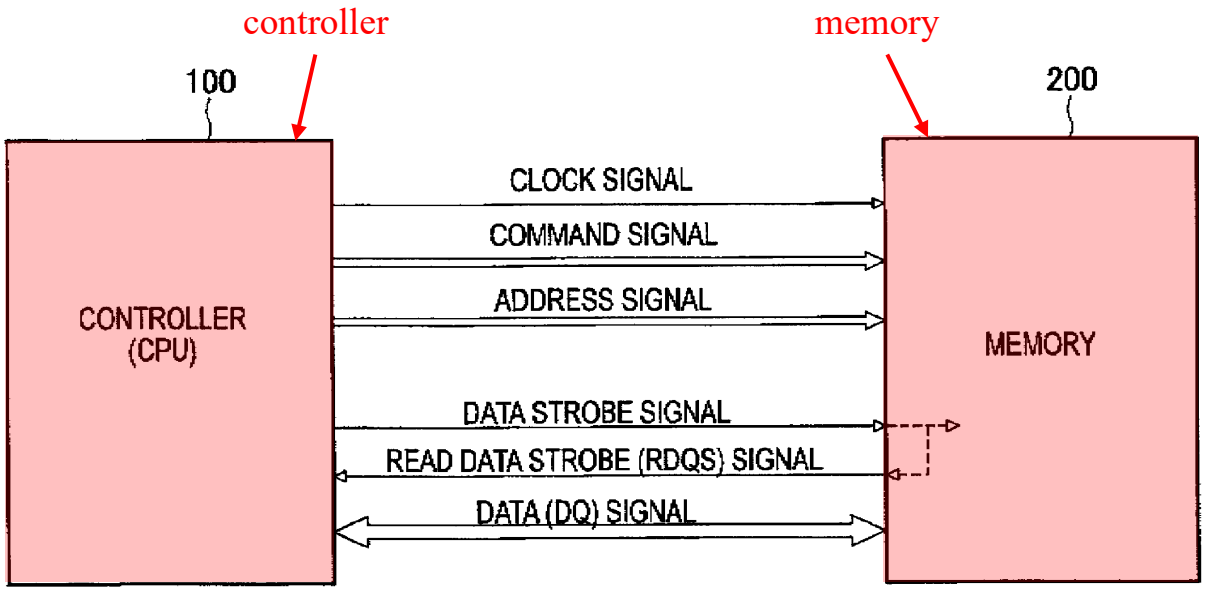
Asynchronous memory, however, is not synchronized with the system clock. *See* EX1005, Lee, [0028]. For example, when the controller writes to memory it sends a data signal to the memory along with a strobe signal. That strobe signal does not have to be synchronized with the system clock. Similarly, in a read operation, the memory transmits data along with a strobe signal that is not necessarily synchronized with the system clock. An example of asynchronous memory is Static Random-Access Memory (SRAM). *See* EX1006, Prince, 21; EX1003, ¶ 30.

Thus, both asynchronous and synchronous memory make use of strobe signals in a similar manner but differ by whether the strobe signals are synchronized with the system clock. In other words, both types of memory use strobe signals that are synchronized with the data signals. But synchronization of

the strobe signal with the data signal is distinct from the concept of "synchronous memory," which refers to synchronizing the strobe signal with the system clock. EX1003, ¶ 31.

V. SUMMARY OF THE '369 PATENT

The '369 patent generally "relates to a system having a controller and a memory and, more particularly, to a data sending/receiving operation between the controller and the memory." EX1001, 1:6-8. Fig. 1 of the '369 patent, shown below, illustrates "a controller 100 and a memory 200." '369 patent, 3:6-8.

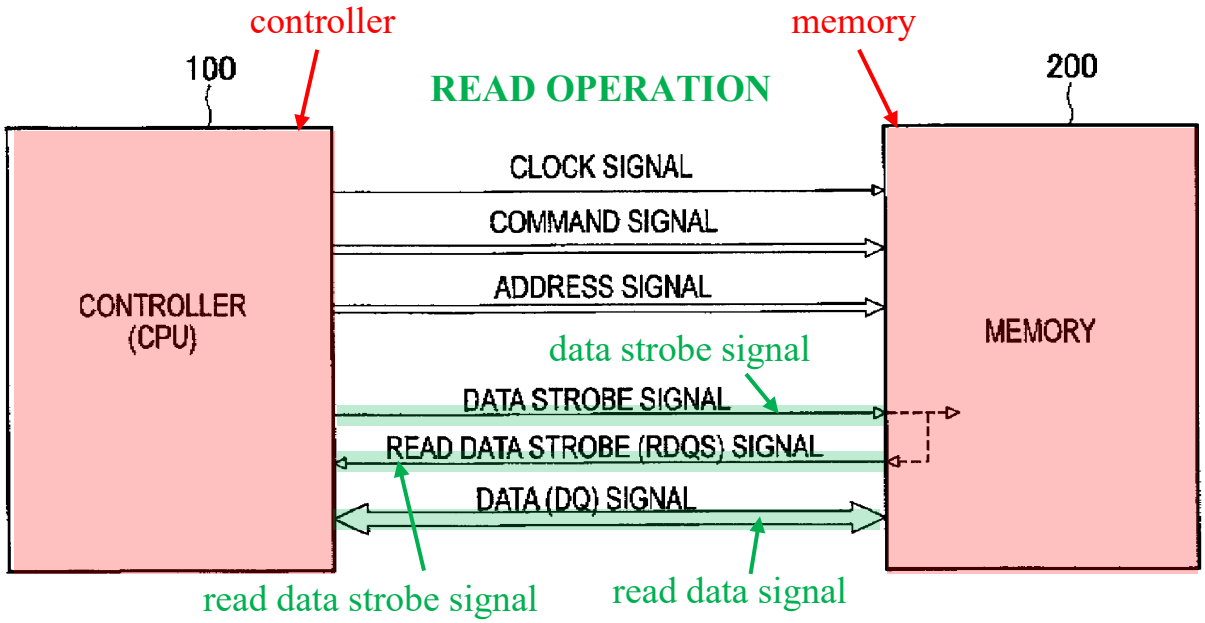


EX1001, Fig. 1 (annotated); EX1003, ¶ 32.

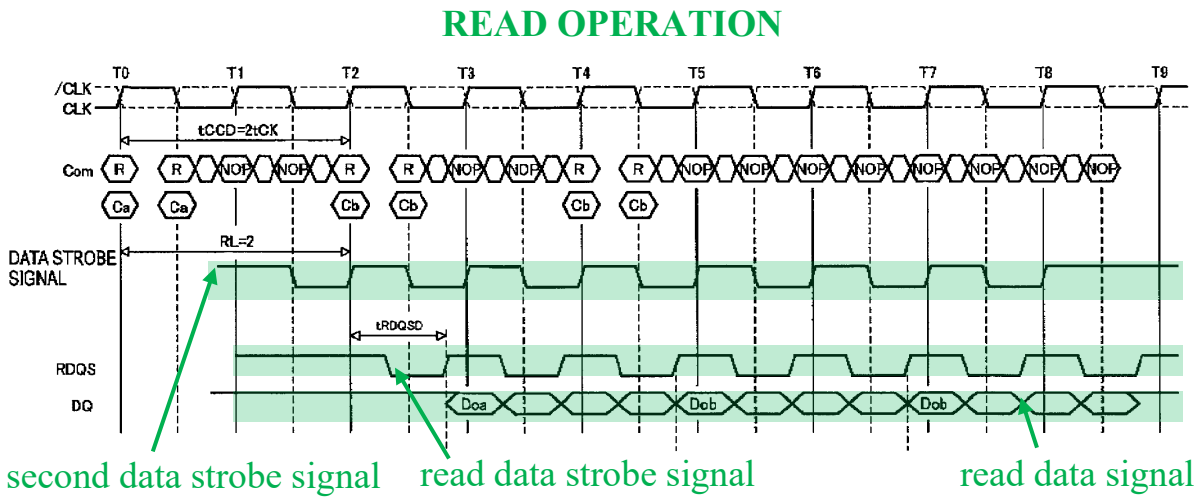
The background section of the '369 patent explains that "[i]n a conventional data sending/receiving operation between the controller and the memory, either the controller or the memory who serves as a sender generates a data strobe." EX1001,

1:9-12. For example, during the write operation—where the controller transmits data to the memory—the controller generates the strobe signal. During the read operation—where the memory transmits data to the controller—the memory generates the strobe signal. EX1003, ¶ 33.

The purported novelty of the ’369 patent is that during the read operation, the memory generates the read data strobe signal in response to a strobe signal from the controller: “The memory 200 is adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and to send out the read data signal synchronized with the read data strobe signal.” EX1001, 3:22-25. By using this technique, “it is not necessary for the memory 200 to produce the data strobe signal from the clock signal nor to make the read data strobe signal synchronize with the clock signal.” EX1001, 3:41-44. Claim 1, for example, recites this concept as follows: “the memory being adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal.” The read operation is illustrated in Figs. 1 and 8 as shown below. EX1003, ¶ 34.



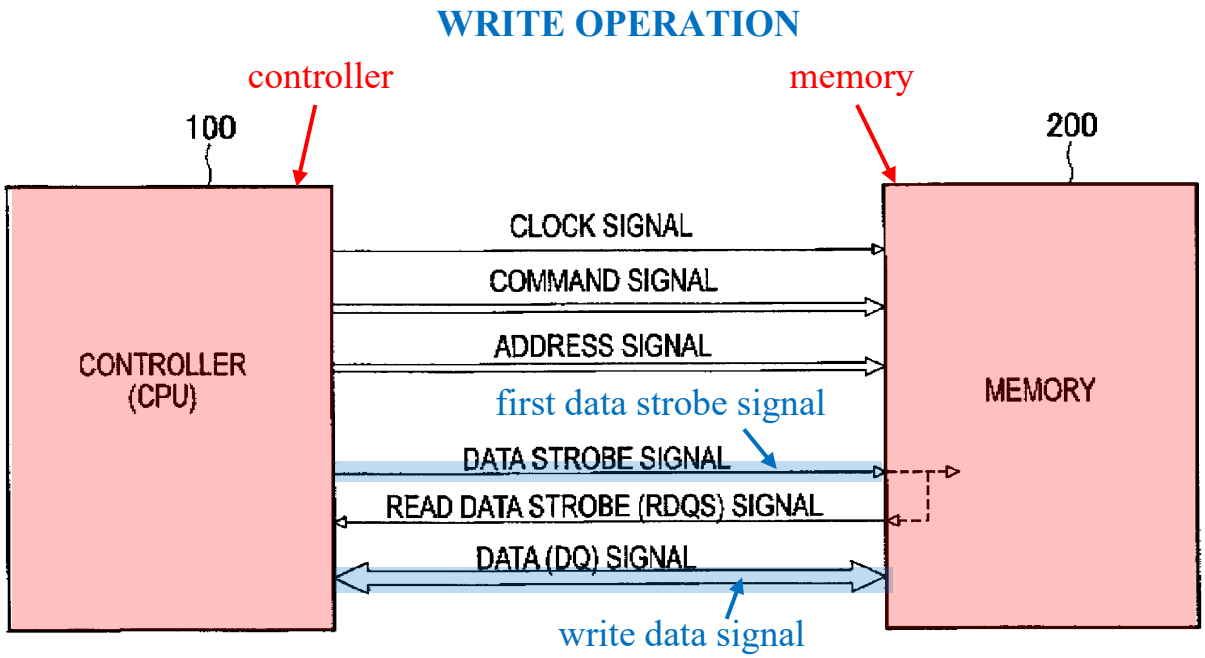
EX1001, Fig. 1 (annotated); EX1003, ¶ 34.



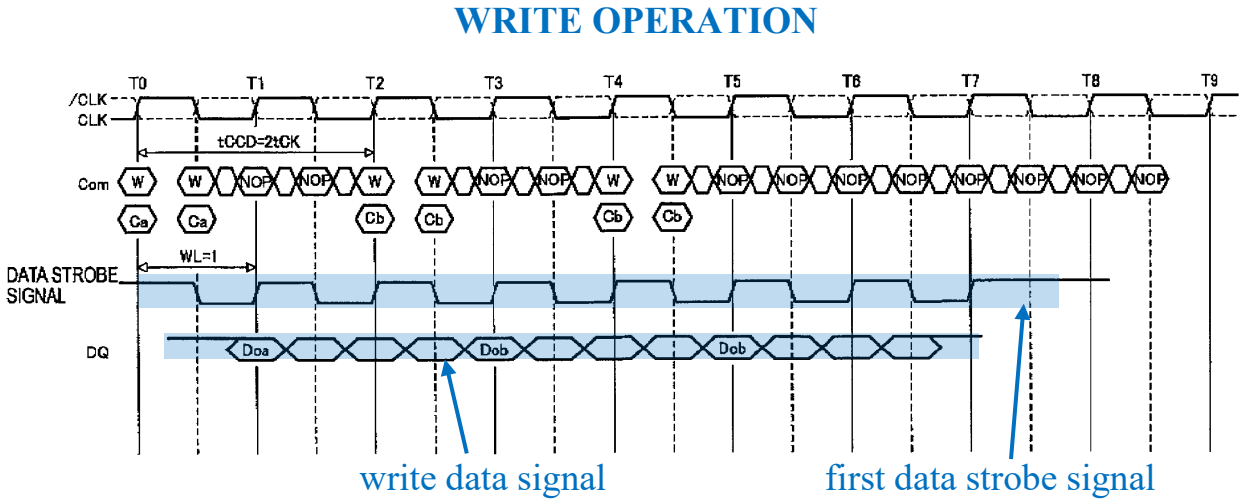
EX1001, Fig. 8 (annotated); EX1003, ¶ 34.

The ’369 patent also describes and claims a conventional write operation. During the write operation, “[t]he controller 100 is adapted to send out a first data strobe signal and a write data signal.” EX1001, 3:12-14. The write operation is

illustrated in Figs. 1 and 6 as shown below. EX1003, ¶ 35.



EX1001, Fig. 1 (annotated); EX1003, ¶ 35.



EX1001, Fig. 6 (annotated); EX1003, ¶ 35.

As will be explained below, the '369 patent describes and claims nothing more than well-known techniques for using data strobe signals during read and

write operations. In particular, the concept of having the memory send a data strobe signal in response to a strobe signal from the controller was well-known at the time the '369 patent was filed. EX1003, ¶ 36.

VI. PROSECUTION HISTORY OF THE '369 PATENT

The '369 patent was filed June 7, 2007, and claims priority to Japanese patent application No. 2006-160204 filed June 8, 2006.

In the first Office Action, the claims were rejected as being anticipated by U.S. Patent No. 7,237,073 to Jang ("Jang") EX1002, 71. Applicant then amended the claims to recite "the read data strobe signal ~~corresponding~~ being received in response to the second data strobe signal." EX1002, 48-59. The Office maintained the rejection over Jang despite the amendments. EX1002, 37-46. Applicant then amended the claims to recite "the read data strobe signal being received by the controller in response to the second data strobe signal." EX1002, 17-31.

The Office then issued a notice of allowance, which did not identify any specific reason for allowance. EX1002, 10-12. The '369 patent then issued on April 13, 2010. EX1002, 1.

For the reasons explained below, the subject matter of the claims as amended to gain allowance was known before the priority date of the '369 patent. In particular, it was known for memory systems to send a read data strobe signal in response to a strobe signal from the controller.

VII. LEVEL OF ORDINARY SKILL IN THE ART

A Person of Ordinary Skill in The Art ("POSITA") in June of 2006 would have had a working knowledge of the memory system art that is pertinent to the '369 patent, including memory systems and memory controllers. A POSITA would have had a bachelor's degree in electrical engineering, or an equivalent, and approximately two years of professional experience relating to field of memory systems. Lack of professional experience can be remedied by additional education, and vice versa. EX1003, ¶¶ 18-20.

VIII. CLAIM CONSTRUCTION

Claim terms in IPR are construed according to their "ordinary and customary meaning" to those of skill in the art. 37 C.F.R. § 42.100(b). Petitioner submits that, for the purposes of this proceeding and the Grounds presented herein, no claim term requires express construction. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). EX1003, ¶ 37.

IX. RELIEF REQUESTED AND THE REASONS FOR THE REQUESTED RELIEF

Petitioner asks that the Board institute a trial for *inter partes* review and cancel the Challenged Claims in view of the analysis below.

X. IDENTIFICATION OF HOW THE CLAIMS ARE UNPATENTABLE

A. Challenged Claims

Petitioner challenges claims 1, 2, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 25, 26, and 27.

B. Statutory Grounds for Challenges

Grounds	Claims	Basis
#1	1, 6, 10, 14, 15, 16, 17, 18, 19, 25, 26, and 27	Obvious under 35 U.S.C. § 103 (Pre-AIA) over Lee
#2	2, 7, and 11	Obvious under 35 U.S.C. § 103 (Pre-AIA) over Lee and JEDEC

U.S. Patent Publication No. 2004/0022095 to Lee *et al.* was filed March 25, 2003 and published on February 5, 2004. Lee is thus prior art to the '369 patent under Pre-AIA 35 U.S.C. 102(b).

The JEDEC Standard: Double Data Rate (DDR) SDRAM Specification, JESD79C is an industry standards document that is dated March of 2003. The metadata of Exhibit 1007 indicates a creation date of March 31, 2003 and a modified date of April 30, 2003.

Exhibit 1007 was obtained from the Internet Archive at the following URL: "https://web.archive.org/web/20030609052112/http://www.jedec.org/download/search/JESD79C.pdf. The availability of the JEDEC standard from the Internet

Archive shows that the standards document was readily available at the JEDEC website (www.jedec.org). Furthermore, as Dr. Baker explains, POSITAs at the time the '369 patent was filed would have been familiar with various standards for memory systems, including JEDEC and ONFI (Open NAND Flash Interface). EX1003, ¶ 105. POSITAs would have relied on the publicly available standards documents, such as JESD79C for memory system design. EX1003, ¶ 105.

Furthermore, various patents, which predate the filing of the '369 patent, refer to the JESD79C standards document. *See e.g.,* EX1009, Streif, 3:17-21 ("The JEDEC DDR SDRAM technical standard is published in a document entitled "JEDEC Standard—Double Data Rate (DDR) SDRAM Specification—JESD79C (Revision of JESD79B)," published March 2003, which is herein included by reference."); EX1010, Simeral, [0009] ("DDR is defined in the JEDEC specification JESD79C, adopted in September, 2003"). EX1003, ¶ 106. The PTAB has also recognized JEDEC standards as printed publications. *See SanDisk Corp. v. Netlist, Inc.*, IPR2015-01020, Paper 36 (PTAB, 2016).

Accordingly, the JEDEC standard JESD79C (EX1007, JEDEC) was thus a printed publication that was publicly available as of at least June 9, 2003. Therefore, JEDEC is prior art to the '369 patent under Pre-AIA 35 U.S.C. 102(b).

C. Discretionary Denial is Not Warranted

Petitioner respectfully submits that the Board should not exercise its

discretion under 35 U.S.C. §§314(a) or 325(d) to deny this Petition.

1. The Fintiv factors favor institution.

Denial would be improper based on factors in Apple v. Fintiv, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential).

a) Factor 1: Stay in District Court Favors Institution

Six litigations concerning the '369 patent are pending in CDCA, all involving the Patent Owner and WDT's customers. *See* XII.B. WDT's motion to intervene was granted in the Amazon Action. EX1012. All litigations are stayed pending the resolution of the Amazon Action with respect to WDT. EX1011. This weighs strongly in favor of institution. *Snap, Inc. v. SRK Tech. LLC*, IPR2020-00820, Paper 15 at 8-9 (PTAB Oct. 21, 2020) (precedential) (granting stay allays concerns about inefficiency and duplication efforts).

b) Factor 2: Unscheduled Trial Date Favors Institution.

In the Amazon Action with respect to WDT, the litigation is in its early stages. The Court has not set a case schedule; the scheduling conference is set to occur on July 21, 2023. Amazon Action, Dkt. 46. No claim construction briefing has been scheduled or filed. No trial date has been set.

c) Factor 3: Lack of Investment in Parallel Proceedings Favors Institution.

The co-pending litigations are either stayed or in early stages, and the

investment has been minimal. The lack of investment in the parallel proceedings favors institution.

d) Factor 4: No Overlapping Issues with the Parallel Proceedings Favors Institution.

There is no overlap of prior art issues at this time. Additionally, if the Board institutes trial, Petitioner will not assert in the co-pending litigations the combination of references on which trial is instituted for the claims on which trial is instituted, to the extent Petitioner even asserts the same combination in the district court. *See Verizon v. Huawei*, IPR2020-01079, Paper 10 at 38 (finding a similar stipulation "mitigates the concern about overlapping issues" and weighs "against discretionary denial of the Petition").

e) Factor 5: Whether Petitioner is Defendant Is Neutral.

Petitioner is an intervener in the Amazon Action with respect to WDT. This factor is neutral and should not be a basis for denying institution. *See HP Inc. v. Slingshot Printing LLC*, IPR2020-01084, Paper 13 at 9 (having the "same parties as parallel proceeding" makes factor 5 "neutral").

f) Factor 6: Other Circumstances Including Merits Favors Institution.

As detailed below, every element of the Challenged Claims is expressly shown in or obvious in the prior art. In view of the striking similarities between the '369 patent claims and the prior art references, this petition "presents compelling

evidence of unpatentability." Director Vidal's Guidance Memorandum, EX1013, 2. Even if the Board determines that the other Fintiv factors favor a discretionary denial—which they do not—the Director's Fintiv Guidance strongly supports institution of this challenge. *See CommScope Technologies LLC v. Dali Wireless, Inc.*, IPR2022-01242, Paper 23 at 4-5 (PTAB Feb. 27, 2023) (precedential).

In short, investments in these parallel proceedings are minimal, and Fintiv factors are either neutral or weigh against discretionary denial. Thus, the Fintiv factors weigh in favor of institution.

2. Advanced Bionics Test Favors Institution.

Denial under 35 U.S.C. § 325(d) is not warranted because the challenges presented in this petition are neither cumulative nor redundant to the prosecution of the '369 patent. The Examiner did not consider any of the references relied upon in this petition. Moreover, the challenges in this petition are non-cumulative because they rely upon prior art that teaches the specific limitations the Examiner found lacking in the prior art of record during prosecution. *Compare* EX1002, 8, 17-31 (allowance after amending the claim to recite "the read data strobe signal being received by the controller in response to the second data strobe signal") with EX1005, Lee, [0025] ("The memory 120 generates the third strobe signal SDfM in response to the received second strobe signal SDtM").

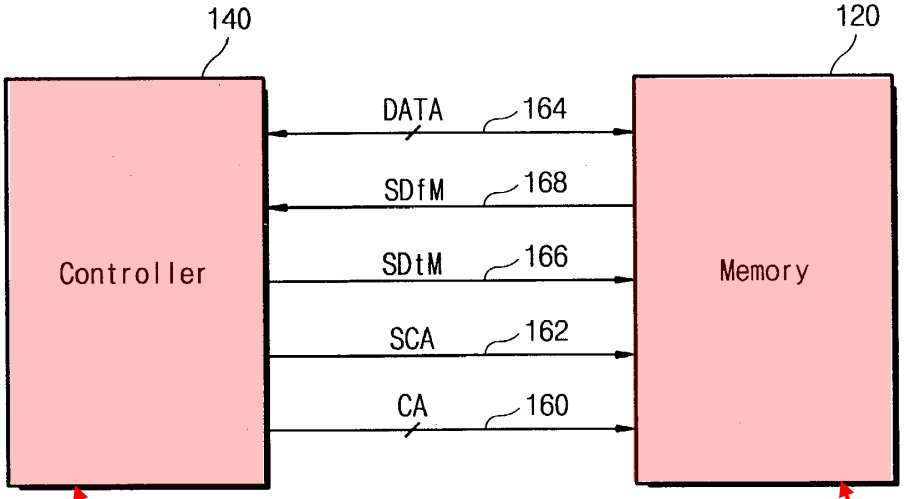
D. Ground 1: Claims 1, 6, 10, 14, 15, 16, 17, 18, 19, 25, 26, and 27

are Obvious in View of Lee

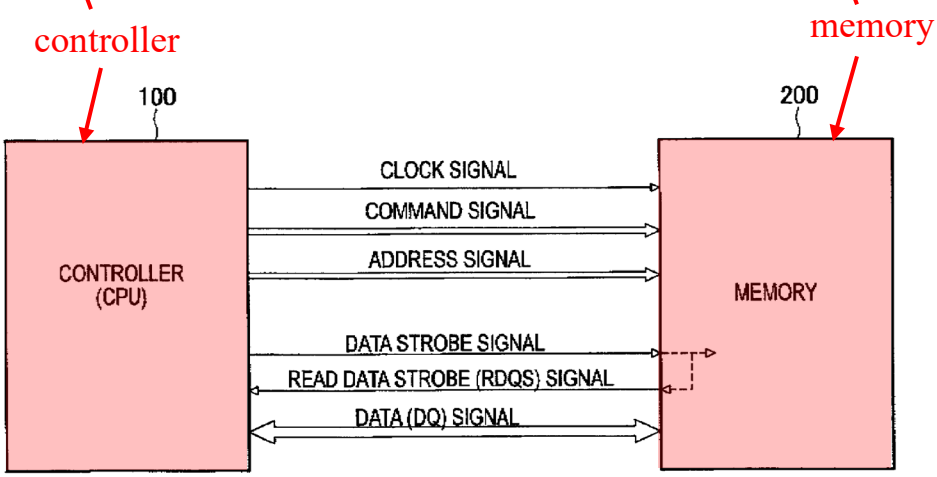
Each of the challenged claims are rendered obvious by Lee. EX1003, ¶¶ 40-44.

1. Summary of Lee

Like the ’369 patent, Lee relates to “a system that performs data transmission between a memory and a memory controller.” EX1005, Lee, [0002]. The similarities between Lee and the ’369 patent can be seen by the figure below, which compares Fig. 1 of Lee and Fig. 1 of the ’369 patent. Both figures illustrate data and strobe signals sent between a memory and a controller. EX1003, ¶ 41.

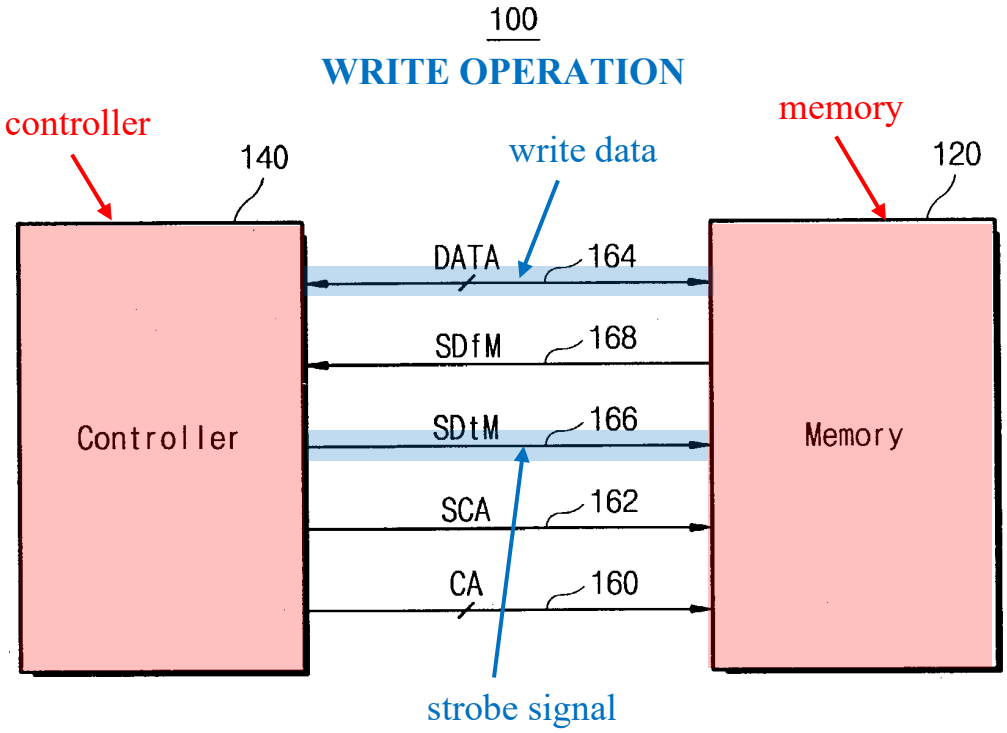


EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 41.

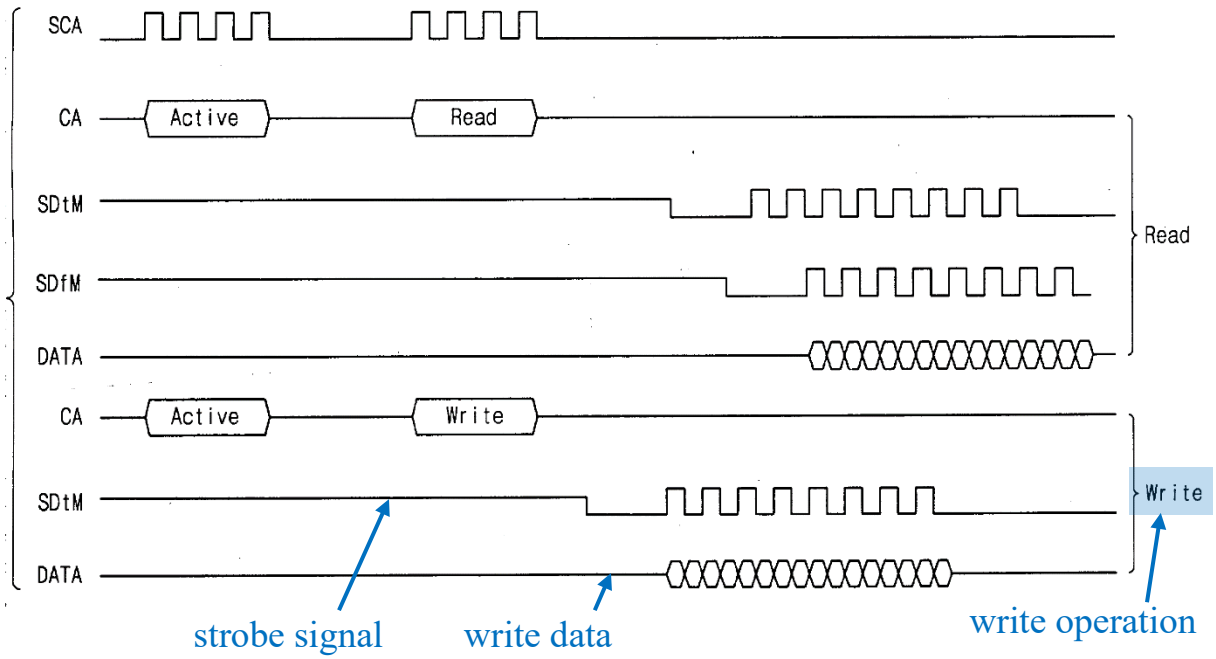


EX1001, Fig. 1 (annotated); EX1003, ¶ 41.

Lee also describes read and write operations that make use of strobe signals in the same way as the '369 patent. *See* EX1005, Lee, [0020]-[0021]. For the write operation, "the write data DATA is sent to the memory 120 from the memory controller 140 together with the second strobe signal SDtM based on the source synchronous interface." EX1005, Lee, [0020]. The write operation is shown in the annotated Figs. 1 and 2 below. EX1003, ¶ 42.



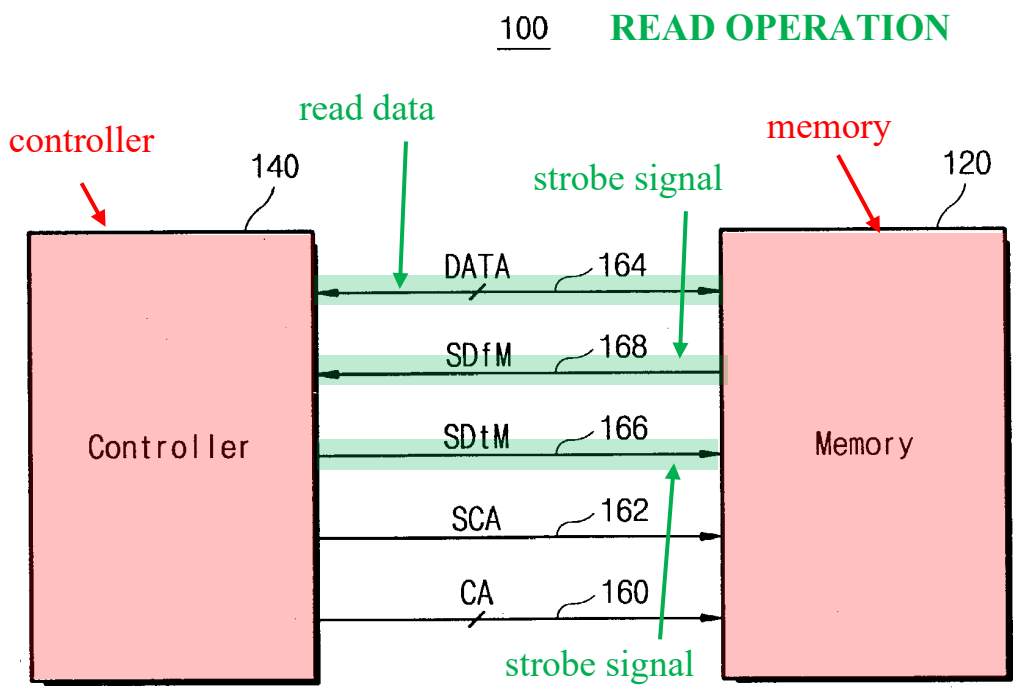
EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 42.



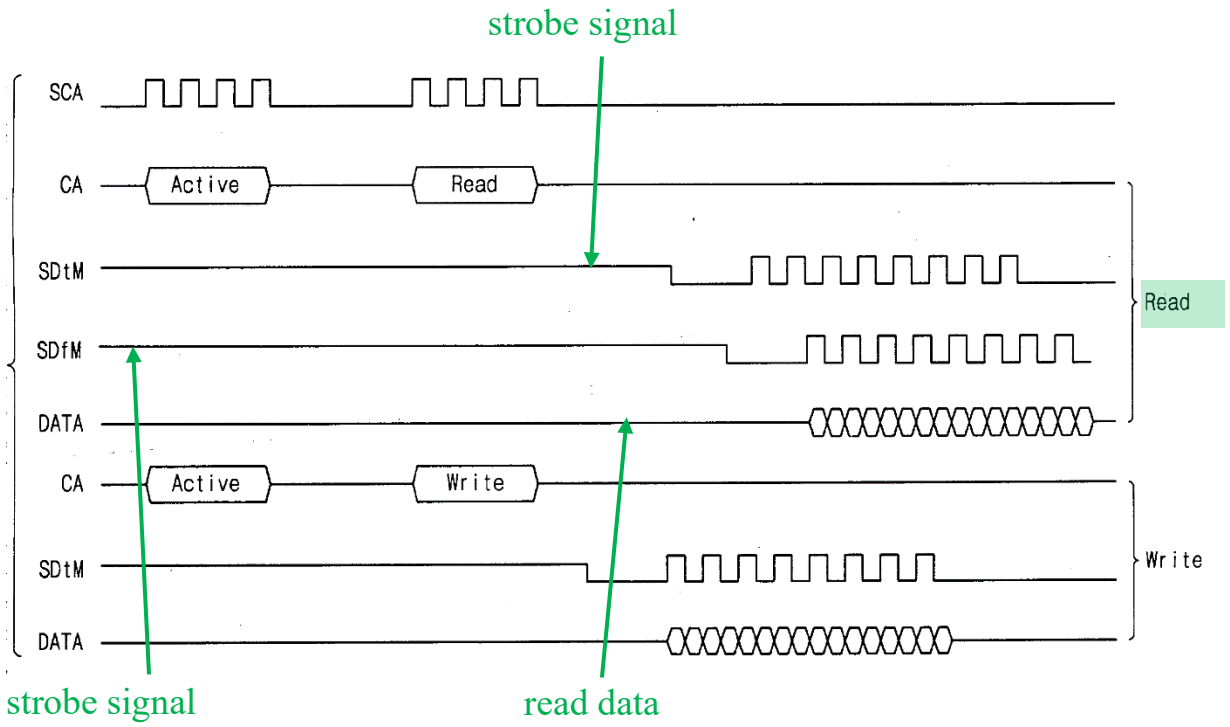
EX1005, Lee, Fig. 2 (annotated); EX1003, ¶ 42.

Lee's read operation also uses strobe signals in the same way as the '369 patent. For the read operation, "[t]he read data that is read from the memory 120 is sent to the memory controller 140 together with the third strobe signal SDfM." EX1005, Lee, [0021]. The third strobe signal is generated in response to a strobe signal from the controller: "the memory controller 140 transfers to the memory 120 the second strobe signal SDtM as a transmission synchronous or reference signal at a time when it wants to receive data read out from the memory 120. The memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM." EX1005, Lee, [0021]. The read operation is shown in the annotated Figs. 1 and 2 below.[1] EX1003, ¶ 43.

[1] While Lee illustrates the timing for both read and write operations in the same figure, a POSITA would have recognized that read and write operations generally do not occur simultaneously. EX1003, ¶ 43.



EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 43.



EX1005, Lee, Fig. 2 (annotated); EX1003, ¶ 43.

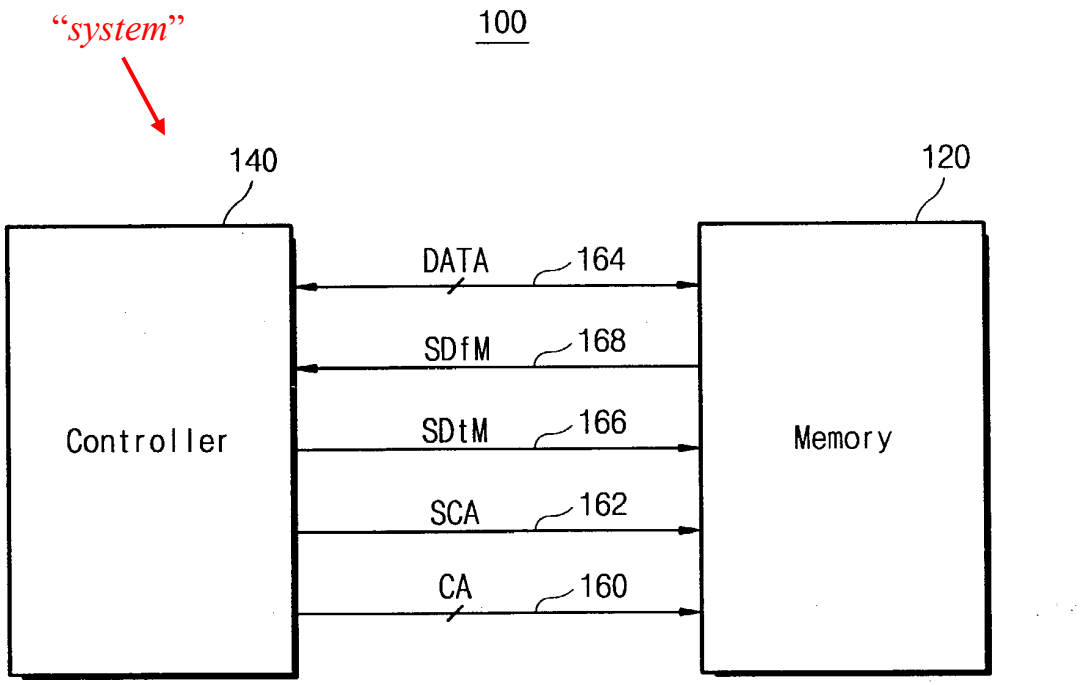
Accordingly, Lee describes the same read and write operations involving a controller and memory that are recited in the challenged claims of the '369 patent. Importantly, Lee's read operation corresponds to the purported novelty of the '369 patent: a memory that transmits a read data strobe signal responsive to a strobe signal from the controller. The analysis below explains how each claim element of the challenged claims is rendered obvious by Lee. EX1003, ¶ 44.

2. Claim 1

[1.0] ***A system comprising:***

Lee describes a system for data transmission between controller and a

memory: "The present invention is related to electronic devices, and, in particular, to **a system** that performs data transmission between a memory and a memory controller." EX1005, Lee, [0002]. Lee further describes "a memory system 100 according to particular embodiments the present invention includes a memory 120 and a memory controller 140." EX1005, Lee, [0017].

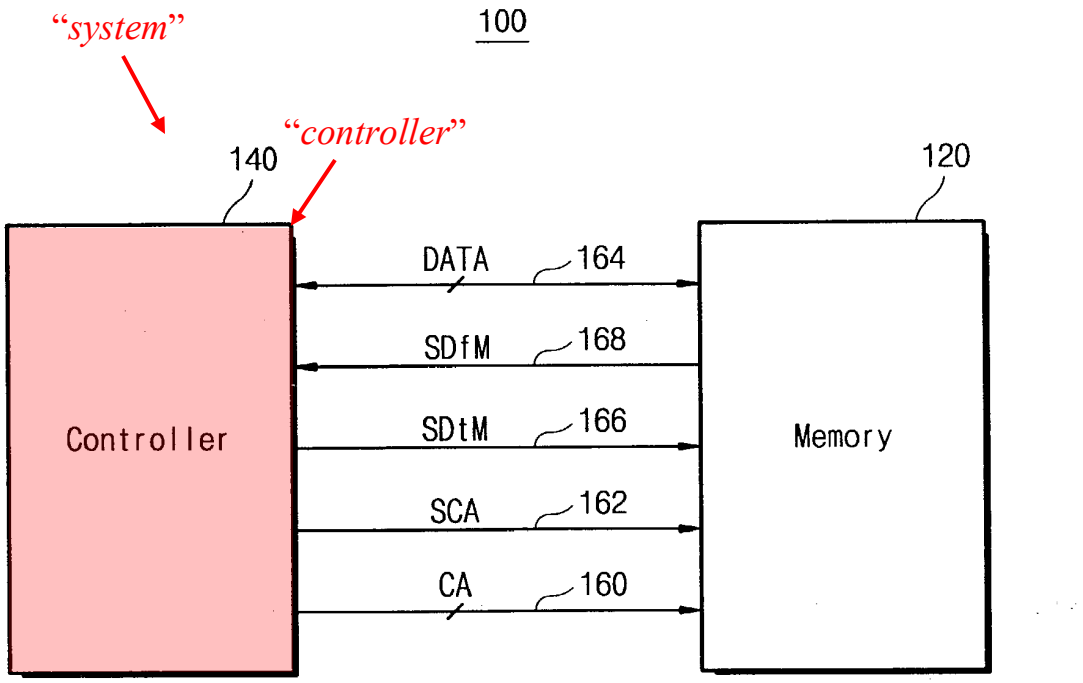


EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 45.

Thus, because Lee describes a memory system that performs data transmission between a memory and a memory controller, Lee renders obvious a "*system*" as claimed. EX1003, ¶¶ 45-46.

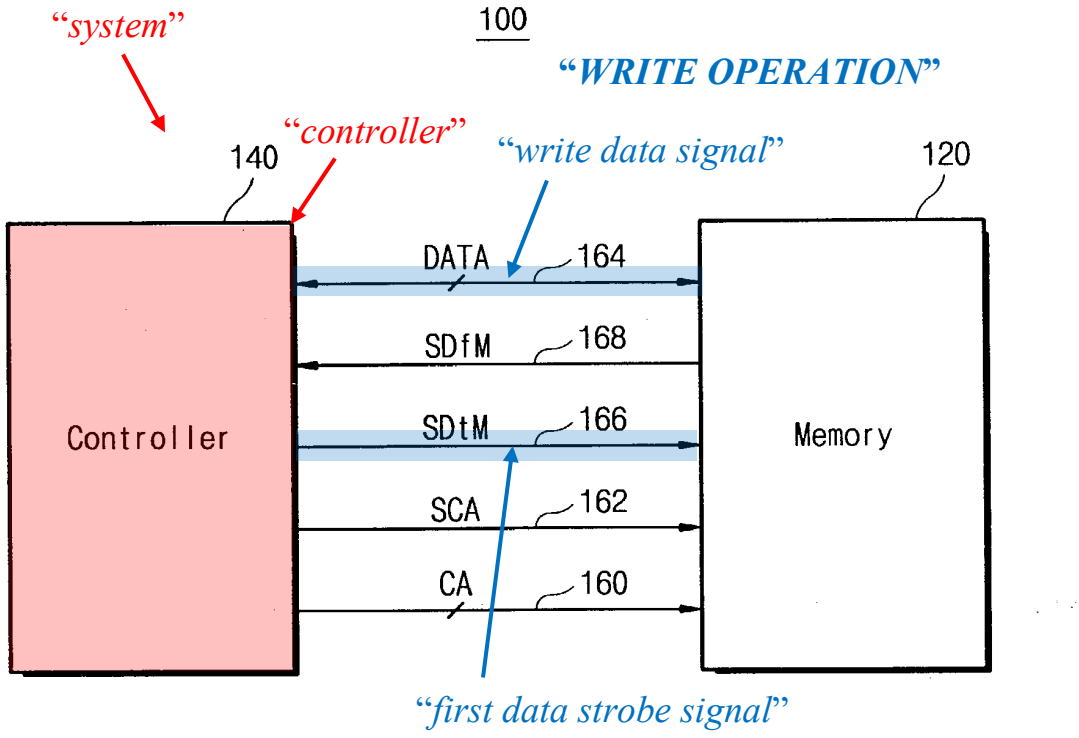
[1.1] ***a controller adapted to send out a first data strobe signal and a write data signal in a write operation,***

First, Lee's system includes a controller 120 ("*controller*"): "[A] memory system 100 according to particular embodiments the present invention includes a memory 120 and a **memory controller 140**." EX1005, Lee, [0017].



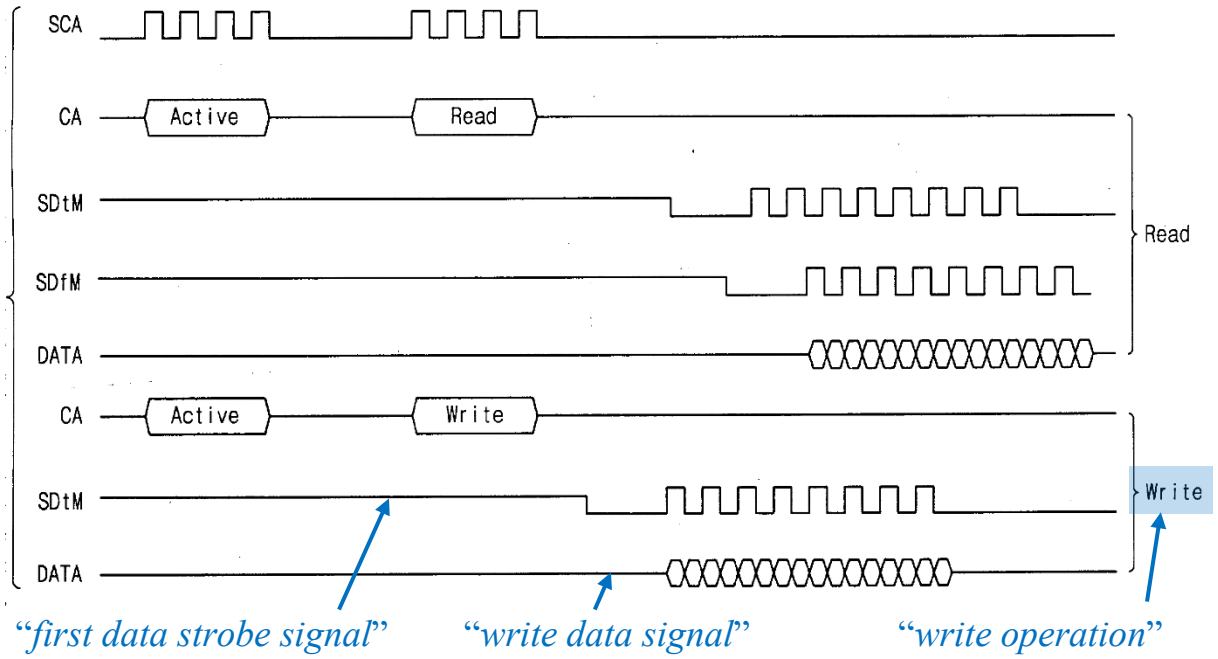
EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 47.

Second, Lee describes a write operation in which the controller transmits strobe signal SDtM ("*first data strobe signal*") over line 166 and data ("*write data signal*") over line 164. Lee explains that during a write operation, "the memory controller 140 transfers data DATA to the memory 120 via a data bus 164, and transfers, as a transmission synchronous signal, the second strobe signal SDtM to the memory 120 via a signal line 166." EX1005, Lee, [0020]. Lee illustrates the data bus 164 and signal line 166 in Fig. 1 below.



EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 48.

Lee further describes the signals of the write operation in Fig. 2 as shown below.



EX1005, Lee, Fig. 2 (annotated); EX1003, ¶ 49.

During the write operations, "data to be written is then sent from the memory controller 140 to the memory 120. Data transmission is accomplished by toggling the second strobe signal SDtM." EX1005, Lee, [0027].

Thus, because Lee describes a controller 140 that transmits a strobe signal SDtM and a data signal over lines 166 and 164 respectively, Lee renders obvious "*a controller adapted to send out a first data strobe signal and a write data signal in a write operation*" as claimed. EX1003, ¶¶ 47-50.

[1.2] ***the write data signal being synchronized with the first data strobe signal,***

Lee explains that the data signal is synchronous with the data strobe signal SDtM: "For a write operation ... the memory controller 140 transfers data DATA

to the memory 120 via a data bus 164, and transfers, **as a transmission synchronous signal**, the second strobe signal SDtM to the memory 120 via a signal line 166." EX1005, Lee, [0020]. A POSITA would have further recognized that the very purpose of a strobe signal is to instruct the receiving system when to sample the transmitted data. *See* EX1005, Lee, [0027] ("The memory 120 latches the write data DATA in response to the second strobe signal SDtM"). Consistent with the discussion above at IV.C., Lee's asynchronous memory still uses strobe signals that are synchronized with their corresponding data signals. [2] A POSITA would have thus understood that the strobe signal is synchronized with the data signal.

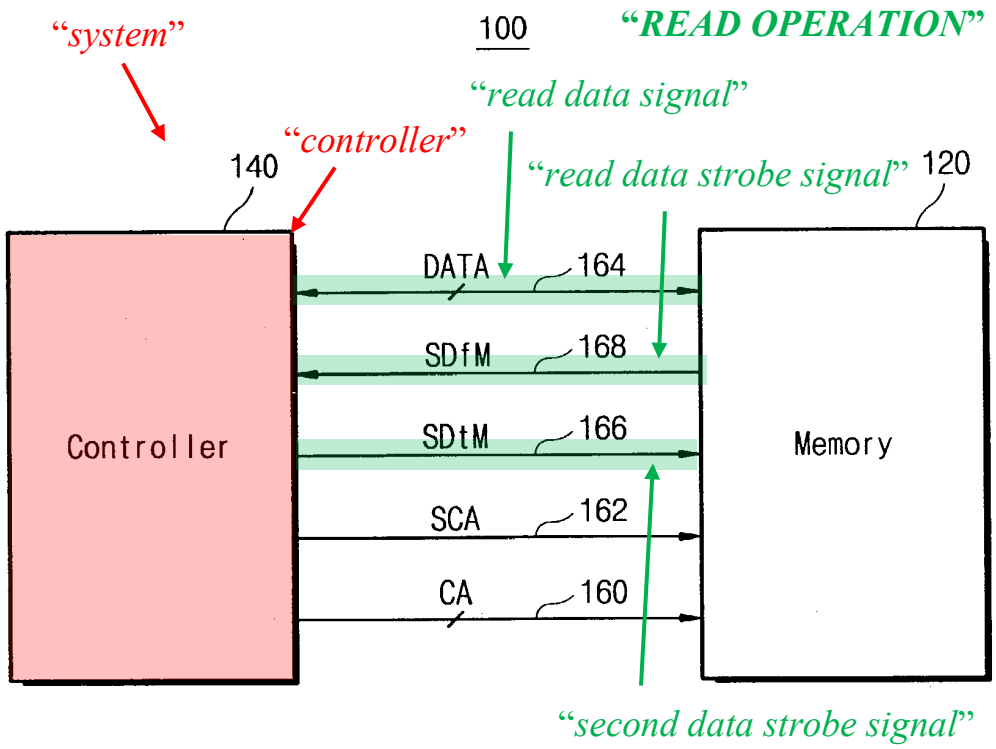
Thus, because Lee describes the strobe signal as a transmission synchronous signal, Lee renders obvious "*the write data signal being synchronized with the first data strobe signal*" as claimed. EX1003, ¶¶ 51-52.

[1.3] ***the controller being adapted, in a read operation, to send out a second data strobe signal and to receive a read data signal in synchronization with a read data strobe signal,***

First, Lee describes a read operation in which the memory transmits strobe signal SDfM ("*read data strobe signal*") over line 168 and data ("*read data*

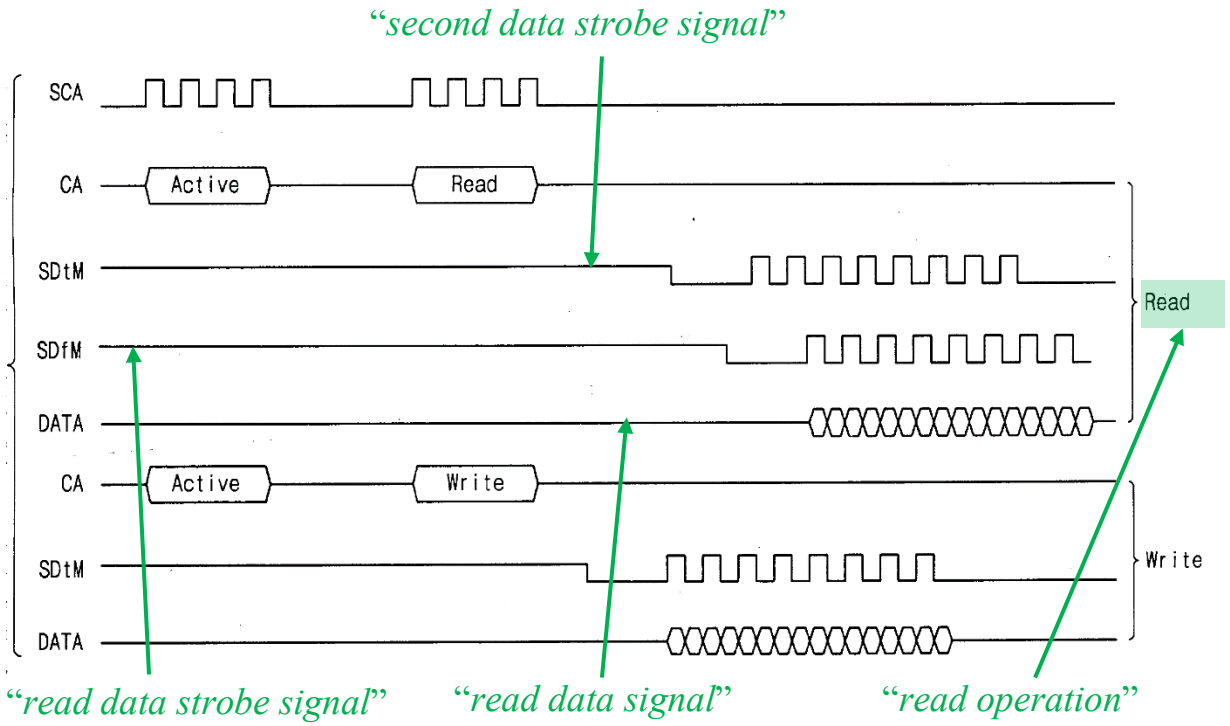
[2] The challenged claims of the '369 patent are agnostic as to whether the memory system is synchronous or asynchronous.

signal") over line 164 in response to the SDtM signal ("*second data strobe signal*"). Lee explains that during a read operation, "the memory controller 140 transfers to the memory 120 the second strobe signal SDtM as a transmission synchronous or reference signal at a time when it wants to receive data read out from the memory 120." EX1005, Lee, [0021]. Lee's controller thus "*send[s] out a second data strobe signal*." The controller then receives data in synchronization with a read strobe signal: "Therefore, during the read operation the memory controller 140 receives the read data DATA from the memory 120 together with the third strobe signal SDfM at a required time." EX1005, Lee, [0021]. Lee's controller thus "*receive[s] a read data signal in synchronization with a read data strobe signal."* The signal lines involved in the read operation are shown below.



EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 53.

Lee further describes the signal timing of the write operation in Fig. 2 as shown below.

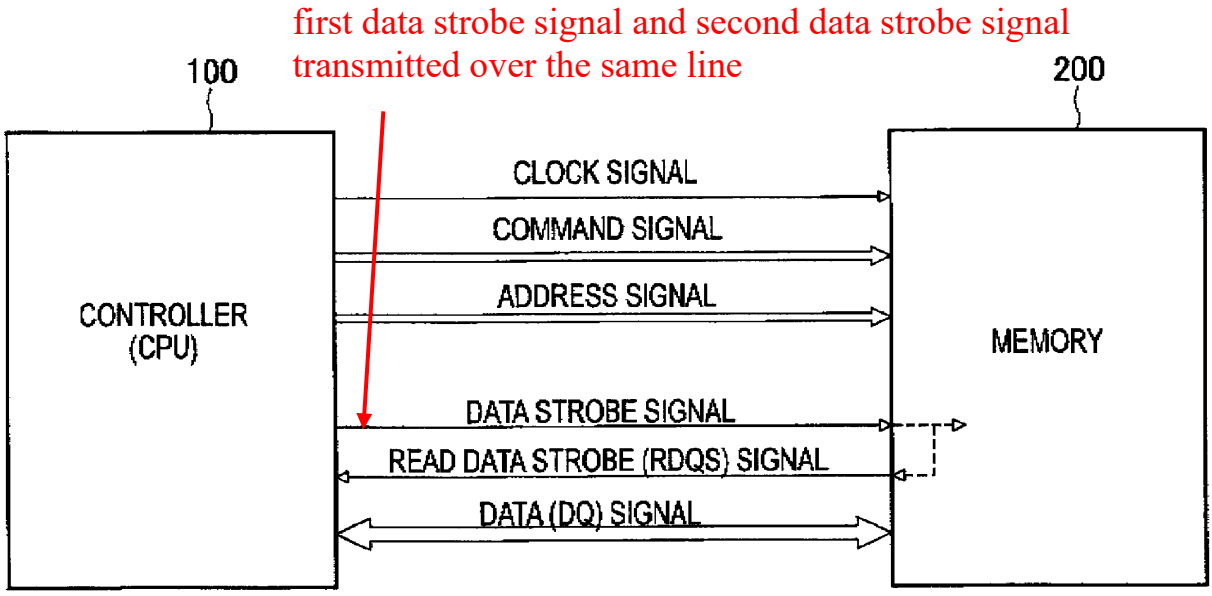


EX1005, Lee, Fig. 2 (annotated); EX1003, ¶ 54.

Lee's read operations are described as "conventional read operations." EX1005, Lee, [0025]. Such conventional read operations include the memory generating the strobe signal SDfM ("*read data strobe signal*") in response to receipt of the strobe signal SDtM ("*second data strobe signal*"). "To send data read from the memory 120 to the memory controller 140, first, the memory controller 140 transfers the second strobe signal SDtM to the memory 120. The memory 120 generates the third strobe signal SDfM **in response to** the received second strobe signal SDtM." EX1005, Lee, [0025].

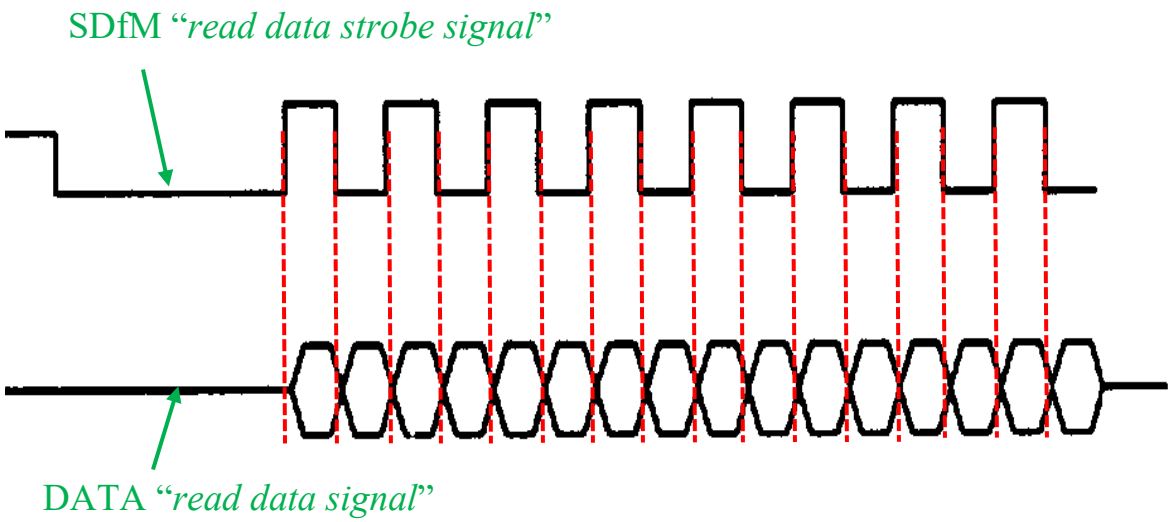
Note that the SDtM signal of the read operation ("*second data strobe*

signal") is different than the SDtM signal of the write operation ("*first data strobe signal*") because they are sent at different times. In other words, while both SDtM signals traverse the same line they are distinct signals because they are sent at different times during different types of operations. The '369 patent describes the claimed "*first data strobe signal*" and "*second data strobe signal*" similarly being transmitted over the same transmission line. *See* '369 patent, Fig. 1.



EX1001, Fig. 1 (annotated); EX1003, ¶ 56.

Second, like the write operation, the SDfM signal ("*read data strobe signal*") is in synchronization with the read data signal. As can be seen in the annotated figure below, the rising and falling times of the strobe signal SDfM.



EX1005, Lee, Fig. 2 (partial, annotated); EX1003, ¶ 57.

Accordingly, a POSITA would have understood that the SDfM signal is "*in synchronization with*" the read DATA signal. Again, a POSITA would have understood that synchronization is done for the purpose of telling the receiving component—in this case the controller—when to sample the data: "The memory controller 140 latches data DATA loaded on the data bus 166 in response to the third strobe signal SDfM." EX1005, Lee, [0025].

Thus, because Lee describes that during a read operation, the memory sends a data signal and a data strobe signal (which are synchronized) responsive to a signal from the controller, Lee renders obvious "*the controller being adapted, in a read operation, to send out a second data strobe signal and to receive a read data signal in synchronization with a read data strobe signal*" as claimed. EX1003, ¶¶ 53-59.

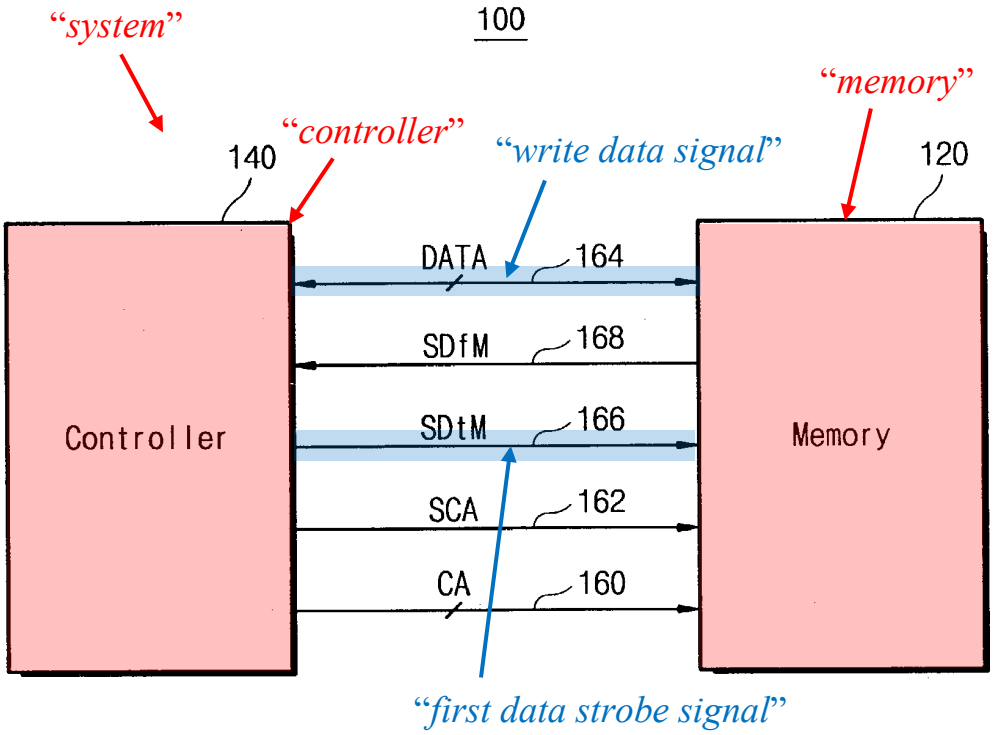
[1.4] ***the read data strobe signal being received by the controller in response to the second data strobe signal; and***

Lee explains that the SDfM signal is received by the controller in response to transmitting the SDtM signal: "The memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM." EX1005, Lee, [0021]; *see also* EX1005, Lee, [0024] ("The memory 120 generates the third strobe signal SDfM in response to the received second strobe signal SDtM").

Thus, because Lee's strobe signal SDfM is received in response to the strobe signal SDtM, Lee renders obvious "*the read data strobe signal being received by the controller in response to the second data strobe signal*" as claimed. EX1003, ¶¶ 60-61.

[1.5] ***a memory adapted to receive the write data signal in synchronization with the first data strobe signal in the write operation,***

First, Lee's system includes a memory 120 ("*memory*"), as described above at [1.0] and [1.1].



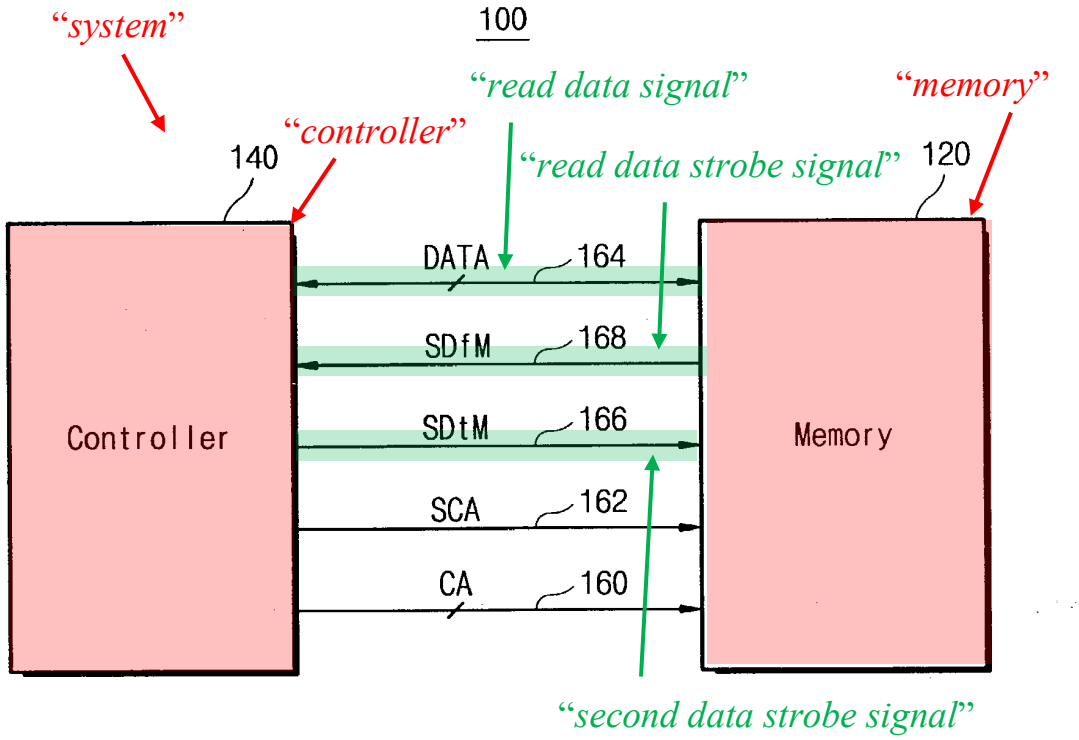
EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 62.

Second, as described above at [1.2], Lee describes the write operation in which the memory receives strobe signal SDtM ("*first data strobe signal*") over line 166 and data ("*write data signal*") over line 164.

Thus, because Lee describes a memory that receives the write data signal along with a strobe signal, Lee renders obvious "*a memory adapted to receive the write data signal in synchronization with the first data strobe signal in the write operation*" as claimed. EX1003, ¶¶ 62-64.

[1.6] ***the memory being adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and to send the read data signal synchronized with the read data strobe signal.***

As explained above at [1.3] and [1.4], Lee describes a read operation in which the memory transmits strobe signal SDfM ("*read data strobe signal*") over line 168 and data ("*read data signal*") over line 164. In Lee's read operation, "the memory controller 140 transfers to the memory 120 the second strobe signal SDtM as a transmission synchronous or reference signal at a time when it wants to receive data read out from the memory 120." EX1005, Lee, [0021]. These signals are transmitted by the memory in response to receiving the SDtM signal ("*second data strobe signal*"). "The memory 120 internally generates a third strobe signal SDfM **in response to** the second strobe signal SDtM. The read data that is read from the memory 120 is sent to the memory controller 140 together with the third strobe signal SDfM." EX1005, Lee, [0021]*; see also* EX1005, Lee [0025].



EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 65.

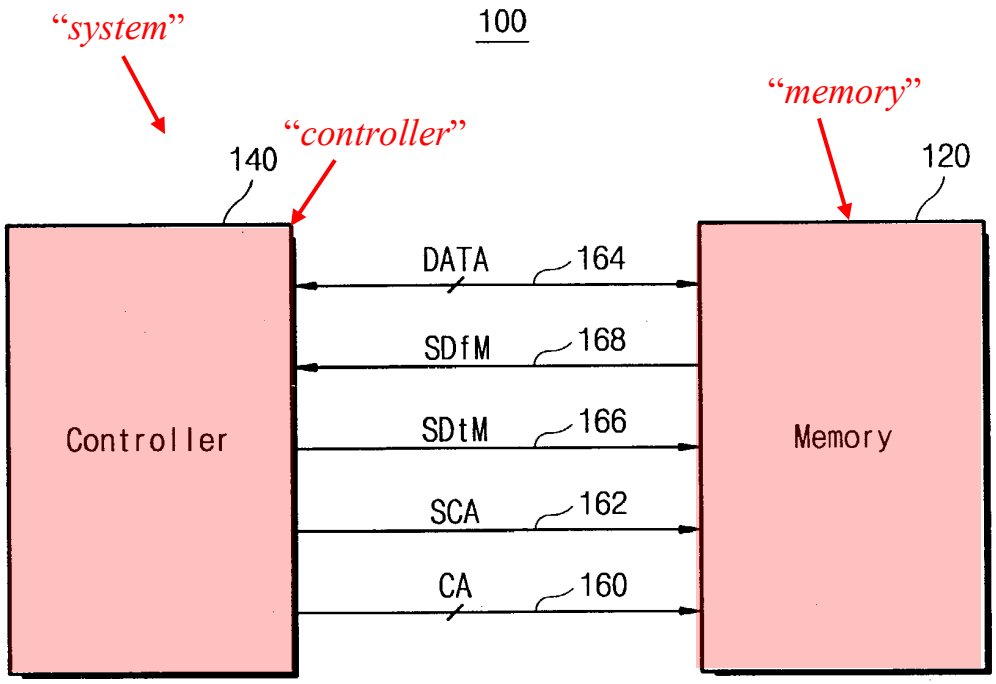
Thus, because Lee's memory system transmits the strobe signal SDfM in response to the SDtM signal, Lee renders obvious "*the memory being adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and to send the read data signal synchronized with the read data strobe signal*" as claimed. EX1003, ¶¶ 65-66.

3. Claim 6

[6.0] ***A controller for use in a system, the system including a memory,***

Lee describes a memory system 100 ("*system*") that includes a controller 140 ("*controller*") and a memory 120 ("*memory*"). "Referring to FIG. 1, a memory

system 100 according to particular embodiments the present invention includes **a memory 120 and a memory controller 140**." EX1005, Lee, [0017].



EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 67.

Thus, because Lee describes a memory system with a controller and a memory, Lee renders obvious a "*controller for use in a system, the system including a memory"* as claimed. EX1003, ¶¶ 67-68.

[6.1] *the controller being adapted to send out a first data strobe signal and a write data signal to the memory in a write operation, the write data signal being synchronized with the first data strobe signal*,

For the reasons explained above at [1.1] and [1.2], Lee renders obvious "*the controller being adapted to send out a first data strobe signal and a write data signal to the memory in a write operation, the write data signal being synchronized*

with the first data strobe signal" as claimed. EX1003, ¶ 69.

[6.2] ***the controller being adapted to send out a second data strobe signal to the memory and to receive a read data signal in synchronization with a read data strobe signal from the memory in a read operation***,

For the reasons explained above at [1.3], Lee renders obvious "*the controller being adapted to send out a second data strobe signal to the memory and to receive a read data signal in synchronization with a read data strobe signal from the memory in a read operation*" as claimed. EX1003, ¶ 70.

[6.3] ***the read data strobe signal received by the controller corresponding to the second data strobe signal in the read operation***.

As explained above at [1.4], Lee's SDfM signal is received by the controller in response to transmitting the SDtM signal: "The memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM." EX1005, Lee, [0021]. Because the SDfM signal ("*read data strobe signal*") is received "in response to" the SDtM signal of the read operation ("*second data strobe signal*"), the SDfM signal *corresponds* to the SDtM signal. The SDfM signal also corresponds to the SDtM signal in that it has the same form: "The third strobe signal SDfM, as illustrated in FIG. 2, may have the same waveform as the second strobe signal SDtM." EX1005, Lee, [0025].

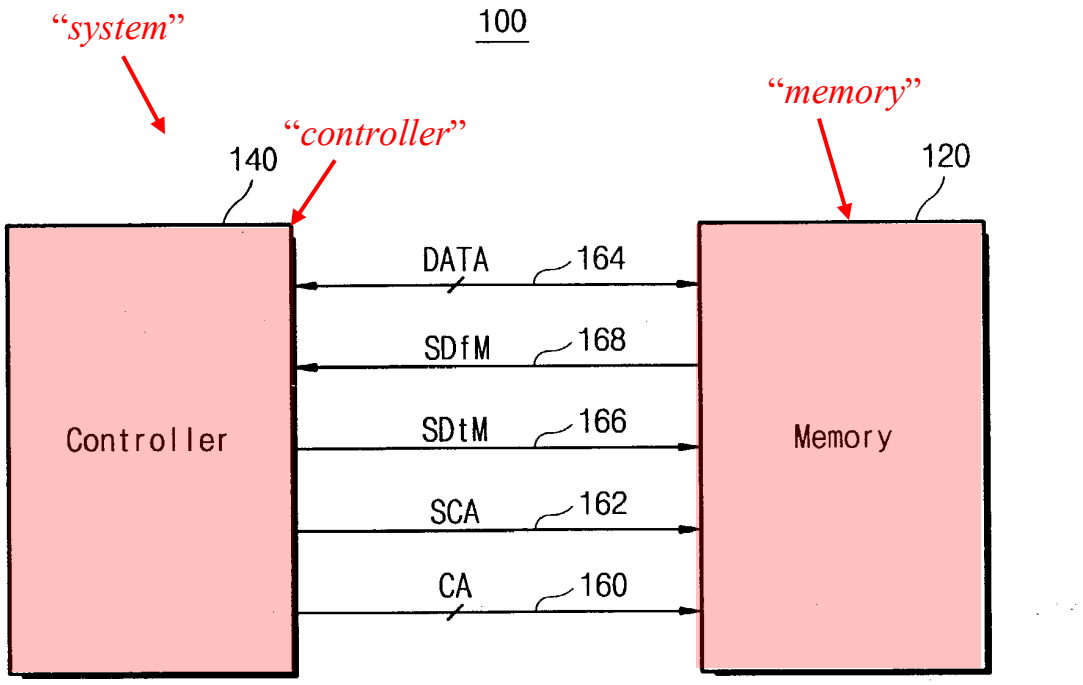
Thus, Lee renders obvious "*the read data strobe signal received by the controller corresponding to the second data strobe signal in the read operation*" as

claimed. EX1003, ¶¶ 71-72.

4. Claim 10

[10.0] ***A memory for use in a system, the system including a controller,***

Lee describes a memory system 100 ("*system*") that includes a controller 140 ("*controller*") and a memory 120 ("*memory*"). "Referring to FIG. 1, a memory system 100 according to particular embodiments the present invention includes **a memory 120 and a memory controller 140**." EX1005, Lee, [0017].



EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 73.

Thus, Lee renders obvious a "*memory for use in a system, the system including a controller"* as claimed. EX1003, ¶¶ 73-74.

[10.1] ***the controller outputting a data strobe signal in a read operation, the***

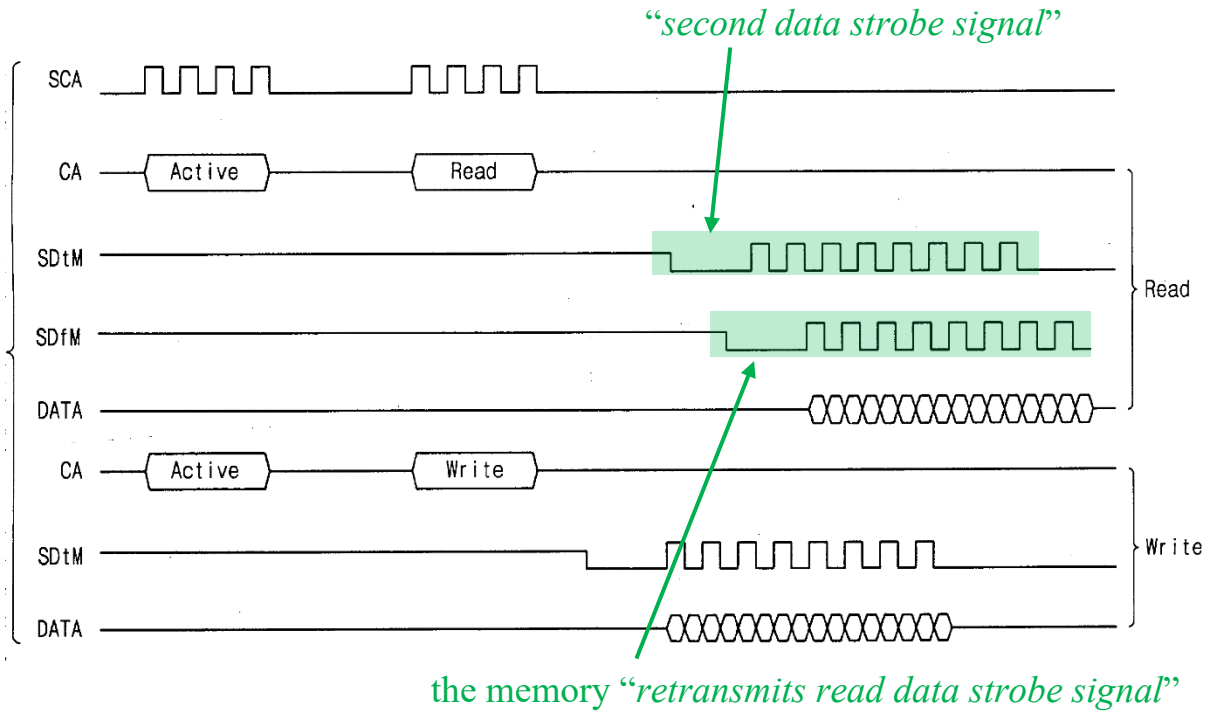
memory being adapted to send out a read data strobe signal to the controller in response to the data strobe signal and to send out a read data signal synchronized with the read data strobe signal in a read operation.

For the reasons explained above at [1.3], [1.4], and [1.6], Lee renders obvious "*the controller outputting a data strobe signal in a read operation, the memory being adapted to send out a read data strobe signal to the controller in response to the data strobe signal and to send out a read data signal synchronized with the read data strobe signal in a read operation*" as claimed. EX1003, ¶ 75.

5. Claim 14

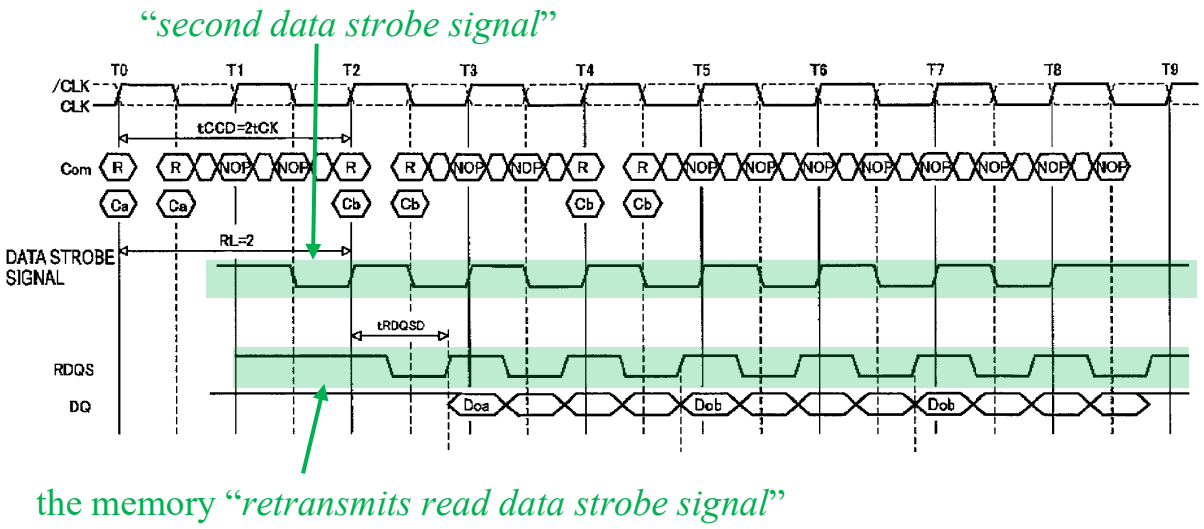
[14.1] ***The system of claim 1, wherein in the read operation the memory retransmits the second data strobe signal as the read data strobe signal.***

Lee explains that "The memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM." EX1005, Lee, [0021]. Lee also explains that "[t]he third strobe signal SDfM, as illustrated in FIG. 2, **may have the same waveform** as the second strobe signal SDtM delayed by a predetermined time." EX1005, Lee, [0025]. Thus, by generating the third strobe signal SDfM ("*read data strobe signal*") that has the same waveform as the received the SDtM signal ("*second data strobe signal*"), the memory system is *retransmitting* the SDtM signal as the SDfM signal. As shown in the figure below, the SDfM signal is identical to the SDtM signal in shape.



EX1005, Lee, Fig. 2 (annotated); EX1003, ¶ 76.

Notably, Lee describes retransmitting the strobe signal with at least the same level of specificity as the '369 patent, the specification of which does not provide any further explanation as to what it means to "retransmit" the second strobe signal as the read data strobe signal. What Lee explains and illustrates is thus similar to how the '369 patent illustrates the "retransmitted" read data strobe signal.



EX1001, Fig. 8 (annotated); EX1003, ¶ 77.

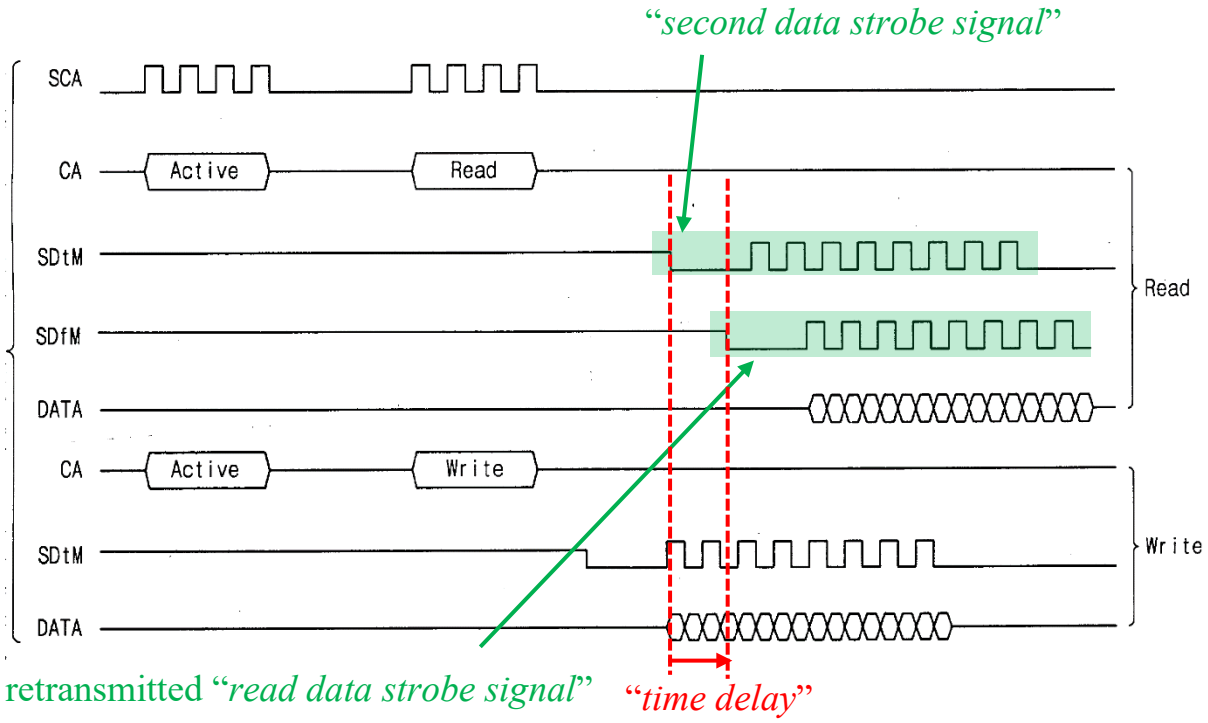
Thus, because Lee describes transmitting the strobe signal SDfM with the same waveform as the received SDtM signal, Lee renders obvious "*wherein in the read operation the memory retransmits the second data strobe signal as the read data strobe signal*" as claimed. EX1003, ¶¶ 76-78.

6. Claim 15

[15.1] ***The system of claim 14, wherein in the read operation the memory retransmits the second data strobe signal with a time delay as the read data strobe signal.***

Lee explains that "[t]he memory 120 internally generates a third strobe signal SDfM in response to the second strobe signal SDtM." EX1005, Lee, [0021]. Lee also explains that "[t]he third strobe signal SDfM, as illustrated in FIG. 2, **may have the same waveform** as the second strobe signal SDtM **delayed by a predetermined time**." EX1005, Lee, [0025]. Thus, by generating the third strobe

signal SDfM ("*read data strobe signal*") with the same waveform as the SDtM signal ("*second data strobe signal*") with a predetermined delay, the memory system is *retransmitting* the SDtM signal as the SDfM signal with a time delay. The time delay can be seen in the figure below.



EX1005, Lee, Fig. 2 (annotated); EX1003, ¶ 79.

Thus, because Lee describes transmitting the strobe signal SDfM with the same wave form as the received SDtM signal with a predetermined delay, Lee renders obvious "*wherein in the read operation the memory retransmits the second data strobe signal with a time delay as the read data strobe signal*" as claimed. EX1003, ¶¶ 79-80.

7. Claim 16

[16.1] ***The controller of claim 6, wherein in the read operation the controller receives a read data signal from the memory which is a retransmission of the second data strobe signal.***

See [14.1]. EX1003, ¶ 81.

8. Claim 17

[17.1] ***The controller of claim 16, wherein in the read operation the controller receives a read data signal from the memory which is a retransmission of the second data strobe signal with a time delay.***

See [15.1]. EX1003, ¶ 82.

9. Claim 18

[18.1] ***The memory of claim 10, wherein in the read operation the read data strobe signal is a retransmission of the received data strobe signal.***

See [14.1]. EX1003, ¶ 83.

10. Claim 19

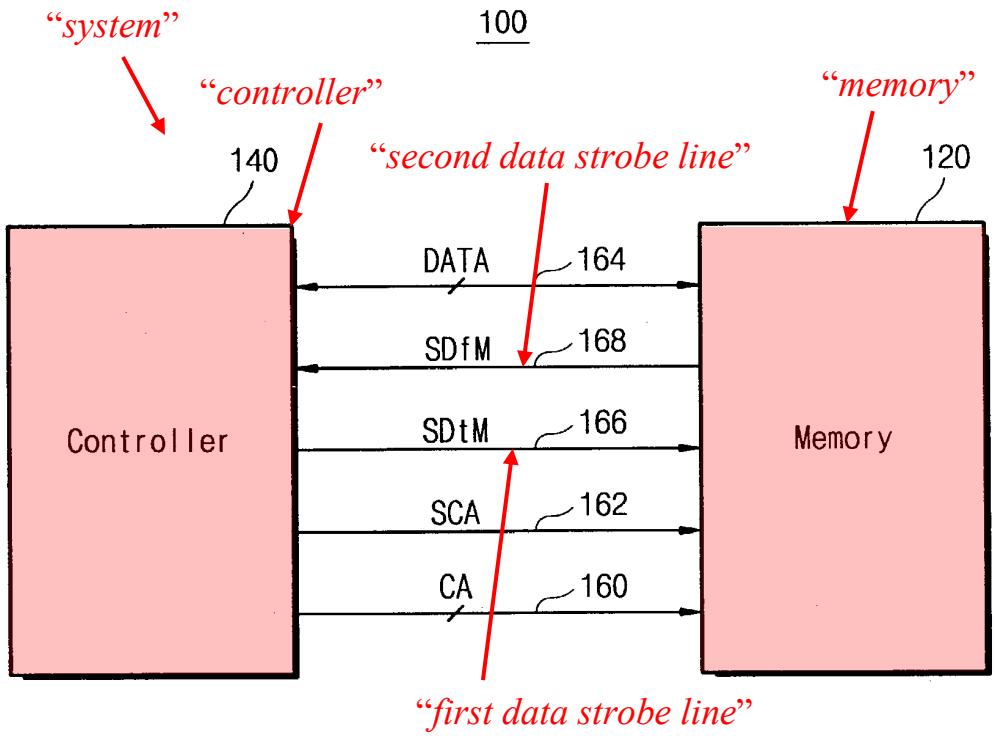
[19.1] ***The memory of claim 18, wherein in the read operation the read data strobe signal is a retransmission of the received data strobe signal with a time delay.***

See [15.1]. EX1003, ¶ 84.

11. Claim 25

[25.1] ***The system according to claim 1, further comprising first and second data strobe lines each provided between the controller and the memory, the first data strobe line transferring the first data strobe signal in the write operation from the controller to the memory, the first data strobe line transferring the second data strobe signal in the read operation from the controller to the memory, and the second data strobe line transferring the read data strobe signal in the read operation from the memory to the controller.***

First, as explained above at [1.1] and [1.3], Lee's system includes signal lines 166 and 168 ("*first and second data strobe lines*") between the memory and the controller.



EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 85.

Second, as explained above at [1.1], the signal line 166 carries the SDtM signal of the write operation ("*the first data strobe line transferring the first data strobe signal in the write operation from the controller to the memory*"): "For a write operation ... the memory controller 140 transfers data DATA to the memory 120 via a data bus 164, and transfers, as a transmission synchronous signal, the second strobe signal SDtM to the memory 120 **via a signal line 166**." EX1005,

Lee, [0020].

Third, as explained at [1.3], the signal line 166 also carries the SDtM signal of the read operation ("*the first data strobe line transferring the second data strobe signal in the read operation from the controller to the memory*"): "For a read operation ... the memory controller 140 transfers to the memory 120 the second strobe signal SDtM." EX1005, Lee, [0020]. *See also* EX1005, Lee, [0021] ("SDtM to the memory 120 **via a signal line 166**.").

Fourth, as also explained at [1.3], the SDfM signal is sent from the memory to the controller during the read operation ("*the second data strobe line transferring the read data strobe signal in the read operation from the memory to the controller*"): "Therefore, during the read operation the memory controller 140 receives the read data DATA from the memory 120 together with the third strobe signal SDfM at a required time." EX1005, Lee, [0021]. Further, the SDfM signal is sent over line 168. EX1005, Lee, [0033] ("the third strobe signal SDfM transferred via the signal line 168.").

Thus, because Lee's system includes signal lines 166 and 168 between the memory controller, and the signal lines carry the strobe signals of the read and write operations, Lee renders obvious "*further comprising first and second data strobe lines each provided between the controller and the memory, the first data strobe line transferring the first data strobe signal in the write operation from the*

controller to the memory, the first data strobe line transferring the second data strobe signal in the read operation from the controller to the memory, and the second data strobe line transferring the read data strobe signal in the read operation from the memory to the controller" as claimed. Ex.1003, ¶¶ 85-89.

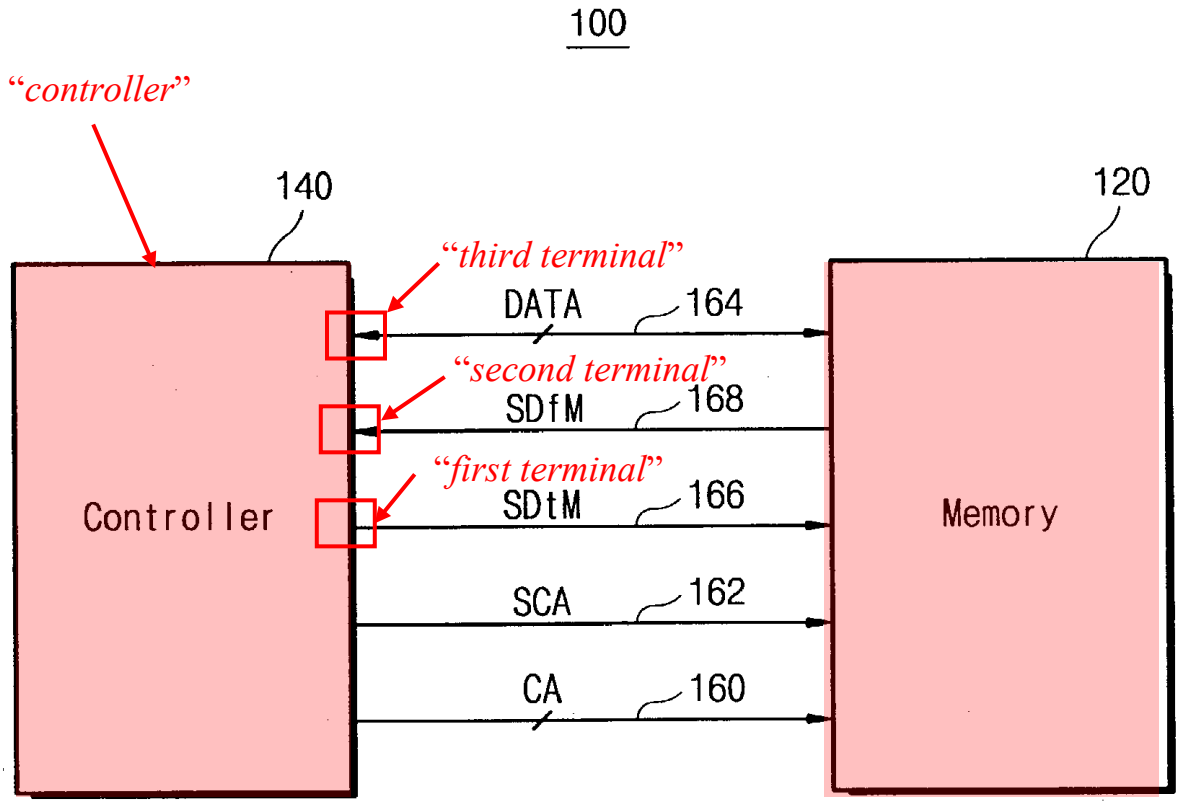
12. Claim 26

[26.0] ***A controller comprising a first terminal, a second terminal, and a third terminal,***

First, Lee describes a memory system 100 that includes a controller 140 ("*controller*") and a memory 120. "Referring to FIG. 1, **a memory system 100** according to particular embodiments the present invention includes **a memory 120** and a **memory controller 140**." EX1005, Lee, [0017].

Lee explains that communication between a memory and a controller uses "pins." "As is known to those of skill in the art, a memory typically provides external communications with, for example, a memory controller or chipset, **via pins (e.g., data pins, address pins, control pins, power pins, and so on**)." EX1005, Lee, [0006].

A POSITA would have understood that the pins for the communication lines 164, 166, and 168 may be referred to as terminals as well. Such terminals are shown in the annotated Fig. 1 below.



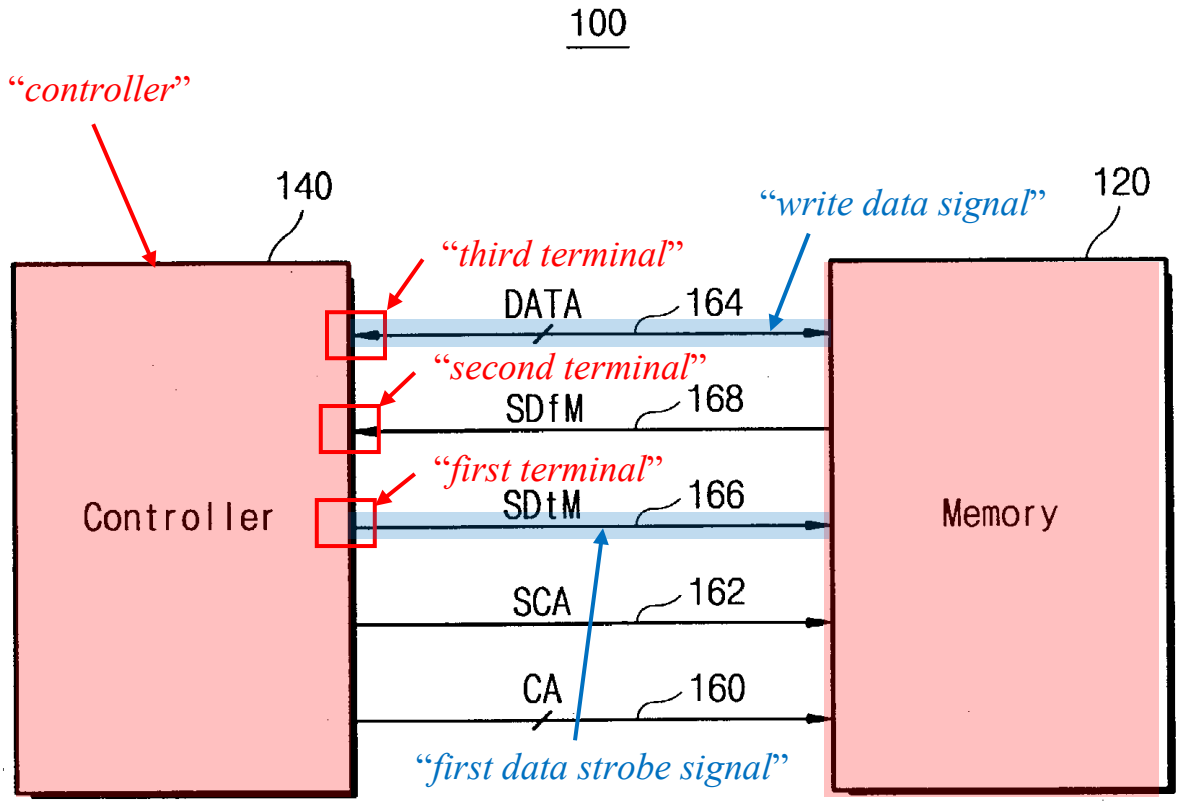
EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 92.

Thus, because Lee's controller includes pins for communicating with the memory, Lee renders obvious a "*controller comprising a first terminal, a second terminal, and a third terminal"* as claimed. EX1003, ¶¶ 90-93.

[26.1] ***the controller being adapted to produce a first data strobe signal at the first terminal and a write data signal at the third terminal in a write operation, the write data signal being synchronized with the first data strobe signal,***

First, Lee describes the write operation in which the controller transmits strobe signal SDtM ("*first data strobe signal*") over line 166 ("*first terminal*") and data ("*write data signal*") over line 164 ("*third terminal*"). "For a write operation, ... the memory controller 140 transfers data DATA to the memory 120 via a data

bus 164, and transfers, as a transmission synchronous signal, the second strobe signal SDtM to the memory 120 via a signal line 166." EX1005, Lee, [0020].



EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 94.

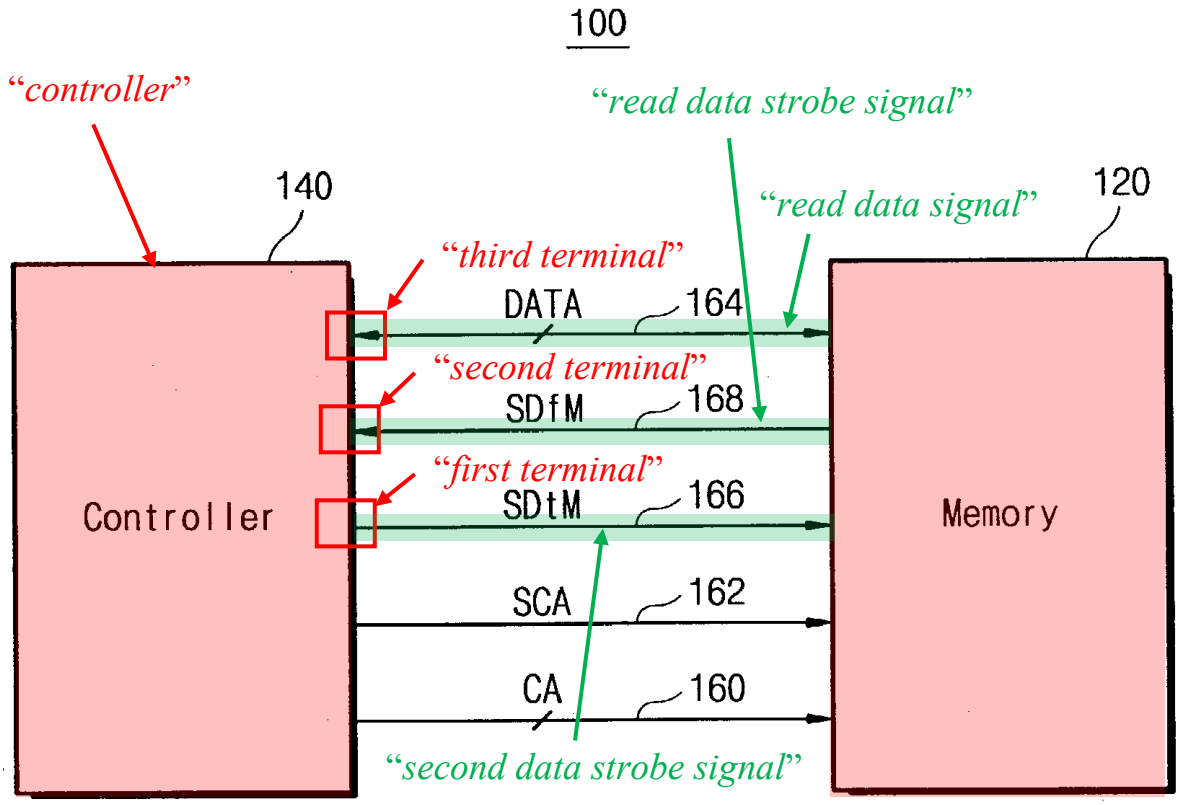
Second, Lee explains that the data signal is synchronous with the data strobe signal SDtM: "For a write operation ... the memory controller 140 transfers data DATA to the memory 120 via a data bus 164, and transfers, **as a transmission synchronous signal**, the second strobe signal SDtM to the memory 120 via a signal line 166." EX1005, Lee, [0020].

Thus, because Lee describes a controller 140 that transmits a strobe signal

SDtM and a data signal over lines 166 and 164 respectively, Lee renders obvious "*the controller being adapted to produce a first data strobe signal at the first terminal and a write data signal at the third terminal in a write operation, the write data signal being synchronized with the first data strobe signal*" as claimed. EX1003, ¶¶ 94-96.

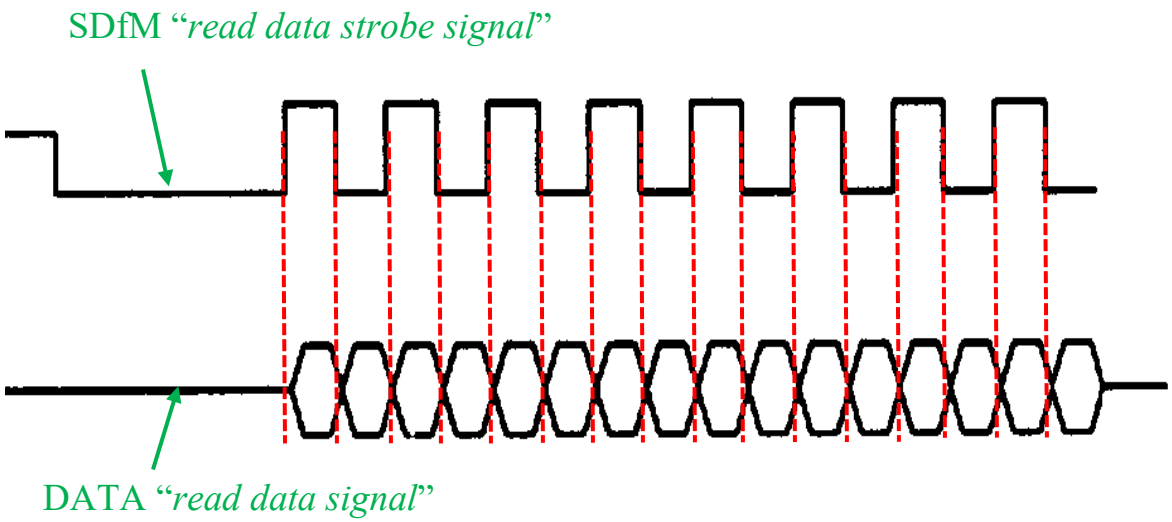
[26.2] ***the controller being adapted to produce a second data strobe signal at the first terminal and to receive a read data signal at the third terminal in synchronization with a read data strobe signal arriving at the second terminal from outside of the controller in a read operation.***

First, consistent with the discussion above at [1.3], Lee describes a read operation in which the memory (which is "*from outside the controller*") transmits strobe signal SDfM ("*read data strobe signal*") over line 168 ("*second terminal*") and data ("*read data signal*") over line 164 ("*third terminal*") in response to the SDtM signal ("*second data strobe signal*"). "For a read operation, ... the memory controller 140 transfers to the memory 120 the second strobe signal SDtM as a transmission synchronous or reference signal at a time when it wants to receive data read out from the memory 120." EX1005, Lee, [0021]. In response, "the memory controller 140 receives the read data DATA from the memory 120 together with the third strobe signal SDfM at a required time." EX1005, Lee, [0021].



EX1005, Lee, Fig. 1 (annotated); EX1003, ¶ 97.

Second, like the write operation, the SDfM signal ("*read data strobe signal*") is in synchronization with the read data signal. As can be seen in the annotated figure below, the rising and falling times of the strobe signal SDfM are synchronized with the switching of the data signal.



EX1005, Lee, Fig. 2 (partial, annotated); EX1003, ¶ 98.

Accordingly, a POSITA would have understood that the SDfM signal is "*in synchronization with*" the read DATA signal. Again, a POSITA would have understood that synchronization is done for the purpose of telling the receiving component—in this case the memory—when to sample the data: "The memory controller 140 latches data DATA loaded on the data bus 166 in response to the third strobe signal SDfM." Lee, [0025]; EX1003, ¶ 99.

Thus because Lee describes memory that transmits a data signal over line 164 and a strobe signal SDfM over line 168 responsive to a strobe signal SDtM over line 166, Lee renders obvious "*the controller being adapted to produce a second data strobe signal at the first terminal and to receive a read data signal at the third terminal in synchronization with a read data strobe signal arriving at the second terminal from outside of the controller in a read operation*" as claimed.

EX1003, ¶¶ 97-100.

13. Claim 27

[27.1] ***The controller according to claim 26, wherein the read data strobe signal is generated outside of the controller in response to the second data strobe signal.***

Lee explains that the SDfM signal is generated by the memory ("*outside of the controller*"): "The **memory 120 internally generates** a third strobe signal SDfM in response to the second strobe signal SDtM." EX1005, Lee, [0021]. Furthermore, as explained above at [1.3] and [1.4], the strobe signal SDfM ("*read data strobe signal*") is generated "in response to" receiving the strobe signal SDtM ("*second data strobe signal*").

Thus, because Lee's memory generates the strobe signal SDfM in response to the strobe signal SDtM, Lee renders obvious "*the read data strobe signal being received by the controller in response to the second data strobe signal*" as claimed. EX1003, ¶¶ 101-02.

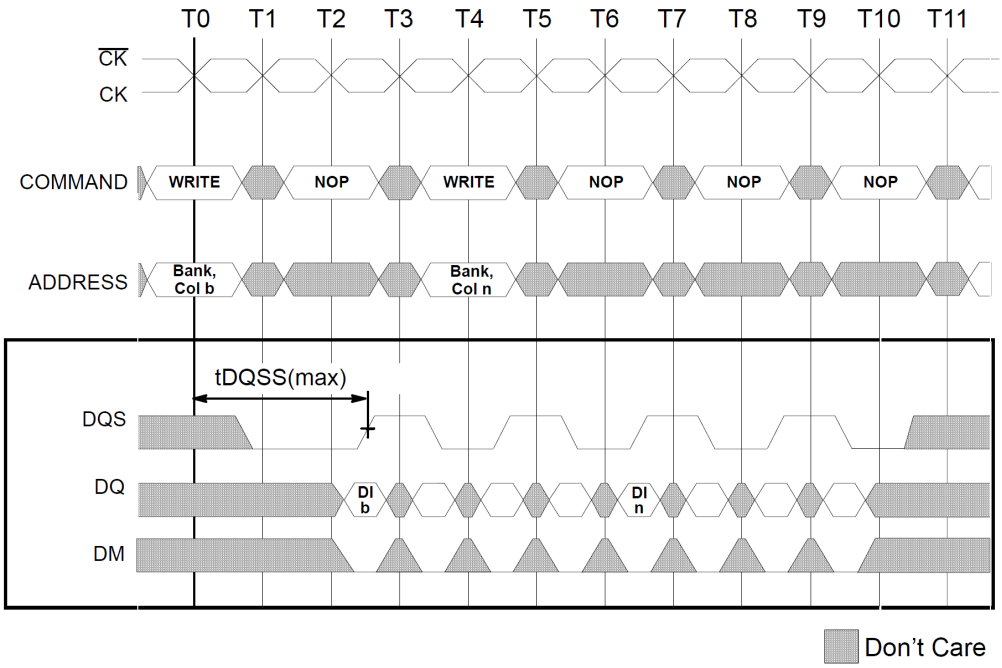
E. Ground 2: Claims 2, 7, and 11 are Obvious in View of Lee and JEDEC

A POSITA would have found it obvious for Lee's SCA signal to be implemented as a continuous clock signal consistent with the JEDEC standard for memory systems. EX1003, ¶ 103.

1. Summary of JEDEC

The Joint Electron Device Engineering Council (JEDEC) is a standard setting body in the electronics industry. The JEDEC Solid State Technology Association produces standards related to memory devices. For example, version JESD79C (EX1007, JEDEC) describes standards for Double Data Rate (DDR) Synchronous DRAM (SDRAM). EX1007, JEDEC, 1; EX1003, ¶¶ 104-06.

The JEDEC standard describes using a clock signal CK that is synchronized with command signals. As shown in the figure below, the CK signal (and its inversion, CK/) is a continuous clock signal that is synchronized with the command signal. EX1003, ¶ 107.



EX1007, JEDEC, Fig. 22.

2. Motivation to Combine Lee and JEDEC

A POSITA would have found it obvious to implement Lee's SCA signal in any of a variety of known and suitable ways—in either a synchronous or asynchronous manner. Lee's SCA signal is used to latch command/address information: "That is, the command/address information CA is transferred to the memory 120 from the memory controller 140 together with the first strobe signal SCA based on the source synchronous interface. The memory 120 latches the command/address information CA in response to the first strobe signal SCA." EX1005, Lee, [0019]. Lee further explains that the SCA signal is applied intermittently: The SCA signal "can be implemented using a clock signal that is toggled only during a desired period, for example, when data is on the CA bus or

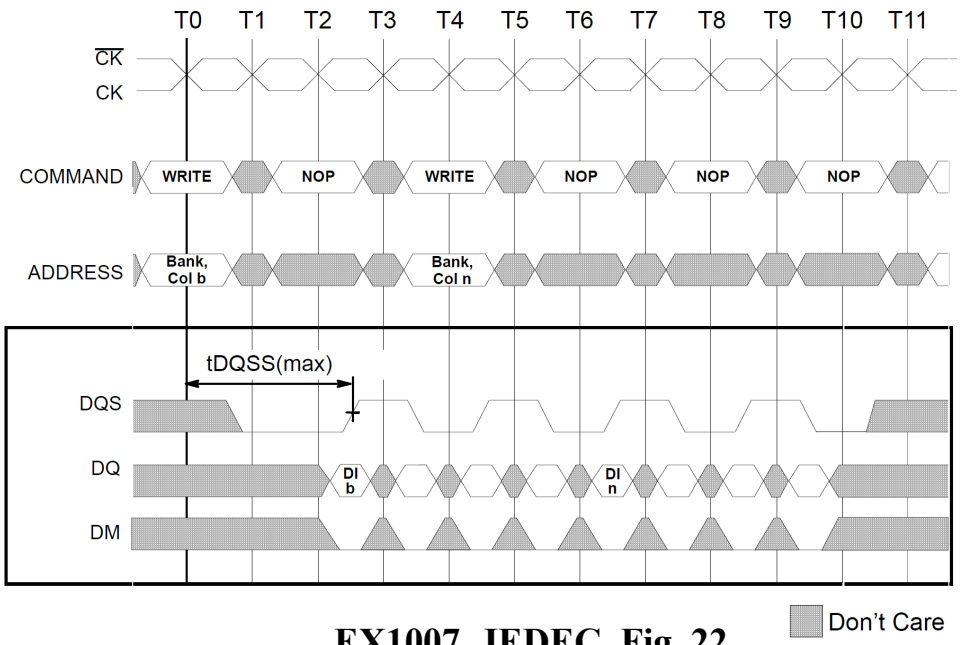
the DATA bus." EX1005, Lee, [0035]. Using such an intermittent signal is an example of asynchronous memory. *See supra*, IV.C.; EX1003, ¶ 108.

While Lee describes using an intermittent SCA signal to latch command/address information (i.e., asynchronous memory), a POSITA would have found it obvious to implement the SCA signal as a clock signal to register command/address information (i.e., synchronous memory). Lee provides evidence that it was known to use either synchronous or asynchronous memory. As Lee explains, "the amount of current consumed by a memory system in a standby state results from the clock signal used to synchronize operations **of a synchronous memory**." EX1005, Lee, [0034]. Lee chooses to use an asynchronous memory. "[A]ccording to embodiments of the present invention, as illustrated for example in FIG. 3, the strobe signals, such as SCA and SDtM, that are used as transmission references or synchronous signals, are used in the memory 120 only as a latch enable or latching signal." EX1005, Lee, [0034]. "This means that the memory 120 performs read and write operations **in an asynchronous manner**, for example, using a delay chain as a state machine." EX1005, Lee, [0034]; EX1003, ¶ 109.

A POSITA would have understood that there are design tradeoffs between using synchronous and asynchronous memories. For example, asynchronous memory can provide the benefit of less power consumption, as explained by Lee. *See* EX1005, Lee, [0034]. Synchronous memory—using a clock signal for

sampling information—provides the benefit of higher bandwidth capabilities. *See* EX.1006 (Prince), 5. Indeed, POSITAs used systems that had the capability to switch between synchronous and asynchronous modes. *See generally* EX1008, Mills, title, abstract. Accordingly, a POSITA implementing a memory system according to Lee's teachings would have found it obvious to use either synchronous or asynchronous memory, as either was a known option, and would choose between the two based on their specific design/power considerations. *See Intel Corp. v. Pact XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023) (It is "not necessary to show that a combination is the *best* option, only that it be a *suitable* option") (emphasis in the original). If a POSITA wanted to design the system for power conservation, they would likely choose Lee's asynchronous option. If a POSITA wanted to design the memory system for high bandwidth, they would likely choose the synchronous option. EX1003, ¶ 110.

POSITAs knew how to implement memories using a clock signal and registers because industry standards defined how to do so. The JEDEC standard is an example. As explained above, the JEDEC standard defines the use of a continuous clock signal that is transmitted from the controller to the memory. EX1003, ¶ 110.



EX1007, JEDEC, Fig. 22

As can be seen from the figure above, the command and address lines are synchronized with the clock signal CK. Also as can be seen from above, the data strobe signal DQS is independent of and separated from the clock signal CK. (Similarly, Lee's data strobe signals are independent of and separated from the SCA signal.) Furthermore, the JEDEC standard does not specify the source of the clock signal, and it would be obvious and in fact common in the art for the memory controller to produce the clock signal, such as is taught by Lee with reference to the SCA signal. EX1005, Lee, [0019]; EX1003, ¶ 111.

Accordingly, a POSITA would have found it obvious to implement Lee's SCA signal using a clock signal, consistent with the JEDEC standard. The results of using a standardized process such as the one described in the JEDEC standard

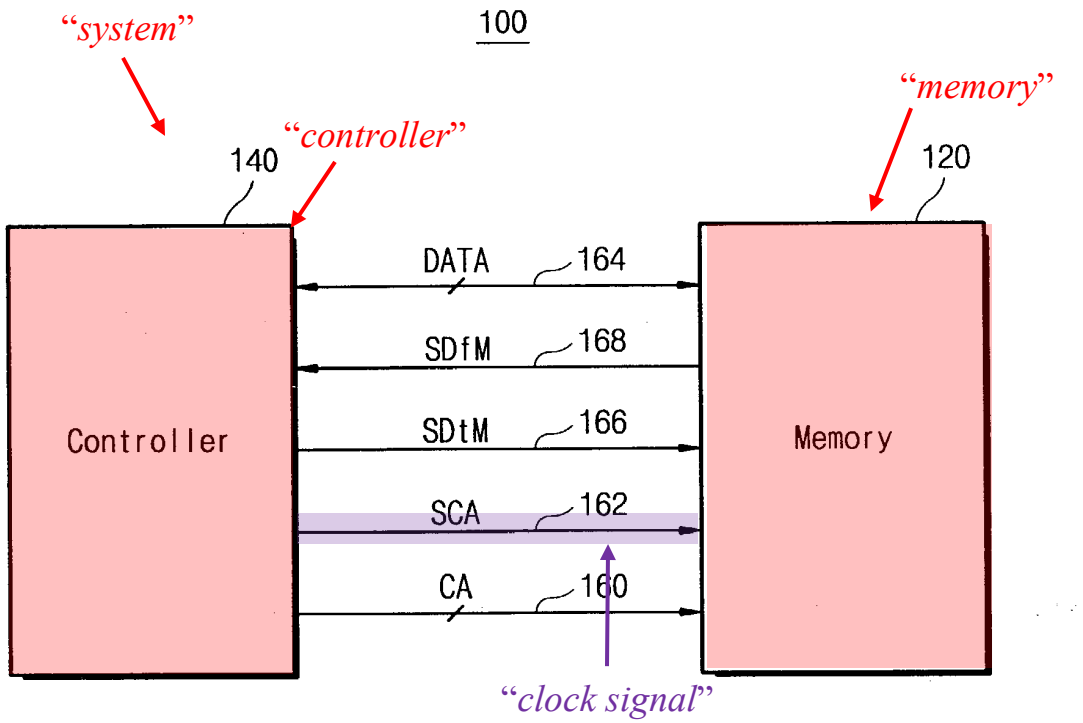
would have been predictable because standardized techniques are heavily vetted: "JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Council level and subsequently reviewed and approved by the EIA General Counsel." EX1007, JEDEC, 2. For this reason, a POSITA also would have had a reasonable expectation of success. EX1003, ¶ 113. Further still, there is a general familiarity and ease-of-design in the art using synchronous devices and a continuous clock, as evidenced by the JEDEC Standard, that would motivate a POSITA to use a continuous clock for the memory device of Lee. EX1003, ¶ 112.

Thus, the combination of Lee and JEDEC is merely a substitute of one known element (Lee's intermittent SCA signal) with another (standardized clock signal) to obtain predictable results. *See KSR Int'l Co. v. Teleflex Inc.,* 550 U.S. 398 (2007); EX1003, ¶ 113.

3. Claim 2

[2.1] ***The system according to claim 1, wherein the controller is further adapted to produce a clock signal and to send the clock signal to the memory, each of the first and the second data strobe signals and the read data strobe signal being independent of and separated from the clock signal***.

First, Lee's memory controller produces the SCA signal which is sent from the controller to the memory: "The memory controller 140 sends the first strobe signal SCA as a transmission reference or synchronous signal to the memory 120 via a signal line 162." EX1005, Lee, [0019].

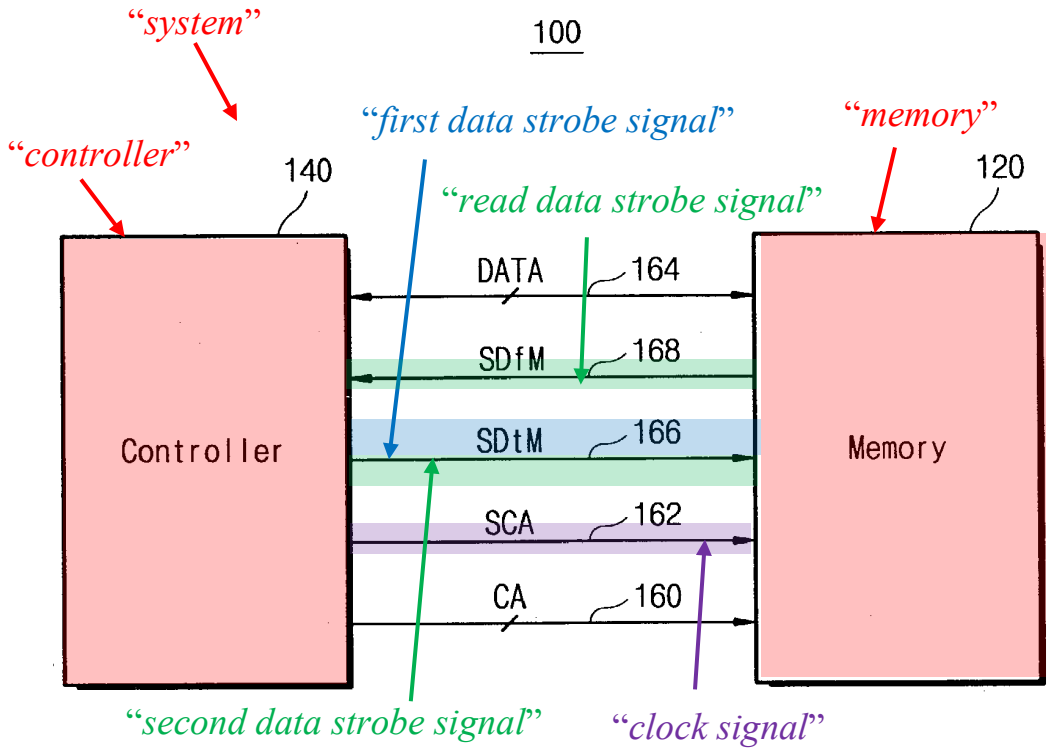


Combination of Lee and JEDEC
(annotated based on EX1005, Lee, Fig. 1); EX1003, ¶ 114.

Lee explains that the SCA signal "can be implemented using a **clock signal** that is toggled only during a desired period." EX1005, Lee, [0035]. A POSITA would have found it obvious to substitute Lee's SCA signal using a clock signal for the reasons explained above at X.E.2. EX1003, ¶ 115. Furthermore, Lee's controller is "*adapted to produce*" the SCA signal because the controller *generates*

the SCA signal: "In FIG. 3, input/output interface circuits of a memory controller 140 are illustrated, however, additional function of the memory controller may be provided, for example, **to control the generation of** the signals SDtM_CON, **SCA_CON**, and CA_CON." EX1005, Lee, [0029].

Second, Lee's SCA signal is independent from the other signals SDtM and SDfM, given that the SCA signal is sent across a different transmission line. Specifically, the SCA signal is sent over line 162, while SDtM ("*first data strobe signal*" in the write operation and "*second data strobe signal*" in the read operation) signals are sent over line 166 and the SDfM signal ("*read data strobe signal*") is sent over line 168.



Combination of Lee and JEDEC
(annotated based on EX1005, Lee, Fig. 1); EX1003, ¶ 117.

The SCA signal in the combination of Lee and JEDEC serves the same function as the clock signal described in the '369 patent. In Lee, the SCA signal is used to let the memory know when to sample data from the command/address lines: "That is, the command/address information CA is transferred to the memory 120 from the memory controller 140 together with the first strobe signal SCA based on the source synchronous interface. The memory 120 latches the command/address information CA in response to the first strobe signal SCA." EX1005, Lee, [0019].

Similarly, the '369 patent itself explains that "the internal clock signal is sent

to the memory 200 via the buffer as the clock signal." EX1001, 4:8-9. The memory system, "upon receiving the clock signal" then sends the "clock signal to circuits for command/address and so on." EX1001, 4:64-5:1; *see also* Fig. 3. A POSITA would have thus understood that the SCA signal in the combination of Lee and JEDEC is analogous to the clock signal recited in claim 2.

Thus, in the combination of Lee and JEDEC, because the controller generates and sends the SCA signal to the memory, and the SCA signal may be implemented as a clock signal that is separate and distinct from the data transfer strobe signals, Lee in view of JEDEC renders obvious "*wherein the controller is further adapted to produce a clock signal and to send the clock signal to the memory, each of the first and the second data strobe signals and the read data strobe signal being independent of and separated from the clock signal*" as claimed. EX1003, ¶¶ 114-120.

4. Claim 7

[2.1] ***The controller according to claim 6, wherein the controller is further adapted to produce a clock signal and to send the clock signal to the memory, each of the first and the second data strobe signals and the read data strobe signal being independent of and separated from the clock signal***.

See [2.1], Ground 2. EX1003, ¶ 121.

5. Claim 11

[11.1] ***The memory according to claim 10, the controller being further adapted to send out a clock signal and to send the clock signal to the memory, wherein each***

of the data strobe signal and the read data strobe signal is independent of and separated from the clock signal.

See [2.1]. EX1003, ¶ 122.

XI. CONCLUSION

Petitioner has established a reasonable likelihood that the Challenged Claims are unpatentable.

XII. MANDATORY NOTICES

A. Real Party-in-Interest

The real party-in-interest ("RPI") is Western Digital Technologies, Inc. ("Petitioner" or "WDT").

As shown in XII.B below, six litigations concerning the '369 Patent are pending, all involving WDT's customers as defendants. Petitioner submits that WDT is the only real party-in-interest, but regardless of whether any defendant should be named as an RPI, no RPI analysis is necessary because there are no time bar or estoppel implication for any defendant. *SharkNinja Operating LLC v. iRobot Corp.*, IPR2020-00734, Paper 11 (Oct. 6, 2020) (precedential) (no RPI analysis necessary at institution absent allegation of time bar or estoppel based on unnamed RPI).

B. Related Matters

Pursuant to 37 C.F.R. § 42.8(b)(2), to the best knowledge of the Petitioner, the '369 patent is or was involved in the following cases:

Case Heading	Number	Court	Filed	Status
Longitude Licensing Limited v. ASUSTeK Computer Inc. et al.	8-23-cv-00033	CDCA	Jan. 09, 2023	stayed pending the resolution of the Amazon Action with respect to WD
Longitude Licensing Limited v. Lenovo Group Limited et al.	8-23-cv-00035	CDCA	Jan. 09, 2023	stayed pending the resolution of the Amazon Action with respect to WD
Longitude Licensing Limited v. Acer Inc. et al.	8-23-cv-00036	CDCA	Jan. 09, 2023	stayed pending the resolution of the Amazon Action with respect to WD
Longitude Licensing Limited v. HP Inc.	8-23-cv-00038	CDCA	Jan. 09, 2023	stayed pending the resolution of the Amazon Action with respect to WD
Longitude Licensing Limited v. Amazon.com, Inc. (Amazon Action)	8-23-cv-00039	CDCA	Jan. 09, 2023	WD's motion to intervene granted; stayed pending the resolution of the Amazon Action with respect to WD

Case Heading	Number	Court	Filed	Status
Longitude Licensing Limited v. Dell Technologies Inc. et al.	8-22-cv-02312	CDCA	Dec. 23, 2023	stayed pending the resolution of the Amazon Action with respect to WD

C. Lead and Back-up Counsel and Service Information

Lead Counsel
David O'Dell
HAYNES AND BOONE, LLP
2323 Victory Ave. Suite 700
Dallas, TX 75219
Phone: (972) 739-8635
Fax: (214) 200-0853
david.odell.ipr@haynesboone.com
USPTO Reg. No. 42,044

Back-up Counsel
Calmann J. Clements
HAYNES AND BOONE, LLP
2323 Victory Ave. Suite 700
Dallas, TX 75219
Phone: (972) 739-8638
Fax: (214) 200-0853
calmann.clements.ipr@haynesboone.com
USPTO Reg. No. 66,910

Hong Shi
HAYNES AND BOONE, LLP
2323 Victory Ave. Suite 700
Dallas, TX 75219
Phone: (512) 867-8440
Fax: (214) 200-0853
hong.shi.ipr@haynesboone.com
USPTO Reg. No. 69,009

Please address all correspondence in this proceeding to lead and back-up counsel. Petitioner consents to service in this proceeding by email at the addresses above

Respectfully submitted,

Dated: July 14, 2023
HAYNES AND BOONE, LLP
2323 Victory Avenue, Suite 700
Dallas, Texas 75219
Customer No. 27683

/David M. O'Dell/
David M. O'Dell
Lead Counsel for Petitioner
Registration No. 42,044

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Petitioner hereby certifies, in accordance with and reliance on the word count provided by the word-processing system used to prepare this Petition, that the number of words in this paper is 9,696. Pursuant to 37 C.F.R. § 42.24(d), this word count excludes the table of contents, table of authorities, mandatory notices under § 42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing.

Dated: July 14, 2023

/David M. O'Dell/
David M. O'Dell
Lead Counsel for Petitioner
Registration No. 42,044

CERTIFICATE OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105, service was made on Patent Owner as detailed below.

Date of service	July 14, 2023
Manner of service	FEDERAL EXPRESS
Documents served	Petition for *Inter Partes* Review Under 35 U.S.C. § 312 and 37 C.F.R. § 42.104 of U.S. 7,697,369; Petitioner's Exhibit List; Exhibits 1001-1013.
Persons served	SUGHRUE MION, PLLC 2000 PENNSYLVANIA AVENUE, N.W. SUITE 9000 WASHINGTON, DC 20006 UNITED STATES

/David M. O'Dell/
David M. O'Dell
Lead Counsel for Petitioner
Registration No. 42,044