UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KIOXIA AMERICA, INC. and KIOXIA CORPORATION,

Petitioners,

v.

BiTMICRO LLC,

Patent Owner.

Case No.: IPR2023-00742
U.S. Patent No. 8,010,740

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,010,740

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Challenged Claims of U.S. Patent No. 8,010,740

Claim element	**Claim 1**
[Claim 1Pre]	A mapping table for optimizing memory operations performed by an electronic storage device in response to receiving an I/O transaction request initiated by a host, said mapping table comprising:
[Claim 1a]	a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs;
[Claim 1b]	a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs; and
[Claim 1c]	wherein, in response to receiving the I/O transaction request, said mapping table causes the electronic storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second LBA sets.
Claim element	**Claim 9**
[Claim 9]	The mapping table of claim 1, wherein said set of access parameters includes a bus identifier, an FDE identifier and a group identifier.
Claim element	**Claim 10**

[Claim 10]	The mapping table of claim 9, wherein said first and second PBA include different bus identifiers, different FDE identifiers and different group identifiers.
Claim element	**Claim 11**
[Claim 11]	The mapping table of claim 9, wherein said first and second PBA respectively include different combinations of said bus identifiers, said FDE identifiers, and said group identifiers.
Claim element	**Claim 12**
[Claim 12]	The mapping table of claim 1, wherein said first and second PBA include different bus identifiers.
Claim element	**Claim 13**
[Claim 13]	The mapping table of claim 1, wherein said first and second PBA include different FDE identifiers.
Claim element	**Claim 14**
[Claim 14]	The mapping table of claim 1, wherein said first and second PBA respectively include a first group identifier and a second group identifier.
Claim element	**Claim 15**
[Claim 15a]	The mapping table of claim 1: wherein said memory store includes a set of solid state memory devices that are coupled to a set of buses and that are controlled by a set of FDEs; and
[Claim 15b]	wherein said access parameter includes a group identifier for identifying at least a portion of said set of memory devices that are respectively controlled by different FDEs from said set of FDEs.
Claim element	**Claim 32**
[Claim 32 Pre]	An electronic storage device that includes a memory system that uses a memory table for increasing the likelihood that an operational load imposed on the storage apparatus during the processing of an I/O transaction request will be optimally distributed across storage device resources, said I/O transaction request received by said storage device from a requesting host, said electronic storage device comprising:

[Claim 32a]	a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA, said first and second LBA sets including respective sets of consecutive LBAs;
[Claim 32b]	a memory store that includes a set of flash devices, said set of flash devices includes a first physical memory location and a second physical memory location that are addressable by said first and second PBAs respectively;
[Claim 32c]	a memory system coupled to said memory store and disposed to use said mapping table during a memory operation;
[Claim 32d]	wherein said first PBA includes a first set of access parameters and said second PBA includes a second set of access parameters, and at least one difference between said first and second PBAs;
[Claim 32e]	and wherein said mapping table increases the likelihood that that the operational load imposed on the storage apparatus during the processing of the I/O transaction request will be optimally distributed across storage device resources.
Claim element	**Claim 34**
[Claim 34a]	The electronic storage device of claim 32, wherein the processing of the I/O transaction request includes a first memory operation performed using said first PBA and a second memory operation performed using said second PBA;
[Claim 34b]	said first and second PBAs respectively associated with a first set of access parameters and a second set of access parameters, and said set of first and second set of access parameters differing by at least one access parameter.

I. INTRODUCTION

KIOXIA Corporation and KIOXIA America, Inc. ("Petitioners") petition for institution of inter partes review ("IPR") of claims 1, 9-15, 32, and 34 ("challenged claims") of U.S. Patent No. 8,010,740 ("the '740 patent"). Ex-1001.

II. GROUNDS FOR STANDING

Petitioners certify that the '740 patent is available for review under 35 U.S.C. § 311(c) and that Petitioners are not estopped from requesting *inter partes* review of the challenged claims on the grounds identified in this Petition.

III. FEES

The Commissioner is hereby authorized to charge or credit the fee specified by 37 C.F.R. § 42.15(a), and any other additional fees, to Bracewell LLP Deposit Account No. 50-0259.

IV. PRECISE RELIEF REQUESTED

Petitioners request review of the challenged claims under 35 U.S.C. § 311 and cancellation of the challenged claims under pre-AIA 35 U.S.C. §§ 102(a), 102(b), and 103(a) in view of the prior art and grounds described herein.

A. Prior Art

1. Sukegawa

Petitioners rely on U.S. Patent No. 5,572,466 ("Sukegawa"). Ex-1005.

Sukegawa was issued on November 5, 1996, more than a year before the alleged priority date for the '740 patent, and qualifies as a prior art printed publication under at least pre-AIA 35 U.S.C. § 102(b).

2. Bruce

Petitioners also rely on U.S. Patent No. 5,822,251 ("Bruce"). Ex-1006. Bruce was issued on October 13, 1998, more than a year before the alleged priority date for the '740 patent, and qualifies as a prior art printed publication under at least pre-AIA 35 U.S.C. § 102(b).

3. Bennett

Petitioners rely on U.S. Patent No. 7,139,864 ("Bennett"). Ex-1007. Bennett was filed on December 30, 2003, and was published on June 30, 2005. Accordingly, Bennett qualifies as a prior art printed publication under at least pre-AIA 35 U.S.C. § 102(a).

B. IPR Grounds

Ground	Claims	Statutory Basis
1	1, 32, 34	Anticipation under pre-AIA § 102(b) in view of Sukegawa
2	9-15	Obviousness under pre-AIA § 103(a) in view of Sukegawa and Bruce
3	1, 32	Anticipation under pre-AIA § 102(a) in view of Bennett

Ground	Claims	Statutory Basis
4	9-15, 34	Obviousness under pre-AIA § 103(a) in view of Bennett and Bruce

V. THE '740 PATENT

A. Overview of the '740 Patent

The '740 Patent purportedly relates to "optimizing memory operations in a memory system suitable for use in an electronic storage device." Ex-1001 at 1:16-18. The '740 patent discloses that non-volatile solid-state memory, as well as "flash memory related techniques that include read-modify-write transactions, wear leveling, bad block management or any combination of these," and the use of "flash translation layers," were all well-known at the time of filing. *Id.* at 1:28-32, 1:54-65. Notwithstanding this fact, the '740 Patent alleges that there existed a need to "optimize[]" memory operations by "increasing the likelihood that . . . the operational load imposed on the storage device by these memory operations will be optimally distributed across different storage device resources." *Id.* at 2:11-21.

The '740 Patent thus discloses a "mapping table" that is "disposed to associate" sets of logical block addresses ("LBAs") from a host system to physical block addresses ("PBAs") in a memory store. *Id.*, Abstract. The PBAs "represent a unique addressable physical memory location" and may be "represented" by a set of "access parameter fields," which may include a bus identifier, a flash DMA engine

(or "FDE") identifier, and a group identifier. *Id.*, at 5:30-38. The access parameters comprising a **bus identifier**, **FDE identifier**, and **group identifier** are shown in annotated Figure 2 of the '740 Patent, below:

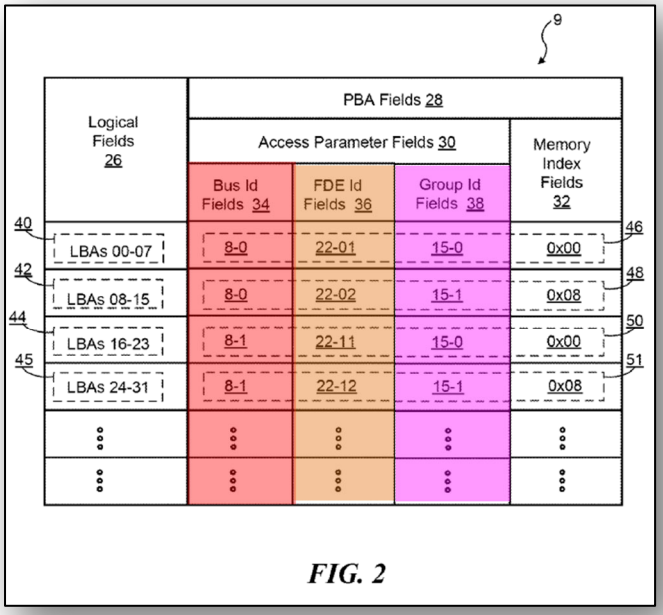

FIG. 2

Despite the '740 patent's assertions, logical to physical address mapping tables were well known prior to the '740 Patent. Both Sukegawa and Bennett, analyzed herein, disclose such tables and confirm that they had been in use long before the priority date of the '740 Patent, as discussed in detail below. The identification of a unique addressable physical memory location (PBA) by identifiers for a bus, DMA engine (or FDE), and a group of flash devices was similarly well-known prior to the '740 Patent's filing date, as demonstrated by Bruce, which is discussed below. Furthermore, use of mapping tables to provide such information

represents a common design approach to improving memory system performance and allowing for optimization of memory operations, which would reasonably include the access parameters of Bruce. Thus, as explained below, a person of ordinary skill in the art ("POSITA") would not have found the '740 Patent's disclosures to be novel or non-obvious.

B. Prosecution History

During the prosecution of the application underlying the '740 Patent, the Examiner did not issue any rejections based on prior art. However, the Examiner did reject the pending claims for failure to comply with the written description requirement, concluding that the specification "does not describe how the mapping table causes the storage device to perform optimized memory operation[s] on memory location[s] in such a way that is understood by one having ordinary skill in the related art." Ex-1002 at 3-4. After the Applicant submitted arguments responding to this rejection, the Examiner issued a Notice of Allowance on April 13, 2011, and subsequently entered clerical amendments to the claims submitted by the applicant on July 12, 2011. *See id.* at 28-36.

VI. LEVEL OF ORDINARY SKILL IN THE ART

As of the priority date, a POSITA would have had at least a Bachelor's degree in electrical or computer engineering, or a similar field, and at least two years of work experiences in the computer memory or data storage industry. Ex-1003, ¶¶ 57-

59. A POSITA could have substituted less formal education with additional relevant work experience, and vice versa. *Id.*

VII. CLAIM CONSTRUCTION

In an IPR, claim terms should be construed according to the *Phillips* standard. *See Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); *see also* 37 C.F.R. § 42.100(b). The Board need only construe terms to the extent necessary to resolve a controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

For purposes of this proceeding only, Petitioners submit constructions for the following terms.[1] Petitioners do not believe that construction of any other term is

[1] While Petitioners propose these constructions for purposes of this proceeding, Petitioners reserve their right to revise or amend these constructions in any other action or forum. *Western Digital Corp. v. Spex Techs., Inc.*, IPR2018-00084, Paper 14 at 11 (PTAB April 25, 2018) ("37 C.F.R. § 104(b)(3) does not require [a p]etitioner to express its subjective agreement regarding correctness of its proffered claim constructions or to take ownership of those constructions"). Petitioners also reserve the right to challenge the validity of the challenged claims under 35 U.S.C. § 112 in another other action or forum. *See Target Corp. v. Proxicom Wireless, LLC*, IPR2020- 00904, Paper 11 at 12-13 (PTAB Nov. 10, 2020) (instituting IPR in view

necessary.

A. "Optimal"

Claims 1 and 32 recite the term "optimal." In the co-pending litigation, the Court held that "optimal" had a plain and ordinary meaning. Ex-1008 at 42-45. Petitioners have applied that construction for purposes of this Petition.

B. "LBA"

The term "LBA," as recited in independent claims 1 and 32, should be construed as "an address that is part of a logical addressing system used by a host." This construction is consistent with the specification of the '740 Patent, which states that "[t]he term 'LBA,' which may also be referred to herein as a logical block address, is intended to represent an address that is part of a logical addressing system . . . used by a host." Ex-1001 at 6:37-40; Ex-1003, ¶¶ 62-65. Petitioners thus apply this construction for purposes of this Petition.

C. "PBA"

The term "PBA," as recited in independent claims 1 and 32, should be construed as a "unique addressable physical memory location." This construction is

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of indefiniteness arguments in parallel lawsuit, explaining that this kind of "alternative pleading before a district court is common practice, especially where it concerns issues outside the scope of *inter partes* review").

consistent with the specification of the ’740 Patent, which states that the memory store, as illustrated in Figure 2 of the patent, has a set of PBA fields “disposed to represent a unique addressable physical memory location, named ‘PBA.’” Ex-1001 at 5:30-33; Ex-1003, ¶¶ 66-70. Petitioners thus apply this construction for purposes of this Petition.

D. “FDE” and “FDE Identifier”

The term “FDE” is recited in dependent claim 15, while the related term “FDE Identifier” (or “FDE identifiers”) is recited in dependent claims 9-11 and 13. This term “FDE” should be construed to mean “a component that controls multiple flash devices and facilitates high speed data transfers to and from a group of flash memory devices.” Similarly, “FDE Identifier” should be construed to mean “an identifier for a component that controls multiple flash devices and facilitates high speed data transfers to and from a group of flash memory devices.”

These proposed constructions are consistent with the specification of the ’740 Patent, which states that “direct memory access engines may be also herein referred to as FDEs.” Ex-1001 at 3:27-35. Moreover, an FDE represents “a device that is capable of controlling a flash memory device and performing DMA operations on the flash memory device in response to commands generated by storage device 2 through storage device controller.” *Id*. at 3:35-39. Likewise, the ’098 Patent, to which the ’740 Patent claims priority, states that the disclosed systems “comprise[]

a number of Flash DMA, or Direct Memory Access, Engines (FDEs)." Ex-1010 at 3:24-25. The '098 Patent further explains that "[a] Flash DMA Engine (FDE) is basically an intelligent DMA controller that facilitates high speed data transfers to/from a group of flash memory devices" and "control[s] multiple flash devices across a set of flash buses." *Id.* at 3:25-28, 42-44. Petitioners thus apply this construction for purposes of this Petition. Ex-1003 ¶¶ 71-74.

E. "group identifier"

The term "group identifier," as recited in dependent claims 9-11 and 14, should be construed to mean "an identifier for identifying one flash memory device from another flash memory device from a set of flash devices that are controlled by the same FDE." The specification of the '740 Patent defines the term as "an identifier for identifying one flash memory device from another flash memory device from a set of flash devices that are controlled by the same FDE." Ex-1001 at 6:2-6, 6:11-15. The '098 Patent, to which the '740 Patent claims priority, further explains that "group interleaving performs parallel operations by having a specific FDE send multiple commands to different flash devices it controls." Ex-1010 at 4:17-20. Petitioners thus apply this construction for purposes of this Petition. Ex-1003, ¶¶ 75-78.

VIII. OVERVIEW OF THE PRIOR ART

A. Prior Art References

1. Overview of Sukegawa

Sukegawa discloses a semiconductor memory system that uses flash memory to store data. Sukegawa explains that prior art memory systems, which typically used magnetic disk drives to store data and information, suffered from several disadvantages, including their size and susceptibility to damage from physical impact. Ex-1005 at 1:15-20; 1:59-61. Sukegawa therefore discusses the need for memory systems that can utilize semiconductor memory while still employing existing host drive accessing schemes. *Id.* at 4:36-47.

Sukegawa's solution is a semiconductor memory system that converts read and write requests from a host, using logical addresses, to "real memory addresses"—or unique addressable physical memory locations—in a flash EEPROM memory store. *Id.* at 4:51-5:13, 9:14-19, 10:14-19. More particularly, Sukegawa discloses an "address conversion table," or mapping table, which is used by an access controller to associate logical addresses from a host with physical addresses in the memory store during a read or write operation. *Id.* at 7:26-40; 7:46-51; 8:17-19. Sukegawa's **access controller**, which comprises the **address conversion table** and which converts logical addresses from the host to real memory

addresses for flash EEPROM chips in the **memory store**, is shown below in annotated Figure 6:

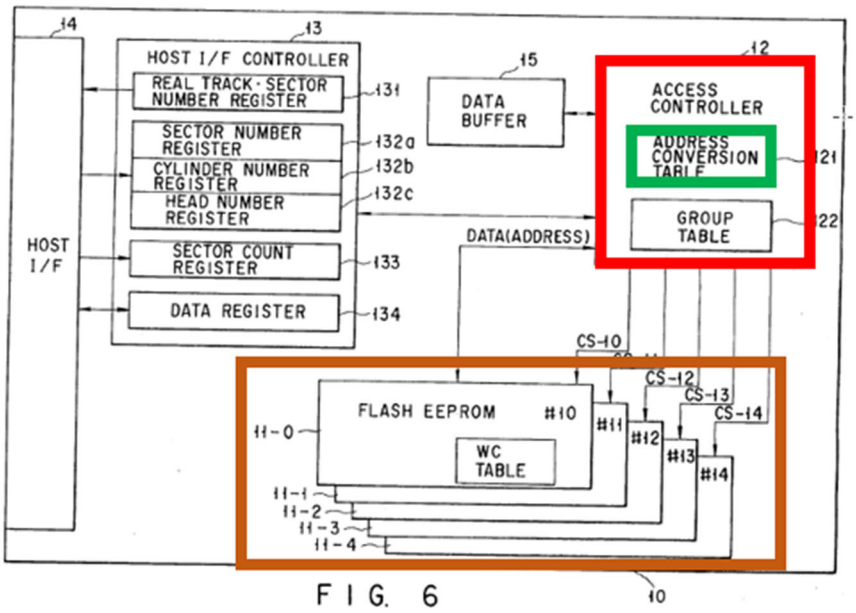


FIG. 6

Sukegawa discloses that host addresses are comprised of "sectors," which are part of a "logical address designated by a host system." *Id*. at 4:67-5:4. As discussed below, Sukegawa's "sectors" are "LBAs" pursuant to Petitioners' proposed construction of the term. *Infra*, § IX.A.1.b. The LBA's are grouped into sets of consecutive LBAs and may, for example, comprise a first set having eight consecutive LBAs, a second set having eight consecutive LBAs, etc. Ex-1005 at 8:66-9:8, 8:36-39, Fig. 11. Sukegawa further teaches that the address conversion table maps the LBAs to "real memory addresses," or PBAs, which correspond to physical memory locations in the flash EEPROM. Various access parameters,

including identifiers for chip numbers and block numbers, are used in the address conversion table to represent physical memory locations. *Id.* at 9:14-21.

As shown below in annotated Figure 11 from Sukegawa, a **first set of LBAs** is associated with a **first PBA**, and a **second set of LBAs** is associated with a **second PBA**. Figure 11 also demonstrates that each LBA set is comprised of eight **consecutive LBAs**:

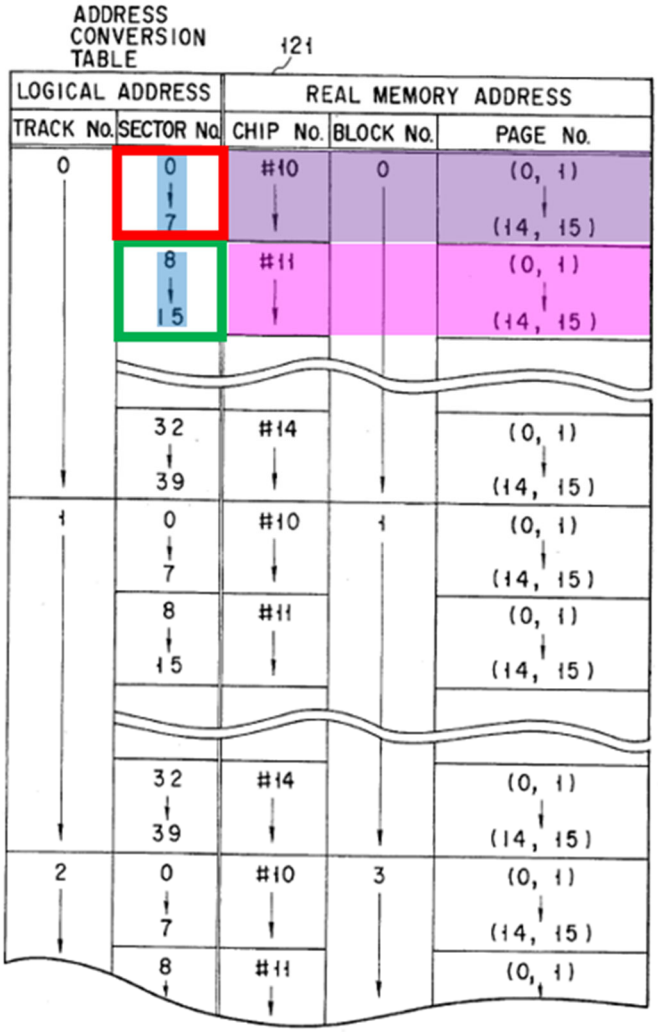


FIG. 11

According to Sukegawa, the address conversion table improves performance by "enabling parallel write operations" on different physical memory sectors in response to a request from a host. *Id.* at 8:39-43, 10:20-21, 12:36-41, 4:51-57.

2. Overview of Bennett

Bennett discloses a high-capacity and high-performance non-volatile memory system that can conduct memory operations in large blocks. Ex-1007 at 4:4-8. Bennett explains that prior art memory devices typically comprise one or more memory chips that include an array of memory cells for data storage. *Id.* at 2:22-26. Bennett further explains that when data needs to be updated in a physical memory location, an entire physical block containing the physical location first needs to be erased and then rewritten, as it is not possible to erase and rewrite only portions of the block. *Id.* at 3:4-14. However, this process is not efficient, can render existing blocks obsolete, and can cause premature aging of the memory. *Id.* at 3:65-4:1.

To address these problems, Bennett teaches a table for mapping between logical groups and physical groups. *Id.* at 23:61-64, 7:9-11, 9:55-58. Bennett's Group Address Table, or "GAT," provides "a list of [physical] metablock addresses for all logical groups of host data in the memory system." *Id.* at 24:19-21. The GAT, which is shown below in Figure 17B from Bennett, "contains one entry for each logical group, ordered sequentially according to logical address." *Id.* at 24:21-22, 25:1-3, 9:55-58.

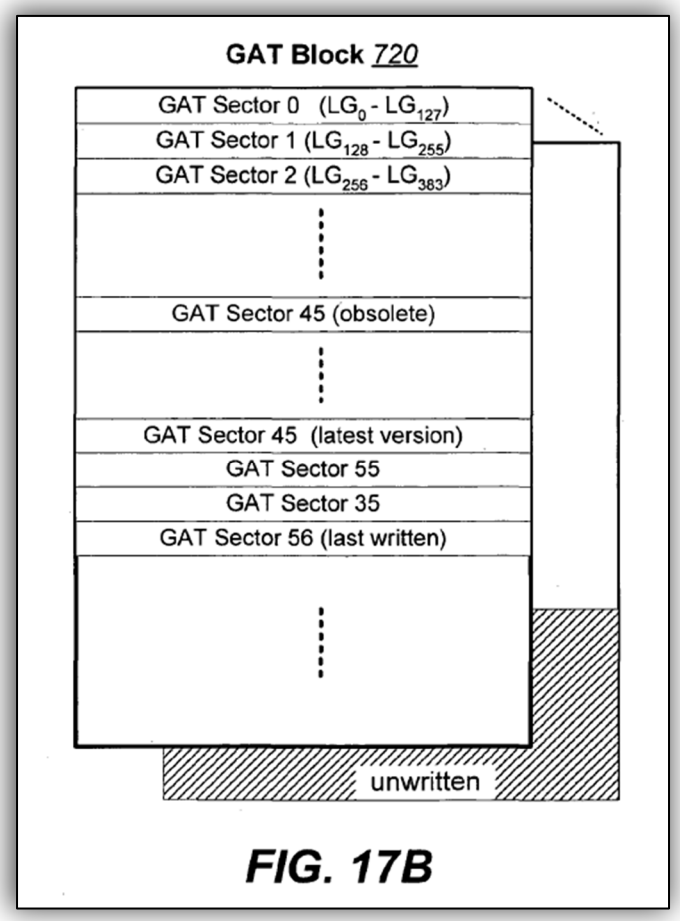
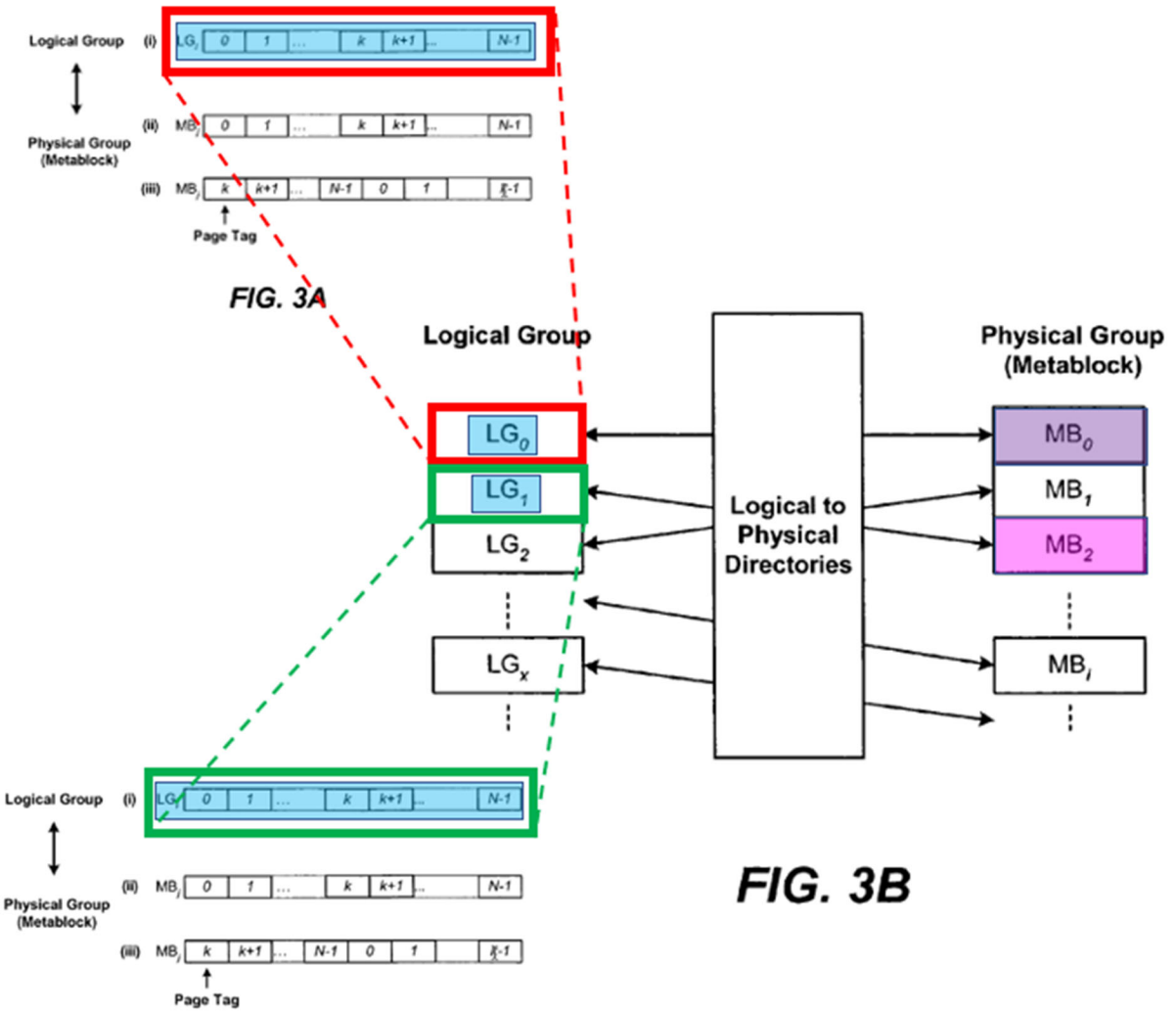


FIG. 17B

Additionally, Bennett teaches that each logical group in the GAT comprises a set of logical sectors that "are in contiguous logical order 0, 1, . . . , N-1." *Id.* at 7:13-15, 6:61-65. These sets of contiguous logical sectors, or "LBAs," are mapped to unique physical "metablocks"—i.e., "PBAs," as explained below—and the "mapping information is maintained in a set of logical to physical directories." *Id.* at 7:38-44; 23:61-64.

The following annotated figures (Figures 3A and 3B of Bennett) show a **first logical field** (LG_0,) comprising **consecutive LBAs** associated with a **first PBA**

(MB_0), and a **second logical field** (LG_1) comprising **consecutive LBAs** associated with a **second PBA** (MB_2), as taught be Bennett:



According to Bennett, the disclosed mapping table optimizes memory operations by enabling parallel memory operations. "In order to maximize programming speed and erase speed, parallelism is exploited as much as possible by arranging for multiple pages of information . . . to be programmed in parallel, and

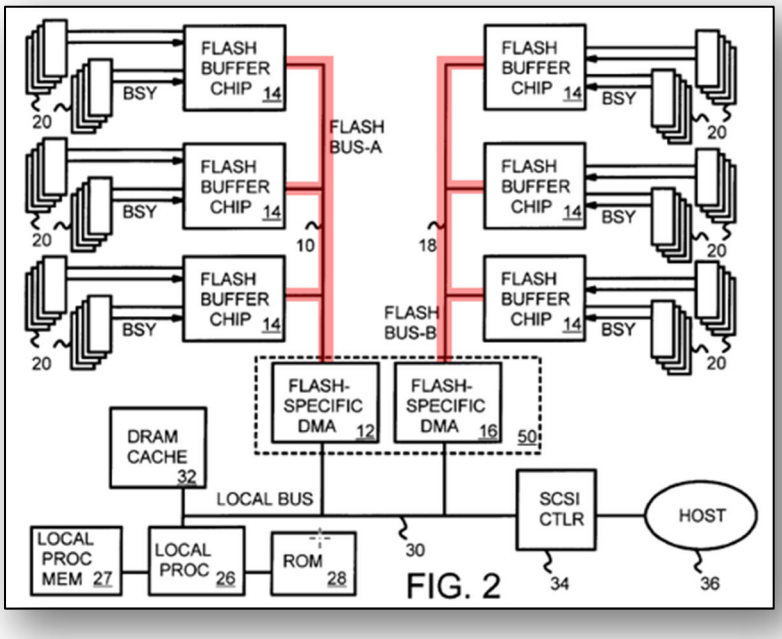
for multiple MEUs [minimum erasable units] to be erased in parallel." Ex-1007 at 8:26-30, 2:57-59. Bennett's mapping table therefore provides a more "efficient use of system resources" by allowing "multiple logical groups to be updated concurrently," which "increases efficiency and reduces overhead." *Id.* at 4:50-52.

3. Overview of Bruce

Bruce discloses a non-volatile memory storage system and expansion of flash memory systems. Ex-1006 at 1:18-20. According to Bruce, prior flash memory systems suffered from various drawbacks, including that expansion was hampered by issues such as rigid bus architectures, and that, while direct-memory access (DMA) was known and used to facilitate data transfers, it was not well-suited to transfer addresses and commands required by flash memory chips. *Id*. at 1:39-43, 2:22-30. Bruce therefore purports to identify a need for a modified DMA controller that allows commands and addresses to be input over shared data/address/command pins, as well as a need for a flash memory system allowing greater expansion and parallel flash operations across all flash chips. *Id.* at 2:40-46.

Accordingly, Bruce teaches flash-specific DMA controllers coupled to flash buses that have shared lines for transmitting the sequence of command bytes and address bytes from the DMA controller. *Id.* at 2:56-59. Bruce's flash buses are each connected to a flash-specific DMA controller, as well as to an array of flash memory chips (through a flash buffer chip). *Id.* at 2:66-3:1. As shown below in annotated

Figure 2 from Bruce, the flash buses are uniquely identified as "**flash bus 10/Flash Bus-A**" and "**flash bus 18/Flash Bus-B**":



Bruce's DMA controllers also have a plurality of state machines, which each control one of four banks of flash-memory chips and allow data to be "interleaved among the four banks for each flash buffer chip, and also interleaved among chips connected to the two flash busses." *Id.*, Abstract, 11:23-25, 6:57-60, 13:32-35. The state machines, identified as "**Bank0 SM**," "**Bank1 SM**," "**Bank2 SM**," and "**Bank3 SM**," are shown below in annotated Figure 3 from Bruce:

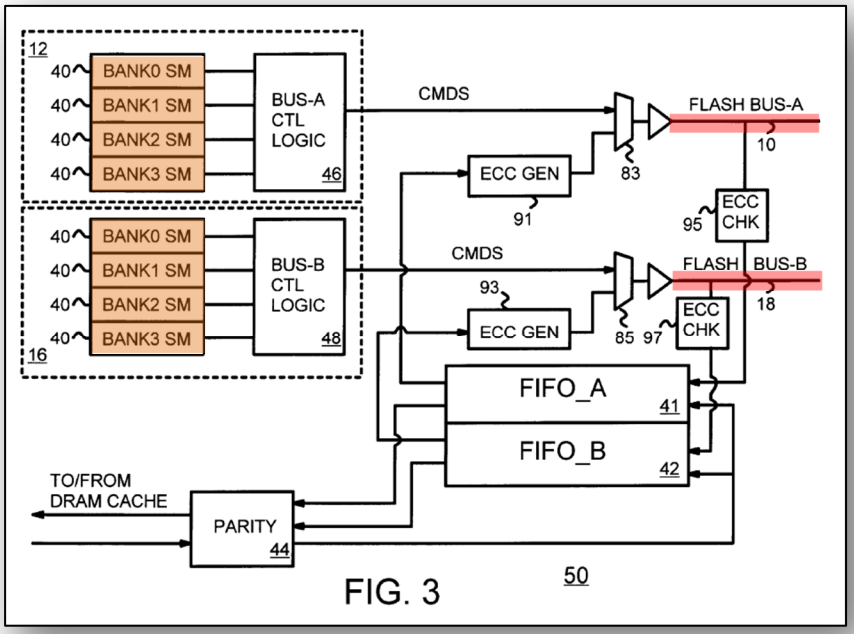


FIG. 3

Bruce also discloses that each individual bank of flash-memory chips "can be separately accessed, allowing many flash operations to be performed in parallel." Ex-1006 at 5:21-23, 6:55-57. The flash memory chips are "uniquely addressed," and therefore the DMA controller sends specific device addresses for each chip to the flash buffer, which then decodes the addresses into chip selects. *Id.* at 7:62-67, 8:46-49, 10:17-19. These unique addresses allow one flash memory device to be identified from another flash memory device from a set of flash devices that are controlled by the same DMA state machine.

Like Sukegawa and Bennett, Bruce explains that it provides "[a] high-performance flash-memory system performing flash operations in parallel … even

when expansion flash chips are added," *id.* at 2:44-46, 13:32-35, which, in turn, improves performance of the memory system. *Id.* at 13:40-44, 5:44-50.

B. A POSITA Would Have Been Motivated to Combine the Prior Art

1. It Would Have Been Obvious to Combine Sukegawa and Bruce

As explained in the attached declaration of Dr. R. Jacob Baker, a POSITA would have been motivated to combine Bruce with Sukegawa. Ex-1003, ¶ 116. These references both recognize disadvantages related to spinning disk drives, as well as the benefits of solid-state non-volatile storage. Ex-1005 at 1:21-28, 52-58; Ex-1006, 1:35-42; Ex-1003, ¶ 117. They also recognize that existing solid-state non-volatile storage suffered from drawbacks related to data management, host addressing schemes, and the erasure and programming of information. Ex-1005 at 4:26-57; Ex-1006, 1:45-52; Ex-1003, ¶ 117. The references are both directed to resolving these issues and improving the function of solid-state non-volatile memory to optimize memory performance. Ex-1005, 4:51-6:5; Ex-1006, 2:40-3:18; Ex-1003, ¶ 117. For example, both references disclose the use of interleaving and parallel memory operations to optimize memory operations. *See* Ex-1005 at 4:51-57, 10:20-21, 5:8-13; Ex-1006, 2:44-46, 13:32-35, 13:45-46; Ex-1003, ¶ 118.

Because Sukegawa and Bruce are from the same field and have interrelated teachings, a POSITA would have been motivated to combine them. Ex-1003, ¶ 119.

Specifically, a POSITA would have been motivated to incorporate Bruce's physical access parameters into Sukegawa's mapping table, which already contains access parameters, because doing so would have allowed Sukegawa's mapping table to utilize the benefits of solid-state, non-volatile memory connected to a host system while maintaining and enhancing parallel memory operations. *Id.*

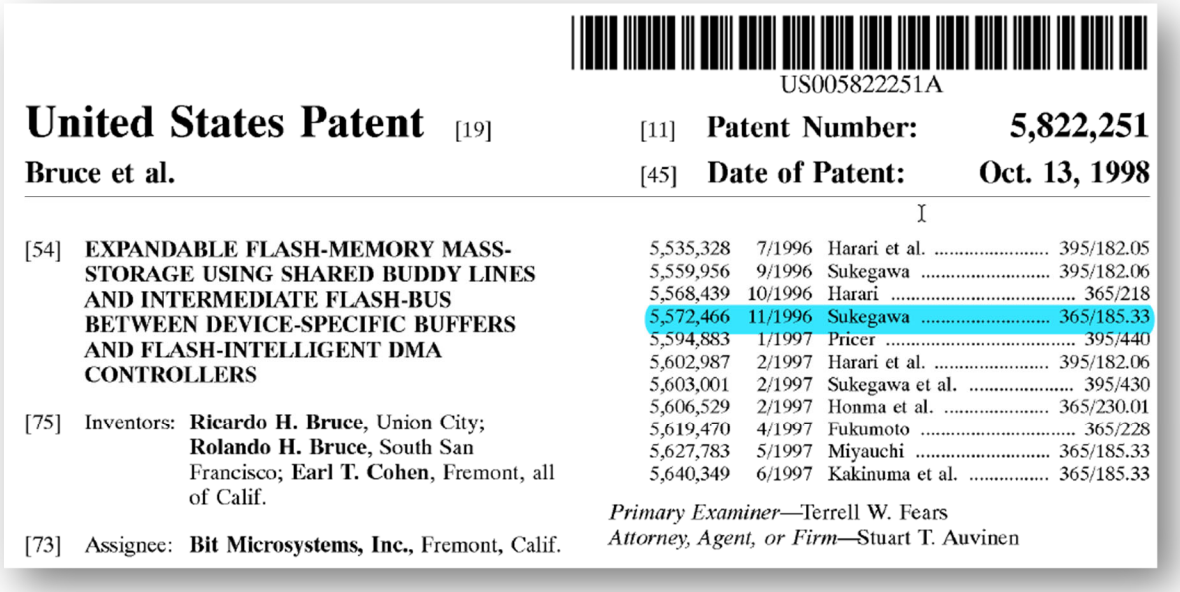
The combination of these references also involves combining well-known prior art elements and techniques, according to known methods, to yield the predictable result of a mapping table that accounts for an expandable solid state storage device. *Id.,* ¶ 120. Indeed, Sukegawa teaches a mapping table comprising fields for access parameters, and Bruce teaches certain types of access parameters that can be used in such a table. *Id.* Moreover, Bruce's teachings rely on well-known techniques that can be readily applied to expand Sukegawa's mapping table. *Id.*

Further, the combination of the references would have been straightforward and predictable, requiring minimal modification. *Id.*, ¶ 121. For example, incorporating Bruce's additional access parameters into Sukegawa's mapping table would require only the modification of adding additional physical access parameters to account for limited additional hardware in an expandable system, such as distinct buses, DMA engines, and flash chip groups. *Id.*

Because of the very minor changes required to modify Sukegawa's mapping table with Bruce's teachings, a POSITA would have had a reasonable expectation

that combining the references in this manner would have been successful. *Id.*, ¶ 122. In combining the references, a POSITA would further have understood that the ability to receive commands over the same type of host interface would have been maintained, and that no external change or new host command and/or interface design would have been required. *Id.*

Further underscoring the motivation for a POSITA to combine these references is the fact that Sukegawa is explicitly referenced on the face of Bruce:



US005822251A

United States Patent [19]

Bruce et al.

[11] **Patent Number: 5,822,251**

[45] **Date of Patent: Oct. 13, 1998**

[54] **EXPANDABLE FLASH-MEMORY MASS-STORAGE USING SHARED BUDDY LINES AND INTERMEDIATE FLASH-BUS BETWEEN DEVICE-SPECIFIC BUFFERS AND FLASH-INTELLIGENT DMA CONTROLLERS**

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[73] Assignee: **Bit Microsystems, Inc.**, Fremont, Calif.

5,535,328	7/1996	Harari et al.	395/182.05
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5,594,883	1/1997	Pricer	395/440
5,602,987	2/1997	Harari et al.	395/182.06
5,603,001	2/1997	Sukegawa et al.	395/430
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5,640,349	6/1997	Kakinuma et al.	365/185.33

Primary Examiner—Terrell W. Fears
Attorney, Agent, or Firm—Stuart T. Auvinen

Ex-1006; *see also* Ex-1003, ¶ 123. Moreover, Bruce is a continuation-in-part of U.S. Patent No. 6,000,006 ("the '006 Patent"), which, like Sukegawa, is directed to a re-mapping table having "a plurality of entries," each with "a physical-block-address field that contains a physical block address of a block in an array of flash memory

devices." Ex-1009 at 2:62-67; Ex-1003, ¶ 124. Indeed, both Sukegawa and the '006 Patent are directed to resolving the same issues in a similar manner. *See* Ex-1005, 4:59-63, 3:27-34, 4:14-19; Ex-1009 at 2:53-59, 5:48-52; Ex-1003, ¶ 125.

For at least these reasons, a POSITA would have been motivated to combine the teachings of Sukegawa and Bruce, including the specific combinations described below, rendering the combination obvious. Ex-1003, ¶ 126.

2. It Would Have Been Obvious to Combine Bennett and Bruce

A POSITA would have also been motivated to combine Bennett and Bruce. Ex-1003, ¶ 230. These references both recognize disadvantages related to spinning disk drives, as well as the benefits of solid-state non-volatile storage. Ex-1007 at 1:20-34; Ex-1006 at 1:35-42; Ex-1003, ¶ 231. They also recognize that existing solid-state non-volatile storage suffered from drawbacks related to data management, host addressing schemes, and the erasure and programming of information. Ex-1007 at 2:57-4:8; Ex-1006 at 1:45-52; Ex-1003, ¶ 231. The references are both directed to resolving these issues and improving the function of solid-state non-volatile memory to optimize memory performance. Ex-1007 at 4:4-8; Ex-1006, 2:40-3:18; Ex-1003, ¶ 231. For example, both references disclose the use of interleaving and parallel memory operations as a way to optimize memory operations. *See* Ex-1007 at 8:26-30, 2:57-59, 4:50-52; Ex-1006 at 2:44-46, 13:32-35, 13:45-46. Ex-1003, ¶ 232.

Because Bennett and Bruce are from the same field and have interrelated teachings, a POSITA would have been motivated to combine them. Ex-1003, ¶ 233. Specifically, a POSITA would have been motivated to incorporate Bruce's physical access parameters into Bennett's mapping table because doing so would have allowed Bennett's mapping table to cover an expandable solid state storage system with parallel memory access. *Id*.

Such a combination of the references would further involve combining well-known prior art elements and techniques, according to known methods, to yield the predictable result of a mapping table that accounts for an expandable solid state storage device. *Id.*, ¶ 234. Indeed, Bennett teaches a table comprising fields for access parameters, and Bruce teaches the types of access parameters that can be used in such a table. *Id.* Moreover, Bruce's teachings rely on well-known techniques that can be readily applied to improve Bennett's mapping table. *Id.*

The combination of the references would have been straightforward and predictable, requiring minimal modification. *Id.*, ¶ 235. For example, incorporating Bruce's additional access parameters into Bennett's mapping table would require only the modification of adding additional physical access parameters to account for limited additional hardware in an expandable system, such as distinct buses, DMA engines, and flash chip groups. *Id.*

Because of the very minor changes required to modify Bennett's mapping

table with Bruce's teachings, a POSITA would have had a reasonable expectation that combining the references in this manner would have been successful. *Id.*, ¶ 236. In combining the references, a POSITA would further have understood that the ability to receive commands over the same type of host interface would have been maintained and that no external change or new host command and/or interface design would have been required. *Id.*

Moreover, as discussed above, Bruce is a continuation-in-part of the '006 Patent. Like Bennett, the '006 Patent is directed to a re-mapping table having "a plurality of entries," each with "a physical-block-address field that contains a physical block address of a block in an array of flash memory devices." Ex-1009 at 2:62-67; Ex-1003, ¶ 237. Indeed, both Bennett and the '006 Patent are directed to resolving the same issues in a similar manner. *See* Ex-1007 at 3:3-17; Ex-1009 at 2:53-59; Ex-1003, ¶ 238.

For at least these reasons, a POSITA would have found it obvious and been motivated to combine the teachings of Bennett and Bruce, including the specific combinations described below. *Id.*, ¶ 239.

IX. THE CHALLENGED CLAIMS ARE UNPATENTABLE AND SHOULD BE CANCELLED

A. Ground 1: Claims 1, 32 and 34 are Anticipated by Sukegawa

1. Sukegawa Anticipates Claim 1

a. [Claim 1 Pre]: "A mapping table for optimizing memory operations performed by an electronic storage device in response to receiving an I/O transaction request initiated by a host, said mapping table comprising:"

To the extent the preamble is limiting, Sukegawa discloses an "address conversion table' that converts logical addresses specified by a host into "real memory addresses" in flash EEPROM chips. Ex-1005 at 10:14-19, 7:48-52, Fig. 11. Sukegawa's address conversion table is thus a "mapping table." Ex-1003, ¶¶ 96-97.

Sukegawa's mapping table also enables optimized memory operations by allowing flash EEPROMS to be "accessed parallely." Ex-1005 at 12:35-40, 4:51-57, 5:8-13, 10:10-13, 10:20-21; Ex-1003, ¶ 98.[2] The district court's claim construction order also identifies "contiguous LBA sets, adjacent LBA sets, [and] adjacent PBA's differing by at least one parameter" as examples of optimization. Ex-1008 at 30; Ex-

[2] The '740 patent states that parallel memory operations are one example of "optimized memory operations." *See, e.g.*, Ex-1001 at 2:14-21 ("***These optimizing memory operations include*** increasing the likelihood that . . . the operational load imposed on the storage devices by these memory operations will be optimally distributed across different storage device resources, ***such as by interleaving or parallel memory operations***") (emphasis added).

1003, ¶ 99. Sukegawa teaches each of these examples. *Infra* §§ IX.A.1.b, IX.A.1.c; Ex-1003, ¶ 99.

Sukegawa also states that these optimized memory operations are performed in response to receiving an I/O transaction request initiated by a host, explaining that the controller accesses memory for read and write transactions "in response to [a] disk access request supplied from a host CPU." Ex-1005 at 7:28-32, 11:3-6; Ex-1003, ¶ 100.

b. [Claim 1a]: "a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs;"

Sukegawa discloses "sectors" that are part of "a logical address designated by a host system." Ex-1005 at 4:67-5:4, 9:14-19, 4:30-35, 8:48-49. These logical sectors thus constitute LBAs, or addresses that are part of a logical addressing system used by a host, under Petitioners' proposed construction. *Supra*, § VII.B; Ex-1003, ¶ 102.

Sukegawa also discloses logical fields that are disposed to represent a plurality of LBA sets, including, for example, a first LBA set comprising eight consecutive LBAs from 0-7, a second LBA set comprising eight consecutive LBAs from 8-15, etc. Ex-1005 at 8:66-9:8, 8:36-39; Ex-1003, ¶ 103.

Sukegawa's **first logical field** and **second logical field**, each of which are disposed to represent **a set of consecutive LBAs**, are shown below:

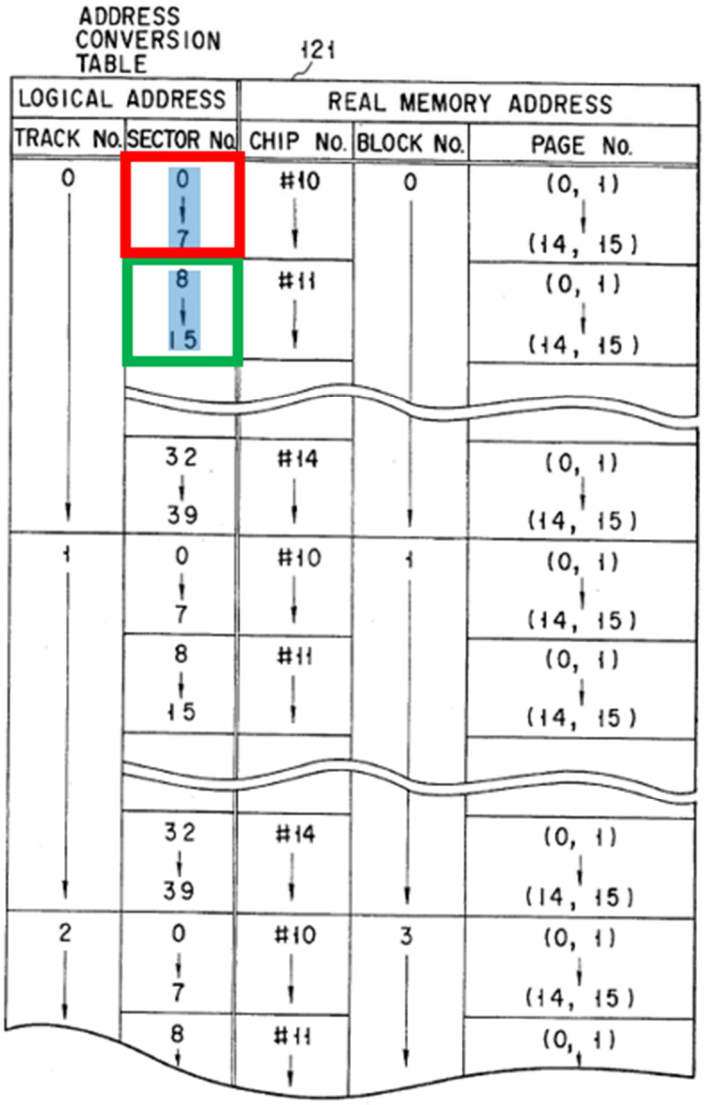


FIG. 11

Ex-1003, ¶ 104.

c. [Claim 1b]: "a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first

set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs; and"

Sukegawa discloses "real memory addresses," which correspond to physical memory locations illustrated by identifiers for a chip number, block number, and page number. Ex-1005 at 9:14-21, 4:30-35, Fig. 11; Ex-1003, ¶ 106. Each of these "real memory addresses" thus constitute a PBA, or a unique addressable physical memory location, pursuant to Petitioner's proposed construction. *Supra* § VII.C; Ex-1003, ¶ 106.

Sukegawa also discloses sets of PBA fields disposed for representing a set of PBAs. For example, Sukegawa teaches fields such as "Chip No." and "Block No." that represent a set of PBAs (real memory addresses). Ex-1005 at 9:14-32; 7:5-45 Sukegawa also teaches identifiers for these fields (e.g., Chip No. 10 and Block No. 0 for the first PBA), which exemplify access parameters representing the physical location of the PBA. *Id.*; Ex-1003, ¶ 107.

In addition, Sukegawa discloses that the address conversion table is disposed to associate the first and second LBA sets with first and second PBA, explaining that the table provides "a correspondence between the logical addresses … specified by the host CPU and the real memory addresses." Ex-1005 at 9:14-19, 10:14-19, 5:46-

51; Ex-1003, ¶ 108.

Annotated Figure 11, below, shows a set of **PBA fields** that includes a first and second PBA field (e.g., chip number and block number), which represent a **first PBA** and a **second PBA**. Annotated Figure 11 also illustrates the **first logical field** associated with the **first PBA**, and the **second logical field** associated with the **second PBA**.

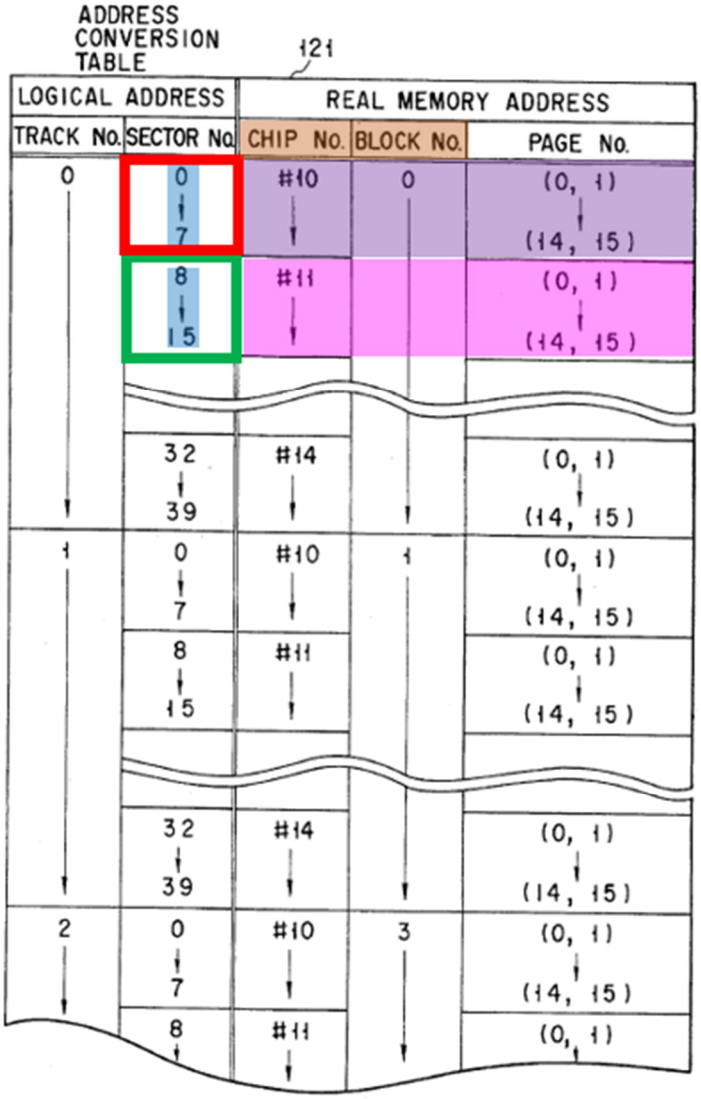


FIG. 11

Ex-1003, ¶ 109.

d. [Claim 1c]: "wherein, in response to receiving the I/O transaction request, said mapping table causes the electronic storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first

and second LBA sets."

Sukegawa teaches that the mapping table causes an electronic storage device to perform optimized memory operations by "enabling parallel write operations" in response to a request from a host. Ex-1005 at 8:39-43; 10:14-21; 4:51-57. As explained above, parallel memory operations are an example of optimized memory operations. *Supra* Footnote 2; Ex-1003, ¶¶ 111-112.

The district court's claim construction order also identifies "contiguous LBA sets, adjacent LBA sets, [and] adjacent PBA's differing by at least one parameter" as examples of optimization. Ex-1008 at 30; Ex-1003, ¶ 113. As explained above, Sukegawa teaches each of these examples as well. *Supra* §§ IX.A.1.b, IX.A.1.c.

Sukegawa further explains that this optimization occurs in response to receiving an I/O transaction request, explaining that the controller accesses memory for read and write transactions "in response to an [sic] disk access request supplied from a host CPU." Ex.-1005 at 7:28-32; *see also id.* at 11:3-6 (explaining that "[w]hen a write access request for a specified address (logical address) occurs, the block corresponding to the specified address is accessed on the basis of the address conversion table 121"); Ex-1003, ¶ 114.

2. Sukegawa Anticipates Claim 32

a. [Claim 32 Pre]: "An electronic storage device that includes a memory system that uses a memory table for increasing the likelihood that an operational load

imposed on the storage apparatus during the processing of an I/O transaction request will be optimally distributed across storage device resources, said I/O transaction request received by said storage device from a requesting host, said electronic storage device comprising:"

Sukegawa teaches an electronic storage device by way of a semiconductor disk drive. Ex-1005 at 7:6-13, 7:26-32; Ex-1003, ¶ 173. Sukegawa also discloses that this electronic storage device comprises a memory system, which the '740 patent describes as comprising a controller and mapping table. Ex-1001 at 3:20-31. In particular, Sukegawa discloses an access controller, which "provides access control of the flash EEPROM chips." Ex-1005 at 7:26-31, 7:46-51. Sukegawa further discloses that the access controller includes and is disposed to use a mapping table—or address conversion table— to select a flash EEPROM and "read[] and write[] data from and into the selected EEPROM." *Id.*, 8:17-19, 7:35-40. The access controller is thus a memory system. Ex-1003, ¶ 174.

The electronic device including an **access controller**, which comprises the **address conversion table** and is coupled to the **memory store**, is shown below:

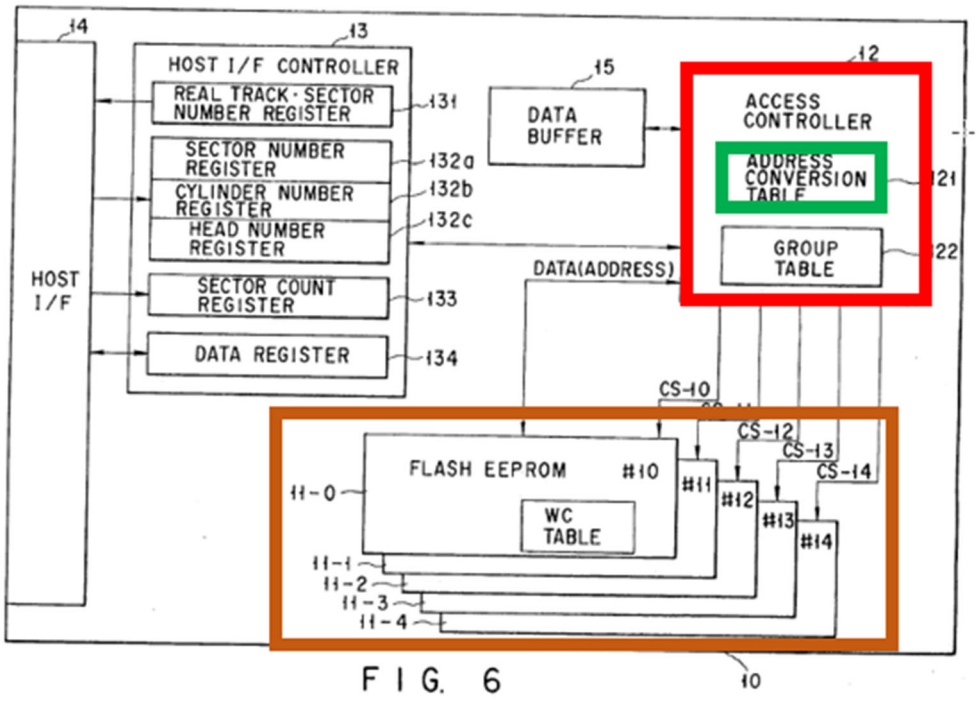


FIG. 6

Ex-1003, ¶ 175.

Sukegawa also discloses that the electronic device uses a memory table—or "address conversion table"—that converts logical addresses from a host into "real memory addresses" in flash EEPROM chips. Ex-1005 at 10:14-19, 7:48-52, Fig. 11; Ex-1003, ¶ 176. Sukegawa's memory table is shown below:

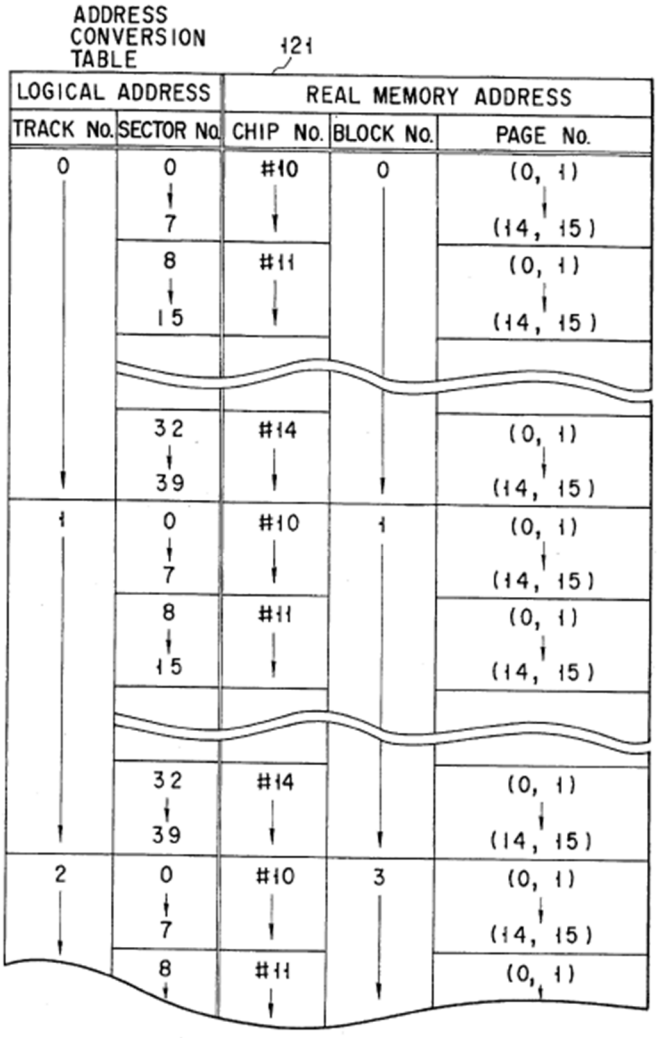


FIG. 11

Id.

In addition, Sukegawa discloses that the memory table increases the likelihood that an operational load imposed on the storage apparatus will be optimally distributed across storage device resources by enabling flash EEPROMS to be "accessed parallelly." Ex-1005 at 12:35-40, 4:51-57, 5:8-13, 10:10-13, 10:20-21; Ex-1003, ¶ 177. As explained above, parallel memory operations are an example

of optimized memory operations. *Supra* Footnote 2; Ex-1003, ¶ 177. Sukegawa also discloses "contiguous LBA sets, adjacent LBA sets, [and] adjacent PBA's differing by at least one parameter," *infra* §§ IX.A.2.b, IX.A.2.c, IX.A.2.e, which the district court has identified as examples of optimized memory operations. Ex-1008 at 30; Ex-1003, ¶ 177.

Sukegawa also demonstrates that these optimized operations are performed in response to an I/O transaction request from a host, noting that the controller accesses memory for read and write transactions "in response to an [sic] disk access request supplied from a host CPU." *Id*. at 7:28-32; 11:3-6; Ex-1003, ¶ 178.

b. [Claim 32a]: "a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA, said first and second LBA sets including respective sets of consecutive LBAs;"

Sukegawa discloses logical "sectors" that are part of "a logical address designated by a host system." Ex-1005 at 4:67-5:4, 9:14-19, 4:30-35. These logical sectors thus constitute LBAs, or addresses that are part of a logical addressing system used by a host, under Petitioners' proposed construction of the term. *Supra* § VII.B; Ex-1003, ¶ 180.

Sukegawa also teaches that the mapping table has first and second LBA sets that include respective sets of consecutive LBAs. Ex-1003, ¶ 181. For example, Sukegawa discloses a first LBA set comprising eight consecutive LBAs from 0-7, a

second LBA set comprising eight consecutive LBAs from 8-15, etc. Ex-1005 at 8:66-9:8, 8:36-39; Ex-1003, ¶ 181.

In addition, Sukegawa discloses "real memory addresses" that correspond to physical memory locations illustrated by identifiers for chip number, block numbers, and page numbers. Ex-1005 at 9:14-21, 4:30-35, Fig. 11, Claim 9; Ex-1003, ¶ 182. Each of these "real memory addresses" thus constitute a PBA, or a unique addressable physical memory location, pursuant to Petitioner's proposed construction. *Supra* § VII.C; Ex-1003, ¶ 182.

Sukegawa further teaches that first and second LBA sets are mapped to first and second PBAs, respectively. Ex-1005, 9:14-19, 10:14-19, 5:46-51; Ex-1003, ¶ 183. For example, annotated Figure 11, below, illustrates Sukegawa's mapping table, which maps a **first LBA set** to a **first PBA** and a **second LBA set** to a **second PBA**, in which each of the LBA sets include sets of **consecutive LBAs**:

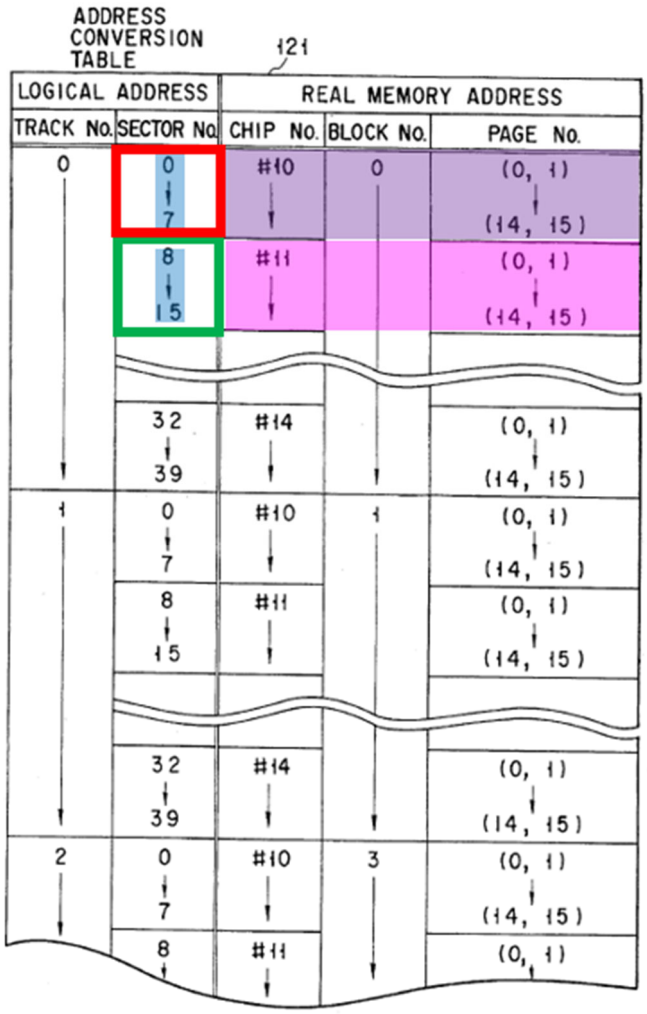


FIG. 11

Ex-1003, ¶ 184.

c. [Claim 32b]: "a memory store that includes a set of flash devices, said set of flash devices includes a first physical memory location and a second physical memory location that are addressable by said first and second PBAs respectively;"

Sukegawa's semiconductor disk drive includes a memory store comprising a plurality of flash EEPROM chips "as data storage." Ex-1005 at 7:6-13; Ex-1003, ¶

186. These flash devices include physical memory locations addressable by PBAs. Specifically, each of Sukegawa's PBAs addresses a specific location within a memory store, as represented by a block number and a page number. Ex-1005 at 9:14-21, Fig. 11; Ex-1003, ¶ 187.

Annotated Figures 6 and 11, below, illustrate Sukegawa's mapping table and its relationship to the **memory store**, demonstrating that a first physical location is represented by **a first PBA**, and a second physical location is represented by a **second PBA**:

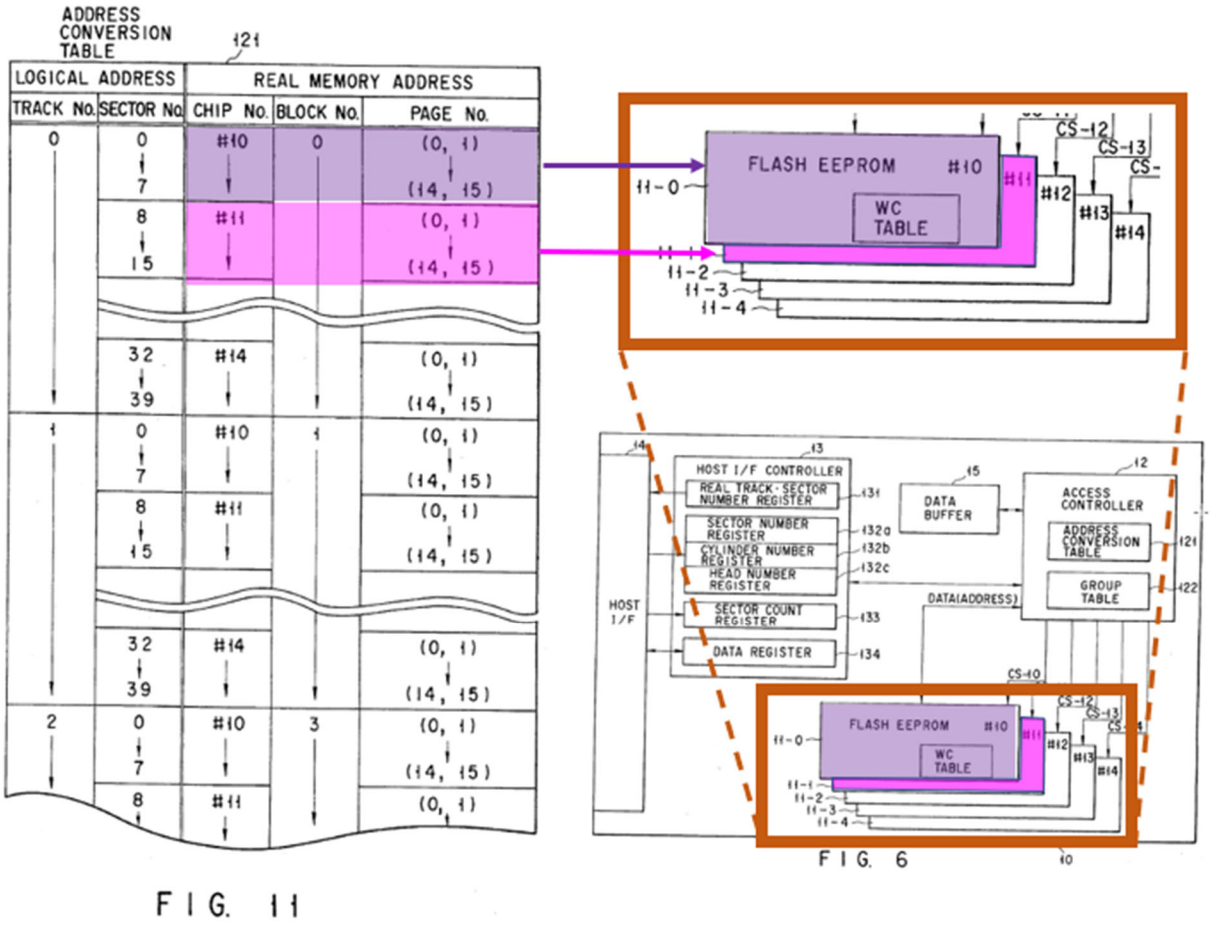


FIG. 11

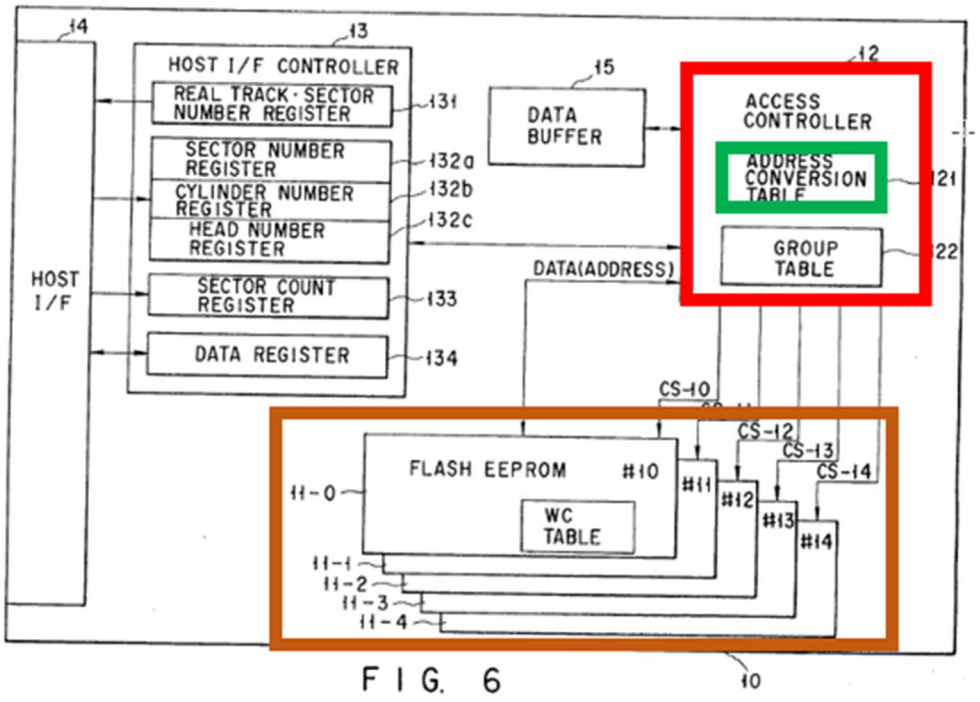
FIG. 6

Ex-1003, ¶ 188.

d. [Claim 32c]: "a memory system coupled to said memory store and disposed to use said mapping table during a memory operation;"

As explained above, Sukegawa discloses a memory system, which the '740 patent describes as comprising a controller and mapping table. Ex-1001 at 3:20-31. In particular, Sukegawa discloses an access controller, which "provides access control of the flash EEPROM chips." Ex-1005 at 7:26-31, 7:46-51; Ex-1003, ¶ 190. Sukegawa further discloses that the access controller includes and is disposed to use a mapping table—or address conversion table—to select a flash EEPROM and "read[] and write[] data from and into the selected EEPROM." *Id.*, 8:17-19, 7:35-40. The access controller is thus a memory system. Ex-1003, ¶ 190.

The **access controller**, comprising the **address conversion table**, which is coupled to the **memory store**, is shown below:



F I G. 6

Id., ¶ 191.

e. [Claim 32d]: "wherein said first PBA includes a first set of access parameters and said second PBA includes a second set of access parameters, and at least one difference between said first and second PBAs;"

As explained above, Sukegawa's PBAs include access parameters, such as chip number and block number, which represent the physical location of a PBA. Ex-1005, 9:14-21, Fig. 11; Ex-1003, ¶ 193; *supra* § IX.A.1.c. Sukegawa also discloses at least one difference between the first and second PBAs, including for example, a **first PBA** that designates chip #10 and a **second PBA** that designates chip #11, as shown below in annotated Figure 11:

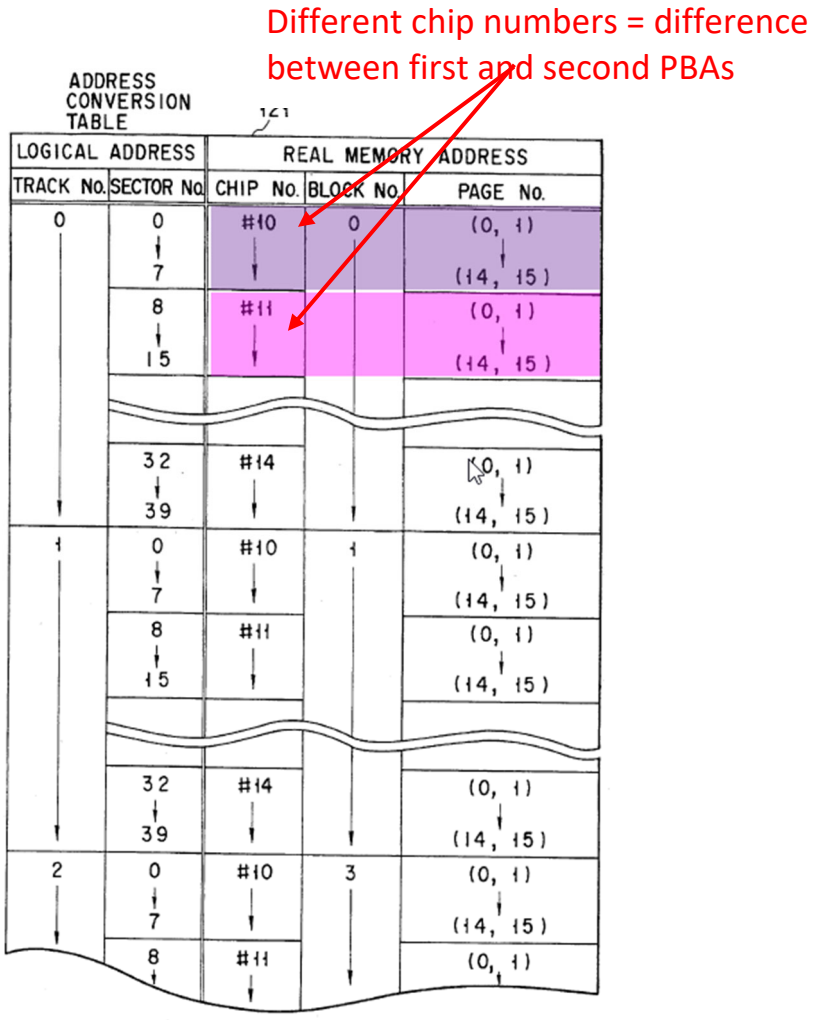


FIG. 11

Ex-1003, ¶ 194.

f. [Claim 32e]: "and wherein said mapping table increases the likelihood that that the operational load imposed on the storage apparatus during the processing of the I/O transaction request will be optimally distributed across storage device resources."

As explained above, Sukegawa's mapping table increases the likelihood that

an operational load will be optimally distributed across on the storage apparatus by "enabling parallel write operations" on different sectors in response to a request from a host. *Supra* § IX.A.1.d; Ex-1005, 8:39-43, 10:20-21, 12:36-41, 4:51-57; Ex-1003, ¶ 196. Sukegawa also discloses "contiguous LBA sets, adjacent LBA sets, [and] adjacent PBA's differing by at least one parameter," *supra* §§ IX.A.2.b, IX.A.2.c, IX.A.2.e, which the district court has identified as additional examples of optimized memory operations. Ex-1008 at 30; Ex-1003, ¶ 196.

Finally, Sukegawa discloses that these operations are performed during the processing of a transaction request, noting that the controller accesses memory for read and write transactions "in response to an [sic] disk access request supplied from a host CPU." *Id*. at 7:28-32; 11:3-6; Ex-1003, ¶ 197.

3. Sukegawa Anticipates Claim 34

a. [Claim 34a]: "The electronic storage device of claim 32, wherein the processing of the I/O transaction request includes a first memory operation performed using said first PBA and a second memory operation performed using said second PBA;"

Sukegawa discloses all elements of claim 32. *Supra*, § IX.A.2. Sukegawa further discloses that processing a request includes first and second memory operations performed using first and second PBAs. In particular, Sukegawa explains that the host CPU specifies a memory write operation, in which the controller begins writing data to page 0, of block 0, in flash EEPROM chip #10. Ex-1005 at 9:35-38,

9:51-54; Ex-1003, ¶ 201. The controller then performs another write operation by writing data to page 0, of block 0, of flash EEPROM chip #11. Ex-1005 at 9:56-65. These locations, respectively, correspond to the **first PBA** and the **second PBA**, as shown below. Ex-1003, ¶¶ 201-202.

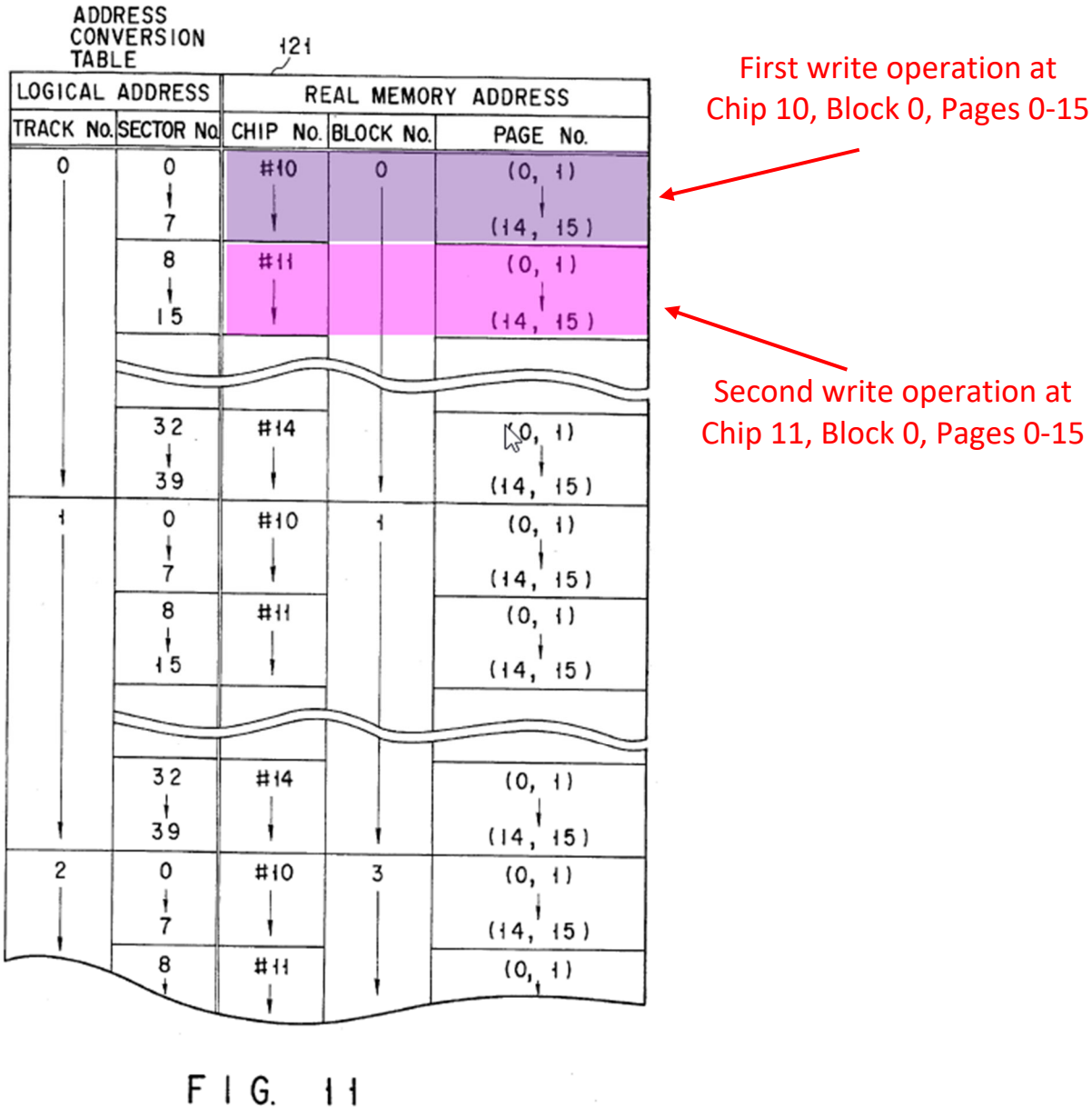


FIG. 11

b. [Claim 34b]: "said first and second PBAs respectively associated with a first set of access parameters and a second set of access parameters, and said set of first and second set of access parameters differing by at least one access parameter."

Sukegawa teaches that each of the PBAs disclosed in the reference are disposed to represent a specific set of access parameters, such as a chip identifier and block identifier. Ex-1005, 9:14-21, Fig. 11; Ex-1003, ¶ 204. Sukegawa further teaches at least one difference between these parameters, including, for example, that the access parameters for the **first PBA** identify chip #10, while the access parameters for the **second PBA** identify chip #11, as shown in annotated Figure 11 below:

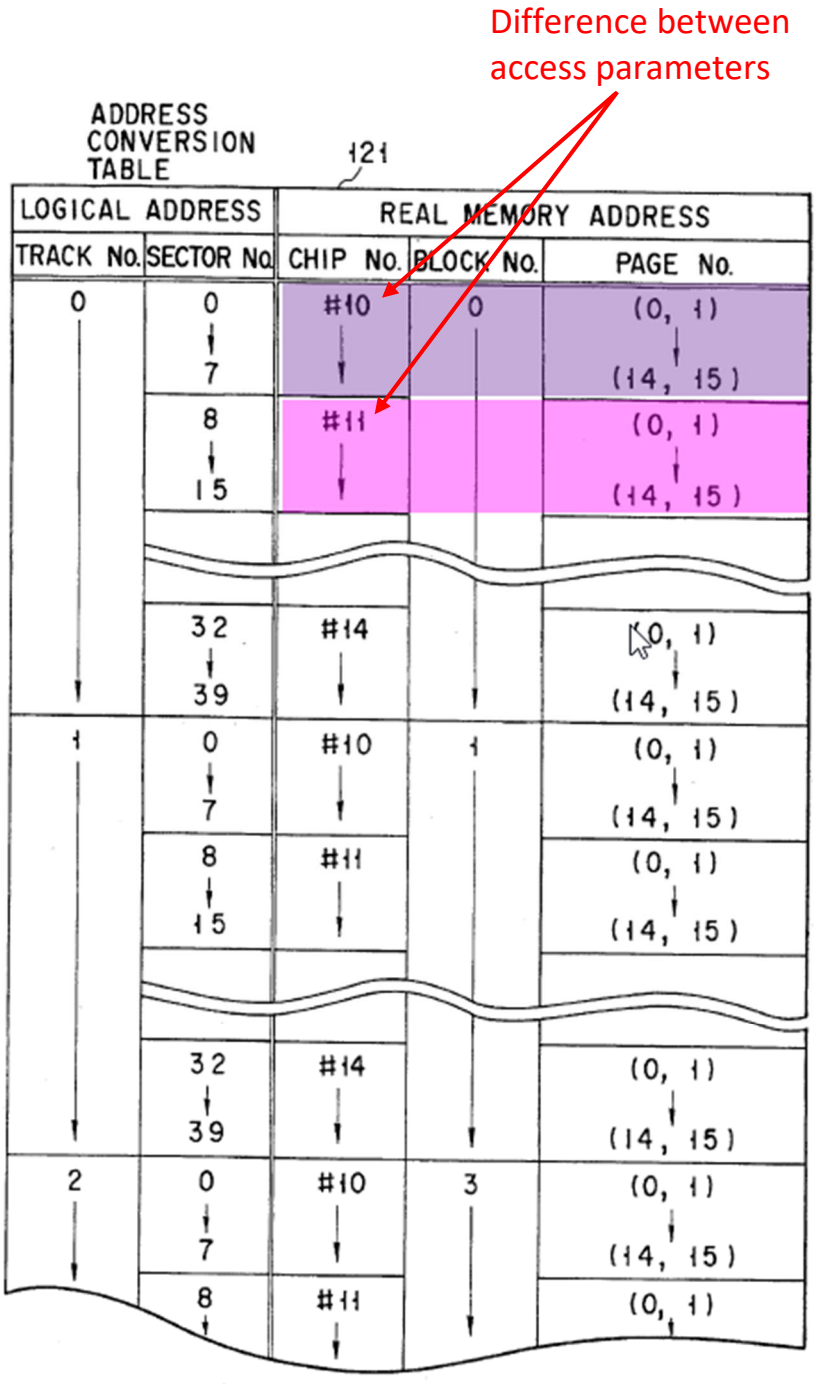


FIG. 11

Ex-1003, ¶ 205.

B. Ground 2: Claims 9-15 are Rendered Obvious by Sukegawa in View of Bruce

1. Claim 9 is Rendered Obvious by Sukegawa and Bruce

a. [Claim 9]: "The mapping table of claim 1, wherein said set of access parameters includes a bus identifier, an FDE identifier and a group identifier."

Sukegawa discloses all elements of claim 1. *Supra*, § IX.A.1. Likewise, Bruce teaches that access parameters representing a physical memory location include the identifiers recited in claim 9.

Specifically, Bruce teaches a bus identifier. Bruce discloses two flash buses—which are coupled to a flash-specific DMA controller and also coupled to flash buffer chips—that pass commands and addresses from the flash-specific DMA controller to flash memory. Ex-1006 at 2:56-59, 3:62-64, 2:63-65; 5:7-12. Each flash bus "can operate at the same time, allowing flash operations to be initiated and processed in parallel." *Id.* at 5:18-20; Ex-1003, ¶ 128. The buses are identified using the identifiers "**flash bus 10/Flash Bus-A**" and "**flash bus 18/Flash Bus-B**," which are illustrated in annotated Figures 1 and 2, below:

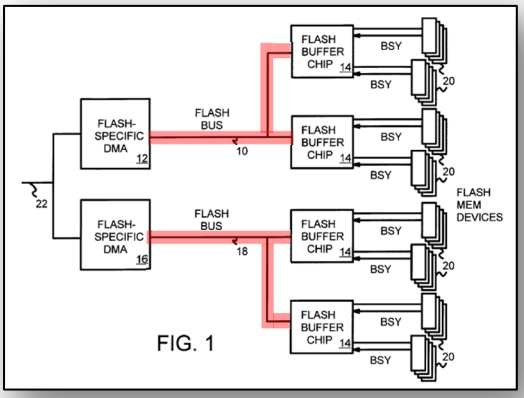


FIG. 1

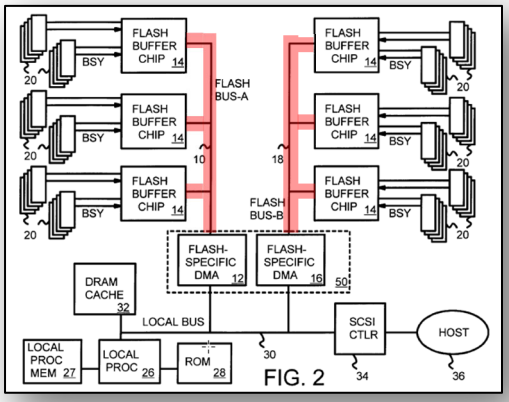


FIG. 2

Thus, Bruce teaches bus identifiers associated with a PBA. Ex-1003, ¶¶ 128-130.

Bruce also teaches an FDE identifier. Bruce's two flash buses are coupled to a specific DMA controller that can generate command, address, and data sequences to the flash memory chips. Ex-1006 at 2:56-57, 3:59-62, 4:8-10, 5:2-6. The dual **flash-specific DMA controllers 12 and 16** are shown below:

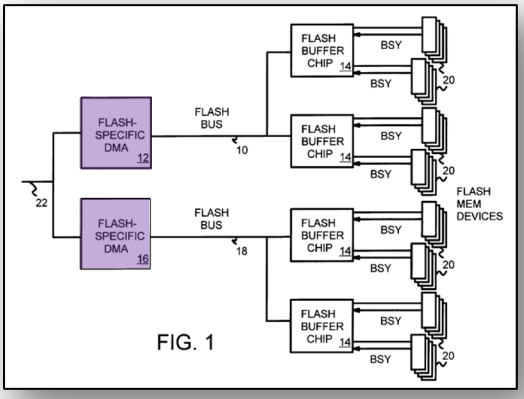


FIG. 1

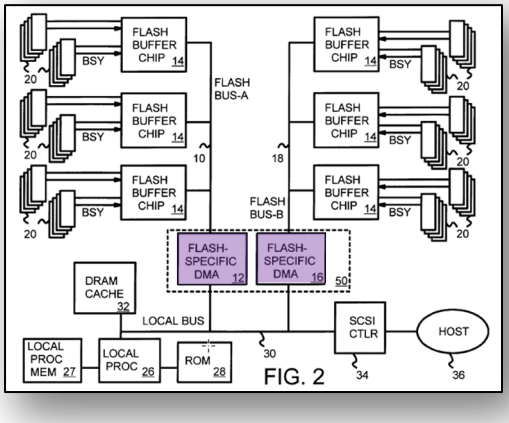


FIG. 2

Within each controller are four "state machines," which control one of four banks of flash-memory chips, *id.*, Abstract, 11:23-25, 6:53-55, thereby permitting a total of eight flash accesses. *Id.*, 6:55-57. Bruce discloses that data can be interleaved

among the four banks for each flash buffer chip, and also interleaved among chips connected to the two flash busses." *Id*. at 6:57-60; 13:32-35; Ex-1003, ¶¶131-132. Annotated Figure 3 illustrates the four **state machines** (identified as "**Bank0 SM**," "**Bank1 SM**," "**Bank2 SM**," and "**Bank3 SM**") within each flash specific **DMA controller**, thereby providing a total of eight state machines:

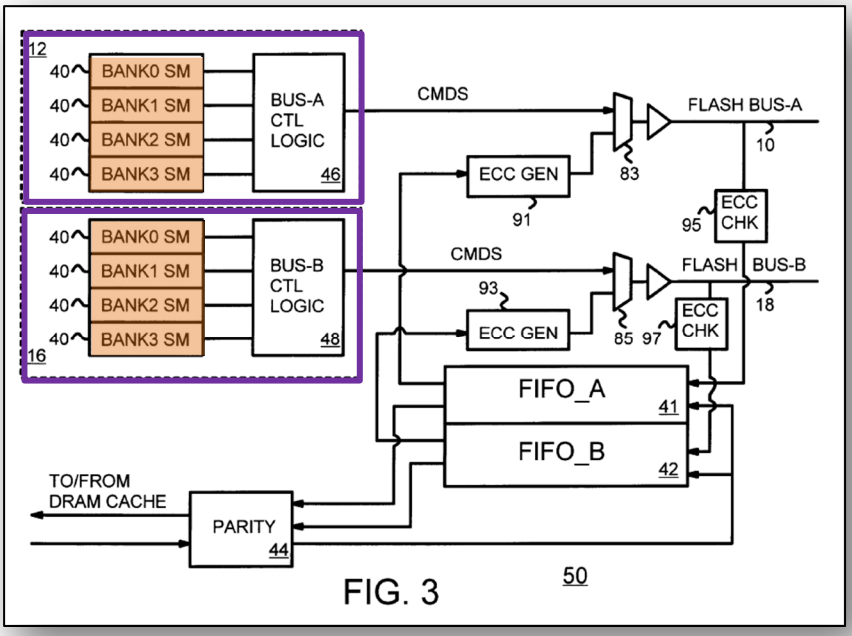


FIG. 3

Accordingly, each state machine is an FDE—or a component that controls multiple flash devices and facilitates high speed data transfers to and from a group of flash memory devices—pursuant to Petitioners' proposed constructions of FDE identifier and PBA. *Supra*, §§ VII.C, VII.D; Ex-1003, ¶¶ 131-134. The identifiers for the state machines (e.g., **Bank0 SM**," "**Bank1 SM**," etc.) thus represent FDE identifiers. Ex-1003, ¶ 134.

Bruce also teaches group identifiers. Bruce discloses multiple memory banks, each comprising a plurality of flash memory chips, and teaches that up to four banks can be connected to one of multiple flash buffer chips. Ex-1006 at 12:59-62, 2:66-3:1, 5:31, 5:58-61; Ex-1003, ¶ 135. These flash memory **chip banks**, which are connected through a plurality of **flash buffer chips**, are shown below.

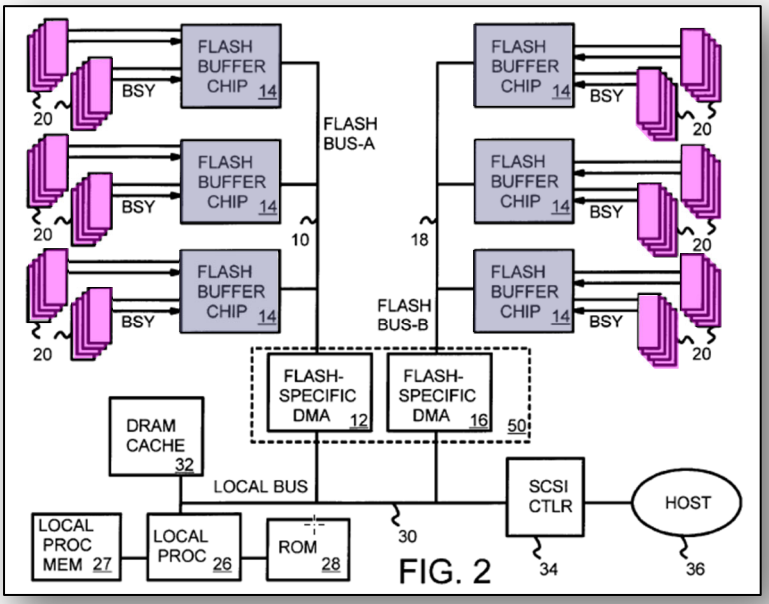


FIG. 2

Bruce also teaches that each bank can be separately accessed, which is enabled by the unique addressing of the flash memory chips connected to each flash buffer. Ex-1006 at 5:21-23, 6:55-57, 7:62-67. Thus, to access the memory, the DMA controller sends specific device addresses for each chip to the flash buffer, which then decodes the address into chip selects. *Id.* at 8:46-49, 10:17-19, 2:40-42; Ex-1003, ¶ 136. Bruce also teaches that each FDE (or state machine) controls an entire

memory bank comprising a plurality of flash chips. Bruce therefore teaches the use of group identifiers, or identifiers for identifying one flash memory device from another flash memory device from a set of flash devices that are controlled by the same FDE, pursuant to Petitioners' proposed construction. *Supra*, §§ VII.C, VII.D; Ex-1003, ¶ 137.

As explained above, it would have been obvious to a POSITA to modify Sukegawa's mapping table to include the identifiers disclosed by Bruce. *Supra*, § VIII.B.1; Ex-1003, ¶ 139. Accordingly, Sukegawa in combination with Bruce renders obvious this claim. Ex-1003, ¶ 139.

2. Claim 10 is Rendered Obvious by Sukegawa and Bruce

a. [Claim 10]: "The mapping table of claim 9, wherein said first and second PBA include different bus identifiers, different FDE identifiers and different group identifiers."

Sukegawa and Bruce teach all elements of claim 9. *Supra*, § IX.B.1; Ex-1003, ¶ 141. Bruce further teaches that the bus identifiers, FDE identifiers, and group identifiers taught therein may be different, including, for example, that a PBA (i.e., a unique addressable physical memory location) for a **first memory chip** on bus 10 would have one bus identifier ("**flash bus 10/Flash Bus-A**"), while a PBA for a **second memory chip** on bus 18 would have a different bus identifier ("**flash bus 18/Flash Bus-B** "), as shown below:

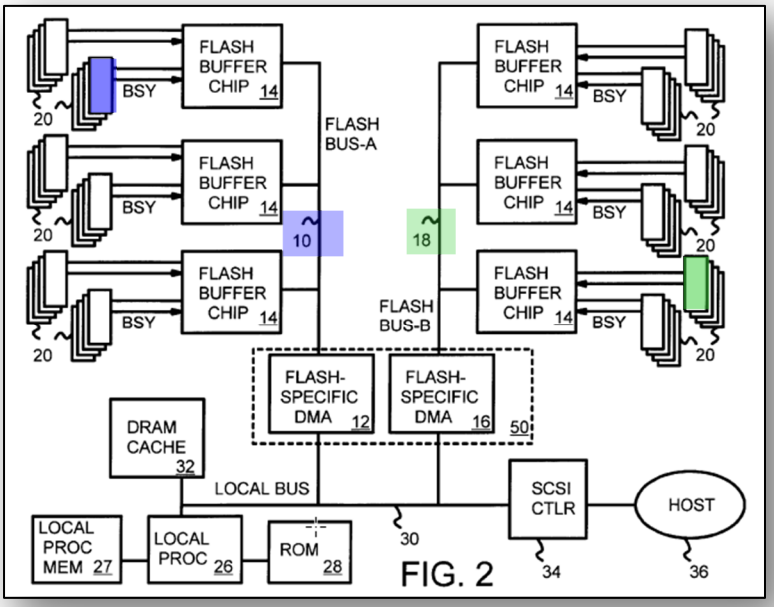


FIG. 2

Ex-1003, ¶ 142.

Bruce also teaches that each bank of memory devices is controlled by its own FDE engine, Ex-1006 at Abstract, 11:23-25, including for example that a PBA on a **first memory chip** located on **bus 10** would have one FDE identifier (e.g., "**Bank0 SM**"), while a PBA for a **second memory chip** located on **bus 18** would have a different FDE identifier (e.g., "**Bank3 SM**"), as shown below:

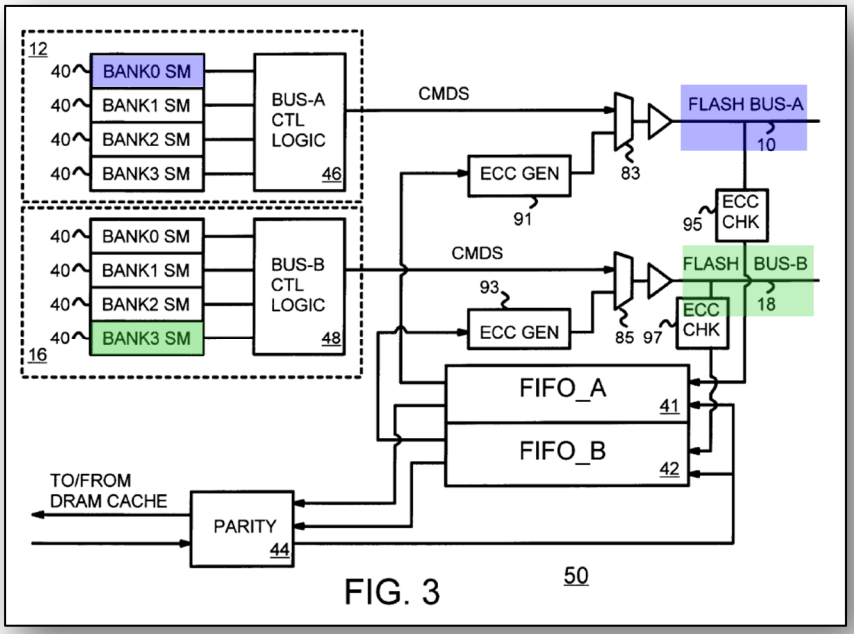


FIG. 3

Ex-1003, ¶ 143.

Bruce similarly teaches that groups of chips can be separately accessed. Ex-1006 at 6:55-57 (noting that "four flash-memory chips [can] be accessed at once for each flash bus, for a total of eight flash accesses"); 10:17-19. As a result, a PBA in one group of flash chips would have a different identifier from another group of flash chips. *Supra* § IX.B.1.a; Ex-1003, ¶ 144.

These specific parameters, and their differences, can be illustrated as follows:

	Access Parameters		
	Bus Identifier	**FDE Identifier**	**Group Identifier**
First unique physical location (PBA)	Bus 10/Bus-A	Bank0 SM	Specific address of first chip
Second unique physical location (PBA)	Bus 18/Bus-B	Bank3 SM	Specific address of second chip

Ex-1003, ¶ 145.

3. Claim 11 is Rendered Obvious by Sukegawa and Bruce

a. [Claim 11]: "The mapping table of claim 9, wherein said first and second PBA respectively include different combinations of said bus identifiers, said FDE identifiers, and said group identifiers."

Sukegawa and Bruce teach all elements of claim 9. *Supra*, § IX.B.1; Ex-1003, ¶ 148. As discussed above, Bruce teaches the use of different bus identifiers, FDE identifiers, and different group identifiers. *Id.* Bruce further teaches that each PBA may include different combinations of the bus identifiers, FDE identifiers, and group identifiers. *Id.*; Ex-1003, ¶ 149.

It would have been obvious to a POSITA to modify Sukegawa's mapping table to include the different identifiers disclosed by Bruce for the reasons noted above. *Supra* § VIII.B.1; Ex-1003, ¶ 150.

4. Claim 12 is Rendered Obvious by Sukegawa and Bruce

a. [Claim 12]: "The mapping table of claim 1, wherein said first and second PBA include different bus identifiers."

Sukegawa discloses all elements of claim 1, *supra*, § IX.A.1, and Bruce further teaches the use of different bus identifiers, as discussed above. *Supra*, §§ IX.B.1.a, IX.B.2.a; Ex-1003, ¶¶ 152-153.

It would have been obvious to a POSITA to modify Sukegawa's mapping table to include the different identifiers disclosed by Bruce for the reasons noted above. *Supra* § VIII.B.1; Ex-1003, ¶ 154.

5. Claim 13 is Rendered Obvious by Sukegawa and Bruce

a. [Claim 13]: "The mapping table of claim 1, wherein said first and second PBA include different FDE identifiers."

Sukegawa discloses all elements of claim 1, *supra*, § IX.A.1, and Bruce further teaches the use of different FDE identifiers, as discussed above. *Supra*, §§ IX.B.1.a, IX.B.2.a; Ex-1003, ¶¶ 156-157.

It would have been obvious to a POSITA to modify Sukegawa's mapping table to include the different identifiers disclosed by Bruce for the reasons noted above. *Supra* § VIII.B.1; Ex-1003, ¶ 158.

6. Claim 14 is Rendered Obvious by Sukegawa and Bruce

a. [Claim 14]: "The mapping table of claim 1, wherein said first and second PBA respectively include a first group identifier and a second group identifier."

Sukegawa discloses all elements of claim 1, *supra*, § IX.A.1, and Bruce further teaches the use of different group identifiers, as discussed above. *Supra*, §§ IX.B.1.a, IX.B.2.a; Ex-1003, ¶¶ 160-161.

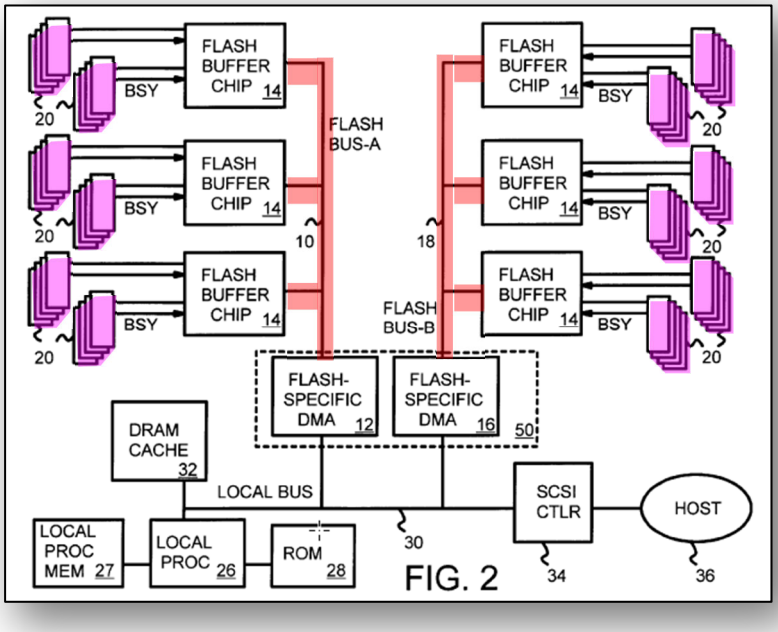
It would have been obvious to a POSITA to modify Sukegawa's mapping table to include the different identifiers disclosed by Bruce for the reasons noted above. *Supra* § VIII.B.1; Ex-1003, ¶ 162.

7. Claim 15 is Rendered Obvious by Sukegawa and Bruce

a. [Claim 15a]: "The mapping table of claim 1: wherein said memory store includes a set of solid state memory devices that are coupled to a set of buses and that are controlled by a set of FDEs; and"

Sukegawa discloses all elements of claim 1. *Supra*, § IX.A.1; Ex-1003, ¶ 164. Bruce discloses multiple memory banks, each of which can be "separately accessed, allowing many flash operations to be performed in parallel." Ex-1006 at 2:66-3:1, 5:31, 5:58-61, 5:21-23. Each of the memory banks therefore comprises a set of solid-state flash memory devices. Ex-1003, ¶ 165; *supra* § IX.B.1.a. As shown below, Bruce also teaches a set of **flash buses (bus 10/ Flash Bus-A** and **bus 18/ Flash**

Bus-B) coupled to a plurality of **sets of solid-state memory devices (flash memory banks)** through flash buffer chips:



Ex-1003, ¶ 166.

Bruce also teaches that the sets of solid-state memory devices are controlled by a set of "state machines," which constitute FDEs. Ex-1006 at Abstract, 11:23-25, 6:53-55, 6:55-57; Ex-1003, ¶ 167; *supra* § IX.B.1.a. Bruce's four **state machines** (or FDEs) within each flash specific **DMA controller** (providing a total of eight FDEs) are illustrated below:

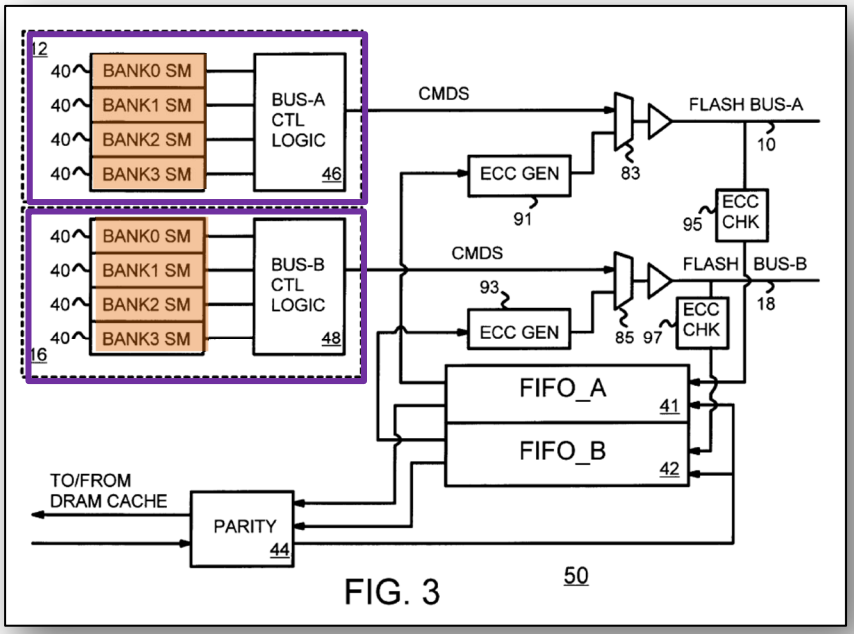


FIG. 3

Ex-1003, ¶168.

It would have been obvious to a POSITA to modify Sukegawa's mapping table to include the different bus identifiers, FDE identifiers, and group identifiers disclosed as explained above. *Supra*, § VIII.B.1. Accordingly, Sukegawa in combination with Bruce renders obvious this claim element. Ex-1003, ¶ 169.

b. [Claim 15b]: "wherein said access parameter includes a group identifier for identifying at least a portion of said set of memory devices that are respectively controlled by different FDEs from said set of FDEs."

As discussed above, Bruce teaches the use of group identifiers, pursuant to Petitioners' proposed constructions of this element. *Supra*, § IX.B.1.a; Ex-1003, ¶¶ 170-171. Bruce further discloses that each flash buffer chip may be connected to

multiple banks of flash memory chips, each of which has its own FDE. Ex-1003, ¶ 170. The group identifiers for the chips within each separate bank attached to flash buffer chip would identify "at least a portion of the set of memory devices" that are controlled by a different FDE from the set of FDEs. *Id.* ¶ 171.

It would have been obvious to a POSITA to modify Sukegawa's mapping table to include the different bus identifiers, FDE identifiers, and group identifiers disclosed by Bruce for the reasons discussed above. *Supra*, § VIII.B.1; Ex-1003, ¶¶ 170-171.

C. Ground 3: Claims 1 and 32 are Anticipated by Bennett

1. Bennett Anticipates Claim 1

a. [Claim 1 Pre]: "A mapping table for optimizing memory operations performed by an electronic storage device in response to receiving an I/O transaction request initiated by a host, said mapping table comprising:"

To the extent the preamble is limiting, Bennett discloses tables for "[m]apping between logical groups and physical groups (metablocks)." Ex-1007 at 23:61-64, 7:9-11, 9:55-58; Ex-1003, ¶ 209. For example, Bennett teaches a Group Access Table, or "GAT," which provides "a list of [physical] metablock addresses for all logical groups of host data in the memory system" and "contains one entry for each logical group, ordered sequentially according to logical address." *Id.* at 24:19-22,

25:1-3, 9:55-58; Ex-1003, ¶ 209. Bennett's GAT, with entries for each logical group, is shown below:

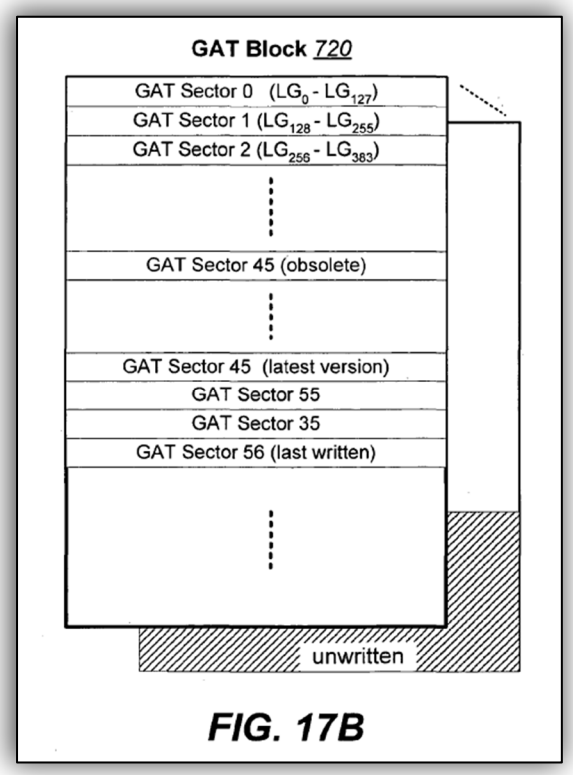


FIG. 17B

Bennett also teaches that the mapping table optimizes memory operations by enabling parallel memory operations. *Id.* at 8:26-30, 2:57-59; Ex-1003, ¶ 211.[3] Bennett's mapping table therefore provides more "efficient use of system resources" by allowing "multiple logical groups to be updated concurrently," which "increases efficiency and reduces overhead." Ex-1007 at 4:50-52; Ex-1003, ¶ 211.

[3] As explained above, the '740 patent states that parallel memory operations are one example of "optimized memory operations. *Supra*, Footnote 2.

The district court's claim construction order also identifies "contiguous LBA sets, adjacent LBA sets, [and] adjacent PBA's differing by at least one access parameter" as examples of optimization. Ex-1008 at 30. As explained below, Bennett teaches each of these examples. *Infra* §§ IX.C.1.b, IX.C.1.c; Ex-1003, ¶ 212.

Bennett also discloses that the mapping table optimizes memory operations in response to processing of an I/O transaction with a host, explaining that the host "accesses the memory" and reads or writes "to the memory system in unit[s] of logical clusters, each consisting of one or more logical sectors." Ex-1007 at 6:53-59; 6:61-65; Ex-1003, ¶ 213.

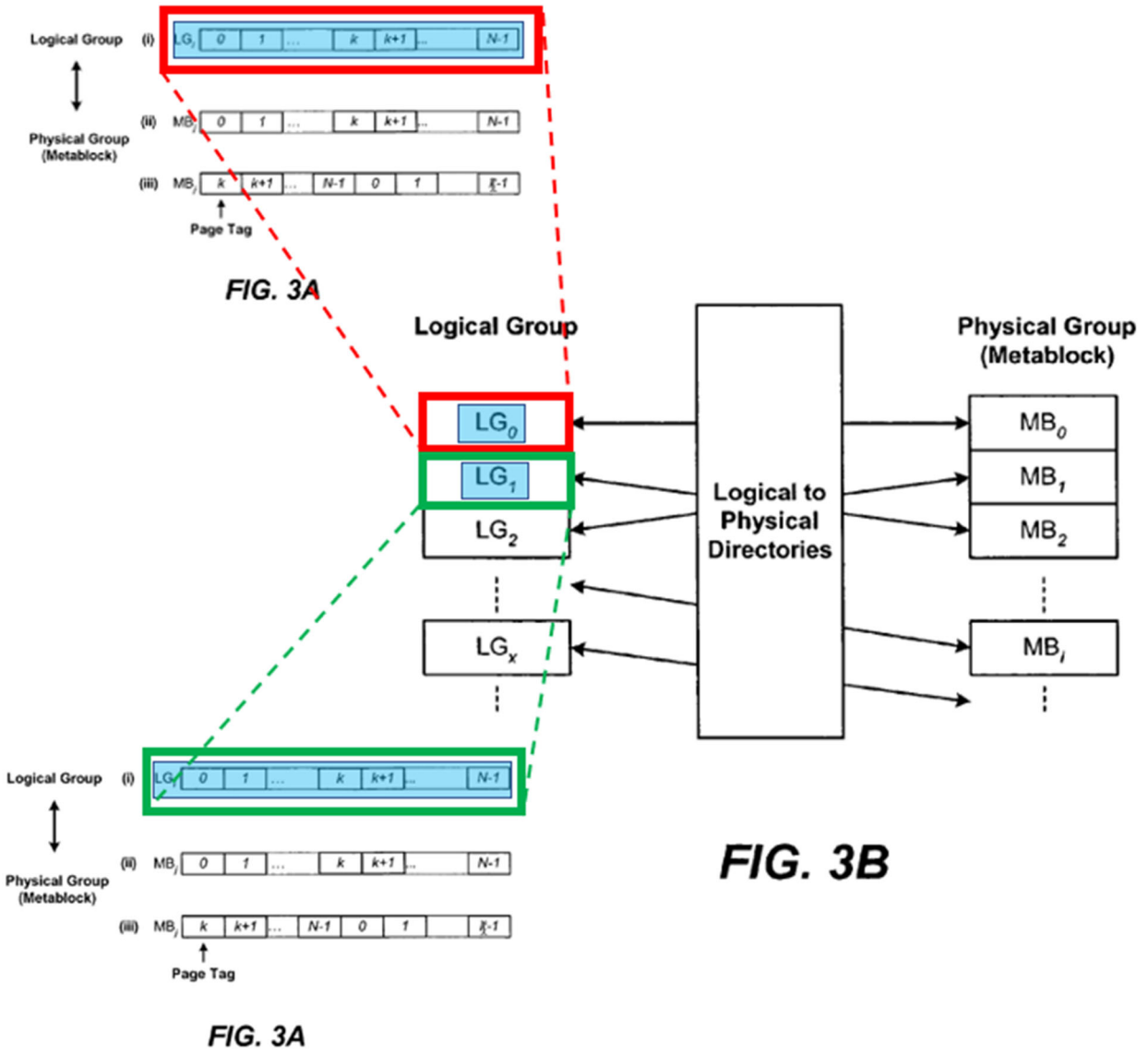
b. [Claim 1a]: "a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs;"

Bennett's discloses GAT sectors that include "logical to physical mapping information for 128 contiguous logical groups." Ex-1007 at 25:1-3, 24:21-22, 24:66-25:1. Each of these logical groups comprises a set of logical sectors which the host uses to address data. *Id.* at 6:54-57, 6:66-7:2. These logical sectors thus constitute LBAs, or addresses that are part of a logical addressing system used by a host, under

Petitioners' proposed construction. *Supra*, § VII.B; Ex-1003, ¶ 215.

Bennett further teaches that each logical group contains LBAs (logical sectors) that "are in contiguous logical order 0, 1, . . . , N-1." Ex-1007 at 7:13-15, 6:61-65, 11:6-9. Accordingly, Bennett discloses a set of logical fields disposed for representing a plurality of LBA sets, in which each LBA set represents a set of consecutive LBAs. Ex-1003, ¶ 217.

Annotated Figures 3A and 3B illustrate a **first logical field** (LG_0) comprising a set of **consecutive LBAs** (logical sectors) from 0 to N-1, and a **second logical field** (LG_1) comprising a set of **consecutive LBAs** (logical sectors):



Id., ¶ 218.

c. [Claim 1b]: "a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second

LBA sets with said first and second PBAs; and"

Bennett teaches metablocks that correspond to physical memory locations, explaining that "[t]he physical address space of the flash memory is treated as a set of metablocks." Ex-1007, 8:17-19, 4:13-15, 23:64-66. These metablocks are therefore PBAs—or unique addressable memory locations—pursuant to Petitioners' proposed construction. *Supra*, § VII.C; Ex-1003, ¶ 220.

Bennett further explains that the table associates the first and second LBA sets with first and second PBAs (or metablocks). Ex-1003, ¶ 221. For example, "[e]ach logical group is mapped to a unique metablock," and the "mapping information is maintained in a set of logical to physical directories." Ex-1007 at 7:38-44, 23:61-64, 9:56-58, 23:64-66. This is demonstrated by annotated Figures 3A and 3B, which illustrate the **first logical field** (LG_0,) associated with the **first PBA** (MB_0), and the **second logical field** (LG_1) associated with the **second PBA** (MB_2):

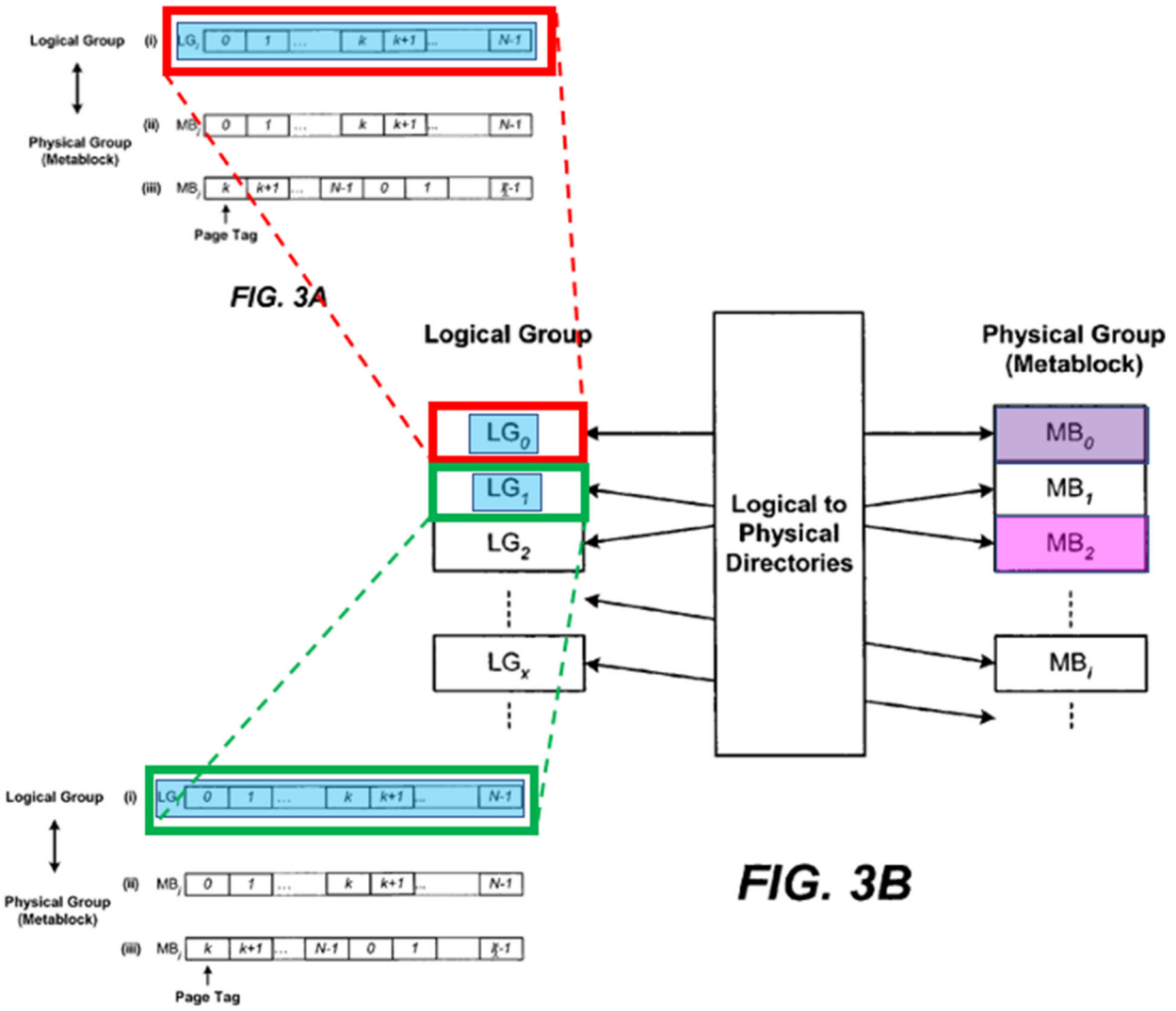


FIG. 3A

FIG. 3B

FIG. 3A

Ex-1003, ¶ 222.

Bennett also teaches sets of PBA fields disposed for representing a set of PBAs. For example, Bennett teaches that each metablock, comprises data fields for the "metablock number . . . and a flag indicating whether the metablock has been relinked." Ex-1007 at 24:39-42. Moreover, the identifiers in these fields for each PBA (e.g., the specific metablock number and relinked flag) exemplify access

parameters for representing the physical memory location of the PBA. *Id*. at 24:39-42, Figs. 3A, 3B, 17A; Ex-1003, ¶ 223.

The **PBA fields** for the **first PBA** (which corresponds to the **first logical field**) and the **second PBA** (which corresponds to the **second logical field**) are shown below in annotated Figures 3A and 17A from Bennett:

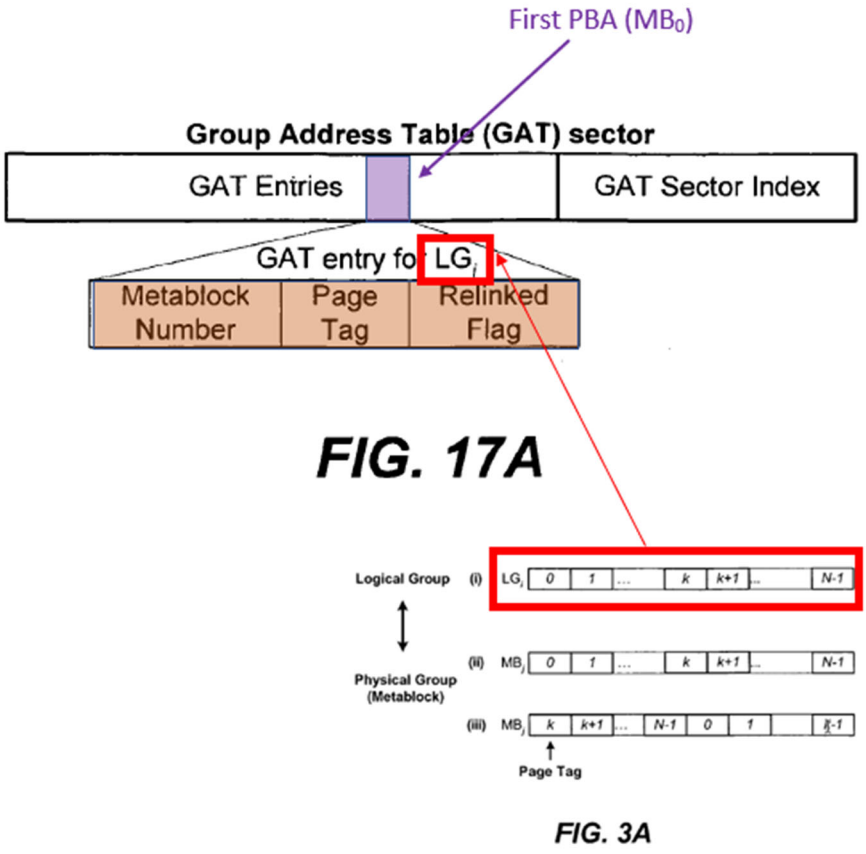


FIG. 17A

FIG. 3A

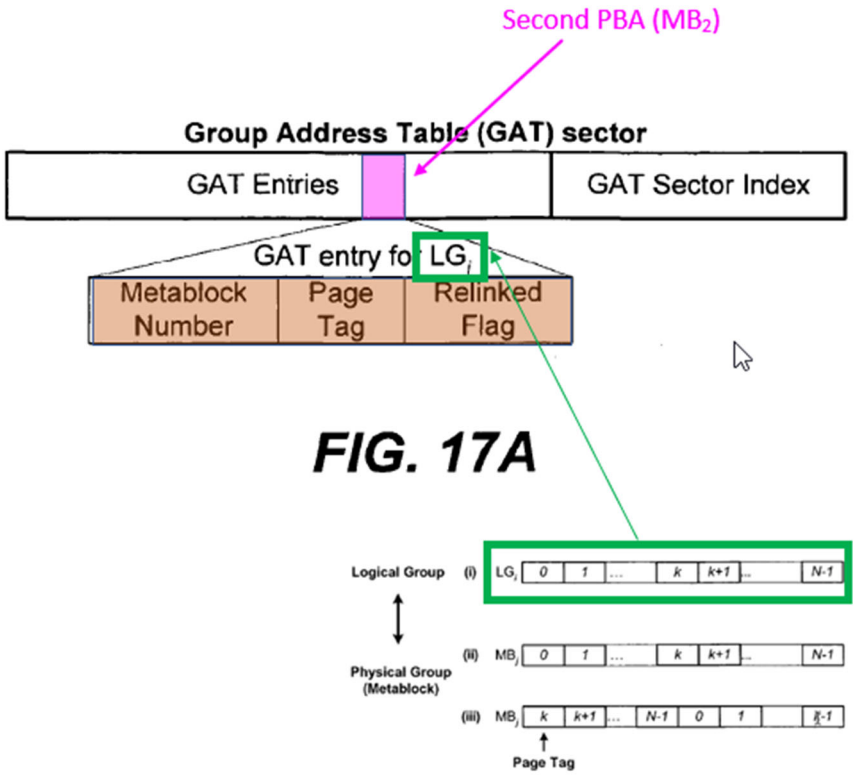


FIG. 17A

FIG. 3A

Ex-1003, ¶ 224.

d. [Claim 1c]: "wherein, in response to receiving the I/O transaction request, said mapping table causes the electronic storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second LBA sets."

Bennett teaches that "[i]n order to maximize programming speed and erase speed, parallelism is exploited as much as possible by arranging for multiple pages of information . . . to be programmed in parallel, and for multiple MEUs [minimum erasable units] to be erased in parallel." Ex-1007 at 8:26-30, 2:57-59. As explained

above, parallel memory operations are an example of optimized memory operations. *Supra* Footnote 2; Ex-1003, ¶ 226. Likewise, Bennett explains that the mapping table provides a more "efficient use of system resources" by allowing "multiple logical groups to be updated concurrently," which "increases efficiency and reduces overhead[]." Ex-1007 at 4:50-52.

The district court's claim construction order also identifies "contiguous LBA sets, adjacent LBA sets, [and] adjacent PBA's differing by at least one parameter" as examples of optimization. Ex-1008 at 30; Ex-1003, ¶ 227. As explained above, Bennett teaches each of these examples of optimized memory operations as well. *Supra* §§ IX.C.1.b, IX.C.1.c; Ex-1003, ¶ 227.

Finally, Bennett also discloses that the mapping table optimizes memory operations in response to receiving an I/O transaction request, explaining that the host "accesses the memory" and reads or writes "to the memory system in unit[s] of logical clusters, each consisting of one or more logical sectors." Ex-1007 at 6:53-59; 6:61-65; Ex-1003, ¶ 228.

2. Bennett Anticipates Claim 32

a. [Claim 32 Pre]: "An electronic storage device that includes a memory system that uses a memory table for increasing the likelihood that an operational load imposed on the storage apparatus during the processing of an I/O transaction request will be optimally distributed across storage device resources, said I/O transaction request received by said storage

device from a requesting host, said electronic storage device comprising:"

To the extent the preamble is limiting, Bennett teaches a memory system that operates with a host, and which takes the form of an electronic storage device such as a memory card or embedded memory system. Ex-1007 at 6:24-27; Ex-1003, ¶ 287.

Bennett also discloses that the electronic storage device uses a memory table for "[m]apping between logical groups and physical groups (metablocks)." *Id.* at 23:61-64, 7:9-11, 9:55-58. For example, Bennett teaches a Group Access Table, or "GAT," which provides "a list of [physical] metablock addresses for all logical groups of host data in the memory system." *Id.* at 24:19-21; Ex-1003, ¶ 288. Bennett's GAT, with entries for each logical group, is shown below:

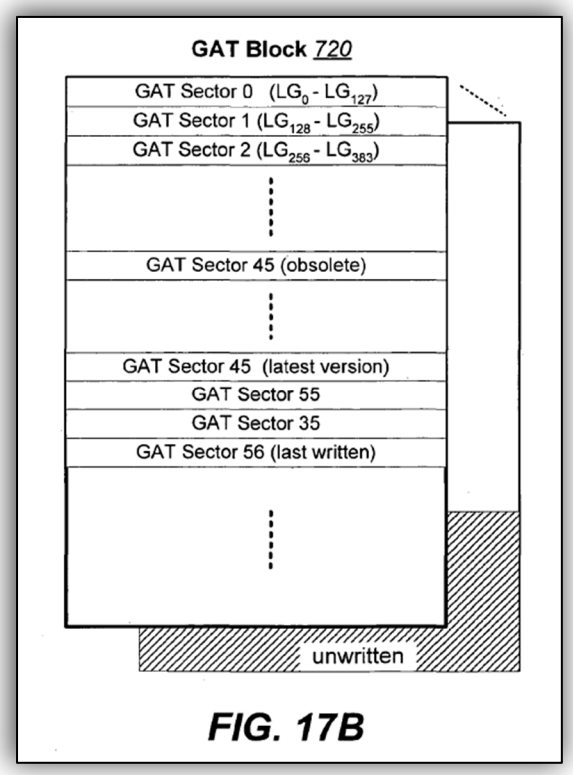


FIG. 17B

Bennett further teaches that the memory table increases the likelihood that an operational load imposed on the storage apparatus will be optimally distributed across storage device resources by enabling parallel memory operations. *Id.*, 8:26-30, 2:57-59; Ex-1003, ¶ 288. As explained above, parallel memory operations are an example of optimized memory operations. *Supra* Footnote 2; Ex-1003, ¶ 288. Bennett also discloses "contiguous LBA sets, adjacent LBA sets, [and] adjacent PBA's differing by at least one parameter," *infra* §§ IX.C.2.b, IX.C.2.c, IX.C.2.e, which the district court has identified as examples of optimized memory operations. Ex-1008 at 30; Ex-1003, ¶ 290.

Bennett also explains that the memory table optimizes memory operations in response to processing of an I/O transaction with a host, including, for example, that the host "accesses the memory" and reads or writes "to the memory system in unit[s] of logical clusters, each consisting of one or more logical sectors." *Id.*, 6:53-59, 6:61-65. Thus, Bennett's system "maps the logical address from the host to a physical memory location." *Id.*, 9:20-22; Ex-1003, ¶ 289.

b. [Claim 32a]: "a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA, said first and second LBA sets including respective sets of consecutive LBAs;"

As explained above, Bennett discloses a mapping table in the form of the GAT, which provides "a list of [physical] metablock addresses for all logical groups of host data in the memory system" and "contains one entry for each logical group, ordered sequentially according to logical address." *Id.*, 24:19-22, 25:1-3, 9:55-58; *supra* § IX.C.2.a; Ex-1003, ¶ 292. Each of these logical groups comprises a set of logical sectors which the host uses to address data. *Id.* at 6:54-57, 6:66-7:2; Ex-1003, ¶¶ 293-294. These logical sectors thus constitute LBAs, or addresses that are part of a logical addressing system used by a host, under Petitioners' proposed construction. *Supra*, § VII.B; Ex-1003, ¶ 295. Bennett further teaches that each logical group contains logical sectors that "are in contiguous logical order 0, 1, . . . , N-1." Ex-1007 at 7:13-15, 6:61-65, 11:6-9. Accordingly, Bennett discloses first and second

LBA sets that include sets of consecutive LBAs. Ex-1003, ¶ 295.

Bennett also teaches metablocks that correspond to physical memory locations, noting that "[t]he physical address space of the flash memory is treated as a set of metablocks." Ex-1007, 8:17-19, 4:13-15, 23:64-66. These metablocks are therefore PBAs—or unique addressable memory locations—pursuant to Petitioners' proposed construction. *Supra*, § VII.C; Ex-1003, ¶ 296.

Bennett further explains that the mapping table associates the first and second LBA sets with first and second PBAs (or metablocks). In particular, "[e]ach logical group is mapped to a unique metablock," and the "mapping information is maintained in a set of logical to physical directories." Ex-1007 at 7:38-44, 23:61-64, 9:56-58, 23:64-66; Ex-1003, ¶ 297. This is demonstrated by annotated Figures 3A and 3B, which illustrate a **first logical field** (LG_0,) comprising **consecutive LBAs** mapped to a **first PBA** (MB_0), and a **second logical field** (LG_1) comprising **consecutive LBAs** mapped to a **second PBA** (MB_2):

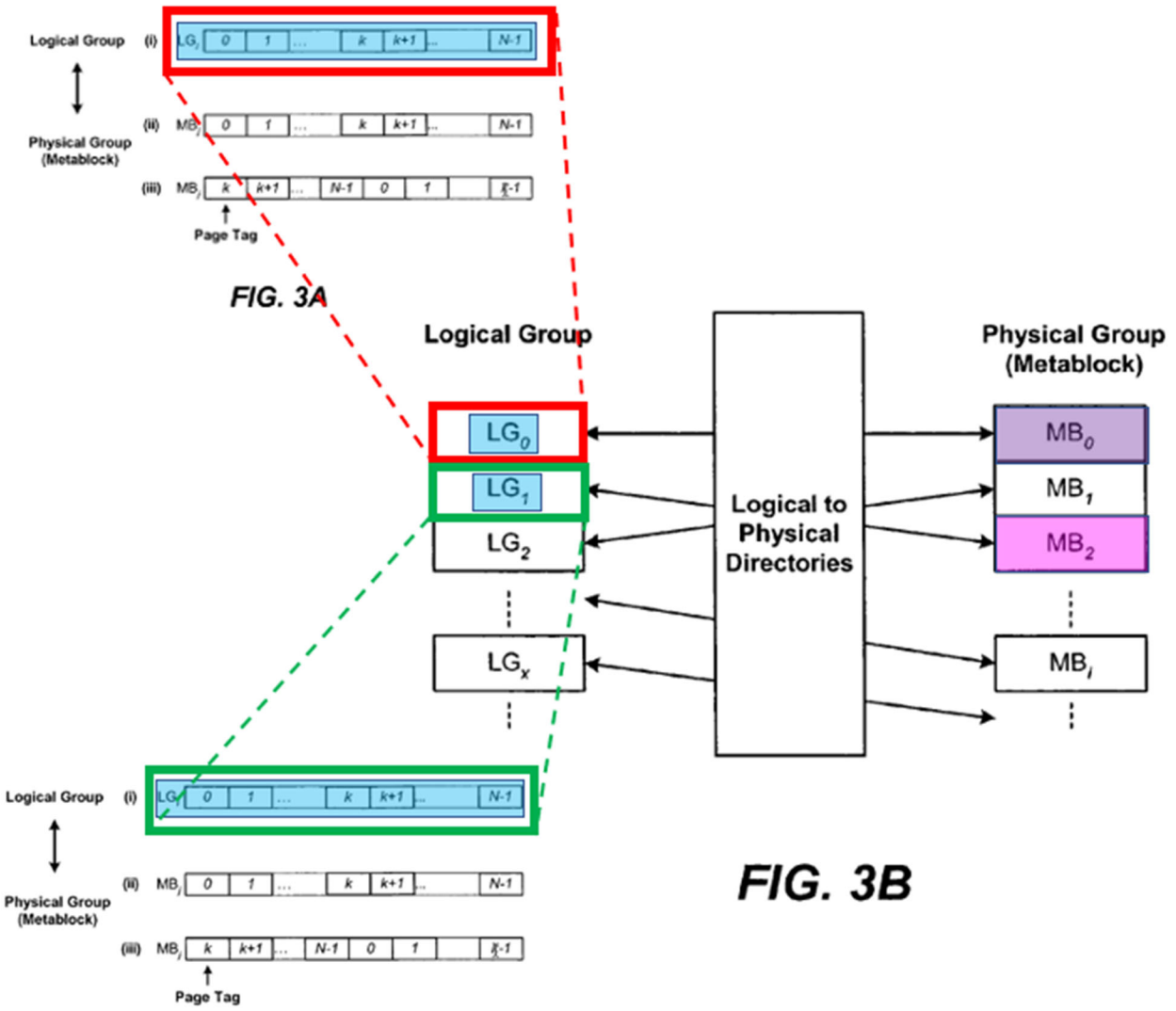


FIG. 3A

FIG. 3B

FIG. 3A

Ex-1003, ¶¶ 298-299.

c. [Claim 32b]: "a memory store that includes a set of flash devices, said set of flash devices includes a first physical memory location and a second physical memory location that are addressable by said first and second PBAs respectively;"

Bennett teaches a memory store, or flash memory 200, which comprises an

array of memory cells that may be "distributed over one or more integrated circuit chip[s]." Ex-1007 at 6:27-31, 8:34-38; Ex-1003, ¶ 300. Each flash chip has a specific memory location. *Id.* at Abstract.

Bennett further teaches that the first and second physical locations are addressable by first and second PBAs (i.e., physical sectors). "The physical address space of the flash memory is treated as a set of metablocks.," *id.* 8:17-19, and each metablock represents "a group of memory locations, e.g., sectors that are erasable together." *Id*. at 8:15-16, 6:50-52. Thus, the first physical memory location would be addressable by a first PBA and a second memory location would be addressable by a second PBA. Ex-1003, ¶ 301.

Annotated Figure 2 from Bennett shows Bennett's memory store with physical memory locations represented by **metablocks (MB_0 . . . MB_i)**:

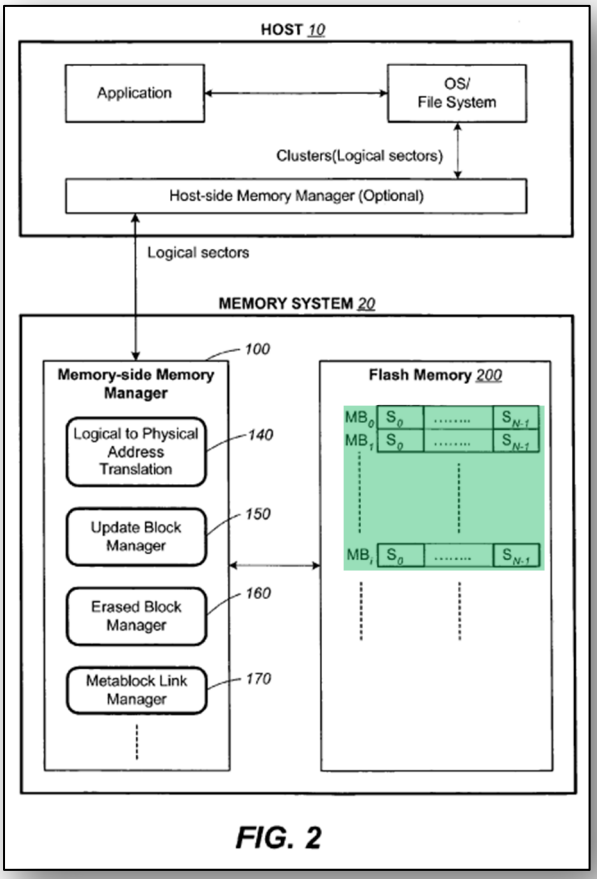


FIG. 2

Ex-1003, ¶ 302.

d. [Claim 32c]: "a memory system coupled to said memory store and disposed to use said mapping table during a memory operation;"

Bennett discloses a memory system, which the '740 patent describes as comprising a controller and mapping table. Ex-1001 at 3:20-31; Ex-1003, ¶ 304. For example, Bennett teaches a memory system comprising a controller 100 that is coupled to the memory store and includes a logical to physical address translation module 140, which utilizes the GAT to "map[] the logical address from the host to

a physical memory location." Ex-1007 at 9:20-22.

Annotated Figure 6, below, illustrated **controller 100** coupled to **flash memory 200**, as well as the logical to physical address translation module 140 (highlighted in yellow) that is connected to and uses information from the GAT during a memory operation:

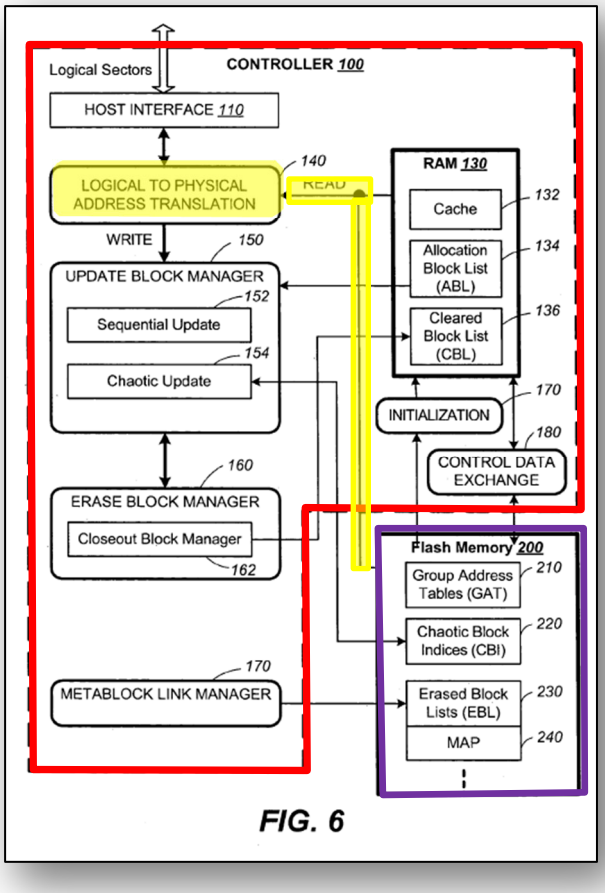


FIG. 6

Ex-1003, ¶ 304.

e. [Claim 32d]: "wherein said first PBA includes a first set of access parameters and said second PBA includes a second set of access parameters, and at least one

difference between said first and second PBAs;"

Bennett teaches that the first and second PBAs include first and second sets of access parameters. Ex-1003, ¶ 306. For example, Bennett teaches that each metablock comprises data fields for the "metablock number . . . and a flag indicating whether the metablock has been relinked." Ex-1007 at 24:39-42. Moreover, the specific identifiers in these fields (e.g., the specific metablock number and relinked flag) exemplify access parameters for representing the physical memory location of the PBA. *Id*. at 24:39-42, Figs. 3A, 3B, 17A; Ex-1003, ¶ 306. Bennett further discloses that at least one difference, in the form of a different metablock number (e.g., MB_0 and MB_2), exists between the PBAs. *Supra* § IX.C.2.c; Ex-1003, ¶ 306.

The access parameters for each of **PBA fields** for the **first PBA** (MB_0) and the **second PBA** (MB_2) are illustrated in the annotated figures below:

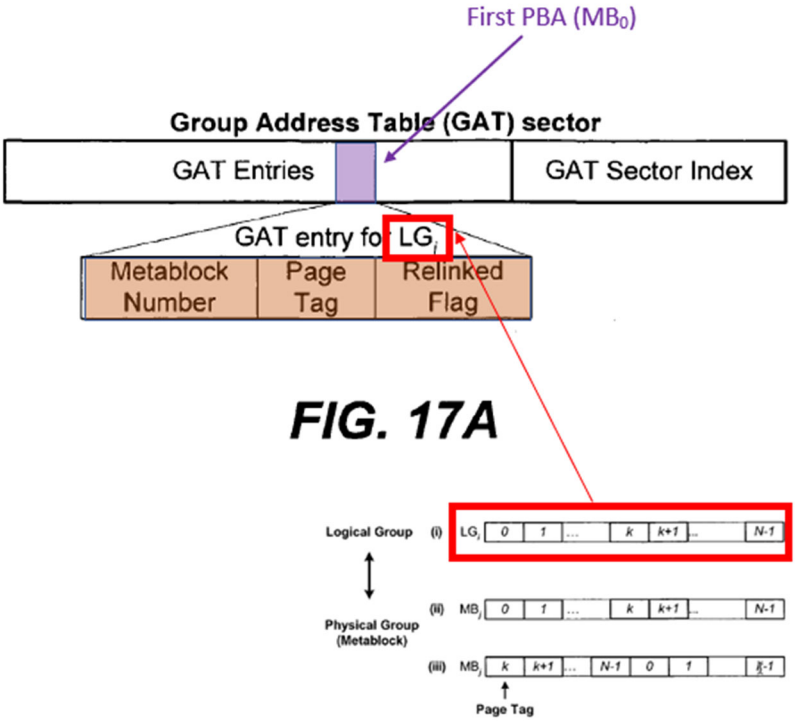


FIG. 17A

FIG. 3A

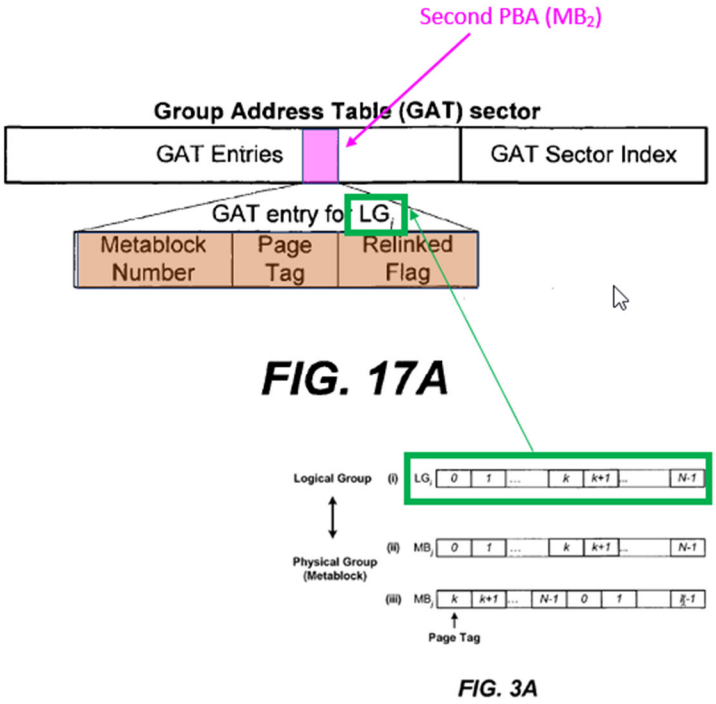


FIG. 17A

FIG. 3A

Ex-1003, ¶ 307.

f. [Claim 32e]: "and wherein said mapping table increases the likelihood that that the operational load imposed on the storage apparatus during the processing of the I/O transaction request will be optimally distributed across storage device resources."

Bennett teaches that "[i]n order to maximize programming speed and erase speed, parallelism is exploited as much as possible by arranging for multiple pages of information . . . to be programmed in parallel, and for multiple MEUs [minimum erasable units] to be erased in parallel." Ex-1007 at 8:26-30, 2:57-59. As explained above, parallel memory operations are an example of optimized memory operations. *Supra* Footnote 2; Ex-1003, ¶ 309. Likewise, Bennett explains that the mapping table provides a more "efficient use of system resources" by allowing "multiple logical groups to be updated concurrently," which "increases efficiency and reduces overhead." Ex-1007 at 4:50-52.

The district court's claim construction order also identifies "contiguous LBA sets, adjacent LBA sets, [and] adjacent PBA's differing by at least one parameter" as examples of optimization. Ex-1008 at 30. As explained above, Bennett teaches each of these examples as well. *Supra* §§ IX.C.2.b, IX.C.2.c, IX.C.2.e; Ex-1003, ¶ 309 & n.16.

In addition, Bennett explains that the mapping table optimizes memory operations in response to processing of an I/O transaction with a host, including, for

example, that the host "accesses the memory" and reads or writes "to the memory system in unit[s] of logical clusters, each consisting of one or more logical sectors." Ex-1007 at 6:53-59, 6:61-65; Ex-1003, ¶ 310.

D. Ground 4: Claims 9-15 and 34 are Rendered Obvious by Bennett in View of Bruce

1. Claim 9 is Rendered Obvious by Bennett and Bruce

a. [Claim 9]: "The mapping table of claim 1, wherein said set of access parameters includes a bus identifier, an FDE identifier and a group identifier."

As explained above, Bennett discloses all the elements of claim 1, *supra*, § IX.C.1, and Bruce discloses each of the access parameters recited in claim 9. *Supra*, § IX.B.1. As explained above, it also would have been obvious to include Bruce's access parameters in Bennett's table. *Supra*, § VIII.B.2; Ex-1003, ¶¶ 241-252.

2. Claim 10 is Rendered Obvious by Bennett and Bruce

a. [Claim 10]: "The mapping table of claim 9, wherein said first and second PBA include different bus identifiers, different FDE identifiers and different group identifiers."

As explained above, Bennett and Bruce disclose all the elements of claim 9, *supra*, § IX.D.1, and Bruce further discloses each of the access parameters recited in claim 10. *Supra*, § IX.B.2. As explained above, it also would have been obvious to include Bruce's access parameters in Bennett's table. *Supra*, § VIII.B.2; Ex-1003,

¶¶ 254-259.

3. Claim 11 is Rendered Obvious by Bennett and Bruce

a. [Claim 11]: "The mapping table of claim 9, wherein said first and second PBA respectively include different combinations of said bus identifiers, said FDE identifiers, and said group identifiers."

As explained above, Bennett and Bruce disclose all the elements of claim 9, *supra*, § IX.D.1, and Bruce further discloses each of the access parameters recited in claim 11. *Supra*, § IX.B.3. As explained above, it also would have been obvious to include Bruce's access parameters in Bennett's table. *Supra*, § VIII.B.2; Ex-1003, ¶¶ 261-263.

4. Claim 12 is Rendered Obvious by Bennett and Bruce

a. [Claim 12]: "The mapping table of claim 1, wherein said first and second PBA include different bus identifiers."

As explained above, Bennett discloses all the elements of claim 1, *supra*, § IX.C.1, and Bruce discloses each of the access parameters recited in claim 12. *Supra*, § IX.B.4. As explained above, it also would have been obvious to include Bruce's access parameters in Bennett's table. *Supra*, § VIII.B.2; Ex-1003, ¶¶ 265-267.

5. Claim 13 is Rendered Obvious by Bennett and Bruce

a. [Claim 13]: "The mapping table of claim 1, wherein

said first and second PBA include different FDE identifiers."

As explained above, Bennett discloses all the elements of claim 1, *supra*, § IX.C.1, and Bruce discloses each of the access parameters recited in claim 13. *Supra*, § IX.B.5. As explained above, it also would have been obvious to include Bruce's access parameters in Bennett's table. *Supra*, § VIII.B.2; Ex-1003, ¶¶ 269-271.

6. Claim 14 is Rendered Obvious by Bennett and Bruce

a. [Claim 14]: "The mapping table of claim 1, wherein said first and second PBA respectively include a first group identifier and a second group identifier."

As explained above, Bennett discloses all the elements of claim 1, *supra*, § IX.C.1, and Bruce discloses each of the access parameters recited in claim 14. *Supra*, § IX.B.6. As explained above, it also would have been obvious to include Bruce's access parameters in Bennett's table. *Supra*, § VIII.B.2; Ex-1003, ¶¶ 274-275.

7. Claim 15 is Rendered Obvious by Bennett and Bruce

a. [Claim 15a]: "The mapping table of claim 1: wherein said memory store includes a set of solid state memory devices that are coupled to a set of buses and that are controlled by a set of FDEs; and"

As explained above, Bennett discloses all the elements of claim 1, *supra*, §

IX.C.1, and Bruce discloses each of the access parameters recited in claim 15a. *Supra*, § IX.B.7.a. As explained above, it also would have been obvious to include Bruce's access parameters in Bennett's table. *Supra*, § VIII.B.2; Ex-1003, ¶¶ 277-282.

b. [Claim 15b]: "wherein said access parameter includes a group identifier for identifying at least a portion of said set of memory devices that are respectively controlled by different FDEs from said set of FDEs."

As explained above, Bruce discloses this claim element. *Supra* § IX.B.7.b. It also would have been obvious to include Bruce's access parameters in Bennett's table for the reasons discussed above. *Supra*, § VIII.B.2; Ex-1003, ¶¶ 283-285.

8. Claim 34 is Rendered Obvious by Bennett and Bruce

a. [Claim 34a]: "The electronic storage device of claim 32, wherein the processing of the I/O transaction request includes a first memory operation performed using said first PBA and a second memory operation performed using said second PBA;"

Bennett discloses all elements of claim 32 as explained above. *Supra*, § IX.C.2; Ex-1003, ¶ 313. As also explained above, Bruce teaches uniquely addressable memory locations (or PBAs) within different memory banks, which are associated with different FDEs, different buses, and different device addresses, as explained above. *Supra*, §§ IX.D.2, IX.D.3, IX.C.2.e. Ex-1003, ¶ 314. The banks of

flash-memory chips "can be separately accessed, allowing many flash operations to be performed in parallel." Ex-1006, 5:21-23, 6:55-57, 10:17-19. This simultaneous or parallel access to different unique memory locations (PBAs) illustrates a first memory operation using a first PBA and second memory operation using a second PBA. Ex-1003, ¶ 314.

It would have also been obvious to a POSITA to combine Bennett with Bruce for the reasons discussed above. *Supra*, § VIII.B.2; Ex-1003, ¶ 315.

b. [Claim 34b]: "said first and second PBAs respectively associated with a first set of access parameters and a second set of access parameters, and said set of first and second set of access parameters differing by at least one access parameter."

Bruce teaches uniquely addressable memory locations (or PBAs) within different memory banks, which are associated with different FDEs, different buses, and different device addresses, as explained above. *Supra*, §§ IX.D.2, IX.D.3, IX.C.2.e; Ex-1003, ¶ 316. Therefore, a first and second PBA can be identified using the following access parameters:

	Access Parameters		
	Bus Identifier	**FDE Identifier**	**Group Identifier**
First unique physical location (PBA)	Bus 10/Bus-A	Bank0 SM	Specific address of first chip

Second unique physical location (PBA)	Bus 18/Bus-B	Bank3 SM	Specific address of second chip

Ex-1003, ¶ 316. A POSITA would therefore understand Bruce to disclose that each of the PBAs is associated with a set of access parameters, in which the first set of access parameters differ by at least on access parameter. Ex-1003, ¶317.

It would have also been obvious to a POSITA to combine Bennett with Bruce for the reasons discussed above. *Supra*, § VIII.B.2; Ex-1003, ¶ 318.

X. INSTITUTION SHOULD NOT BE DISCRETIONARILY DENIED

A. The Board Should Not Exercise Its Discretion Under 35 U.S.C. § 314(a)

Petitioners hereby stipulate that, should the Petition be granted, they will not pursue in the district court the same grounds that are raised or could have reasonably been raised in this Petition pursuant to *Sotera Wireless, Inc., v. Masimo Corp.* IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020) (precedential as to § II.A). Under the June 21, 2022, *Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation*, the Director has stated that "the PTAB will not discretionarily deny institution of on an IPR" in view of such a stipulation. Interim Procedures at 7; *id*. at 3 and n.3 (discussing *Sotera*).

Accordingly, Petitioners' stipulation is dispositive in establishing that institution should not be discretionarily denied pursuant to 35 U.S.C. § 314(a).

B. The Board Should Not Exercise Its Discretion under 35 U.S.C. § 325(d)

In evaluating arguments under § 325(d), [the PTAB] use[s] a two-part framework: (1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of the first part of the framework is satisfied, whether the petition has demonstrated that the Office erred in a manner material to the patentability of challenged claims." *The Data Co. Techs., Inc. v. Bright Data Ltd.*, IPR2022-00135, Paper 12 at 15 (PTAB June 1, 2022) (citing *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020); *Slayback Pharma LLC v. Eye Therapies, LLC*, IPR2022-00146, Paper 14 at 7 (PTAB May 18, 2022).

The PTAB also considers the non-exclusive factors set forth in *Becton, Dickinson and Co. v. B. Braun Melsungen AG*. IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential in relevant part); *see also The Data Co.*, IPR2022-00135, Paper 12 at 15. These factors include: (a) the similarities and material differences between the asserted art and the prior art involved during examination; (b) the cumulative nature of the asserted art and the prior art evaluated during examination; (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection; (d) the extent

of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art; (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments. *Becton, Dickinson*, Paper 8 at 17-18. "[F]actors (a), (b), and (d) [of *Becton*] relate to whether the same or substantially the same art or arguments previously were presented to the Office" under *Advanced Bionics*. *Slayback*, IPR2022-00146, Paper 14 at 8. "[F]actors (c), (e), and (f) [of *Becton*] relate to whether the petitioner has demonstrated a material error by the Office" under *Advanced Bionics*. *Id*.

Here, none of Sukegawa, Bennett, or Bruce are printed on the face of the '740 patent, were listed on an IDS during examination of the application that led to the '740 patent, or were addressed in any office action for the '740 patent. Nor were any other prior art or arguments substantially similar to those presented in this Petition presented to the Office during prosecution of the '740 patent. Thus, the *Advanced Bionics* framework should not apply because the first part is not satisfied. *Id.* at 17.

Nonetheless, Petitioners note that the '740 patent is a purported continuation-

in-part of '098 patent, and that Bruce was cited against the '098 patent.[4] Ex-1010 at 1. Petitioners do not believe that this has any bearing on the analysis. To the extent that the Board disagrees, however, the *Advanced Bionics* framework strongly disfavors discretionary denial.

1. The Same Arguments Were Not Previously Presented to the Patent Office

"The Board has consistently declined exercising its discretion under Section 325(d) when the only fact a Patent Owner can point to is that a reference was disclosed to the Examiner during the prosecution." *Amgen, Inc. v. Alexion Pharms, Inc.*, IPR2019-00739, Paper 15 at 62 (PTAB Aug. 30, 2019) (collecting cases and declining to exercise discretion to deny institution where a reference was identified on an IDS but not substantively discussed during prosecution); *Amazon.com, Inc. v. M2M Solutions, LLC*, IPR2019-01204, Paper 14 at 16 (Jan. 23, 2020) ("The Board frequently holds that a reference that 'was neither applied against the claims nor discussed by the Examiner' does not weigh in favor of exercising the Board's discretion under § 325(d) to deny a petition") (citation omitted). This is particularly true where "the Examiner did not make any prior art rejections during prosecution."

[4] As noted above, Bruce was not presented to Office during prosecution of the '740 patent, nor is it printed on the face of the '740 patent.

Navistar, Inc. v. Fatigue Fracture Tech., LLC, IPR2018-00853, Paper 13, at 17-18 (PTAB Sept. 12, 2018).

Here, Bruce was neither identified during prosecution of the ’740 patent nor relied on by the Examiner in any rejection for the ’740 patent. Indeed, the Examiner made no prior art rejections whatsoever during prosecution of the ’740 patent; the only rejection was for failure to comply with the written description requirement of 35 U.S.C. § 112. Ex-1002 at 3-4. This fact “weighs strongly against exercising [] discretion to deny institution under 35 U.S.C. § 325(d).” *Intel Corp. v. Qualcomm Inc.*, IPR2019-00128, (PTAB May 29, 2019) (emphasis added); *Amgen*, IPR2019-00739, Paper 15 at 62-63; *Navistar*, IPR2018-00853, Paper 13, at 17-18; *Amazon.com*, IPR2019-01204, Paper 14 at 16.

To the extent that the Board considers relevant the disclosure of Bruce during prosecution of the ’098 patent, Petitioners note that the specification of the ’098 patent differs drastically from the specification of the ’740 patent which, as noted above, is a continuation-in-part. Indeed, the ’740 patent specification appears to have been completely rewritten. Accordingly, Petitioners do not accede that the ’740 patent is entitled to claim priority to the filing of the ’098 patent. Moreover, Petitioners note that the claims of the ’098 patent differ drastically from the claims of the ’740 patent. As a result, the same arguments were not presented to the patent office in the ’098 patent as were presented in the ’740 patent, and this factor

disfavors exercising the Board's discretion.

2. The Examiner Erred In Not Rejecting the '740 Patent In View of the Prior Art

Where "the first part of the *Advanced Bionics* framework is not satisfied, [the Board] need not consider the second part of the framework." *The Data Co.*, IPR2022-00135, Paper 12 at 17; *Navistar*, IPR2018-00853, Paper 13, at 18. Thus, while Petitioners do not believe there is a need to address this part of the framework, they nonetheless do so for the sake of completeness and note that—to the extent the Board determines the disclosure of Bruce in the '098 patent is relevant—the Examiner materially erred in not rejecting the '740 patent in view of Bruce.

In particular, during prosecution of the '098 patent, the Examiner found that Bruce taught: "'a plurality of flash buses;' (e.g., Flash Bus-A10 and Flash Bus-B18 in Fig. 2.)"; "'a plurality of DMA Engines coupled to at least to least two of the plurality of flash buses'"; and "'a plurality of flash devices coupled to at least two of the plurality of DMA engines.'" Ex-1011 at 3-4. This rejection led the applicant to cancel the independent claim subject to the rejection, *id*. at 9, a tacit admission of the applicability of Bruce's disclosure, and instead incorporate those elements into a dependent claim reciting a number of additional features that are not relevant to the claims of the '740 patent. *Id*. at 9-10.

Here, Bruce is relied on only for the dependent claims. Dependent claims 9-

15 of the ’740 patent recite a bus identifier, an FDE (or DMA engine) identifier, and a group identifier for flash devices. As explained above, the Examiner found that these components were disclosed by Bruce during prosecution of the ’098 patent, leading the applicant to cancel the original independent claim 1 in that patent. Accordingly, to the extent the disclosure of Bruce in the ’098 patent is relevant to the ’740 patent, the Examiner erred in failing to: 1) recognize that these identifiers were disclosed, as determined during the prosecution of the ’098 patent; 2) address Bruce; or 3) provide any rationale or explanation for why these dependent claims were allowable notwithstanding the Patent Office’s own conclusions regarding Bruce.

To be sure, this error was like caused by the fact that the applicant failed to cite Bruce to the Examiner on an IDS during prosecution of the ’740 patent, even though it cited ***other*** references from the ’098 patent during prosecution of the ’740 patent. *Compare* Ex-1001 at 1 (listing a reference to “Zilberman”) *with* Ex-1010 at 1 (citing the same reference). This additional evidence strongly warrants consideration of the prior art discussed herein.

For at least these reasons, the Board should reach the merits of the Petition and institute review of the challenged claims, particularly in light of the expert declaration of Dr. R. Jacob Baker, Sukegawa, and Bennett, which also were not before the Examiner during prosecution.

XI. MANDATORY NOTICES

A. Real Parties in Interest—37 C.F.R. § 42.8(b)(1)

The following entities are real parties in interest to this proceeding: KIOXIA Corporation and KIOXIA America, Inc. No other parties had access to or control over this Petition, and no other parties funded this Petition.

B. Related Matters—37 C.F.R. § 42.8(b)(2)

To the best of Petitioner's knowledge, the '740 patent has been or is involved in the following cases:

- *BiTMICRO LLC v. KIOXIA Am. Inc., et al.*, Case NO. 6:22-cv-00331 (W.D. Tex. 2022). This case is ongoing.
- *BiTMICRO LLC v. Intel Corp.*, Case No. 5:23-cv-00625 (N.D. Cal.), which was transferred from the District Court for the Western District of Texas, Case No. 6-22-cv-00335. This case is ongoing.

Petitioners are not aware of any other matters involving the '740 patent.

C. Lead and Back-Up Counsel—37 C.F.R. § 42.8(b)(3)

Petitioners provide the following designation of counsel.

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D. Service Information—37 C.F.R. § 42.8(b)(4)

Please address all correspondence and service to the address listed above. Petitioners consent to electronic service by email at Bracewell-IP@bracewell.com.

XII. CONCLUSION

The prior art references cited herein demonstrate that the challenged claims of the ’740 patent are anticipated and obvious. Petitioners thus request that the PTAB grant this Petition, institute *inter partes* review, and cancel the challenged claims.

Respectfully Submitted,

Dated: March 23, 2023

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24, the undersigned certifies that the foregoing Petition for *Inter Partes* Review contains 13,877 words excluding the caption, table of contents, table of authorities, table of exhibits, claim listing, mandatory notices, certificate of service, and certificate of word count. Petitioners have relied on the word count feature of the word processing system used to create this paper in making this certification.

Dated: March 23, 2023

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CERTIFICATE OF SERVICE

I hereby certify that on March 23, 2023, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review, associated exhibits, and power of attorney to be served via overnight courier upon the following counsel of record for Patent Owner per 37 CFR §§ 42.105(a) and 42.205(a).

Patent Office Counsel of Record	**Litigation Counsel of Record**
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I further certify that I served courtesy copies of the foregoing documents via electronic mail on March 23, 2023, upon Patent Owner's counsel of record as follows:

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