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16
17 **IN THE UNITED STATES DISTRICT COURT**
18 **FOR THE SOUTHERN DISTRICT OF CALIFORNIA**
19

20 BELL SEMICONDUCTOR, LLC

21 Plaintiff,

22 v.

23 NXP USA, INC.

24 Defendant.

Case No. 3:22-cv-00594-H-KSC

**SECOND AMENDED
COMPLAINT**

JURY TRIAL DEMANDED

1 Plaintiff Bell Semiconductor, LLC (“Bell Semic” or “Plaintiff”) brings this
 2 Complaint against Defendant NXP USA, Inc. (“NXP”) for infringement of U.S. Patent
 3 No. 7,007,259 (“the ’259 patent”) and U.S. Patent No. 6,436,807 (“the ’807 patent”).
 4 Plaintiff, on personal knowledge of its own acts, and on information and belief as to all
 5 others based on investigation, alleges as follows:

6 **SUMMARY OF THE ACTION**

7 1. This is a patent infringement suit relating to NXP’s unauthorized and
 8 unlicensed use of the ’259 and ’807 patents. The circuit design methodologies claimed
 9 in the ’259 and ’807 patents are used by NXP in the production of one or more of its
 10 semiconductor chips, including at least the NXP LS1043A Quad-Core Networking
 11 Processor devices (“NXP Accused Product”).

12 2. Semiconductor devices include different kinds of materials to function as
 13 intended. For example, these devices typically include both metal (*i.e.*, conductor) and
 14 insulator materials, which are deposited or otherwise processed sequentially in layers
 15 to form the final device. These layers—and the interconnects and components formed
 16 within them—have gotten much smaller over time, increasing the performance of these
 17 devices dramatically. As a result, it has become even more important to keep the layers
 18 planar as the device is being built because defects and warpage can cause fabrication
 19 issues and malfunctioning of the device. Manufacturers use a process called Chemical
 20 Mechanical Planarization/Polishing (“CMP”) to smooth out the surface of the device to
 21 prepare the device for further processing, such as deposition of another layer. This
 22 allows subsequent layers to be built and connected more easily with fewer opportunities
 23 for short circuits or other errors that render the device defective. CMP functions best
 24 when there is a certain density and variance of the same material on the surface of the
 25 chip. This is because different materials will be “polished” away at different rates,
 26 leading to erosion or dishing on the surface. To reduce this problem “dummy” material,
 27 also known as “dummy fill,” is typically inserted into low-density regions of the device
 28

1 to increase the overall uniformity of the structures on the surface of the layer and reduce
2 the density variability across the surface of the device. However, dummy fill can
3 increase capacitance if it is placed too close to signal wires, which slows the
4 transmission speed of signals and degrades the overall performance of the device.

5 3. Prior to development of the methodology described in the '807 patent, the
6 placement of dummy fill in the open areas of the interconnect layer was performed
7 based upon a predetermined set density. However, use of predetermined set densities
8 was not ideal because it often resulted in unnecessary placement of dummy fill and
9 increased capacitance. For example, if the density of an active interconnect feature was
10 high in relation to an adjacent open area, then it would not be necessary to place dummy
11 fill in the corresponding open area at the predetermined density.

12 4. Recognizing these drawbacks, as well as the importance of having a flat or
13 planarized surface on the devices, Donald Cwynar, Sudhanshu Misra, Dennis Ouma,
14 Vivek Saxena, and John Sharpe ("the '807 Inventors"), the inventors of the '807 patent,
15 set out to develop a design process that would achieve uniform density throughout the
16 interconnect layer.

17 5. The '807 Inventors ultimately conceived of a method for making the layout
18 for an interconnect layout that allows for uniform density throughout the layer and
19 facilitates planarization during manufacturing of the device. The claimed invention
20 begins by determining an active interconnect feature density for each of a plurality of
21 layout regions of the interconnect layout. Dummy fill is then added to each layout
22 region in order to obtain a desired density of active interconnect features and dummy
23 fill features in order to facilitate uniformity of planarization. In order to add dummy fill
24 in this manner, one must define a minimum dummy fill feature lateral dimension based
25 upon a dielectric layer deposition bias for a dielectric layer to be deposited over the
26 interconnect layer.

1 6. The inventions disclosed in the '807 patent provide many advantages over the
2 prior art. In particular, having a uniform density for each layout region facilitates
3 uniformity of planarization during manufacturing of the semiconductor device. *See* Ex.
4 D at 3:3–5, 5:9–12. Furthermore, adding dummy fill features to obtain a desired density
5 of active interconnect features and dummy fill features also helps ensure that dummy
6 fill features are not unnecessarily added. *Id.* at 2:63–67, 5:19–22. Avoiding unnecessary
7 dummy fill features is desirable because it decreases the parasitic capacitance of the
8 interconnect layer. *Id.* at 2:67–3:2, 5:22–24. The invention claimed in the '807 patent
9 also provides for the selective positioning of dummy fill features, which minimizes
10 parasitic capacitance. *Id.* at 5:28–33. These significant advantages are achieved through
11 the use of the patented inventions and thus the '807 patent presents significant
12 commercial value for companies like NXP.

13 7. The development of the design methodology claimed in the '259 patent
14 represented another important advancement related to the design of semiconductor
15 devices. Prior to development of the methodology described in the '259 patent, the
16 most widely implemented technology for insertion of dummy metal into a circuit design
17 required hardcoding a large “stay-away” distance between the dummy metal and clock
18 nets, which led to less space available for dummy metal insertion. This methodology
19 often made it impossible to insert enough dummy metal to meet the required minimum
20 density. The traditional dummy fill tools would often complete their run without
21 reaching the minimum density, thus requiring at least a second run of the tool for the
22 problem areas. In each problem area, the “stay-away” distance was reduced manually.
23 And if there were more than one problem area, the manufacturer would have to make
24 multiple runs of the tool, as it would have to address one problem area at a time. This
25 was an involved, iterative process that had the potential to negatively impact the
26 fabrication schedule and potentially the yield of the run, causing costs to go up.

1 8. Vikram Shrowty and Santhanakrishnan Raman (“the ’259 Inventors”), the
2 inventors of the ’259 patent, understood the drawbacks of this “stay-away” design
3 process and set out to develop a more efficient method for inserting dummy metal into
4 a circuit design. The ’259 Inventors ultimately conceived of a dummy fill procedure
5 that minimizes the negative timing impact of dummy metal on clock nets, while still
6 achieving minimum density in a single run. The claimed invention begins by identifying
7 free spaces on each layer of the circuit design suitable for dummy metal insertion as
8 dummy regions. The dummy regions are then prioritized such that the dummy regions
9 located adjacent to clock nets are filled with dummy metal last, thereby minimizing any
10 timing impact on the clock nets.

11 9. The inventions disclosed in the ’259 patent provide many advantages over the
12 prior art. In particular, they provide a simple and efficient method for dummy metal
13 insertion that minimizes the timing impact to clock nets and at the same time guarantees
14 reaching minimum density in a single pass. *See* Ex. A at 6:11–15. As mentioned above,
15 the patented invention results in the dummy regions being prioritized such that the
16 dummy regions located adjacent to clock nets are filled with dummy metal last, thereby
17 minimizing the timing impact on the clock nets. *See* Ex. A at 2:29–47. Additionally,
18 some embodiments of the patented invention further prioritize the dummy regions such
19 that the dummy regions adjacent to wider clock nets are filled with dummy metal after
20 dummy regions that are located adjacent to narrower clock nets. *See* Ex. A at 2:35–39.
21 These significant advantages are achieved through the use of the patented inventions
22 and thus the ’259 patent presents significant commercial value for companies like NXP.

23 10. Bell Semic brings this action to put a stop to NXP’s unauthorized and
24 unlicensed use of the inventions claimed in the ’259 and ’807 patents.

1 Fellow and Broadcom Fellow. He is known throughout the world as an innovator with
2 more than 300 patents to his name, and he has a sterling reputation for helping
3 semiconductor fabs improve their efficiency. Bell Semic's CEO took a brief hiatus from
4 the semiconductor world to work with Nortel Networks in the telecom industry during
5 its bankruptcy. His efforts saved the pensions of tens of thousands of Nortel retirees
6 and employees. In addition, several Bell Semic executives previously served as
7 engineers at many of these companies and were personally involved in creating the
8 ideas claimed throughout Bell Semic's extensive patent portfolio.

9 15. On information and belief, NXP has its principal place of business and
10 headquarters at 6501 William Cannon Drive West, Austin, TX 78735.

11 16. On information and belief, NXP develops, designs, and/or manufactures
12 products in the United States, including in this District, according to the '259 and '807
13 patented processes/methodologies; and/or uses the '259 and '807 patented
14 processes/methodologies in the United States, including in this District, to make
15 products; and/or distributes, markets, sells, or offers to sell in the United States and/or
16 imports products into the United States, including in this District, that were
17 manufactured or otherwise produced using the patented process. Additionally, NXP
18 introduces those products into the stream of commerce knowing that they will be sold
19 and/or used in this District and elsewhere in the United States.

20 **JURISDICTION AND VENUE**

21 17. This is an action for patent infringement arising under the Patent Laws of
22 the United States, Title 35 of the United States Code. Accordingly, this Court has
23 subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

24 18. This Court has personal jurisdiction over NXP under the laws of the State
25 of California, due at least to its substantial business in California and in this District.
26 NXP has purposefully and voluntarily availed itself of the privileges of conducting
27 business in the United States, in the State of California, and in this District by
28

continuously and systematically placing goods into the stream of commerce through an established distribution channel with the expectation that they will be purchased by consumers in this District. In the State of California and in this District, NXP, directly: (i) performs at least a portion of the infringements alleged herein; (ii) develops, designs, and/or manufactures products according to the '259 and '807 patented processes/methodologies; (iii) distributes, markets, sells, or offers to sell products formed according to the '259 and '807 patented processes/methodologies; and/or (iv) imports products formed according to the '259 and '807 patented processes/methodologies.

19. On information and belief, venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and 1400 because NXP has committed, and continues to commit, acts of infringement in this District and has a regular and established place of business in this District. For example, NXP maintains a regular and established place of business in the District at Innovation Drive, Suite 150, San Diego, CA 92128. On information and belief, NXP current employs more than 75 engineers in the San Diego area. *See* Search Results for Current NXP Employees, LinkedIn (available at https://www.linkedin.com/search/results/people/?currentCompany=%5B%221088%22%5D&geoUrn=%5B%22103918656%22%2C%2290010472%22%5D&keywords=engineer&origin=FACETED_SEARCH&sid=or8) (last visited January 6, 2022).

20. Currently, on information and belief, NXP is advertising jobs in the San Diego area. These positions include those that relate to the '259 and '807 patented technologies, such as a position for an MCU/MPU Engineering Quality and Infrastructure PM. *See* NXP Job Listings, NXP (https://nxp.wd3.myworkdayjobs.com/careers?Location_Country=bc33aa3152ec42d4995f4791a106ed09&locations=98d67abaaa8a100fa6344859d7d49369) (last visited January 6, 2022).

1 21. Venue is also convenient in this District. This is at least true because of
2 this District's close ties to this case—including the technology, relevant witnesses, and
3 sources of proof noted above—and its ability to quickly and efficiently move this case
4 to resolution.

5 22. On information and belief, Bell Semic's cause of action arises directly
6 from NXP's circuit design work and other activities in this District. Moreover, on
7 information and belief, NXP has derived substantial revenues from its infringing acts
8 occurring within the State of California and within this District.

9 **U.S. PATENT NO. 7,007,259**

10 23. Bell Semiconductor is the owner by assignment of the '259 patent. The
11 '259 patent is titled "Method for Providing Clock-Net Aware Dummy Metal Using
12 Dummy Regions."

13 24. A true and correct copy of the '259 patent is attached as Exhibit A.

14 25. The inventors of the '259 patent are Vikram Shrowty and
15 Santhanakrishnan Raman.

16 26. The application that resulted in issuance of the '259 patent was filed on
17 July 31, 2003. The '259 patent claims priority to July 31, 2003.

18 27. The '259 patent generally relates to "methods for patterning dummy metal
19 to achieve planarity for chemical-mechanical polishing of integrated circuits, and more
20 particularly to a dummy fill software tool that provides clock-net aware dummy metal
21 using dummy regions." Ex. A at 1:7–11.

22 28. The background section of the '259 patent identifies the shortcomings of
23 the prior art. More specifically, the specification describes that the prior circuit design
24 methodology was disadvantageous because it was "often impossible to insert enough
25 dummy metal into a tile to meet the required minimum density without reducing the
26 large dummy-to-clock distance." Ex. A at 2:3–10. Use of this design process meant that
27 a second run of the metal-fill tool was often required in order to meet the density
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1 requirements for all of the tiles. Ex. A at 2:10–14. Having to rerun the tool to meet the
 2 density requirements made the design process an “involved, iterative process[,]” which
 3 could “significantly impact the design schedule.” Ex. A at 2:14–18.

4 29. In light of the drawbacks of the prior art, the ’259 Inventors recognized
 5 the need to “minimize[] the negative timing impact of dummy metal on clock nets,
 6 while at the same time achieving minimum density in a single run.” Ex. A at 2:19–23.
 7 The inventions claimed in the ’259 patent addresses this need.

8 30. The ’259 patent contains three independent claims and 37 total claims,
 9 covering a method and computer readable medium for circuit design. Claim 1 reads:

10 1. A method for inserting dummy metal into a circuit design, the
 11 circuit design including a plurality of objects and clock nets, the
 12 method comprising:

13 (a) identifying free spaces on each layer of the circuit design
 14 suitable for dummy metal insertion as dummy regions, and

15 (b) prioritizing the dummy regions such that the dummy
 16 regions located adjacent to clock nets are filled with dummy
 17 metal last, thereby minimizing any timing impact on the clock
 18 nets.

19 31. This claim, as a whole, provides significant as a whole, provides
 20 significant benefits and improvements to the function of the semiconductor device, *e.g.*,
 21 minimizing the negative timing impact of dummy metal on clock nets while also
 22 reducing the opportunity for dishing and erosion that could result in inaccurate transfer
 23 of patterns during lithography, suboptimal layouts/designs, inaccurate timing, reduced
 24 signal integrity, crosstalk delay, noise issues increased probability of failure, and
 ultimately defective or underperforming devices. *See, e.g.*, Ex. A at 6:11–15.

25 32. The claims of the ’259 patent also recite inventive concepts that improve
 26 the functioning of the fabrication process, particularly as to dummy filling. The claims
 27 of the ’259 patent disclose a new and novel solution to specific problems related to
 28

1 improving semiconductor fabrication. As explained in detail above and in the '259
 2 patent specification, the claimed inventions improve upon the prior art processes by
 3 prioritizing dummy regions such that the dummy regions located adjacent to clock nets
 4 are filled with dummy metal last. This has the advantage of reducing the impact of
 5 dummy metal on signal and clock lines and increasing the efficiency, yield, and
 6 design/layout miniaturization and flexibility of the manufacturing process. The claimed
 7 inventive processes also increase performance and signal integrity, while reducing
 8 crosstalk delay, noise issues, probability of failure, and defective and/or
 9 underperforming devices.

10 **U.S. PATENT NO. 6,436,807**

11 33. Bell Semic is the owner by assignment of the '807 patent. The '807 patent
 12 is titled "Method for Making an Interconnect Layer and a Semiconductor Device
 13 Including the Same." The '807 patent issued on August 20, 2002. A true and correct
 14 copy of the '807 patent is attached as Exhibit D.

15 34. The inventors of the '807 patent are Donald Cwynar, Sudhanshu Misra,
 16 Dennis Ouma, Vivek Saxena, and John Sharpe.

17 35. The application that resulted in the issuance of the '807 patent was filed
 18 on January 18, 2000. The '807 patent claims priority to January 18, 2000.

19 36. The '807 patent generally relates to "a method for making a layout for an
 20 interconnect layer that has uniform density throughout to facilitate planarization during
 21 manufacturing of a semiconductor device." Ex. D at 2:43–46. The background section
 22 of the '807 patent identifies the shortcomings of the prior art. More specifically, the
 23 specification describes that the prior circuit design methodology was disadvantageous
 24 because it could lead to "protrusions[] in the upper surface of the dielectric material[]
 25 above respective active interconnect features[.]" *Id.* at 1:40–42. The specification states
 26 that "if pattern density variations of the active interconnect features[] are large, CMP is
 27 not adequate to sufficiently planarize the interconnect layer[.]" *Id.* at 1:67–2:2.

1 Although “[c]onventional layout algorithms” were typically used to place dummy fill
 2 features in open areas of the interconnect layer, those algorithms placed dummy metal
 3 “based upon a predetermined set density.” *Id.* at 2:17–21. Relying on “predetermined
 4 set densit[ies]” could lead to the unnecessary placement of dummy fill features, which
 5 in turn could increase the parasitic capacitance of the interconnect layer. *Id.* at 2:31–33.
 6 The specification notes that “variations in the density of the interconnect layer [could]
 7 cause deviations when the interconnect layer [was] planarized.” *Id.* at 2:35–37.

8 37. In light of the drawbacks of the prior art, the ’807 Inventors recognized “a
 9 need for making a layout for an interconnect layer that determines placement of dummy
 10 fill features for achieving a uniform density throughout the interconnect layer.” Ex. D
 11 at 2:37–40. The inventions claimed in the ’807 patent address this need.

12 38. The ’807 patent contains two independent claims and 18 total claims.
 13 Claim 1 reads:

14 1. A method for making a layout for an interconnect layer of a
 15 semiconductor device to facilitate uniformity of planarization
 16 during manufacture of the semiconductor device, the method
 17 comprising the steps of:

18 (a) determining an active interconnect feature density for each
 19 of a plurality of layout regions of the interconnect layout; and

20 (b) adding dummy fill features to each layout region to obtain
 21 a desired density of active interconnect features and dummy
 22 fill features to facilitate uniformity of planarization during
 23 manufacturing of the semiconductor device, the adding
 24 comprising defining a minimum dummy fill feature lateral
 dimension based upon a dielectric layer deposition bias for a
 dielectric layer to be deposited over the interconnect layer.

25 39. This claim, as a whole, provides significant benefits and improvements to
 26 the function of the semiconductor device, *e.g.*, uniform planarization during
 27

1 manufacturing, avoidance of adding unnecessary dummy fill features, and minimizing
2 parasitic capacitance. *See, e.g.*, Ex. D at 5:9–34.

3 40. The claims of the '807 patent also recite inventive concepts that improve
4 the functioning of the fabrication process, particularly as to dummy filling. The claims
5 of the '807 patent disclose a new and novel solution to specific problems related to
6 improving semiconductor fabrication. As explained in detail above and in the '807
7 patent specification, the claimed inventions improve upon the prior art processes by
8 determining an active interconnect feature density for each of a plurality of layout
9 regions of the interconnect layout and adding dummy fill to each layout region to obtain
10 a desired density of active interconnect features and dummy fill features to facilitate
11 uniformity of planarization. This has advantages such as avoiding the unnecessary
12 adding of dummy fill features and minimizing the parasitic capacitance of the
13 interconnect layer.

14 **COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,007,259**

15 41. Bell Semic re-alleges and incorporates by reference the allegations of the
16 foregoing paragraphs as if fully set forth herein.

17 42. The '259 patent is valid and enforceable under the United States Patent
18 Laws.

19 43. Bell Semic owns, by assignment, all right, title, and interest in and to the
20 '259 patent, including the right to collect for past damages.

21 44. A copy of the '259 patent is attached at Exhibit A.

22 45. On information and belief, NXP has and continues to directly infringe
23 pursuant to 35 U.S.C. § 271(a) one or more claims of the '259 patent by using the
24 patented methodology to design one or more semiconductor devices, including as one
25 example the NXP Accused Product, in the United States.

26 46. On information and belief, NXP employs a variety of design tools, for
27 example, Cadence, Synopsys, and/or Siemens tools, to insert dummy metal into a
28

1 circuit design (the “’259 Accused Processes”) as recited in the ’259 patent claims. As
2 one example, NXP’s Accused Processes perform a method for inserting dummy metal
3 into a circuit design, where the circuit design includes a plurality of objects and clock
4 nets as required by claim 1 of the ’259 patent. NXP does so by employing a design tool,
5 such as at least one of a Cadence, Synopsys, and/or Siemens tool, to insert dummy
6 metal into a circuit design for the NXP Accused Product. The NXP Accused Product’s
7 design includes a plurality of objects, such as cells, interconnects, signal nets, and clock
8 nets.

9 47. NXP’s ’259 Accused Processes also identify free spaces on each layer of
10 the circuit design suitable for dummy metal insertion as dummy regions. NXP does so
11 by employing a design tool, such as at least one of the Cadence, Synopsys, and/or
12 Siemens tools, to identify free spaces on each layer of the NXP Accused Product’s
13 circuit designs suitable for dummy metal insertion as dummy regions.

14 48. NXP’s ’259 Accused Processes also prioritize the dummy regions such
15 that the dummy regions located adjacent to clock nets are filled with dummy metal last,
16 thereby minimizing any timing impact on the clock nets. NXP does so by employing a
17 design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to
18 prioritize dummy regions such that those adjacent to clock nets are filled with dummy
19 metal last. For example, the ’259 Accused Processes assign a “high cost” to adding
20 metal fill near the clock nets and “lower cost” to adding metal fill near signal, power,
21 and ground nets. Assigning “cost” in this way fills dummy regions adjacent to clock
22 nets last and minimizes any timing impact on the clock nets.

23 49. An exemplary infringement analysis showing infringement of one or more
24 claims of the ’259 patent is set forth in Exhibit B. The declaration of Lloyd Linder, an
25 expert in the field of semiconductor device design, is attached at Exhibit C and further
26 describes NXP’s infringement of the ’259 patent.

1 50. NXP's '259 Accused Processes infringe and continue to infringe one or
2 more claims of the '259 patent during the pendency of the '259 patent.

3 51. On information and belief, NXP has and continues to infringe directly
4 pursuant to 35 U.S.C. § 271, *et. seq.*, either literally or under the doctrine of equivalents,
5 by using the '259 Accused Processes in violation of one or more claims of the '259
6 patent. NXP has and continues to infringe directly pursuant to 35 U.S.C. § 271, *et. seq.*,
7 either literally or under the doctrine of equivalents, by making, selling, or offering to
8 sell in the United States, or importing into the United States products manufactured or
9 otherwise produced using the '259 Accused Processes in violation of one or more
10 claims of the '259 patent.

11 52. NXP's infringement of the '259 patent is exceptional and entitles Bell
12 Semic to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C.
13 § 285.

14 53. Bell Semic has been damaged by NXP's infringement of the '259 patent
15 and will continue to be damaged unless NXP is enjoined by this Court. Bell Semic has
16 suffered and continues to suffer irreparable injury for which there is no adequate
17 remedy at law. The balance of hardships favors Bell Semic, and public interest is not
18 disserved by an injunction.

19 54. Bell Semic is entitled to recover from NXP all damages that Bell Semic
20 has sustained as a result of NXP's infringement of the '259 patent, including without
21 limitation and/or not less than a reasonable royalty.

22 **COUNT II – INFRINGEMENT OF U.S. PATENT NO. 6,436,807**

23 55. Bell Semic re-alleges and incorporates by reference the allegations of the
24 foregoing paragraphs as if fully set forth herein.

25 56. The '807 patent is valid and enforceable under the United States Patent
26 Laws.

1 57. Bell Semic owns, by assignment, all right, title, and interest in and to the
2 '807 patent, including the right to collect for past damages.

3 58. A copy of the '807 patent is attached at Exhibit D.

4 59. On information and belief, NXP has and continues to directly infringe
5 pursuant to 35 U.S.C. § 271(a) one or more claims of the '807 patent by using the
6 patented methodology to design one or more semiconductor devices, including as one
7 example the NXP Accused Product, in the United States.

8 60. On information and belief, NXP employs a variety of design tools, for
9 example, Cadence, Synopsys, and/or Siemens tools, to make a layout for an
10 interconnect layer of a semiconductor device (the "'807 Accused Processes") as recited
11 in the '807 patent claims. As one example, NXP's '807 Accused Processes perform a
12 method for making a layout for an interconnect layer of a semiconductor device, where
13 the layout facilitates uniformity of planarization during manufacture of the
14 semiconductor device as required by claim 1 of the '807 patent. NXP does so by
15 employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens
16 tool, to make a layout for the interconnect layer of its NXP Accused Product. The NXP
17 Accused Product layout facilitates uniformity of planarization during manufacture of
18 the device.

19 61. NXP's '807 Accused Processes also determine an active interconnect feature
20 density for each of a plurality of layout regions of the interconnect layout. NXP does
21 so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or
22 Siemens tools, to determine an active interconnect feature density for each of a plurality
23 of layout regions of the interconnect layout of its Accused Product.

24 62. NXP's '807 Accused Processes also add dummy fill features to each layout
25 region to obtain a desired density of active interconnect features and dummy fill
26 features to facilitate uniformity of planarization during manufacturing of the
27 semiconductor device, the adding comprising defining a minimum dummy fill feature
28

1 lateral dimension based upon a dielectric layer deposition bias for a dielectric layer to
2 be deposited over the interconnect layer.

3 63. NXP does so by employing a design tool, such as at least one of the Cadence,
4 Synopsys, and/or Siemens tools, to add dummy fill features to each layout region to
5 obtain a desired density of active interconnect features and dummy fill features to
6 facilitate uniformity of planarization during manufacturing of the semiconductor
7 device. The adding of dummy fill through the use of these design tools comprises
8 defining a minimum dummy fill feature lateral dimension based upon a dielectric layer
9 deposition bias for a dielectric layer to be deposited over the interconnect layer. An
10 exemplary infringement analysis showing infringement of one or more claims of the
11 '807 patent is set forth in Exhibit E. The declaration of Lloyd Linder, an expert in the
12 field of semiconductor device design, is attached at Exhibit C and further describes
13 NXP's infringement of the '807 patent.

14 64. NXP's '807 Accused Processes infringe and continue to infringe one or
15 more claims of the '807 patent during the pendency of the '807 patent.

16 65. On information and belief, NXP has and continues to infringe directly
17 pursuant to 35 U.S.C. § 271, *et. seq.*, either literally or under the doctrine of equivalents,
18 by using the '807 Accused Processes in violation of one or more claims of the '807
19 patent. NXP has and continues to infringe directly pursuant to 35 U.S.C. § 271, *et. seq.*,
20 either literally or under the doctrine of equivalents, by making, selling, or offering to
21 sell in the United States, or importing into the United States products manufactured or
22 otherwise produced using the '807 Accused Processes in violation of one or more
23 claims of the '807 patent.

24 66. NXP's infringement of the '807 patent is exceptional and entitles Bell Semic
25 to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

1 67. Bell Semic is entitled to recover from NXP all damages that Bell Semic has
2 sustained as a result of NXP's infringement of the '807 patent, including without
3 limitation and/or not less than a reasonable royalty.

4 **PRAYER FOR RELIEF**

5 WHEREFORE, Bell Semic respectfully requests that this Court enter judgment
6 in its favor as follows and award Bell Semic the following relief:

- 7 (a) a judgment declaring that NXP has infringed one or more claims of the
8 '259 and '807 patents in this litigation pursuant to 35 U.S.C. § 271, *et seq.*;
- 9 (b) an award of damages adequate to compensate Bell Semic for infringement
10 of the '259 and '807 patents by NXP, in an amount to be proven at trial,
11 including supplemental post-verdict damages until such time as NXP
12 ceases its infringing conduct;
- 13 (c) a permanent injunction, pursuant to 35 U.S.C. § 283, prohibiting NXP and
14 its officers, directors, employees, agents, consultants, contractors,
15 suppliers, distributors, all affiliated entities, and all others acting in privity
16 with NXP, from committing further acts of infringement with respect to
17 the '259 patent;
- 18 (d) a judgment requiring NXP to make an accounting of damages resulting
19 from NXP's infringement of the '259 and '807 patents;
- 20 (e) the costs of this action, as well as attorneys' fees as provided by 35 U.S.C.
21 § 285;
- 22 (f) pre-judgment and post-judgment interest at the maximum amount
23 permitted by law;
- 24 (g) all other relief, in law or equity, to which Bell Semic is entitled.
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1 Dated: January 31, 2023

/s/ Alan Block

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DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury trial for all issues so triable.

Dated: January 31, 2023

/s/ Alan Block

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