UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SOLAREDGE TECHNOLOGIES LTD.,
Petitioner,

v.

KOOLBRIDGE SOLAR, INC.,
Patent Owner.

Patent No. 10,784,710
Filing Date: August 14, 2017
Issue Date: September 22, 2020
Title: TRANSFORMERLESS DC TO AC CONVERTER

Inter Partes Review No.: IPR2022-00015

PETITION 3 OF 3 FOR *INTER PARTES* REVIEW UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *et seq*.

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SolarEdge Technologies Ltd ("Petitioner") petitions for *inter partes* review and cancellation of claims 1-17 of U.S. Patent No. 10,784,710 ("the '710 patent") (Ex. 1201).

I. MANDATORY NOTICES

A. 37 C.F.R. § 42.8(b)(1)&(2): Real Parties in Interest & Related Matters

The real party-in-interest is Petitioner SolarEdge Technologies Ltd. No unnamed entity is funding, controlling, or directing this Petition, or otherwise has had an opportunity to control or direct this Petition or Petitioner's participation in any resulting IPR.

The '710 patent has been asserted against SolarEdge in the District of Delaware in *Koolbridge Solar, Inc. v. SolarEdge Technologies, Inc.*, No. 1:20-cv-01374-MN (D. Del.). The earliest date of service on SolarEdge was October 12, 2020. The Patent Owner ("PO"), after having been notified of Petitioner's intent to against the '710 Patent, voluntarily dismissed its lawsuit without prejudice.

The references relied upon herein were not cited during prosecution. No arguments presented in this Petition were raised during prosecution of the '710 patent.

B. 37 C.F.R. § 42.8(b)(3)&(4): Lead & Back-Up Counsel, and Service Information

Petitioner designates counsel listed below. A power of attorney for counsel is being concurrently filed.

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II. COMPLIANCE WITH THE REQUIREMENTS FOR A PETITION FOR *INTER PARTES* REVIEW

A. Payment of Fees

The undersigned authorizes the charge of any required fees to Deposit Account No. 19-0733.

B. Grounds for Standing

Petitioner certifies that the ’710 patent is available for review and that Petitioner is not barred or estopped from requesting review challenging claims 1-17.

III. SUMMARY OF ARGUMENT

U.S. Patent No. 10,784,710 (“the ’710 patent”) describes a well-known inverter, a device that converts “direct-current” (DC) electrical power (a type of power received from a battery and/or solar panel) to “alternating-current” (AC) electrical power (a type of power used in a home). The type of inverter claimed uses multiple DC supply voltages as inputs and sums these voltages together in different combinations over a time sequence to approximate a desired AC sinusoid wave. The inverter connects the DC supply voltages to the inputs of a plurality of “reversing switches” (also called “H-bridges”). Each switch is controlled to output either: (1) its DC supply voltage, (2) its DC supply voltage with negative polarity, or (3) zero volts. This is called “ternary” control, since the switches are controlled to be placed into one of three states: the +1, -1, or 0 state. The switch outputs are connected in series, and via control of the switch states their sum output voltage gradually steps up and down to generate a sequence of voltages approximating the sine wave.

At the time the ’710 patent was filed, such inverters and the concepts behind their design and implementation were well-known. Ex. 1202, ¶¶ 61-106. Bowles (U.S. Patent No. 5,757,633, Ex. 1232), which is relied upon in this petition, is just

one example of prior art disclosing the structure of the ’710 patent. The dependent claims challenged herein add only obvious features that were also in the prior art and are taught in Iwata and additional secondary references relied on herein.

Accordingly, claims 1-17 of the ’710 patent are unpatentable and should be cancelled.

IV. OVERVIEW OF THE ’710 PATENT

A. Brief Description

Figure 1 of the ’710 patent (reproduced and annotated below) illustrates a top-level block diagram of the claimed inverter.

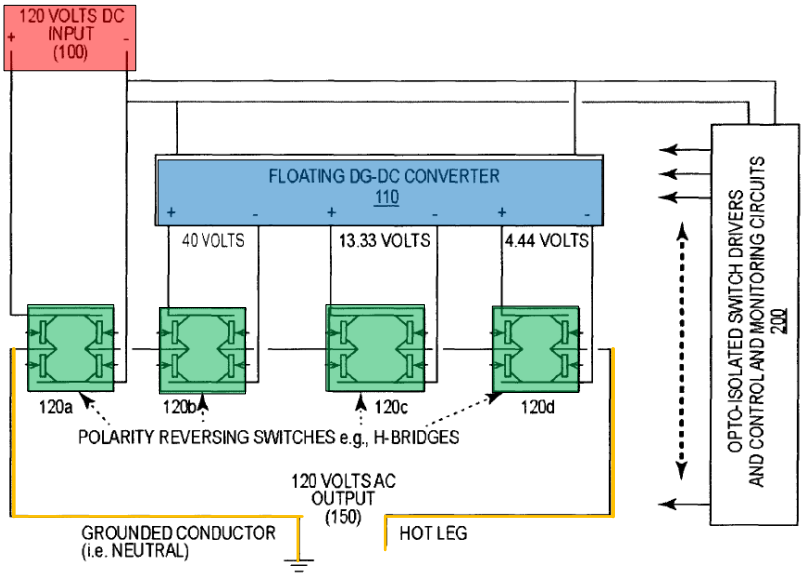


FIG. 1

Ex. 1201, Fig. 1 (annotated)

As shown above, the inverter has a 120V DC input (**red**) and a 120V AC output (**yellow**). Ex. 1201, 1:18-23, 2:41-43, 4:11-29, 5:41-52, 6:65-7:7, 7:57-65, 8:18-20; Ex. 1202 ¶¶ 93-96. This output is identified in the patent as being

"transformerless," to distinguish it from other inverters that couple the output to the grid or load through an electrical transformer. *See* Ex. 1203, pp. 294-296. The inverter also includes a bidirectional DC-DC converter (**blue**) that converts the DC input voltage to three additional DC voltages—40V, 13.33V, and 4.44V. Ex. 1201, 3:61-4:10, 6:65-7:7, 15:12-19, 16:30-32, 19:36-50. The 120V, 40V, 13.33V, and 4.44V DC voltages are respectively connected to inputs of four "polarity reversing switches" (H-bridges) 120a, 120b, 120c, and 120d (**green**). Ex. 1201, Abstract, 3:61-4:10, 5:41-52, 6:65-7:7, 7:31-42, 10:16-23, 15:17-19, 19:36-38, Fig. 2. Each switch can be controlled based on a ternary control signal to apply a multiplier of +1, -1, or 0 to the input voltage. *Id.*, Abstract, 1:18-23, 3:61-4:10, 5:41-52, 6:65-7:7, 7:23-28, 8:33-54. A control value of +1 causes the respective DC supply at the switch input to be connected with the switch output resulting in the DC supply voltage being output from the switch with a positive polarity. *Id.* A control signal of -1 causes the respective DC supply at the switch input to be connected in reverse polarity to the switch output resulting in the DC supply voltage being output from the switch with a negative polarity. *Id.* A control signal of 0 causes the respective DC supply to be bypassed resulting in 0 voltage being output from the switch. *Id.*

The outputs of the switches are connected in series, thus generating a sum voltage (**yellow**) of the positive, negative, and bypassed supply voltages, depending on the state of the ternary control signals to each of the switches. Ex. 1201, Abstract,

1:18-23, 2:41-43, 3:61-4:29, 5:41-52, 6:65-7:7, 7:31-42, 7:57-65, 8:18-20, 10:16-23, 15:17-19, 19:36-38, Fig. 2; Ex. 1202 ¶¶ 97-98. For example, for ternary valued (+1, -1, 0) signals T4, T3, T2, and T1 controlling switches 120a, 120b, 120c, and 120d, respectively, the inverter sum output voltage would be (120*T4)+(40*T3)+(13.33*T2)+(4.44*T1) volts. *Id.*, 7:23-65. If all switches output their associated positive voltage (T4, T3, T2, and T1 all equal +1), the output voltage would be 120+40+13.33+4.44=177.77 volts, but if the 4.44 volt switch changes to output 0 volts (T1=0), the summed output voltage would become 120+40+13.33=173.33 volts. *Id.*, 7:65-8:5.

Switch states can be controlled to produce a sinusoidal waveform, as seen below in Figure 12. *Id.*, Abstract, 1:18-23, 3:61-4:10, 5:41-52, 7:23-36, 7:60-8:7, 9:26-10:40.

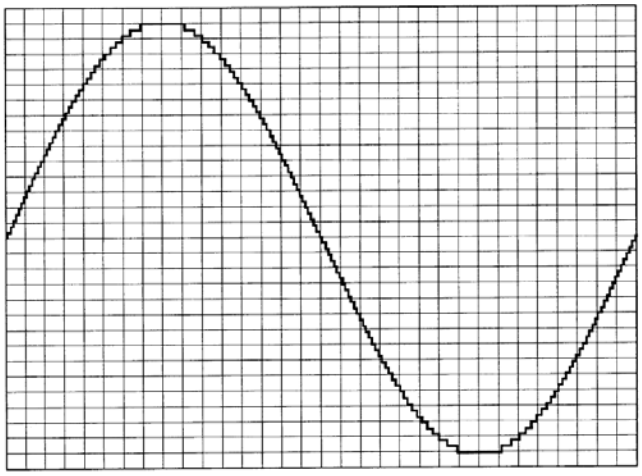


FIG. 12

Ex. 1201, Fig. 12

B. Prosecution History

The Patent application that led to the '710 patent was filed August 14, 2017. Following an initial rejection of certain claims as being anticipated by U.S. Patent No. 4,180,853 to Scroso (Ex. 1203, 188), the PO argued that Scroso lacked the required ternary control of the switches. *Id.*, 229-232. The Examiner then rejected the claims as obvious in light of Scroso in view of U.S. Patent No. 5,373,433 to Thomas, which taught ternary control of H-bridge switches in an inverter. *Id.*, 261-268. PO then amended the claims to require a "transformerless" output and also to require that the output connections of the plurality of switches are "directly" connected in series to output a sum voltage that approximates the desired waveform. *Id.*, 286. PO argued that the outputs of the H-bridge switches in Thomas were passed across transformers, and then the output of those transformers were summed to approximate the desired waveform. *Id.*, 294-296. PO did not dispute that the ternary control of H-bridge switches was taught in the art. *Id.*

The Examiner then allowed the claims, referencing the lack in the prior art of the output of ternary controlled switches being directly connected in series to output a sum voltage approximating the desired waveform. *Id.*, 312-313; Ex. 1202, ¶¶ 107-112.

C. Earliest Priority Date for the Claims

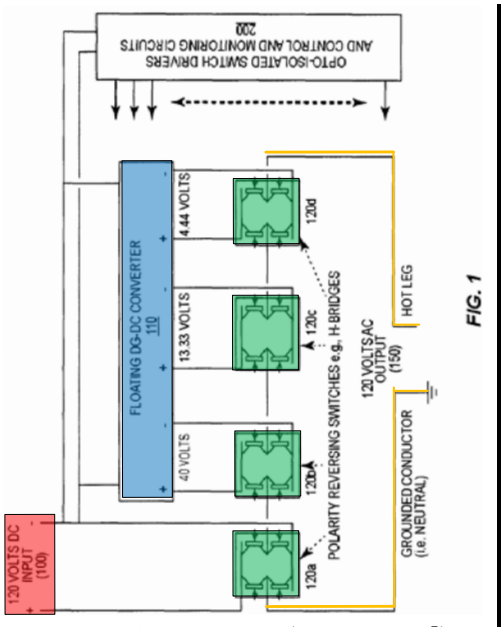
The earliest entitled possible priority date for the '710 patent claims is the filing date of U.S. Patent Application No. 13/103,070—filed May 8, 2011. Ex. 1202, ¶ 116.

V. OVERVIEW OF PRIOR ART

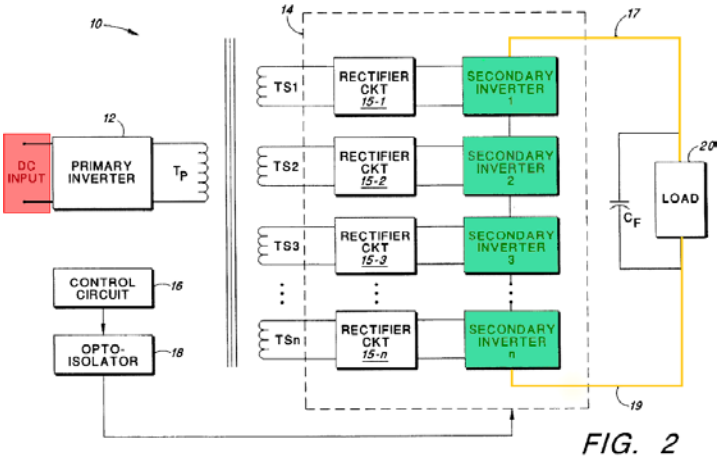
A. Bowles

Bowles (Ex. 1232) is a U.S. Patent issued on May 26, 1998, making it prior art under 35 U.S.C. § 102(b).[1] Ex. 1202, ¶ 123.

Bowles discloses a DC to AC inverter similar to that in the '710 patent. *Compare* Ex. 1201, Fig. 1 *with* Ex. 1232, Fig. 2; Ex. 1202, ¶¶ 124-125.



Ex. 1201, Fig. 1 (annotated)



Ex. 1232, Fig. 2 (annotated)

[1] Citations to 35 U.S.C. §§ 102 and 103 refer to the pre-AIA versions.

As shown above on the right, Bowles's inverter has a DC input (**red**) and AC output (**yellow**). Ex. 1232, 3:53-59, 4:29-46, 5:9-30, 8:21-30, Figs. 2-4. Primary inverter 12 receives the DC input and converts it into an intermediate AC signal. *Id.*, 3:55-60. This intermediate AC signal is transformer-coupled to a multistep inverter 14 which consists of a plurality of secondary inverters 1, 2, … n (**green**) connected in series. *Id.*, 3:61-63. As shown above in Figure 2, primary transformer winding Tp generates AC input signals on secondary transformer windings Ts1-Tsn, which are then rectified by rectifiers 15-1 … 15-n into DC signals. *Id.*, 3:63-4:3. The secondary inverters (**green**) thus have DC input voltages from the rectifier circuits. *Id.*, 3:59-4:3, Fig. 2; Ex. 1202, ¶¶ 121-26.

Bowles, again like the '710 patent, discloses that each of the secondary inverters consists of switching devices, such as transistors in an H-bridge configuration (**green**). *Compare* Ex. 1201, 8:33-40, Fig. 3 *with* Ex. 1232, 5:13-30, Fig. 3; Ex. 1202, ¶ 127.

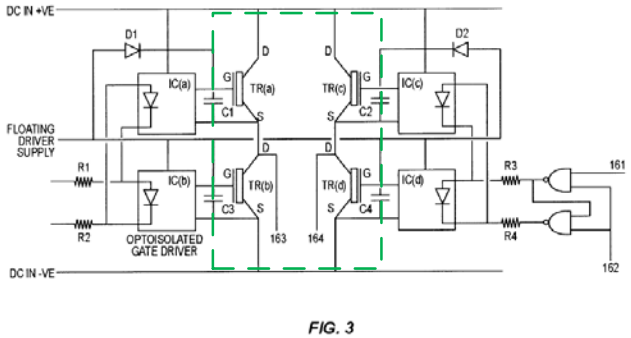


FIG. 3

Ex. 1201, Fig. 3 (annotated)

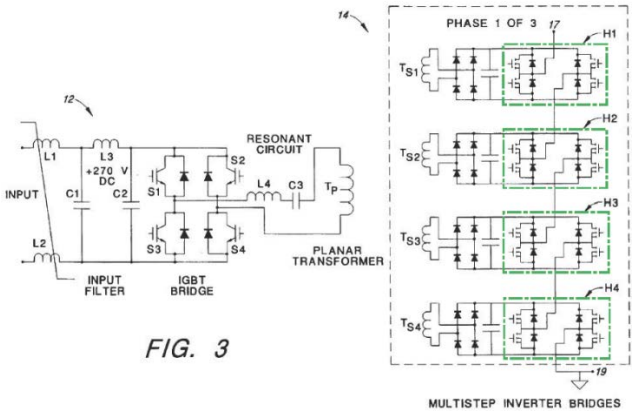


FIG. 3

Ex. 1232, Fig. 3 (annotated)

In Bowles, each secondary inverter 1, 2, … n has a DC supply voltage and is controlled like the H-bridge switches disclosed in the ’710 patent via a ternary-valued selection signal to operate in three states Bowles refers to as +V, -V, and 0V. Ex. 1232, 2:39-50, 4:10-16, 5:13-30, 10:23-48, Figs. 3-4. For example, Bowles discloses that H-bridges in secondary inverters 1, 2, 3 … n (Ex. 1232, Fig. 2) can output either a positive or negative (*i.e.*, “inverted polarity”) voltage of their respective input voltage, or a zero voltage based on whether the H-bridge’s respective switches are controlled by control signals received from a control circuit (*e.g.*, control circuit 16) to be in the +V, -V, or 0 state. Ex. 1232, 4:10-18, 4:36-46, 5:13-47, 10:23-48, Figs. 2-4; Ex. 1202, ¶ 127.

Bowles controls the states of the switching devices over time and sums the outputs of the secondary inverters to generate an AC output wave. Ex. 1232, 4:8-19, 4:29-46, 5:43-46, 6:7-23, Figs. 2-3, 8-9; Ex. 1202, ¶ 128.

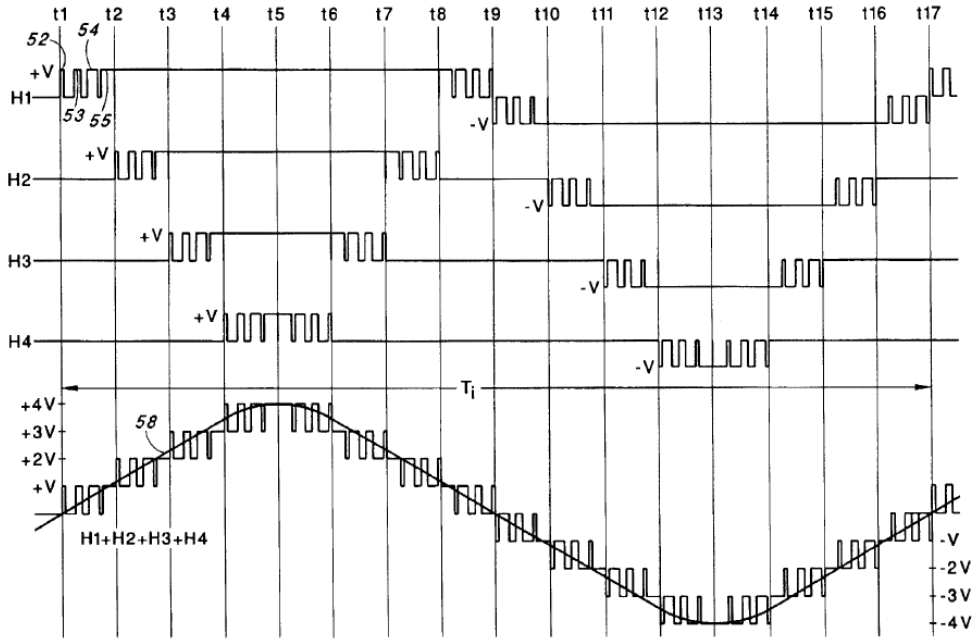


FIG. 8

Ex. 1232, Fig. 8

As illustrated in Figure 8, Bowles discloses how the ternary-valued control signal supplied by control circuit 16 can be used to control a multistep inverter having four H-bridges (H1, H2, H3 and H4) connected in series to produce "a sinusoidal-type waveform." Ex. 1232, 6:7-7:48, Figs. 2, 3, 8. The top half of Figure 8 illustrates the output voltages of each of the four H-bridge circuits H1, H2, H3, and H4 as a function of time, and the bottom half of Figure 8 illustrates the sum of the output voltages (H1+H2+H3+H4) as a function of time. Ex. 1232, 6:7-28, Fig. 8. As shown in Figure 8, the sum of the output voltages approximates a sinusoidal-type waveform. *Id.*; Ex. 1202, ¶ 128.

B. Lipo

Lipo (Ex. 1233) is a U.S. Patent issued on December 21, 1999, making it prior

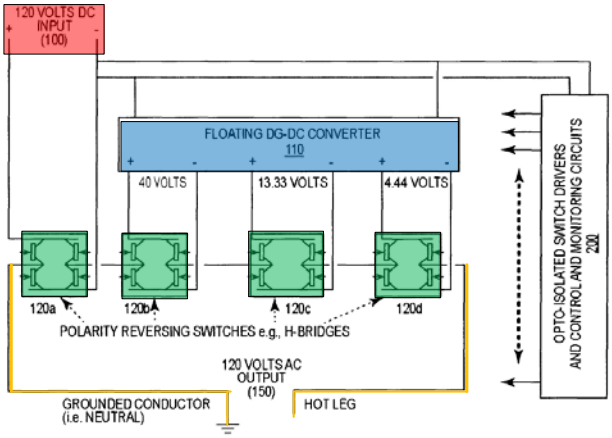
art under 35 U.S.C. § 102(b). Ex. 1202, ¶ 155.

Lipo discloses a power converter that, like Bowles, uses series connected H-bridge inverters. Ex. 1233, Abstract, 10:40-49, Fig. 5. Lipo teaches using DC source voltages associated with the plurality of H-bridge inverters that have different values. For example, Lipo discloses using DC source voltage levels varying in a binary fashion, and teaches that this allows for achieving 2^{n+1}-1 distinct voltage levels with n inverters. Ex. 1233, 7:13-30, 12:28-34. Lipo further discloses that with two inverters and DC source voltage levels varying in a binary fashion, seven voltage levels can be obtained, while a topology having equal source DC levels would require three inverters to achieve the same number of output voltage levels. Ex. 1233, 12:28-44; Ex. 1202, ¶¶ 155-156.

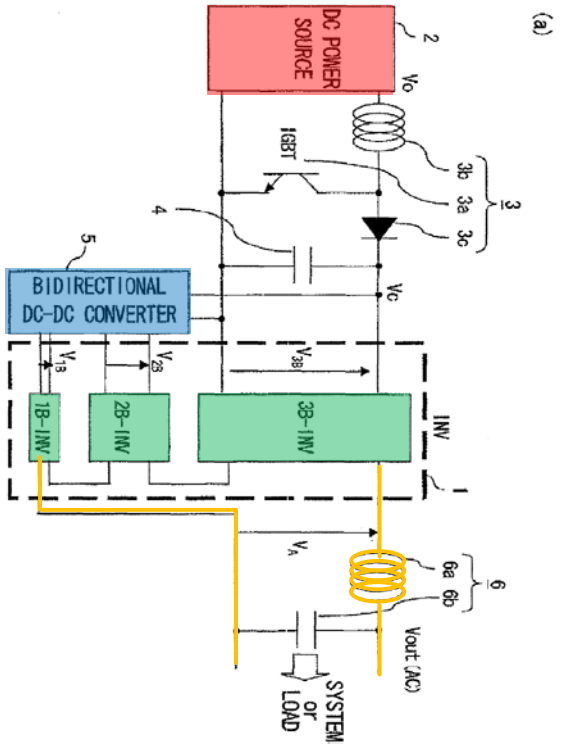
C. Iwata

Iwata (Ex. 1204) is a U.S. Patent Application Publication published on August 14, 2008, making it prior art under 35 U.S.C. § 102(b). Ex. 1202, ¶ 223.

Iwata discloses an inverter similar to that in the ’710 patent. *Compare* Ex. 1201, Fig. 1 *with* Ex. 1204, Fig, 1(a).



Ex. 1201, Fig. 1 (annotated)



Ex. 1204, Fig. 1(a) (annotated)

As shown above on the right, Iwata's inverter has a DC power source (**red**) and AC output V_A (**yellow**). Ex. 1204, Abstract, [0045], [0047]. Iwata's inverter also includes a bidirectional DC-DC converter (**blue**) that converts the DC input into a set of DC voltages V_{1B} and V_{2B}. Ex. 1204, [0048], [0077], [0084], [0097], Fig. 1(a). The single-phase inverters 1B-INV, 2B-INV and 3B-INV (**green**) have DC input voltages V_{1B} (from the DC to DC converter), V_{2B} (from the DC to DC converter), and V_{3B} (from the DC power source), respectively. Ex. 1204, [0048]-[0049], [0051]; Ex. 1202, ¶¶ 224-228.

D. **Bower**

Bower (Ex. 1211) is a U.S. Patent issued on June 15, 2004, making it prior art under 35 U.S.C. § 102(b). Ex. 1202, ¶ 186.

Bower discloses inverters that can connect to both utility grids and residences. Ex. 1211, 2:19-26, 2:32-46, 2:55-64, 10:16-29, 10:47-65, 11:11-18, 12:34-44, Figs. 1-5, 7, 11, 13. Specifically, Bower's inverters provide AC power at voltages and frequencies used in standard households, such as "at 120V or any other single-phase voltage with one terminal grounded that is intended to be connected to the neutral conductor in the house." *Id.*, 10:16-29; Ex. 1202, ¶ 187.

Bower also teaches different methods for connecting an inverter with a two-terminal output to an electrical grid having two hot input terminals and a single neutral terminal in accordance with the NEC 2008 standards. Ex. 1211, 6:66-7:2, 10:16-11:18, Figs. 3-7, 11. For example, Bower teaches the AC output of these inverters can provide AC power across a hot terminal and a neutral terminal. *Id.*, 10:21-29, 11:11-18, Figs. 3-7, 11; Ex. 1202, ¶¶ 188-189.

E. Mori '265

Mori '265 (Ex. 1216, certified translation Ex. 1207) is a PCT Published International Application published on July 22, 2010, making it prior art under 35 U.S.C. § 102(a). Ex. 1202, ¶ 196.

Mori '265 teaches a power converter that combines the outputs of a plurality of inverters to generate a desired AC output waveform. Ex. 1207, [0047], Fig. 14. Like Bowles and Iwata, each inverter has transistors in an H-bridge configuration and outputs one of three levels (+V, -V, or 0) based on the combinations of the ON

and OFF states of the transistors in the inverters. Ex. 1207, [0011], [0028], [0032], [0047], Figs. 11, 14. Mori '265 explains the ternary control signals that are generated to place the switches into either a +1, -1, or 0 state. Ex. 1207, [0011], [0028], [0032], [0048]-[0050], Fig. 11; Ex. 1202, ¶ 197. Gate driving signals which are controlled by a pair of binary bits are sent to switching device gates of each of the inverters. Ex. 1207, [0031], [0050]. There are four possible patterns for the binary values of these two bits (*i.e.*, 00, 01, 10, and 11) and each such pattern places an H-bridge switch into one of its three possible states. Ex. 1207, [0031]-[0032], [0050]. More particularly, one combination places a switch into the +1 state, another places the switch into the -1 state, and the remaining two combinations place the switch into the 0 state. Ex. 1207, [0032], [0050]; Ex. 1202, ¶ 198.

F. **Flanagan**

Flanagan (Ex. 1208) is a U.S. Patent issued on March 21, 1995, making it prior art under 35 U.S.C. § 102(b). Ex. 1202, ¶ 210.

Flanagan teaches a programmed PWM controller for controlling an inverter comprising three pairs of inverter switches. Ex. 1208, Abstract, 4:64-68. Flanagan's controller outputs a sequence of gating signals to the control line to generate the desired inverter output. *Id.*, 5:18-29. Specifically, the memory of the controller stores a series of drive data words, each of which includes both a driveword for controlling the switch states of the inverter and a drivetime word providing timing

information within the PWM sequence. *Id.*, 5:29-34; Ex. 1202, ¶ 211. The first driveword and corresponding drivetime word are retrieved from the memory and output onto data buses. Ex. 1208, 5:55-6:35. When the address counter is incremented, the next driveword and corresponding drivetime word in the sequence are retrieved from the memory and output onto the data buses. *Id*. This procedure is repeated for each drive data word in the sequence to control the inverter to produce the desired output voltages at the desired times. *Id.*, 6:35-50; Ex. 1202, ¶ 211.

G. Tracy

Tracy (Ex. 1209) is a U.S. Patent issued on August 8, 2006, making it prior art under 35 U.S.C. § 102(b). Ex. 1202, ¶ 247.

Tracy teaches a power converter apparatus that can include, as shown below, a battery (**red**) as an uninterruptable power supply (UPS) as the DC power source for an inverter. Ex. 1209, 1:6-47, 4:50-59, 5:1-6, 5:41-52, 6:46-49. As Tracy states, the use of batteries as the DC power source for inverters in the context of UPSs were commonly used to provide auxiliary power for electronic computer systems, telecommunications systems, and medical equipment. Ex. 1209, 1:10-16; Ex. 1202, ¶ 248.

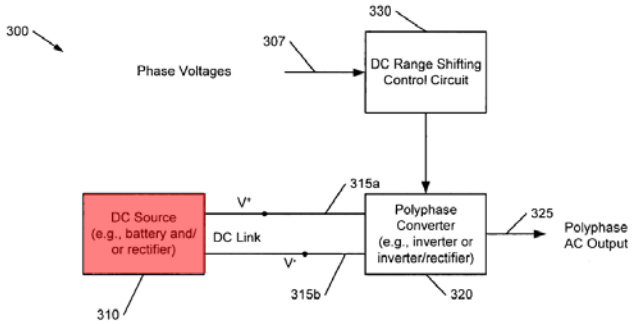


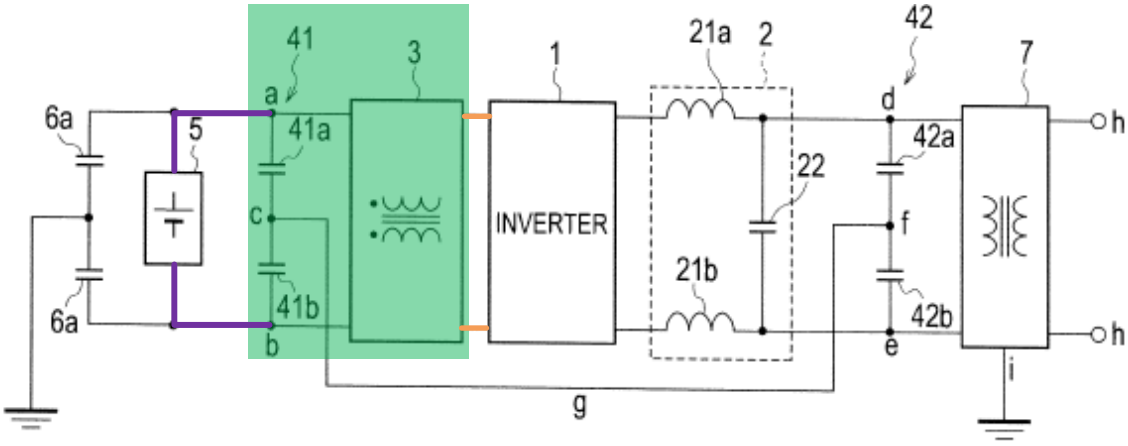
FIG. 3

Ex. 1209, Fig. 3 (annotated)

H. **Koyama**

Koyama (Ex. 1213) is a PCT patent application publication first published on May 20, 2010. Koyama is prior art under 35 U.S.C. § 102(a). Ex. 1202, ¶ 263.

As shown in Figure 5 reproduced below, Koyama discloses a common mode filter (**green**), including a first common mode choke coil 3a and capacitors 41a, 41b, connected between DC input terminals of an inverter 1 (**orange**) and positive and negative terminals of DC power source 5 (**purple**). Ex. 1213, 1:54-2:17, 2:45-53, 5:6-26, 5:50-6:4, 6:40-62, Figs. 1, 5; Ex. 1202, ¶ 264.



Ex. 1213, Fig. 5 (annotated)

I. Phadke

Phadke (Ex. 1215) is a U.S. Patent based on an application filed on December 22, 2010, making it prior art under 35 U.S.C. § 102(e). Ex. 1202, ¶ 302.

Phadke discloses DC to DC converters (**blue**) attached between photovoltaic (PV) arrays (**red**) to provide power sources for an inverter (**green**). Ex. 1215, 1:14-16, 3:57-65, 4:32-41, 4:66-5:6; Ex. 1202, ¶ 303.

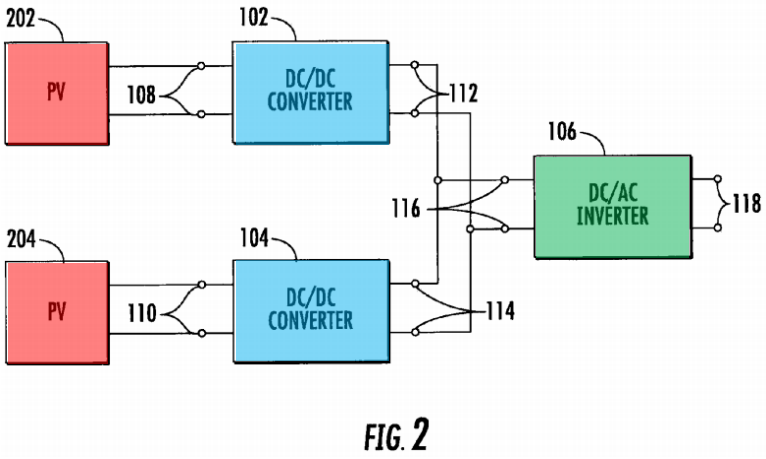


FIG. 2

Ex. 1215, Fig. 2 (annotated)

Within the DC to DC converters, Phadke discloses the use of two stages with a switch and a resistor inserted in parallel between the two stages, as shown in Figure 6 below:

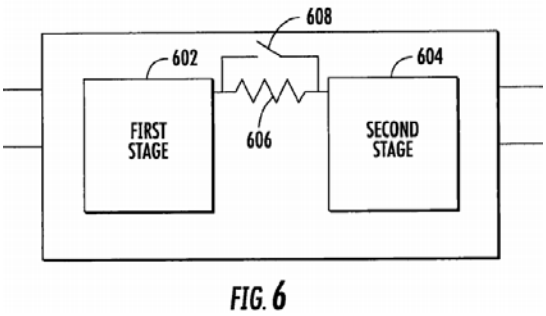


FIG. 6

Ex. 1215, Fig. 6

To protect the circuit during startup, Phadke discloses that the switch is held open so that the resister provides a high resistance path limiting the amount of current flowing to the second stage. Ex. 1215, 7:1-8, 7:19-27. Once a certain threshold of current or voltage is reached, the switch 608 is closed, thus removing any impedance between the two stages by effectively shorting the resistor. Ex. 1215, 7:8-11; Ex. 1202, ¶¶ 304-305.

J. Ahmed

Ahmed (Ex. 1212) is an article published and available to the public in 2007, making it prior art under 35 U.S.C. § 102(b). Ex. 1202, ¶ 274; Ex. 1239, ¶¶ 41-65.

Ahmed discloses a design method for low pass LC filters to reduce switching frequency harmonics of inverters. Ex. 1212, 1, Fig. 1 (reproduced below).

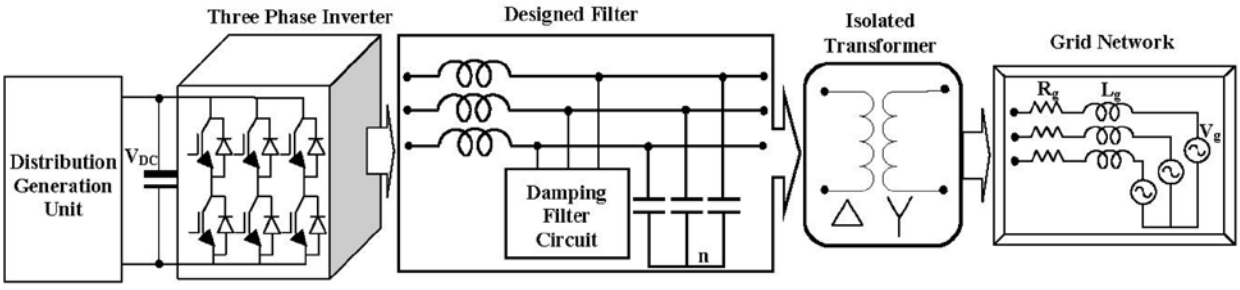


Fig. 1. Block diagram of the proposed interfacing system

Ahmed identifies the problem in such filters of resonance between the inductor (L) and capacitor (C) components, and provides a solution to reduce resonance by adding a damping circuit, which includes a resistor with an additional capacitor and/or inductor. Ex. 1212, 7-8, Figs. 13-15; Ex. 1202, ¶¶ 275-276.

F. Nishimura

Nishimura (Ex. 1214) is a U.S. Patent Application Publication first published on April 2, 2009, making it prior art under 35 U.S.C. § 102(b). Ex. 1202, ¶ 255.

Nishimura provides a structure for a bidirectional DC-DC converter similar to the structure of the ’710 patent, including center-tapped windings (**red**) that are connected to the positive terminal of the DC input or output (**blue**) with ends of the windings connected to the drains of N-Type MOSFET pairs (**green**):

FIG.4

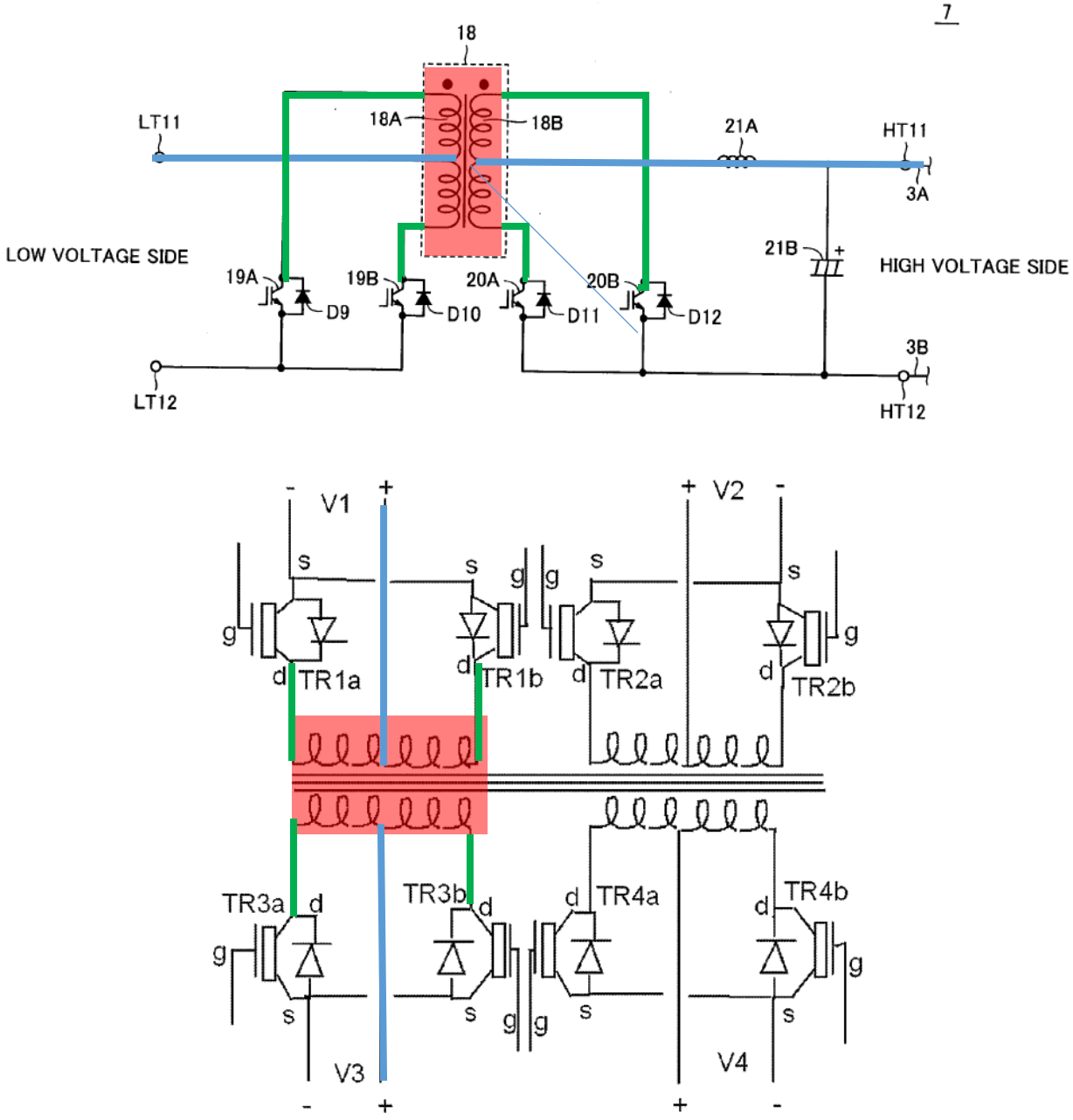


FIGURE 2: BIDIRECTIONAL DC-DC CONVERTER

Ex. 1214, [0091]-[0101], Fig. 4 (annotated, top); Ex. 1201, 18:34-47, Fig. 2. (annotated, bottom); Ex. 1202, ¶ 256.

VI. IDENTIFICATION OF CHALLENGE PURSUANT TO 37 C.F.R. § 42.104(b)

A. Claims for Which Review is Requested and Grounds on Which Challenge Is Based

Petitioner requests review of claims 1–17 on the following grounds and references. ; Ex. 1202 ¶¶ 118-119.

Ground(s)	References	Basis	Claims Challenged
A	Bowles	§ 102	1, 7, 8
B	Bowles-Lipo	§ 103(a)	2, 4-5, 12
C	Bowles-Bower	§ 103(a)	3
D	Bowles-Mori ‘265	§ 103(a)	6
E	Bowles-Flanagan	§ 103(a)	9
F	Bowles-Iwata	§ 103(a)	10-11
G	Bowles-Iwata-Tracy	§ 103(a)	10-11
H, I	Bowles-Iwata and Bowles-Iwata-Tracy, both in view of Nishimura	§ 103(a)	10-11
J, K	Bowles-Iwata and Bowles-Iwata-Tracy, both in view of Koyama	§ 103(a)	13
L, M	Bowles-Lipo-Iwata-Koyama and Bowles-Lipo-Iwata-Tracy-Koyama, both in view of Ahmed	§ 103(a)	14-15
N	Bowles-Iwata-Ahmed	§ 103(a)	16
O	Bowles-Phadke	§ 103(a)	17

None of the prior art listed above was considered during prosecution. Ex. 1201, cover.

B. Level of Ordinary Skill

A person of ordinary skill in the art ("POSITA") would have had a bachelor's degree in electrical engineering, or a similar discipline and at least 3 years of design experience with power electronics, including experience designing power converters. Ex. 1202, ¶¶ 20-23.

C. Claim Construction

All claim terms herein should be given their ordinary and customary meaning.. Further, Petitioner does not contend for this IPR that the claims include any means-plus-function limitations but identifies the following claim elements, including their respective structures, in the case the Board finds them to be means-plus-function elements. 37 C.F.R. § 42.104(b)(3).

1. "a switch selection signal generator operative to"

To the extent the Board finds this is a means-plus-function term in claims 7-9, the function is to produce ternary-valued selection signals as set forth in claims 7-9 respectively, and the corresponding structure is controller 200 illustrated in Figure 1 or controller 202-2 illustrated in Figure 11, which include a microcontroller, microprocessor, or an equivalent structure that send the signals to switch driving circuits. Ex. 1201, 12:54-56, 13:21-27, 13:33-47, 15:39-41, 16:48-51, 16:61-63, Figs. 1, 11; Ex. 1202, ¶¶ 120-121.

2. "bi-directional DC-DC conversion circuitry operative to"

To the extent the Board finds this is a means-plus-function term in claims 10 and 11, the function is to derive the lower voltage values (claim 10) or lower mean power (claim 11) from the battery and the corresponding structure is windings on one or more transformers which have turn ratios in proportion to the voltage ratios being output wherein each winding corresponding to the lower voltage values or lower mean power is center tapped, or an equivalent structure. *Id.*, 16:30-32, 19:41-48, 20:9-28, Fig. 2; Ex. 1202, ¶ 122.

VII. SPECIFIC GROUNDS FOR UNPATENTABILITY

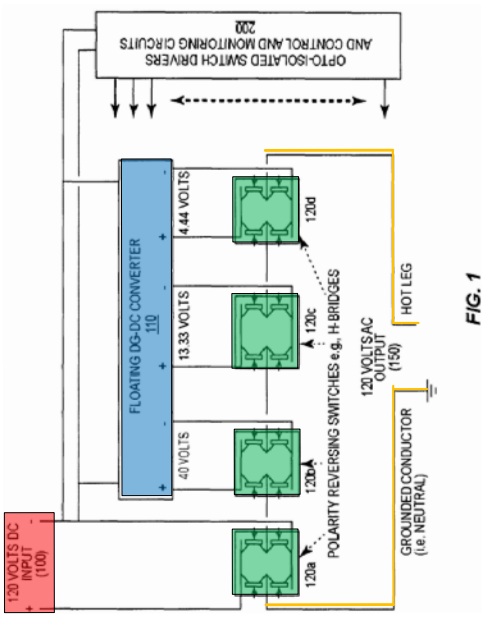
A. Ground A: Claims 1, 7 and 8 are Anticipated by Bowles

1. Independent Claim 1

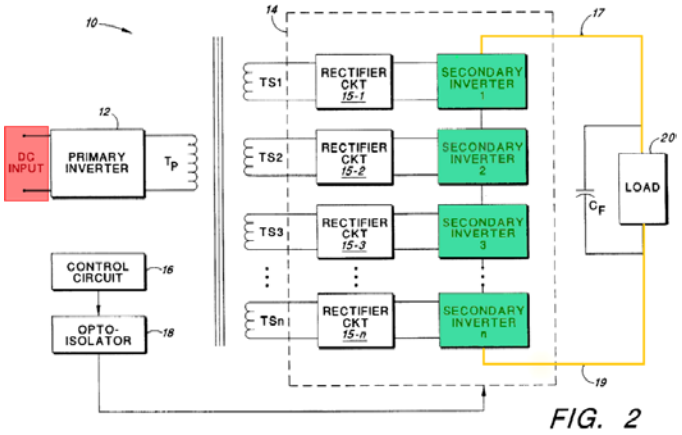
Elements [1A]-[1F] are anticipated by Bowles. Ex. 1202, ¶¶ 129-146, 30-33.

a. [1A]: "A DC to AC converter having"

Bowles discloses a DC to AC inverter similar to that in the '710 patent with an output that approximates a sinewave by summing the output of a set of series-connected single-phase inverters, each single-phase inverter consisting of a switching circuit. *Compare* Ex. 1201, 6:65-7:7, Fig. 1 *with* Ex. 1232, 2:26-67, 4:36-43, 5:9-30, 6:7-28, 8:21-30, Figs. 2, 8.



Ex. 1201, Fig. 1 (annotated)

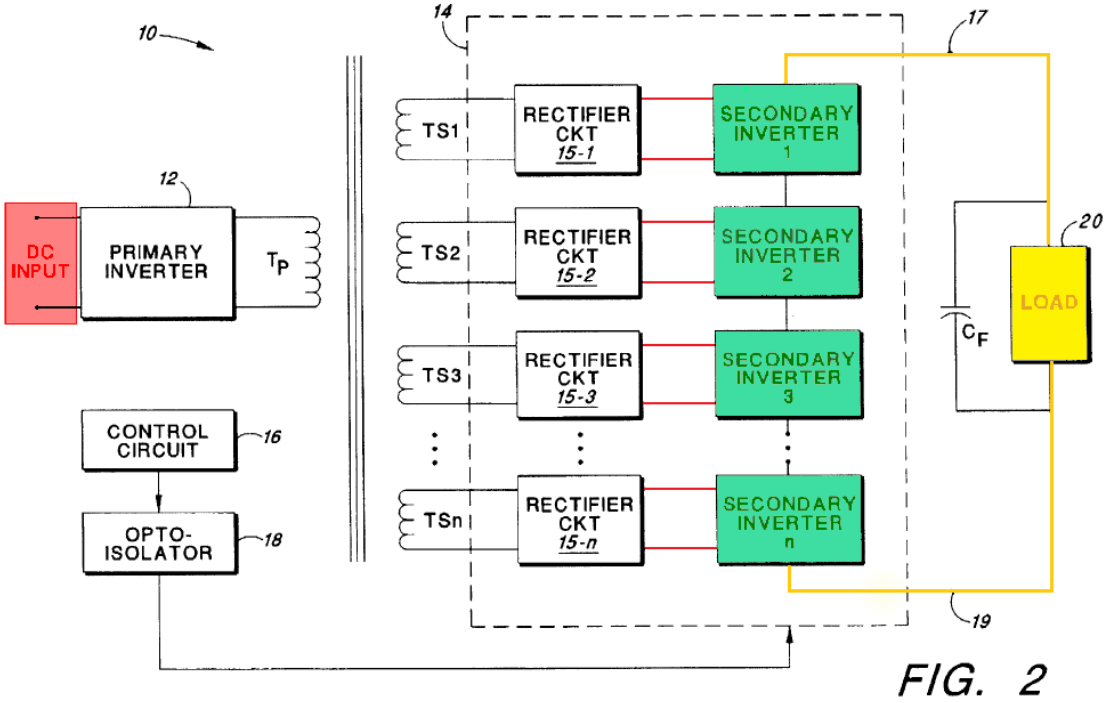


Ex. 1232, Fig. 2 (annotated)

Thus, Bowles discloses [1A]. Ex. 1202, ¶ 131.

b. [1B] "a transformerless output, and operative to convert DC power to an AC power having a desired voltage and waveform,"

Bowles's multistep inverter apparatus discloses a DC to AC converter that is operative to convert DC power [DC input (**red**)] to an AC power [AC output on terminals 17 and 19 (**yellow**)] as shown in Figure 2 below. Ex. 1232, 4:29-46, 5:9-30, 8:21-30, Figs. 2-4; Ex. 1202, ¶ 132. Bowles's multistep inverter outputs a desired voltage and waveform by generating different voltage levels through different combinations of the outputs of secondary inverters 1, 2, 3, … n, to "produce a sinusoidal-type waveform" as shown in Figure 8. *See, e.g.*, Ex. 1232, 2:60-67, 4:36-43, 6:7-28, 8:21-30, Figs. 2-4, 8-9; Ex. 1202, ¶ 132.



Ex. 1232, Fig. 2 (annotated)

Bowles's multistep inverter, shown above, does not include a transformer between the series connected secondary inverters 1, 2, 3 …n (*see* H-bridges H1-H4 at Ex. 1232, Fig. 4) and the output terminals 17 and 19, and thus the output is "transformerless." *Compare* Ex. 1232, 4:29-34, 5:9-30, Figs. 2-4 (output terminals 17 and 19) *with* Ex. 1201, 7:60-61, 2:44-47 (admitting transformerless inverters were known in the prior art), Fig. 1 ("120VOLTS AC OUTPUT (150)"); Ex. 1202, ¶ 133.

Thus, Bowles discloses [1B]. Ex. 1202, ¶¶ 132-133.

c. [1C]: "and to output the AC power between hot and neutral output terminals,"

A PHOSITA would have understood that a "neutral output terminal" includes a grounded output terminal. *Id.*, ¶ 134; Ex. 1201, 6:65-7:7, Fig. 1.

The AC power signal in Bowles is output between terminals 17 and 19 of multistep inverter 14. Ex. 1232, 4:29-34, Figs. 2-3. In one example, the signal is applied across load 20. *Id*. In addition, Bowles provides a "circuit level diagram" in which output terminal 19 is grounded (shown in **yellow** in Figure 3 below). *Id.*, 4:29-34, 5:13-30, Fig. 3; Ex. 1202, ¶ 135. Bowles thus discloses that the AC power signal is output between output terminal 17 and grounded output terminal 19 (the claimed "to output the AC power between hot and neutral output terminals"). Ex. 1202, ¶ 135.

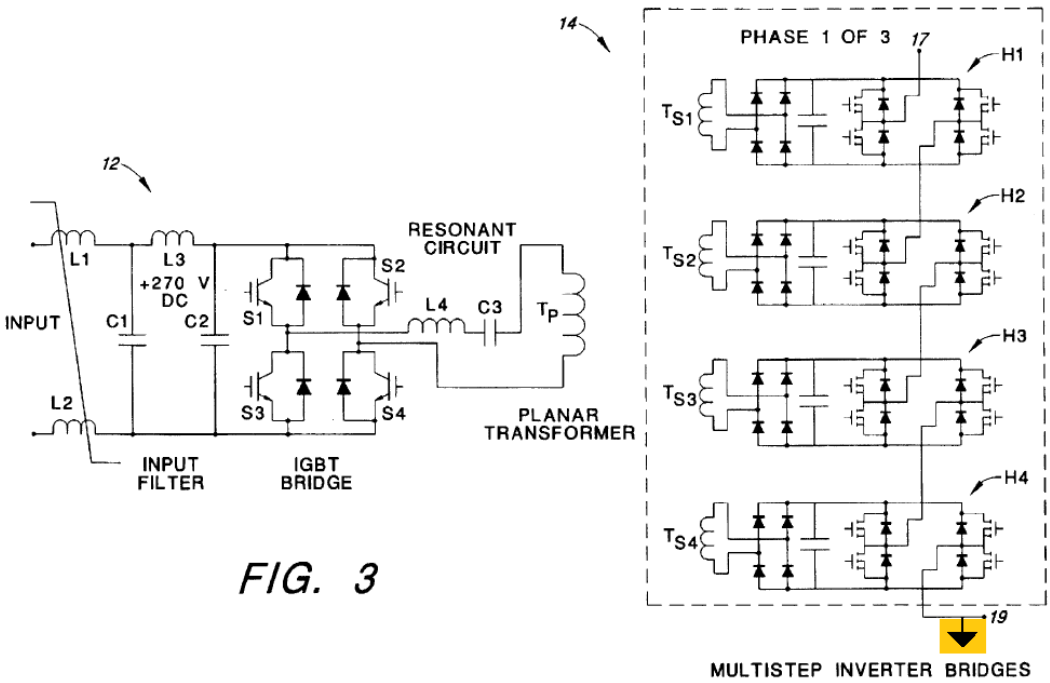
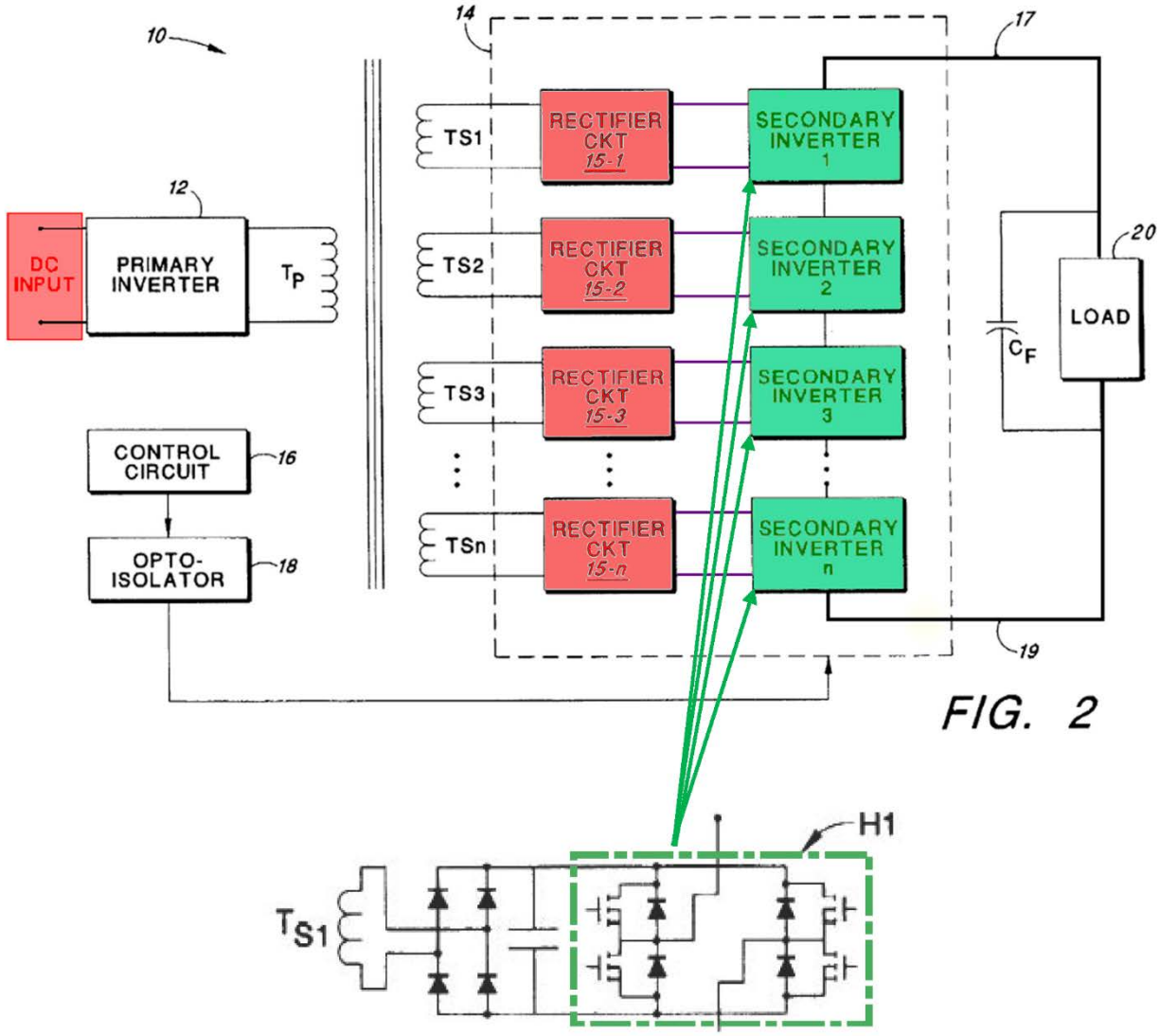


FIG. 3

Ex. 1232, Fig. 3 (annotated)

d. [1D]: "the DC to AC converter comprising: a plurality of controlled switches, each having a power input connection operative to accept DC power from an associated DC power source at an associated DC voltage, and"

Bowles's DC to AC multistep inverter includes a plurality of controlled switches (**green**), each having a power input connection (**purple**) operative to accept DC power from an associated DC power source (**red**) at an associated DC voltage. Ex. 1202, ¶ 136; Ex. 1232, 4:47-49, 5:9-30, Figs. 2-3.



Ex. 1232, Fig. 2, Excerpt of Fig. 3 (annotated)

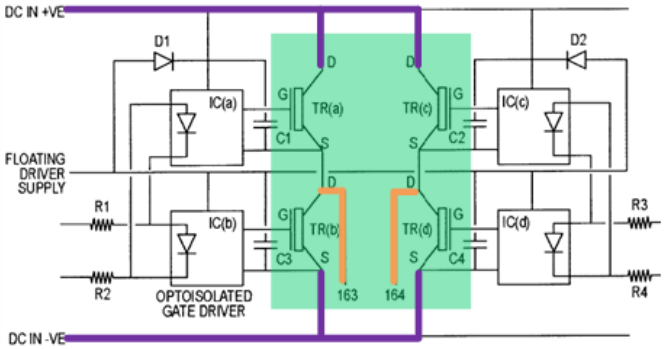
As highlighted in Figures 2-3 above, multistep inverter 14 comprises "a plurality of controlled switches" (**green**), included in secondary inverters 1, 2, 3 … n. Ex. 1232, 4:8-19, 5:9-26. Each switch includes a plurality of switching devices arranged in an H-bridge switch like those disclosed in the '710 patent as shown in the comparison figures below. *Id.*, 5:9-26, Fig. 3; Ex. 1202, ¶ 137. As will be discussed in more detail in relation to Element [1E] below, these switches are controlled to produce positive, negative, or zero voltages from their respective DC power sources. Ex. 1232, 4:8-16, 5:13-47, Figs. 3-4; Ex. 1202, ¶ 137, 140-142.

Each of these switches have input connections (highlighted in **purple** above) connected to and receiving power from an associated DC power source (highlighted in **red** above), which is a rectifier circuit 15-1, 15-2, 15-3, … 15-n connected to each secondary inverter. Ex. 1232, 4:47-49, 5:9-26, Figs. 2-3; Ex. 1202, ¶ 138. In Bowles's embodiment from Figures 2-3, for example, outputs from rectifying circuits 15-1, 15-2, 15-3, … 15-n are the DC power source voltage inputs, respectively, for the plurality of switches included in secondary inverters 1, 2, 3 … n. Ex. 1232, 3:66-4:3, 4:47-49, 5:9-26, 5:47-51, Figs. 2-3; Ex. 1202, ¶ 138.

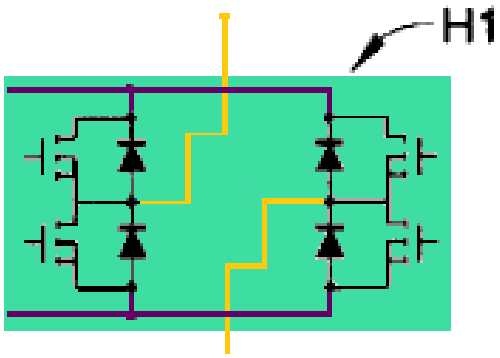
Thus, Bowles discloses [1D]. Ex. 1202, ¶¶ 136-139.

e. [1E]: "each controlled switch further having a power output connection operative to output a selected one of: (a) the associated DC voltage, (b) the associated DC voltage having an inverted polarity, and (c) zero voltage, in response to an associated ternary-valued selection signal representing the multiplier values +1, −1, or 0 respectively,"

Bowles's inverters are arranged and controlled like the H-bridge switches disclosed in the '710 patent (as shown in the comparison figures below) via a ternary-valued selection signal to operate in three states Bowles refers to as +V, -V, and 0V. Ex. 1232, 2:39-50, 4:10-16, 5:13-30, 10:23-48, Figs. 3-4; Ex. 1201, 7:23-28, 8:33-54, 9:58-64, 11:5-13, 11:26-35, Fig. 3; Ex. 1202, ¶ 140.



Ex. 1201, Fig. 3 (annotated)



Ex. 1232, Excerpt of Fig. 3 (annotated)

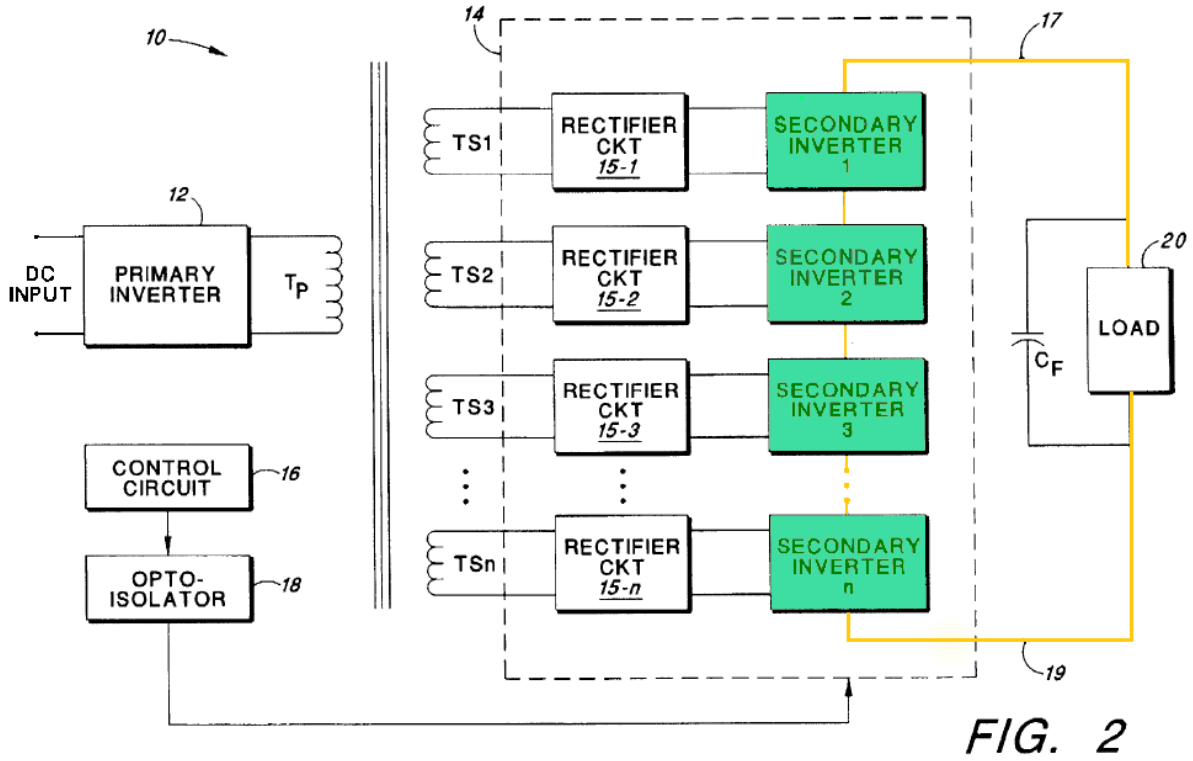
For example, Bowles discloses that H-bridges in secondary inverters 1, 2, 3 … n (Ex. 1232, Fig. 2) can output either a positive or negative (*i.e.*, "inverted polarity") voltage of their respective input voltage, or a zero voltage based on whether the H-bridges's respective switches are controlled by control signals received from a control circuit (*e.g.*, control circuit 16) to be in the +V, -V, or 0 state. Ex. 1232, 4:10-18, 4:36-46, 5:13-47, 10:23-48, Figs. 2-4; Ex. 1202, ¶ 141.

Thus, Bowles's switches have a power output connection operative to output a selected one of: "(a) the associated DC voltage" in response to a control signal received from a control circuit (the claimed "associated ternary-valued selection signal representing the multiplier value[] +1"); "(b) the associated DC voltage having an inverted polarity" in response to a control signal received from a control circuit (the claimed "associated ternary-valued selection signal representing the multiplier value[] … -1"), and "(c) zero voltage" in response to a control signal received from a control circuit (the claimed "associated ternary-valued selection signal representing the multiplier value[] … 0"). Ex. 1232, 4:10-16, 5:20-47, 10:23-48, Figs. 2-4; Ex. 1202, ¶ 142. This is described in more detail with an example from Figure 8 of Bowles, immediately below. Section VII.A.1.f, *infra*.

Thus, Bowles discloses [1E]. Ex. 1202, ¶¶ 140-142.

f. [1F]: "the power output connections of the plurality of switches being directly connected in series to output a sum voltage approximating the desired AC output voltage and waveform."

The outputs of Bowles's switches (**green**) are directly connected in series (**yellow**). Ex. 1232, 4:8-19, 4:36-46, 5:43-46, 6:7-23, Figs. 2-3, 8-9; Ex. 1202, ¶ 143.



Ex. 1232, Fig. 2 (annotated)

Bowles's switches are directly connected in series to sum the outputs of secondary inverters 1, 2, 3 … n at output terminal 17 in Figure 2. Ex. 1232, 4:8-19, 4:29-46, 5:43-46, 6:7-23, Figs. 2-3, 8-9; Ex. 1202, ¶ 144. As discussed above for [1E], the Bowles secondary inverters are each controlled to output either an associated DC voltage, or the inverted polarity of that associated DC voltage, or a zero voltage in response to a control signal received from control circuit 16 that represents a multiplier value of +1, -1, or 0. Section VII.A.1.e., *supra*.

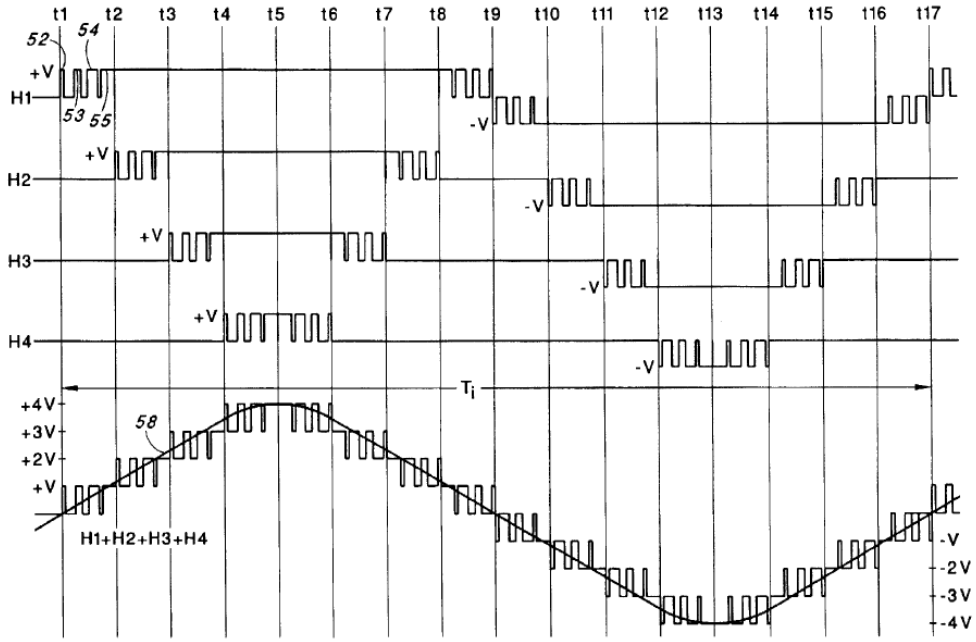


FIG. 8

Ex. 1232, Fig. 8

In one example illustrated in Figure 8 (shown above), the ternary-valued control signal supplied by control circuit 16 can be used to control a multistep inverter having four H-bridges (H1, H2, H3 and H4) connected in series to produce "a sinusoidal-type waveform." Ex. 1232, 6:7-7:48, Fig. 8. The top half of Figure 8 illustrates the output voltages of each of the four H-bridge circuits H1, H2, H3 and H4 over time, and the bottom half of Figure 8 illustrates the sum of the output voltages (H1+H2+H3+H4) over time. *Id.*, 6:7-28, Fig. 8. As shown in Figure 8, the sum of the output voltages approximates a sinusoidal-type waveform. *Id.*; Ex. 1202, ¶ 145.

Thus, Bowles discloses [1F] and anticipates claim 1. Ex. 1202, ¶¶ 143-146.

2. Claims 7 and 8

Claims 7 and 8 each depend from claim 1 and require "a switch selection signal generator operative to produce the ternary-valued selection signals, the switch selection signal generator being configured to produce [] sets of switch selection signals." Ex. 1201, claims 7, 8.

As described above in Section VII.A.1.e, Bowles discloses that the DC to AC converter of claim 1 uses control signals (the claimed "ternary-valued selection signals") to control a plurality or set of H-bridge switches such that each H-bridge switch provides three output voltage states. Section VII.A.1.e, *supra*. Bowles discloses that the control signals are produced by control circuit 16 illustrated in Figure 2. Ex. 1232, 2:50-3:5, 4:8-46, 5:13-42, 8:60-9:8, Figs. 2, 8; Ex. 1202, ¶ 149. As described above in Section VII.A.1.f, Bowles discloses an example in which the control signals produced by control circuit 16 can be used to control an inverter having four H-bridge switches to produce a sinusoidal-type waveform (the claimed "a switch selection signal generator operative to produce the ternary-valued selection signals, the switch selection signal generator being configured to produce [] sets of switch selection signals"). Section VII.A.1.f, *supra*; Ex. 1232, 2:50-3:5, 4:8-46, 5:13-42, 8:60-9:8, Figs. 2, 8.

Claim 7 further requires the sets of switch selection signals to be produced "at given time instants, such that the sum voltage output is momentarily the best

approximation to the instantaneous voltage values of the desired waveform at the given instants." Ex. 1201, claim 7. Claim 8 further requires the sets of switch selection signals to be "sequential" and the generator to be "configured to produce each new set of switch selection signals at a time instant at which the new set of switch selection signals would cause the sum voltage to be a better approximation to an instantaneous voltage value of the desired waveform at that time instant than the immediately previously output set of switch selection signals." *Id.*, claim 8.

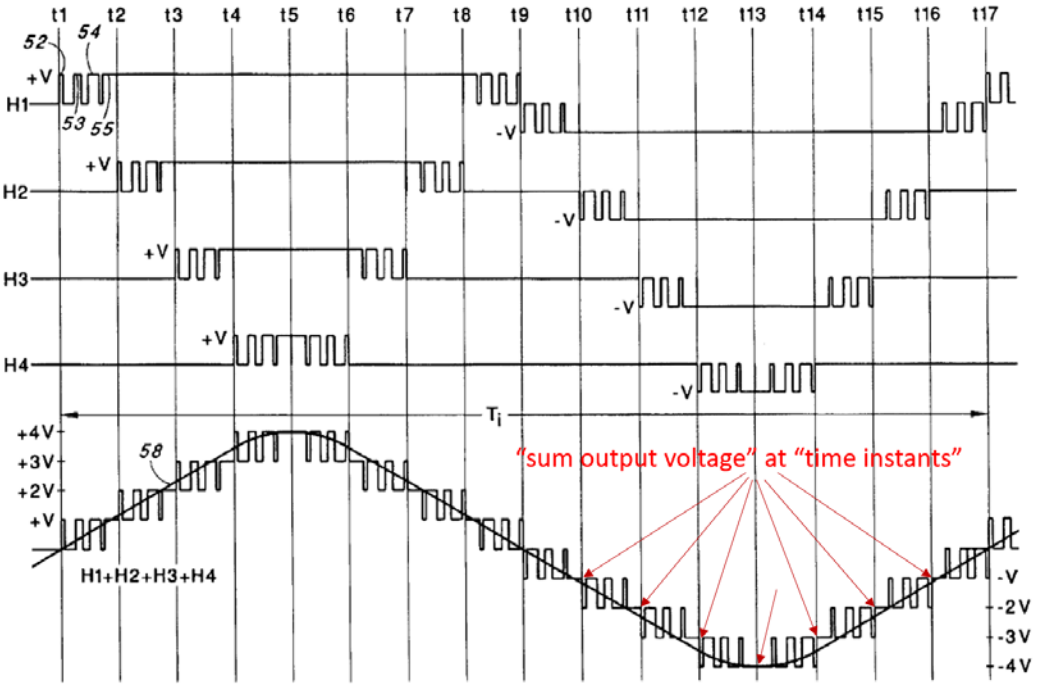


FIG. 8

Ex. 1232, Fig. 8 (annotated)

As annotated in Figure 8 above, Bowles discloses sequential time instants at which each new set of switch selection signals produce a sum output voltage (voltage levels in Figure 8 at t1, t2, etc.) that approximates "the instantaneous voltage values

of the desired waveform" (smooth curve in Figure 8). These sum output voltages at the time instants t1, t2, etc. are the "best approximation … at the given instants" as recited in claim 7, and "a better approximation … at that time instant than the immediately previously output set of switch selection signals" as recited in claim 8, because the sum voltage is set to approximate the desired waveform at each time instant t1, t2, etc., and the voltage level at each time instant (*e.g.*, t3) better approximates the instantaneous voltage value of the desired waveform at that time instant than the immediately previous voltage level at the previous time instant (*e.g.*, t2). Ex. 1202, ¶ 151. Thus, Bowles discloses the additional limitations of claims 7 and 8. *Id*., ¶¶ 147-151.

To the extent that the "switch selection signal generator" is a means plus function term, it is still met by Bowles. *Id.*, ¶ 152. As explained above, the function recited in the claims following the words "configured to" are performed by the proposed combination. *Id*. To the extent there is corresponding structure in the patent for producing these signals, it is controller 200, which includes a microcontroller, or an equivalent structure that sends the signals to switch driving circuits. Ex. 1201, 12:54-56, 13:45-47, Fig. 1; Ex. 1202, ¶ 152. Bowles discloses a control circuit 16 that controls the H-bridge switches by sending control signals to the switches through the opto-isolator. Ex. 1232, 4:10-18, 4:36-46, 5:13-47, 10:23-48, Figs. 2-4. A PHOSITA would understand that control circuit 16 includes a

microcomputer or a microcomputer-based controller that sends the signals to the H-bridge switches. Ex. 1202, ¶ 152. Bowles's control circuit is the equivalent structure of the '710 patent's controller 200. *Id*.

Thus, whether or not "switch selection signal generator" is a means plus function term, Bowles discloses it as recited in claims 7 and 8. *Id.*, ¶¶ 153-154.

B. Ground B: Claims 2, 4, 5 and 12 are Rendered Obvious by Bowles-Lipo

1. Claims 2 and 5

Claims 2 and 5 depend from claim 1. Claim 2 further requires "at least some of the DC voltages associated with the plurality of controlled switches have different values," and claim 5 further requires that "each associated DC voltage differs from another DC voltage nominally by a factor of 3." Ex. 1201, claims 2, 5.

Bowles does not disclose DC voltages associated with the plurality of controlled switches having different values. In one example, Bowles describes using a common DC voltage level of V for 5 H-bridges. Ex. 1232, 5:48-51, Fig. 5. With a common DC voltage level and 5 H-bridges, Bowles describes obtaining 11 voltage states. *Id*. A PHOSITA would have appreciated that the smoothness of the generated sine wave increases as the number of voltage steps increases. Ex. 1202, ¶ 160. Bowles teaches that smoother sine waves are advantageous because they have lower distortion, require smaller and lighter filtering circuits and have lower conversion losses during transistor switching. Ex. 1232, Abstract, 2:32-36.

Lipo discloses a power converter that uses series-connected H-bridge inverters. Ex. 1233, Abstract, Fig. 5, 10:40-49. Lipo teaches that there are advantages associated with using DC voltages associated with the plurality of H-bridge inverters that have different values. For example, using DC source voltage levels varying in a binary fashion allows for achieving 2^{n+1}-1 distinct voltage levels with n inverters. *Id.*, 7:13-30, 12:28-34. With two inverters and DC source voltage levels varying in a binary fashion seven voltage levels can be obtained, while a topology having the same DC levels would require three inverters to achieve seven output voltage levels. *Id.*, 12:28-44.

Lipo further teaches using DC source voltage levels varying in a geometric progression with a factor of three allows for achieving 3^n distinct voltage levels with n inverters. *Id.*, 7:30-38, 20:14-54, 20:65-21:17. Lipo describes using 3^n distinct voltage levels instead of equal DC source voltages provides the advantage of having a substantially higher number of output voltage levels. *Id.*, 21:5-15.

A PHOSITA would have found it obvious to modify Bowles so that the DC voltages associated with the plurality of H-bridges differed from one another by a factor of three to increase the number of output voltage levels obtained and improve the spectral performance of the resulting sine wave without increasing the number of H-bridge inverters, as taught by Lipo. *Id.*, 12:28-44, 21:5-15; Ex. 1202, ¶¶ 157-168. Such a modification would also have been obvious because it merely represents

the use of a known technique (using DC voltages associated with the plurality of H-bridges that differ from one another, such as by a factor of three, as disclosed in Lipo) to improve a similar device (Bowles' inverter that includes H-bridges with associated DC input voltages) in the same way (increasing the number of output voltage levels obtained and improving the spectral performance of the resulting sine wave without increasing the number of H-bridge inverters). Ex. 1202, ¶¶ 163, 167-168.

The combination merely requires applying different DC voltages to the plurality of H-bridges in Bowles and adjusting the signals used to control the H-bridges, which was well within the skill level of a PHOSITA. *Id.*, ¶¶ 164, 167-168, 102.

2. Claim 4

Claim 4 depends from claim 1 and further requires "wherein the controlled switches are MOSFETs connected in H-bridge configurations, and the associated DC power sources are floating relative to each other and relative to the DC to AC converter hot and neutral output terminals." Ex. 1201, claim 4.

Bowles uses field effect transistors (FETs) for the switching elements of the H-bridges. Ex. 1232, 5:13-19, 6:18-22, 8:60-62. However, Bowles does not describe using a specific type of FETs. Ex. 1202, ¶¶ 169-170.

As described above, Lipo discloses a power converter that uses series

connected H-bridge inverters. Ex. 1233, Abstract, Fig. 5, 10:40-49; Section VII.B.1, s*upra*. Lipo discloses "low voltage" H-bridges as having a DC source voltage of 1.5 kV and "high voltage" H-bridges as having a DC source voltage of 3 kV. Ex. 1233, 14:33-37, 15:3-8. With respect to low voltage H-bridges, Lipo teaches using MOSFETs to provide high frequency switching devices. *Id.*, 14:15-18. MOSFETs were also widely available and commonly used as switching devices in electronic devices. Ex. 1202, ¶¶ 170-171, 79.

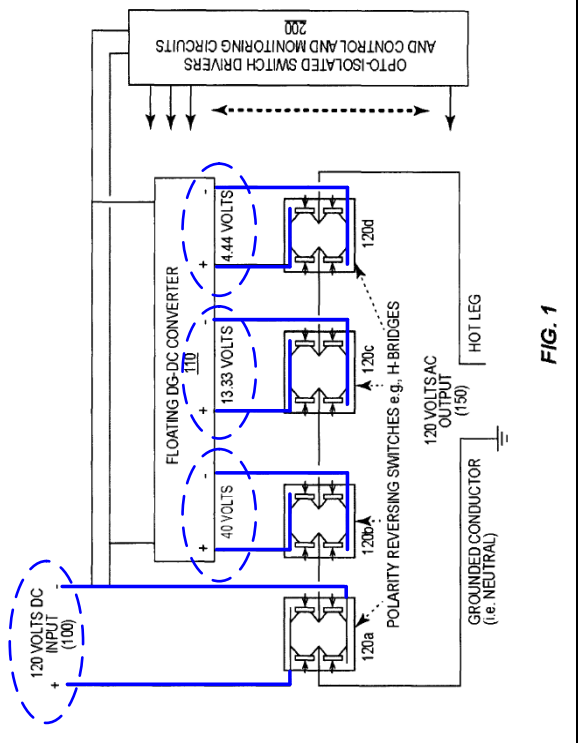
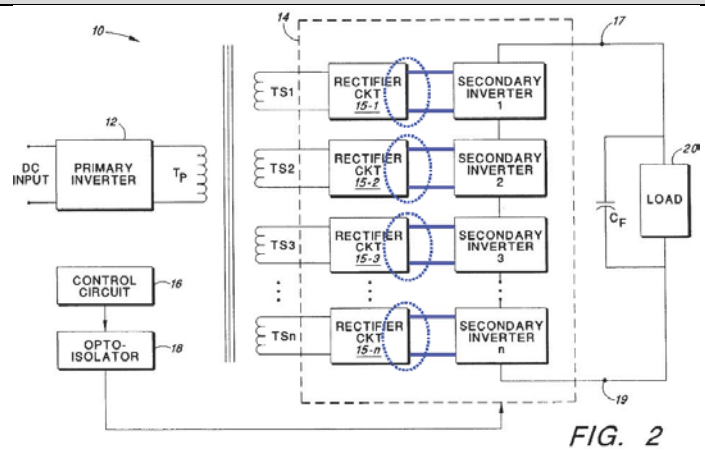
Bowles discloses an example of using four H-bridges to output a 110 VAC sine wave. Ex. 1232, 7:58-61. Bowles discloses another example that uses three multistep step inverters to output an AC waveform with a line to neutral voltage of 115 V. *Id.*, 9:9-14. The H-bridges in Bowles therefore fall within what Lipo characterizes as "low voltage" H-bridges because the DC source voltages used are far less than 1.5 kV. Ex. 1202, ¶ 172.

A PHOSITA would have found it obvious to implement the FETs used in the H-bridges of Bowles with MOSFETs to provide high frequency switching devices that were suitable for use with low voltage H-bridges, as taught by Lipo. *Id.*, ¶ 173.

Such a modification is also obvious because it merely represents the simple substitution of one known element (MOSFETs used in H-bridges) for another (FETs used in H-bridges) to obtain predictable results (H-bridges that include high frequency switching devices). *Id.*, ¶ 174.

Implementing the FETs in Bowles with MOSFETs merely requires using commercially available components connected in the manner described in Bowles, which was well within the skill level of a PHOSITA. *Id.*, ¶ 175.

Further, the DC power supply input to Bowles's switches are in the same configuration as in the '710 Patent. *Id.*, ¶ 176. The floating DC power sources (circled in dashed blue lines) along with their outputs (shown in solid blue) of the '710 Patent are shown on the below left, while the floating DC power sources (circled in dashed blue lines) along with their output connections (shown in solid blue) of Bowles are shown on the below right:

'710 Patent	Bowles
	

In both the '710 Patent and Bowles, the output terminals of each DC power

source are connected to input terminals of a corresponding H-bridge switch. Ex. 1201, Fig. 1, 7:57-60; Ex. 1232, Figs. 2-3, 3:66-4:3, 5:9-26. The switches can change the series arrangement of the voltage sources (*e.g.*, sometimes connecting them in a positive polarity, sometimes connecting them in the reverse polarity, or bypassing them) to generate different sum series voltages. Ex. 1232, 6:7-7:48, Fig. 8; Ex. 1202, ¶ 177. For example, Bowles's secondary inverter 1 alternatively connects either the plus or minus of its input terminals to the output terminal 17 while connecting the opposite input terminal in series to the other voltage sources through secondary inverters 2, 3, … n. Ex. 1232, Figs. 2-3. This requires (as is illustrated above in Figure 2) the DC power source for secondary inverter 1 (*i.e.*, rectifier 15-1) to be floating with respect to the output terminal 17 and with respect to the other DC power sources. The other DC power sources (*i.e.*, rectifiers 15-2, 15-3, … 15-n) operate in a similar manner and are further offset from output terminal 17 by the varying voltage output by the adjacent secondary inverter 1. Thus, the other DC power sources (*i.e.*, rectifiers 15-2, 15-3, … 15-n) are likewise floating. Ex. 1202, ¶ 177.

Bowles thus teaches the claimed "wherein the controlled switches are … connected in H-bridge configurations, and the associated DC power sources are floating relative to each other and relative to the DC to AC converter hot and neutral output terminals," just as shown in the '710 Patent. *Id.*, ¶¶ 176-178.

3. Claim 12

Claim 12 depends from claim 1 and requires "one of the power output connections of the controlled switch having the associated DC power source of the highest associated DC voltage is one of the end terminals of the series connection, and is connected to the neutral output terminal." Ex. 1201, claim 12. Claim 12 lacks antecedent support in claim 1 for "the DC power source of the highest associated DC voltage." Ex. 1202, ¶¶ 179-181. Under any reasonable interpretation that could overcome this lack of support, Bowles-Lipo renders claim 12 invalid as obvious.

While Bowles does not disclose that the DC power sources associated with the plurality of controlled H-bridge switches have different values, Lipo does for the same reasons explained above in Section VII.B.1. A PHOSITA would have found it obvious to modify Bowles so that the DC power sources associated with the plurality of H-bridges differed from one another by a factor of three, as taught by Lipo, for the same reasons described above in Section VII.B.1. Ex. 1202, ¶ 182.

Further, as discussed above for [1C], Figure 3 of Bowles (shown below) illustrates an example of an inverter that includes controlled H-bridge switches H1-H4 connected in series. Section VII.A.1.c, *supra*. As illustrated in Figure 3, switch H4 is at one end of the series connection and has a power output connection connected to ground/neutral at output terminal 19. Section VII.A.1.c, *supra*; Ex. 1202, ¶ 183.

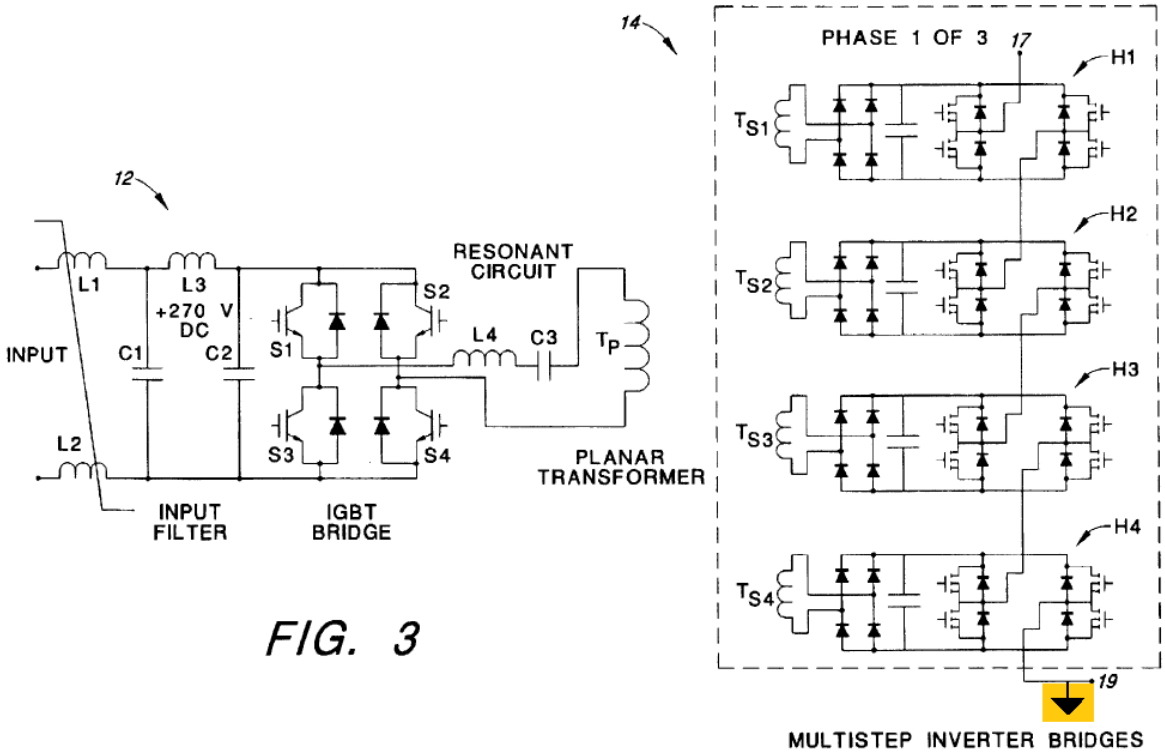


FIG. 3

Ex. 1232, Fig. 3 (annotated)

As discussed above, the Bowles-Lipo combination teaches that the H-bridge switches H1-H4 are connected in series, and that the DC power sources associated with H1-H4 differ from one another by a factor of three, with the highest and lowest voltages at the ends of the series. Ex. 1233, Fig. 14. It would have been obvious to a PHOSITA to have H4 (which is one of the end terminals of the series connection and has a power output connection connected to neutral at output terminal 19) be the controlled switch connected to the associated DC power source of the highest associated DC voltage because there are only a limited number of possibilities to determine which H-bridge switch is connected to the highest DC voltage, and choosing between them would have been a case of using an "obvious to try" solution,

i.e., choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success. Ex. 1202, ¶ 184. A PHOSITA would have understood the benefits of connecting the highest associated DC voltage to Bowles's inverter H4 because such an arrangement reduces electromagnetic interference produced by the inverter. *Id.*

Bowles-Lipo thus renders claim 12 obvious. *Id.*, ¶¶ 182-185.

C. Ground C: Claim 3 is Rendered Obvious by Bowles-Bower

Claim 3 depends from claim 1 and requires "the desired voltage is a voltage of a standard household electricity supply and the desired waveform is sinusoidal at a standard household electricity supply frequency." Ex. 1201, claim 3. While Bowles does not disclose the standard household voltage and frequency requirements in claim 3, Bower does.

Bower discloses the use of an inverter to convert DC power of a solar grid to AC power for use within a standard household, having a standard household frequency. Ex. 1211, 2:55-64, 8:34-36, 10:16-29, 10:47-11:18; Ex. 1202, ¶ 192. Specifically, Bower outputs single-phase 240V, 60Hz AC power or "power at 120V or any other single-phase voltage with one terminal grounded that is intended to be connected to the neutral conductor in the house." Ex. 1211, 10:16-29; Ex. 1202, ¶ 193. Sixty hertz is a standard household frequency. Ex. 1202, ¶¶ 192-193.

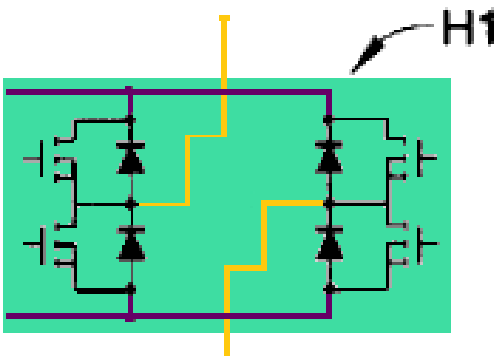
It would have been obvious to use a known technique (producing an AC waveform with the voltage and frequency used in a standard household) to improve a similar device (Bowles's inverter) in the same way (Bower produces AC power for a standard household). *Id.*, ¶ 193. A PHOSITA was familiar with designing an inverter to produce AC power for use in a household and had the skills to do so, providing an expectation of success. *Id.*, ¶ 194.

Thus, Bowles-Bower renders claim 3 obvious. *Id.*, ¶¶ 190-195.

D. Ground D: Claim 6 is Rendered Obvious by Bowles-Mori '265

Claim 6 depends from claim 1 and requires "the ternary-valued selection signals comprise pairs of binary bits, each bit pair having in total four combinations of possible values, of which two of the four combinations represent the zero multiplier value." Ex. 1201, claim 6.

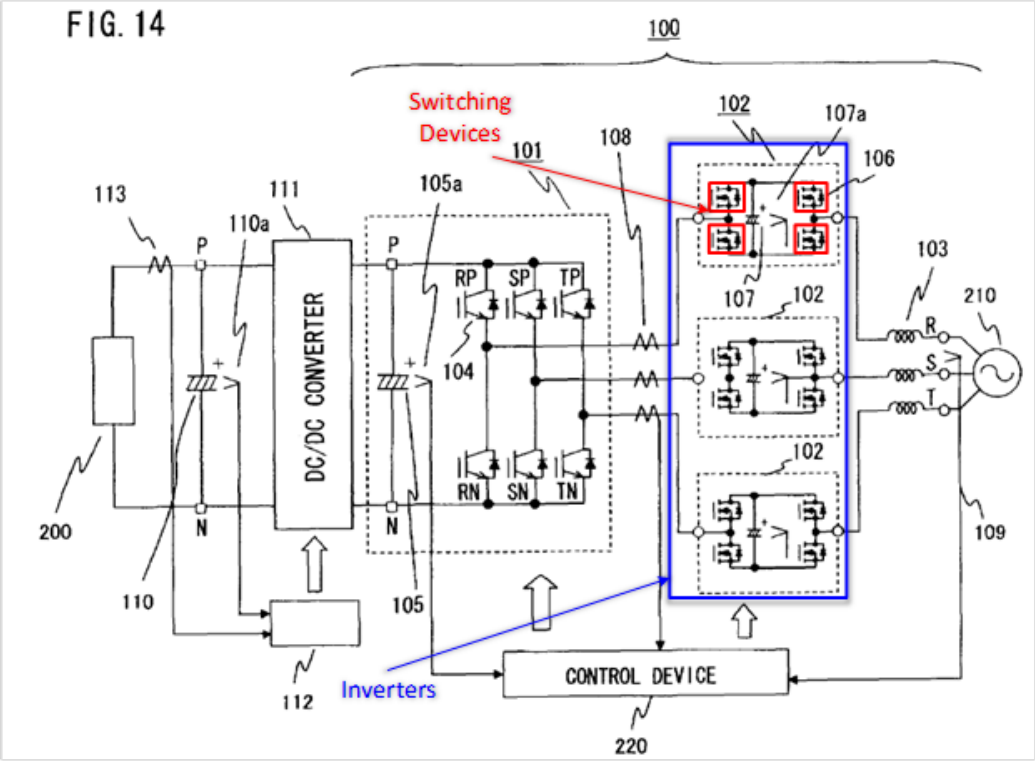
As discussed in Section VII.A.1 above, Bowles's H-bridges are controlled such that they output the supply voltage (V), the negative of its supply voltage (-V), or zero volts (0). Ex. 1232, 4:10-18, 4:36-46, 5:13-47, 10:23-48, Figs. 2-4; Ex. 1202, ¶ 201. As shown below in the excerpt from Figure 3, the H-bridges are a group of four transistors each receiving a signal (not shown) on its gate, which turns the transistor "on" or "off." By turning only certain transistors on, the H-bridge will be placed in either the "+V", "-V" or "0V" states to output +V, -V, and 0 volts, respectively. Ex. 1202, ¶ 201.



Ex. 1232, Excerpt of Fig. 3 (annotated)

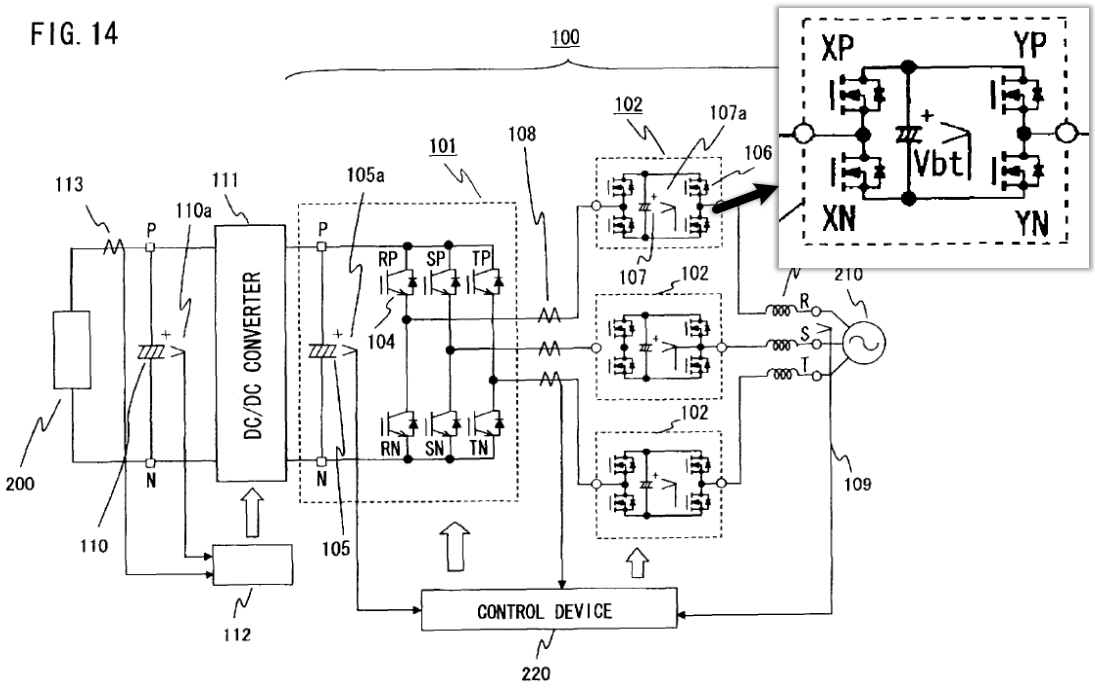
While Bowles discloses that its ternary-valued control signals control each H-bridge, and thus the four signals controlling the four transistors, Bowles does not explicitly disclose that the ternary-valued selection signals comprise pairs of binary bits as recited in claim 6. Ex. 1202, ¶ 202. However, this was a common control scheme for H-bridge switches, and is disclosed by Mori '265. *Id.*

Mori '265, like Bowles, teaches a power converter that uses H-bridge structures in an inverter to output one of three levels: -V, 0, or +V, based on a combination of ON and OFF states of the transistors in the H-bridge. Ex. 1207, [0011], [0028], [0047]-[0050], Fig. 14 (transistors 106, highlighted below); Ex. 1202, ¶ 203.



Ex. 1207, Fig. 14 (annotated)

In particular, gate driving signals are sent to the gates of the transistors (XP, YP, XN, YN) of each of the H-bridges, shown in Figures 1 and 14 below. Ex. 1207, [0031], [0050]; Ex. 1202, ¶ 204.



Ex. 1207, Figs. 1 (excerpted) and 14

The value of the four gate driving signals (to the 4 transistors in the H-bridge) is determined based on two binary control signals RX and RY (the claimed pair of "binary bits ... having in total four combinations of possible values,"). Ex. 1207, [0031], [0050], Fig. 11 (reproduced below); Ex. 1202, ¶ 205.

	SW	A	B	C	D
RX →	XP	1	0	1	0
	XN	0	1	0	1
RY →	YP	0	1	1	0
	YN	1	0	0	1
	SUB-OUTPUT	+	—	0	0

Ex. 1207, Fig. 11

As illustrated in Figure 11, RX may have one of two values such that the first value causes XP and XN to be 1 and 0, respectively, and the second value causes XP and XN to be 0 and 1, respectively. Ex. 1207, [0032]; Ex. 1202, ¶ 206. Likewise, RY may have one of two values such that the first value causes YP and YN to be 1 and 0, respectively, and the second value causes YP and YN to be 0 and 1, respectively. *Id*. Each column (A, B, C, and D) indicates the states of the four switching devices XP, XN, YP, and YN in an H-bridge for each of the four possible combinations of binary values RX and RY. As shown in the last row of the table, one of the combinations (i.e., A) places the H-Bridge into the "+1" state, one of the combinations (i.e., B) places the H-Bridge into the "-1" state, and two of the combinations (i.e., C and D) place the H-bridge into the "0" state, thus disclosing the claim 6 feature of "two of the four combinations represent the zero multiplier value." Ex. 1202, ¶ 206.

A PHOSITA would have been motivated to use Mori '265's two-bit control signal encoding in Bowles because it is efficient and eliminates superfluous control logic for Bowles's ternary-valued control signal. *Id.*, ¶ 207. This is an obvious combination of prior art elements (Bowles's H-bridge switches and Mori '265's two-bit control signal) in a known manner (providing Mori '265's two-bit control signal to control Bowles's H-bridge switches) to achieve predictable results (the H-bridges

receive a two-bit encoded signal that enables the generation of four output states: positive, negative, and two zero states). *Id.*, ¶¶ 207-208, 85-86, 102.

This modification was within the skill set of a PHOSITA, who was familiar with H-bridge switches and basic control logic needed to implement the two-bit control signals, providing a reasonable expectation of success. *Id.*, ¶ 208.

Thus, Bowles-Mori '265 renders obvious claim 6. *Id.*, ¶¶ 199-209.

E. Ground E: Claim 9 is Rendered Obvious by Bowles-Flanagan

Claim 9 depends from claim 8, and recites: "[the] DC to AC ... further comprising, where the desired waveform is repetitive: memory operative to store precomputed sequential sets of switch selection signals and the associated time instants at which each set is to be output; and wherein the switch selection signal generator is operative to retrieve the precomputed sequential sets of switch selection signals and associated time instants from the memory, and to output the switch selection signals at the associated times." Ex. 1201, claim 9.

As discussed above in Section VII.A.1.f, Bowles teaches that its control circuit 16 ("switch selection generator") generates control signals that control the output voltages of each of the secondary inverters of multistep inverter 14 such that the signal applied across load 20 approximates a sinewave (the claimed "where the desired waveform is repetitive"). Section VII.A.1.f, *supra*. While Bowles does not

expressly describe a memory with the functionality described in claim 9, Flanagan does.

Flanagan teaches a programmed PWM controller for controlling a DC/AC inverter. Ex. 1208, Abstract. Flanagan's inverter is a full-bridge, three-phase inverter with three pairs of inverter switches. *Id.*, 4:64-68, Figs. 1, 2. Flanagan teaches a gating signal that is output to a control line to control the state of the inverter's individual switches. *Id.*, 5:5-8; Ex. 1202, ¶ 216.

Flanagan's PWM controller includes a memory, a cycle counter, an address counter, a comparator, and a clock. Ex. 1208, 5:24-29. The controller outputs a sequence of gating signals (referred to as "drivewords") to the control line to generate the desired inverter output. *Id.*, 5:18-23; Ex. 1202, ¶ 217.

Specifically, the memory of the PWM controller stores a series of drive data words, each of which includes both a driveword for controlling the switch states of the inverter and a drivetime providing timing information within the PWM sequence (the claimed "memory operative to store precomputed sequential sets of switch selection signals and the associated time instants at which each set is to be output"). Ex. 1208, 5:29-35; Ex. 1202, ¶ 218. The first drive data word (*e.g.*, first driveword and corresponding drivetime) is retrieved from the memory and output onto data buses. Ex. 1208, 5:55-6:35. When the address counter is incremented, the next drive data in the sequence (*e.g.*, the next driveword and corresponding drivetime) are

retrieved from the memory and output onto the data buses. *Id*. This procedure is repeated for each drive data word in the PWM sequence (the claimed retrieval of "the precomputed sequential sets of switch selection signals and associated time instants from the memory" to "output the switch selection signals at the associated times.") *Id.*, 6:35-50; Ex. 1202, ¶ 218.

A PHOSITA would have been motivated to implement Bowles's signal generator to include the memory and functionality of Flanagan's programmed PWM controller because using a series of precomputed signals reduces or eliminates the need for processing power dedicated to calculating the signals in real time. Ex. 1202, ¶ 219. This modification merely represents a combination of prior art elements (the switch selection signal generator of Bowles and the use of Flanagan's programmed controller) in a known manner (programming the signal generator to store and retrieve the precomputed signals using the pre-stored timing sequence) to achieve predictable results (the reliable and straightforward generation of a series of control signals at the appropriate times). *Id.*

Implementing the switch selection signal generator and generating gating signals according to Flannagan as described above would have required nothing more than the use of basic digital logic and memory devices, which a PHOSITA was familiar with, providing a reasonable expectation of success. *Id.*, ¶ 220.

To the extent the "switch selection signal generator" is a means-plus-function term in claim 9, Bowles-Flanagan teaches this element for the same reasons described in claim 7, and because—as described above in this section—the structure in Bowles-Flanagan performs the same function recited in claim 9. Section VII.A.2, *supra*; Ex. 1202, ¶ 221. Additionally, Flanagan teaches the same, or equivalent memories as disclosed in the '710 patent. Ex. 1202, ¶ 221-222.

Thus, Bowles-Flanagan renders obvious claim 9. *Id.*, ¶¶ 212-222.

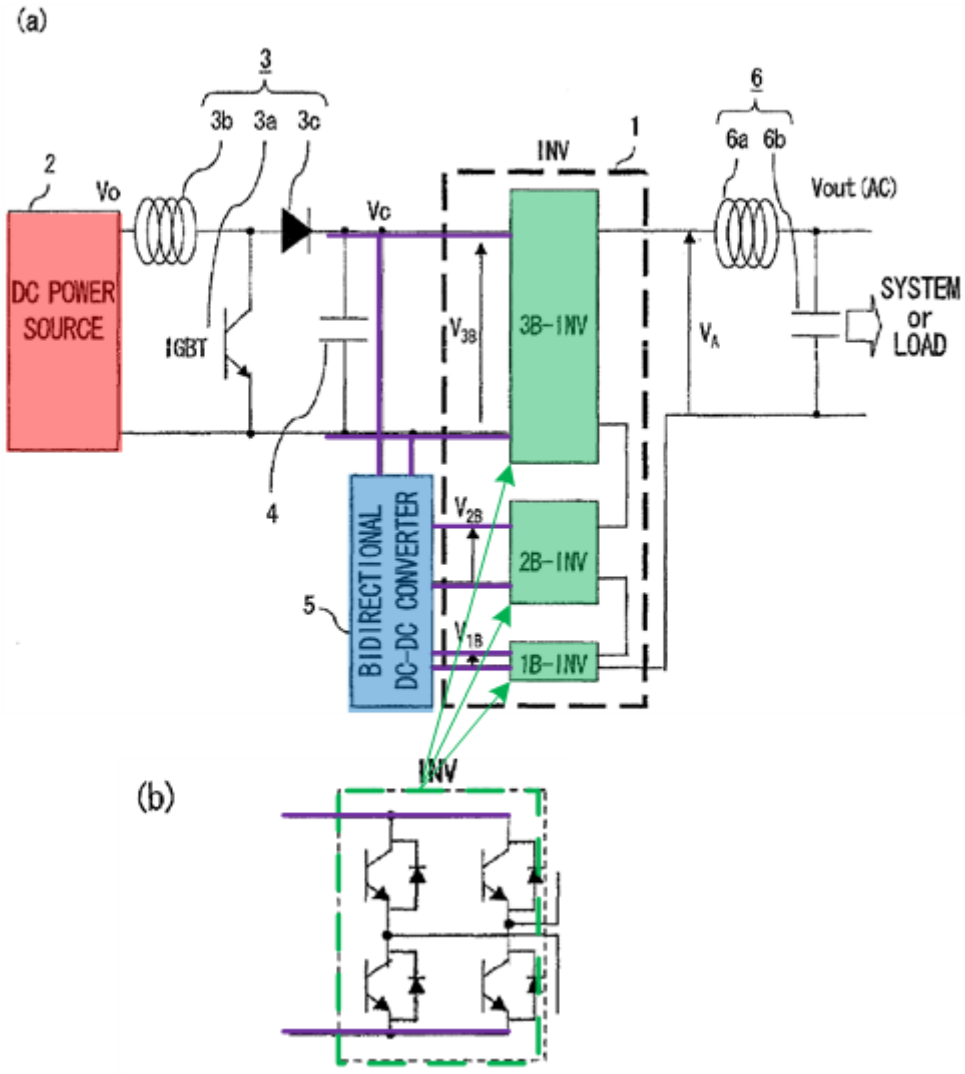
F. Ground F: Claims 10-11 are Rendered Obvious by Bowles-Iwata

1. Claim 10

Claim 10 depends from claim 1 and requires "the DC power source having the highest voltage value is a battery and the DC power sources having lower voltages values comprise bi-directional DC-DC conversion circuitry operative to derive the lower voltage values from the battery." Ex. 1201, claim 10. Claim 10 lacks antecedent support in claim 1 for "the DC power source having the highest voltage", and "the DC power sources having lower voltages." Ex. 1202, ¶¶ 229-231. Under any reasonable interpretation that could overcome this lack of support, Bowles-Iwata renders claim 10 invalid as obvious.

While Bowles does not disclose "wherein the DC power source having the highest voltage is a battery" and the "DC-DC conversion circuitry" recited in claim 10, Iwata does. Iwata discloses a DC to AC inverter that converts DC power [DC

input (**red**)] to an AC power [AC output Vout (AC)] as shown in Figure 1 below. Ex. 1202, ¶¶ 224-228; Ex. 1204, [0001], [0006]-[0009], [0050]-[0053], [0061], [0078], [0090], [0097], [0119], Figs. 1-2, 4-5. Iwata's inverter comprises "a plurality of controlled switches" (**green**), described as three single-phase inverters 3B-INV, 2B-INV and 1B-INV. Ex. 1204, [0045]-[0049]. Each switch includes a plurality of switching devices arranged in an H-bridge switch. *Id.*, [0046], Fig. 1; Ex. 1202, ¶ 226. Like the H-bridges of Bowles, these switches are controlled to produce positive, negative, or zero voltages from their respective DC power sources. Ex. 1204, [0047], [0050], [0059], Fig. 2, 4-5; Ex. 1202, ¶ 227.



Ex. 1204, Fig. 1 (annotated)

Each of these switches have input connections (highlighted in **purple** above) connected to and receiving DC power from an associated DC power source (highlighted in **red** and **blue** above), which is either DC power source 2 (for the 3B-INV switches) or bidirectional DC-DC converter (for the 1B-INV and 2B-INV switches). Ex. 1204, [0046], [0048]-[0049], [0077], [0083]-[0084], [0097], [0100], [0103]-[0111], Figs. 1, 14, 16-18; Ex. 1202, ¶ 225. In Iwata's embodiment from

Figure 1, for example, V_{1B}, V_{2B}, and V_{3B} are the DC power source voltage inputs, respectively, for the plurality of switches 1B-INV, 2B-INV and 3B-INV. Ex. 1204, [0049], Fig. 1; Ex. 1202, ¶¶ 225, 228. Further, "V_{1B}, V_{2B}, and V_{3B} are controlled to have predetermined voltage ratio by the DC-DC converter 5," which can include 1:2:4 or 1:3:9. Ex. 1204, [0048], [0050], [0051], Figs. 2, 4-5.

Iwata's bidirectional DC-DC converter 5 (**blue**) derives the lower voltage DC power sources from the primary (highest voltage) DC power source 2 generating V3B (the highest voltage input to inverter 3B-INV). Ex. 1204, [0046], [0048], [0077], [0083], [0097]-[0098], [0100], [0103]-[0104], [0108]; Ex. 1202, ¶ 225. Iwata further describes that its inverter may be used in a power conditioner for a decentralized power source and describes an example that uses a solar battery as its DC power source. Ex. 1204, [0001]-[0003]. Iwata further discloses that the inverter is used in an "uninterruptible power supply" (UPS), which a POSITA would understand includes a battery to provide uninterrupted power as the backup power source, when the primary power source (*e.g.*, rectifier connected to a utility grid), was disconnected or not operating. Ex. 1204, [0119]; Ex. 1202, ¶ 233. Thus, Iwata teaches the "battery" and "DC-DC conversion circuitry" recited in claim 10. Ex. 1202, ¶¶ 232-233.

It would have been obvious to a POSITA to modify Bowles's inverter to utilize a battery, as taught by Iwata, as the DC power source. *Id.*, ¶ 234. Iwata

discloses that utilizing such a configuration is desirable because a converter that includes a battery can be "broadly applied" to an uninterruptible power supply apparatus. Ex. 1204, [0119]; Ex. 1202, ¶ 234. Therefore, a POSITA would have been motivated to modify Bowles's inverter to include a battery, as taught by Iwata, to allow the inverter to provide uninterrupted power as the backup power source when the primary power source is disconnected or not operating. Ex. 1202, ¶ 234.

Such a modification would have been obvious as the simple substitution of one known element (Iwata's battery as an uninterruptible DC power source) for another (Bowles's DC power source) to yield predictable results (the battery serves as a reliable uninterruptible DC power source). Ex. 1204, [0119]; Ex. 1202, ¶ 235. A POSITA would have been familiar with batteries as beneficial DC power sources for inverters such as when used for backup power in a UPS, and would have had the skills to implement Bowles-Iwata with a battery. Ex. 1202, ¶ 235, 77, 92.

It also would have been obvious to a POSITA to modify Bowles's voltage input circuitry to utilize DC-DC conversion circuitry to provide different voltage levels for the inverters, as taught by Iwata. *Id.*, ¶ 236. As explained above, in Iwata's embodiment from Figure 1, V_{1B}, V_{2B}, and V_{3B} are the DC power source voltage inputs, respectively, for the plurality of switches 1B-INV, 2B-INV and 3B-INV. Ex. 1204, [0049], Fig. 1; Ex. 1202, ¶ 236. Iwata discloses that "V_{1B}, V_{2B}, and V_{3B} are controlled to have predetermined voltage ratio by the DC-DC converter 5," which

can include 1:3:9. Ex. 1204, [0048], [0050], [0051], Figs. 2, 4-5. In this example, Iwata describes obtaining 14 voltage states, which provides a "substantially sine wave-like output voltage waveform 11 ..." *Id.*, [0050], Fig. 2(b).

Bowles does not disclose DC voltages associated with the plurality of controlled switches having different values. Ex. 1202, ¶ 237. In one example, Bowles describes using a common DC voltage level of V for 5 H-bridges. Ex. 1232, 5:48-51, Fig. 5. With a common DC voltage level and 5 H-bridges, Bowles describes obtaining 11 voltage states. *Id*. A PHOSITA would have appreciated that the smoothness of the generated sine wave increases as the number of voltage steps increases. Ex. 1202, ¶ 237. Bowles teaches that smoother sine waves are advantageous because they have lower distortion, require smaller and lighter filtering circuits and have lower conversion losses during transistor switching. Ex. 1232, Abstract, 2:32-36.

A PHOSITA would have found it obvious to modify Bowles to include the DC-DC conversion circuitry taught by Iwata so that the DC voltages associated with the plurality of H-bridges differed from one another to increase the number of output voltage levels obtained and improve the spectral performance of the resulting sine wave without increasing the number of H-bridge inverters. Ex. 1232, 4:46-5:3, Figs. 1(a), 2; Ex. 1202, ¶ 238. In such a combination, the DC power source having the highest voltage is a battery, and the DC power sources having lower voltages

comprise bi-directional DC-DC conversion circuitry operative to derive the lower voltages from the battery, as taught by Iwata. Ex. 1232, 4:46-5:3, Fig. 1(a); Ex. 1202, ¶ 238.

Such a modification would have also been obvious because it merely represents the use of a known technique (using DC voltages associated with the plurality of H-bridges that differ from one another, as disclosed in Iwata) to improve a similar device (Bowles' inverter that includes H-bridges with associated DC input voltages) in the same way (increasing the number of output voltage levels obtained and improving the spectral performance of the resulting sine wave without increasing the number of H-bridge inverters). Ex. 1202, ¶ 239. This combination would have been a straightforward matter of substituting the voltage input circuitry in Bowles (*e.g.*, the DC input as described above, primary inverter 12, transformer and rectifier circuits 15-1–15-n illustrated at Ex. 1232, Fig. 2) with the voltage input circuitry in Iwata (*i.e.*, the DC power source (battery) as described above, chopper circuit 3, smoothing capacitor 4 and bidirectional DC-DC converter illustrated at Ex. 1204, Fig. 1(a)), and adjusting the signals used to control the H-bridges, all of which was well within the level of ordinary skill in the art. *Id*.

2. Claim 11

Claim 11 depends from claim 1 and requires "the DC power source supplying the highest mean power is a battery and the DC power sources supplying lower mean

power comprise bi-directional DC-DC conversion circuitry operative to derive the lower mean power from the battery." Ex. 1201, claim 11. Claim 11 lacks antecedent support in claim 1 for "the DC power source supplying the highest mean power", and "the DC power sources supplying lower mean power." Ex. 1202, ¶¶ 240-241. Under any reasonable interpretation that could overcome this lack of support, Bowles-Iwata renders claim 11 invalid as obvious.

While Bowles does not disclose the "battery" and "DC-DC conversion circuitry" recited in claim 11, Iwata does. As explained with respect to claim 10, Iwata discloses a bidirectional DC-DC converter 5 operative to derive the lower voltage DC power sources from the primary DC power source 2, and that the inverter is used in an "uninterruptible power supply," which means a battery would be included as a backup DC power source when the primary power source was not providing power. Ex. 1204, [0046], [0048], [0077], [0083], [0097]-[0098], [0100], [0103]-[0104], [0108], [0119]; Ex. 1202, ¶ 242; Section VII.F.1, *supra*.

While claim 10 focuses on the *voltage value* of the different DC power supplies, claim 11 focuses on the *mean power* of the different DC power supplies. *See* Ex. 1201, claims 10, 11. But in the context of Iwata's inverter, this is not a meaningful distinction and Iwata teaches both. Ex. 1202, ¶ 243. Mean power is the average power output over a certain time period. *Id.*, ¶ 244. Power is calculated by multiplying the voltage by the current. *Id*.

In Iwata, the DC power source (V_{3B}) is taught to have a voltage higher than the other two power sources (V_{1B} and V_{2B}), for example so that the voltage ratio for the three sources is 1:3:9, and the switches are controlled in such a way that the mean power of that source (which is proportional to the voltage) would be higher than the other two. Ex. 1204, [0048], [0050], [0051], Figs. 2, 4-5; Ex. 1202, ¶ 245. This is the same as is disclosed in the '710 patent, that also has a voltage ratio of 1:3:9 and a similar switching pattern. *See, e.g.,* Ex. 1201, 11:5-18, Fig. 4; Ex. 1202, ¶ 245. Thus, the additional limitations of claim 11 are taught by Iwata, and Bowles-Iwata renders claim 11 invalid as obvious. The rationale for modifying Bowles in view of Iwata is the same as that described for claim 10 in Section VII.F.1, *supra*. Ex. 1202, ¶ 246.

G. Ground G: Claims 10-11 Are Rendered Obvious by Bowles-Iwata in view of Tracy

As explained in Sections VII.F.1-VII.F.2, claims 10 and 11 are taught by Bowles-Iwata. Sections VII.F.1-VII.F.2, *supra*. To the extent PO argues the "battery" of claims 10 and 11 is not taught by Bowles-Iwata, Tracy discloses the use of a battery (**red**) as a backup power source for an inverter in an uninterruptable power supply (UPS) as shown in Figure 3 below. Ex. 1209, 1:6-47, 4:50-59, 5:1-6, 5:41-52, 6:46-49, Figs. 1-3; Ex. 1202, ¶ 252.

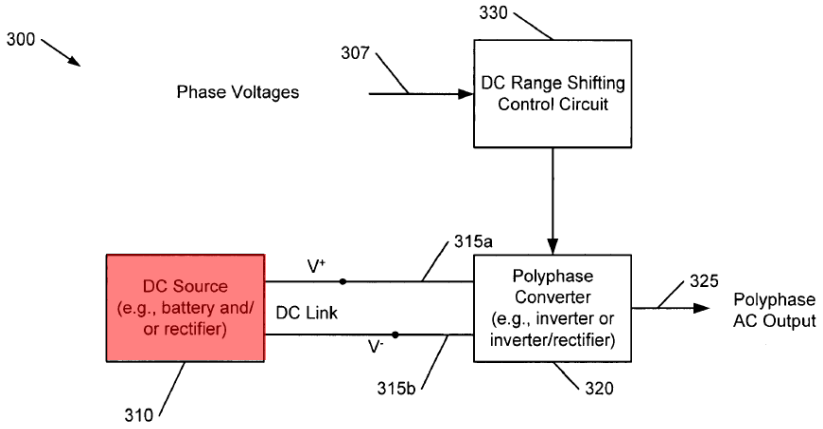


FIG. 3

Ex. 1209, Fig. 3 (annotated)

The use of Tracy's battery as an uninterruptible DC power source in Bowles-Iwata's inverter that also teaches the use of an uninterruptible DC power source, would have been obvious as the simple substitution of one known element (Tracy's battery as an uninterruptible DC power source) for another (Bowles-Iwata's uninterruptible power source having the highest voltage value) to yield predictable results (the battery serves as a reliable uninterruptible DC power source). Ex. 1204, [0119]; Ex. 1209, 5:41-52, 6:46-49, Figs. 1-3; Ex. 1202, ¶ 253. A POSITA would have been familiar with batteries as beneficial DC power sources for inverters such as when used for backup power in a UPS, and would have had the skills to implement Bowles-Iwata with a battery as the highest voltage power source. Ex. 1202, ¶ 253,

77, 92. Tracy itself explains that the use of batteries in this way was well known in the art. Ex. 1209, 1:6-47.

Thus, Bowles-Iwata-Tracy renders obvious claims 10 and 11 for the reasons stated above in Sections VII.F.1-VII.F.2, and for these further reasons. Ex. 1202, ¶¶ 249-254.

H. Grounds H and I: Claims 10-11 are Rendered Obvious by Bowles-Iwata and Bowles-Iwata-Tracy, Each in View of Nishimura

To the extent that the "bi-directional DC-DC conversion circuitry" of claims 10 and 11 is a means plus function term, Nishimura discloses an equivalent structure. Ex. 1214, Fig. 4; Ex. 1202, ¶ 260. As explained above, the function recited in the claims following the words "operative to" are performed by the proposed combination. Ex. 1202, ¶ 260; Section VII.F, *supra*. To the extent there is corresponding structure in the '710 patent for deriving the lower voltage values from the battery, it is Figure 2, which includes transformer windings, which have turn ratios in proportion to the voltage ratios wherein the lower voltage windings are center tapped. Ex. 1201, 19:41-44, 20:9-28, Fig. 2; Ex. 1202, ¶ 260. Nishimura similarly discloses a voltage converting unit, which includes multiple center tapped windings in proportion to the desired voltages. Ex. 1214, [0070]-[0071], Fig. 2; Ex. 1202, ¶ 260. Nishimura's voltage converting unit is the equivalent structure of the '710 patent's bi-directional DC-DC conversion circuitry. Ex. 1202, ¶ 261. Further, implementing Bowles-Iwata's and Bowles-Iwata-Tracy's bidirectional DC-DC

converter with Nishimura's variable windings to produce different DC voltages that are lower than the primary DC power source would be the simple substitution of one known element (Nishimura's voltage converting unit) for another (Bowles-Iwata's or Bowles-Iwata-Tracy's bi-directional DC-DC converter) with predictable results (creation of different DC input voltages for Bowles-Iwata's and Bowles-Iwata-Tracy's switches). *Id*. A POSITA would have had the skills to implement this known circuit structure and would have had a reasonable expectation of success. *Id*.

Thus, to the extent "bi-directional DC-DC conversion circuitry" is a means plus function term, the combinations of Bowles-Iwata-Nishimura and Bowles-Iwata-Tracy-Nishimura renders obvious claims 10 and 11. *Id.*, ¶¶ 257-262.

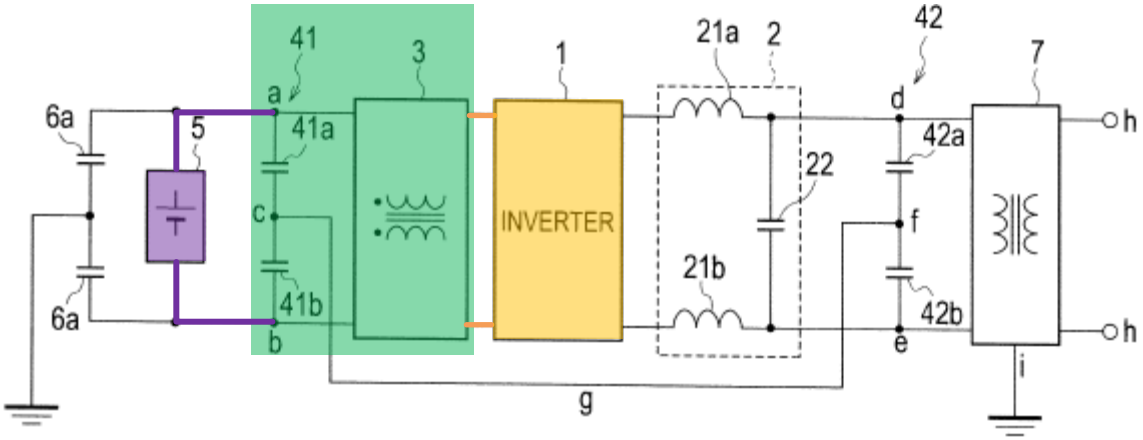
I. Grounds J and K: Claim 13 is Rendered Obvious by Bowles-Iwata-Koyama and Bowles-Iwata-Tracy-Koyama

Claim 13 depends from claim 1 and requires "the associated DC power source of one of the controlled switches is a battery, and further comprising a common-mode filter interposed between the battery and the controlled switch." Ex. 1201, claim 13.

As explained above with respect to claims 10 and 11, while Bowles does not disclose that one of the DC power sources of one of the controlled H-bridge switches is a battery, Bowles-Iwata and Bowles-Iwata-Tracy each teach using a battery (*e.g.*, in a UPS) as the DC power source for Bowles-Iwata's inverter, which is also the power source for Bowles-Iwata's H-bridge switches (controlled switch). Sections

VII.F and VII.G, *supra*. These combinations as disclosed above thus teach "wherein the associated DC power source of one of the controlled switches is a battery." Section VII.F and VII.G, *supra*.

While Bowles-Iwata and Bowles-Iwata-Tracy do not teach the additional limitation in claim 13 requiring a common-mode filter interposed between the battery and the controlled switch, Koyama does. Ex. 1202, ¶¶ 265-269. Koyama discloses including a common mode filter (**green**) interposed between an inverter 1 (**orange**) and a floating DC power source 5 (**purple**), such as between the H-bridge switches in Bowles-Iwata's secondary inverters 1, 2, … n and the DC input as further recited in claim 13. Ex. 1213, [0005]-[0007], [0012]-[0013], [0024]-[0026], [0030]-[0031], [0036]-[0038], Figs. 1, 4, 5; Ex. 1202, ¶¶ 264, 269.



Ex. 1213, Fig. 5 (annotated).

Koyama explains that floating DC power sources (described as a solar cell, fuel cell, or battery) may include stray capacitances 6 between the terminals of the

DC power source and ground, which can provide a path for common mode leakage current. Ex. 1213, [0012]-[0013], [0002]-[0003], [0016]-[0018], [0026], [0036]-[0038]; Ex. 1202, ¶ 270. Moreover, common mode noise generated by the inverter may cause impermissible electromagnetic interference (EMI). Ex. 1202, ¶ 271. A PHOSITA would have been motivated to add Koyama's common mode filter between the floating battery (*e.g.*, of Bowles-Iwata's or Bowles-Iwata-Tracy's UPS battery and other DC power sources) and the H-bridge switches in Bowles's secondary inverters 1, 2, … n to suppress common-mode currents and minimize EMI. Ex. 1213, [0012]-[0013], [0019]-[0021]; Ex. 1202, ¶ 271.

Bowles-Iwata, and Bowles-Iwata-Tracy, each combined with Koyama, which disclose claim 13 as described above, represent the obvious use of a known technique (inserting Koyama's common mode filter between a power source and inverter) to improve a similar device (Bowles's inverter fed by Iwata's or Tracy's battery) in the same way (by suppressing the common mode current and EMI). Ex. 1202, ¶¶ 272-273. The combination merely requires inserting additional filter components and adjusting component values, which was well within the skill of a PHOSITA. *Id*.

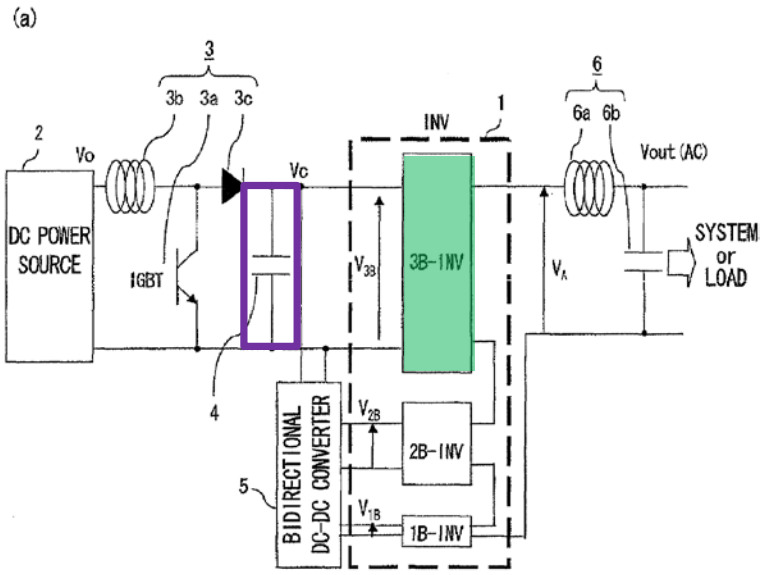
J. Grounds L and M: Claim 14-15 are Rendered Obvious by Bowles-Lipo-Iwata-Koyama-Ahmed and Bowles-Lipo-Iwata-Tracy-Koyama-Ahmed

Claim 14 depends from claim 12, and claim 15 depends from claim 14. Claims 14 and 15 recite specific circuit components of "the common mode filter" connected between "DC power input terminals of the controlled switch" and "the battery," but there is no antecedent common mode filter or battery in claim 12, from which claims 14 and 15 depend. Ex. 1202, ¶¶ 277-280. Under any reasonable interpretation that could overcome this lack of support, Bowles-Lipo-Iwata-Koyama-Ahmed and Bowles-Lipo-Iwata-Tracy-Koyama-Ahmed render claims 14 and 15 obvious. *Id*.

As explained above with respect to claim 13, it would have been obvious to connect Koyama's common mode filter between a DC power source (a battery as disclosed in Iwata or Tracy) and the Bowles-Iwata inverter to reduce the common mode leakage current and EMI emitted by the inverter in the Bowles-Iwata and Bowles-Iwata-Tracy combinations. Section VII.I, *supra*. Bowles-Lipo (Ground B) is identical to Bowles (Ground A) with respect to the connection between the DC power source and the input to the inverter, and thus it would have been obvious to combine Iwata and Koyama, or Iwata, Koyama and Tracy, with Bowles-Lipo (Ground B) in the same way and for the same reasons discussed above with respect to Bowles-Iwata (Ground F) (combining Iwata's battery with Bowles's inverter),

Bowles-Iwata-Tracy (Ground G) (combining Tracy's battery with Bowles's inverter), and Bowles-Iwata-Koyama and Bowles-Iwata-Tracy-Koyama (Grounds J and K) (combining Koyama's common mode filter between the battery and Iwata's inverter). Ex. 1202, ¶ 281.

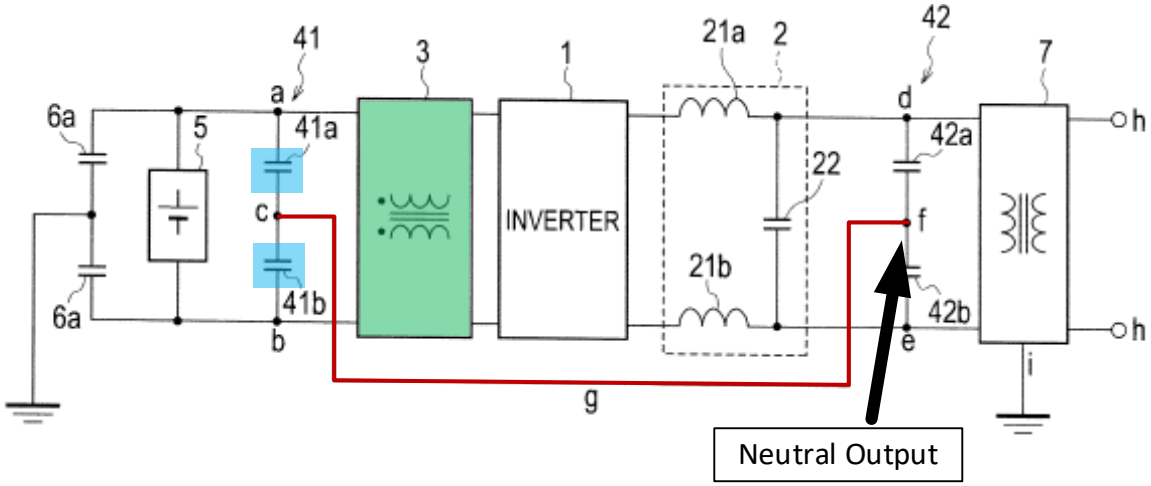
Further, Bowles-Lipo-Iwata-Koyama and Bowles-Lipo-Iwata-Tracy-Koyama, combined with Ahmed, teach the common mode filter structures of claims 14 and 15. As shown below, Iwata teaches (in **purple**) the claim 14 "capacitor connected between DC power input terminals of a controlled switch" (in **green**). Ex. 1204, [0045], [0048], [0058], Figs. 1, 4, 14, 16-18; Ex. 1202, ¶ 282.



Ex. 1204, Fig. 1(a) (annotated)

Koyama, as shown below, discloses the claim 14 "common-mode choke" [**green**] connected between a DC power source (*e.g.*, Iwata's or Tracy's battery) and

the DC power input terminals of the controlled switch (*e.g.*, Bowles's H-bridge switch H4). Ex. 1213, [0029], [0036]-[0038], Figs. 4-5. Ex. 1202, ¶ 283.



Ex. 1213, Fig. 5 (annotated).

Koyama also teaches the claim 14 "first pair capacitors [**blue**] connected respectively from positive and negative terminals of the battery [*e.g.*, Iwata's or Tracy's Battery as DC power source 5] to the neutral output terminal [Bowles's neutral output terminal as AC neutral point f]." Ex. 1213, [0024]-[0026], [0030]-[0031], [0035]-[0038], Figs. 4-5; Ex. 1202, ¶ 284.

Ahmed teaches to modify Koyama's first pair of capacitors to add a damping circuit meeting the remaining claim 14 and 15 limitations. Specifically, Ahmed identifies the problem in filters such as the one disclosed in Koyama of resonance between inductors and capacitor components, which may lead to ringing, voltage overshoot and instability at particular resonant frequencies. Ex. 1212, Abstract, 6; Ex. 1220, [0018]-[0019], [0027]; Ex. 1202, ¶ 285. To reduce this resonance, *e.g.*,

Ahmed teaches that an LC filter as shown on the left in the figures below can be modified by adding a series-connected resistor and capacitor (**blue**), or additionally modified with an additional inductor in parallel with the resistor (**green**). Ex. 1202, ¶ 272.

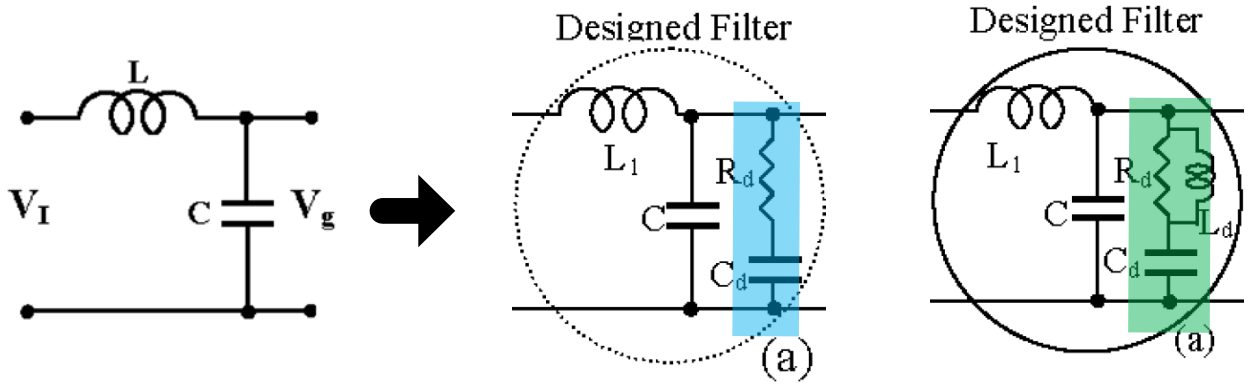
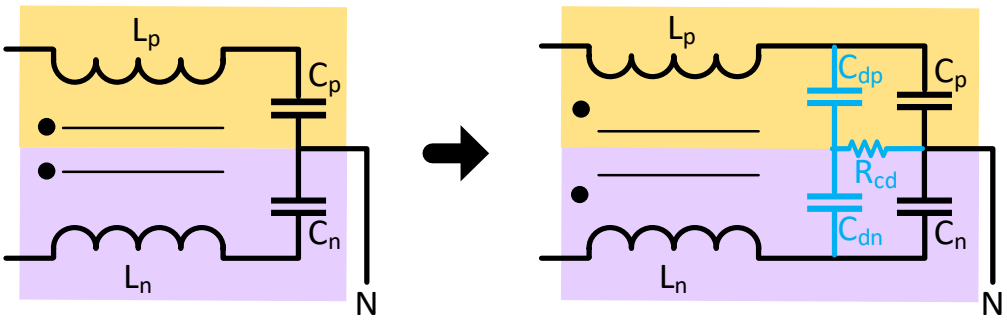


Fig. 2(b) (excerpt) Fig. 14(a) (excerpt) Fig. 15(a) (excerpt)

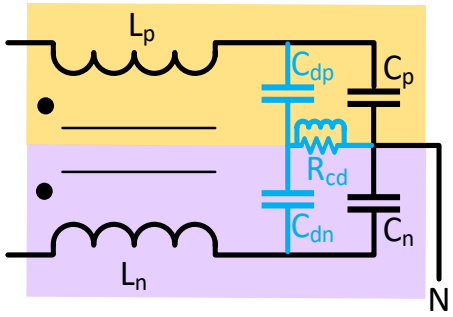
Ex. 1212, Figs. 2(b), 14(a), 15(a) (excerpted and annotated)

A PHOSITA at the time would have understood how to apply these damping techniques taught to the equivalent common mode versions of these filters, which are illustrated below. Ex. 1202, ¶ 286.



In the left figure, the common mode LC filter disclosed in Koyama includes a top half (**orange**) and a bottom half (**purple**). Each half is analogous to the filter

illustrated in the Ahmed Figure 2(b) above having a single series inductor and a capacitor connected between the power line (positive or negative) and neutral. Ex. 1202, ¶ 287. A PHOSITA would have understood that each half of the common mode filter would be modified according to the teachings of Ahmed to add a capacitor (C_{dp} and C_{dn}) analogous to C_d in Figure 14(a) connected through a resistor R_{cd} to neutral, where R_{cd} is the parallel equivalent of two resistors R_d in Ahmed Figure 14(a), one for each half of the common mode filter (shown above). *Id.* Similarly, Ahmed teaches to add an inductor analogous to L_d in Figure 15a in parallel with R_{cd}, as shown below. *Id.*



Koyama as modified by Ahmed above, thus discloses the claim 14 "damping resistor connected to the neutral output terminal; and a second pair of capacitors connected respectively from the positive and negative terminals of the battery to the other end of the damping resistor than the neutral terminal," and the claim 15 "inductor connected in parallel with said damping resistor." Ex. 1202, ¶ 288.

Using Ahmed's damping circuits as described above to modify Koyama's common mode filter would reduce resonance in the filter. Ex. 1202, ¶ 289. The

addition of the inductor in parallel with damping resistor provides the additional benefit of reducing power dissipation of the damping circuit. Ex. 1212, 7, 9; Ex. 1202, ¶ 289. As such, these combinations which disclose all of the features of claims 14 and 15, represent the obvious use of a known technique (inserting Ahmed's damping circuits in an LC filter) to improve a similar device (Koyama's common mode LC filter) in the same way (by suppressing the resonance between the choke and capacitors and reducing power dissipation of the damping resistor). Ex. 1202, ¶¶ 289-290. A PHOSITA was familiar with designing passive LC filter circuits, and would have had the skills to do so, resulting in an expectation of success. *Id*.

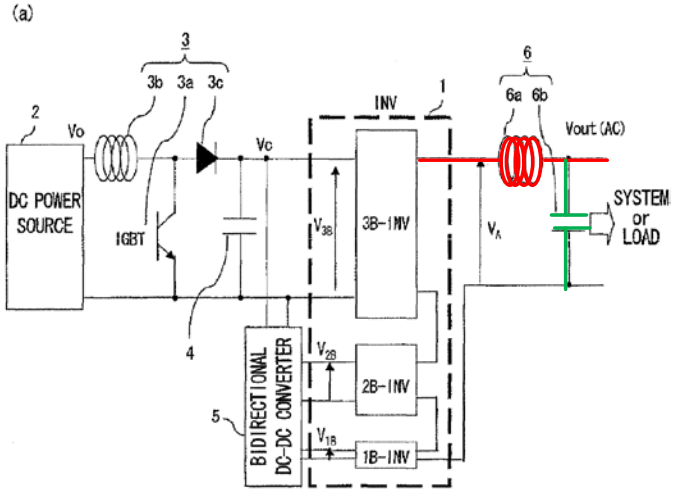
K. Ground N: Claim 16 is Rendered Obvious by Bowles-Iwata-Ahmed

Claim 16 depends from claim 1 and requires "a low-pass output filter comprising: an inductor connected between the sum voltage at the end of the series connection of switches and the hot output terminal; a first capacitor connected across the hot and neutral output terminals; a damping resistor connected to the neutral output terminal; and a second capacitor connected from the hot output terminal to the other end of the damping resistor than the neutral terminal." Ex. 1201, claim 16.

While Bowles discloses "a first capacitor [high frequency filter capacitor Cf] connected across the hot [output terminal 17] and neutral output [output terminal 19] terminals" that shunts high frequency signals, it does not disclose "an inductor

connected between the sum voltage at the end of the series connection of switches and the hot output terminal." Ex. 1232, 4:29-35, Fig. 2; Ex. 1202, ¶ 295. Iwata does.

Specifically, Iwata discloses a low-pass filter comprising an inductor (**red**) connected between the sum voltage at the end of the series connection of switches and the hot output terminal, and a first capacitor (**green**) connected across the hot and neutral output terminals. Ex. 1204, [0003], [0047], [0101], Figs. 1, 7, 14, 16-18; Ex. 1202, ¶ 296.

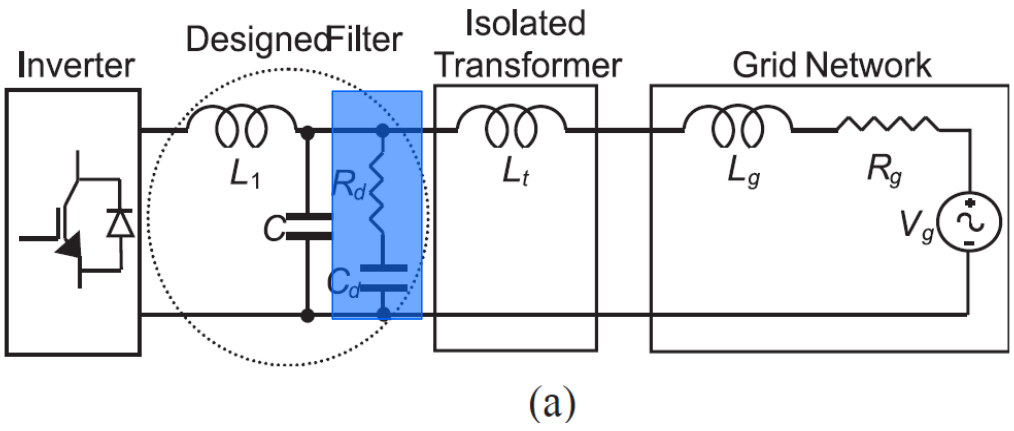


Ex. 1204, Fig. 1(a) (annotated)

A POSITA would have understood that low pass filters that consisted of an inductor in series with a load and a capacitor in parallel with a load, as shown in Iwata, were widely known and used low pass filters. Ex. 1202, ¶ 297. It would have been obvious to modify Bowles to implement a conventional low pass filter comprising inductor in series with a load and a capacitor in parallel with a load, as shown in Iwata, to filter high frequency signals more effectively than a circuit that

only utilizes a capacitor in parallel with a load. *Id*. Such a modification would have been nothing more than the use of a known technique (utilizing an LC filter at the output of an inverter) to improve a similar device (the "high frequency filter Cf" at the output of Bowles's inverter) in the same way (filtering high frequency signals more effectively). *Id*. A PHOSITA was familiar with filtering the output from inverters, and would have had the skills to do so, resulting in an expectation of success. *Id*.

Ahmed teaches to modify Bowles-Iwata's low pass filter to include the remaining claim 16 elements. Ex. 1202, ¶¶ 298-299, 274-276, 291-294. Ahmed discloses that LC filters can resonate, causing instability in the system, and adds a damping circuit (blue) with a resistor connected in series with a capacitor across the grid terminals (shown below) to attenuate those effects. Ex. 1212, 6-9 Figs. 1, 14; Ex. 1202, ¶ 298.



Ex. 1212, Fig. 14(a) (annotated)

A PHOSITA would have recognized that connecting the capacitor and series resistor in reverse order makes no functional difference. Ex. 1202, ¶ 299. Thus, Ahmed teaches the claim 16 "damping resistor connected to the neutral output terminal; and a second capacitor connected from the hot output terminal to the other end of the damping resistor than the neutral terminal." *Id*.

Modifying Bowles-Iwata's low pass filter by adding Ahmed's damping RC circuit would reduce unwanted resonance effects. Ex. 1212, 6-9; Ex. 1202, ¶ 300. As such, the combination of Bowles-Iwata with Ahmed, which discloses all of the limitations of claim 16, represents the obvious use of a known technique (inserting Ahmed's damping circuits in an LC filter) to improve a similar device (Bowles-Iwata's output LC filter) in the same way (by suppressing the resonance between the inductor and capacitor). Ex. 1202, ¶¶ 300-301. A PHOSITA was familiar with filtering the output from inverters, and would have had the skills to do so, resulting in an expectation of success. *Id*.

L. Ground O: Claim 17 is Rendered Obvious by Bowles-Phadke

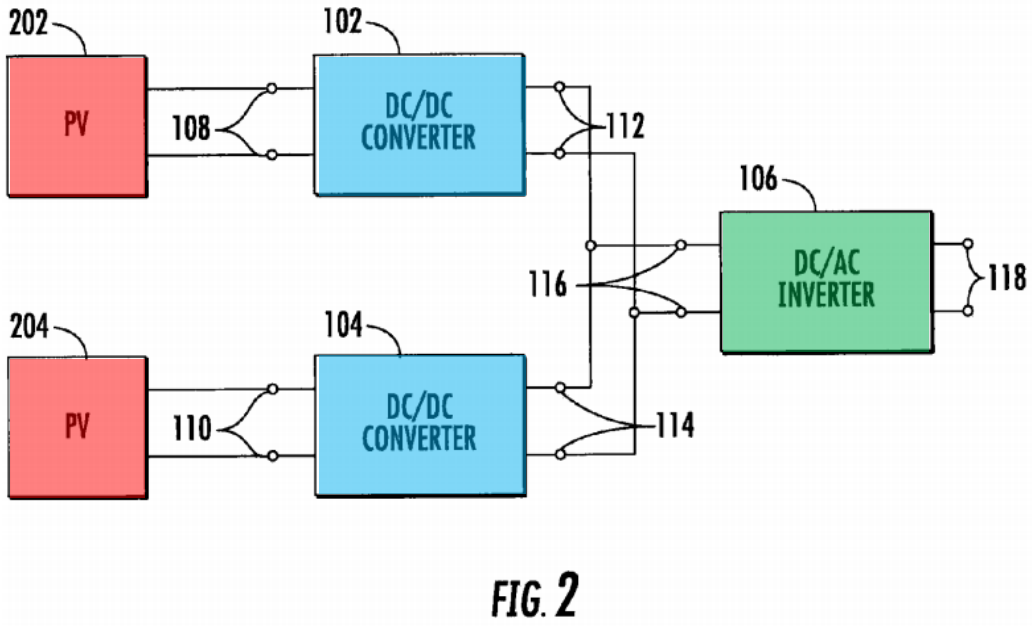
Claim 17 depends from claim 1 and requires:

> "a start-up in-rush current limiting circuit interposed between at least one of the controlled switches and its associated DC power source, the start-up in-rush current limiting circuit comprising:
>
> > one or more switches operative to insert a series impedance between the DC power source and the controlled switch when the DC to AC converter is initially powered on and no electrical load is connected to an AC output, and further operative to remove the series impedance and connect the DC power source

to the controlled switch when the in-rush current has dropped below a threshold."

Ex. 1201, claim 13.

Bowles does not disclose claim 17's "start-up in-rush current limiting circuit" between its DC power sources and controlled switches, but Phadke does. As shown below, Phadke discloses DC to DC converters (**blue**) attached between photovoltaic (PV) arrays (**red**) to provide power sources for an inverter (**green**). Ex. 1215, 1:14-16, 3:57-65, 4:32-41, 4:66-5:6; Ex. 1202, ¶ 309.



Ex. 1215, Fig. 2 (annotated)

Within the DC to DC converters, Phadke discloses the use of two stages with a switch 608 and resistor 606 inserted in parallel between the two stages, as shown in Figure 6 below. Ex. 1202, ¶ 310.

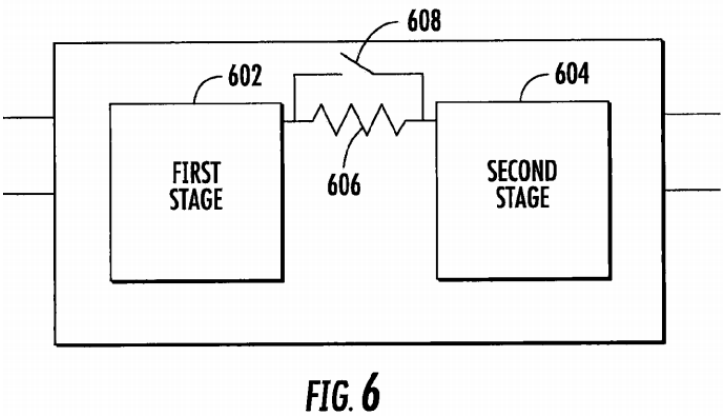


FIG. 6

Ex. 1215, Fig. 6

During the circuit's startup or to protect the circuit from damage before a load is connected correctly, Phadke discloses that switch 608 is held open so that resistor 606 ("a series impedance") is inserted to provide a high resistance path, limiting current flow to the second stage. Ex. 1215, 7:1-8, 7:19-27, *see also* 8:20-34, Fig. 7; Ex. 1202, ¶ 311. Once a certain threshold of current or voltage is reached, switch 608 is closed, thus removing any impedance between the two stages by effectively shorting resistor 606. Ex. 1215, 7:8-11, 8:44-56. Thus, Phadke discloses the "start-up in-rush current limiting circuit" of claim 17. Ex. 1202, ¶ 311.

It would have been obvious to use Phadke's startup circuit between one of Bowles's DC power sources and the controlled H-bridge switches. This would have been nothing more than combining known elements (Phadke's startup circuit and Bowles's power sources providing power to its H-bridge switches) according to known methods (inserting the startup circuit between the power source and switches as taught in Phadke) to yield predictable results (protecting Bowles's H-bridge

circuitry by limiting the amount of current entering the switches during startup). Ex. 1202, ¶ 312, 106. A PHOSITA was familiar with startup circuits, and would have had the skills to insert such a circuit between a power source and a switch, resulting in an expectation of success. *Id*.

Bowles-Phadke renders claim 17 obvious. Ex. 1202, ¶¶ 306-313.

VIII. GROUNDS FOR STANDING & FEE PAYMENT

Petitioner certifies that the '710 patent is available for *inter partes* review, and that Petitioner is not barred or estopped from requesting *inter partes* review challenging claims 1-17 on the identified grounds in this Petition.

The undersigned authorizes the charge of any required fees to Deposit Account No. 19-0733.

IX. CONCLUSION

For the foregoing reasons, *inter partes* review of claims 1-17 of the '710 patent should be instituted and claims 1-17 should be canceled. Ex. 1202, ¶¶ 314-316.

Dated: October 8, 2021

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CERTIFICATION UNDER 37 CFR § 42.24(d)

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for Inter Partes Review totals 13,865, which is less than the 14,000 allowed under 37 CFR § 42.24(a)(1)(i). This total includes 13,854 words as counted by the Word Count feature of Microsoft Word and 11 words used in annotations.

Pursuant to 37 C.F.R. § 42.24(a)(1), this count does not include the table of contents, the table of authorities, mandatory notices under § 42.8, the certificate of service, this certification of word count, the claims listing appendix, or appendix of exhibits.

BANNER & WITCOFF, LTD

Dated: October 8, 2021

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.105, I hereby certify that I caused a true and correct copy of the Petition 3 of 3 for *Inter Partes* Review in connection with U.S. Patent No. 10,784,710 and supporting evidence to be served via FedEx Priority Overnight on October 8, 2021, on the following:

COATS & BENNETT, PLLC (24112)
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An electronic courtesy copy is concurrently being e-mailed to the following:

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CLAIM LISTING APPENDIX

U.S. Pat. No. 10,784,710

Designation	Claim Language
Claim 1	
[1A]	1. A DC to AC converter having
[1B]	a transformerless output, and operative to convert DC power to an AC power having a desired voltage and waveform,
[1C]	and to output the AC power between hot and neutral output terminals,
[1D]	the DC to AC converter comprising: a plurality of controlled switches, each having a power input connection operative to accept DC power from an associated DC power source at an associated DC voltage, and
[1E]	each controlled switch further having a power output connection operative to output a selected one of: (a) the associated DC voltage, (b) the associated DC voltage having an inverted polarity, and (c) zero voltage, in response to an associated ternary-valued selection signal representing the multiplier values +1, −1, or 0 respectively,
[1F]	the power output connections of the plurality of switches being directly connected in series to output a sum voltage approximating the desired AC output voltage and waveform.
Claim 2	
2	2. The DC to AC converter of claim 1 wherein at least some of the DC voltages associated with the plurality of controlled switches have different values.
Claim 3	
3	3. The DC to AC converter of claim 1 wherein the desired voltage is a voltage of a standard household electricity supply and the desired waveform is sinusoidal at a standard household electricity supply frequency.
Claim 4	
4	4. The DC to AC converter of claim 1 wherein the controlled switches are MOSFETs connected in H-bridge configurations, and the associated DC power sources are floating relative to each other and relative to the DC to AC converter hot and neutral output terminals.
Claim 5	

Designation	Claim Language
5	5. The DC to AC converter of claim 1 wherein each associated DC voltage differs from another DC voltage nominally by a factor of 3.
Claim 6	
6	6. The DC to AC converter of claim 1 wherein the ternary-valued selection signals comprise pairs of binary bits, each bit pair having in total four combinations of possible values, of which two of the four combinations represent the zero multiplier value.
Claim 7	
[7A]	7. The DC to AC converter of claim 1 further comprising:
[7B]	a switch selection signal generator operative to produce the ternary-valued selection signals, the switch selection signal generator being configured to produce sets of switch selection signals, at given time instants, such that the sum voltage output is momentarily the best approximation to the instantaneous voltage values of the desired waveform at the given instants.
Claim 8	
[8A]	8. The DC to AC converter of claim 1 further comprising:
[8B]	a switch selection signal generator operative to produce the ternary-valued selection signals, the switch selection signal generator being configured to produce sequential sets of switch selection signals, and being configured to produce each new set of switch selection signals at a time instant at which the new set of switch selection signals would cause the sum voltage to be a better approximation to an instantaneous voltage value of the desired waveform at that time instant than the immediately previously output set of switch selection signals.
Claim 9	
[9A]	9. The DC to AC converter of claim 8 further comprising, where the desired waveform is repetitive:
[9B]	memory operative to store precomputed sequential sets of switch selection signals and the associated time instants at which each set is to be output; and
[9C]	wherein the switch selection signal generator is operative to retrieve the precomputed sequential sets of switch selection signals and associated time instants from the memory, and to output the switch selection signals at the associated times.

Designation	Claim Language
Claim 10	
10	10. The DC to AC converter of claim 1 wherein the DC power source having the highest voltage value is a battery and the DC power sources having lower voltages values comprise bi-directional DC-DC conversion circuitry operative to derive the lower voltage values from the battery.
Claim 11	
11	11. The DC to AC converter of claim 1 wherein the DC power source supplying the highest mean power is a battery and the DC power sources supplying lower mean power comprise bi-directional DC-DC conversion circuitry operative to derive the lower mean power from the battery.
Claim 12	
12	12. The DC to AC converter of claim 1 wherein one of the power output connections of the controlled switch having the associated DC power source of the highest associated DC voltage is one of the end terminals of the series connection, and is connected to the neutral output terminal.
Claim 13	
13	13. The DC to AC converter of claim 1 wherein the associated DC power source of one of the controlled switches is a battery, and further comprising a common-mode filter interposed between the battery and the controlled switch.
Claim 14	
[14A]	14. The DC to AC converter of claim 12 wherein the common mode filter comprises:
[14B]	a capacitor connected between DC power input terminals of the controlled switch;
[14C]	a common-mode choke connected between the battery and the DC power input terminals of the controlled switch;
[14D]	a first pair capacitors connected respectively from positive and negative terminals of the battery to the neutral output terminal;
[14E]	a damping resistor connected to the neutral output terminal; and
[14F]	a second pair of capacitors connected respectively from the positive and negative terminals of the battery to the other end of the damping resistor than the neutral terminal.
Claim 15	

Designation	Claim Language
15	15. The DC to AC converter of claim 14 further comprising an inductor connected in parallel with said damping resistor.
Claim 16	
[16A]	16. The DC to AC converter of claim 1 further comprising a low-pass output filter comprising:
[16B]	an inductor connected between the sum voltage at the end of the series connection of switches and the hot output terminal;
[16C]	a first capacitor connected across the hot and neutral output terminals;
[16D]	a damping resistor connected to the neutral output terminal; and
[16E]	a second capacitor connected from the hot output terminal to the other end of the damping resistor than the neutral terminal.
Claim 17	
[17A]	17. The DC to AC converter of claim 1 further comprising a start-up in-rush current limiting circuit interposed between at least one of the controlled switches and its associated DC power source, the start-up in-rush current limiting circuit comprising:
[17B]	one or more switches operative to insert a series impedance between the DC power source and the controlled switch when the DC to AC converter is initially powered on and no electrical load is connected to an AC output, and further operative to remove the series impedance and connect the DC power source to the controlled switch when the in-rush current has dropped below a threshold.