UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

LED WAFER SOLUTIONS LLC.
Patent Owner

Patent No. 8,952,405

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,952,405

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I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner" or "Samsung") requests *inter partes* review of claims 1-17 ("the challenged claims") of U.S. Patent No. 8,952,405 ("the '405 patent") (Ex. 1001), which, according to PTO records, is assigned to LED Wafer Solutions LLC. ("Patent Owner" or "PO"). For the reasons discussed below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES

Real Parties-in-Interest: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc.

Related Matters: The '405 patent is at issue in *LED Wafer Solutions LLC v. Samsung Electronics Co., Ltd. et al*, Case No. 6:21-CV-00292.

Counsel and Service Information: Lead counsel: Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), and (2) Paul M. Anderson (Reg. No. 39,896). Service information is Paul Hastings LLP, 2050 M St., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-LEDWafer-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '405 patent is available for review, and Petitioner is not barred/estopped from requesting review on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

Claims 1-17 should be canceled as unpatentable based on the following grounds:

Ground 1: Claims 1-3, 5-6, and 8-16 are rendered obvious by U.S. Patent Publication No. 2010/0148198 to Sugizaki *et al.* ("Sugizaki") (Ex. 1005) and U.S. Patent No. 7,419,839 to Camras *et al.* ("*Camras*") (Ex. 1006);

Ground 2: Claim 4 is rendered obvious by Sugizaki, Camras, and U.S. Patent Publication No. 2009/0001869 to Tanimoto et al. ("Tanimoto") (Ex. 1007);

Ground 3: Claims 7 and 17 are rendered obvious by Sugizaki, Camras, and U.S. Patent Publication No. 2008/0031295 to Tanaka ("Tanaka") (Ex. 1008);

Ground 4: Claims 1, 3, and 8-16 are rendered obvious by Sugizaki and the Applicant Admitted Prior Art ("AAPA")[1].

The '405 patent issued February 10, 2015, from U.S. App. No. 13/413,293 ("the '293 application"), filed March 6, 2012. The '405 patent claims priority to U.S. Provisional Patent Application Nos. 61/449,685 (Ex. 1013) and 61/449,686 (Ex. 1014) ("the provisional applications"), both of which were filed March 6, 2011. However, the claims of the '405 patent are not entitled to priority to the provisional applications as the only independent claims, claims 1 and 12, recite "an intrinsic region" where the positioning of the intrinsic region is specified in claim 1 as being between a positively-doped region and a negatively-doped region and specified in claim 12 as "between said positively-doped layer and a first surface of said LED." (Ex. 1001, 8:8-10, 9:27-30.) Neither of the provisional applications provides written description support for these features (*See* Exs. 1013, 1014), and therefore the earliest possible priority date for the '405 patent is the March 6, 2012 filing date of the '293 application. While the provisional applications mention an intrinsic layer,

[1] AAPA qualifies as prior art at least under pre-AIA 35 U.S.C. §§ 102(a) and 311(b) for the '137 patent. *See, e.g.*, *One World Techs., Inc. v. Chamberlain Group, Inc.*, IPR2017-00126, slip op. at 9-10 (May 4, 2017) (Paper 8); *see also Apple Inc., v. Qualcomm Inc.,* IPR2018-01316, slip op. at 22 (January 18, 2019) (Paper 7).

they do not provide any specificity as to where the intrinsic layer is positioned relative to other layers in the light emitting diode (LED) structure disclosed. (*Id*.)

Sugizaki was published on June 17, 2010. Camras issued September 2, 2008. Tanimoto was published January 1, 2009. Tanaka published on Feb. 7, 2008. Thus, based on the March 6, 2012 filing date of the '293 application, which is the earliest possible priority date for the '405 patent, all of these references qualify as prior art to the '405 patent under pre-AIA 35 U.S.C. § 102(b). Even if the March 6, 2011 filing date of the provisional applications is taken as the priority date for the '405 patent, Camras, Tanaka, and Tanimoto are still prior art under pre-AIA 35 U.S.C. § 102(b), while Sugizaki is prior art at least under pre-AIA 35 U.S.C. § 102(e). None of these references were considered during prosecution. (*See generally* Ex. 1004.)

VI. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art as of the claimed priority date of the '405 patent ("POSITA") would have had a bachelor's degree in electrical engineering, material science, or the equivalent, and two or more years of experience with light emitting diodes (LEDs). (Ex. 1002, ¶¶20-21.)[2] More education can supplement practical experience and vice versa. (*Id.*)

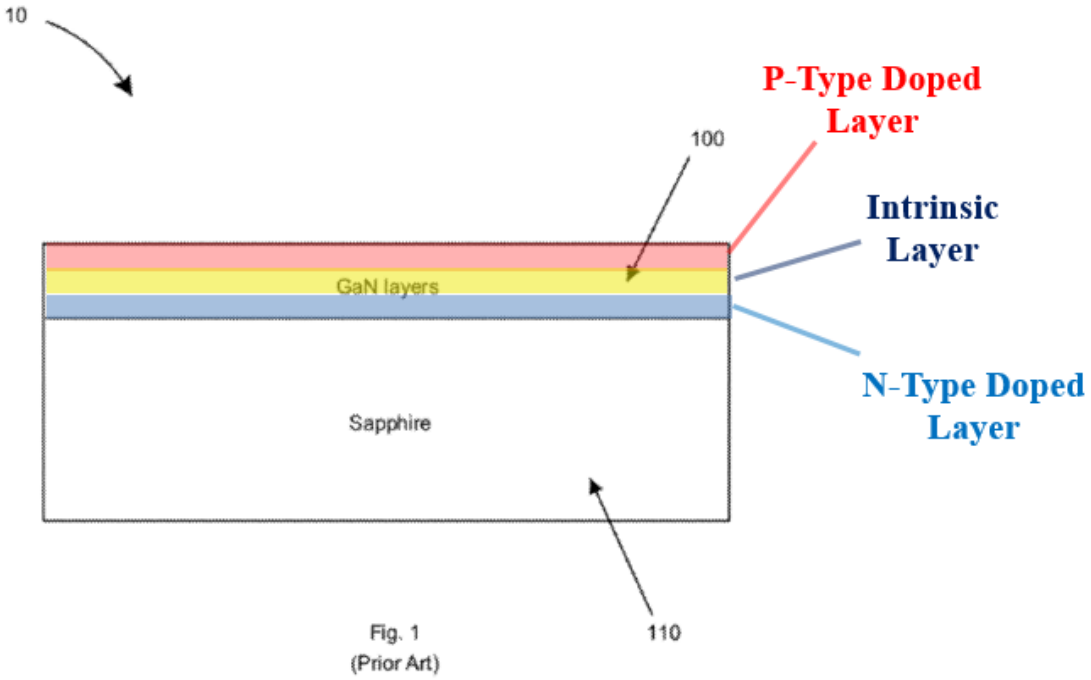
[2] Petitioner submits the declaration of Dr. R. Jacob Baker, Ph.D., P.E. (Ex. 1002), an expert in the field of the '405 patent. (Ex. 1002, ¶¶5-15; Ex. 1003.)

VII. THE '405 PATENT

The '405 patent is entitled "Light Emitting Diode Package and Method of Manufacture" and describes the structure and formation of LED devices. (Ex. 1001, Title; Ex. 1002, ¶¶30-38.) The '405 patent "is directed to a light emitting diode (LED) device implemented on a wafer cover layer and provided with features permitting efficient and repeatable manufacture of the same." (Ex. 1001, 1:13-16.) The '405 patent states that conventional LED packaging includes silicon or ceramic carrier substrates, which can increase the manufacturing costs for such LEDs. (*Id*., 1:55-63.) According to the '405 patent, the carrier substrate can also adversely affect the heat removal characteristics for the LED. (*Id*., 1:63-65.) In attempting to overcome these issues, the '405 patent discloses embodiments where "the LED is manufactured by epitaxial growth or other chemical or physical deposition techniques of a plurality of layers," where "[c]ertain layers act to promote mechanical, electrical, thermal, or optical characteristics of the device." (*Id*., 2:2-8.)

Figures 1 and 2 of the '405 patent illustrate prior art gallium nitride (GaN) LEDs that "are typically grown on a sapphire substrate." (*Id*., 3:10-13, 3:34-36, 3:44-46.) According to the '405 patent, "[t]hese LEDs comprise a P-I-N junction device having an intrinsic (I) layer disposed between an N-type doped layer and a P-type doped layer." (*Id*., 3:13-16.) Figure 1 of the '405 patent is annotated below to show the doped and intrinsic layers that the '405 patent describes as being present

in the prior art LED devices. (*Id*., 3:9-16, 3:33-35 ("FIG. 1 illustrates a LED device 10 such as those described above . . . .").)



(*Id*., FIG. 1 (annotated); Ex. 1002, ¶31.)

Similarly, figure 2 of the '405 patent, annotated below to show the doped and intrinsic layers, illustrates a prior art LED device "like the one shown in FIG. 1 where a GaN layer 200 is disposed above a sapphire layer 210" and "a recess or groove or channel 202 is etched into a portion of the GaN layer 200." (Ex.1001, 3:44-47.)

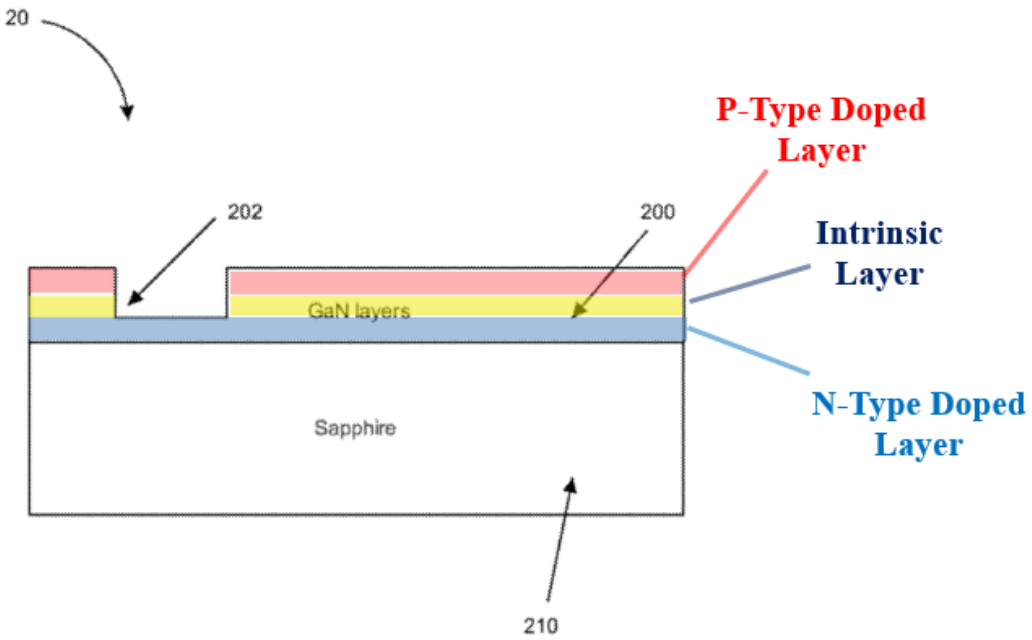
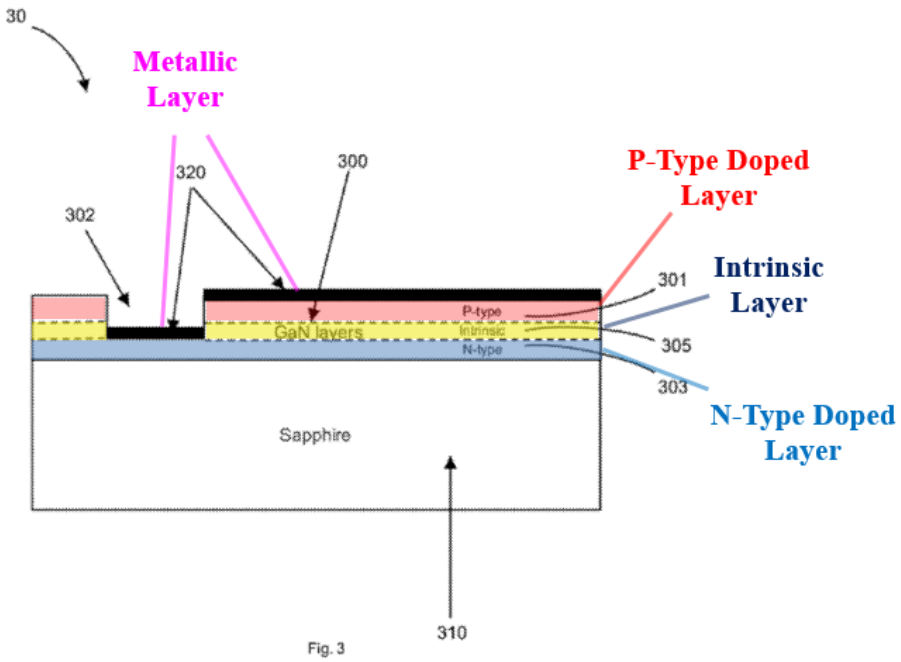


Fig. 2
(Prior Art)

(*Id*., FIG. 2 (annotated); Ex. 1002, ¶32.)

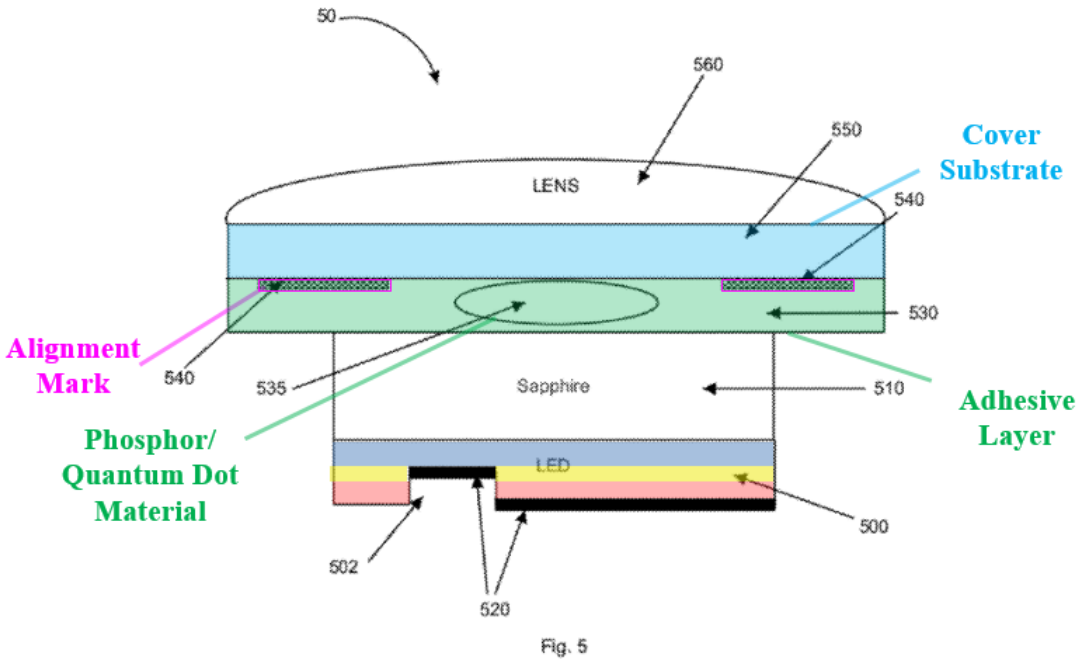
Building on the basic prior art structure of the LED, figure 3 shows "the result of metallization of the surface of the GaN layer 200 of the device of FIG. 2," where "the GaN layer 300 comprises a P-I-N junction having strata therein including a P-type doped layer 301 that is proximal to the bulk surface of the GaN layer 300 and distal from the sapphire layer 310, a N-type doped layer 303 within GaN layer 300 that is proximal to the sapphire layer 310, and an intrinsic (I) semiconductor layer 305 in the middle, between the P and N type layers 301 and 303." (Ex. 1001, 3:64-4:8.)



(*Id*., FIG. 3 (annotated); Ex. 1002, ¶33.)

The metallization is provided in order to provide contacts to the P- and N-type regions such that current flows through the LED to cause photon emission from the intrinsic layer 305. (Ex. 1001, 4:8-10 ("In operation, electrical biasing of the P-type layer 301 against the N-type layer 303 causes photon emission from intrinsic layer 305."), 4:22-27 ("In this way, a set of contacts can be applied to the N-type layer 303 and the P-type layer 301 to drive or excite the LED device 30. Current can thus generally flow from a conducting electrode coupled to the N-type layer 303 to another conducting electrode coupled to the P-type layer 301.").)

Figure 5 of the '405 patent provides a cross sectional view of an LED device 50 that includes the LED shown in figure 3 above, where the figure 3 structure has been flipped vertically so that the sapphire substrate is on the top of the LED. (*Id.*, 4:65-5:2, FIGs. 3, 5.)

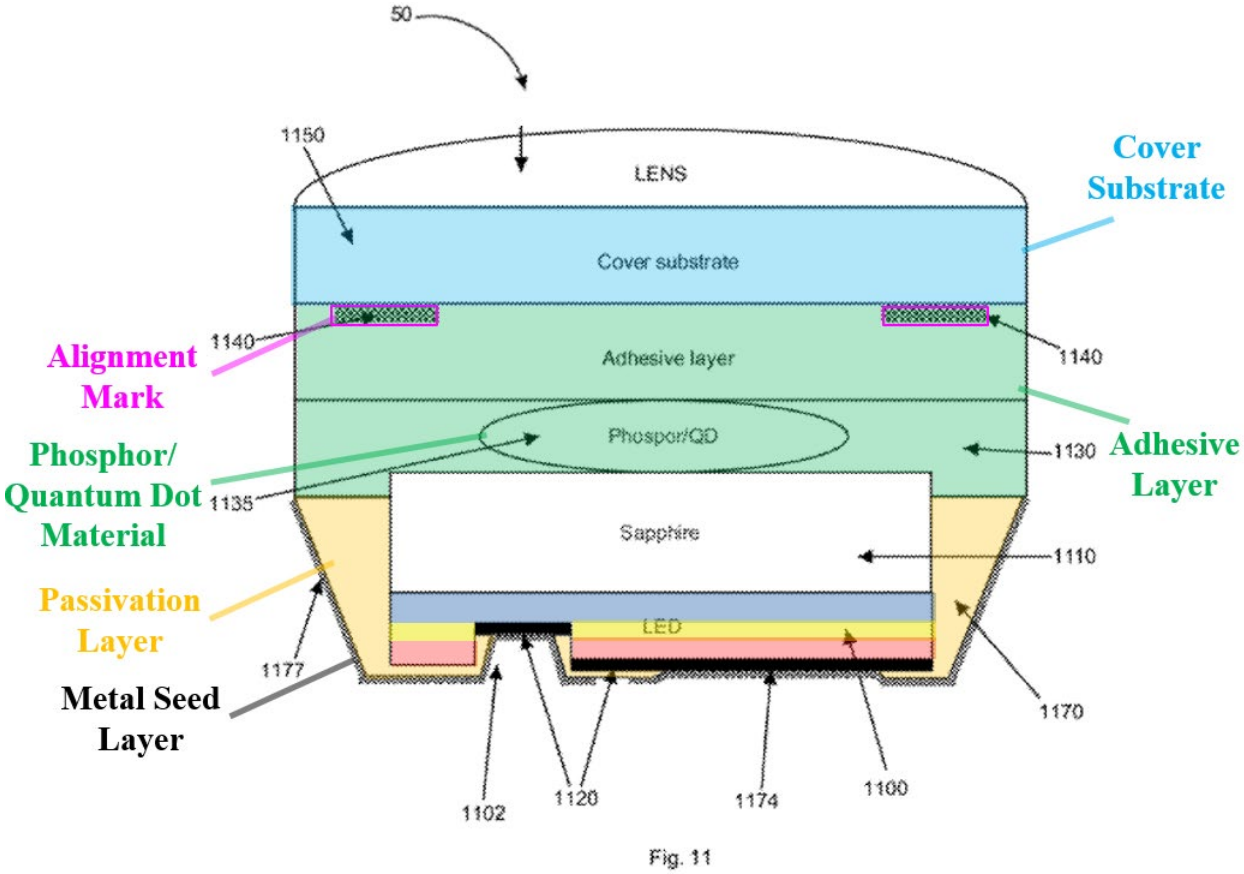


(*Id.*, FIG. 5 (annotated); Ex. 1002, ¶35.)

As shown in annotated figure 5 above, the LED device 50 includes "an optically transparent or transmissive adhesive layer 530," where "[w]ithin, or contiguous to transparent adhesive layer 530 is a region containing phosphor and/or quantum dot material (QD) 535." (Ex. 1001, 5:3-8, 5:15-17.) The LED device 50 also includes alignment marks 540 on the adhesive layer 530 that are used to align the LED body over a cover substrate 550. (*Id.*, 5:24-27.) The cover substrate 550

is "transparent or optically transmissive to light in the wavelength emitted by LED layer 500 or by the combination of the LED layer 500 and the phosphor material." (*Id*., 5:29-32.) An optical lens 560 on the cover substrate 550 "can act to spread, diffuse, collimate, or otherwise redirect and form the output of the LED." (*Id*., 5:33-37.)

Figure 11 illustrates another embodiment of an LED device that also includes passivation layer 1170 and a metal seed layer 1177 applied to the passivation layer. (*Id*., 7:24-26, FIG. 11.)



(*Id*., FIG. 11 (annotated); Ex. 1002, ¶37.)

The ’405 patent discloses that the passivation layer can be a non-conductive layer such as SiO_2, SiN, AlN, Al_2O_3 or an organic material such as epoxy or electrophoretic deposited paint. (Ex. 1001, 6:14-20.) The passivation layer is shown in figure 11 to be shaped to provide optical reflectivity. (*Id*., 6:33-38.) The contact holes can be drilled or etched through the passivation layer. (*Id*., 6:47-59.) The metal seed layer 1177 provides enhanced electrical conductivity, heat removal, and reflectivity of light. (*Id*., 7:43-47.)

As explained below and in the accompanying declaration of Dr. Baker, all the limitations in the challenged claims were known in the prior art. (*See infra* Section IX; Ex. 1002 ¶¶40-179; *see also* Ex. 1002, ¶¶22-29 (technical background), citing Ex. 1023.)

VIII. CLAIM CONSTRUCTION

During IPR, claims are construed according to the “*Phillips* standard,” as set forth in *Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 83 Fed. Reg. 51341 (Oct. 11, 2018). The Board only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015). Petitioner believes that no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims. (Ex. 1002, ¶39.)

IX. DETAILED EXPLANATION OF GROUNDS

A. Ground 1: Claims 1-3, 5-6, and 8-16 Are Obvious Over Sugizaki In View of Camras

1. Claim 1

a) A light emitting device, comprising:

To the extent the preamble of claim 1 is limiting, Sugizaki discloses the limitations therein. (Ex. 1002, ¶51.) For instance, Sugizaki is entitled "Light Emitting Device and Method for Manufacturing Same" and discloses a "method for manufacturing a light emitting device . . . ." (Ex. 1005, Title, ¶[0007].) The light emitting device shown in figure 18B below constitutes a "light emitting device" as recited in claim 1. (*Id*., ¶¶[0031], [0027], [0092], FIG. 18B, Ex. 1002, ¶51.)

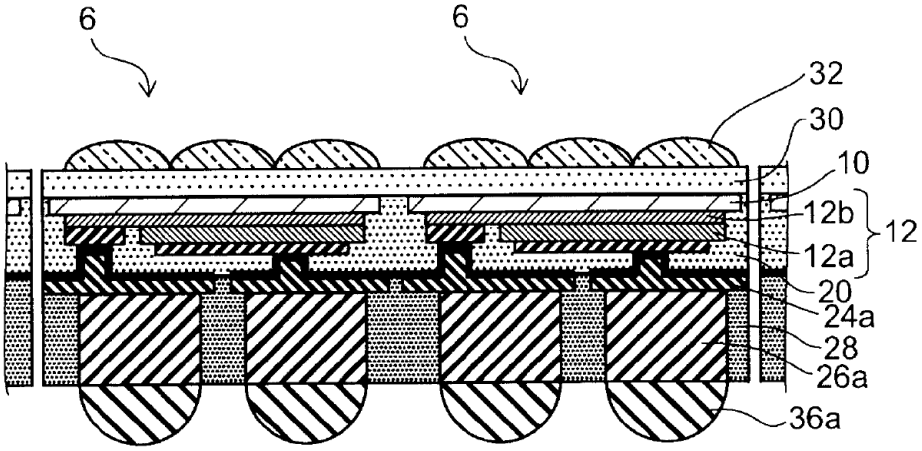


FIG. 18B

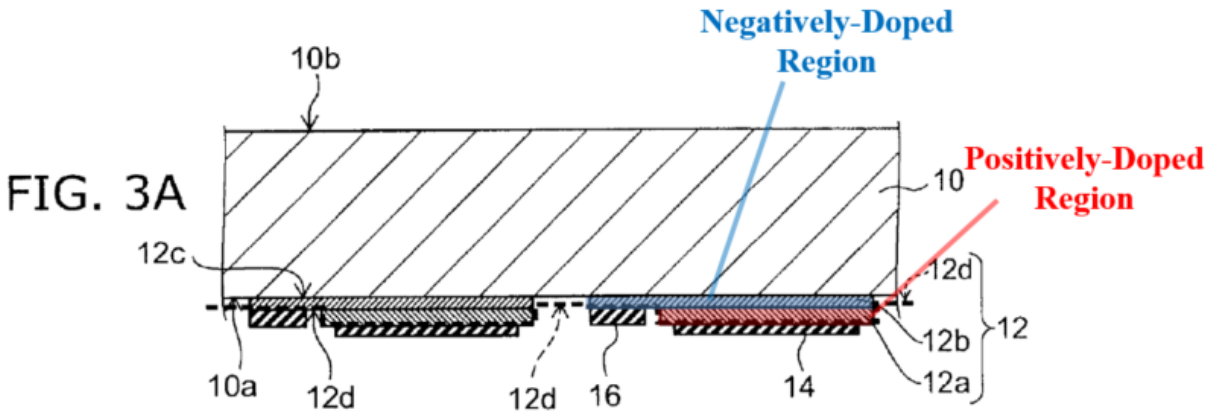
(Ex. 1001, FIG. 18B.)

b) a semiconductor LED including a positively-doped region, an intrinsic region, and a negatively-doped region, wherein said intrinsic region is between said positively-doped region and said negatively-doped region, said semiconductor LED defining a first recess to expose a negatively-doped surface of said negatively –doped region;

Sugizaki in view of Camras discloses or suggests these limitations. (Ex. 1002, ¶¶52-66.) For example, Sugizaki discloses that the light emitting device in figure 18B includes a multilayer body 12 ("semiconductor LED"), where details of the multilayer body 12 that are also applicable to figure 18B are described in the context of figures 1A and 1B of Sugizaki. Sugizaki discloses that the multilayer body "has an upper layer 12a, including a light emitting layer 12e, and a lower layer 12b." (Ex. 1005, ¶[0032].) Sugizaki further discloses that "[t]he upper layer 12a may include a p-type cladding layer" and "[t]he lower layer 12b may be of n-type and serve as a lateral path of current." (*Id*.) As described by Sugizaki, "light from the light emitting layer 12e can be emitted primarily from the first surface 12c of the multilayer body 12 in the upward direction of figure 1A." (*Id*., ¶[0039]; Ex. 1002, ¶52.)

Sugizaki discloses the formation of the multilayer body 12 of figure 18B in conjunction with figure 3A, which is replicated in annotated form below. As shown in figure 3A, the multilayer body 12 is formed to have a lower layer 12b "including a buffer layer and an n-type layer, and an upper layer 12a." (Ex. 1005, ¶[0047].)

Therefore, Sugizaki discloses that the multilayer body 12 ("semiconductor LED") includes a lower layer 12b ("negatively doped region") and an upper layer 12a ("positively doped region"). (Ex. 1002, ¶¶53-55.)



(Ex. 1005, FIG. 3A (annotated); Ex. 1002, ¶55.)

Sugizaki does not explicitly disclose "an intrinsic region" where the "intrinsic region is between said positively-doped region and said negatively-doped region" as recited in claim 1. However, Camras discloses an LED with an intrinsic region between a positively-doped region and a negatively-doped region, and it would have been obvious to form an LED as disclosed by Sugizaki such that an undoped layer ("intrinsic region") is included between the positively-doped (p-type) and negatively-doped (n-type) regions. (Ex. 1002, ¶¶56-63.)

Camras, like Sugizaki, is directed to LED structures formed on a sapphire substrate that include an n-type layer, a p-type layer, and a light emitting active region. (Ex. 1006, 2:27-32, 2:44-61.) Camras discloses that the light emitting active

region of the LED is between p-type layer 110 and n-type layer 108 and includes intrinsic (undoped) material. (Ex. 1006, 2:44-54 ("**active region 112 includes one or more semiconductor layers that are** doped n-type or p-type or are **undoped**") (emphasis added); Ex. 1002, ¶57.) Camras further discloses that "[a]ctive region 112 emits light upon application of a suitable voltage across contacts 114 and 116." (*Id*., 2:62-63.) Figure 1B of Camras, shown in annotated form below, illustrates the intrinsic layer 112 between p-type layer 110 and n-type layer 108.

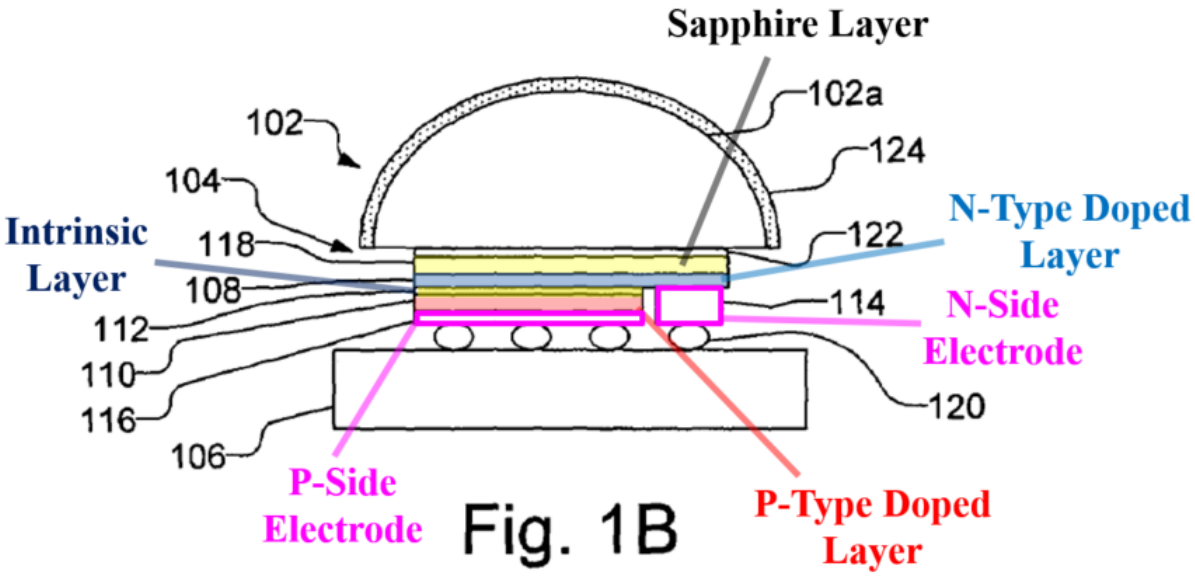


Fig. 1B

(Ex. 1006, FIG. 1B (annotated); Ex. 1002, ¶58.)

A POSITA would have looked to Camras for guidance regarding implementing LED devices as disclosed by Sugizaki, particularly because Camras and Sugizaki are references in the same field that disclose LED devices with many common features. (Ex. 1002, ¶59.) Having looked to Camras, such a POSITA

would have found it obvious to implement the light-emitting layer in Sugizaki such that it includes an intrinsic layer between the p-type and n-type doped regions. (*Id*.)

The multilayer body 12 disclosed by Sugizaki is specified to include a p-type layer, an n-type layer, and a light emitting layer. (Ex. 1005, ¶[0032].) Sugizaki, however, does not disclose specific details regarding the composition of the light emitting layer. As discussed above, Camras discloses LED structures that include multilayer bodies with an intrinsic light-emitting layer sandwiched between p-type and n-type regions. (Ex. 1006, 2:44-52.) A POSITA would have found it obvious to use a multilayer body that includes an intrinsic light-emitting layer between the p-type and n-type doped regions, as disclosed by Camras, in conjunction with an LED device as disclosed by Sugizaki. (Ex. 1002, ¶60.) Sugizaki does not disclose the details of the composition of the light emitting layer included in its LED device, and therefore a POSITA would have looked to Camras, which discloses such details. (*Id*.)

Such a POSITA would also have been motivated to use an intrinsic layer for the light emitting layer in an LED as disclosed by Sugizaki because using an intrinsic layer is one of a limited number of alternatives disclosed by Camras, where those alternatives include p-type, n-type and intrinsic semiconductor material. (Ex. 1006, 2:50-52; Ex. 1002, ¶61.) Indeed, the '405 patent discloses that LEDs with an intrinsic layer between p-type and n-type material were known and in use. (*See*

supra Section VII; Ex. 1001, 3:9-16, 3:33-35, 3:44-47, 3:64-4:8, FIGs. 1-3; Ex. 1002, ¶61.) Similarly, Sugawara also demonstrates that a POSITA would have been aware of the use of intrinsic layers between p- and n-type layers in LEDs. (Ex. 1009, 3:45-51.)[3]

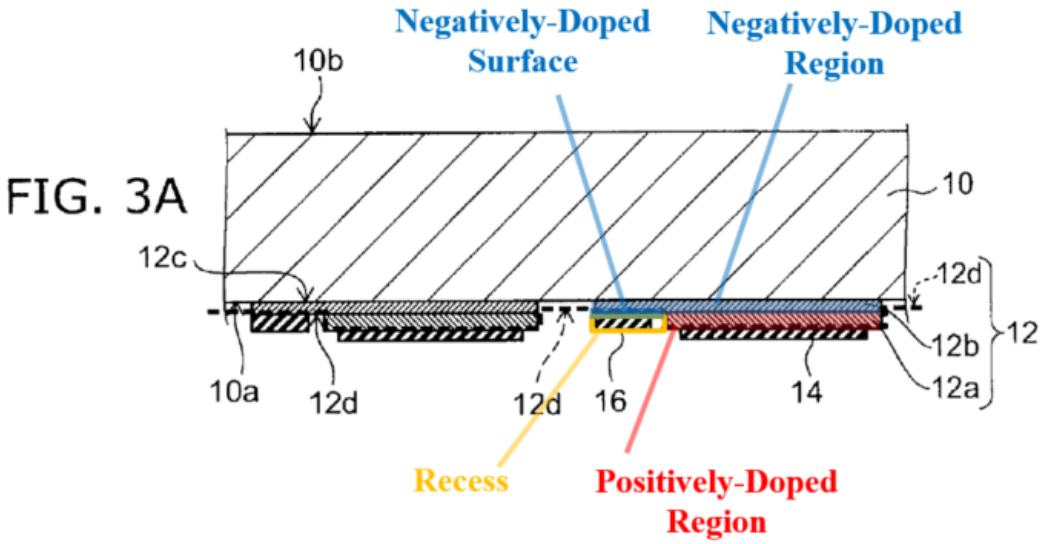
A POSITA reading Sugizaki would have understood that various known light-emitting multilayer bodies could be used in conjunction with Sugizaki's LED devices. (Ex. 1002, ¶62.) Indeed, Sugizaki explicitly contemplates that the use of different multilayer structures. (Ex. 1005, ¶[0104]; Ex. 1002, ¶62.)

A POSITA would have found it straightforward to use an intrinsic layer as disclosed by Camras in an LED device as disclosed by Sugizaki because Camras discloses such an intrinsic layer in a device very similar to that of Sugizaki. (Ex. 1002, ¶63.) Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-18 (2007). Moreover, such a skilled person would have had a reasonable expectation of success because, as demonstrated by Camras, as well as Sugawara and the '405 patent (*see supra* Section VII.A; Ex. 1001, 3:9-16, 3:33-35, 3:44-47, 3:64-4:8, FIGs. 1-3), LEDs

[3] Sugawara is cited to demonstrate the knowledge of a POSITA at the time of the alleged invention.

with intrinsic light-emitting layers were well known in the art, and Sugizaki specifically contemplates using different multilayer bodies with the light emitting device embodiments disclosed. *See Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1364 (Fed. Cir. 2007) ("only a reasonable expectation of success, not a guarantee, is needed" in an obviousness analysis). Therefore, the Sugizaki-Camras combination discloses or suggests a multilayer structure 12 like that shown in the figures of Sugizaki, where the multilayer structure includes an intrinsic layer sandwiched between p-type and n-type regions ("an intrinsic region . . . between said positively-doped region and said negatively-doped region"). (Ex. 1002, ¶63.)

The Sugizaki-Camras combination also discloses or suggests a first recess that exposes a negatively-doped surface of the negatively-doped region as recited in claim 1. (Ex. 1002, ¶¶64-66.) For example, Sugizaki discloses that a portion of the positively-doped region 12a is removed to expose the surface of the negatively-doped region 12b. (Ex. 1005, ¶[0047]; FIG. 3A.) In the Sugizaki-Camras combination, in order to expose the negatively-doped surface, the portion removed would include a portion of the intrinsic layer ("intrinsic region"). (Ex. 1002, ¶64.) The exposure of the negatively-doped region results in the second surface of the multilayer body having a step difference ("said semiconductor LED defining a first recess to expose a negatively-doped surface of said negatively-doped region") shown in figures 3A and 18B below. (Ex. 1005, ¶[0047].)



(Ex. 1005, FIG. 3A (annotated); Ex. 1002, ¶65.)

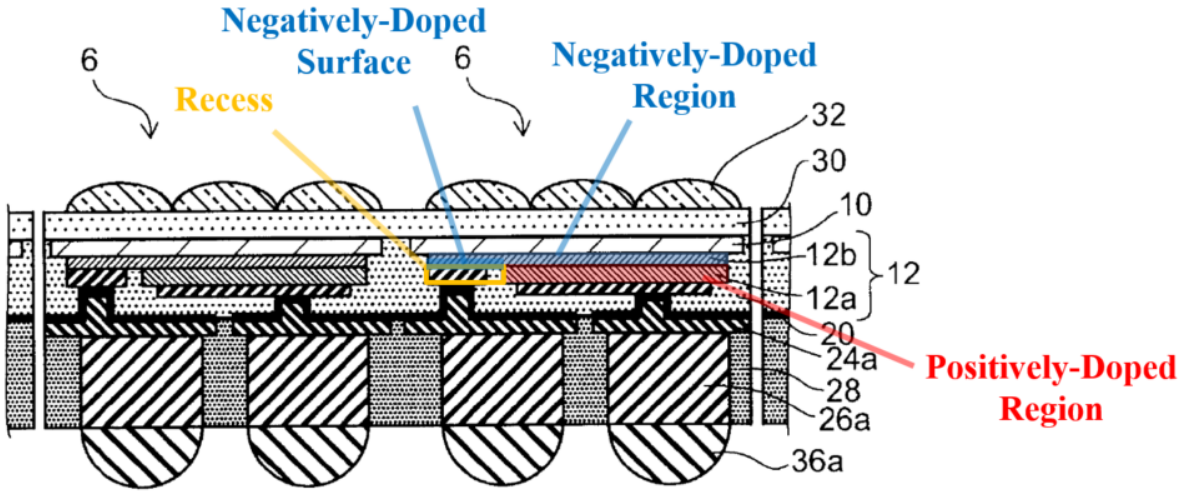


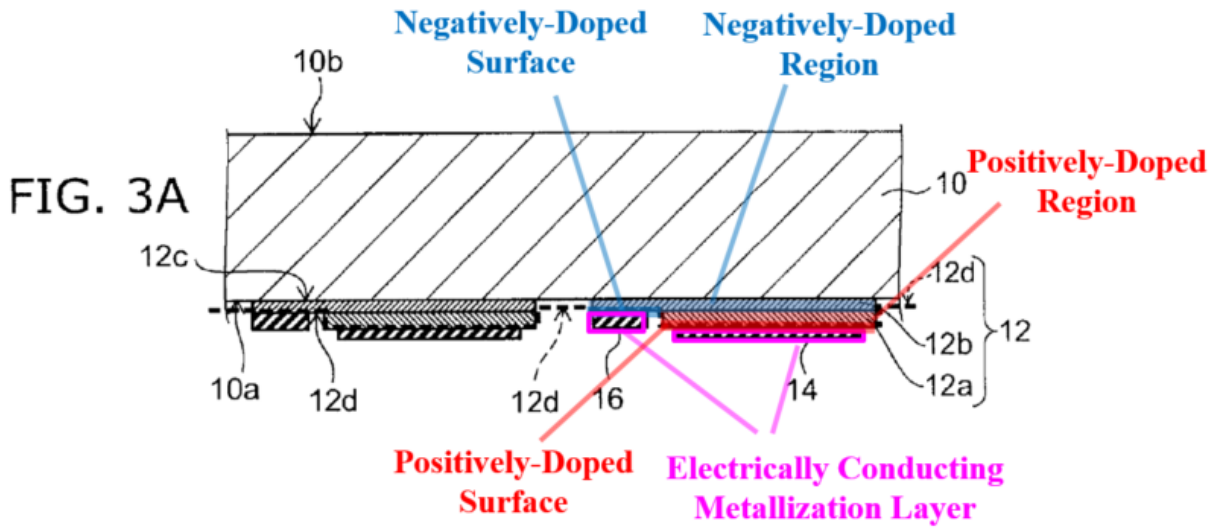
FIG. 18B

(Ex. 1005, FIG. 18B (annotated); Ex. 1002, ¶66.)

Therefore, the Sugizaki-Camras combination discloses or suggests the features of claim element 1(b). (Ex. 1002, ¶66.)

c) an electrically conducting metallization layer in direct contact with at least a portion of each of a positively-doped surface and said negatively-doped surface of said semiconductor LED, wherein said positively-doped surface is on an exposed portion of said positively-doped region of said semiconductor LED and said negatively-doped surface and said positively-doped surface are parallel with each other;

The Sugizaki-Camras combination discloses or suggests these limitations. (Ex. 1002, ¶¶67-70.) For instance, Sugizaki describes formation of "an electrically conducting metallization layer" that includes a p-side electrode 14 and an n-side electrode 16 in conjunction with figure 3A below. (Ex. 1002, ¶67.)



(Ex. 1005, FIG. 3A (annotated); Ex. 1002, ¶67.)

The p-side electrode 14 of the metallization layer is "provided on the surface of the upper layer 12a of the multilayer body" (Ex. 1005, ¶[0033]), and therefore is "in direct contact with at least a portion of . . . a positively-doped surface . . . of said

semiconductor LED" as recited in claim element 1(b). (*Id*., ¶[0048]; *see also id*., ¶[0033]; Ex. 1002, ¶69.) Similarly, "the n-side electrode is formed on the surface of the lower layer 12b" (Ex. 1005, ¶[0048]), and therefore constitutes a portion of the metallization layer that is "in direct contact with at least a portion of . . . said negatively-doped surface of said semiconductor LED." (Ex. 1002, ¶69.)

Sugizaki discloses that the electrodes 14 and 16 are made using metal. (Ex. 1005, ¶[0049].) While Sugizaki discloses forming example multi-layer electrodes that include multiple metal layers, it would have been obvious to form the electrodes 14 and 16 by depositing an electrically conducting metallization layer on the positively- and negatively-doped surfaces of the LED as such electrode formation was a well-known technique widely used in LED device formation. (Ex. 1002, ¶68.) Such an understanding is supported by Camras, which discloses that p- and n-contacts similar to the Sugizaki's electrodes can be formed using metal. (Ex. 1006, 3:8-12, 2:50-56, FIGs. 1A, 1B.) As confirmed by the '405 patent, the formation of contacts or electrodes by deposition of metal was well-known and the "state of the art method of electrode formation." (Ex. 1001, 4:15-35; *see also* Ex. 1009, 11:47-12:3.)

Because the portion of the metallization layer corresponding to the p-side electrode 14 is formed on the surface of the upper layer 12a, that surface is an "exposed surface" as that term is used in claim 1 of the '405 patent, and Sugizaki

discloses that the "positively-doped surface is on an exposed portion of said positively-doped region of said semiconductor LED" as recited in claim 1. (Ex. 1002, ¶69.) Moreover, as shown in figure 3A above, and as is consistent with the understanding of a POSITA based on the way such layers are formed, the "negatively-doped surface and said positively-doped surface are parallel with each other." (*Id.*)

Annotated figure 18B below shows the same features discussed above with respect to figure 3A, where the description in Sugizaki does not repeat the formation details of the electrodes that are also applicable to figure 18B. In other words, the description of the layers and formation of layers shown in figure 3A is also applicable to figure 18B. (Ex. 1002, ¶70.)

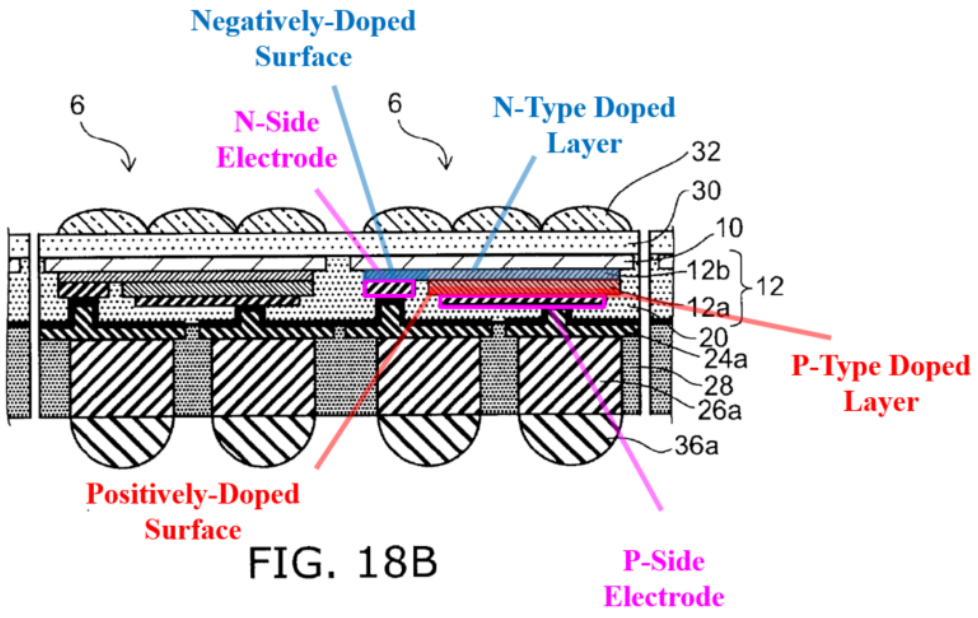
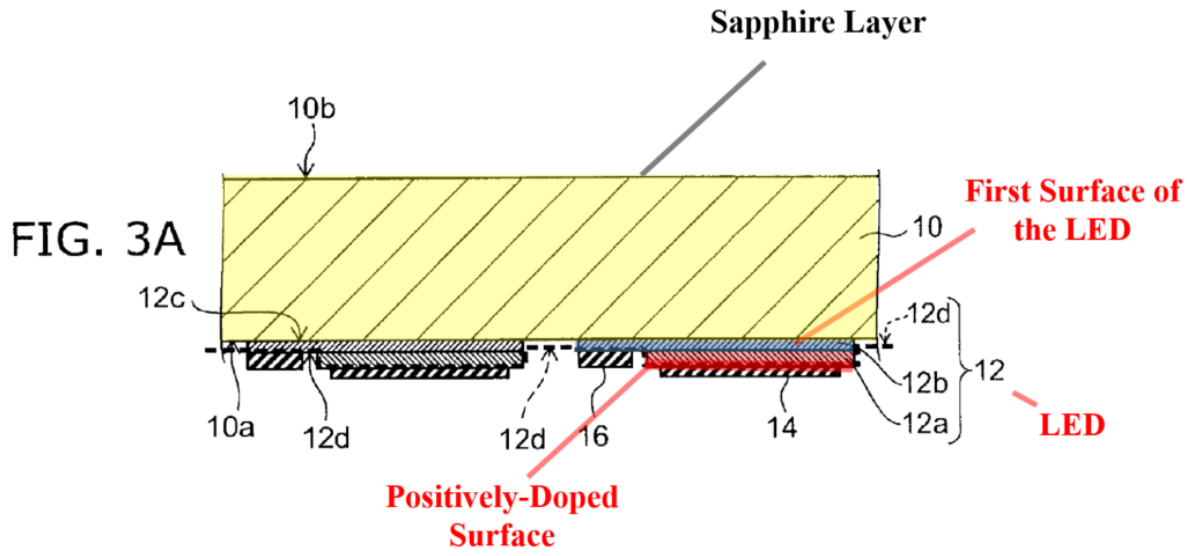


FIG. 18B

(Ex. 1005, FIG. 18B (annotated); Ex. 1002, ¶70.)

d) a sapphire layer in direct contact with a first surface of said semiconductor LED, said positively-doped surface and said first surface of said semiconductor LED being parallel with one another and on opposing faces of said semiconductor LED;

The Sugizaki-Camras combination discloses or suggests these limitations. (Ex. 1002, ¶¶71-74.) As shown in annotated figures 3A and 18B below, Sugizaki discloses that the layers of the LED 12 are formed on a translucent substrate 10 that is sapphire. (Ex. 1005, ¶[0047] ("translucent substrate 10 illustratively made of sapphire."); Ex. 1002, ¶71.)



(Ex. 1005, FIG. 3A (annotated); Ex. 1002, ¶71.)

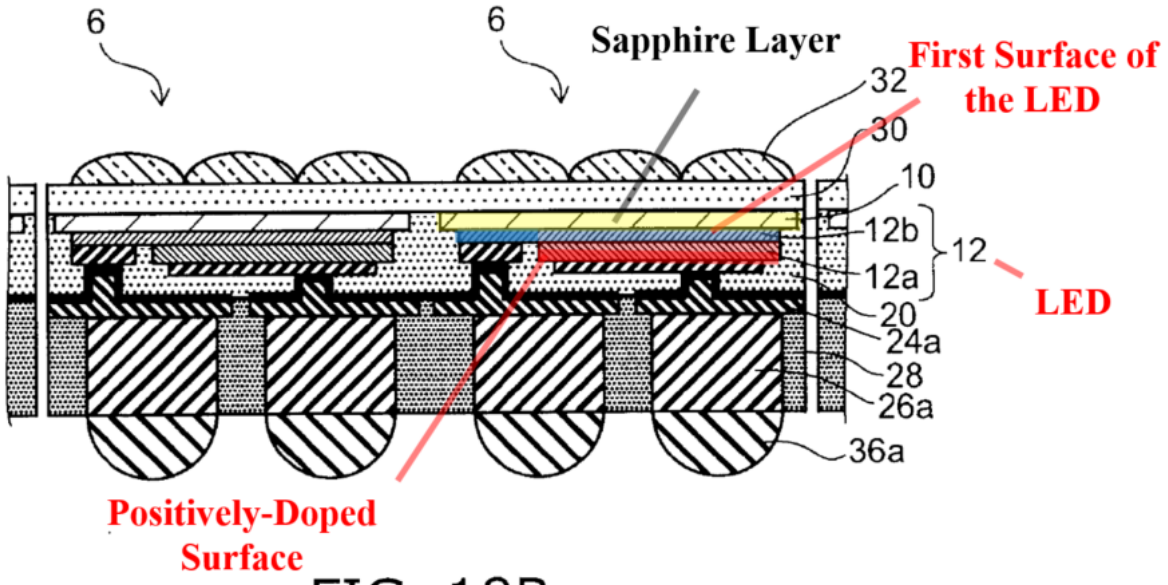


FIG. 18B

(Ex. 1005, FIG. 18B (annotated); Ex. 1002, ¶74.)

In figure 18B, the thickness of the sapphire substrate has been reduced by, for example grinding. (Ex. 1005, ¶[0044], FIG. 18B; Ex. 1002, ¶¶73-74.) As shown in figures 3A and 18B, the sapphire layer 10 is in "direct contact" with a first surface of the LED and, consistent with the understanding of a POSITA, the top face 12c of the LED in figure 3A ("first surface of said semiconductor LED") is parallel to the positively-doped surface of the LED, which is the bottom face the LED. (Ex. 1005, ¶[0047], FIG. 3A; Ex. 1002, ¶¶72, 74.) Therefore, Sugizaki discloses "said positively-doped surface and said first surface of said semiconductor LED being parallel with one another and on opposing faces of said semiconductor LED." (Ex. 1002, ¶74.)

e) an optically permissive layer in direct contact with said sapphire layer, said optically permissive layer comprising an optically definable material containing quantum dots and/or phosphor, said optically definable material adapted to change the frequency of at least some of emitted light passing therethrough;

The Sugizaki-Camras combination discloses or suggests this limitation. (Ex. 1002, ¶¶75-76.) As shown in annotated figure 18B below, Sugizaki discloses that a phosphor layer 30 is deposited on the surface of the sapphire layer 10. (Ex. 1005, ¶¶[0061], [0081], FIGs. 6A, 12A-12E, 18B.) Sugizaki further discloses that "the phosphor layer 30 can be formed to a thickness in the range from several to several hundred μm illustratively by a sputtering method, an ink-jet method, a method of applying a silicon resin mixed with phosphor particles, and a method of applying a liquid glass mixed with phosphor particles (FIG. 7B)." (*Id*., ¶[0068]; Ex. 1002, ¶75.)

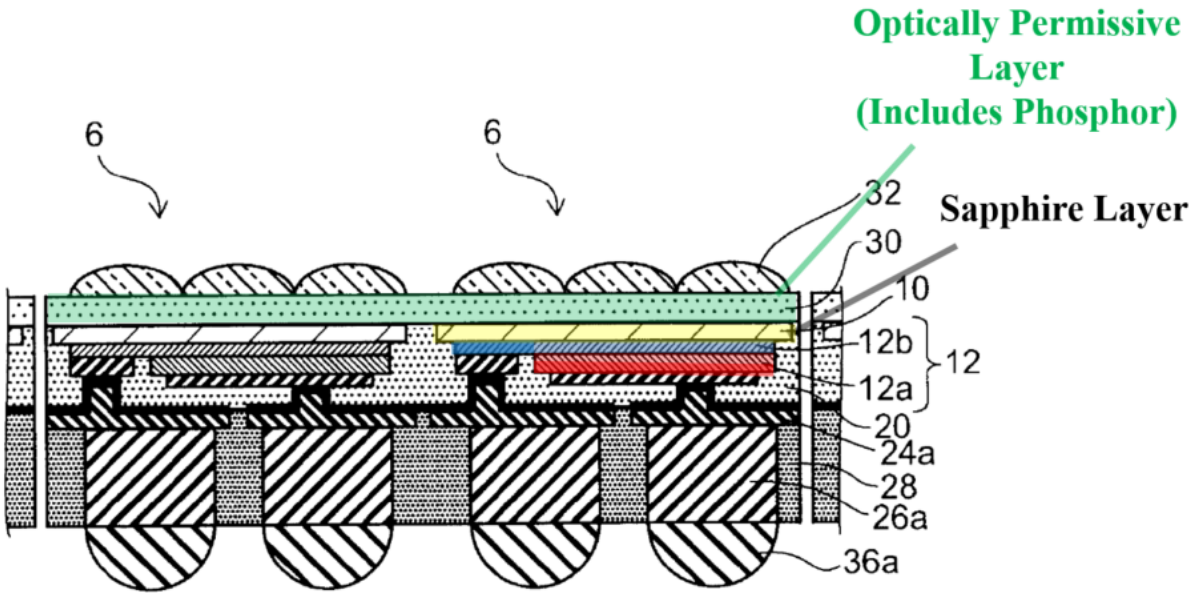


FIG. 18B

(Ex. 1005, FIG. 18B (annotated); Ex. 1002, ¶75.)

Sugizaki discloses that the phosphor layer 30, which is in direct contact with the sapphire layer, permits the light from the LED to pass through the phosphor layer and therefore is "optically permissive." (Ex. 1005, ¶[0061]; Ex. 1002, ¶76.) The phosphor layer 30 includes phosphor ("optically definable material containing quantum dots and/or phosphor") that is "adapted to change the frequency of at least some of emitted light passing therethrough" as recited in claim element 1(e). (Ex. 1005, ¶[0061]; Ex. 1002, ¶76.) A POSITA would have understood that wavelength-converted light is light that has had its frequency changed. (Ex. 1002, ¶76.) Sugizaki discloses that a mixture of light from the LED and wavelength-converted light is

emitted (Ex. 1005, ¶[0061]) such that "at least some of the emitted light" has its frequency changed. (Ex. 1002, ¶76.) Therefore, Sugizaki discloses the "optically permissive layer" recited in claim element 1(e). (*Id*.)

f) an optically permissive cover substrate covering at least a portion of the above components; and

The Sugizaki-Camras combination discloses or suggests this limitation.[4] (Ex. 1002, ¶¶77-81.) For instance, Sugizaki discloses covering the LED structure with translucent material that includes a lens ("optically permissive cover substrate") to converge or diverge the light generated by the LED. (Ex. 1005, ¶¶[0063]-[0065]; (Ex. 1002, ¶77.) As shown below, Sugizaki's Figure 18B LED device includes an array lens 32 with multiple convex lenses.

[4] For this proceeding, Petitioner assumes "the above components" refers to claim elements 1(b)-(e), but does not concede that claim 12 is not indefinite.

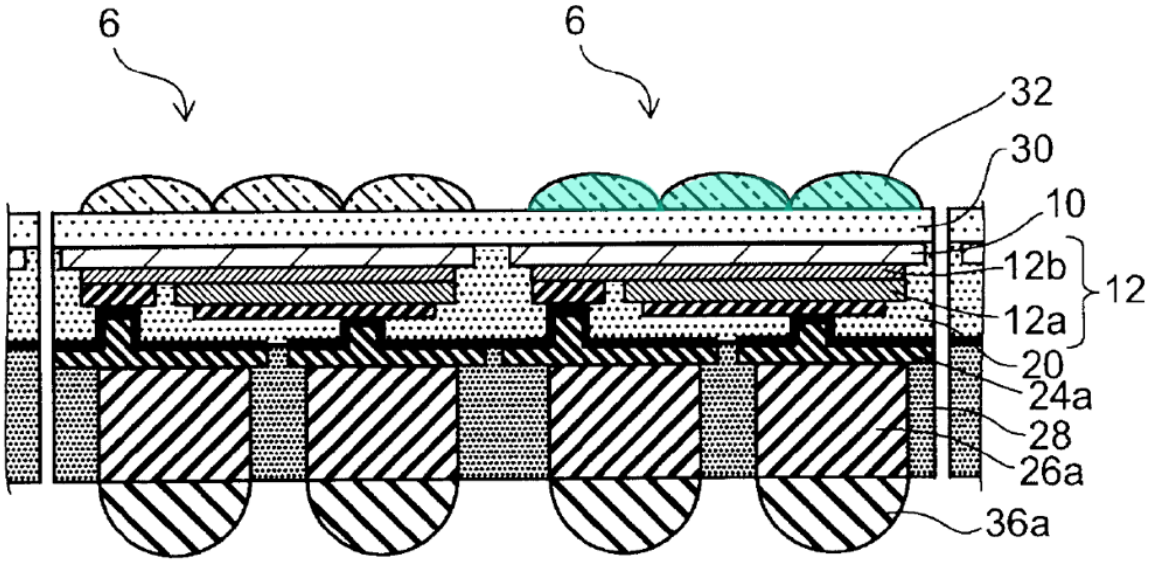
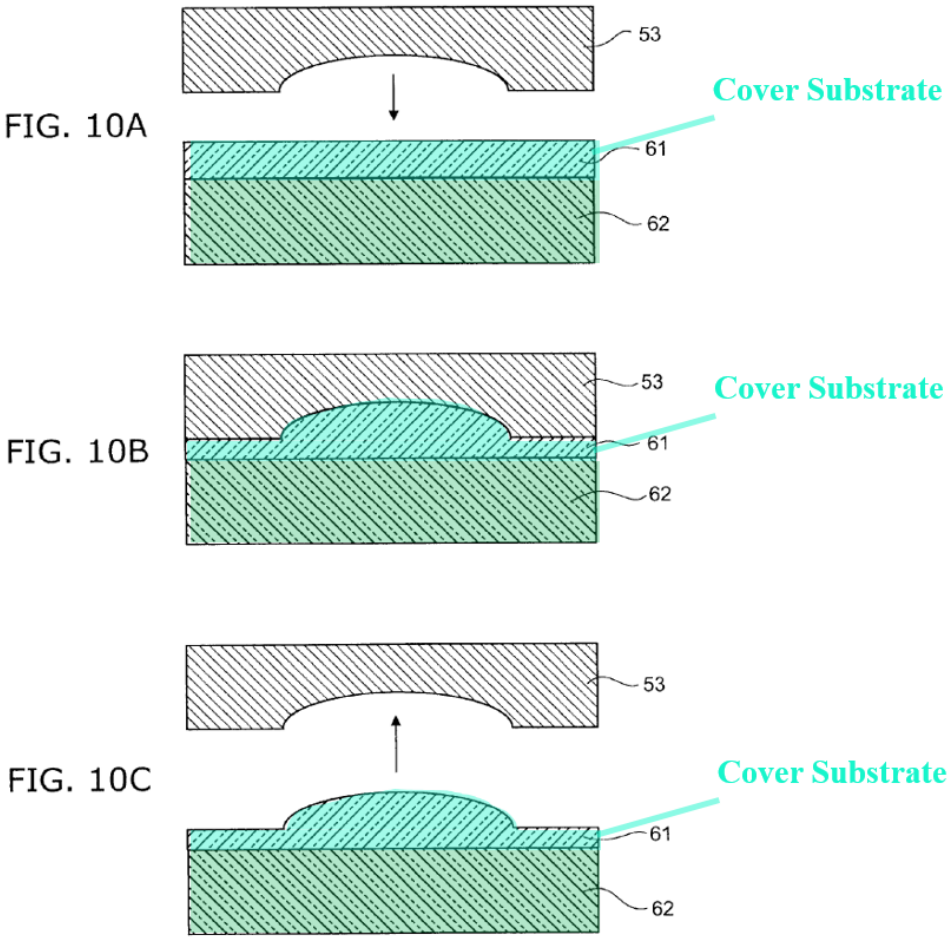


FIG. 18B

(Ex. 1005, FIG. 18B (annotated); Ex. 1002, ¶77.)

Sugizaki, however, discloses that a single lens can be used instead of an array lens like that shown in figure 18B. (Ex. 1005, ¶[0086] ("[u]se of a single lens can simplify the optical design and manufacturing process."); Ex. 1002, ¶78.) Sugizaki discloses an example technique for forming such a lens in figures 10A-10C that includes depositing a layer of spin on glass or similar material and then stamping the layer with a mold in order to produce the desired lens shape. (Ex. 1005, ¶¶[0075]-[0076], claim 7 ("applying a liquid glass on the first surface side of the multilayer body, and forming a lens by mold press."), FIGs. 10A-10C; Ex. 1002, ¶¶79-80.)



(Ex. 1005, FIGs. 10A-10C (annotated); Ex. 1002, ¶80.)

Modified figure 18B of Sugizaki below illustrates a non-limiting example of an LED device according to the Sugizaki-Camras combination with a single lens. (Ex. 1002, ¶81.) As is apparent from modified figure 18B below, the lens, which constitutes "an optically permissive cover substrate" covers "at least a portion" of the components recited in claim features 1(b)-1(e). (*Id.*)

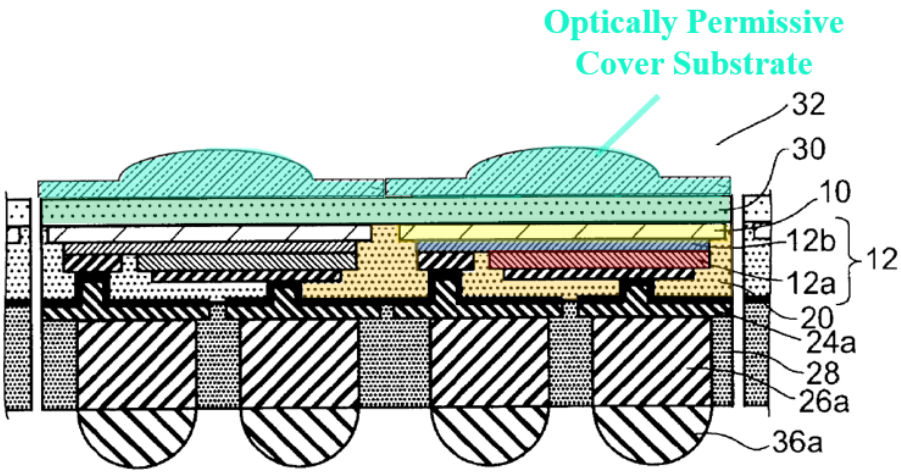


FIG. 18B

(Ex. 1005, FIG. 18B (modified, annotated); Ex. 1002, ¶81.)

g) a passivation layer in direct contact with said metallization layer, said sapphire layer, a surface of said optically permissive layer, and said semiconductor LED,

The Sugizaki-Camras combination discloses or suggests these limitations. (Ex. 1002, ¶¶82-84.) Notably, the positioning of the passivation layer with respect to the other layers as recited in claim 1 was a feature the Examiner identified as being absent in the prior art during prosecution. (Ex. 1004, 74 (Interview summary noting that the Examiner offered suggestions "regarding Applicant's Fig. 10 to include additional limitations to describe the relationship of the passivation layer with the surrounding/contacting layers (e.g. the LED, sapphire substrate, and layer 1030).").) Indeed, the Examiner noted that "[i]f amended to more clearly describe features of

the passivation layer 1070 shown in Fig. 10, this would over come the applied prior art." (*Id*.) Applicant subsequently amended the claims as suggested by the Examiner, and the claims were then allowed. (*Id*., 49-50, 57-58, 11-12.) As demonstrated below, Sugizaki discloses the recited features regarding the passivation layer positioning that the Examiner believed were absent from the prior art. (Ex. 1002, ¶82.)

For instance, Sugizaki discloses depositing a "dielectric film 20 made of an organic or inorganic material" (Ex. 1005, ¶[0033]) that constitutes a "passivation layer" as recited in claim element 1(g). (Ex. 1002, ¶83.) Dielectric films were commonly used to isolate electrically conductive elements from each other, to provide mechanical and chemical protection for certain circuit components or features of circuit components both during and after fabrication, and for masking during semiconductor device formation. (*Id*.) Such dielectric films are non-conductive, which is confirmed by Sugizaki's formation of openings in the dielectric film to allow electrical contact to the electrodes. (*See infra* Sections IX.A.1(h)-(i).)

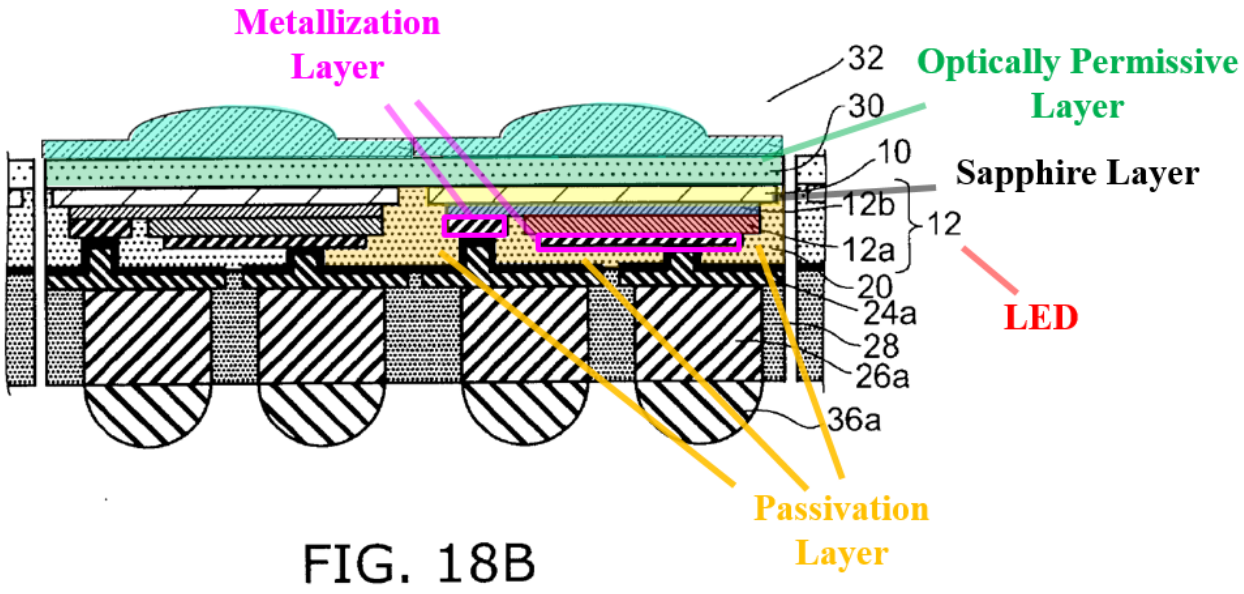


FIG. 18B

(Ex. 1005, FIG. 18B (annotated); Ex. 1002, ¶83.)

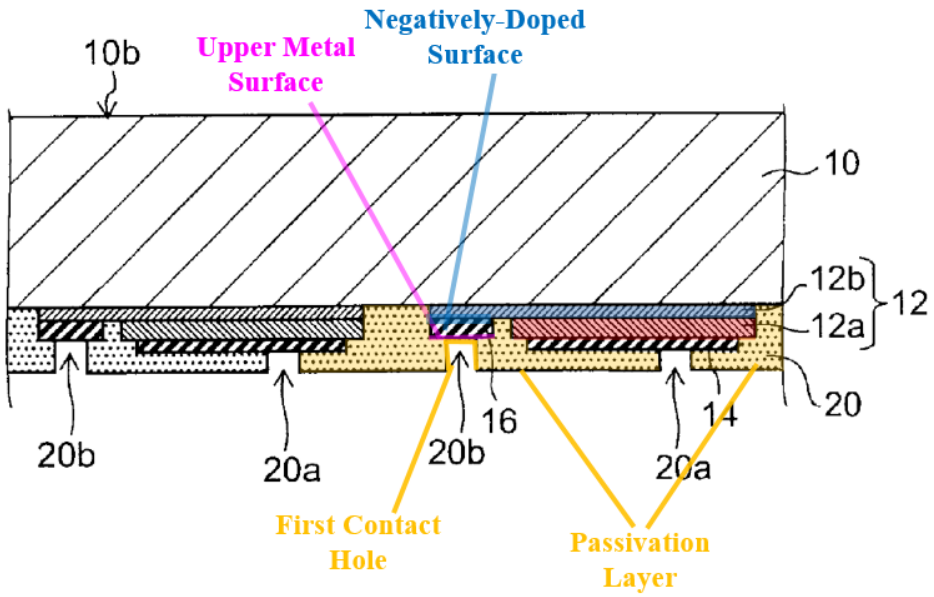
As is apparent from figure 18B above, the dielectric layer 20 ("passivation layer") in direct contact with: (1) the "metallization layer" that includes the p-side electrode and an n-side electrode, (2) the sapphire layer 10, (3) the bottom surface of the phosphor layer ("optically permissive layer"), and (4) the LED 12, thereby disclosing the passivation layer positioning recited in claim 1. (Ex. 1002, ¶84.)

h) wherein said passivation layer defines a first contact hole to expose a first portion of an upper metal surface of said metallization layer disposed on said negatively-doped surface and said passivation layer is in direct contact with a second portion of said upper metal surface of said metallization layer disposed on said negatively-doped surface,

The Sugizaki-Camras combination discloses or suggests these limitations. (Ex. 1002, ¶¶85-89.) As shown in annotated figure 3C below, Sugizaki discloses

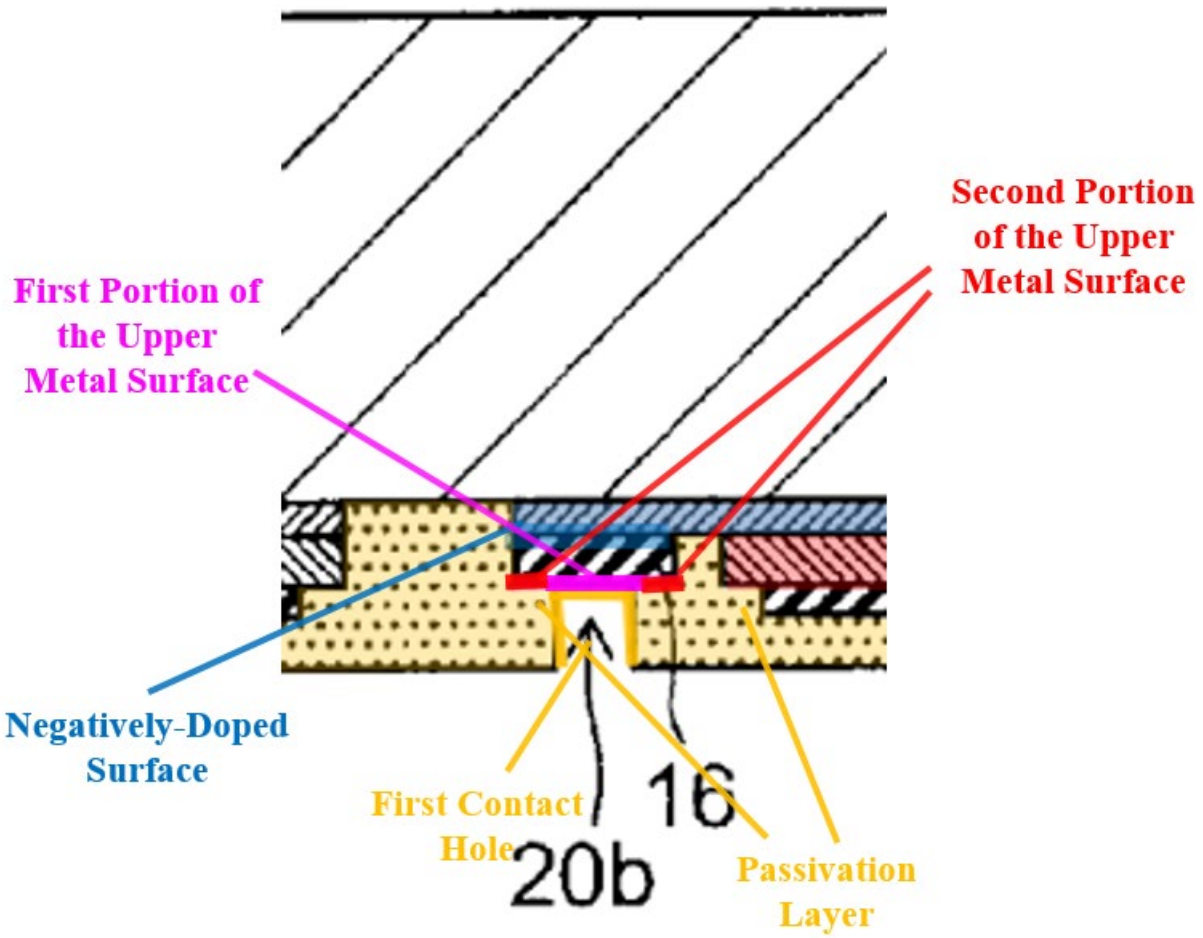
that, after deposition, a portion of the dielectric film ("passivation layer") is removed to expose the lower portion of the n-side electrode 16 ("an upper metal surface of said metallization layer"). (Ex. 1005, ¶[0048] ("A dielectric film 20 is formed so as to cover the p-side electrode 14 and the n-side electrode 16, and openings (first opening and second opening) 20a, 20b are formed so as to expose part of the p-side electrode 14 and n-side electrode 16, respectively (FIG. 3C).").) In addition to defining a first contact hole that exposes a portion of the n-side electrode 16, the remaining dielectric is also in direct contact with the portion of the upper metal surface that is not exposed by the contact hole ("said passivation layer is in direct contact with a second portion of said upper metal surface of said metallization layer disposed on said negatively-doped surface"). (Ex. 1002, ¶85.)

FIG. 3C



(Ex. 1005, FIG. 3C (annotated); Ex. 1002, ¶85.)

The enlarged portion of figure 3C below is annotated to show the "first portion" and the "second portion" of the "upper metal surface of said metallization layer."



(Ex. 1005, FIG. 3C (excerpt, annotated); Ex. 1002, ¶86.)

Similarly, as shown in annotated figure 18B and the excerpt of annotated figure 18B below, a portion of the dielectric layer 20 ("passivation layer") has been removed to define a first contact hole as recited in claim 1, where the dieelectric layer is also in direct contact with the portion of the upper metal surface that is not

exposed by the contact hole. (Ex. 1005, Abstract, ¶¶[0007]-[0009], [0048], FIG. 18B, claims 1, 9, 10; Ex. 1002, ¶87.)

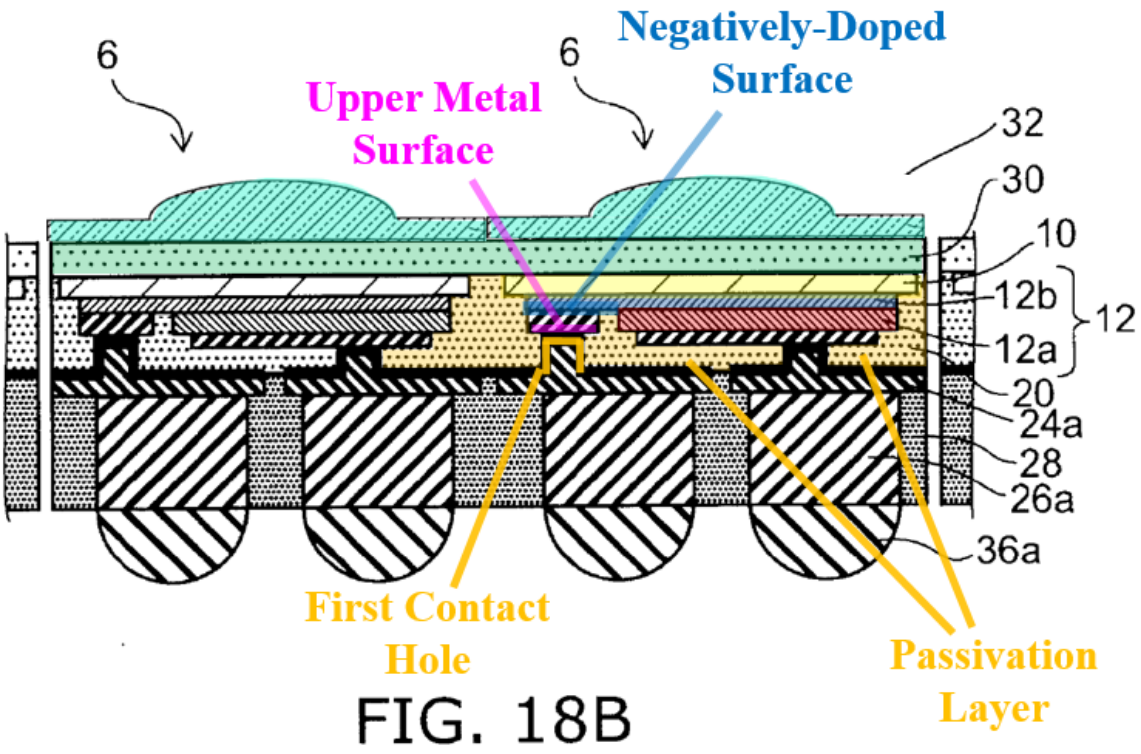
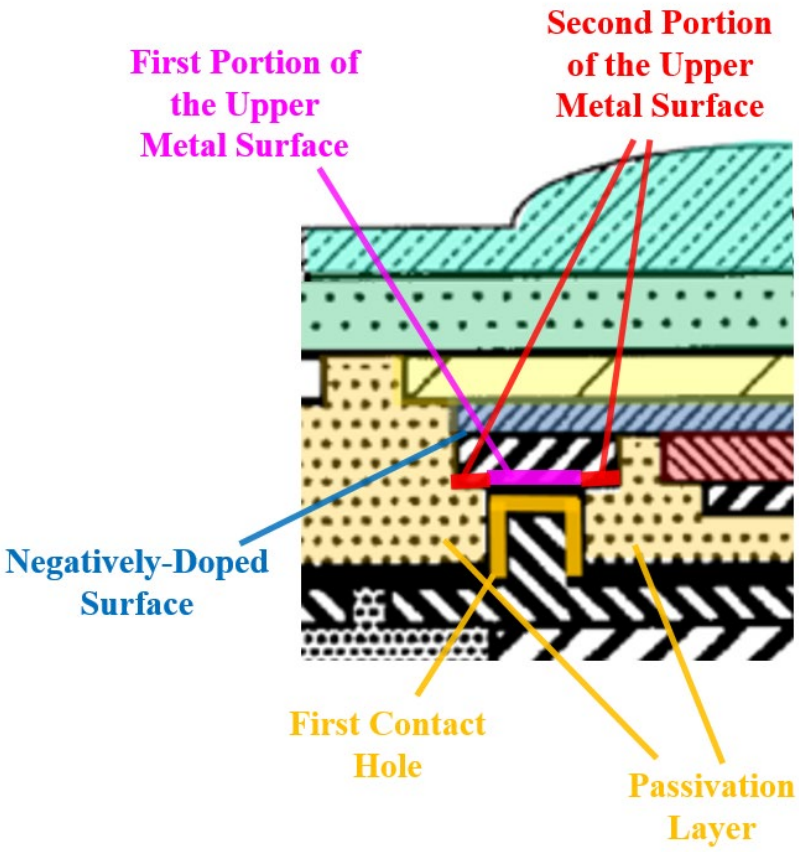


FIG. 18B

(Ex. 1005, FIG. 18B (modified, annotated); Ex. 1002, ¶87.)



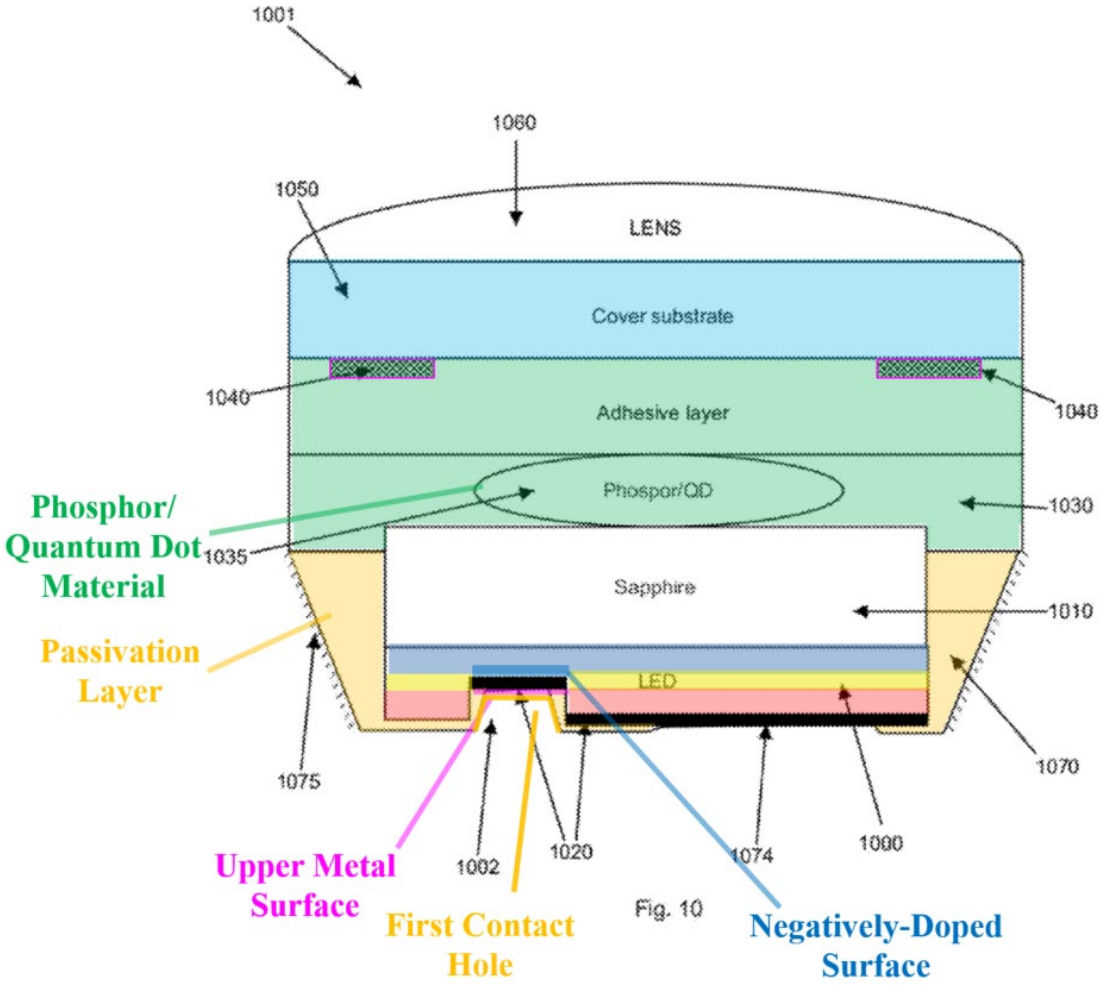
(Ex. 1005, FIG. 18B (excerpt, modified, annotated); Ex. 1002, ¶87.)

Sugizaki further discloses a layer of seed metal formed in the contact hole to foster good electrical contact to the electrode. (Ex. 1005, ¶[0048].) The inclusion of the seed metal layer, discussed in detail with respect to claim 8 below (*see infra* Section IX.A.6), is consistent with the disclosure of the '405 patent and does not interfere with Sugizaki's disclosure of claim feature 1(h). (Ex. 1002, ¶88.)

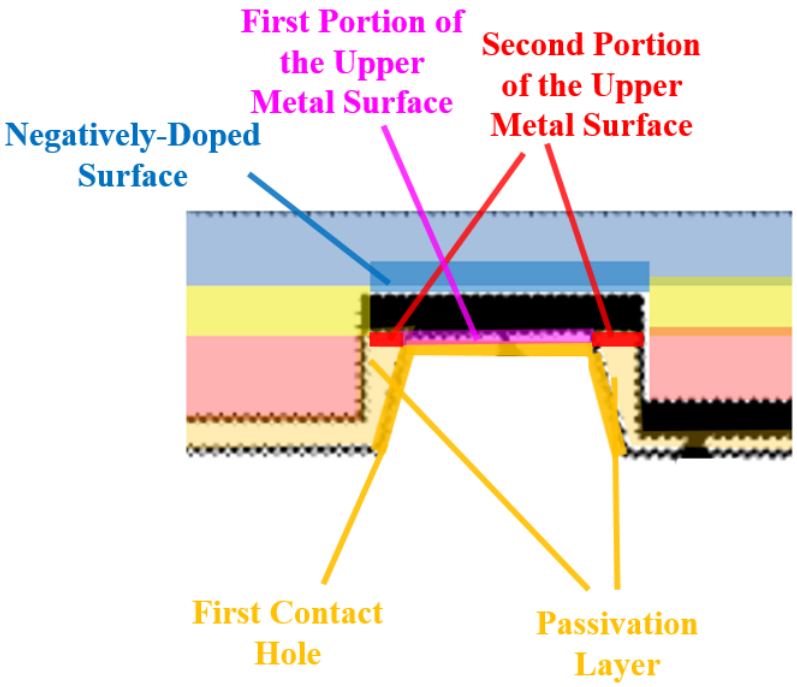
Sugizaki's disclosure of these claim features is consistent with the disclosure of the '405 patent. (Ex. 1002, ¶89.) For example, the recited features are shown in

annotated figure 10 and the enlarged excerpt of figure 10 of the '405 patent below.

(Ex. 1001, 6:45-64, FIG. 10; Ex. 1002, ¶89.)



(Ex. 1001, FIG. 10 (annotated); Ex. 1002, ¶89.)



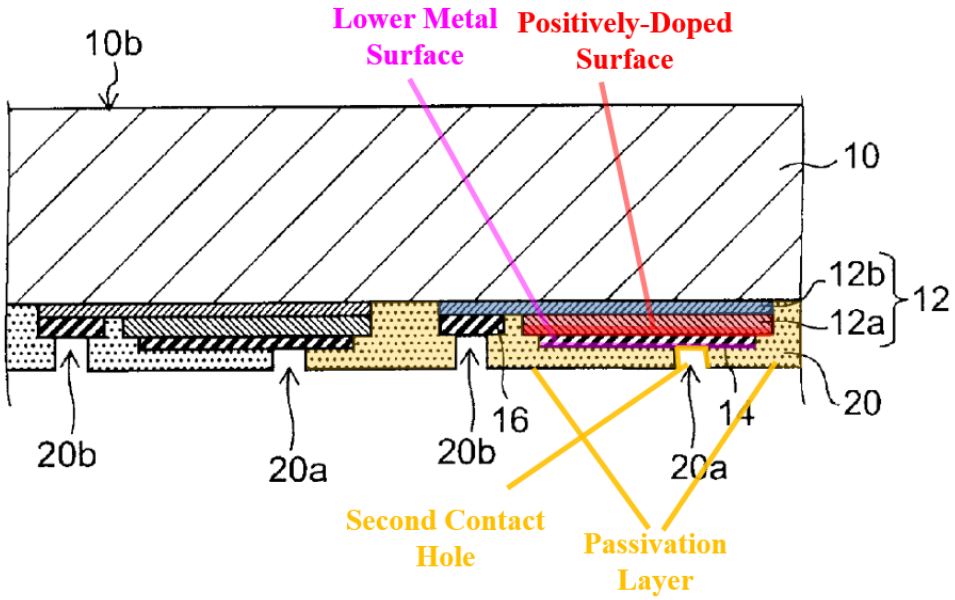
(Ex. 1001, FIG. 10 (exerpt, annotated); Ex. 1002, ¶89.)

i) wherein said passivation layer defines a second contact hole to expose a first portion of a lower metal surface of said metallization layer disposed on said positively-doped surface and said passivation layer is in direct contact with a second portion of said lower metal surface of said metallization layer disposed on said positively-doped surface, and

Sugizaki-Camras combination discloses or suggests these features. (Ex. 1002, ¶¶90-94.) As shown in annotated figure 3C below, Sugizaki discloses that a portion of the dielectric film ("passivation layer") is removed to expose the lower portion ("a second portion") of the p-side electrode 14 ("a lower metal surface of said metallization layer"). (Ex. 1005, ¶[0048].) In addition to defining a first contact hole that exposes a portion of the p-side electrode 14, the remaining dielectric is also

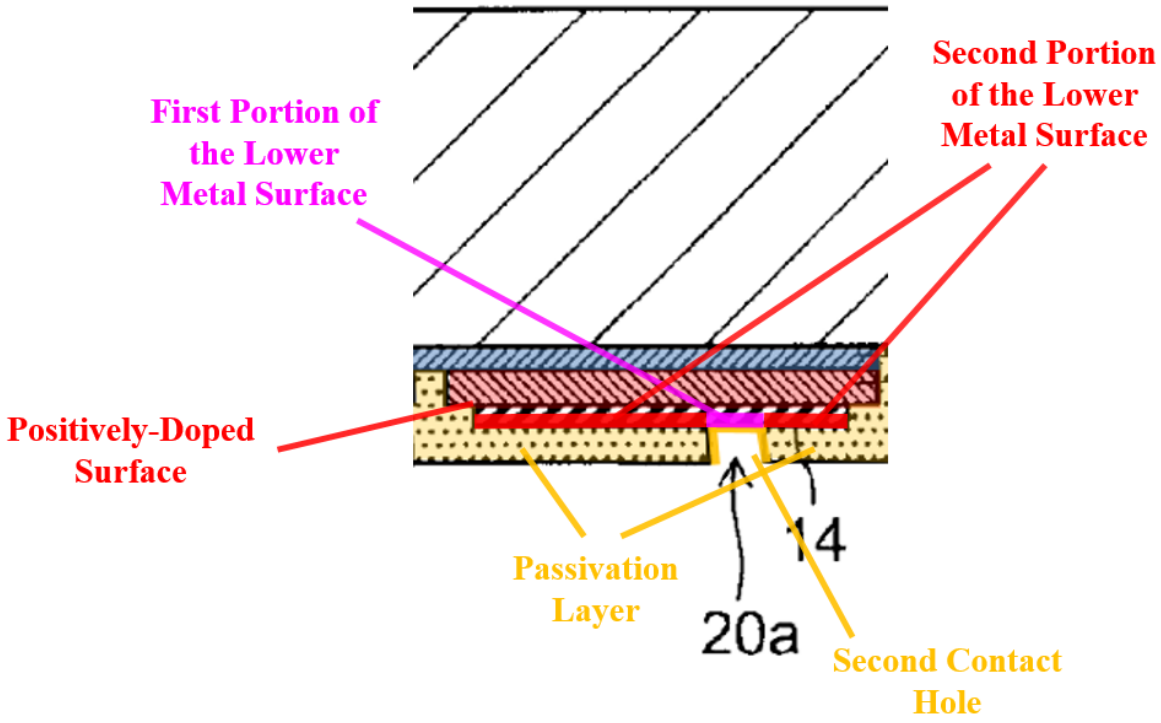
in direct contact with the portion of the upper metal surface that is not exposed by the contact hole ("said passivation layer is in direct contact with a second portion of said lower metal surface of said metallization layer disposed on said positively-doped surface"). (Ex. 1002, ¶90.)

FIG. 3C



(Ex. 1005, FIG. 3C (annotated); Ex. 1002, ¶90.)

The enlarged portion of figure 3C below is annotated to show the "first portion" and the "second portion" of the "lower metal surface of said metallization layer."



(Ex. 1005, FIG. 3C (excerpt, annotated); Ex. 1002, ¶91.)

Similarly, as shown in annotated figure 18B and the excerpt of figure 18B below, a portion of the dielectric layer 20 ("passivation layer") has been removed to define a second contact hole as recited in claim 1, where the dielectric layer is also in direct contact with the portion of the lower metal surface that is not exposed by the contact hole. (Ex. 1005, Abstract, ¶¶[0007]-[0009], [0048], FIG. 18B, claims 1, 9, 10; Ex. 1002, ¶92.)

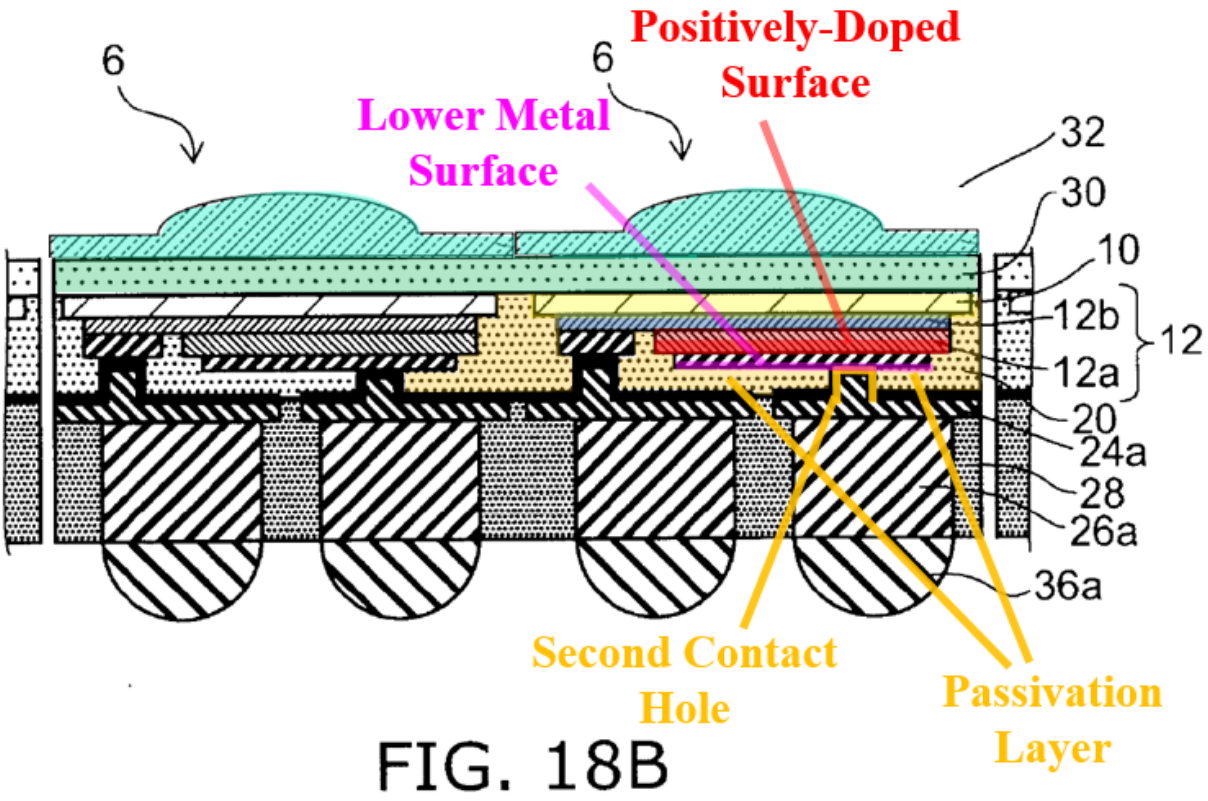
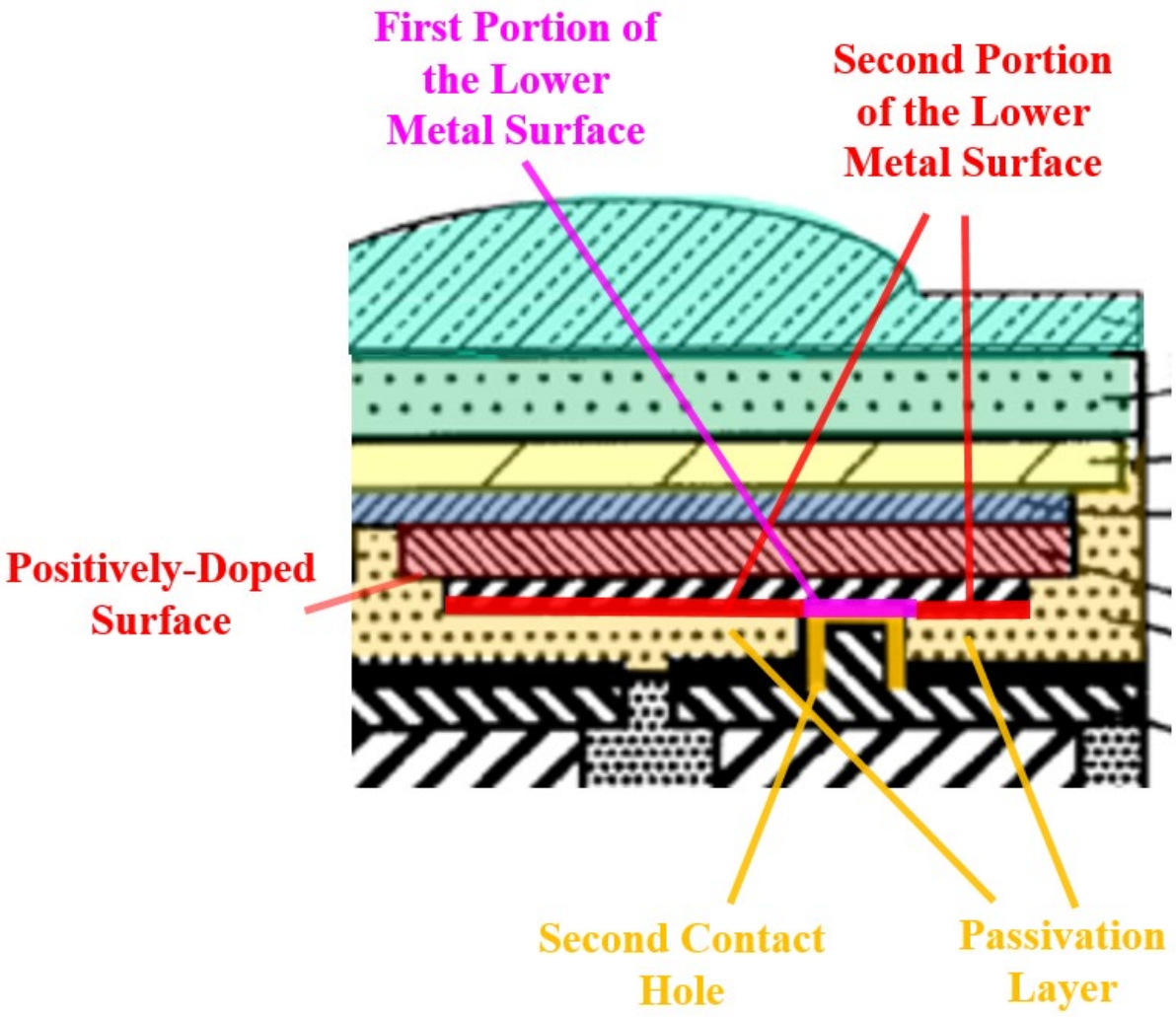


FIG. 18B

(Ex. 1005, FIG. 18B (modified, annotated); Ex. 1002, ¶92.)



(Ex. 1005, FIG. 18B (excerpt, modified, annotated); Ex. 1002, ¶92.)

As noted above for claim feature 1(h), the inclusion of the seed metal layer (*see infra* Section IX.A.6) is consistent with the disclosure of the '405 patent and does not interfere with Sugizaki's disclosure of claim feature 1(i). (*Supra* Section IX.A.1(h); Ex. 1002, ¶93.)

Sugizaki's disclosure of this feature is consistent with the disclosure of the '405 patent. (Ex. 1002, ¶94.) For example, the recited features are shown in

annotated figure 10 and the enlarged excerpt of figure 10 of the '405 patent below.

(Ex. 1001, 6:45-64, FIG. 10; Ex. 1002, ¶94.)

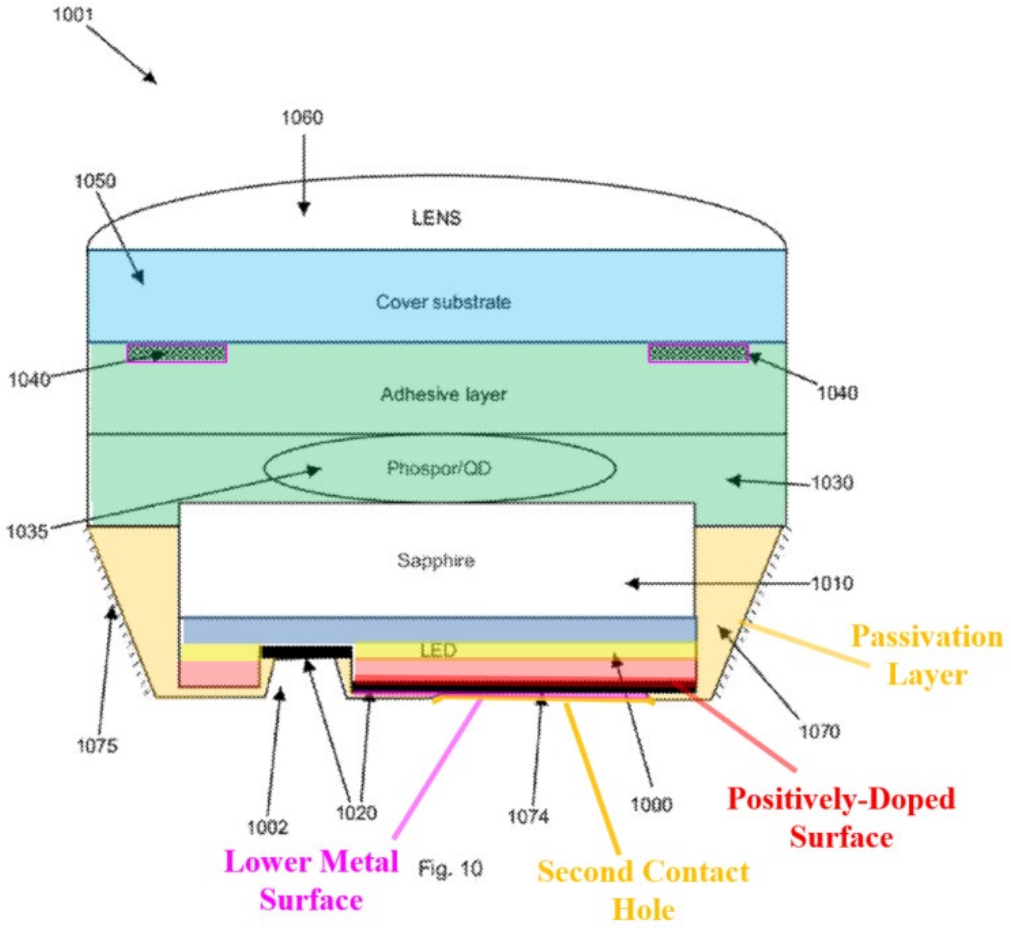
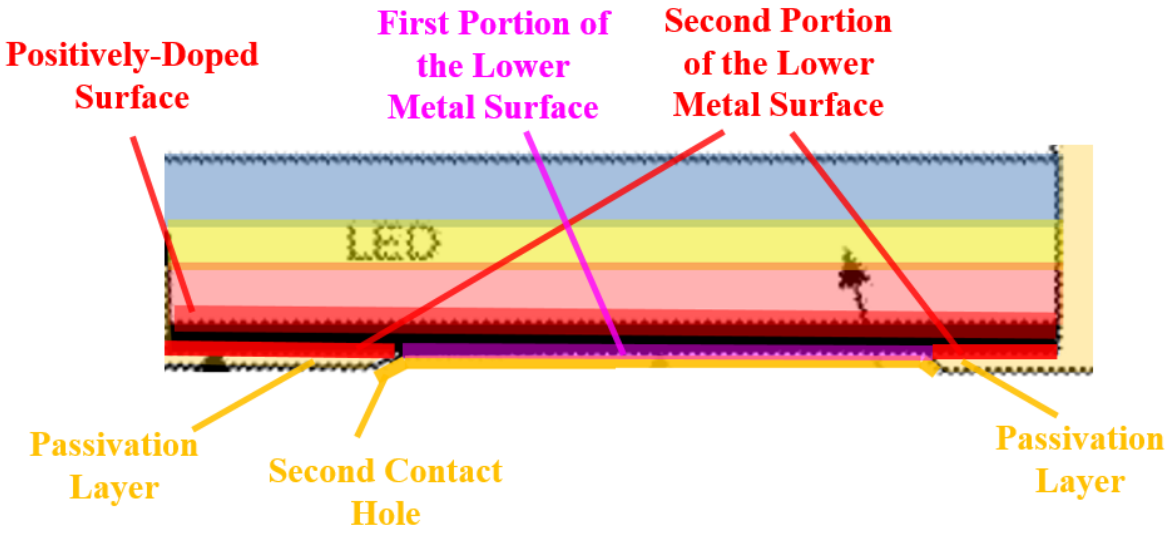


Fig. 10

(Ex. 1001, FIG. 10 (annotated); Ex. 1002, ¶94.)



(Ex. 1001, FIG. 10 (excerpt, annotated); Ex. 1002, ¶94.)

j) wherein said upper metal surface, said lower metal surface, said negatively-doped surface, said positively-doped surface, and said surface of said optically permissive layer are parallel with one another.

The Sugizaki-Camras combination discloses or suggests these features. (Ex. 1002, ¶95.) As shown in annotated figure 18B of Sugizaki below, the upper metal surface, lower metal surface, negatively-doped surface, positively-doped surface, and the surface of the optically permissive layer identified above with respect to claim features 1(g)-(i) are parallel with one another. (*Id.*) Indeed, the depiction of these layers as being parallel with each other in figure 18B is consistent with how a POSITA would understand the layers to be relatively oriented based on the way they are formed. (*Id.*)

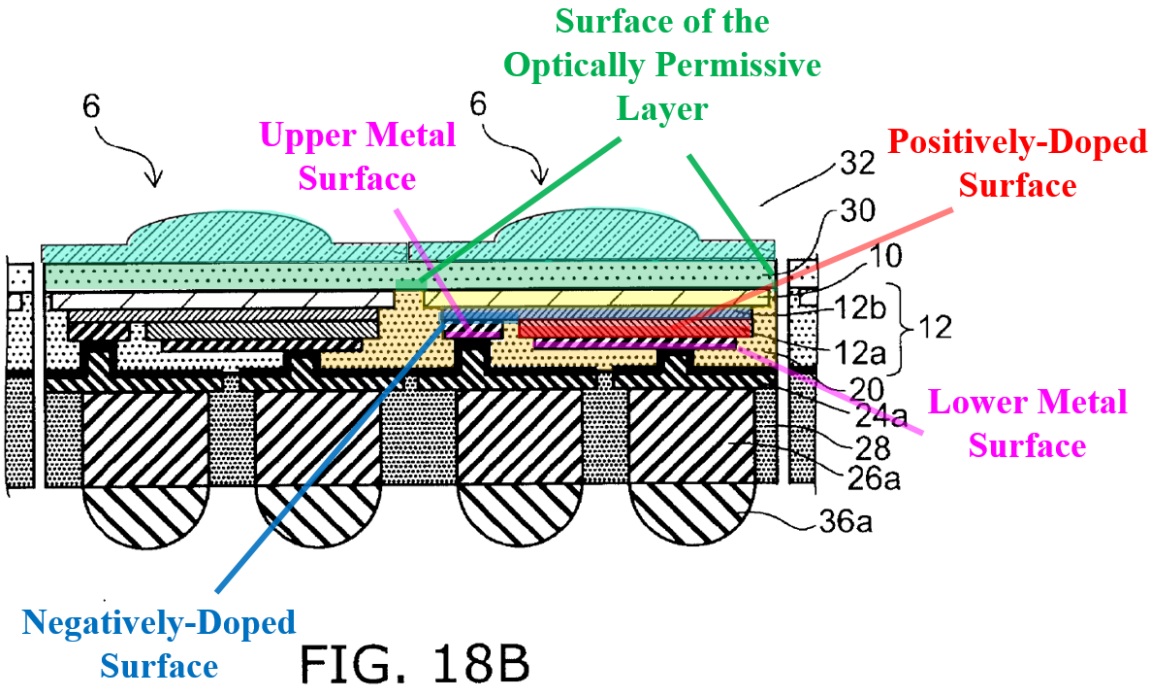


FIG. 18B

(Ex. 1005, FIG. 18B (modified, annotated); Ex. 1002, ¶95.)

2. Claim 2

a) The light emitting device of claim 1, further comprising a lens covering at least a portion of said optically permissive cover substrate.

Sugizaki in view of Camras discloses or suggests these features. (Ex. 1002, ¶¶96-101.) As discussed above with respect to claim feature 1(f), Sugizaki discloses covering the LED structure with translucent material that includes a lens that constitutes an "optically permissive cover substrate." (*See supra* Section IX.A.1(f).)

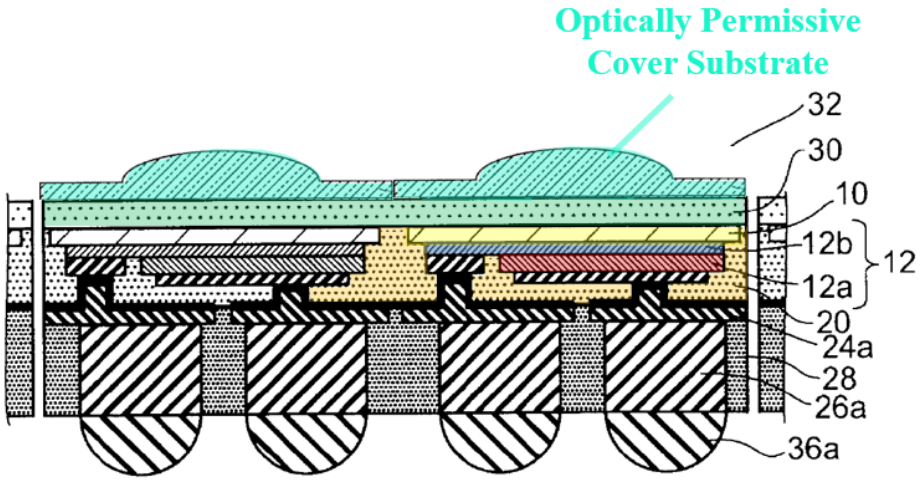


FIG. 18B

(Ex. 1005, FIG. 18B (modified, annotated); Ex. 1002, ¶96.)

Sugizaki does not disclose a lens that covers at least a portion of the cover substrate illustrated in modified figure 18B above. Camras, however, discloses an embodiment where an array of LEDs, each of which includes a lens like that shown in modified figure 18B of Sugizaki above, are mounted on a board where an additional lens is formed over the group of LEDs. (Ex. 1006, 9:11-51, FIG. 7; Ex. 1002, ¶97.)

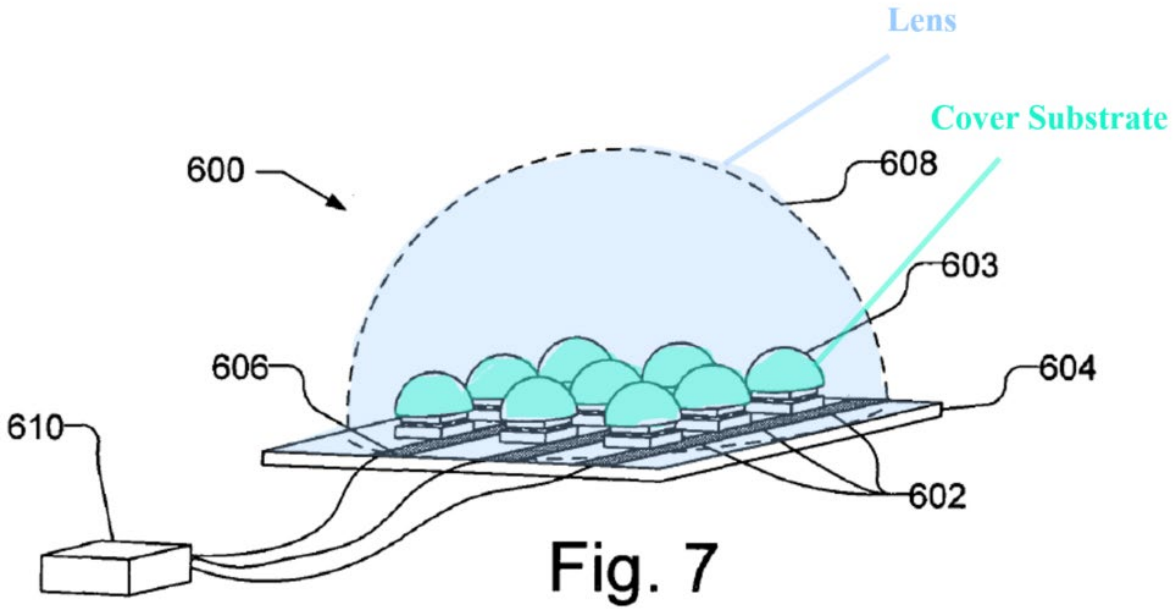


Fig. 7

(Ex. 1006, FIG. 7 (annotated); Ex. 1002, ¶97.)

As disclosed by Camras, the LEDs in the array of LEDs shown in figure 7 include phosphor, where different LEDs in the array each produce white light with different correlated color temperatures (CCTs). (Ex. 1006, 9:15-18.) Camras further discloses that "[b]y mixing the white light with different CCTs in array 600, a light with a desired CCT may be produced." (*Id.*) The mixing of the white light is accomplished by including a transparent element 608 ("lens" highlighted in annotated figure 7 above) made of, for example, glass, plastic, epoxy or silicone, where the "transparent element 608 may be filled, e.g., with epoxy or silicone, which assists the extracting and mixing of the light and to protect the LEDs 602." (*Id.*, 9:18-23; Ex. 1002, ¶98.)

As discussed above with respect to claim element 1(b), a POSITA implementing an LED device like that disclosed by Sugizaki would have had reason to look to Camras. (*See supra* Section IX.A.1(b).) Such a POSITA would have recognized that, just as is disclosed in figure 7 of Camras, the LED devices of the Sugizaki-Camras combination could be used in an array to generate white light. (Ex. 1002, ¶99.) Such a skilled person would have found it obvious to use, and been motivated to use, Sugizaki-Camras LED devices in such a device as it would have enhanced the utility of those LED devices and provided an additional application in which the Sugizaki-Camras LEDs could be used. (*Id*.) In such an embodiment, where the Sugizaki-Camras LEDs are used in an array like that disclosed in figure 7 of Camras, the inclusion of the additional lens covering the array of LEDs would promote the mixing of white light and further protection of the LEDs. (*Id*.) Such benefits, which are disclosed by Camras, would have been appreciated by a POSITA. (*Id*.)

Moreover, a POSITA would have had a reasonable expectation of success. (Ex. 1002, ¶100.) The LEDs of Camras and Sugizaki are similar in many ways, and using LEDs of the Sugizaki-Camras combination in an array like in figure 7 of Camras would have been the simple substitution of one device for another similar device in a predictable manner to produce the expected result of an LED array with better white light production and improved protection for the LEDs. (*Id*.)

The lens over the array of Sugizaki-Camras LEDs, which covers the entirety of each of those LEDs, constitutes a "lens" that covers "at least a portion of said optically permissive substrate" for each LED as recited in claim 2. (Ex. 1002, ¶101.) Therefore, an LED device according to the Sugizaki-Camras combination that includes an additional lens overlying an array of LEDs discloses or suggests the features of claim 2. (*Id*.)

3. Claim 3

a) The light emitting device of claim 1, wherein said passivation layer is substantially electrically non-conductive.

Sugizaki in view of Camras discloses or suggests these features. (Ex. 1002, ¶102.) As discussed above with respect to claim feature 1(g), Sugizaki discloses a dielectric film 20 that corresponds to the "passivation layer" and is non-conductive as demonstrated by the need to form holes to contact the electrodes. (*See supra* Section IX.A.1(g); Ex. 1002, ¶102.)

4. Claim 5

a) The light emitting device of claim 1, further comprising an optically permissive adhesive layer coupling said optically permissive layer and said sapphire layer.

Sugizaki in view of Camras discloses or suggests these features. (Ex. 1002, ¶¶103-105.) Sugizaki does not explicitly disclose an optically permissive adhesive layer coupling the phosphor layer 30 ("optically permissive layer") to the sapphire

layer 10, but Camras discloses using such an adhesive layer to bond a phosphor-containing layer to a sapphire substrate, and a POSITA would have found it obvious to include such an adhesive layer in an LED device according to the Sugizaki-Camras combination. (Ex. 1002, ¶103.)

Camras discloses that a layer of wavelength converting material 510 (e.g., a phosphor coating) ("optically permissive layer") is bonded to the sapphire layer using a bonding layer. (Ex. 1006, 7:64-65, 8:27-61; Ex. 1002, ¶104.) The bonding layer 508 ("adhesive layer") between the sapphire layer of the LED and the phosphor-containing wavelength converting layer 510 is shown in annotated figure 5 of Camras below.

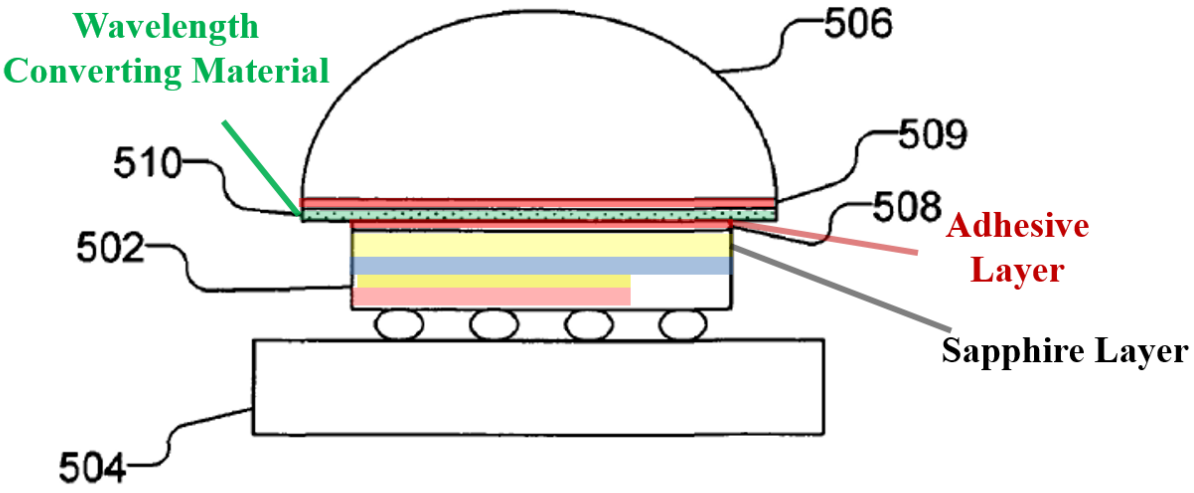


Fig. 5

(Ex. 1006, FIG. 5 (annotated); Ex. 1002, ¶105.)

A POSITA would have found it obvious to include such an adhesive layer in the Sugizaki-Camras combination in order to enable independently formed materials to be used as the phosphor layer 30 shown in figure 18B of Sugizaki, where the phosphor layer is used to convert the wavelength of the light generated by the LED. (Ex. 1005, ¶[0061]; Ex. 1002, ¶106.) For example, Camras discloses wavelength converting material such as "phosphor impregnated glass or wavelength converted ceramic that is **formed independently** and then bonded to the LED die 502 and optical element 506." (Ex. 1006, 8:42-45 (emphasis added).)

Using independently-formed wavelength converting materials, such as ceramics or glass that include phosphor, would have been desirable in some applications and would provide additional flexibility in terms of formation of the LED device of the Sugizaki-Camras combination. (Ex. 1002, ¶107.) Such a skilled person would have understood that an adhesive material, like the bonding layer 508 disclosed by Camras, would be used to bond such independently-formed wavelength converting materials to, for example, the sapphire layer in the Sugizaki-Camras combination, where such bonding and layer ordering is consistent with the disclosure of both Sugizaki and Camras. (*Id*.) Indeed, using such a bonding layer to adhere an independently-fabricated layer including phosphor to the sapphire substrate would have been nothing more than the application of a known technique to a known device to achieve a predictable result. *KSR*, 550 U.S. at 416-18.

The adhesive layer used to bond the optically permissive layer to the sapphire layer would be "optically permissive" to allow the light generated by the LED to be emitted from the LED device. (Ex. 1002, ¶108.) Moreover, Camras discloses bonding layers that are "optically permissive adhesive layers" as that term is used in the '405 patent, as Camras discloses bonding layers of epoxies and silicones. (Ex. 1006, 4:27-53; Ex. 1010, ¶[0044]; Ex. 1001, 5:8-10 ("The transparent adhesive layer 530 may be composed of silicone or some other suitable adhesive…."); Ex. 1002, ¶108.) Therefore, the Sugizaki-Camras combination discloses or suggests the features of claim 5. (Ex. 1002, ¶108.)

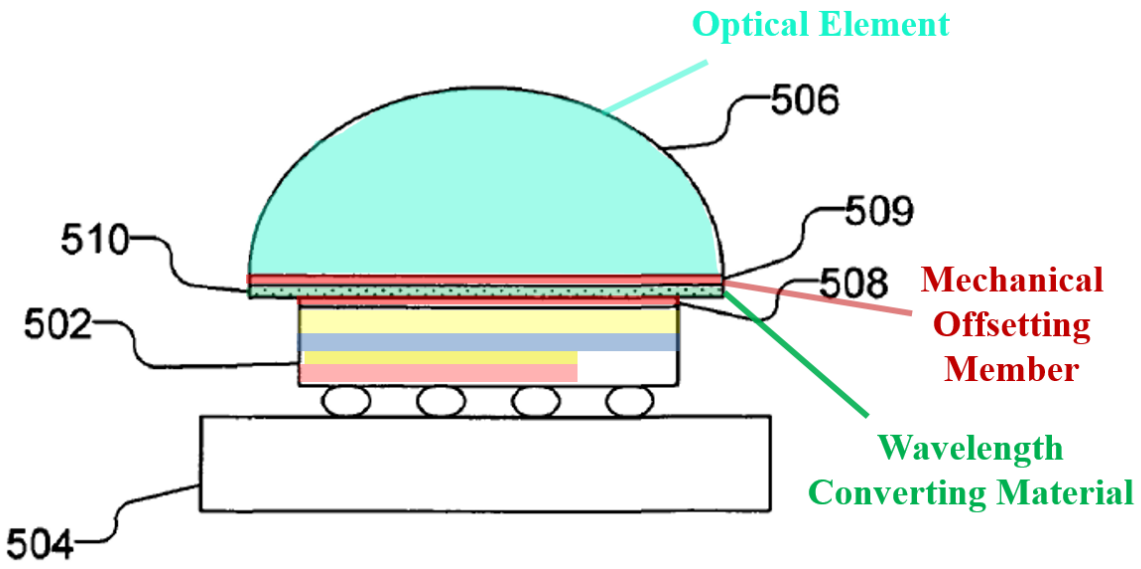
5. Claim 6

a) The light emitting device of claim 1, further comprising a mechanical offsetting member providing a dimensional spacing between said optically permissive layer and said optically permissive cover substrate.

The Sugizaki-Camras combination discloses or suggests these limitations. (Ex. 1002, ¶¶109-114.) Sugizaki does not explicitly disclose a mechanical offsetting member between the phosphor layer and the optically permissive substrate, but Camras discloses an adhesive layer, which constitutes a "mechanical offsetting member," between similar layers, and a POSITA would have found it obvious to include such a layer in the LED device of the Sugizaki-Camras combination. (Ex. 1002, ¶109.)

As discussed above with respect to claim 5, Camras discloses embodiments where a wavelength converting material 510 is independently formed and then bonded to the sapphire layer using a bonding layer 508. (*See supra* Section IX.A.4; Ex. 1006, 8:27-61.) Camras further discloses another bonding layer 509 that is used to bond the wavelength converting material 510 to the optical element 506. (Ex. 1006, 8:38-42, 8:48-54; Ex. 1002, ¶110.)

The bonding layer 509 ("mechanical offsetting member") between the wavelength converting layer 510 and the optical element 506 is shown in annotated figure 5 of Camras below. The bonding layer 509 constitutes a "mechanical offsetting member" as recited in claim 6 as it lies between the cover substrate and the optically permissive layer, thereby providing a mechanical offset therebetween. (Ex. 1002, ¶111.)



(Ex. 1006, FIG. 5 (annotated); Ex. 1002, ¶111.)

A POSITA would have found it obvious to include such a mechanical offsetting member in an LED device according to the Sugizaki-Camras combination in order to enable independently formed materials to be used as the phosphor layer 30 shown in figure 18B of Sugizuaki, where the phosphor layer is used to convert the wavelength of the light generated by the LED. (Ex. 1005, ¶[0061]; Ex. 1002, ¶112.)

For example, Camras discloses wavelength converting material such as "phosphor impregnated glass or wavelength converted ceramic that is **formed independently** and then bonded to the LED die 502 and optical element 506." (Ex. 1006, 8:42-45.) Using independently formed wavelength converting materials, such as ceramics or glass that include phosphor, would have been desirable in some applications. (Ex. 1002, ¶113.) Such a skilled person would have understood that a bonding material that provides a mechanical offset would be used to bond such independently-formed wavelength converting materials (the "optically permissive layer" in claim element 1(e)) to, for example, the cover substrate ("optically permissive cover substrate" in claim element 1(f)) in the Sugizaki-Camras combination, where such placement is consistent with the disclosure of both Sugizaki and Camras. (*Id*.) Indeed, using such a bonding layer to adhere an independently-fabricated layer including phosphor to the cover substrate would have

been nothing more than the application of a known technique to a known device to achieve a predictable result. *KSR*, 550 U.S. at 416-18.

The mechanical offsetting layer used to bond the optically permissive layer to the sapphire layer would also provide a dimensional spacing between said optically permissive layer and said optically permissive cover substrate. (Ex. 1002, ¶114.) Camras discloses example bonding materials formed from glass or semiconductors that would provide separation ("dimensional spacing") between the layers as well as additional mechanical support. (Ex. 1006, 4:27-53.) Therefore, the Sugizaki-Camras combination discloses or suggests the features of claim 6. (Ex. 1002, ¶114.)

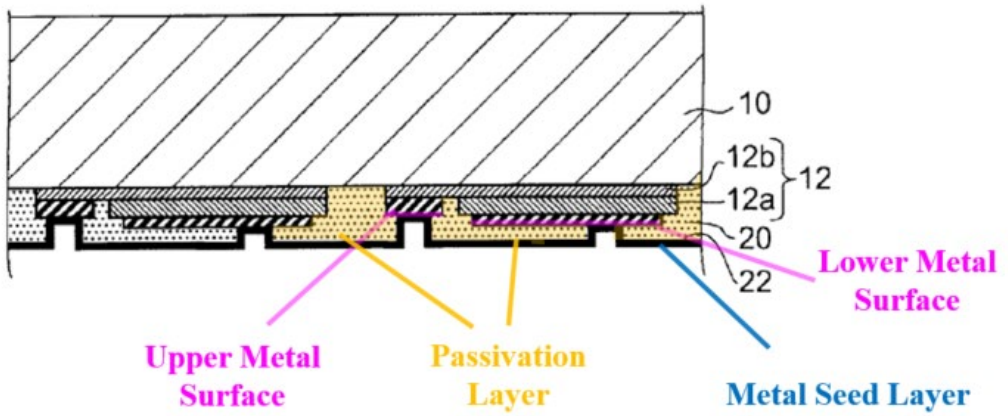
6. Claim 8

a) The light emitting device of claim 1 further comprising a metal seed layer in direct contact with said passivation layer, said upper metal surface of said metallization layer, and said lower metal surface of said metallization layer.

The Sugizaki-Camras combination discloses or suggests these features. (Ex. 1002, ¶¶115-116.) For example, Sugizaki discloses depositing a seed metal on the dielectric film ("passivation layer") as well as on the exposed surfaces of the n-side electrode ("upper metal surface of said metallization layer") and p-side electrode ("lower metal surface of said metallization layer"). (Ex. 1005, Abstract, ¶¶[0007]-[0008], [0033], [0048] ("a seed metal 22 illustratively made of Ti/Cu is formed by sputtering, for example (FIG. 3D)"), FIGs. 2A, 3D, 6A, 18B, claims 1, 9; Ex. 1002,

¶115.) Formation of the of seed metal layer 22 ("metal seed layer") is shown with respect to figure 3D, where, as shown in figures 3D and 18B below, the seed metal 22 is in direct contact with the dielectric film ("passivation layer") and the n- and p-side electrodes 16 and 14, respectively, ("metallization layer"). (Ex. 1005, ¶[0007], FIGs. 3D, 18B; Ex. 1002, ¶¶115-116.) Therefore, Sugizaki in combination with Camras discloses or suggests the features of claim 8. (Ex. 1002, ¶116.)

FIG. 3D



(*Id*., FIG. 3D (annotated); Ex. 1002, ¶115.)

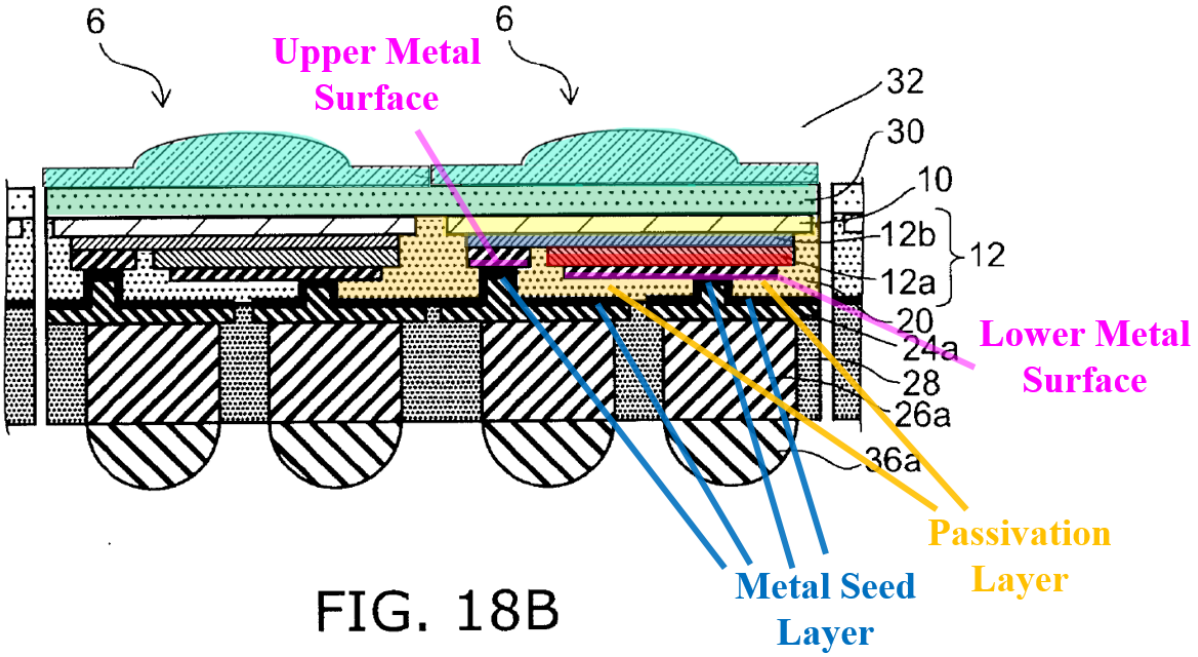


FIG. 18B

(Ex. 1005, FIG. 18B (modified, annotated); Ex. 1002, ¶116.)

7. Claim 9

a) The light emitting device of claim 8 wherein said metal seed layer is patterned.

The Sugizaki-Camras combination discloses or suggests these features. (Ex. 1002, ¶¶117-118.) For example, Sugizaki discloses that, after forming the seed metal, etching is performed to separate the seed metal into a p-side seed metal portion 22a and an n-side seed metal portion 22b, where each portion of the seed metal provides an electrical connection to the respective n- or p- contact. (Ex. 1005, Abstract, ¶[0054]; Ex. 1002, ¶117.) Annotated figures 5B and 5C below show the patterning of the seed metal layer 22.

FIG. 5B

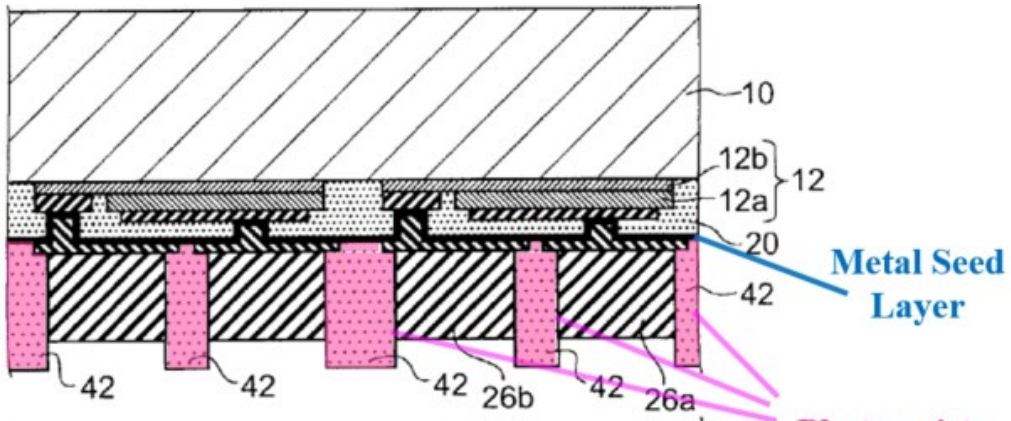
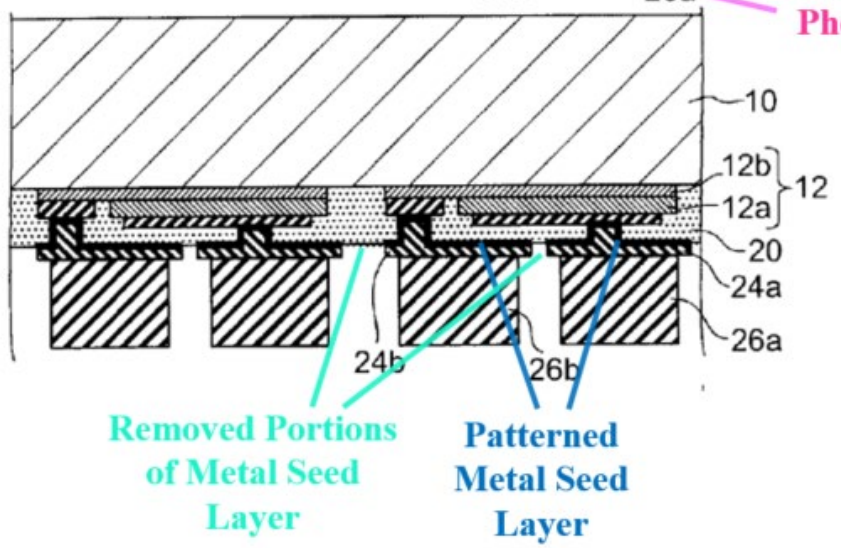


FIG. 5C



(Ex. 1005, FIGs. 5B, 5C (annotated); Ex. 1002, ¶117.)

The patterned seed metal layer shown in figure 5C is also shown in annotated figure 18B below, where the removed seed metal material results in separated p- and n-electrodes for the LED device on the right. (Ex. 1005, FIG. 18B; Ex. 1002, ¶118.) Therefore, the Sugizaki-Cammras combination discloses or suggests the features of claim 9. (Ex. 1002, ¶118.)

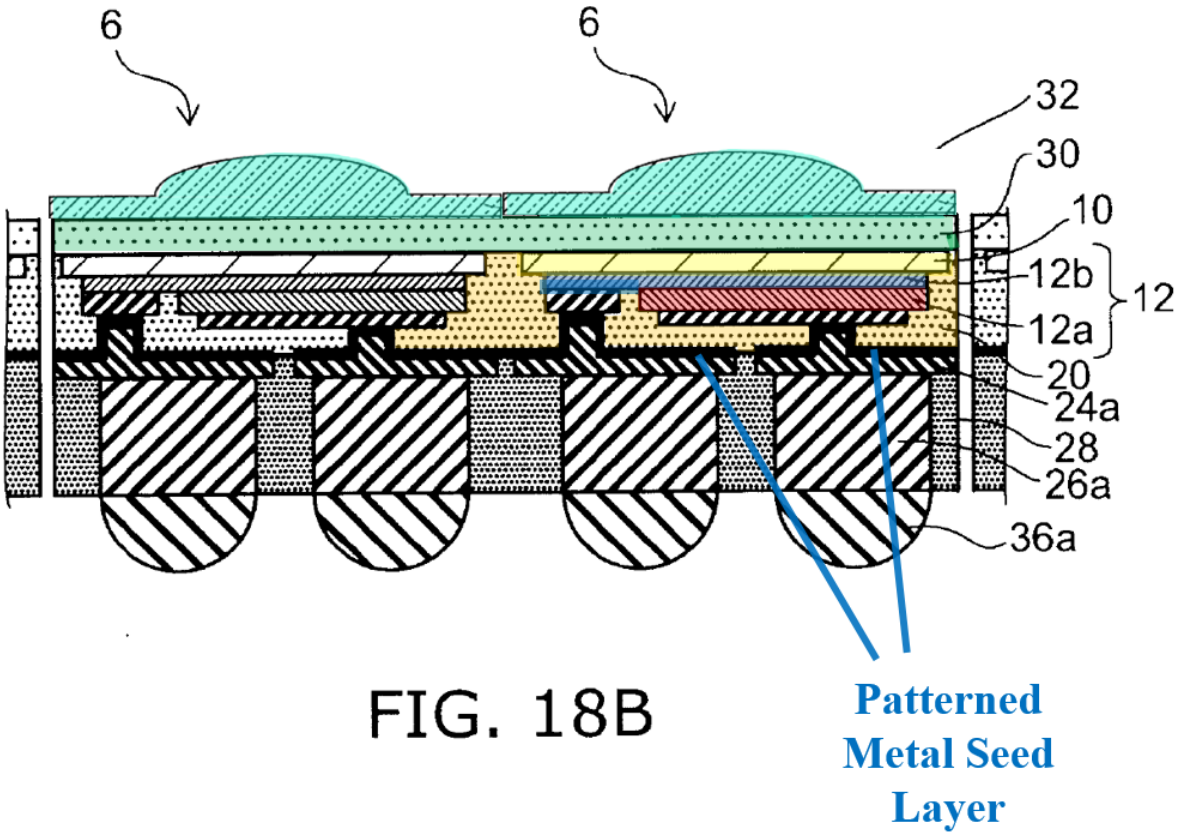


FIG. 18B

(Ex. 1005, FIG. 18B (modified, annotated); Ex. 1002, ¶118.)

8. Claim 10

a) The light emitting device of claim 8 further comprising a metal layer on said seed metal layer, said metal layer having a thickness of between about 10 microns and about 40 microns.

The Sugizaki-Camras combination discloses or suggests these features. (Ex. 1002, ¶¶119-120.) For example, Sugizaki discloses that, after forming and patterning the seed metal as discussed above with respect to claims 8 and 9, copper interconnect layers 24a and 24b and copper pillars 26a and 26b are formed. (Ex. 1005, ¶¶[0051], [0053]; Ex. 1002, ¶119.)

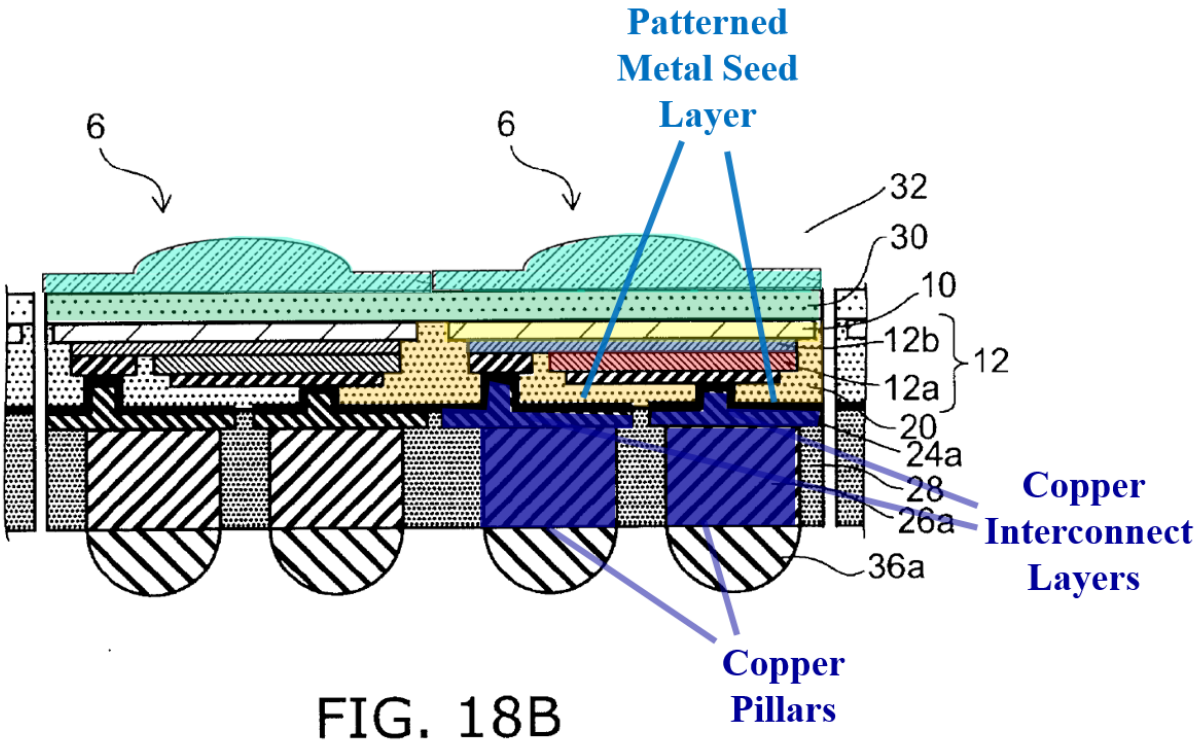


FIG. 18B

(Ex. 1005, FIG. 18B (modified, annotated); Ex. 1002, ¶119.)

Sugizaki further discloses embodiments where the thickness of the deposited copper pillars 26 is in a range of "10 to several hundred μm." (Ex. 1005, ¶[0053].) As such, the copper pillars disclosed by Sugizaki constitute a "metal layer on said seed metal layer, said metal layer having a thickness of between about 10 microns and about 40 microns" as recited in claim 10. (Ex. 1002, ¶120.)

9. Claim 11

a) The light emitting device of claim 8 wherein the metal seed layer is comprised of a light reflecting material.

The Sugizaki-Camras combination discloses or suggests these features. (Ex. 1002, ¶121.) For example, Sugizaki discloses that, the seed metal layer 22 ("metal

seed layer") can be formed of titanium and copper (Ti/Cu), which are "light reflecting material(s)." (Ex. 1005, ¶[0048]; Ex. 1002, ¶121.)

10. Claim 12

a) A method for making a light emitting device, the method comprising:

To the extent the preamble of claim 12 is limiting, Sugizaki discloses the limitations therein. (Ex. 1002, ¶¶122-123.) For instance, Sugizaki is entitled "Light Emitting Device and Method for Manufacturing Same" and discloses a "method for manufacturing a light emitting device" like that shown in figure 18B. (*Id*.; Ex. 1005, Title, ¶¶[0007], [0031], [0027], [0092], FIG. 18B; *see supra* Section IX.A.1(a).)

b) forming a light emitting device (LED) comprised of a positively-doped layer, an intrinsic layer, and a negatively-doped layer, wherein said intrinsic layer is between said positively-doped layer and a first surface of said LED is in direct contact with a sapphire layer;

The Sugizaki-Camras combination discloses or suggests these limitations. (Ex. 1002, ¶¶124-127.)[5] As discussed above with respect to claim feature 1(b), the Sugizaki-Camras combination discloses or suggests forming an LED with a

[5] For this proceeding, Petitioner assumes that limitation 12(b) should be read as "said intrinsic layer is between said positively-doped layer and a first surface of said LED *that* is in direct contact with a sapphire layer." Petitioner, however, does not concede that claim 12 is not indefinite.

multilayer body where an intrinsic layer is sandwiched between a positively-doped layer and a negatively doped layer. (*See supra* Section IX.A.1(b).)

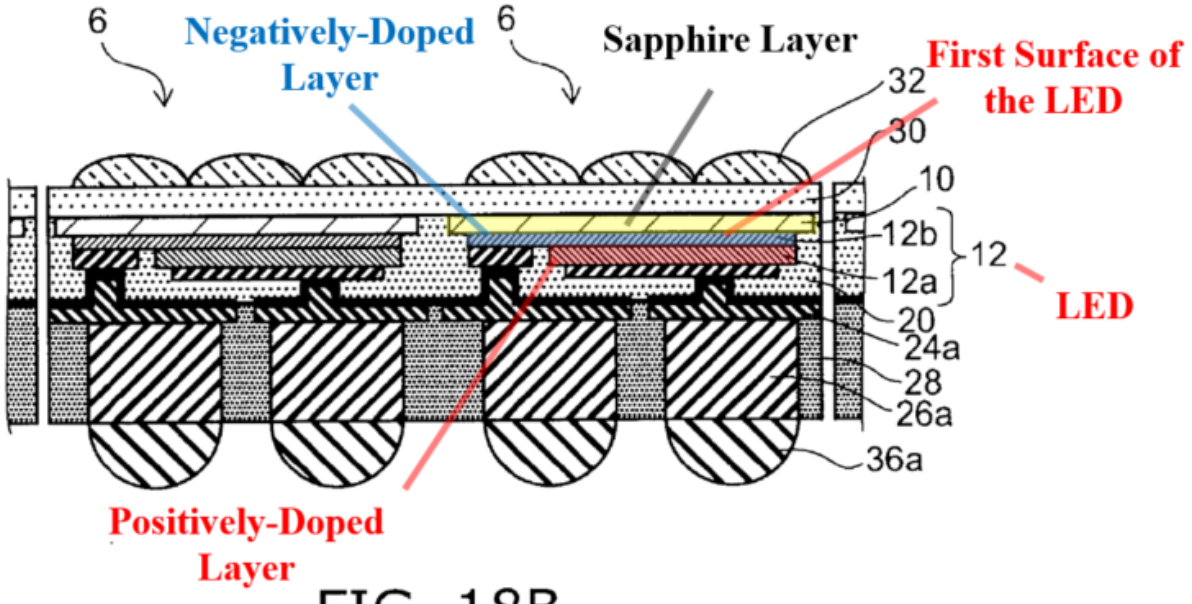


FIG. 18B

(Ex. 1005, FIG. 18B (annotated); Ex. 1002, ¶127.)

As shown in figure 18B above, the sapphire layer 10 is in "direct contact" with a first surface of the LED, and the positively-doped layer is on the opposite side of the LED from the sapphire layer as recited in claim element 12(b). (Ex. 1005, ¶[0047], FIGs. 3A, 18B; Ex. 1002, ¶¶126-127.) Therefore, the intrinsic layer, which is between the doped layers, is formed "between said positively-doped layer and a first surface of said LED [that] is in direct contact with a sapphire layer." (Ex. 1002, ¶¶126-127.)

c) forming a recess in said positively-doped layer and said intrinsic layer of said LED so as to expose a negatively-doped surface of said negatively-doped layer;

The Sugizaki-Camras combination discloses or suggests these limitations for the same reasons discussed above with respect to the recess recited in claim feature 1(b). (*See supra* Section IX.A.1(b); Ex. 1005, ¶[0047]; Ex. 1002, ¶¶128-129.)

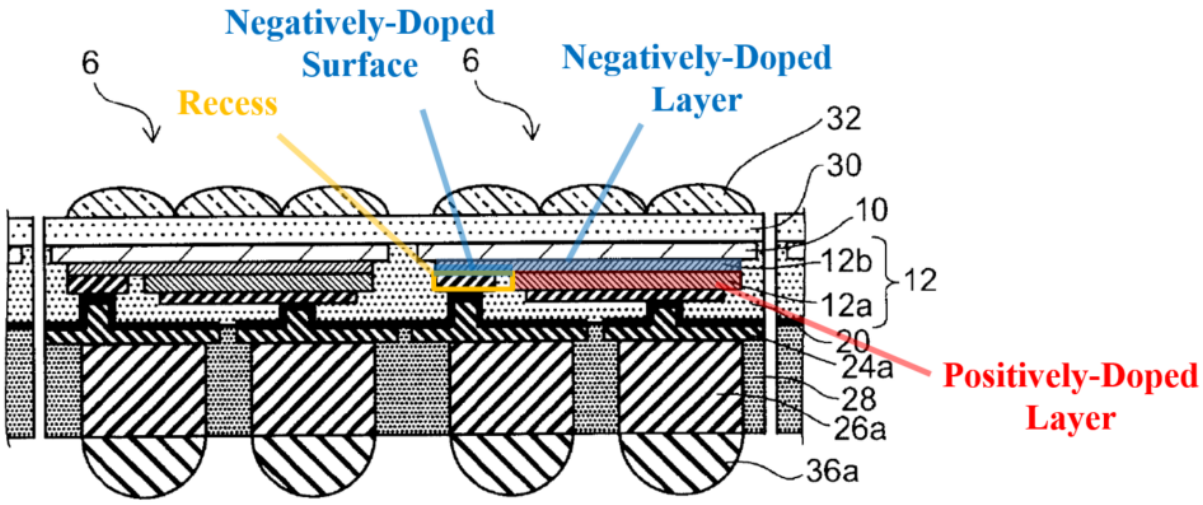
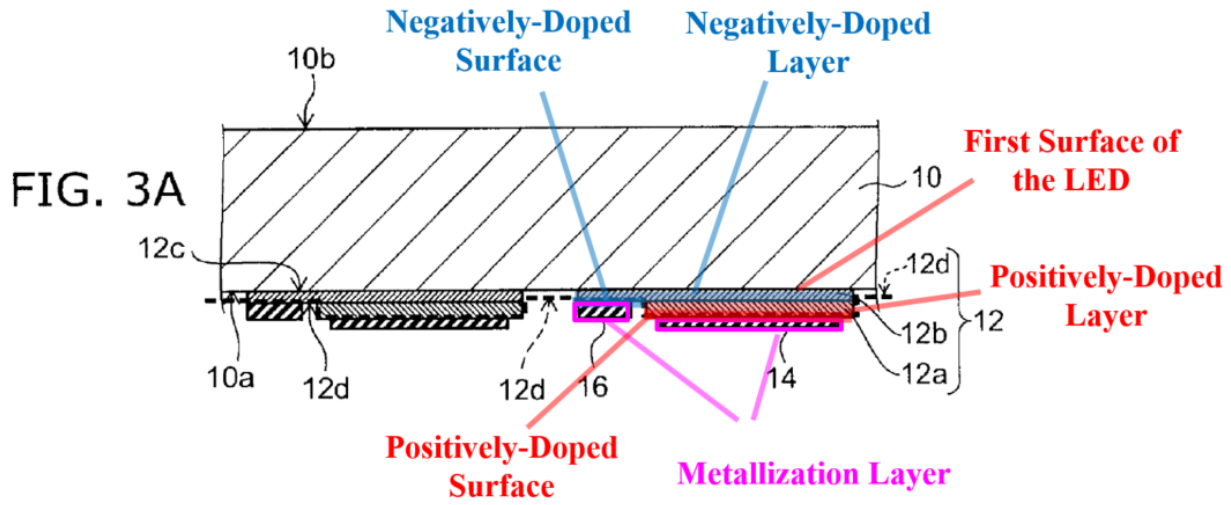


FIG. 18B

(Ex. 1005, FIG. 18B (annotated); Ex. 1002, ¶129.)

d) depositing a metallization layer on a positively-doped surface of said positively-doped layer and said negatively-doped surface of said negatively-doped layer to provide electrical contact with said positively-doped layer and said negatively-doped layer of said LED, said positively-doped layer surface and said first surface on opposing faces of said LED;

The Sugizaki-Camras combination discloses or suggests these limitations. (Ex. 1002, ¶¶130-134.) For instance, as shown in annotated figure 3A below and discussed above with respect to claim element 1(c), Sugizaki discloses forming a "metallization layer" on a positively-doped surface of the positively-doped layer and the negatively-doped surface of the negatively-doped layer. (Ex. 1002, ¶130; *supra* Section IX.A.1(c).) As also discussed above with respect to claim element 1(c), a POSITA would have found it obvious to form the electrodes by deposition of a metallization layer. (Ex. 1002, ¶130; *supra* Section IX.A.1(c).)



(Ex. 1005, FIG. 3A (annotated); Ex. 1002, ¶130.)

The p-side electrode 14 portion of the metallization layer is "on a positively-doped surface of said positively-doped layer" and the n-side electrode portion is "on . . . said negatively-doped surface." (*Id.*, ¶[0048]; *see also id.*, ¶[0033]; Ex. 1002, ¶131.) The metallization layer formation disclosed for figure 3A is applicable to figure 18B. (Ex. 1002, ¶132.)

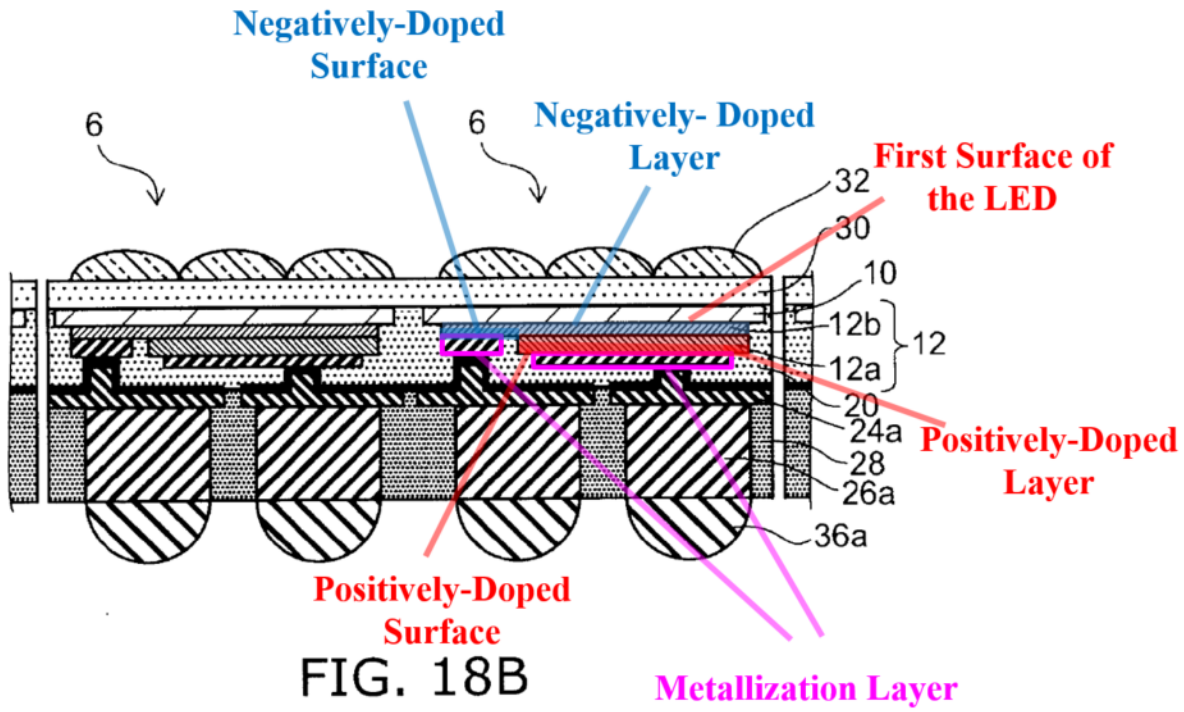


FIG. 18B

(*Id.*, FIG. 18B (annotated); Ex. 1002, ¶132.)

The metallization layer, which includes the p- and n-side electrodes, is connected to additional interconnect in order to allow electrical contact from outside the LED to the positively- and negatively-doped layers ("provide electrical contact with said positively-doped layer and said negatively doped layer of said LED"). (Ex. 1005, ¶¶[0033]-[0037]; Ex. 1002, ¶133.)

As shown in figure 18B above and consistent with the understanding of a POSITA, the "positively-doped surface," which corresponds to the lower surface of the positively doped layer, and the first surface, which is the top side of the negatively doped layer where it meets the sapphire layer, are "on opposing faces of said LED." (Ex. 1005, FIG. 18B; Ex. 1002, ¶134.)

e) depositing an optically permissive layer on said sapphire layer, said optically permissive layer comprising an optically definable material containing quantum dots and/or phosphor, said optically definable material adapted to change the frequency of at least some of the emitted light passing therethrough;

The Sugizaki-Camras combination discloses or suggests these limitations. (Ex. 1002, ¶¶135-136.) As discussed above with respect to claim element 1(e), Sugizaki discloses depositing a phosphor layer 30 ("optically permissive layer") on the surface of the sapphire layer 10. (*See supra* Section IX.A.1(e); Ex. 1005, ¶¶[0061], [0068], [0081], FIGs. 6A, 12A-12E, 18B; Ex. 1002, ¶135.)

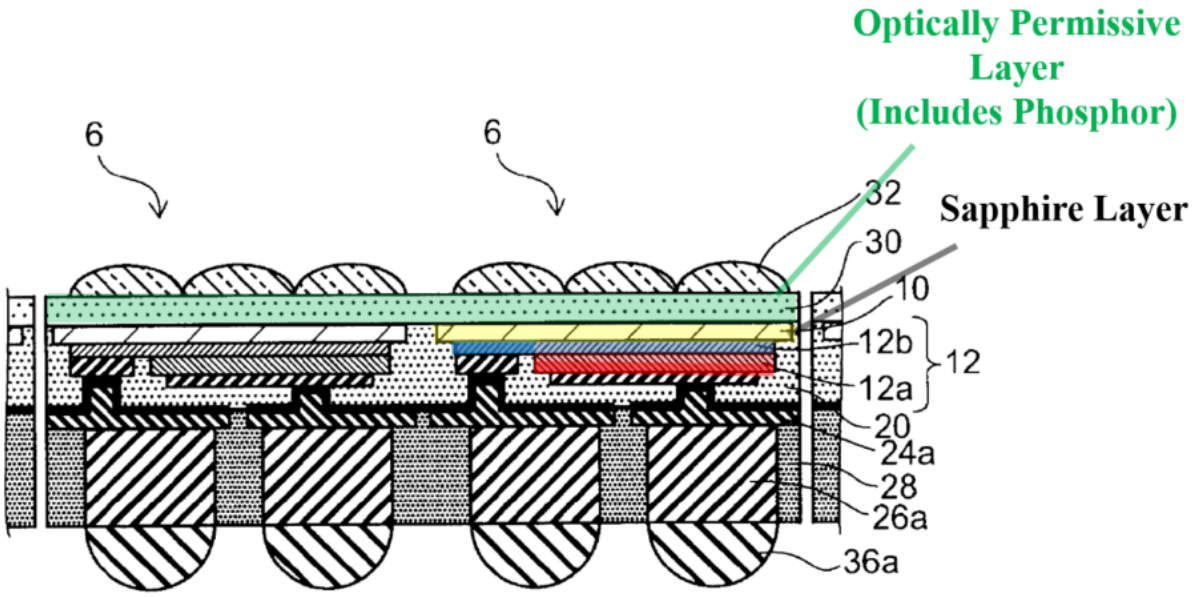


FIG. 18B

(Ex. 1005, FIG. 18B (annotated); Ex. 1002, ¶135.)

The phosphor layer 30 includes "an optically definable material containing quantum dots and/or phosphor," where the included phosphor is "adapted to change the frequency of at least some of the emitted light passing therethrough." (*See supra* Section IX.A.1(e); Ex. 1002, ¶136.)

f) depositing a passivation layer in direct contact with said metallization layer, said sapphire layer, a surface of said optically permissive layer, and said LED,

The Sugizaki-Camras combination discloses or suggests these limitations. (Ex. 1002, ¶¶137-138.) As discussed above with respect to claim element 1(g), Sugizaki discloses depositing a dielectric film ("passivation layer") in direct contact

with the metallization layer, the sapphire layer 10, the bottom surface of the phosphor layer ("optically permissive layer"), and the LED 12. (*See supra* Section IX.A.1(g); Ex. 1002, ¶138.)

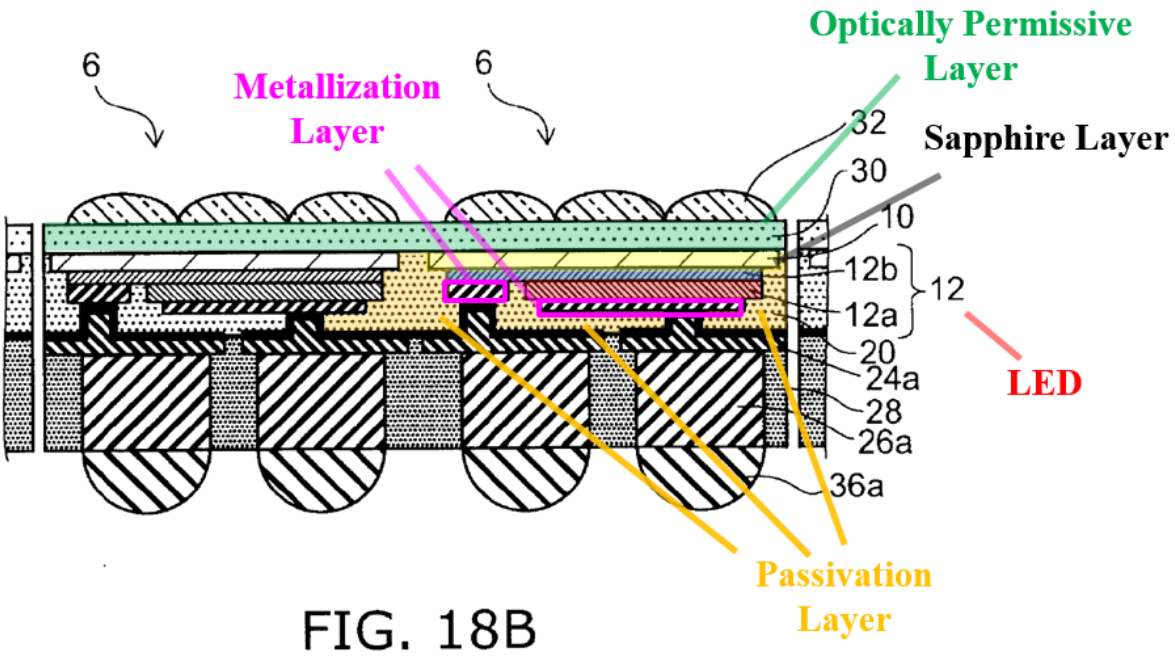


FIG. 18B

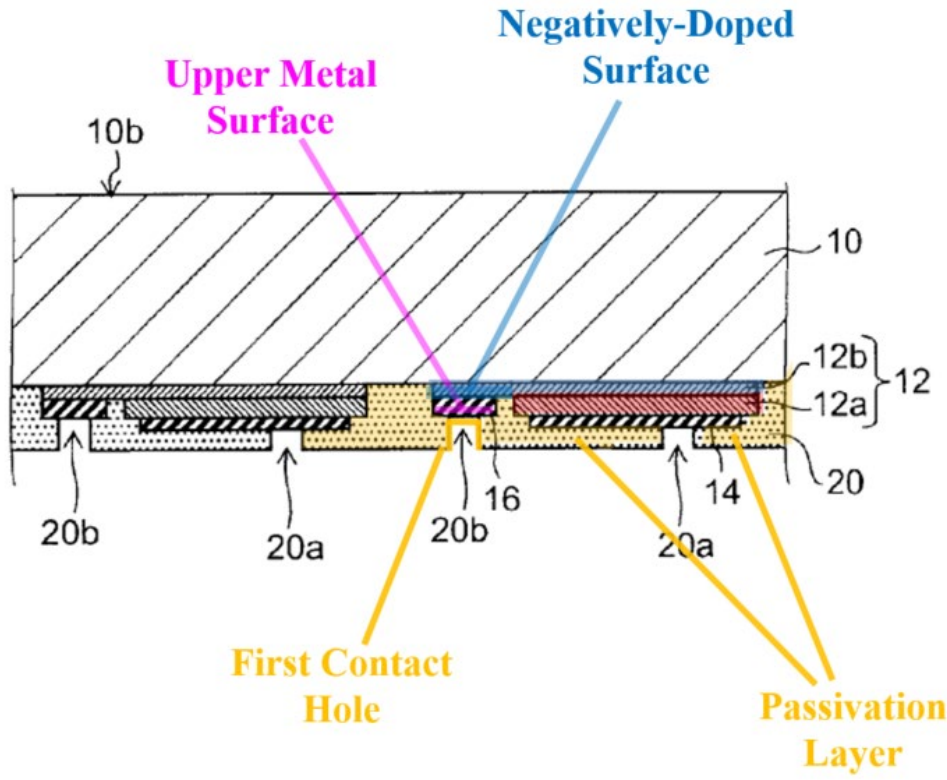
(Ex. 1005, FIG. 18B (annotated); Ex. 1002, ¶137.)

g) defining a first contact hole in said passivation layer to expose a first portion of an upper metal surface of said metallization layer disposed on said negatively-doped surface wherein said passivation layer is in direct contact with a second portion of said upper metal surface of said metallization layer disposed on said negatively-doped surface,

The Sugizaki-Camras combination discloses or suggests these limitations. (Ex. 1002, ¶¶139-140.) As discussed above with respect to claim element 1(h), a portion of the dielectric layer 20 ("passivation layer") is removed to define a first

contact hole that exposes the lower portion ("a first portion") of the n-side electrode 16 ("an upper metal surface of said metallization layer"). (*See supra* Section IX.A.1(h); Ex. 1005, Abstract, ¶¶[0007]-[0009], [0048], FIGs. 3C, 18B, claims 1, 9, 10; Ex. 1002, ¶139.)

FIG. 3C



(Ex. 1005, FIG. 3C (annotated); Ex. 1002, ¶139.)

The dielectric layer is also in direct contact with the portion of the upper metal surface that is not exposed by the contact hole ("said passivation layer is in direct contact with a second portion of said upper metal surface of said metallization layer disposed on said negatively-doped surface"). (*See supra* Section IX.A.1(h); Ex. 1005, FIG. 18B; Ex. 1002, ¶140.)

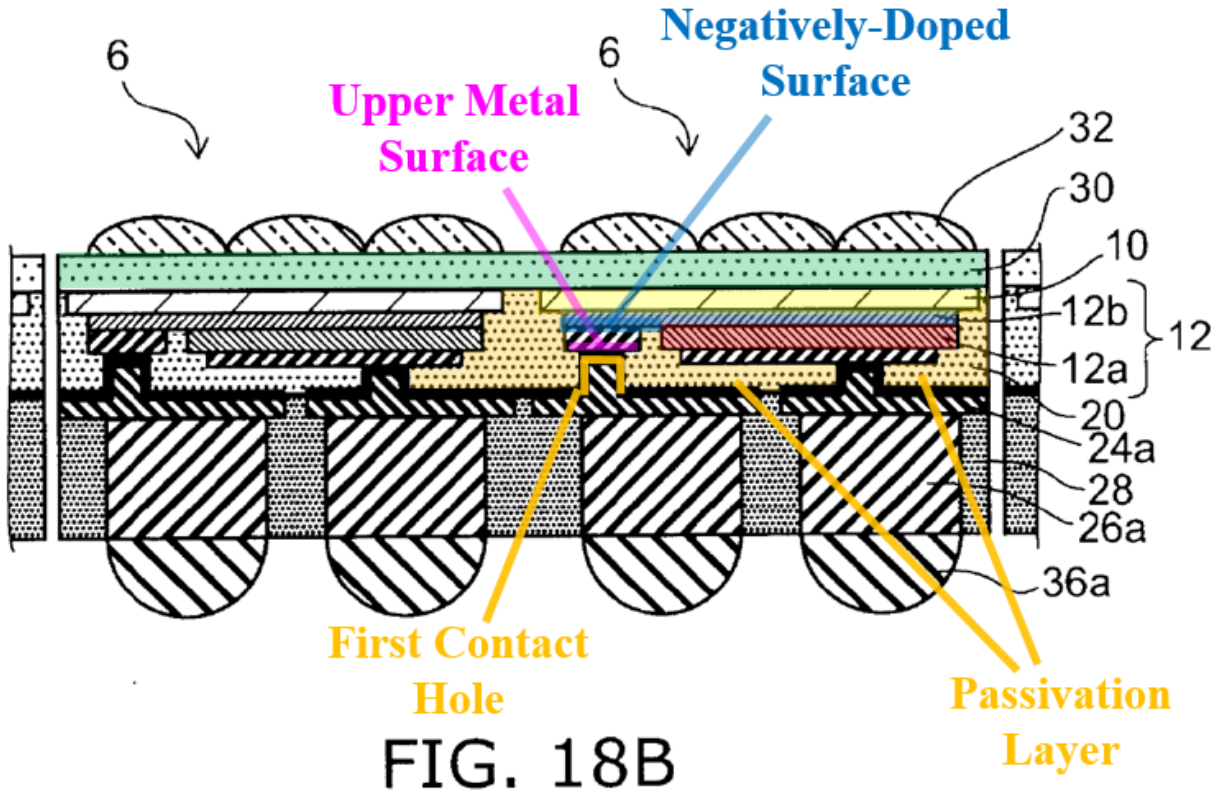


FIG. 18B

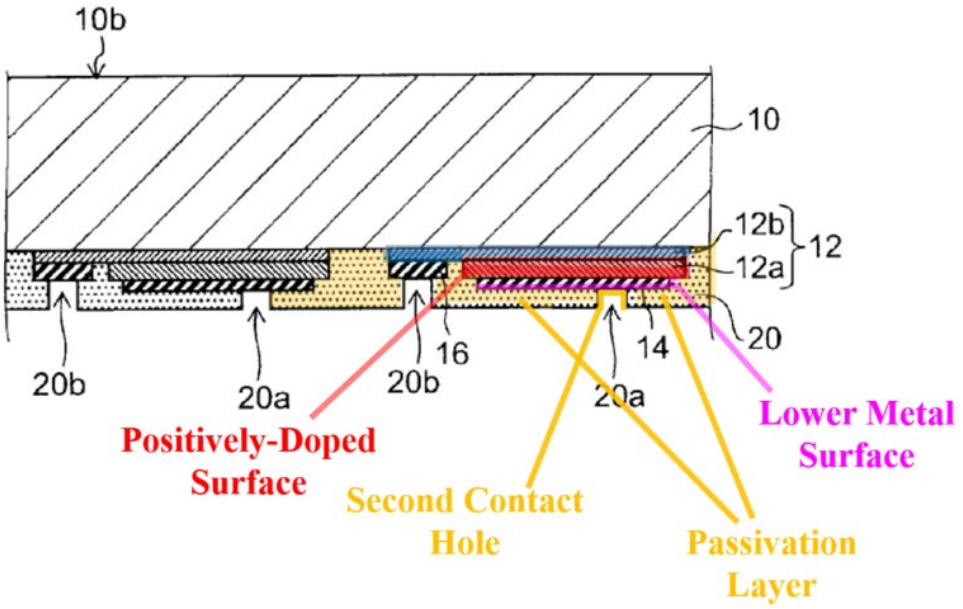
(Ex. 1005, FIG. 18B (annotated); Ex. 1002, ¶140.)

h) defining a second contact hole in said passivation layer to expose a first portion of a lower metal surface of said metallization layer disposed on said positively-doped surface wherein said passivation layer is in direct contact with a second portion of said lower metal surface of said metallization layer disposed on said positively-doped surface, and

The Sugizaki-Camras combination discloses or suggests these limitations. (Ex. 1002, ¶¶141-142.) For instance, as discussed above with respect to claim element 1(i), a portion of the dielectric layer 20 ("passivation layer") is removed to define a second contact hole that exposes the lower portion ("a first portion") of the p-side electrode 14 ("a lower metal surface of said metallization layer disposed on

said positively-doped surface"). (*See supra* Section IX.A.1(i); Ex. 1005, Abstract, ¶¶[0007]-[0009], [0048], FIGs. 3C, 18B, claims 1, 9, 10; Ex. 1002, ¶141.)

FIG. 3C



(Ex. 1005, FIG. 3C (annotated); Ex. 1002, ¶141.)

The dielectric layer is also in direct contact with the portion of the lower metal surface that is not exposed by the contact hole ("said passivation layer is in direct contact with a second portion of said lower metal surface of said metallization layer disposed on said positively-doped surface"). (*See supra* Section IX.A.1(i); Ex. 1005, FIG. 18B; Ex. 1002, ¶142.)

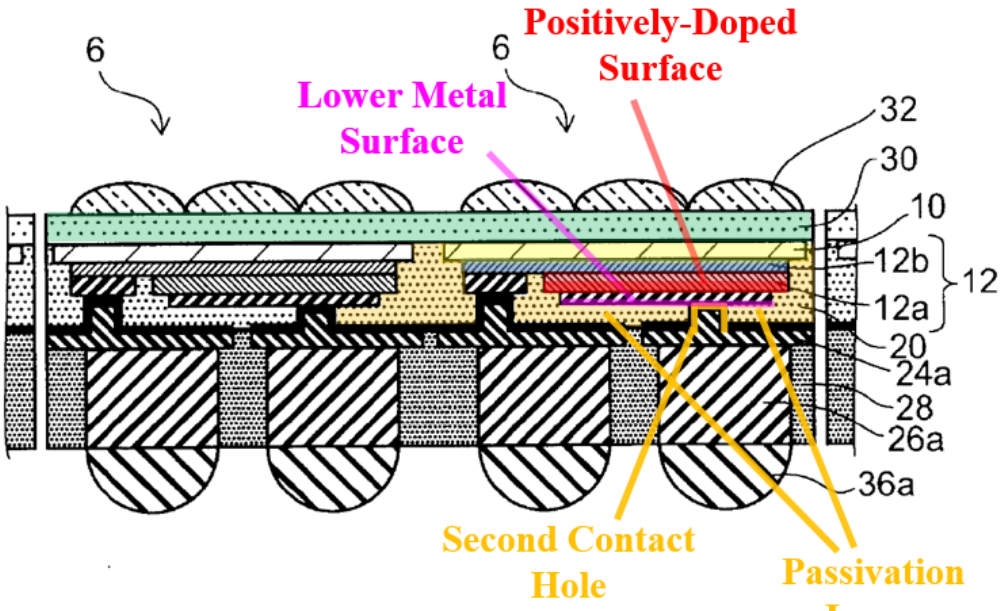


FIG. 18B

(Ex. 1005, FIG. 18B (annotated); Ex. 1002, ¶142.)

i) wherein said upper metal surface, said lower metal surface, said negatively-doped surface, said positively-doped surface, and said surface of said optically permissive layer are parallel with one another.

The Sugizaki-Camras combination discloses or suggests these limitations for the same reasons discussed above with respect to claim feature 1(j). (*See supra* Section IX.A.1(j); Ex. 1002, ¶143.)

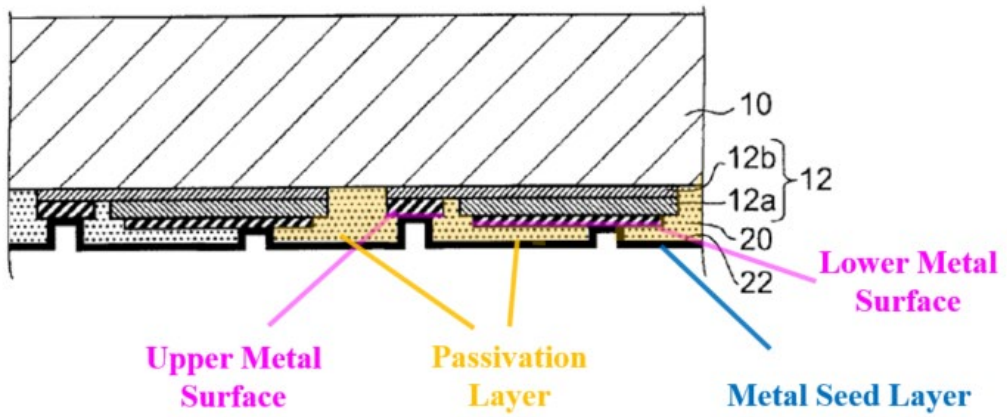
11. Claim 13

a) The method of claim 12, further comprising depositing a metal seed layer on said passivation layer, said upper metal surface of said metallization layer, and lower second metal surface of said metallization layer.

The Sugizaki-Camras combination discloses or suggests these features for the same reasons discussed with respect to claim 8 above. (*See supra* Section IX.A.6; Ex. 1002, ¶144.)[6] For example, Sugizaki discloses depositing a seed metal on the dielectric film ("passivation layer") as well as on the exposed surfaces of the n-side electrode ("upper metal surface of said metallization layer") and p-side electrode ("lower metal surface of said metallization layer"). (Ex. 1005, Abstract, ¶¶[0007]-[0008], [0033], [0048], FIGs. 2A, 3D, 6A, 18B, claims 1, 9.) Figure 3D of Sugizaki shows the deposition of seed metal layer 22 ("metal seed layer") in direct contact with the dielectric film ("passivation layer") and the n- and p-side electrodes 16 and 14, respectively, ("metallization layer"). The seed metal layer 22 is deposited by, for example, sputtering. (*Id*., ¶[0048]; Ex. 1002, ¶144.)

[6] For this proceeding, Petitioner assumes that the "lower second metal surface of said metallization layer" corresponds to the "lower metal surface" recited in claim 12. Petitioner, however, does not concede that claim 13 is not indefinite.

FIG. 3D



(Ex. 1005, FIG. 3D (annotated); Ex. 1002, ¶144.)

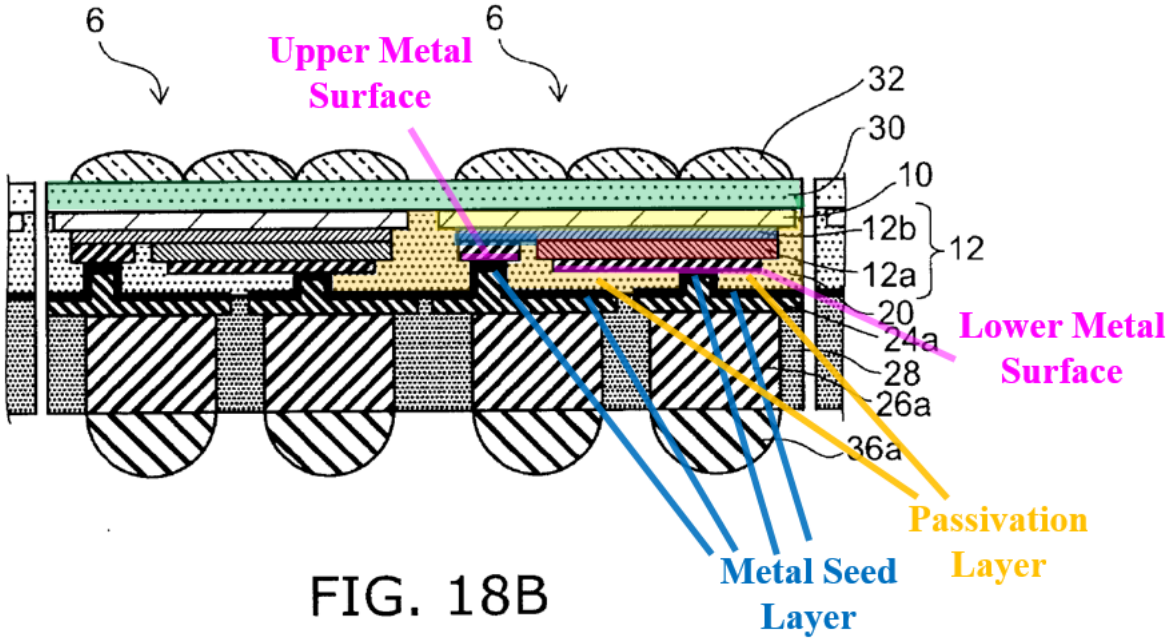


FIG. 18B

(Ex. 1005, FIG. 18B (annotated); Ex. 1002, ¶144.)

12. Claim 14

a) The method of claim 13 where said metal seed layer is comprised of a light reflecting material.

The Sugizaki-Camras combination discloses or suggests these features for the same reasons discussed above with respect to claim 11. (*See supra* Section IX.A.9; Ex. 1002, ¶145.)

13. Claim 15

a) The method of claim 13, further comprising depositing a metal layer on said seed metal layer, said metal layer having a thickness of between about 10 microns and about 40 microns.

The Sugizaki-Camras combination discloses or suggests these features for the same reasons discussed above with respect to claim 10. (*See supra* Section IX.A.8; Ex. 1002, ¶146.)

14. Claim 16

a) The method of claim 12, further comprising depositing an optically permissive cover substrate covering said optically permissive layer, said sapphire layer, and said LED.

The Sugizaki-Camras combination discloses or suggests these features. (Ex. 1002, ¶147.) For example, as discussed above with respect to claim feature 1(f), Sugizaki discloses depositing a layer of "optically permissive" material and then imprinting the lens pattern on that layer of material. (*See* supra Section IX.A.1(f); Ex. 1005, ¶¶[0075]-[0076], FIGs. 10A-10C; Ex. 1002, ¶147.) As shown in the

demonstrative below, the optically permissive cover substrate covers the optically permissive layer, the sapphire layer, and the LED. (Ex. 1002, ¶147.)

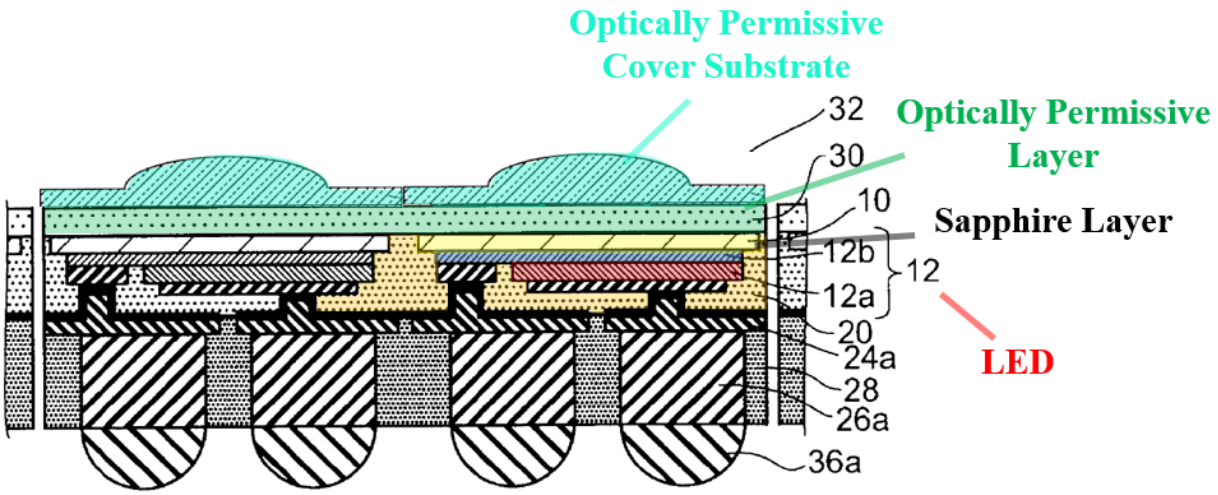


FIG. 18B

(Ex. 1005, FIG. 18B (modified, annotated); Ex. 1002, ¶147.)

B. Ground 2: Claim 4 Is Obvious Over Sugizaki in View of Camras and Tanimoto

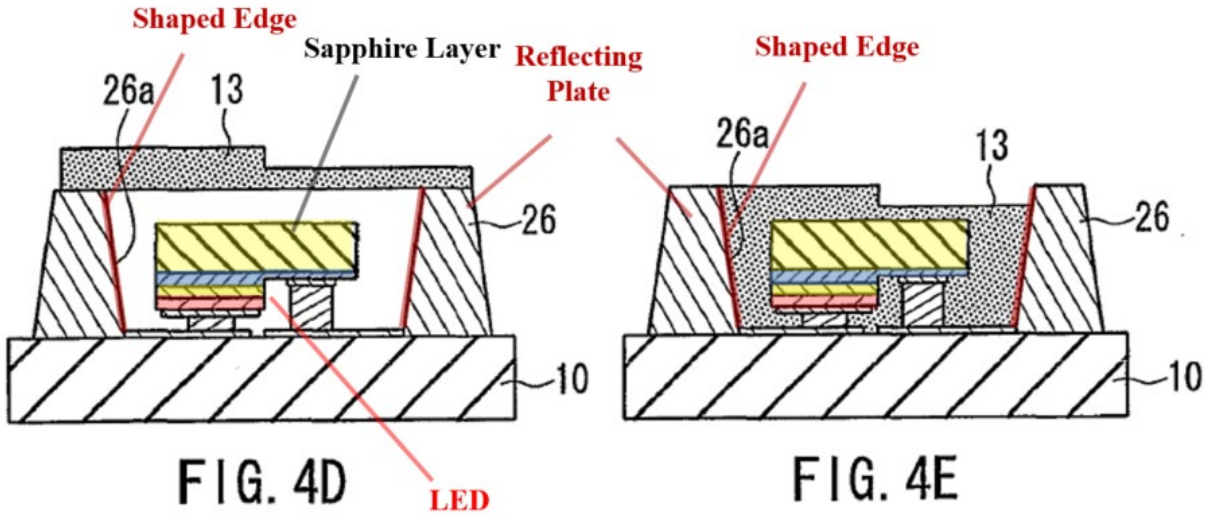
1. Claim 4

a) The light emitting device of claim 1, said passivation layer further comprising a shaped edge on a lateral portion of said passivation layer at least between said positively-doped surface and said first surface, said shaped edge configured to reflect light generated by said light emitting device outwardly therefrom.

Sugizaki in combination with the Camras and Tanimoto discloses or suggests these features. (Ex. 1002, ¶¶148-157.) As discussed above with respect to claim elements 1(g)-(i), the Sugizaki-Camras combination discloses or suggests a

passivation layer as recited in claim 1. (*See* supra Sections IX.A.1(g)-(h).) However, neither Sugizaki nor Camras explicitly disclose a shaped edge on a lateral portion of the passivation layer to reflect light as recited in claim 4. But Tanimoto discloses such a feature, and a POSITA would have found it obvious to include such a shaped edge on the passivation layer of the Sugizaki-Camras combination. (Ex. 1002, ¶149.)

Tanimoto, like Sugizaki and Camras, is directed to LED devices formed using a plurality of semiconductor layers on a sapphire substrate, where a layer that includes phosphor is used to adjust the wavelength of the light emitted by the LED. (Ex. 1007, ¶¶[0026], [0028], [0030]-[0031], [0048]; Ex. 1002, ¶150.) For example, figures 4D and 4E of Tanimoto, reproduced in annotated form below, show such an LED device, where a reflecting plate with a shaped edge is provided. (Ex. 1007, ¶¶[0059]-[0060].) Such a reflecting plate would help direct light generated by the LED outward from the LED (in a direction opposite the underlying substrate 10). (Ex. 1002, ¶150.)



(Ex. 1007, FIGs. 4D, 4E (annotated); Ex. 1002, ¶150.)

Tanimoto further discloses that the area between the shaped edges of the reflecting plate can be hollow or filed with a phosphor layer. (Ex. 1007, ¶¶[0059]-[0060].) In view of Tanimoto, a POSITA would have found it obvious to include a similarly configured reflecting plate in the LED of the Sugizaki-Camras combination in order to direct the light from the LED in the intended direction. (Ex. 1002, ¶151.)

A POSITA would have looked to Tanimoto for guidance regarding implementing LED devices as disclosed or suggested by the Sugizaki-Camras combination, particularly because Sugizaki, Camras, and Tanimoto are all references in the same field that disclose LED devices with many common features. (Ex. 1002, ¶152.) Having looked to Tanimoto, such a person would have been motivated to include a reflecting plate in the LED of the Sugizaki-Camras combination. (*Id.*)

As discussed above with respect to the Sugizaki-Camras combination, a passivation layer surrounds various aspects of the LED structure. (*See supra* Sections IX.A.1(g)-(i).) Tanimoto discloses LED structures that include a reflecting plate on both sides of the LED structure, where the reflecting plate directs the light generated by the LED. (Ex. 1007, ¶¶[0059]-[0060], FIGs. 4D, 4E.) A POSITA would have been motivated to use the reflecting plates as disclosed by Tanimoto in an LED device according to the Sugizaki-Camras combination because such reflecting plates facilitate the upward reflection of light to be emitted. (Ex. 1002, ¶¶153-154.) Indeed, Sugizaki discloses that that portions of the p- and n-side electrodes can be formed of reflecting material in order to aid in directing the generated light upward, thereby confirming the desirability of such upward reflection. (Ex. 1005, ¶[0049]; Ex. 1002, ¶154.)

A POSITA would have found it straightforward to use reflecting plates as disclosed by Tanimoto in an LED device according to the Sugizaki-Camras combination based on the person's knowledge and Tanimoto's disclosure as to how to implement such a feature in a similar device. (Ex. 1002, ¶155.) Moreover, such skilled person would have had a reasonable expectation of success in using reflecting plates in an LED device according to the Sugizaki-Camras combination because, as demonstrated by Tanimoto, such reflecting plates and similarly shaped features used

to direct light outward from LEDs were commonplace in the prior art. (Ex. 1002, ¶155.)

Indeed, including such reflecting plates in the LED of the Sugizaki-Camras combination would have been nothing more than applying a known feature (reflecting plates on both sides of the LED device as disclosed by Tanimoto) to a particular device (the LED of the Sugizaki-Camras combination) to achieve a predictable result (improved directionality of the light generated by the LED). *KSR*, 550 at 416. As discussed above, Sugizaki, Camras, and Tanimoto all describe LED devices for generating light, but Tanimoto describes reflecting plates not found in Sugizaki and Camras for providing upward light reflection. Therefore, a POSITA would have recognized that Tanimoto's teachings relating to improved light output through the use of reflecting plates could have been applied to the Sugizaki-Camras LED in a similar way. *Id.* at 417.

A POSITA would also have been motivated to include such reflecting plates in the Sugizaki-Camras-Tanimoto combination such that the area inside the reflecting places is filled by the passivation layer discussed above with respect to claim element 1(g) having a tapered shape on both sides of the LED. (Ex. 1002, ¶156.) The border of the area filled with the passivation layer would correspond to the area defined by the shaped edges of the reflecting plates shown in annotated figures 4D and 4E of Tanimoto above. (*Id*.) As such, the passivation layer would

have included a "shaped edge on a lateral portion of said passivation layer at least between said positively-doped surface and said first surface" as recited in claim 4. (*Id*.)

Moreover, the shaped edges, which correspond to the reflecting plates on the sides of the LED device "are configured to reflect light generated by said light emitting device outwardly therefrom" as also recited in claim 4. (*Id*., ¶157.) Indeed, the use of reflecting plates in conjunction with the passivation layer is consistent with the disclosure of the '405 patent. (Ex. 1001, 6:33-38 ("FIG. 9 illustrates an exemplary LED device 90 having a shaped [and] **optionally mirrored or metalized passivation layer 970** to enhance the performance of the device. The passivation at the diode side can be patterned in a manner to provide for example optical reflectivity by angling or shaping the edges 975 of passivation layer 970.") (emphasis added).) Tanimoto similarly discloses that the reflecting plates "may be e.g., **metal having a high reflectance such as aluminum** or a ceramic material having a high reflectance such as alumina." (Ex. 1007, ¶[0072] (emphasis added); Ex. 1002, ¶157.) Therefore, the Sugizaki-Camras-Tanimoto combination discloses or suggests the features of claim 4.

C. Ground 3: Claims 7 and 17 Are Obvious Over Sugizaki In View of Camras and Tanaka

1. Claim 7

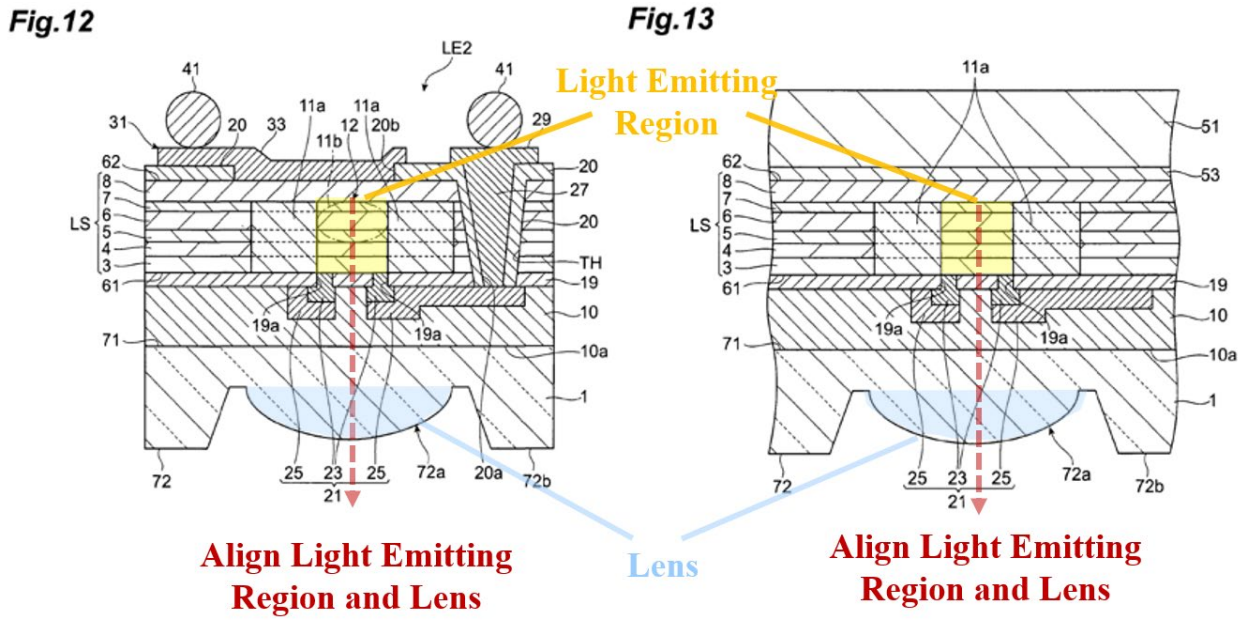
a) The light emitting device of claim 1, further comprising at least one alignment mark indicative of a required position of said device with respect to said optically permissive cover substrate.

Sugizaki in combination with the Camras and Tanaka discloses or suggests these features. (Ex. 1002, ¶¶158-166.)[7] Neither Sugizaki nor Camras explicitly disclose the use of alignment marks to position the LED with respect to the optically permissive cover substrate discussed above with respect to claim element 1(f) above. (*See supra* Section IX.A.1(f).) Tanaka, however, discloses such a feature, and a POSITA would have found it obvious to include such alignment marks in the LED device according to the Sugizaki-Camras combination. (Ex. 1002, ¶159.)

Tanaka, like Sugizaki and Camras, is directed to LED devices formed using a plurality of semiconductor layers, where a lens is affixed to the LED device. (Ex. 1008, ¶¶[0001], [0004]-[0006]; Ex. 1002, ¶160.) For example, annotated figures 12 and 13 of Tanaka, reproduced below, show such an LED device, where "the rear

[7] For this proceeding, Petitioner assumes "said device" in claim 7 refers to the LED as the cover substrate is part of the claimed "device" recited in the preamble of claim 1. Petitioner does not concede that claim 12 is not indefinite.

face 72 of the glass substrate 1 is formed with lens part 72a for receiving the light emitted from the multilayer structure LS." (Ex. 1008, ¶¶[0111]-[0112].)



(*Id*., FIGs. 12, 13 (annotated); Ex. 1002, ¶160.)

Tanaka discloses that the glass substrate 1 is bonded to the semiconductor substrate, where, as described by Tanaka, the lens is aligned with the light emitting region of the LED using a marker. (Ex. 1008, ¶¶[0115],[0116]; Ex. 1002, ¶¶161.)

A POSITA would have looked to Tanaka for guidance regarding implementing LED devices as disclosed or suggested by the Sugizaki-Camras combination, particularly because Sugizaki, Camras, and Tanaka are all references in the same field that disclose LED devices with many common features. (*Id*., ¶162.) Having looked to Tanaka, such a person would have found it obvious to include an

alignment mark in the LED device of the Sugizaki-Camras combination in order to allow an independently formed substrate that includes a lens to be properly deposited in a position on the LED device such that the lens properly directs the light generated by the LED. (*Id*.)

As discussed above with respect to the Sugizaki-Camras combination, both Sugizaki and Camras disclose the inclusion of a lens on the LED device in order to direct the light generated by the LED. (*See supra* Sections IX.A.1(f), IX.A.2.) Tanaka discloses LED structures that include multilayer bodies with a light emitting region, where an independently-formed lens is later affixed to the LED structure and a marker is used to ensure proper positioning of the lens with respect to the rest of the LED device. (Ex. 1008, ¶¶[0115]-[0116]; Ex. 1002, ¶163.) A POSITA would have found it obvious to use such an alignment mark, as disclosed by Tanaka, in conjunction with an LED device according to the Sugizaki-Camras combination. (Ex. 1002, ¶163.)

A POSITA would have been motivated to use an alignment mark as disclosed by Tanaka because such an alignment mark would have allowed independently-formed substrates ("optically permissive cover substrates") that include lenses to be used with the LED devices of the Sugizaki-Camras combination while still ensuring proper relative placement of the lens with respect to the LED. (Ex. 1002, ¶164.) Indeed, Tanaka discloses that because the glass substrate 1 including the lens 72a

"can be processed before bonding, the processing method is less restricted, which achieves a higher degree of freedom in designing the lenses in terms of lens forms and the like." (Ex. 1008, ¶[0120]; Ex. 1002, ¶164.)

A POSITA would have found it straightforward to use an alignment mark as disclosed by Tanaka in an LED device according to the Sugizaki-Camras combination as such alignment marks were commonplace in semiconductor manufacturing and often used to properly orient different layers and structures in such semiconductor devices. (Ex. 1002, ¶165; *see also* Ex. 1011, 1:33-35; Ex. 1012 ¶¶[0005]-[0007].)[8] Moreover, such a skilled would have had a reasonable expectation of success in using an alignment mark in an LED device according to the Sugizaki-Camras combination because, as demonstrated by Tanaka, such alignment marks were known for use in aligning a lens with a light emitting region in LED devices. (Ex. 1002, ¶166.) Indeed, doing so would have been nothing more than applying a known technique (including an alignment mark in the LED device as disclosed by Tanaka) to a particular device (the LED device of the Sugizaki-Camras combination) to achieve a predictable result (proper alignment of the LED and the overlying lens). (*Id*.); *KSR*, 550 at 416. Such an alignment mark is

[8] Koizumi (Ex. 1011) and Willwohl (Ex. 1012) demonstrate the knowledge of a POSITA.

"indicative of a required position of said device with respect to said optically permissive cover substrate" as recited in claim 7. (Ex. 1002, ¶166.)

2. Claim 17

a) The method of claim 16, further comprising placing one or more alignment marks on said LED so as to permit proper positioning of said LED with respect to an optically permissive cover substrate.

Sugizaki in combination with the Camras and Tanaka discloses or suggests these features. (Ex. 1002, ¶167.) As discussed above with respect to claim 7, a POSITA would have found it obvious to include an alignment mark in the LED device of the Sugizaki-Camras-Tanaka combination in order to allow a lens to be properly positioned with respect to the light emitting portion of the LED. A POSITA would have understood that such alignment marks could be placed on any one or more of the cover substrate, lens, and LED, in order to provide proper alignment of the structures. (*Id*.) Indeed, Tanaka discloses using a "double-sided aligner" thereby suggesting that marks on both the LED and cover substrate are aligned with each other. (*Id*.; Ex. 1008, ¶[0116]) Therefore, the Sugizaki-Camras-Tanaka combination discloses or suggests the features of claim 14.

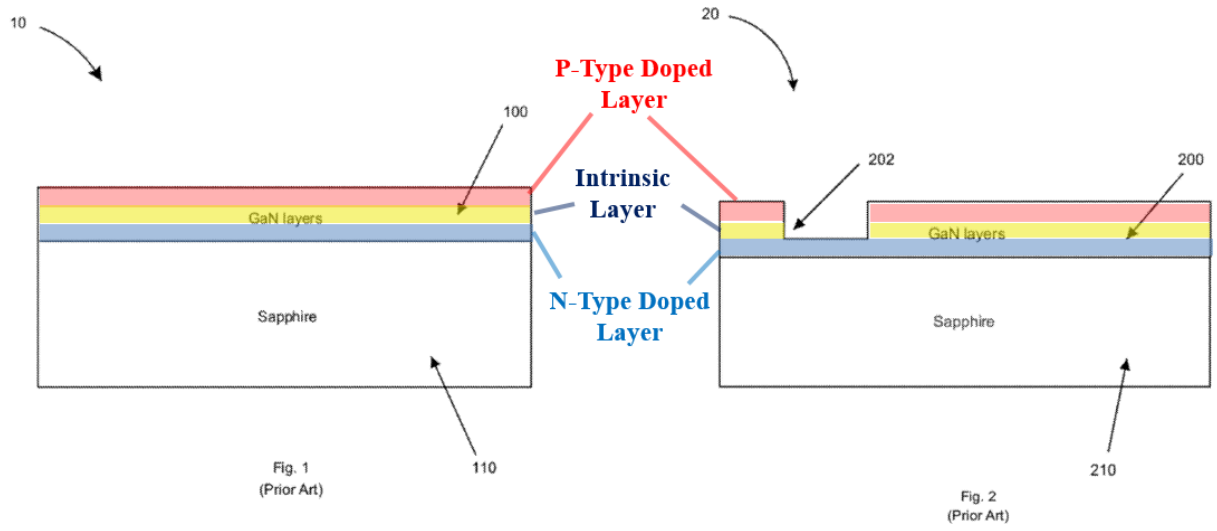
D. Ground 4: Claims 1, 3, and 8-16 Are Obvious Over Sugizaki In View of the AAPA[9]

Sugizaki in view of the AAPA discloses or suggests all of the features of claims 1, 3, and 8-16. (Ex. 1002, ¶¶168-178.) As discussed above with respect to the Sugizaki-Camras combination, Sugizaki discloses or suggests all of the features of claims 1, 3, and 8-16 with the exception of "an intrinsic region" "between said positively-doped region and said negatively-doped region" as recited in claim 1 and an "intrinsic layer" "between said positively-doped layer and a first surface of said LED" as recited in claim 12. (*See supra* Sections IX.A.1, IX.A.3, IX.A.6-14; Ex. 1002, ¶169.) As also discussed above, it would have been obvious to include such an intrinsic layer in an LED device like that disclosed by Sugizaki in view of Camras. (*See e.g. supra* Section IX.A.1(b).) A POSITA would also have found it obvious to include such an intrinsic layer in an LED device like that disclosed by Sugizaki in view of the Applicant Admitted Prior Art (AAPA) of the '405 patent, and therefore the Sugizaki-AAPA combination discloses or suggests all of the features of claims 1, 3, and 8-16. (Ex. 1002, ¶¶169-172.)

Figures 1 and 2 of the '405 patent illustrate prior art gallium nitride (GaN) LEDs that "are typically grown on a sapphire substrate." (Ex. 1001, 3:10-13, 3:34-

[9] Petitioners do not repeat the language of the challenged claims, which is presented above.

36, 3:44-46.) According to the '405 patent, "[t]hese LEDs comprise a P-I-N junction device having an intrinsic (I) layer disposed between a N-type doped layer and a P-typed doped layer." (*Id*., 3:13-16.) Figures 1 and 2 of the '405 patent, both of which are labeled "Prior Art," are annotated below to show the doped and intrinsic layers that the '405 patent describes as being present in prior art LED devices. (*Id*., 3:9-16, 3:33-35 ("FIG. 1 illustrates a LED device 10 **such as those described above** . . . ") (emphasis added), 3:44-47 ("FIG. 2 illustrates a LED device 20 like the one shown in FIG. 1 where a GaN layer 200 is disposed above a sapphire layer."), 3:64-4:8 (disclosing that figure 3 shows "the **result of metallization of the surface of the GaN layer 200 of the device of FIG. 2**," where "**the GaN layer 300 comprises a P-I-N junction** having strata therein including a P-type doped layer 301 that is proximal to the bulk surface of the GaN layer 300 and distal from the sapphire layer 310, a N-type doped layer 303 within GaN layer 300 that is proximal to the sapphire layer 310, and **an intrinsic (I) semiconductor layer 305 in the middle**, between the P and N type layers 301 and 303.") (emphases added.); Ex. 1002, ¶173.)



(Ex. 1001, FIGs. 1, 2 (annotated); Ex. 1002, ¶173.)

The multilayer body 12 disclosed by Sugizaki includes a p-type layer, an n-type layer, and a light emitting layer (Ex. 1005, ¶[0032]), but Sugizaki does not disclose additional details regarding the composition of the multilayer body 12, including the composition of the light emitting layer. (Ex. 1002, ¶174.) The '405 patent discloses that conventional LED structures that include a multilayer body with an intrinsic layer between a p-type layer and an n-type layer (P-I-N) were know in the art (Ex. 1001, 3:9-16, 3:33-35, 3:44-47, 3:64-4:8), and a POSITA would have found it obvious to use such a P-I-N multilayer body in an LED device as disclosed by Sugizaki. (Ex. 1002, ¶174.)

Sugizaki explicitly contemplates the use of different multilayer structures in conjunction with the disclosed LED devices (Ex. 1005, ¶[0104]) and a POSITA would have been motivated to use a well-known P-I-N multilayer body in

conjunction with the LED device disclosed by Sugizaki as such a multilayer body was well known and would provide the desired light emitting characteristics using a limited number of layers, which results in a simpler design, fewer processing steps, and reduced costs. (Ex. 1002, ¶¶175-176.) Indeed, according the Examiner that allowed the '405 patent, "[i]ncluding an undoped or intrinsic active region between the n- and p-sides makes the LED more efficient while maintaining higher breakdown voltage with lower reverse leakage by keeping n- and p- type dopants out of the active region." (Ex. 1004, 251.) Moreover, a skilled person would also have been motivated to use such a P-I-N multilayer body because Sugizaki does not disclose all of the details of the disclosed multilayer body, and, as confirmed by the '405 patent, such P-I-N multilayer bodies were well-known and within the capabilities of a POSITA. (Ex. 1002, ¶176.)

Using a P-I-N multilayer body would have simply been the use of a known feature (a P-I-N multilayer body as disclosed by the AAPA of the '405 patent) in a known device (an LED device as disclosed by Sugizaki) to achieve the expected result of a multilayer body that emits light when a bias voltage is applied across it. (*Id*., ¶177.) A POSITA would have had a reasonable expectation of success because such P-I-N multilayer bodies were well known, and Sugizaki specifically contemplates using different multilayer bodies. (*Id*.)

Therefore, the Sugizaki-AAPA combination discloses or suggests an LED device that includes an intrinsic region between the positive- and negative-doped regions as recited in claim 1 and an intrinsic layer between said positively-doped layer and a first surface of said LED as recited in claim 12. Sugizaki discloses or suggests the remaining features of claims 1, 3 and 8-16 for the reasons discussed above with respect to the Sugizaki-Camras combination. (*Supra* sections IX.A.1, IX.A.3, IX.A.6-14; Ex. 1002, ¶178.)

X. DISCRETIONARY DENIAL IS NOT APPROPRIATE

The Board should decline any arguments for a discretionary denial under 35 U.S.C. §§ 314(a) or 325(d). The '405 patent is not at issue in any other proceeding before the Board. Therefore, the factors concerning discretionary denial under 35 U.S.C. § 314(a) set forth in *General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper No. 19 at 3, 8, 15-19 (Sept. 6, 2017), are not applicable here. Nor does Petitioner rely on any art or arguments that are the same or substantially the same as those previously presented to the Office. *See Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (Feb. 13, 2020) (precedential).

Similarly, *NHK Spring Co., Ltd. v. Intri-Plex Techs, Inc.*, IPR2018-00752, Paper 8 (P.T.A.B. Sept. 12, 2018) does not apply here. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 3 (P.T.A.B. Mar. 20, 2020) (precedential) ("*NHK* applies … where the district court has set a trial date to occur earlier than the Board's deadline to issue a final written decision in an instituted proceeding."). The six-factor test addressed in *Fintiv* favors institution. *See id.*, 5-6.

For the *first factor* (stay), there is no stay, but courts routinely issue stays after institution. *Western Digital Corp. et al v. Kuster*, IPR2020-01391, Paper 10 at 8-9 (Mar. 11, 2021); *Samsung Elec. Am., Inc. v. Snik LLC*, IPR2020-01427, Paper 10 at

10 (Mar. 9, 2021). At a minimum, this factor deserves little weight given that factors two through four and six weigh in favor of institution. *See Fintiv*, 7.

The second (proximity of trial dates) and third (investment in parallel proceedings) factors weigh in favor of institution. The district court has not set a trial date, and, there has not been significant resource investment by the court and the parties, particularly compared to the resource expenditures leading up to a trial. *See Resideo Techs., Inc. v. Innovation Sciences, LLC*, IPR2019-01306, Paper 19 at 11 (Jan. 27, 2020). Furthermore, the court's order governing patent proceedings sets a default Markman hearing date as "23 weeks after [case management conference] (or as soon as practicable)" and a default trial date as "52 weeks after Markman hearing (or as soon as practicable)." (Ex. 1022, 9, 11); *see Precision Planting, LLC. v. Deere & Co.*, IPR2019-01044, Paper 17 at 14-15 (P.T.A.B. Dec. 2, 2019) (weighs against finding that case is at "an advanced stage"); *Abbott Vascular, Inc. v. FlexStent, LLC*, IPR2019-00882, Paper 11 at 30 (P.T.A.B. Oct. 7, 2019) (same). Additionally, WDTX civil trials "may possibly slip" due to "months of backlogged trials." *HP Inc. v. Slingshot Printing LLC*, IPR2020-01085, Paper 12 at 7 (Jan. 14, 2021). Nevertheless, even "an early trial date" is "non-dispositive" and simply means that "the decision whether to institute will likely implicate other factors," which, as explained, favor institution. *Fintiv*, 5, 9.

Furthermore, the Board has held "that it is often reasonable for a petitioner to wait to file its petition until it learns which claims are being asserted against it in the parallel proceeding." *Id.* at 11.

The fourth factor (overlap) also weighs in favor of institution. PO's infringement contentions only assert claims 1-5, 7-9, 11-14, 16, and 17 of the '405 patent while the present Petition challenges claims 1-17 of the '405 patent. (Section IX.) Moreover, Petitioner hereby stipulates that, if the IPR is instituted, Petitioner will not pursue the IPR grounds in the district court litigation. Thus, "[i]nstituting trial here serves overall system efficiency and integrity goals by not duplicating efforts and by resolving materially different patentability issues." *Apple, Inc. v. SEVEN Networks, LLC*, IPR2020-00156, Paper 10 at 19 (P.T.A.B. June 15, 2020) (finding the fourth factor "strongly favored" institution even though there was no stipulation and a significant dispute about the extent of overlap); *see also Sand Revolution II, LLC v. Continental Intermodal Group-Trucking LLC*, IPR2019-01393, Paper 24 at 12 (P.T.A.B. June 16, 2020) (finding the fourth factor weighs in favor of institution due, in part, to petitioner's stipulation that it will not pursue the same grounds in district court).

For the fifth factor (parties), the Petitioner and PO are the same parties as in district court.

The sixth factor (other circumstances) weighs in favor of institution given the undeniable similarity between Petitioner's primary reference and the '405 patent and that Petitioner diligently filed this Petition within six months of PO's complaint. (Ex. 1021). Institution is consistent with the significant public interest against "leaving bad patents enforceable." *Thryv, Inc. v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020). This Petition is the ***sole*** challenge to the '405 patent before the Board—a "crucial fact" favoring institution. *Google LLC v. Uniloc 2017 LLC*, IPR2020-00115, Paper 10 at 6 (May 12, 2020).

XI. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 1-17 of the '405 patent based on each of the grounds specified in this petition.

Respectfully submitted,

Dated: September 3, 2021 By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,952,405 contains, as measured by the word-processing system used to prepare this paper, 13,974 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: September 3, 2021

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on September 3, 2021, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,952,405 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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A courtesy copy was also sent via electronic mail to the Patent Owner's litigation counsel at the following addresses:

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