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CBI 12-070

November 15, 2011

VIA HAND DELIVERY

The Honorable James R. Holbein
Secretary
U.S. International Trade Commission
500 E Street, S.W., Room 112
Washington, D.C. 20024

Re: *In the Matter of Certain Semiconductor Chips with DRAM Circuitry, and Modules and Products Containing Same*

Dear Secretary Holbein:

Enclosed for filing on behalf of Complainants Elpida Memory, Inc. and Elpida Memory (USA) Inc. (collectively "Elpida" or "Complainants") are documents supporting Elpida's request that the Commission commence an investigation pursuant to Section 337 of the Tariff Act of 1930, as amended. A request for confidential treatment of the Confidential Complaint Confidential Exhibits 27C – 35C is included in this filing.

As described below, the original and all required copies of the Complaint are in paper form. All other exhibits and appendices attached thereto are in electronic form and are being provided on CDs. If any additional paper copies of documents are needed, Complainants will provide those copies at the Secretary's request.

Elpida submits the following documents to accompany the Complaint filing:

1. An original and eight (8) copies of both the verified Non-Confidential Complaint and verified Confidential Complaint in paper form pursuant to Rule II.C.(2)(b)(i) of the United States International Trade Commission Handbook on Filing Procedures, effective November 7, 2011;

2. Two (2) copies of both the verified Non-Confidential Complaint and verified Confidential Complaint in paper form pursuant to Commission Rule 210.11(a)(i), intended for service on each proposed respondent;

3. One (1) copy of both the verified Non-Confidential Complaint and the verified Confidential Complaint in paper form pursuant to pursuant to Commission Rule 210.11(a)(ii), intended for service on the Taipei Economic and Cultural Representative Office in the U.S.;

4. Three (3) copies of the Non-Confidential Exhibits in support of the Complaint in electronic form (on CDs) pursuant to Rule II.C.(2)(b)(i) of the United States International Trade Commission Handbook on Filing Procedures, effective November 7, 2011 intended for 1) the Commission and 2) each proposed respondent;

5. Three (3) copies of the Confidential Exhibits in support of the Complaint in electronic form (on CDs) pursuant to Rule II.C.(2)(b)(i) of the United States International Trade Commission Handbook on Filing Procedures, effective November 7, 2011 intended for 1) the Commission and 2) each proposed respondent;

6. Copies of United States Patent Nos. 6,150,689 ("the '689 Patent"), 6,635,918 ("the '918 Patent"), 6,555,861 ("the '861 Patent"), 7,659,571 ("the '571 Patent"), 7,713,828 ("the '828 Patent"), 7,495,453 ("the '453 Patent"), and 7,906,809 ("the '809 Patent) (collectively, "the Asserted Patents") included as Exhibits 1-7, respectively pursuant to Commission Rule 210.12(a)(9)(i) (certified copies forthcoming);

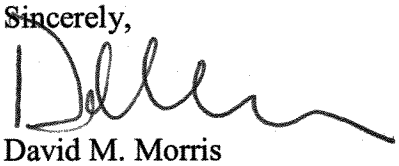
7. Copies of the assignments for the Asserted Patents included as Exhibits 8-14, respectively, pursuant to Commission Rule 210.12(a)(9)(ii) (certified copies forthcoming);

8. An original and four (4) copies of the prosecution histories of each of the Asserted Patents in electronic form (on CDs) as Appendices A-G pursuant to Commission Rule 210.12(c)(1) (certified copies for the '689, '918, '861, and '453 Patents forthcoming); and

9. An original and four (4) copies of the technical references identified in the prosecution histories of the Asserted Patents in electronic form (on CDs) as Appendices H-N pursuant to Commission Rule 210.12(c)(2) .

Please contact me if you have any questions about this submission. Thank you for your assistance in this matter.

Sincerely,



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500 E Street, S.W. Room 112
Washington, D.C. 20024

Re: In the Matter of Certain Semiconductor Chips with DRAM Circuitry, and Modules and Products Containing Same

Dear Secretary Holbein:

This firm represents Complainants Elpida Memory, Inc. and Elpida Memory (USA) Inc. ("Elpida" or "Complainants"), who are currently filing a Complaint pursuant to Section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337.

In accordance with Commission Rules 201.6, 210.5, 19 C.F.R. §§ 201.6, and 210.5, Complainants request confidential treatment of the confidential business information contained in the Confidential Complaint and Confidential Exhibits 27C-35C.

The information for which confidential treatment is sought is proprietary information not otherwise publicly available. Specifically, the Confidential Complaint contains proprietary information related to Elpida's licenses, products, and investments in the domestic industry. Exhibit 27C contains proprietary commercial information related to Elpida's licenses. Exhibit 28C contains proprietary commercial information related to Elpida's investments in the domestic industry. Finally, Exhibits 29C-35C contain proprietary technical information.

The information described above qualifies as confidential business information pursuant to Rule 201.6(a) because:

1. It is not available to the general public;

2. Unauthorized disclosure of such information could cause substantial harm to the competitive position of Complainants; and

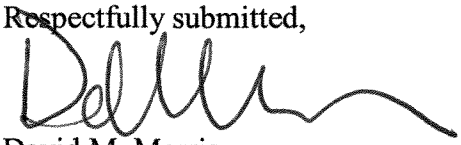
3. The disclosure of the information could impair the Commission's ability to obtain information necessary to perform its statutory function.

In accordance with 19 C.F.R. § 201.6(b)(iv), copies of each of the Complaint and Confidential Exhibits 27C-35C are enclosed with an indication on the cover the portions thereof that include confidential information and with the materials therein containing confidential information identified with brackets. In accordance with 19 C.F.R. § 201.6(b)(v), a copy of a nonconfidential version of the complaint is provided. There are no nonconfidential versions of Exhibits 27C-35C as confidential information is located throughout these exhibits.

For good cause shown, I respectfully request confidential treatment of the Confidential Complaint and Exhibits 27C-35C in support of the Complaint. Please contact me if you have any questions about this request or if this request is not granted in full.

By my signature below, I declare under penalty of perjury that information substantially identical to the proprietary information identified above is not available to the public.

Respectfully submitted,



David M. Morris
Morgan, Lewis & Bockius LLP
Counsel for Complainants
Elpida Memory, Inc.
Elpida Memory (USA) Inc.

Enclosures

UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C. 20436

In the Matter of	)	
CERTAIN SEMICONDUCTOR CHIPS WITH DRAM CIRCUITRY, AND MODULES AND PRODUCTS CONTAINING SAME	)	Investigation No. 337-TA-_____

COMPLAINT UNDER SECTION 337 OF
THE TARIFF ACT OF 1930, AS AMENDED

COMPLAINANTS:

ELPIDA MEMORY, INC.
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Telephone: +81-3-3281-1500

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1175 Sonora Court
Sunnyvale, CA 94086
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RESPONDENTS:

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No. 669, FuhShing 3RD,
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TABLE OF EXHIBITS

PUBLIC EXHIBITS

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Exh. 3	Copy of U.S. Patent No. 6,555,861
Exh. 4	Copy of U.S. Patent No. 7,659,571
Exh. 5	Copy of U.S. Patent No. 7,713,828
Exh. 6	Copy of U.S. Patent No. 7,495,453
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Exh. 12	Copies of recorded assignments for the Asserted Patent U.S. Patent No. 7,713,828
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APPENDICES

App. A	Copy of the prosecution history of U.S. Patent No. 6,150,689 and three

I. INTRODUCTION

1. Elpida Memory, Inc. and Elpida Memory (USA) Inc. (collectively, "Elpida" or "Complainants") file this Complaint pursuant to Section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337 ("Section 337"), based on the unlawful importation into the United States, the sale for importation, and/or the sale within the United States after importation, of certain DRAM (Dynamic Random Access Memory) semiconductor devices manufactured, imported and/or sold by, or on behalf of, Nanya Technology Corporation ("Nanya Taiwan") and Nanya Technology Corporation U.S.A. ("Nanya USA") (collectively, "Nanya" or "Respondents") which embody the circuits, structural features and/or are made by processes claimed in certain United States patents owned by Elpida Memory, Inc.

2. This Complaint is directed to certain Nanya and/or Nanya Elixir branded DRAM semiconductor products including: (1) the Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and other similarly structured infringing Nanya and Nanya Elixir 50nm "B die" SDRAM products, including, but not limited to, the Nanya Elixir N2CB2G16BP-DI, N2CB2G16BP-CG, N2CB2G16BP-BE, N2CB2G80BN-DI, N2CB2G80BN-BE, N2CB2G40BN-DI, N2CB2G40BN-CG and N2CB2G40BN-BE SDRAM 50nm semiconductor devices; (2) the Nanya Elixir DRAM memory modules M2F2G64CB88B7N-BE, M2F2G64CB88B7N-DI, M2F2G64CB88B7N-CG, M2F4G64CB8HB5N-BE, M2F4G64CB8HB5N-DI, M2F4G64CB8HB5N-CG, M2F2G64CB88BHN-BE, M2F2G64CB88BHN-DI, M2F2G64CB88BHN-CG, M2F4G64CB8HB9N-BE, M2F4G64CB8HB9N-DI, M2F4G64CB8HB9N-CG, M2S2G64CB88B5N-BE, M2S2G64CB88B5N-CG, M2S4G64CB8HB5N-BE, M2S4G64CB8HB5N-CG, M2S1G64CBH4B5P-BE, M2S1G64CBH4B5P-CG, and other Nanya or Nanya Elixir DRAM

memory modules containing one or more of the Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM device or other similarly structured Nanya or Nanya Elixir 50nm "B die" SDRAM products such as the Nanya Elixir N2CB2G16BP-DI, N2CB2G16BP-CG, N2CB2G16BP-BE, N2CB2G80BN-DI, N2CB2G80BN-BE, N2CB2G40BN-DI, N2CB2G40BN-CG and N2CB2G40BN-BE SDRAM semiconductor devices; (3) the Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM, and other similarly structured Nanya or Nanya Elixir 42nm "D die" SDRAM products; (4) the Nanya Elixir DRAM memory module M2S2G64CB88D5N-CG and other Nanya or Nanya Elixir DRAM memory modules which contain the Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM or other similarly structured Nanya or Nanya Elixir 42nm "D die" SDRAM products; (5) the Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3 and other similarly structured Nanya or Nanya Elixir 68nm "C die" SDRAM products; (6) the Nanya Elixir DRAM module M2Y2G64CB8HC5N-CG and other Nanya or Nanya Elixir DRAM memory modules which contain one or more of the Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3 or other similarly structured Nanya or Nanya Elixir 68nm "C die" SDRAM products; and (7) products containing one or more of (a) Nanya or Nanya Elixir 50nm "B die" SDRAM products that have similar structure as the Nanya Elixir 50nm products listed above, and/or (b) Nanya or Nanya Elixir 42nm "D die" SDRAM products that have similar structure as the Nanya Elixir 42nm product listed above, and/or (c) Nanya or Nanya Elixir 68nm "C die" SDRAM products that have similar structure as the Nanya Elixir 68nm product listed above (collectively the "Accused Products").

3. The Accused Products are sold as stand-alone products and, on information and belief, are used in many consumer products, such as laptop computers, personal computers

and/or computer servers, and are imported into the United States and sold after importation by, and/or on behalf of, Respondents.

4. Each of the Accused Products infringes at least one or more of the following claims of Elpida Memory, Inc.'s patents: (i) claims 1-6, 8-11 and 15-18 of United States Patent No. 6,150,689 ("the '689 Patent"); (ii) claims 1-16 and 18-21 of United States Patent No. 6,635,918 ("the '918 Patent"); (iii) claims 1, 3, 4 and 9-14 of United States Patent No. 6,555,861 ("the '861 Patent"); (iv) claims 1, 3 and 4 of United States Patent No. 7,659,571 ("the '571 Patent"); (v) claims 1, 5 and 6 of United States Patent No. 7,713,828 ("the '828 Patent"); (vi) claims 1, 15 and 27 of United States Patent No. 7,495,453 ("the '453 Patent"); and claims 1 and 2 of U.S. Patent No. 7,906,809 ("the '809 patent")(collectively, "the Asserted Claims of the Asserted Patents").

5. Certified copies of the Asserted Patents are either attached as Exhibit Nos. 1 through 7, respectively, or will be submitted upon receipt from the U.S. Patent and Trademark Office. Elpida Memory, Inc. owns all right, title, and interest in each of the Asserted Patents. Certified copies of recorded assignments demonstrating the chain of title of the Asserted Patents are either attached as Exhibit Nos. 8 through 14, respectively, or will be submitted upon receipt from the U.S. Patent and Trademark Office.

6. The proposed respondents are Nanya Taiwan and Nanya USA.

7. An industry as required by 19 U.S.C. § 1337(a)(2) and (3) exists in the United States relating to the technology protected by the Asserted Patents.

8. As set forth more fully below, Elpida seeks, as relief, a permanent, limited exclusion order, or if proven to be appropriate pursuant to discovery in this matter, a general exclusion order, barring from entry into the United States all infringing Nanya and/or Nanya Elixir SDRAM products that are sold for importation into the United States, imported, or sold after importation by or on behalf of Nanya. Elpida also seeks, as relief, cease and desist orders prohibiting Respondents' sale for importation into the United States, importation, sale after importation into the United States, offer for sale, solicitation of sales, advertising, testing, technical support, and other commercial activity related to Nanya and/or Nanya Elixir SDRAM products and products containing the same that infringe one or more of the Asserted Claims of the Asserted Patents.

II. COMPLAINANTS

9. Elpida Memory, Inc. is a Japanese corporation having its headquarters and principal place of business at Sumitomo Seimei Yaesu Bldg. 3F, 2-1 Yaesu 2-chome, Chuo-ku, Tokyo 104-0028, Japan. Elpida Memory (USA) Inc. a wholly-owned subsidiary of Elpida Memory, Inc., is a Delaware corporation with its principal place of business at 1175 Sonora Court, Sunnyvale, California 94086. Elpida Memory, Inc. holds all right, title, and interest in the Asserted Patents. (Exhibit Nos. 8-14.)

10. Elpida is a leading designer and manufacturer of DRAM integrated circuits, and is recognized as an industry leader in developing DRAM solutions for a wide range of applications. Elpida develops high-density, high-speed, high-quality DRAM products that support the growing functional sophistication of computer servers, personal computers, mobile communication devices, and other electronic devices requiring DRAM.

11. Elpida's innovations include semiconductor devices that successfully reduce leakage currents of semiconductor devices in the DRAM, dynamically adjust impedances of the DRAM, allow for increased integration of semiconductor circuits in the DRAM, allow for increased memory capacity of the DRAM, and reduce electrical interferences within the DRAM memory cells and peripheral circuits.

12. Elpida has also developed advanced process technologies that bring greater productivity to semiconductor device manufacturing, such as novel methods of filling a contact conductor plug in a contact hole during fabrication and novel methods of producing improved metal-oxide-semiconductor (MOS) field-effect transistors within the DRAM.

13. Elpida engages in engineering, testing, support, repair, and product design services at Elpida Memory (USA) Inc.'s principal place of business in Sunnyvale, California, including engineering, testing, support, repair, and product design for Elpida's DRAM products utilizing Elpida's patented DRAM technology.

III. PROPOSED RESPONDENTS

14. On information and belief, Respondent Nanya Taiwan is a corporation organized and existing under the laws of Taiwan (R.O.C.), with its principal place of business located at No. 669, FuhShing 3RD, KueiShan, TaoYuan, Taiwan, R.O.C. (Exhibit No. 15.)

15. On information and belief, Nanya Taiwan is in whole or in part responsible for the design, fabrication, manufacturing, testing, shipping, sales and marketing of Nanya DRAM products, including the Accused Products.

16. On information and belief, Nanya Taiwan is involved in the sale for importation, importation, and sale after importation of the Accused Products.

17. On information and belief, Nanya Taiwan's DRAM products, including the Accused Products, are included in electronic consumer goods, including computer servers, laptops and/or desk top computers manufactured by major computer manufacturers in the United States and/or major computer manufactures outside of the United States who import computer servers, laptops and/or desk top computers into the United States.

18. On information and belief, Respondent Nanya USA is a corporation organized and existing under the laws of California, with its principal place of business located at 5104 Old Ironsides Dr., Suite 113, Santa Clara, CA 95054. (Exhibit No. 16.)

19. On information and belief, Nanya USA is a wholly owned independent subsidiary of Nanya Taiwan and is in whole or in part responsible for sales and marketing of Nanya Taiwan's DRAM products, including the Accused Products, throughout the United States.

20. On information and belief, Nanya USA is in whole or in part responsible for selling, offering for sale and importation of Nanya's DRAM products, including the Accused Products, into the United States.

IV. THE TECHNOLOGY AND PRODUCTS AT ISSUE

21. The descriptions of the technology at issue that are set forth in this section are intended as general descriptions of the technology and improvements, and the descriptions particular to each Asserted Patent are separately set forth below in Section V. The technologies at issue relate generally to DRAM semiconductor memory products and methods of

manufacturing DRAM semiconductor memory products. Elpida's Asserted Patents are generally directed to DRAM semiconductor device designs, and methods of manufacturing DRAM devices, that address the technical, material and system challenges arising from the design of high-speed, highly integrated DRAM semiconductor devices that require increasingly larger numbers of integrated circuits and memory cells in order to increase the DRAM device's memory capacity, but with lower power consumption and at faster speeds. Achieving these goals requires designing ever smaller and more highly integrated devices such as metal-oxide-semiconductor (MOS) field-effect transistors, metal-insulator-semiconductor field-effect transistors, conductors and capacitors that are used in DRAM circuits. These goals introduce new challenges caused by physical and electrical limitations of the materials used to form these and other semiconductor devices in highly integrated DRAM circuits.

22. For example, the Asserted Patents disclose DRAM semiconductor devices and methods of manufacturing DRAM devices within highly-integrated circuits that incorporate several field-effect transistors and capacitors, which may include either MOSFETs (metal-oxide-semiconductor field effect transistors) and/or MISFETs (metal-insulator-semiconductor field effect transistors) arranged in various topologies, that result in improved circuit resistances, reduced power consumption, and yield greater memory capacity for the DRAM, but without sacrificing operating speed.

23. The Asserted Patents also disclose DRAM semiconductor devices utilizing memory cells having novel stacked capacitor structures, wherein multiple MISFET transistors are designed in "capacitor over bitline" (COB) structures such that the information storage capacitor is designed to be "over" the bit lines and the MISFETs. The Asserted Patents also

disclose DRAM devices with novel word line designs that have lower resistances by using novel structures and materials.

24. The Asserted Patents also disclose DRAMs with improved and novel contact conductor plugs in contact holes that are more easily manufactured and provide better electrical contact to the transistors and with less resistance by using novel designs and materials.

25. The Asserted Patents also disclose devices and methods of manufacturing DRAMs with much improved and novel MOS transistor and MISFET transistor designs, utilizing novel insulating films for the gate electrodes of the transistors.

26. The Asserted Patents also disclose DRAMs using transistors having novel trench-gate-type electrode structures that prevent occurances of electrical breakdowns in the transistors and minimize resistance defects between the gate electrode of the transistor and the source or drain regions of the transistor.

27. The Asserted Patents also disclose novel methods of manufacturing MOS transistors of a DRAM by creating improved contact plugs for the source and drain regions of the MOS transistors. The Asserted Patents also disclose novel methods of manufacturing a MOS transistor of a DRAM by creating improved contact plugs for the source and drain regions of the MOS transistor.

28. The Asserted Patents also disclose DRAM devices using a novel output circuit for the DRAM, whereby the the output impedance of the DRAM is dynamically adjusted and calibrated quickly, depending on the operating conditions of the DRAM.

29. On information and belief, the Nanya Elixir memory modules M2F2G64CB88B7N-BE, M2F2G64CB88B7N-DI, M2F2G64CB88B7N-CG, M2F4G64CB8HB5N-BE, M2F4G64CB8HB5N-DI, M2F4G64CB8HB5N-CG, M2F2G64CB88BHN-BE, M2F2G64CB88BHN-DI, M2F2G64CB88BHN-CG, M2F4G64CB8HB9N-BE, M2F4G64CB8HB9N-DI, M2F4G64CB8HB9N-CG, M2S2G64CB88B5N-BE, M2S2G64CB88B5N-CG, M2S4G64CB8HB5N-BE, M2S4G64CB8HB5N-CG, M2S1G64CBH4B5P-BE, and M2S1G64CBH4B5P-CG, are believed to contain one or more of the Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, or other similar Nanya or Nanya Elixir 50nm "B die" SDRAM products such as the Nanya Elixir N2CB2G16BP-DI, N2CB2G16BP-CG, N2CB2G16BP-BE, N2CB2G80BN-DI, N2CB2G80BN-BE, N2CB2G40BN-DI, N2CB2G40BN-CG and N2CB2G40BN-BE SDRAM semiconductor devices, which incorporate the DRAM technology disclosed and claimed in the Asserted Patents.

30. On information and belief, Nanya Elixir memory modules M2S2G64CB88D5N-CG are believed to contain one or more of the Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM, or other similar Nanya or Nanya Elixir 42nm "D die" SDRAM products, which incorporate the DRAM technology disclosed and claimed in certain of the Asserted Patents.

31. On information and belief, Nanya Elixir memory modules M2Y2G64CB8HC5N-CG are believed to contain one or more of the Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3, or other similar Nanya or Nanya Elixir 68nm "C die" SDRAM products, which incorporate the DRAM technology disclosed and claimed in certain of the Asserted Patents.

32. The identification of a specific model, trade name, or type of semiconductor device is not intended to limit the scope of this Investigation. The remedy sought in this

Complaint should extend to all infringing Nanya or Nanya Elixir DRAM prodcuts, and consumer products containing same.

V. THE ASSERTED PATENTS

A. U.S. Patent No. 6,150,689

1. Identification and Ownership of the '689 Patent

33. On November 21, 2000, the U.S. Patent and Trademark Office duly, properly and legally issued U.S. Patent No. 6,150,689, entitled "Semiconductor Integrated Circuit Device and Method for Manufacturing the Same," to inventors Seiji Narui, Tetsu Udagawa, Kazuhiko Kajigaya and Makoto Yoshida. (Exhibit No. 1.)

34. The '689 patent issued from U.S. Patent Application No. 08/782,351, filed January 13, 1997.

35. The '689 patent has 4 independent claims and 14 dependent claims. At this time, Elpida is asserting at least claims 1-6, 8-11 and 15-18 of the '689 patent in this Investigation.

36. Elpida Memory, Inc. owns by assignment the entire right, title, and interest in and to the '689 patent. Inventors Seiji Narui, Tetsu Udagawa, Kazuhiko Kajigaya and Makoto Yoshida assigned all right, title, and interest in the '689 patent to Hitachi, Ltd.; Hitachi, Ltd. assigned all right, title, and interest in the '689 patent to Elpida Memory, Inc. (Exhibit No. 8.)

37. Pursuant to Commission Rule 210.12(c), this Complaint is either accompanied by a certified copy of the U.S. Patent and Trademark Office prosecution history for the '689 patent and three copies thereof, or these documents will be submitted once they are received from the

United States Patent and Trademark Office.[1] (App. A.) This Complaint also is accompanied by four copies of each technical reference identified in the prosecution history of the '689 patent. (App. H.)

2. Nontechnical Description of the Invention Claimed in the '689 Patent

38. The '689 patent is generally directed to semiconductor integrated circuit devices, particularly dynamic random access memory (DRAM) devices. DRAMs are essentially arrays of capacitors which store electrical current (charge) and corresponding transistors which serve as switches allowing access to and from the capacitors. Each of the transistors periodically allows for the supply of electrical current to or from an associated capacitor that stores electrical charge. When a charge is stored in a capacitor the charge corresponds to "information" storage. Typically, charged capacitors represent a "1" and uncharged capacitors represent a "0" in binary computer language. The "1s" and "0s" may be read as bits and together form bytes (8 bits) which are "words" in binary language.

39. In order to read and write information to DRAMs (in terms of charges stored in or not stored in the array of capacitors in the form of "0"s and "1"s), long lines of electrically conductive "wires" must run across the memory array portion of the DRAM device in columns and rows. The conductive wires are associated with sets of charge storage capacitors and transistors (*i.e.*, "memory cell") in the array. One set of these conductive lines is called "bit

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[1] At the filing of this Complaint, Complainants had requested from the United States Patent and Trademark Office certified copies of the Asserted Patents, the recorded assignments and the file histories for those patents. Where Complainants had received certified copies of these documents when the Complaint was filed, those documents are being submitted herewith, and where they have not been received, non-certified copies have been submitted. When additional certified copies are received for these documents, Complainant will submit them to replace any non-certified copies that have been submitted.

lines." Bit lines are conductive and provide or receive electrical current to or from the charge storage capacitors via the transistors. Generally, the transistors act as switches, allowing access to and from the capacitors. The other set of long lines of electrically conductive "wires" is called "word lines." Word lines control the transistors by "turning on" or "turning off" the transitor via the gate electrodes of the transistors. Generally, when the transistor is turned on, the bit line may access the capacitor via the transistor. Conversely, when the transistor is turned off, the bit line is isolated from the capacitor because the transistor does not conduct. Thus, generally, the bit lines receive current from, or provide current to, the storage capacitors via the transistors. As explained in the '689 patent, the DRAM has a peripheral circuit area located on the periphery of the memory array portions of the DRAM. Generally, the peripheral circuit area includes other devices, such as transistors and amplifiers, which are used to control ("drive") the word lines and bit lines of the memory array. By driving the word lines and the bit lines, information is read into, or read from, the memory array in the form of "1s" and "0s".

40. As DRAMs are designed to have higher memory capacity, the number of the individual components (*e.g.*, capacitors and transistors, etc.) necessary to form memory cells in the memory array portion of the DRAM, and the number of peripheral circuits necessary to control the memory array increases. The components in these circuits must become smaller and smaller and are located closer together inside the DRAM. Accordingly, electrical interferences occur between the devices. Additionally, the number of conductors needed to control the components increases, which increases complexity and electrical resistances. According to the '689 patent, materials are chosen and the design layout of the DRAM is optimized in order to minimize electrical interferences between the closely spaced circuits, decrease electrical resistances in the circuits, and thereby allow for more circuits which yields an increase in the

memory capacity of the DRAM, an increase in performance (speed) of the DRAM and an improved yield. More specifically, as the number of transistors in the memory array increases, the electrical resistances of the word lines (conductors that are connected to and control the transistors) and the bit lines (conductors that that receive or provide current to or from the capacitors) increases. As the resistance of the word lines increases, additional amplifiers are needed in the periphery of the memory array on the DRAM to overcome losses due to resistance in the word and bit lines. If the number of sense amplifiers and word drivers increases, the DRAM size has to increase, the DRAM becomes more complex to manufacture, and the DRAM consumes more power. The '689 patent discloses novel word line structures, bit line structures and methods for manufacturing the circuits of the DRAM that minimize steps in manufacturing DRAMs, improve the speed of the circuits in the DRAM and allow for increased memory cells in the memory array.

41. This nontechnical description is intended as illustrative and exemplary only and does not interpret or limit the claims of the '689 patent.

3. Foreign Counterparts

42. The following foreign counterpart patents or applications correspond to the '689 patent. No other foreign applications or patents corresponding to the '689 patent have been filed, abandoned, or rejected.

Jurisdiction	Application No.	Publication No.	Patent No.	Status
Japan	H08-003648 (1996)	None	None	Withdrawn
Japan	H08-309369 (1996)	H09-252098	None	Abandoned
Korea	97-0000413 (1997)	(Unknown)	420250	Issued
Singapore	9700019-4 (1997)	(Unknown)	54456	Abandoned
China	97102023.X (1997)	1307721C	97102023.X	Issued
Malaysia	PI97000121 (1997)	(Unknown)	None	Abandoned
Taiwan	85115937 (1997)	(Unknown)	508757	Issued

4. Licenses

43. As required under Commission Rule 210.12(a)(9)(iii), a list of licensed entities is attached to this Complaint as Confidential Exhibit No. 27C. [redacted]

B. U.S. Patent No. 6,635,918

1. Identification and Ownership of the '918 Patent

44. On October 21, 2003, the U.S. Patent and Trademark Office duly, properly and legally issued U.S. Patent No. 6,635,918, entitled "Semiconductor Integrated Circuit Device and Method for Manufacturing the Same," to inventors Seiji Narui, Tetsu Udagawa, Kazuhiko Kajigaya and Makoto Yoshida. (Exhibit No. 2.)

45. The '918 patent issued from U.S. Patent Application No. 09/714,127, filed November 17, 2000, which was a continuation of U.S. Patent Application No. 08/782,351, filed on January 13, 1997, now U.S. Patent No. 6,150,689.

46. The '918 patent has 5 independent claims and 16 dependent claims. At this time, Elpida is asserting claims 1-16 and 18-21 of the '918 patent in this Investigation.

47. Elpida Memory, Inc. owns by assignment the entire right, title, and interest in and to the '918 patent. Inventors Seiji Narui, Tetsu Udagawa, Kazuhiko Kajigaya and Makoto Yoshida assigned all right, title, and interest in the '918 patent to Hitachi, Ltd.; Hitachi, Ltd. assigned all right, title, and interest in the '918 patent to Elpida Memory, Inc. (Exhibit No. 9.)

48. Pursuant to Commission Rule 210.12(c), this Complaint is either accompanied by a certified copy of the U.S. Patent and Trademark Office prosecution history for the '918 patent

and three copies thereof, or these documents will be submitted once they are received from the United States Patent and Trademark office. (App. B.) This Complaint is also accompanied by four copies of each technical reference identified in the prosecution history of the '918 patent. (App. I.)

2. Nontechnical Description of the Invention Claimed in the '918 Patent

49. The '918 patent is a continuation of the '689 patent and, as discussed above, is generally directed to semiconductor integrated circuit devices, particularly dynamic random access memory (DRAM) devices. DRAMs are essentially arrays of capacitors which store electrical current (charge) and corresponding transistors which serve as switches allowing access to and from the capacitors. Generally, each of the transistors periodically allows current to flow to or from an associated capacitor. When a charge is stored in a capacitor the charge corresponds to information storage, as charged capacitors may represent a "1" and uncharged capacitors may represent a "0" in binary computer language. The "1s" and "0s" may be read as bits and together form bytes (8 bits) which are "words" in binary language.

50. In order to read and write information to DRAMs (in terms of arrays of "0"s and "1"s), long lines of electrically conductive "wires" must run across the array in columns and rows and are associated with the capacitors and transistors (*i.e.*, "memory cell") in the array. One set of these lines is called"bit lines." Bit lines are conductive and provide or receive electrical current to or from the capacitors via the transistors which act as switches allowing access to and from the capacitors. The other set of long lines of electrically conductive "wires" is called "word lines." Word lines control the transistors by turning on or turning off the transitor via the gates of the transistors. Generally, the bit lines receive current from or provide current to the capacitors via the transistor.

51. As DRAMs become more complex and are designed to have higher memory capacity, the individual components (*e.g.,* capacitors and transistors, etc.) become smaller and smaller and are located closer together. Accordingly, electrical interferences occur between the devices. Materials are chosen and the design layout of the memory array is optimized in order to minimize the electrical interferences and increase performance (speed) of the transistors. As the number of transistors in the array gets larger, the electrical resistance of the word lines that control the transistors and the resistance of the bit lines that receive or provide current to or from the capacitors increases. As the resistance of the word lines increases, additional sense amplifiers and word driver amplifiers are needed in the periphery of the memory array on the DRAM to overcome losses due to resistance in the word and bit lines. If the number of sense amplifiers and word drivers increases, the chip size has to increase, the chip becomes more complex to manufacture, and the DRAM consumes more power. The '918 patent is a continuation of the '689 patent and also provides novel DRAM device designs that include transistors known as metal insulator semiconductor field effect transistors (MISFETs). The '918 patent claims capacitor-over-bit line structures (COB), wherein the capacitor is formed over the bit lines and the corresponding MISFET that is connected to and controls access to the capacitor. The MISFETs gate electrodes (word lines of the memory array) have a multi-layer design which provides a low resistance to current flow. Consequently, this allows for a decrease in the number of amplifiers in the periphery area (outside the memory array) of the DRAM and allows for an increase in the number of memory cells in the memory array portion of the DRAM. Thus, the decrease in resistance allows a relatively reduced chip size and improved degree of integration of the DRAM. Additionally, the bit lines are made from a low resistance conductor film. Further, the '918 patent discloses a DRAM design such that the bit lines are formed simultaneously with

other interconnections (conductors) in the periphery of the memory array, thereby reducing the number of steps required for manufacturing, improving yield and reducing the cost of manufacturing the DRAM.

52. This nontechnical description is intended as illustrative and exemplary only and does not interpret or limit the claims of the '918 patent.

3. Foreign Counterparts

53. The following foreign counterpart patents or applications correspond to the '918 patent. No other foreign applications or patents corresponding to the '918 patent have been filed, abandoned, or rejected.

Jurisdiction	Application No.	Publication No.	Patent No.	Status
Japan	H08-003648 (1996)	None	None	Withdrawn
Japan	H08-309369 (1996)	H09-252098	None	Abandoned
Korea	97-0000413 (1997)	(Unknown)	420250	Issued
Singapore	9700019-4 (1997)	(Unknown)	54456	Abandoned
China	97102023.X (1997)	1307721C	97102023.X	Issued
Malaysia	PI97000121 (1997)	(Unknown)	None	Abandoned
Taiwan	85115937 (1997)	(Unknown)	508757	Issued

4. Licenses

54. As required under Commission Rule 210.12(a)(9)(iii), a list of licensed entities is attached to this Complaint as Confidential Exhibit No. 27C. [redacted]

C. U.S. Patent No. 6,555,861

1. Identification and Ownership of the '861 Patent

55. On April 29, 2003, the U.S. Patent and Trademark Office duly, properly and legally issued U.S. Patent No. 6,555,861, entitled "Semiconductor Integrated Circuit Device and

Process for Manufacturing the Same," to inventors Satoru Yamada, Kiyonori Oyu, Takafumi Tokunaga, Hiroyuki Enomoto, and Toshihiro Sekiguchi. (Exhibit No. 3.)

56. The '861 patent issued from U.S. Patent Application No. 09/765,574, filed January 22, 2001.

57. The '861 patent has 5 independent claims and 20 dependent claims. At this time, Elpida is asserting claims 1, 3, 4 and 9-14 of the '861 patent in this Investigation.

58. Elpida Memory, Inc. owns by assignment the entire right, title, and interest in and to the '861 patent. Inventors Satoru Yamada, Kiyonori Oyu, Takafumi Tokunaga, Hiroyuki Enomoto, and Toshihiro Sekiguchi assigned all right, title, and interest in the '861 patent to Hitachi, Ltd. (Tokyo, JP); Hitachi, Ltd. assigned all right, title, and interest in the '861 patent to Elpida Memory, Inc. (Exhibit No. 10.)

59. Pursuant to Commission Rule 210.12(c), this Complaint is either accompanied by a certified copy of the U.S. Patent and Trademark Office prosecution history for the '861 patent and three copies thereof, or these documents will be submitted once they are received from the United States Patent and Trademark office. (App. C.) This Complaint is also accompanied by four copies of each technical reference identified in the prosecution history of the '861 patent. (App. J.)

2. Nontechnical Description of the Invention Claimed in the '861 Patent

60. The '861 patent is generally directed to semiconductor integrated circuit devices, particularly DRAM devices. Generally, DRAMs are essentially arrays of capacitors which store electrical current (charge) and corresponding transistors each of which periodically supplies

current to a capacitor. Charge stored in a capacitor corresponds to information storage in terms of bits and bytes, as charged capacitors may represent a "1" and uncharged capacitors may represent a "0" in binary computer language. In order to read and write information to DRAMs (in terms of arrays of "0"s and "1"s), long lines of electrically conductive "wires" must run across each of the capacitors/transistors (i.e., "memory cell") in the array, and provide/receive electrical current to/from the capacitors/transistors. These long lines of electrically conductive "wires" are called "word lines" and "bit lines."

61. As DRAMs become more complex and have higher memory capacity, and as individual components (transistors, etc.) become smaller and smaller, it becomes more difficult to manage electrical power consumption and the number of memory cells to which a given bit line can be connected. The '861 patent provides for a DRAM device including metal-insulator-semiconductor field-effect transistors (MISFETs), which allow for a reduction in the capacity of a bit line. Consequently, this allows for an increase in the voltage in the bit line at the time of reading charge (information) accumulated in the capacitor in a memory cell. Less current is used to operate and maintain the "memory" in the DRAM memory cells, and overall power consumption can be decreased. For example, the '861 patent discloses novel insulation structures for the transistors and the conductors in the DRAM circuits. The '861 patent discloses a novel transistor with an insulating film structure for the gate electrode (of a given memory cell transistor) arranged such that the effective dielectric constant (*i.e.*, ability of the material to resist electrical current) of the side wall insulating film can be made relatively small, which minimizes the electrical interferences between the circuits in the DRAM, which allows the DRAM to have more closely spaced circuits and, therefore, increases memory capacity of the DRAM because more memory cells can be manufactured on the chip. Additionally, the '861

patent discloses improved side wall designs for conductors formed in contact used to connect to the source and drain regions of the transistors. These novel structures decrease electrical interferences inside the DRAM circuits and allow for increased circuit integration and more memory capacity of the DRAM.

62. This nontechnical description is intended as illustrative and exemplary only and does not interpret or limit the claims of the '861 patent.

3. Foreign Counterparts

63. The following foreign counterpart patents or applications correspond to the '861 patent. No other foreign applications or patents corresponding to the '861 patent have been filed, abandoned, or rejected.

Jurisdiction	Application No.	Publication No.	Patent No.	Status
Japan	2000-13476	2001-203337 A	3645463 B2	Issued
Japan	2004-367664	2005-094044	4215711	Issued
Korea	10-2001-0003400	10-2001-0076421	10-0737200	Issued
Taiwan	090100268	508757	508757	Issued

4. Licenses

64. As required under Commission Rule 210.12(a)(9)(iii), a list of licensed entities is attached to this Complaint as Confidential Exhibit No. 27C. There are no other current licenses involving the '861 patent. [redacted]

D. U.S. Patent No. 7,659,571

1. Identification and Ownership of the '571 Patent

65. On February 9, 2010, the U.S. Patent and Trademark Office duly, properly and legally issued U.S. Patent No. 7,659,571, entitled "Semiconductor Device and Method for Manufacturing the Same," to inventor Yasushi Yamazaki. (Exhibit No. 4.)

66. The '571 patent issued from U.S. Patent Application No. 11/445,236, filed June 2, 2006.

67. The '571 patent has 2 independent claims and 6 dependent claims. At this time, Elpida is asserting at least claims 1, 3 and 4 of the '571 patent in this Investigation.

68. Elpida Memory, Inc. owns by assignment the entire right, title, and interest in and to the '571 patent. Inventor Yasushi Yamazaki assigned all right, title, and interest in the '571 patent to Elpida Memory, Inc. (Exhibit No. 11.)

69. Pursuant to Commission Rule 210.12(c), this Complaint is either accompanied by a certified copy of the U.S. Patent and Trademark Office prosecution history for the '571 patent and three copies thereof, or these documents will be submitted once they are received from the United States Patent and Trademark Office. (App. D.) This Complaint is also accompanied by four copies of each technical reference identified in the prosecution history of the '571 patent. (App. K.)

2. Nontechnical Description of the Invention Claimed in the '571 Patent

70. The '571 patent is generally directed to semiconductor integrated circuit devices, particularly dynamic random access memory (DRAM) devices. DRAMs are essentially arrays

of transistors and capacitors used for storing electrical current (charge). Each of the transistors periodically allows for the supply of current to or from an associated capacitor. When a charge is stored in a capacitor the charge corresponds to information storage, as charged capacitors may represent a "1" and uncharged capacitors may represent a "0" in binary computer language. The "1s" and "0s" may be read as bits and together form bytes (8 bits) which are "words" in binary language.

71. The '571 patent discloses novel "trench-gate" type transistors used in the DRAM circuits. DRAMs use transistors to access the storage capacitors in the memory array of the DRAM. As DRAMs become more and more integrated, the channel length (gate length) of the transistors (generally, the distance between the source and the drain regions of the transistor) becomes shorter and shorter. However, as channel lengths of the transistors become shorter, problems known as "short channel effects" occur due to electrical limitations of the materials used to create the transistor and electrical fields caused by the close proximity of the devices in the memory array. The '571 patent discloses a transistor design that utilizes a novel trench-gate, which maintains a short channel length beneath the gate electrode, but increases the "effective length" of the channel length. The '571 patent's trench-gate transistor design is free from electrical breakdown resistance defects between the gate electrode and the source and drain regions of the semiconductor substrrate. By using a trench-gate type gate, and Lightly Dosed Drain (LDD) regions as part of the source and drain regions of the transistor, the '571 transistor has decreased leakage current and electrical breakdown. Improved transistors as disclosed in the '571 patent allow for smaller memory cells and increased memory capacity of the DRAM.

72. This nontechnical description is intended as illustrative and exemplary only and does not interpret or limit the claims of the '571 patent.

3. Foreign Counterparts

73. The following foreign counterpart patents or applications correspond to the '571 patent. No other foreign applications or patents corresponding to the '571 patent have been filed, abandoned, or rejected.

Jurisdiction	Application No.	Publication No.	Patent No.	Status
Japan	2005-163575 (2005)	2006-339476	None	Abandoned
China	200610093015.2 (2006)	1874003A	200610093015.2	Issued
Taiwan	95119540 (2006)	(Unknown)	324386	Issued

4. Licenses

74. As required under Commission Rule 210.12(a)(9)(iii), a list of licensed entities is attached to this Complaint as Confidential Exhibit No. 27C.

E. U.S. Patent No. 7,713,828

1. Identification and Ownership of the '828 Patent

75. On May 11, 2010, the U.S. Patent and Trademark Office duly, properly and legally issued U.S. Patent No. 7,713,828, entitled "Semiconductor Device and Method of Forming the Same," to inventor Kazuyoshi Yuki. (Exhibit No. 5.)

76. The '828 patent issued from U.S. Patent Application No. 11/940,831, filed November 15, 2007.

77. The '828 patent has 1 independent claim and 6 dependent claims. At this time, Elpida is asserting at least claims 1, 5 and 6 of the '828 patent in this Investigation.

78. Elpida Memory, Inc. owns by assignment the entire right, title, and interest in and to the '828 patent. Inventor Kazuyoshi Yuki assigned all right, title, and interest in the '828 patent to Elpida Memory, Inc. (Exhibit No. 12.)

79. Pursuant to Commission Rule 210.12(c), this Complaint is either accompanied by a certified copy of the U.S. Patent and Trademark Office prosecution history for the '828 patent and three copies thereof, or these documents will be submitted once they are received from the United States Patent and Trademark Office. (App. E.) This Complaint is also accompanied by four copies of each technical reference identified in the prosecution history of the '828 patent. (App. L.)

2. Nontechnical Description of the Invention Claimed in the '828 Patent

80. The '828 patent is generally directed to semiconductor integrated circuit devices, particularly dynamic random access memory (DRAM) devices. DRAMs are essentially arrays of memory cells that use capacitors to store electrical current (charge) and corresponding transistors which serve as switches allowing access to and from the capacitors. DRAMs also have peripheral circuits used to access the memory array of the DRAM. DRAMs use metal-oxide-semiconductor (MOS) field-effect transistors in the memory array and in the peripheral circuits. As DRAMs get smaller and smaller, the memory array and the peripheral circuits require more integration including MOS transistors in closer and closer proximity to each other.

81. The '828 patent discloses novel methods of manufacturing transistors used in DRAMs. DRAMs use transistors to access the storage capacitors in the memory array of the DRAM. DRAMs also use transistors in the peripheral circuits of the DRAM. As DRAMs become more and more minatureized, the channel length (gate length) of the transistors (generally, the distance between the source and the drain of the transistor) becomes shorter and shorter. However, as channel lengths of the transistors become shorter, problems known as "short channel effects" occur due to electrical limitations of the materials and electrical fields caused by the close proximity of the devices in the memory array. One way of preventing "short

channel" effects is to use epitaxial silcon layers as the source and drain regions of the transistors. The '828 patent discloses a method of forming a transistor that has epitaxial silicon layers formed at the source and drain regions stacked on diffusion layers. Contact plugs formed as epitaxial layers are connected to the source and drain regions and impurities are introduced into the source and drain regions via the plugs with ion implantation. By using the epitaxial layer of the contact plug to control diffusion into the source and drain regions as described in the '828 patent, short channel effects (electrical interferences) are reduced and improved transistor performances for the DRAM circuits are realized. This allows for faster operating speeds, improved manufacturing proceses and more memory capacity for the DRAM design. Further, as disclosed in the '828 patent, by using the methods of forming a MOS tranistor as disclosed in the '828 patent, the contact resistances between the contact plugs and the bit lines are reduced which yields a DRAM with lower power consumption.

82. This nontechnical description is intended as illustrative and exemplary only and does not interpret or limit the claims of the '828 patent.

3. Foreign Counterparts

83. The following foreign counterpart patents or applications correspond to the '828 patent. No other foreign applications or patents corresponding to the '828 patent have been filed, abandoned, or rejected.

Jurisdiction	Application No.	Publication No.	Patent No.	Status
Japan	2006-313179 (2006)	2008-130756	4552926	Issued

4. Licenses

84. As required under Commission Rule 210.12(a)(9)(iii), a list of licensed entities is attached to this Complaint as Confidential Exhibit No. 27C.

F. U.S. Patent No. 7,495,453

1. Identification and Ownership of the '453 Patent

85. On February 24, 2009, the U.S. Patent and Trademark Office duly, properly and legally issued U.S. Patent No. 7,495,453, entitled "Output Circuit for Semiconductor Device, Semiconductor Device Having Output Circuit, and Method of Adjusting Characteristics of Output Circuit," to inventor Hiroki Fujisawa. (Exhibit No. 6.)

86. The '453 patent issued from U.S. Patent Application No. 11/783,787, filed April 12, 2007, which is a division of U.S. Patent Application No. 11/327,425, filed on January 9, 2006, now U.S. Patent No. 7,215,128.

87. The '453 patent has 3 independent claim and 32 dependent claims. At this time, Elpida is asserting at least claims 1, 15 and 27 of the '453 patent in this Investigation.

88. Elpida Memory, Inc. owns by assignment the entire right, title, and interest in and to the '453 patent. Inventor Hiroki Fujisawa assigned all right, title, and interest in the '453 patent to Elpida Memory, Inc. (Exhibit No. 13.)

89. Pursuant to Commission Rule 210.12(c), this Complaint is either accompanied by a certified copy of the U.S. Patent and Trademark Office prosecution history for the '453 patent and three copies thereof, or these documents will be submitted once they are received from the United States Patent and Trademark Office. (App. F.) This Complaint is also accompanied by

four copies of each technical reference identified in the prosecution history of the '809 patent. (App. M.)

2. Nontechnical Description of the Invention Claimed in the '453 Patent

90. The '453 patent discloses output circuitry used on DRAMs for dynamically adjusting the output impedance of the DRAM using a number of buffer circuits. DRAMs must transfer data at very high data rates. High data rates require increasingly smaller signals into and out of the DRAM, which requires precise impedances for the output buffer of the DRAM. Impedances of the DRAM can vary due to process conditions during manufacture. Therefore, the output impedance of the DRAM must be calibrated during data out. Additionally, when plural DRAMs are connected in parallel, there is sometimes signal reflection when the impedances are not matched. This requires a procedure known as ODT (On Die Termination) function to prevent signal reflection. Depending on whether the DRAM is in ODT operation or data output time, the DRAM must dynamically adjust the output impedance. These adjustments requires increased circuitry in the DRAM, which is not optimal for decreasing the size and manufacturing costs of the DRAM. The '453 patent discloses an output buffer design that uses plural unit buffers with same circuit structures that are engaged as necessary depending on the operation of the DRAM. By using the same circuit structures connected in parallel, the DRAM disclosed in the '453 patent can adjust the impedance at data output time and/or ODT time more quickly and with a smaller size circuit on the DRAM. This allows for better data rate transfer to and from the DRAM, but minimizes the complexity of the DRAM circuit design which minimizes manufacturing costs and increases space available on the DRAM for memory capacity.

3. Foreign Counterparts

91. The following foreign counterpart patents or applications correspond to the '453 patent. No other foreign applications or patents corresponding to the '453 patent have been filed, abandoned, or rejected.

Jurisdiction	Application No.	Publication No.	Patent No.	Status
Japan	2005-011272	2006-203405	4159553	issued
Japan	2008-104237	2008-228332	4618602	issued
China	200610003624.4	CN1808902A	ZL200610003624.4	issued

4. Licenses

92. As required under Commission Rule 210.12(a)(9)(iii), a list of licensed entities is attached to this Complaint as Confidential Exhibit No. 27C.

G. U.S. Patent No. 7,906,809

1. Identification and Ownership of the '809 Patent

93. On March 15, 2011, the U.S. Patent and Trademark Office duly, properly and legally issued U.S. Patent No. 7,906,809, entitled "Semiconductor Device Having an Elevated Source/Drain Structure of Varying Cross-Section," to inventor Fumiki Aiso. (Exhibit No. 7.)

94. The '809 patent issued from U.S. Patent Application No. 12/272,036, filed November 17, 2008, which is a division of U.S. Patent Application No. 11/410,118, filed on April 25, 2006, now U.S. Patent No. 7,482,235.

95. The '809 patent has 1 independent claim and 2 dependent claims. At this time, Elpida is asserting at least claims 1 and 2 of the '809 patent in this Investigation.

96. Elpida Memory, Inc. owns by assignment the entire right, title, and interest in and to the '809 patent. Inventor Fumiki Aiso assigned all right, title, and interest in the '809 patent to Elpida Memory, Inc. (Exhibit No. 14.)

97. Pursuant to Commission Rule 210.12(c), this Complaint is either accompanied by a certified copy of the U.S. Patent and Trademark Office prosecution history for the '809 patent and three copies thereof, or these documents will be submitted once they are received from the United States Patent and Trademark Office. (App. G.) This Complaint is also accompanied by four copies of each technical reference identified in the prosecution history of the '809 patent. (App. N.)

2. Nontechnical Description of the Invention Claimed in the '809 Patent

98. The '809 patent discloses novel transistor structures used in the DRAM circuits. DRAMs use transistors in a number of ways in the DRAM circuits. They are used in the memory array of the DRAM to control access to the capacitors that hold charges as a "1" or a "0", which represents the information that is stored in the memory array. Transistors are also used in the periphery circuits of the DRAM that control access to and from the DRAM memory array and control data exchange to and from the DRAM. As DRAMs become more and more integrated, to increase memory capacity, the transistors on the DRAM become closer together. This causes electrical interferences between the transistors as electrical fields interact between the transistors when they are spaced close together. The '809 patent discloses a novel transistor structure that has "elevated" source and drain regions (parts of the transistors) that are shielded from electrical interferences from neighboring transistors. The '809 patent's novel transistor design allows for the creation of "elevated" source and drains on the transistors, but minimizes the defects that can occur when creating transistors with "elevated" source and drains. The

transistor devices disclosed in the '809 patent increase DRAM memory yield, decrease unstable performance and circuit failures that can occur in DRAM circuits due to faulty connections to the transistors.

3. Foreign Counterparts

99. The following foreign counterpart patents or applications correspond to the '809 patent. No other foreign applications or patents corresponding to the '809 patent have been filed, abandoned, or rejected.

Jurisdiction	Application No.	Publication No.	Patent No.	Status
Japan	2005-125921 (2005)	2006-303336	4274566	Issued
Korea	06-0037054 (2006)	(Unknown)	745929	Issued
China	200610075163.1 (2006)	1855492A	200610075163.1	Issued
Taiwan	95114687 (2006)	(Unknown)	298540	Issued

4. Licenses

100. As required under Commission Rule 210.12(a)(9)(iii), a list of licensed entities is attached to this Complaint as Confidential Exhibit No. 27C.

VI. UNLAWFUL AND UNFAIR ACTS OF RESPONDENT—PATENT INFRINGEMENT

101. Respondents have engaged in unfair trade practices, including the sale for importation into the United States, importation into the United States, and/or sale in the United States after importation of certain Nanya and/or Nanya Elixir 42nm "D die", 50nm "B die" and 68nm "D die" DRAM semiconductor chips and products containing same that infringe one or more of the Asserted Claims of the Asserted Patents. On information and belief, Respondents directly infringe one or more of the Asserted Claims of the Asserted Patents by selling for importation into the United States, importing, and/or selling after importation in the United States the Accused Products. On information and belief, Respondents indirectly infringe one or

more of the Asserted Claims of the Asserted Patents by contributing to and/or inducing the infringement of these patents by providing Accused Products that are not a staple article of commerce suitable for substantial non-infringing use and/or encouraging and facilitating others to perform actions known by Respondents to infringe, with the intent that performance of the actions will infringe. Complainants have conducted several meetings with Respondents in which they discussed Respondents' infringement, including most recently a meeting on October 28, 2011, in which Elpida presented infringement claims concerning the '689, '861, '571 and '828 patents, but upon information and belief, Respondents have continued to infringe one or more of the Asserted Claims of the Asserted Patents.

1. Infringement of the '689 Patent

102. On information and belief, Respondents directly and indirectly infringe at least claims 1-6, 8-11 and 15-18 of the '689 patent. Charts that apply representative independent claims 1, 8, 15 and 17 of the '689 patent to representative Nanya Accused Products are attached to this Complaint as Exhibit Nos. 17(A)(1-4), 17(B), and 17(C).

103. On information and belief, Respondents directly infringe at least claims 1-6, 8-11 and 15-18 of the '689 patent through at least their sales for importation into the United States, importation into the United States, and/or sales after importation in the United States of one or more Accused Products, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and at least claims 1, 2, 6, 15 and 16 of the '689 patent through their sales for importation into the United States, importation into the United States, and/or sales after importation in the United States of at least the M2Y2G64CB8HC5N-CG, which contains the accused Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3, and the Nanya Elixir

memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM.

104. On information and belief, Respondents contribute to the infringement of at least claims 1-6, 8-11, and 15-18 of the '689 patent.

105. On information and belief, third party product developers and manufacturers use Accused Products, either the accused Nanya DRAM products or modules containing same, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, the M2Y2G64CB8HC5N-CG, which contains the accused Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3, and the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM, in their products, thereby directly infringing one or more of claims 1-6, 8-11 and 15-18 of the '689 patent.

106. On information and belief, Respondents induce others to infringe at least one or more of claims 1-6, 8-11 and 15-18 of the '689 patent by encouraging and facilitating others to perform actions known by Respondents to infringe, and do so with the intent that performance of the actions will infringe.

107. On information and belief, Respondents encourage third party developers and manufacturers to use the claimed inventions in their products by marketing, providing instructions for, and supporting the use of Accused Products, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, the

M2Y2G64CB8HC5N-CG, which contains the accused Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3, and the accused Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM.

108. On information and belief, third party product developers and manufacturers use Accused Products, either the accused Nanya DRAM products or modules containing same, including Nanya Elixir M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the infringing Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, the Nanya Elixir M2Y2G64CB8HC5N-CG, which contains the accused Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3, and the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM, in their products, thereby directly infringing one or more of at least claims 1-6, 8-11 and 15-18 of the '689 patent.

2. Infringement of the '918 Patent

109. On information and belief, Respondents directly and indirectly infringe at least claims 1-16 and 18-21 of the '918 patent. Charts that apply representative independent claims 1, 6, 11, 16 and 19 of the '918 patent to representative Respondents' Accused Products are attached to this Complaint as Exhibit Nos. 18(1-5).

110. On information and belief, Respondents directly infringe one or more of at least claims 1-16 and 18-21 of the '918 patent through at least their sales for importation into the United States, importation into the United States, and/or sales after importation in the United States of one or more Accused Products, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused

Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and at least claims 1, 2, 3, 4 and 5 of the '918 patent through their sales for importation into the United States, importation into the United States, and/or sales after importation in the United States of at least the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM.

111. On information and belief, Respondents contribute to the infringement of at least claims 1-16 and 18-21 of the '918 patent.

112. On information and belief, third party product developers and manufacturers use Accused Products, either the accused Nanya DRAM products or modules containing same, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM, in their products, thereby directly infringing one or more of at least claims 1-16 and 18-21 of the '918 patent.

113. On information and belief, Respondents induce others to infringe one or more of at least claims 1-16 and 18-21 of the '918 patent by encouraging and facilitating others to perform actions known by Respondents to infringe, and do so with the intent that performance of the actions will infringe.

114. On information and belief, Respondents encourage third party developers and manufacturers to use the claimed inventions in their products by marketing, providing instructions for, and supporting the use of Accused Products, including the Nanya Elixir memory

modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM.

115. On information and belief, third party product developers and manufacturers use Accused Products, either the accused Nanya DRAM products or modules containing same, including Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM, in their products, thereby directly infringing one or more of at least claims 1-16 and 18-21 of the '918 patent.

3. Infringement of the '861 Patent

116. On information and belief, Respondents directly and indirectly infringe at least claims 1, 4 and 9-14 of the '861 patent. Charts that apply representative independent claims 1 and 9 of the '861 patent to representative Accused Products are attached to this Complaint as Exhibit Nos. 19(1-2).

117. On information and belief, Respondents directly infringe one or more of at least claims 1, 3, 4 and 9-14 of the '861 patent through at least its sales for importation into the United States, importation into the United States, and/or sales after importation in the United States of one or more Accused Products, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and at least the Nanya Elixir

memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM.

118. On information and belief, Respondents contribute to the infringement of one or more of at least claims 1, 3, 4 and 9-14 of the '861 patent.

119. On information and belief, third party product developers and manufacturers use Accused Products, either the accused Nanya DRAM products or modules containing same, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and the accused Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM, in their products, thereby directly infringing one or more of at least claims 1, 4 and 9-14 of the '861 patent.

120. On information and belief, Respondents induce others to infringe one or more of at least claims 1, 3, 4 and 9-14 of the '861 patent by encouraging and facilitating others to perform actions known by Respondents to infringe, and do so with the intent that performance of the actions will infringe.

121. On information and belief, Respondents encourage third party developers and manufacturers to use the claimed inventions in their products by marketing, providing instructions for, and supporting the use of Accused Products, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and the Nanya Elixir

memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM.

122. On information and belief, third party product developers and manufacturers use Accused Products, either the accused Nanya DRAM products or modules containing same, including Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM, in their products, thereby directly infringing one or more of at least claims 1, 3, 4 and 9-14 of the '861 patent.

4. Infringement of the '571 Patent

123. On information and belief, Respondents directly and indirectly infringe at least claims 1, 3 and 4 of the '571 patent. A chart that applies representative independent claim 1 of the '571 patent to representative Accused Products are attached to this Complaint as Exhibit No. 20.

124. On information and belief, Respondents directly infringe at least claims 1, 3 and 4 of the '571 patent through at least their sales for importation into the United States, importation into the United States, and/or sales after importation in the United States of one or more Accused Products, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and the M2Y2G64CB8HC5N-CG, which contains the accused Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3, and M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM.

125. On information and belief, Nanya contributes to the infringement of at least claims 1, 3 and 4 of the '571 patent.

126. On information and belief, third party product developers and manufacturers use Accused Products, either the accused Nanya DRAM products or modules containing same, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and the M2Y2G64CB8HC5N-CG, which contains the accused Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3, and the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM, in their products, thereby directly infringing claims 1, 3 and 4 of the '571 patent.

127. On information and belief, Nanya induces others to infringe at least claims 1, 3 and 4 of the '571 patent by encouraging and facilitating others to perform actions known by Nanya to infringe, and does so with the intent that performance of the actions will infringe.

128. On information and belief, Nanya encourages third party developers and manufacturers to use the claimed inventions in their products by marketing, providing instructions for, and supporting the use of Accused Products, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and the M2Y2G64CB8HC5N-CG, which contains the accused Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3, and the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM.

129. On information and belief, third party product developers and manufacturers use Accused Products, either the accused Nanya DRAM products or modules containing same, including M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and the M2Y2G64CB8HC5N-CG, which contains the accused Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3, and the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM, in their products, thereby directly infringing at least claims 1, 3 and 4 of the '571 patent.

5. Infringement of the '828 Patent

130. On information and belief, Respondents directly and indirectly infringe at least claims 1, 5 and 6 of the '828 patent. A chart that applies representative independent claim 1 of the '828 patent to representative Accused Products are attached to this Complaint as Exhibit No. 21.

131. On information and belief, Respondents directly infringe at least claims 1, 5 and 6 of the '828 patent through at least their sales for importation into the United States, importation into the United States, and/or sales after importation in the United States of one or more Accused Products, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, the M2Y2G64CB8HC5N-CG, which contains the accused Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3, and the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM.

132. On information and belief, Respondents contribute to the infringement of at least claims 1, 5 and 6 of the '828 patent.

133. On information and belief, third party product developers and manufacturers use Accused Products, either the accused Nanya DRAM products or modules containing same, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and the M2Y2G64CB8HC5N-CG, which contains the accused Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3, and the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM, in their products, thereby directly infringing claims 1, 5 and 6 of the '828 patent.

134. On information and belief, Respondents induce others to infringe at least claims 1, 5 and 6 of the '828 patent by encouraging and facilitating others to perform actions known by Nanya to infringe, and does so with the intent that performance of the actions will infringe.

135. On information and belief, Respondents encourage third party developers and manufacturers to use the claimed inventions in their products by marketing, providing instructions for, and supporting the use of Accused Products, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and the M2Y2G64CB8HC5N-CG, which contains the accused Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3, and the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM.

136. On information and belief, third party product developers and manufacturers use Accused Products, either the accused Nanya DRAM products or modules containing same, including M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and the M2Y2G64CB8HC5N-CG, which contains the accused Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3, and the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM, in their products, thereby directly infringing at least claims 1, 5 and 6 of the '828 patent.

6. Infringement of the '453 Patent

137. On information and belief, Respondents directly and indirectly infringe at least claims 1, 15 and 27 of the '453 patent. Charts that apply representative independent claims 1, 15 and 27 of the '453 patent to representative Accused Products are attached to this Complaint as Exhibit Nos. 22(1-3).

138. On information and belief, Respondents directly infringe at least claims 1, 15 and 27 of the '453 patent through at least their sales for importation into the United States, importation into the United States, and/or sales after importation in the United States of one or more Accused Products, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and at least the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM.

139. On information and belief, Respondents contribute to the infringement of at least claims 1, 15 and 27 of the '453 patent.

140. On information and belief, third party product developers and manufacturers use Accused Products, either the accused Nanya DRAM products or modules containing same, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and at least the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM, in their products, thereby directly infringing claims 1, 15 and 27 of the '453 patent.

141. On information and belief, Respondents induce others to infringe at least claims 1, 15 and 27 of the '453 patent by encouraging and facilitating others to perform actions known by Respondents to infringe, and do so with the intent that performance of the actions will infringe.

142. On information and belief, Respondents encourage third party developers and manufacturers to use the claimed inventions in their products by marketing, providing instructions for, and supporting the use of Accused Products, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and at least the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM.

143. On information and belief, third party product developers and manufacturers use Accused Products, either the accused Nanya DRAM products or modules containing same,

including M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and at least the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM, in their products, thereby directly infringing at least claims 1, 15 and 27 of the '453 patent.

7. Infringement of the '809 Patent

144. On information and belief, Respondents directly and indirectly infringe at least claims 1 and 2 of the '809 patent. A chart that applies representative independent claim 1 of the '809 patent to representative Accused Products is attached to this Complaint as Exhibit No. 23.

145. On information and belief, Respondents directly infringe one or more of at least claims 1 and 2 of the '809 patent through at least its sales for importation into the United States, importation into the United States, and/or sales after importation in the United States of one or more Accused Products, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and at least the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM.

146. On information and belief, Respondents contribute to the infringement of one or more of at least claims 1 and 2 of the '809 patent.

147. On information and belief, third party product developers and manufacturers use Accused Products, either the accused Nanya DRAM products or modules containing same, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and

M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and the accused Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM, in their products, thereby directly infringing one or more of at least claims 1 and 2 of the '809 patent.

148. On information and belief, Respondents induce others to infringe one or more of at least claims 1 and 2 of the '809 patent by encouraging and facilitating others to perform actions known by Respondents to infringe, and do so with the intent that performance of the actions will infringe.

149. On information and belief, Respondents encourage third party developers and manufacturers to use the claimed inventions in their products by marketing, providing instructions for, and supporting the use of Accused Products, including the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM.

150. On information and belief, third party product developers and manufacturers use Accused Products, either the accused Nanya DRAM products or modules containing same, including Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM, and the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the

accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM, in their products, thereby directly infringing one or more of at least claims 1 and 2 of the '809 patent.

VII. SPECIFIC INSTANCES OF UNFAIR IMPORTATION AND SALE

151. From at least September to October 2011, samples of certain of the Accused Products were sold and/or offered for sale in the United States.

152. On or about November 12, 2010, the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM chips were purchased in the United States. Exhibit No. 24(A) includes a copy of the purchase order, shipping information, billing information and a photograph of the chip, which includes the designation "TW." On information and belief, this signifies that the chip was fabricated in Taiwan.

153. On or about October 17, 2011, the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM chips, as incorporated in Nanya Elixir memory modules M2F4G64CB8HB5N-CG, were purchased in the United States. Exhibit No. 24(B) includes a copy of the website order page, the purchase receipt and a photograph of the chip, which includes the designation "TW." On information and belief, this signifies that the chip was fabricated in Taiwan.

154. On or about September 7, 2011, the accused Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM chips, as incorporated in Nanya Elixir memory module M2F2G64CB88B7N-CG, were offered for sale in the United States. Exhibit No. 24(C) includes copies of several sources offering the memory modules for sale and a photograph of the chip, which includes the designation "TW." On information and belief, this signifies that the chip was fabricated in Taiwan.

155. On or about September 8, 2011, Nanya Elixir memory modules M2Y2G64CB8HC5N-CG, containing the accused Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3 SDRAM, were purchased from two different locations in the United States. Exhibit No. 25 includes a copies of multiple website ordering pages, an invoice for the memory module and a photograph of the chip, which includes the designation "TW." On information and belief, this signifies that the chip was fabricated in Taiwan.

156. On or about September 19, 2011, Nanya Elixir memory modules M2S2G64CB88D5N-CG, containing the accused Nanya Elixir N2CB2G80DN-CG 42nm 2Gbits DDR3 SDRAM, were purchased in the United States. Exhibit 26 includes copies of a purchase order, shipping label, and invoice for the memory modules, as well as a photograph of the chip, which includes the designation "TW." On information and belief, this signifies that the chip was fabricated in Taiwan.

VIII. HARMONIZED TARIFF SCHEDULE ITEM NUMBERS

157. On information and belief, the Harmonized Tariff Schedule ("HTS") of the United States item numbers under which the infringing semiconductor chips having DRAM circuitry have been imported into the United States include at least the following HTS numbers: 8542.32.00 (Electronic integrated circuits: Memories) and 8542.31.00 (Electronic integrated circuits: Processors and controllers).

IX. RELATED LITIGATION

158. In *Elpida Memory, Inc. v. Infineon Technologies AG, et al.*, Case No. 2:10-cv-152 (E.D. Va., filed April 2, 2010), Elpida reached a confidential settlement with Infineon Technologies AG and Infineon Technologies North America Corp. (collectively, "Infineon")

shortly after the Complaint was filed. There, Elpida asserted one of the patents asserted here, the '861 patent. Prior to any substantive activity in the case, Elpida and Infineon entered into a cross-license agreement.

159. A civil action in the United States District Court for the Northern District of California asserting infringement by Nanya of a number of Elpida patents is currently pending. The case name and docket number of that case are: *Elpida Memory, Inc. v. Nanya Technology Corporation, Nanya Technology Corporation U.S.A. and Nanya Technology Corporation Delaware*, CV11-04411 (MEJ) (N.D. Ca. filed Sept. 6, 2011). Prior to service, the Complaint in that action is being amended to include each of the Asserted Patents herein, and this newly amended Complaint has not been served on Respondents, and, of course, no answer has been filed.

160. There have been no other litigations involving the Asserted Patents.

X. DOMESTIC INDUSTRY

161. An industry in the United States, relating to the semiconductor devices protected by the Asserted Patents, exists under 19 U.S.C. § 1337(a)(2) and § 1337(a)(3)(A)-(C), comprising significant investments in plant and equipment, and employment of labor and capital.

A. Elpida's Investments in the Domestic Industry

[redacted]

[redacted]

[redacted]

166. [redacted]

[redacted]

167. An exemplary claim chart comparing an Elpida Domestic Industry Product to a representative claim of the '689 patent is attached as Confidential Exhibit No. 29C.

168. An exemplary claim chart comparing an Elpida Domestic Industry Product to a representative claim of the '918 patent is attached as Confidential Exhibit No. 30C.

169. An exemplary claim chart comparing an Elpida Domestic Industry Product to a representative claim of the '861 patent is attached as Confidential Exhibit No. 31C.

170. An exemplary claim chart comparing an Elpida Domestic Industry Product to a representative claim of the '571 patent is attached as Confidential Exhibit No. 32C.

171. An exemplary claim chart comparing an Elpida Domestic Industry Product to a representative claim of the '828 patent is attached as Confidential Exhibit No. 33C.

172. An exemplary claim chart comparing an Elpida Domestic Industry Product to a representative claim of the '453 patent is attached as Confidential Exhibit No. 34C.

173. An exemplary claim chart comparing an Elpida Domestic Industry Product to a representative claim of the '809 patent is attached as Confidential Exhibit No. 35C.

XI. RELIEF REQUESTED

WHEREFORE, by reason of the foregoing, Elpida requests that the United States International Trade Commission:

a. Institute an immediate investigation pursuant to Section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337(a)(1)(B)(i) and (b)(1), with respect to violations of Section 337 by Respondents Nanya Taiwan and Nanya USA and based upon their sale for importation, importation, and/or sale after importation into the United States of certain semiconductor chips with DRAM circuitry, and products containing same, that infringe one or more of the Asserted Claims of Elpida's United States Patent Nos. 6,150,689; 6,635,918; 6,555,861; 7,659,571; 7,713,828, 7,495,453 and 7,906,809.

b. Schedule and conduct a hearing on said unlawful acts and, following said hearing;

c. Issue a permanent, limited exclusion order pursuant to 19 U.S.C. § 1337(d)(1), barring from entry into the United States all Accused Products that infringe one or more of the Asserted Claims of Elpida's United States Patent Nos. 6,150,689; 6,635,918; 6,555,861; 7,659,571; 7,713,828, 7,495,453 and 7,906,809, including but not limited to (1) the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the Nanya Elixir N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM; (2) all similarly structured infringing "B die" Nanya or Nanya Elixir DRAM products and modules containing same including all memory size configurations; (3) the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM; (4) all similarly structured infringing "D die" Nanya or Nanya Elixir DRAM

products and modules containing same including all memory size configurations; (5) the Nanya Elixir memory module M2Y2G64CB8HC5N-CG, which contains the Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3; (6) all similarly structured infringing "C die" Nanya or Nanya Elixir DRAM products and modules containing same including all memory size configurations; (7) the Nanya Elixir N2CB2G16BP-DI, N2CB2G16BP-CG, N2CB2G16BP-BE, N2CB2G80BN-DI, N2CB2G80BN-BE, N2CB2G40BN-DI, N2CB2G40BN-CG and N2CB2G40BN-BE SDRAM 50nm DRAM products and other similary structured Nanya or Nanya Elixir "B die" DRAM devices manufactured by Nanya and products containing same; (8) the Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM and other similarly structured infringing Nanya or Nanya Elixir "D die" DRAM devices manufactured by Nanya and products containing same; and (9) the Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3 and other similarly structured infringing "C die" DRAM devices manufactured by Nanya and products containing same, that are sold for importation into the United States, imported, or sold after importation by or on behalf of Nanya.

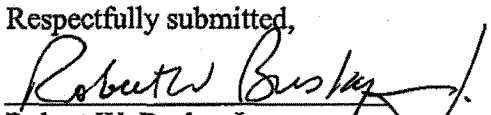
d. Issue permanent cease and desist orders, pursuant to 19 U.S.C. § 1337(f), directing Respondents to cease and desist from selling for importation into the United States, importing, selling after importation into the United States, using, offering for sale, marketing, advertising, demonstrating, sampling, warehousing inventory for distribution, offering for sale, selling, distributing, licensing, testing, providing technical support, or other related commercial activity, involving imported Accused Products that infringe one or more of the Asserted Claims of Elpida's United States Patent Nos. 6,150,689; 6,635,918; 6,555,861; 7,659,571; 7,713,828, 7,495,453 and 7,906,809, including but not limited (1) the Nanya Elixir memory modules M2F2G64CB88B7N-CG and M2F4G64CB8HB5N-CG, each of which contain the Nanya Elixir

N2CB2G80BN-CG 50nm 2Gbit DDR3 SDRAM; (2) all similarly structured infringing "B die" Nanya or Nanya Elixir DRAM products and modules containing same; (3) the Nanya Elixir memory module M2S2G64CB88D5N-CG, which contains the Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM; (4) all similarly structured infringing "D die" Nanya or Nanya Elixir DRAM products and modules containing same; (5) the Nanya Elixir memory module M2Y2G64CB8HC5N-CG, which contains the Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3; (6) all similarly structured infringing "C die" Nanya or Nanya Elixir DRAM products and modules containing same; (7) the Nanya Elixir N2CB2G16BP-DI, N2CB2G16BP-CG, N2CB2G16BP-BE, N2CB2G80BN-DI, N2CB2G80BN-BE, N2CB2G40BN-DI, N2CB2G40BN-CG and N2CB2G40BN-BE SDRAM 50nm DRAM products and other similary structured Nanya or Nanya Elixir "B die" DRAM devices manufactured by Nanya, including all memory size configurations; (8) the Nanya Elixir N2CB2G80DN-CG 42nm 2Gbit DDR3 SDRAM and other similarly structured infringing Nanya or Nanya Elixir "D die" DRAM devices manufactured by Nanya incldluing all memory size configurations; and (9) the Nanya Elixir N2CB1G80CN-CG 68nm 1GBits DDR3 and other similarly structured infringing "C die" DRAM devices manufactured by Nanya including all memory size configurations.

e. Grant such other and further relief as the Commission deems just and proper based on the facts determined by the investigation and the authority of the Commission.

Dated: November 15, 2011

Respectfully submitted,



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VERIFICATION OF COMPLAINT

I, Teruki Sasaki, declare, in accordance with 19 C.F.R. §§ 210.4 and 210.12(a), under penalty of perjury, that the following statements are true:

1. My title is Professional and I am a member of the Intellectual Property Group, of Complainant Elpida Memory, Inc., and am duly authorized to sign this Complaint on behalf of both Complainants Elpida Memory, Inc. and Elpida Memory (USA) Inc.;

2. I have read the foregoing Complaint;

3. To the best of my knowledge, information and belief, based on reasonable inquiry, the foregoing Complaint is well-grounded in fact and is warranted by existing law or by a good-faith argument for the extension, modification, or reversal of existing law, or establishment of new law;

4. The allegations and other factual contentions have evidentiary support or are likely to have evidentiary support after a reasonable opportunity for further investigation or discovery; and

5. The foregoing Complaint is not being filed for any improper purpose.

Executed November 15, 2011 in Sagamihara, Kanagawa, Japan

佐々木輝記

Teruki Sasaki