



Overview

Optimized for 5 V mixed-signal applications, the C5 process family from ON Semiconductor offers a medium-density, high-performance mixed-signal technology capable of integrating complex analog functions, digital content and 20 V capability. This process delivers the advantages of a dedicated mixed-signal 0.5 μm process without the costs associated with the extra mask steps of a BCD process. Low-voltage transistors are also available for the 0.5 μm process making it well-suited for low-power applications.

Features

- 2 or 3 Metal Layers
- Poly to Poly Capacitors
- EEPROM
- Schottky Diodes
- High-voltage I/O – 12/20 V
- High-resistance Poly
- Low-voltage Modules

PROCESS CHARACTERISTICS

Operating Voltage	5, 12 V
Substrate Material	P-Type, Bulk or EPI
Drawn Transistor Length	0.6 μm
Gate Oxide Thickness	13.5 nm
Contact/Via Size	0.5 μm
Contacted Gate Pitch	3.9 μm
Top Metal Thickness	675 nm
Contacted Metal Pitch	
Metal 1	1.5 μm
Metal 2, 3	1.6 μm
Metal Composition	TiN/AlCu/TiN

SAMPLE PROCESS OPTIONS

	Mask Layers*
Standard CMOS with 20 V extended drain	13/15
Plus double poly cap	14/16
All of the above plus 1,000 Ω /square resistor	15/17
All of the above plus 12 V gate	16/18
All of the above plus low V_t devices	19/21

*2 Metal / 3 Metal.

DEVICE CHARACTERISTICS

(All Values Typical at 25°C)

HIGH-VOLTAGE TRANSISTORS 12 V DUAL GATE NESTED DRAIN

N-Ch 12 V (NU)	Typical Value	Units
V_t	0.95	V
I_{dsat}	450	$\mu\text{A}/\mu\text{m}$
B_{VDSS}	19	V
P-Ch 12 V (PU)	Typical Value	Units
V_t	-1.6	V
I_{dsat}	-110	$\mu\text{A}/\mu\text{m}$
B_{VDSS}	-14.5	V

20 V EXTENDED DRAIN, 15 V GATE

N-Ch 20 V (NX)	Typical Value	Units
V_t	0.95	V
I_{dsat}	400	$\mu\text{A}/\mu\text{m}$
B_{VDSS}	28	V
P-Ch 20 V (PU)	Typical Value	Units
V_t	-1.65	V
I_{dsat}	-130	$\mu\text{A}/\mu\text{m}$
B_{VDSS}	-28	V

20 V EXTENDED DRAIN, 5 V GATE

N-Ch 20 V (NT)	Typical Value	Units
V_t	0.75	V
I_{dsat}	145	$\mu A/\mu m$
B_{VDSS}	28	V
P-Ch 20 V (PT)	Typical Value	Units
V_t	-1.0	V
I_{dsat}	-55	$\mu A/\mu m$
B_{VDSS}	-28	V

STANDARD TRANSISTORS

N-Channel	Typical Value	Units
V_t	0.7	V
I_{dsat}	450	$\mu A/\mu m$
P-Channel	Typical Value	Units
V_t	-0.9	V
I_{dsat}	-260	$\mu A/\mu m$

RESISTORS

	Typical Value	Units
Poly	25	Ω/square
Hi-R Poly	1000	Ω/square
N-Diffusion	80	Ω/square
P-Diffusion	110	Ω/square
N-Well	855	Ω/square

CAPACITORS

Poly-Poly	Typical Value	Units
Area	0.9	fF/ μm^2
Periphery	0.065	fF/ μm

LIBRARIES

(All Values Typical at 3.3 V, 25°C)

Front-End Digital Design	
Digital	Synthesis Libraries
	Simulation Libraries
Analog – General Design Information (GDI)	Design Rules
	Spice Models
Digital Design	
High Performance Core	4.2 K gates/ mm^2 *
	1.58 $\mu W/\text{MHz/gate}$
Tall Pads for High I/O Count Designs	103 ps gate delay (2 Input NAND, fanout = 2)
	86 μm in-line pad pitch
	60 μm staggered pad pitch
	558 μm pad height
Mixed-Signal Design	
Cadence Technology File	Separate substrate bus for reduced digital noise
Cadence Transistor Library	7.4 K gates/ mm^2 *
Mixed-Signal Core	0.63 $\mu W/\text{MHz/gate}$
	558 μm pad height
Mixed Signal Short Pads for High Logic Contact Designs	128 ps gate delay (2 Input NAND, fanout = 2)
	135 μm in-line pad pitch
	388 μm pad height
Mixed-Signal Medium Height Pads	86 μm in-line pad pitch
	567 μm pad height

*Routed gate density.

MEMORY OPTIONS

SRAM	
Single Port Synchronous*	191 $\mu m^2/\text{bit}$ (64 k bit memory)
Dual Port Synchronous*	567 $\mu m^2/\text{bit}$ (64 k bit memory)
ROM	
Asynchronous*	14.65 $\mu m^2/\text{bit}$ (64 k bit memory)
EEPROM	
NASTEE (No Additional Steps EEPROM)	Vector (1x4 up to 1x32)
	Array (2x4 up to 32x32)

*Compiled

CAD TOOL COMPATIBILITY

Digital Design	Synopsys Design Compiler
	Cadence Verilog
Analog Design	Cadence DFII (4.4.6)
	Spectre
Place and Route	Synopsys Apollo, Astro
	Cadence Silicon Ensemble
Physical Verification	Mentor Calibre

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