CMOS Synchronous Buck Switching Power Supply

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Part 1 Bandgap: The first part of the project was to design a band gap to output a reference voltage of 1.25 volts. The bandgap was built to not vary in voltage no matter the temperature of the simulation. The output voltage V_{ref} stays constant in a bandgap and isn't affected by temperature or varying vdd.

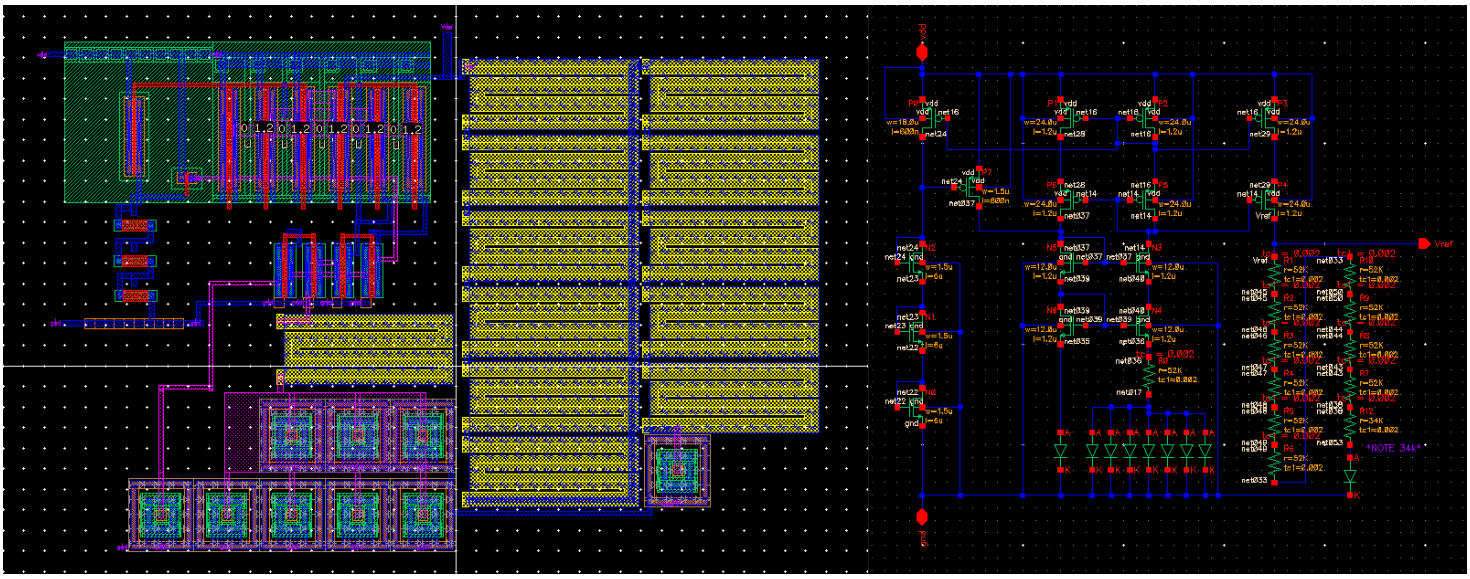
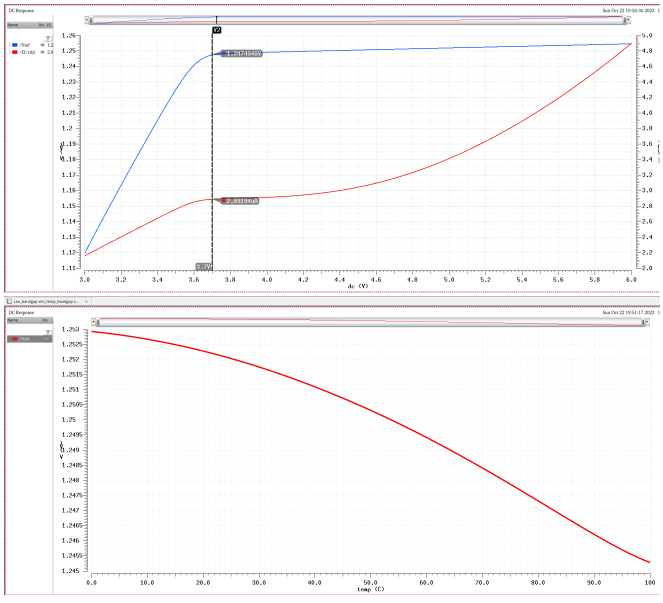


Figure 1 : Bandgap Layout and Schematic

There are two variables we consider with the Bandgaps performance. We test the circuit's performance with a changing supply voltage, and a changing temperature.



The first curve shows that our power supply has a lower limit of 3.7 before our output starts to drop off.

For anything $\geq$ $3.7V$ The output reference voltage will be approximately 1.25V.

As our power supply voltage increases, the current draw (red trace) increases exponentially.

The second curve shows that from a temperature sweep from 0℃ $\rightarrow$ 100℃ our voltage only shows a drop of 8mV which less than a 1% loss at $.64\%$

These characteristics are within our design parameters as our vdd will vary from 4V to 5.5V thus meeting the 3.7V threshold for this design

Part 2 Comparator: The comparator is the brains behind our circuit as it is in charge of operating the circuit. The positive input of the comparator will be held at 1.25V by the Bandgap discussed above, the other input will be used by the feedback of the circuit after passing through the resistors. If the Feedback voltage exceed the our V_{ref} the comparator outputs a logic 0, otherwise it will output a logic 1. The sensitivity of the comparator is very important to being able to detect differences in the input. Ideally we want a comparator that responds to the smallest difference in voltage. However this is impractical as the smallest noise would cause unwanted oscillations when the Feedback is very close in voltage. Thus a small amount of hysteresis was added. That being an upper and lower limit where the comparator will switch values. We designed this to be as small as possible without causing false positives. Using 3 stages of differential amplifiers, then we sent it through a 3 stage buffer to smooth out the signal. The 2 inverters produce the sensitivity we aimed to achieve without being too susceptible to noise.

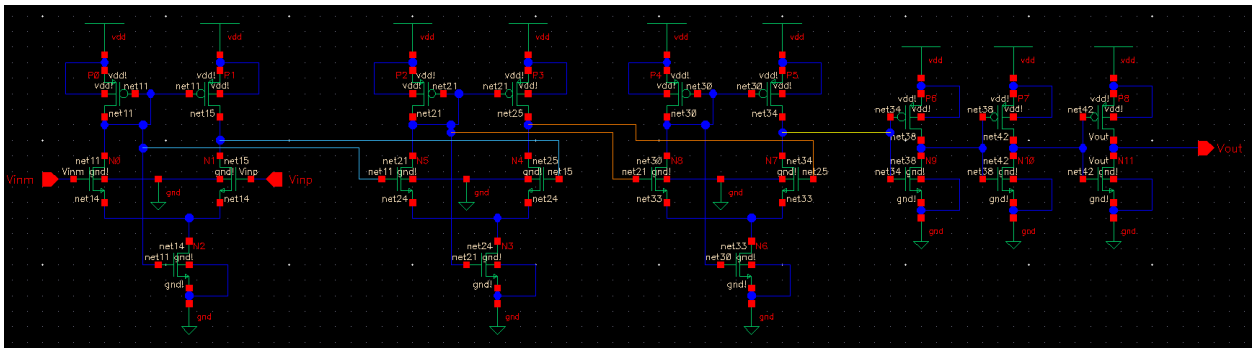


Figure 2: Schematic of comparator

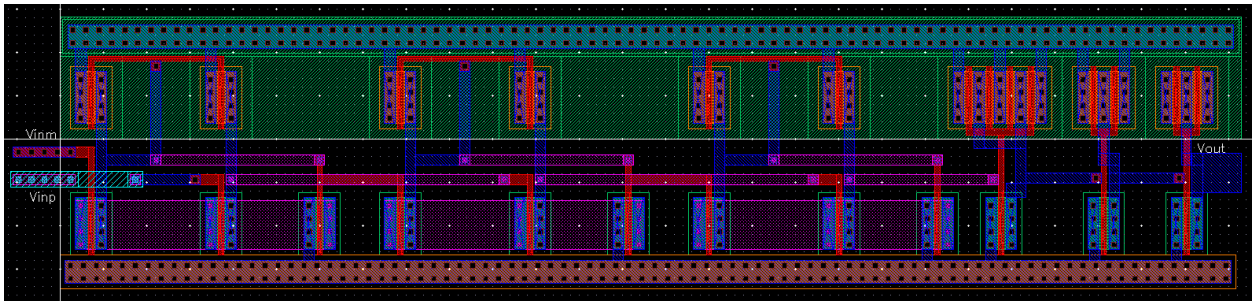
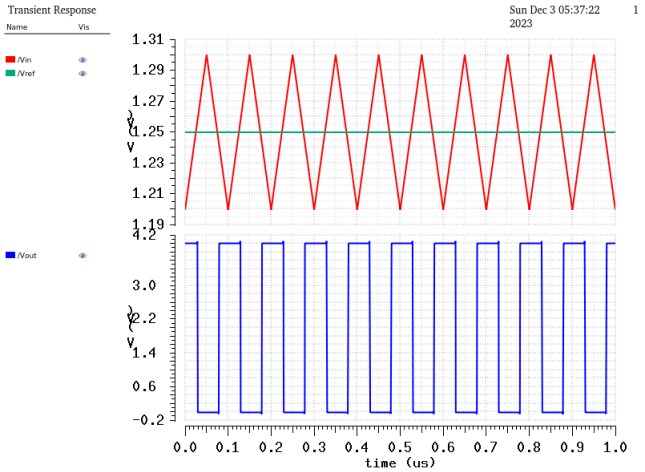


Figure 3: Comparator layout



In the graph, V_{out} (in blue) is the enable signal for our NAND gate. The output is a decisive switch right when the input (V_{in} in red) crosses V_{ref}(in green)

Part 3 SR Latch (Pull up Pull down): This switch regulating latch consists of 2 NAND gates and an odd number of inverters. Since we are implementing 2 NMOS pull up we have taken into account that the MU (top NMOS) has to be driven to a higher voltage in order for MU to turn on. The first portion of the circuit was designed as a Non-Overlapping clock generator to ensure MU and MD are never on at the same time. This reduces the crossover current.

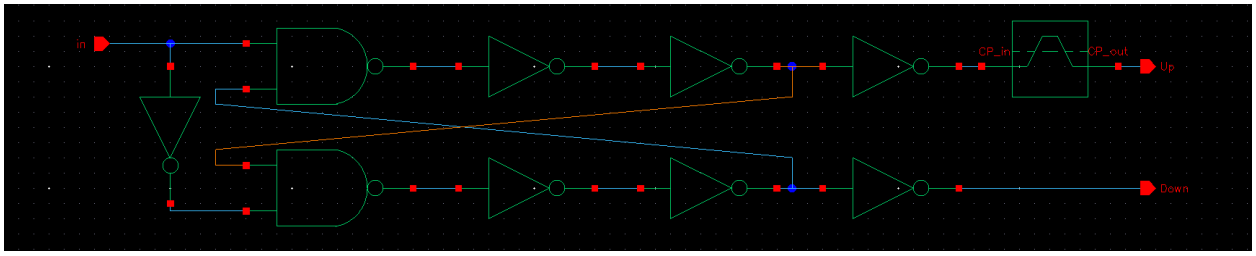


Figure 4: SR latch with Charge Pump

The last two inverters are scaled up by a factor of 8 to help drive up the signal before either the Charge pump or to the bottom NMOS. The first 5 inverters (including the left most) are at a size of 18u/6u and the last two at 144u/48u. The reason for the different sizes of the inverted in the latch is to amplify current that will be supplied to the NMOS's

Part 4 Charge Pump: The Charge pump is meant to double the vdd singal Assuming vdd is between 4.5V and 5.5V, a valid input logic 0 is 1V or less, a valid input logic 1 is 3V or more. Notice in the schematic that Node (A) does not supply any power to the output. Its only purpose is to turn on M2 thus allowing node (B) to be precharged to VDD when the input is low.
For the next cycle we will achieve an output voltage closer to our 2VDD that we desire. This is necessary to turn on our top NMOS for that we chose CAP(2) to be 12.25pF which is at least 10x the total input capacitance of MU and MD. We exceed that as

$$C_{MU} = C'_{ox} * L * W = 2.5fF/\mu m^2 * (.6\mu)(2m)$$

$$C_{MD} = C'_{ox} * L * W = 2.5fF/\mu m^2 * (.6\mu)(2m)$$

$$C_{tot} = C_{MU} + C_{MD} = 6 * 10^{-18} = 6aF$$

This is sufficient to drive our two nmos C_{load}. This design was also tested at various Vdd and C_{load} to ensure it would work from 4.5V to 5V to ensure proper switching speed of less than 4nS for all scenarios. Below is that data.

	4.0V Low to High	4.0V High to Low	4.5V Low to High	4.5V High to Low	5.0V Low to High	5.0V High to Low	5.5V Low to High	5.5V High to Low
0pF	250.2pS	769.7pS	177.1pS	917.3nS	140.9pS	877.1pS	101.3pS	836.6pS
0.5pF	603.5pS	1.293nS	130.7pS	1.123nS	144.3pS	1.105nS	141.9pS	1.090nS
1pF	886.7pS	1.702nS	430.6pS	1.242nS	308.9pS	1.243nS	351.1pS	1.253nS

Part 5 NMOS Transistors: In order to figure out the sizes for our transistors we need to set out duty cycles. To do that we use the following equation $V_{out} = D * V_s$ if we want our $V_{out} = 3.125$ at our worst case scenario of $V_s = 4V$ our duty cycle will have to be at least 78.125%. However I did not want to be on the edge of 3.125 so I increased the duty cycle to 80% as this ~ 2% increase will inevitably affect our Feedback average by ~ + 2% which is 3.13V. Now to figure out the actual size for our transistors this is done with the keeping in mind that ideally R_U & R_D would each be 0Ω this is impractical as to achieve that we would need infinite W/L. This hold true for the PMOS NMOS switch however we are using the NMOS Pull-up and that requires both NMOS transistors to at 3x multiplier of each other $R_U = 3R_D$ however after plugging in values that made sense those being MU = 1080 and MD = 360 we were unable to achieve our desired Feedback so remember the prior relationship to size and us wantong larger resistance of our transistors we doubled MU and kept MD the same this proved to let us get closer to our desired FeedBack. We were able to finally achieve the desired FeedBack by setting MD near the same size of MU(2m).

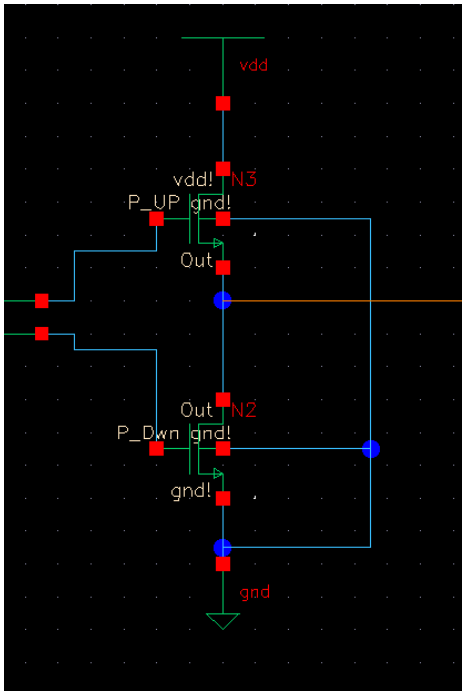


Figure 5: NMOS Transistors

Part 6 Assembly of Buck Converter: Now we construct the synchronous Buck switching power supply. We assemble all the devices we mentioned above that being: Bandgap, Comparator, SR Latch with Charge pump, and NMOS Pull-up. All of these create a signal we will refer to as out from here on forward. This signal will need to be fed through a low pass filter which is used to smooth out our signal and only allow our desired Feedback to generate a DC voltage for supplying our load with its desired 50mA current. The inductor, capacitor, and resistor are all off chip. To get the desired $I_{out} = 50mA$ we used R to represent our load and set that to 62.5Ω. With that determined I was able to calculate the minimum inductance needed with $L_{min} = \frac{R(1-D)}{2f}$ we set our frequency at 1MHz with that we get $6.25\mu H$. However we ended up using 10x this value later in the design. With the inductor value calculated we can use it to find out Capacitor value with the following $C_{min} = \frac{1-D}{8*L*(\Delta V_{out}/V_{out})f^2}$ this results in us getting $4\mu F$.

Another thing we have to set for our assembly is a voltage divider that will make out 3.125 into 1.25 for the comparator to read it. We did this with 52k Resistors as I already had them in my design library and they met design specifications of the comparator for current $10\mu A \leq I_{Drawn} \leq 50\mu A$

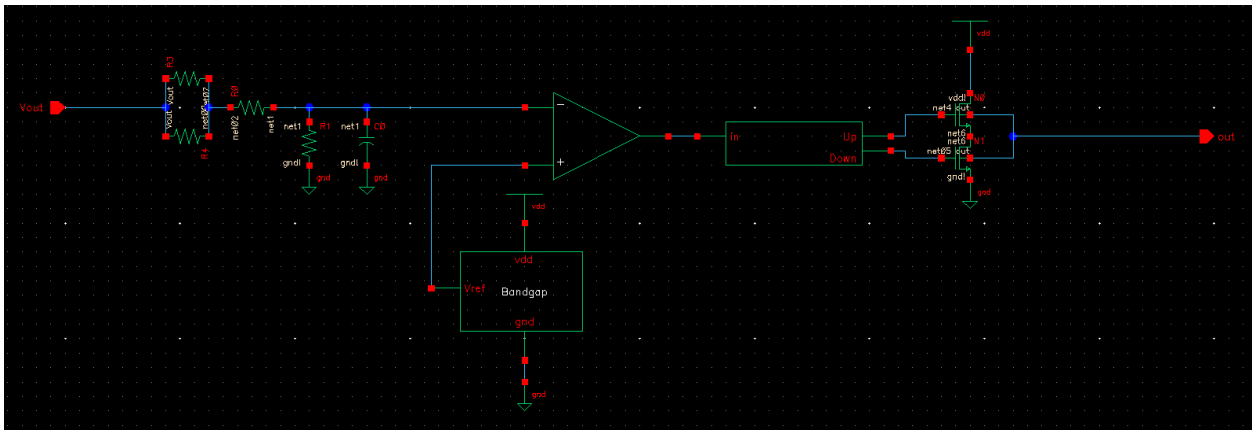


Figure 6: Buck Converter Schematic within Chip

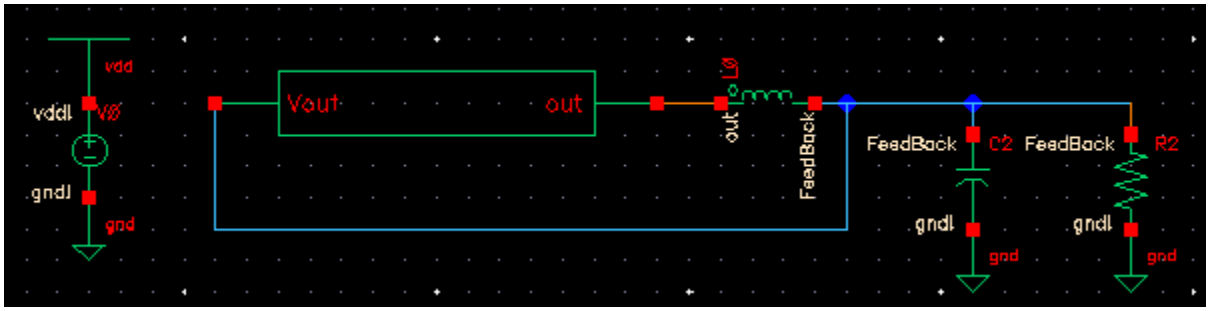


Figure 7: Testing with Symbol

Part 7 Layout:

For the layout I wanted to utilize one rail being a global VDD and one rail being a Global GND and to do that I will be instantiating my components and they will have their own VDD and GND rails which in the end should allow me to have a compact design that is space efficient and practical.

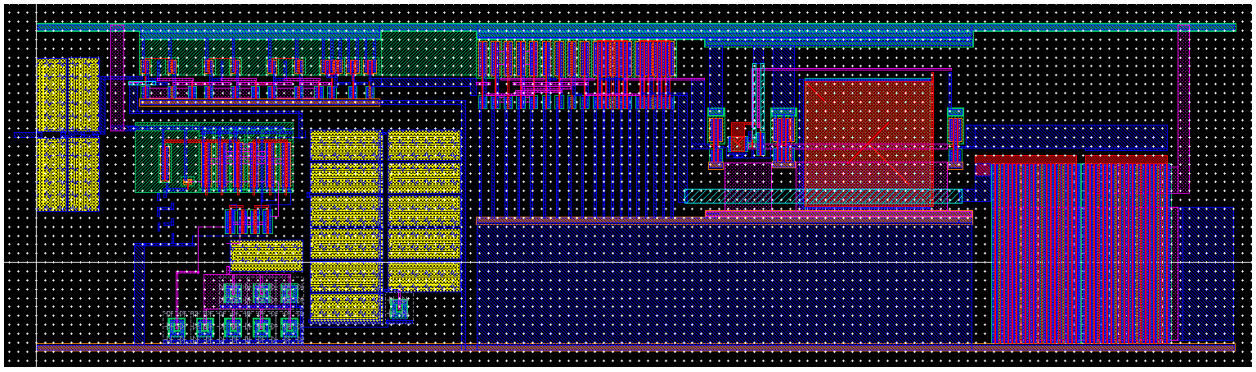


Figure 8: Layout of Buck Converter

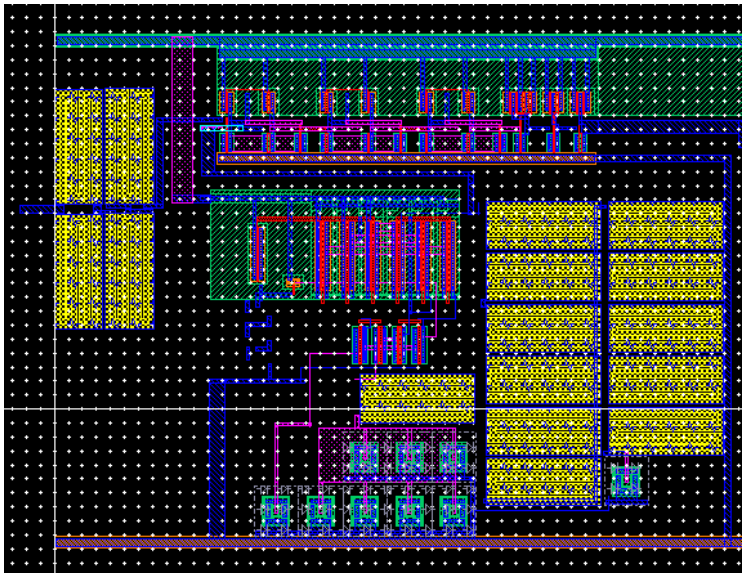


Figure 9: First half of layout with Voltage divider, bandgap, and comparator

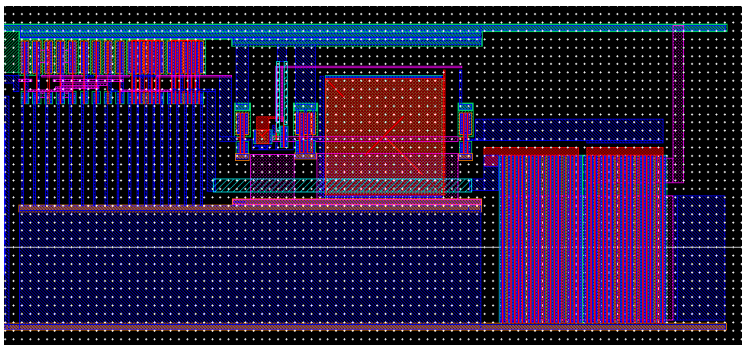


Figure 10: Second half of layout with SR Latch and Pull up NMOSs.

Part 8 Testing at Varring $Vdds\ 4V \rightarrow 5.5V$:
We testes a wide range of parameters
$Feedback$ - Voltage being feedback to the system
$\Delta Feedback$ - Ripple of Voltage in Feedback
I_R - Current through Resistor
I_S - Current through Source
I_L - Current through Inductor
ΔI_L - Ripple of current in Inductor
I_{comp} - Current feed into comparator
E_{ff} - Efficiency

VDD	4V	5V	5.5V
$Feedback$	3.112V	3.123V	3.13V
$\Delta Feedback$	26mV	38mV	43mV
I_R	49.79mA	49.98mA	50.08mA
I_S	42.05mA	35.26mA	33.0mA
I_L	49.79mA	50.09mA	50.14mA
ΔI_L	92.51mA	153.2mA	173.01mA
I_{comp}	23.94mA	24.03mA	24.08
E_{ff}	92.41%	88.73%	86.46%

Part 9 Test varying temperature 0℃ → 100℃**:**
For the last portion of testing we ran a parametric analysis on the circuit to test Feedback at different temperatures ranging from 0℃ → 100℃ in steps of 10℃**.**

	0℃	**10**℃	**20**℃	**30**℃	**40**℃	**50**℃	**60**℃	**70**℃	**80**℃	**90**℃	**100** ℃
4.0V	3.114	3.113	3.113	3.112	3.059	2.754	1.643	-	-	-	-
5.0V	3.126	3.125	3.124	3.123	3.122	3.12	2.782	-	-	-	-
5.5V	3.132	3.132	3.131	3.13	3.128	3.126	3.124	-	-	-	-

From the data we can extrapolate that we need to provide cooling before we hit 50℃ after 60℃ The circuit suffers from overheating and the performance suffers and eventually we are led to total failure. We also notice that as VDD increase we are able to withstand the higher temperatures better but not overcome the 60℃ temperature failure. We would need forced air cooling in the form of a small fan or ambient cooling provided by another commonet if we pertain to a larger system.

Future Improvements:
It is clear I have not optimized the low pass filter as while the original 6.25µ*H* did provide the best efficiency it also let in a lot of negative current. The temporary fix of increasing the Inductor 10 fold solved the problem by at worst case scenario allowing -40mA versus the 6.25µ*H* at points letting in over -150mA. Another area we can improve on is our transistor placement as we did have 2 PMOS not in the shared well and a large portion of the NMOS did not share the same active.

Conclusion:
In the end it is still clear to see that the choice of a flyback converter is still superior to a buck as we can configure both step up and step down in voltage. We are also able to have multiple output windings, each with a different voltage. This makes them suitable for applications requiring multi - voltage outputs such as consumer electronics. The most crucial point is in reliability as when tested on the same range of temperatures the flyback saw no loss in efficiency this is due to less stress imposed on the semiconductors.
That is not to say there aren't situations where a buck is practical, one of them being in simplicity and cost. Another area they are heavily used is in battery powered devices to help regulate voltage to extend the life of products.