Prelab 9

Thursday, April 16, 2015 11:01 PM

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EE 420 L

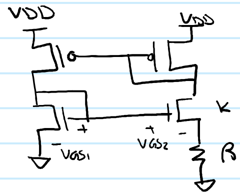
$g_m = 20\mu A/V$ $\quad \frac{W}{L} = \frac{500\mu}{5\mu}$ $\quad k_{pn} = 9.38\times10^{-6}$, $k_{pp} = 4.8\times10^{-6}$ $\quad V_{THN} = 1.2$, $V_{THP} = 1.75$

NMOS

$$g_m = \sqrt{2 k_{pn} \tfrac{W}{L} I_D}$$

$$20\mu = \sqrt{2 \cdot 9.38\times10^{-6}\ \tfrac{500\mu}{5\mu} I_D}$$

$$I_D = 213nA$$



$$V_{GS1} = V_{GS2} + I_D R$$

$$\sqrt{\frac{2I_D}{k_{pn}\frac{W}{L}}} + V_{THN} = \sqrt{\frac{2I_D}{k_{pn}\frac{KW}{L}}} + V_{THN} + I_D R$$

$$\left(1 - \frac{1}{\sqrt{K}}\right)\sqrt{\frac{2I_D}{k_{pn}\frac{W}{L}}} = I_D R$$

$$\left(1 - \frac{1}{\sqrt{K}}\right)^2 \frac{2I_D}{k_{pn}\frac{W}{L}} = I_D^2 R^2$$

$$R^2 = \left(1 - \frac{1}{\sqrt{K}}\right)^2 \frac{2}{I_D k_{pn}\frac{W}{L}}$$

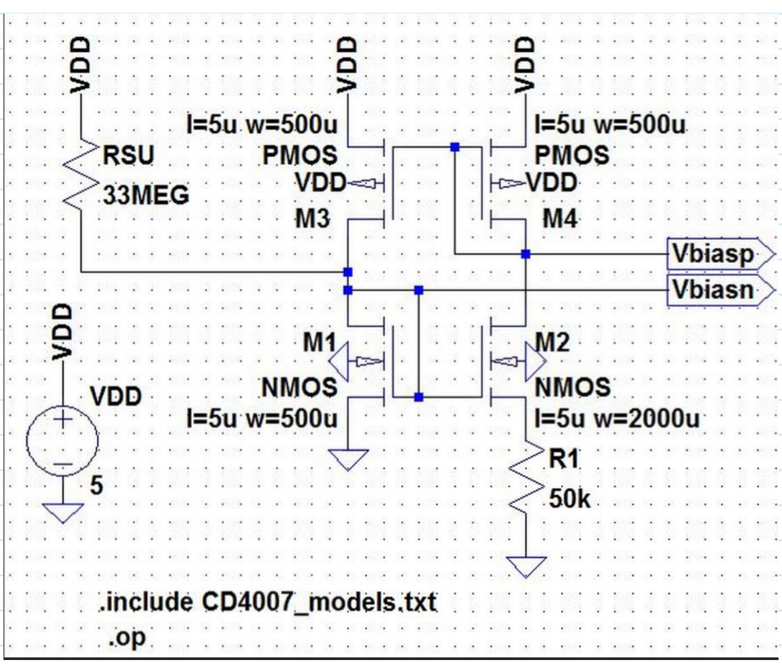
$$R = 1 - \frac{1}{\sqrt{K}}\sqrt{\frac{2}{I_D k_{pn}\frac{W}{L}}} \qquad \text{let } K = 4$$

$$R = \sqrt{\frac{1}{2 I_D k_{pn}\frac{W}{L}}} \Rightarrow \frac{1}{R} = g_m = 20\mu = \sqrt{2 I_D k_{pn}\tfrac{W}{L}}$$

$$\boxed{R = \frac{1}{20\mu} = 50k}$$

Min VDD for Vbiasn to stabalize

$$V_{GS} + V_{DS,sat} + V_{SG}$$
$$= 1.2 + 0 + 1.75$$
$$= 2.95 \Rightarrow \text{min VDD}$$



P2

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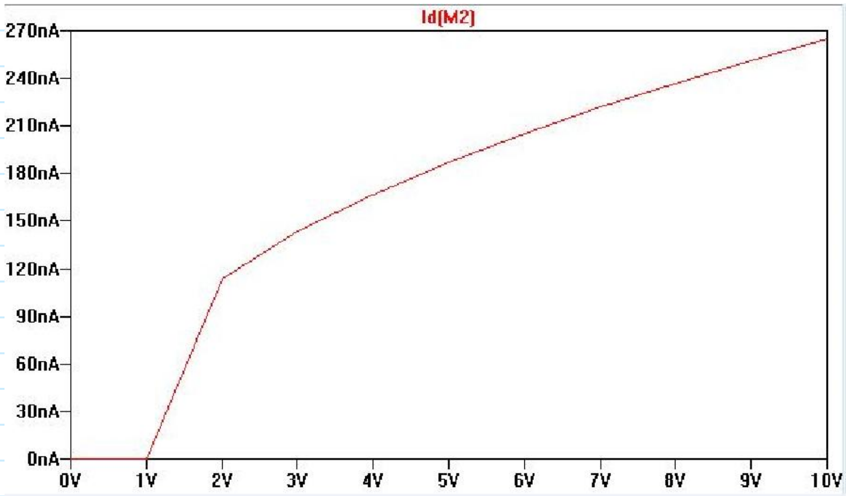

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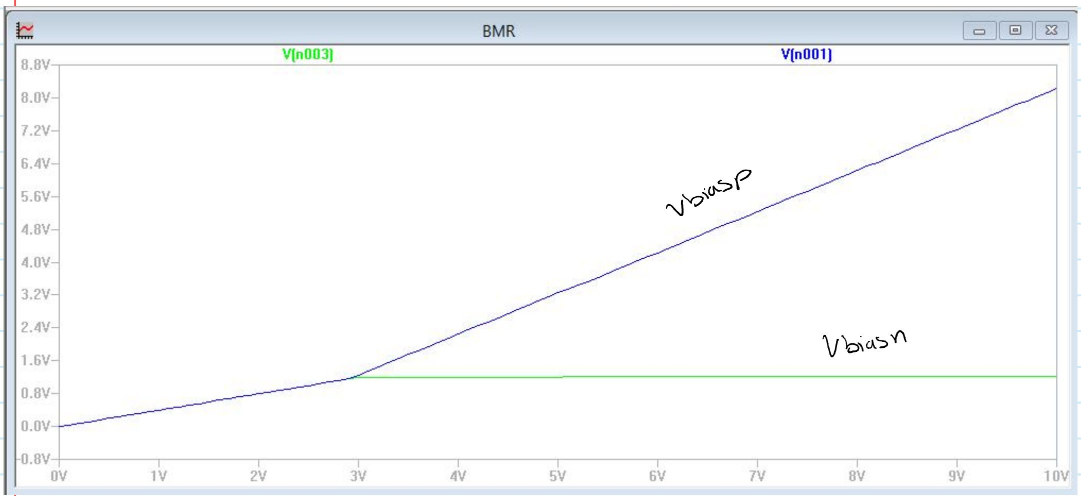
We can see that our BMR from simulations rounds out at around 180-250nA. One of the possible reasons for this may be because that we are using a resistor as a startup and the resistor will steal some current form the mirror.



Vbiasn and Vbiasp

From the figure above, we can see that Vbiasn stays constant after the minimum VDD voltage (~3V) and Vbiasp follows VDD after that same minimum VDD voltage.