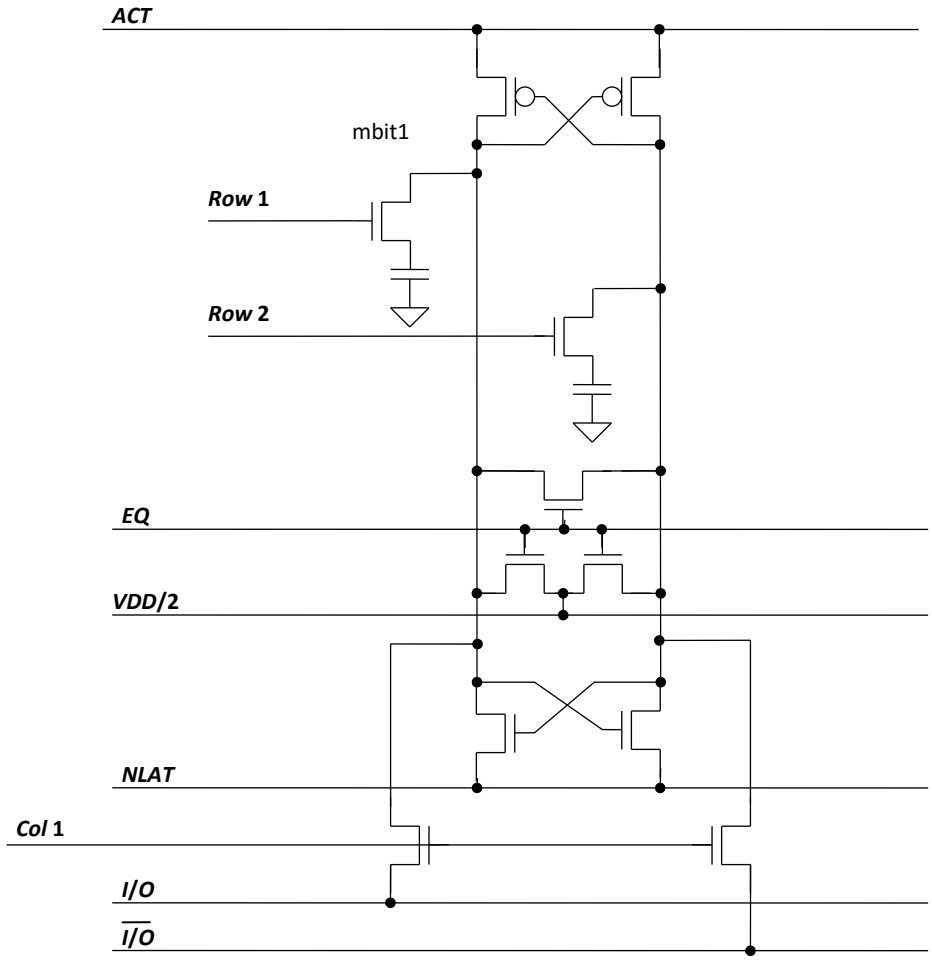
ECG 721 Memory Circuit Design, Midterm exam

Practice, University of Nevada, Las Vegas

Name: _____

- Show your work to get credit.
- Open book and closed notes.
- Do all work on these test sheets only (no extra paper).

1. On the back of this piece of paper sketch the waveforms, using a common time axis but several y-axes to make things clear, we would have if we write a 0 to mbit1 in the circuit seen below. State all assumptions. (15 points)



2. In a DRAM charge sharing example (Fig. 16.71 with $V_3 = V_4 = 0$) show, using equations, how energy ($0.5CV^2$) is not conserved. Where does the lost energy go (where is power dissipated in the circuit)? (15 points)

3. Discuss, **in your own words**, the advantage of precharging the bit lines to *VDD* in a 6T SRAM. What are the drawbacks? Is there any advantage if an SRAM cell using polysilicon pull-up resistors is used? Show your schematics and state all assumptions. Are n- or p-sense amplifiers needed? Why or why not? (15 points)

4. Is it possible to have only an n-well in a Flash memory technology? If so how and if not why? Use cross-sectional views to illustrate your understanding. (15 points)

5. Derive the relationship between V_R and V_I for the DSM circuit seen in Fig. 17.36. Is it bad if $V_R > V_I$? Why or why not? (20 points)

6. Show how to design a negative charge pump (voltage generator) that outputs a voltage less than -2*VDD*. Comment on your design and, of course, show a schematic. (20 points)