Use and Design of Synchronous Mirror Delays (SMDs)

Abraham Lopez

ECG 721 – Memory Circuit Design

Fall 2021

Introduction

- What are SMDs?
  - SMDs, like phase-locked loops (PLLs) and delay-locked loops (DLLs), are clock synchronization circuits.
  - Clock synchronization circuits help to deal with clock skew, synchronizing input and output clocks to read in data correctly, by generating an output clock that is the same as the input clock.
- How are they different from PLLs and DLLs?
  - SMDs are open loop systems where as PLLs and DLLs are closed feedback loop systems.
- How are SMDs implemented?
  - SMDs can be implemented using digital and analog designs both of which will be covered.

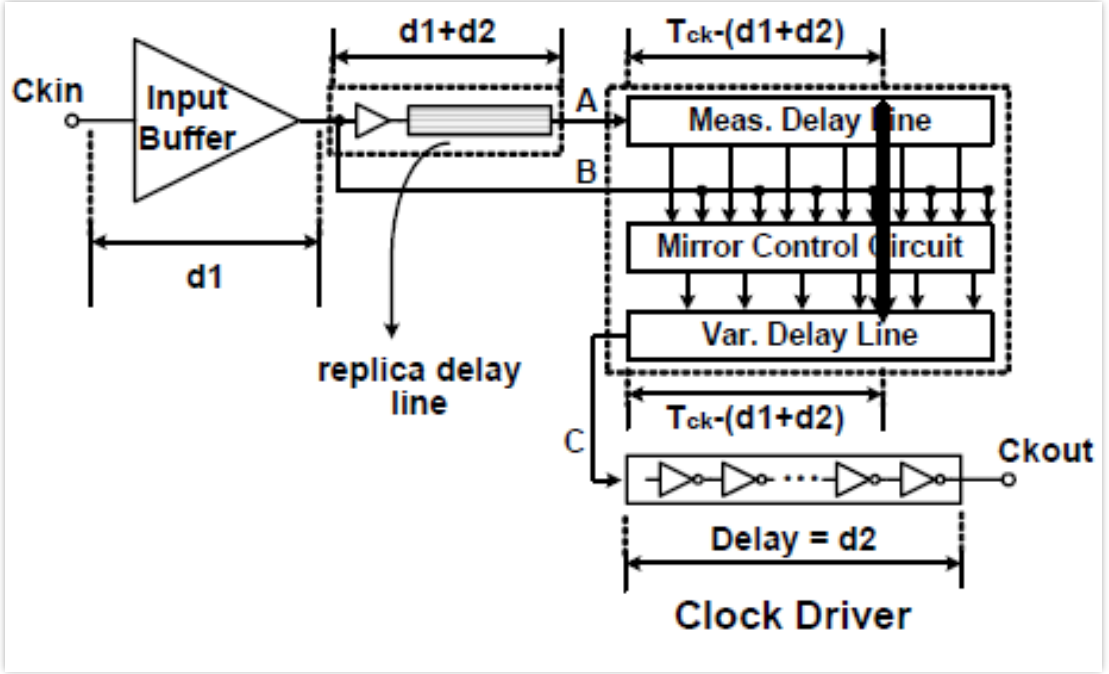
Applications

- As mentioned before in the previous slide SMDs are an open loop system this allows the SMD to have a short lock time as it only needs two clock cycles to synchronize with an input clock. Compared to PLLs and DLLs that need hundreds of cycles in order to lock.
- With such a short lock time the SMD has a smaller idle power consumption than closed loop systems. Also, open loop systems are much simpler to use while occupying a smaller layout on a chip than closed loop systems, as they are higher order systems while taking up more space.
- These advantages make for useful applications in memory architectures like Synchronous DRAM (SDRAM), Rambus DRAM (RDRAM) and system on chip systems (SOCs). As advances in these technologies grows, then these systems and architectures need to operate at higher frequencies with faster data access without increasing clock skew.

Digital Synchronous Mirror Delay (DSMD)

- Now we'll move on to covering the digital design of the SMD
- Six components make up the DSMD
  - Input buffer
  - Replica delay line (RDL)
  - Measurement delay line (MDL)
  - Mirror control circuit (MCC)
  - Variable delay line (VDL)
  - Clock Driver

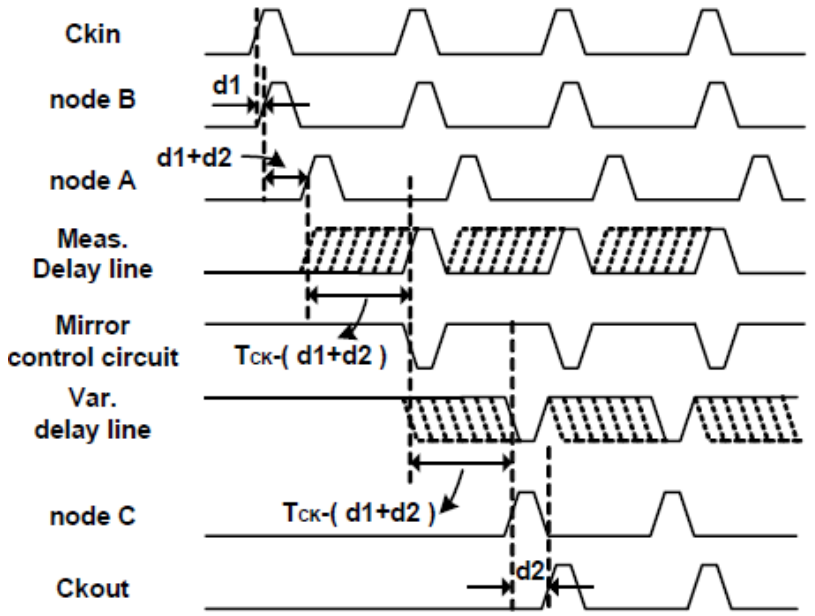
DSMD Block Diagram



Operation of DSMD

- The DSMD operates by taking in an input clock Ckin which goes through the input buffer and adds a delay d1 at Node B.
- Then the signal goes through the DM, which is a replica of the delay of the input buffer and clock driver, that delays the signal further to d1+d2.
- It then heads to the MDL which measures the time it starting from node A until node B goes high, and this time is noted as the delay of Tck – (d1+d2).
- This delay time is mirrored by the MCC until node B goes high, which causes the MCC to go low starting the VDL.

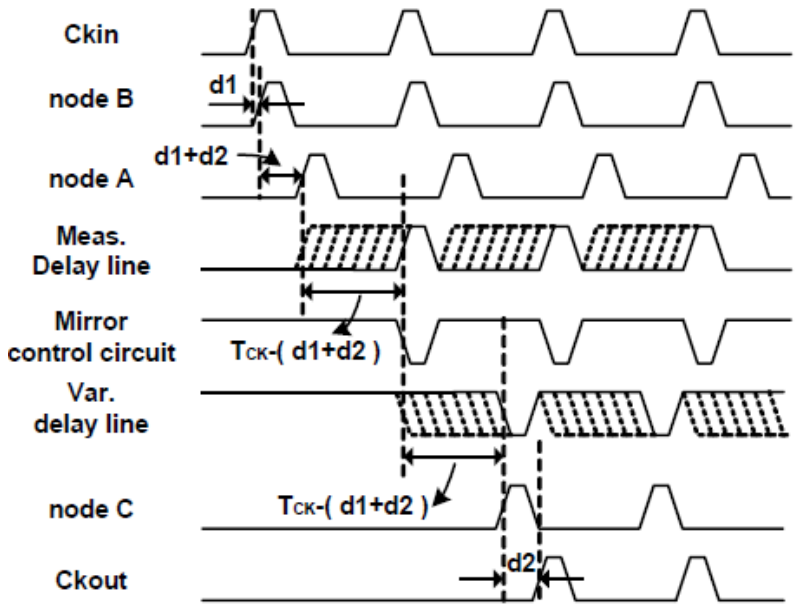
DSMD Timing Diagram



Operation of DSMD (continued)

- As the VDL is on it takes the delay from the MCC of Tck – (d1+d2) and after that delay set node C high.
- After Node C is high it is then pushed through the clock driver with a delay of d2 which is then the synchronized output clock Ckout.
- The total time for Ckout is Td = d1+(d1+d2)+ Tck – (d1+d2)+Tck – (d1+d2)+d2 = 2*Tck
- Proving the early point mentioned where the SMD only takes two clock cycles in order to lock up.

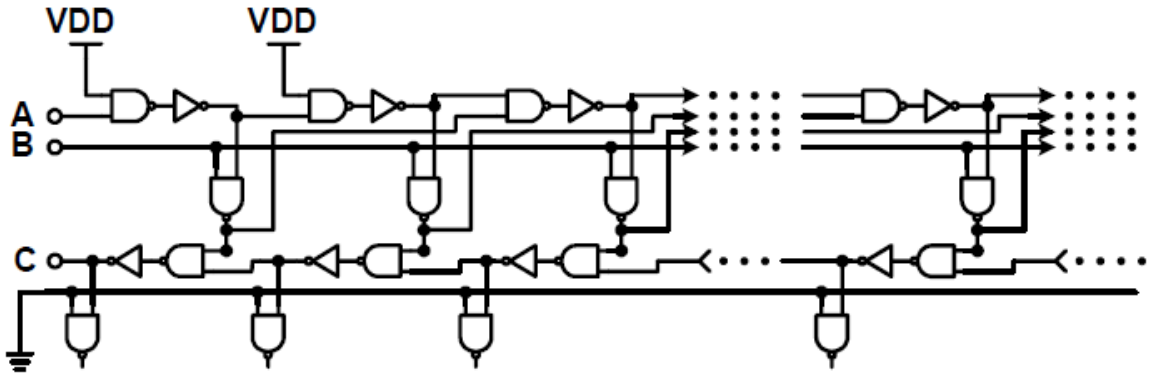
DSMD Timing Diagram



DSMD Circuit

- Here we can see the basic circuit that makes up the MDL, MCC, and VDL.
- Where each delay element is an AND gate (NAND and inverter) in the MDL and VDL. With the MCC composed of NAND gates.
- Also, the dotted lines indicate the circuit can be made with a certain number of stages we'll call N.

DSMD Circuit Diagram



DSMD Design

- When designing a DSMD there are several things to account for with the one being the number of stages N that the DSMD will have.
- This can be calculated from the maximum clock period, $T_{ck,max} = d1+d2+(N*dc)$, then solving for $N = (T_{ck} – (d1+d2))/dc$. Note dc is the delay through each cell and that the minimum clock period is $T_{ck,min} = d1+d2$.
- An important note is that the DSMD suffers from a quantization error if N is not a whole number.
- We also know from earlier the time delay of the DSMD is $T_d = d1+(d1+d2)+T_{ck} – (d1+d2)+T_{ck} – (d1+d2)+d2 = 2*T_{ck}$. With these equations in mind, we can solve for a desired clock period Tck, along with the delays due to the input buffer (d1), clock driver (d2), cell (dc) and the number of stages N. All values that can be selected with designed elements which we'll see in the next slide.

DSMD Example Calculations

- Let us consider we designed an input buffer, cell, and clock driver with delays of d1 = 50 ps, dc = 60 ps, and d2 = 100 ps. We also want this DSMD to be able to operate at a clock speed of 1 GHz (Tck = 1ns).
- Hence solving for N, we get N = 14.1667 or N = 14 as we want whole numbers to avoid quantization errors.
- It should be noted that if we want the circuit to operate at lower frequencies that we increase the number of stages. For example, a DSMD operating at 500 MHz then N = 31 or at 100 MHz, then N = 164. Here we see that the stages can increase significantly taking up more layout space on a chip.
- While the delay from the cell (dc) can be increased to lessen this effect, it will in turn increase the quantization error. It is ideal then that dc is the smallest value possible to keep the error low while allowing for a smaller number of stages for the DSMD.

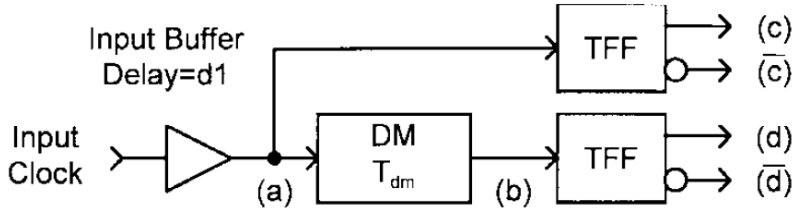
DSMD Benefits and Drawbacks

- Benefits
  - Short lock time of two clock cycles
  - Low idle power consumption
  - Simple design
  - No clock jitter
  - Robust to PVT variations
- Drawbacks
  - Inherent quantization error
  - Lower frequencies require a higher number of stages
  - Duty cycle cannot be 50% or more; input pulse width must be narrow
  - Can only be operated at designed frequency

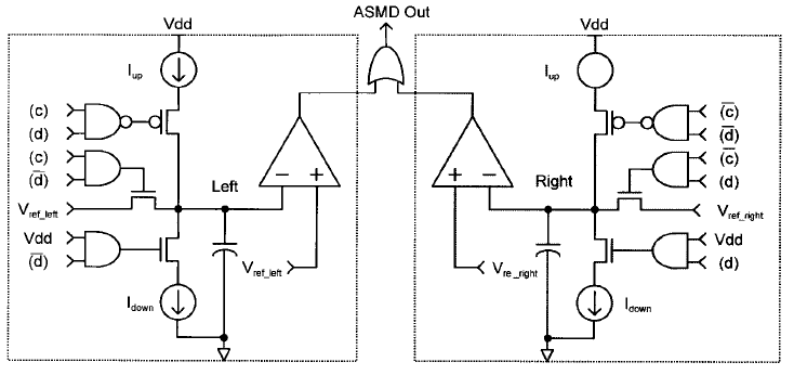
Analog Synchronous Mirror Delay (ASMD)

- We'll now move on to discussing the ASMD
- Five components make up the ASMD
  - Input Buffer
  - Delay Monitor (DM)
  - Toggle Flip-Flop (TFF)
  - Charge pump (CP)
  - Comparator

ASMD Input Buffer, DM and TFF



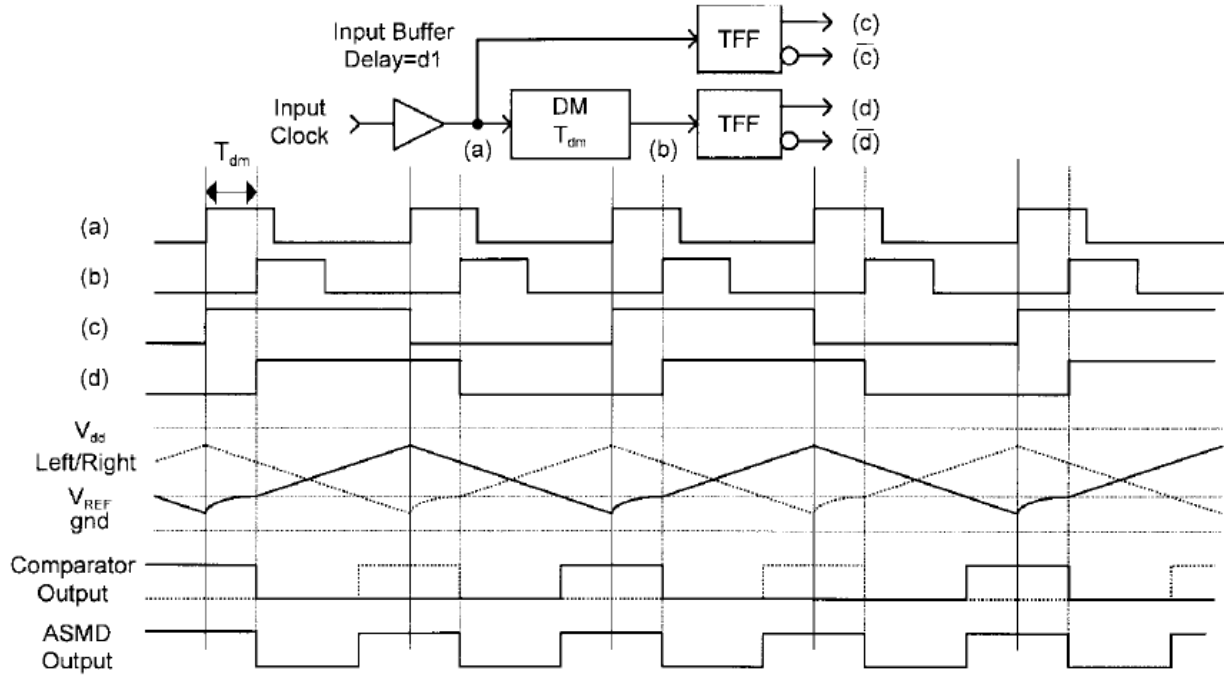
ASMD CP and Comparator



Operation of ASMD

- The ASMD works by first inputting a clock signal through the input buffer.
- At node A then the signal is split with one to a TFF and the other through the DM.
- We see that the DM introduces some delay Tdm at node B before it is then sent to the other TFF.
- The two TFFs output a set of complementary signals (c ,c_ , d, d_) that control the CP and comparator.

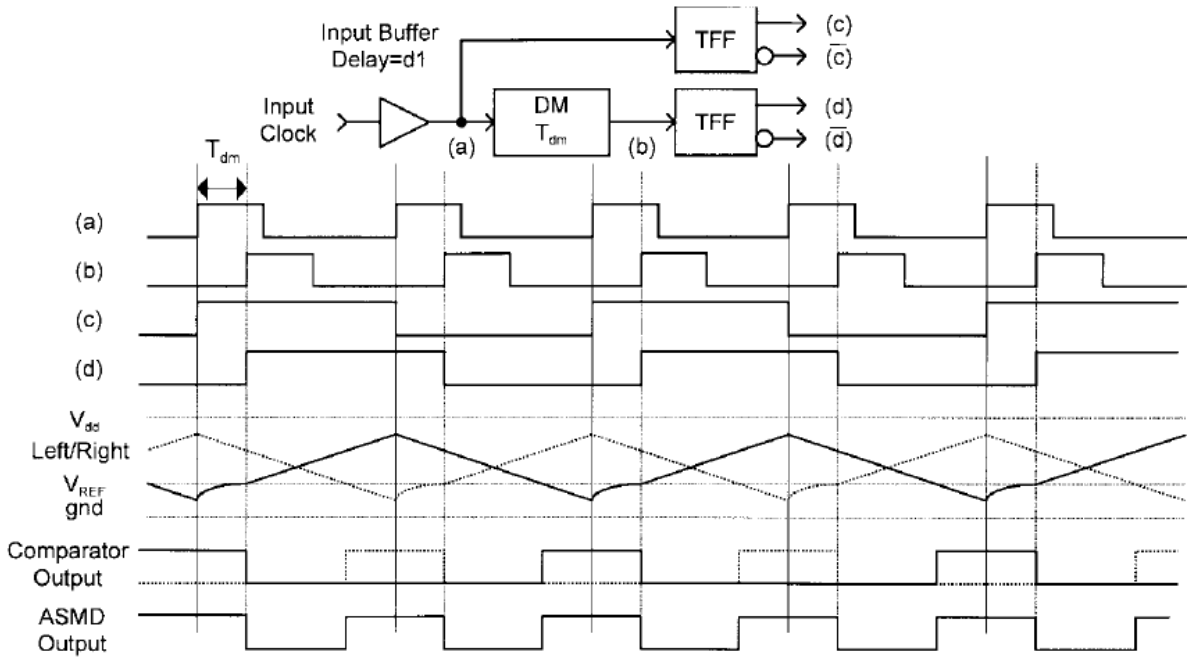
ASMD Timing Diagram



Operation of ASMD (continued)

- If c is high and d is low, then the voltage from the left side of the comparator is equalized to voltage reference Vref.
- The same can be said for the right side of the comparator if c is low and d is high.
- Looking at the timing diagram we can see that as the right voltage line crosses Vref the comparator output and ASMD output go high and low when it crosses again.

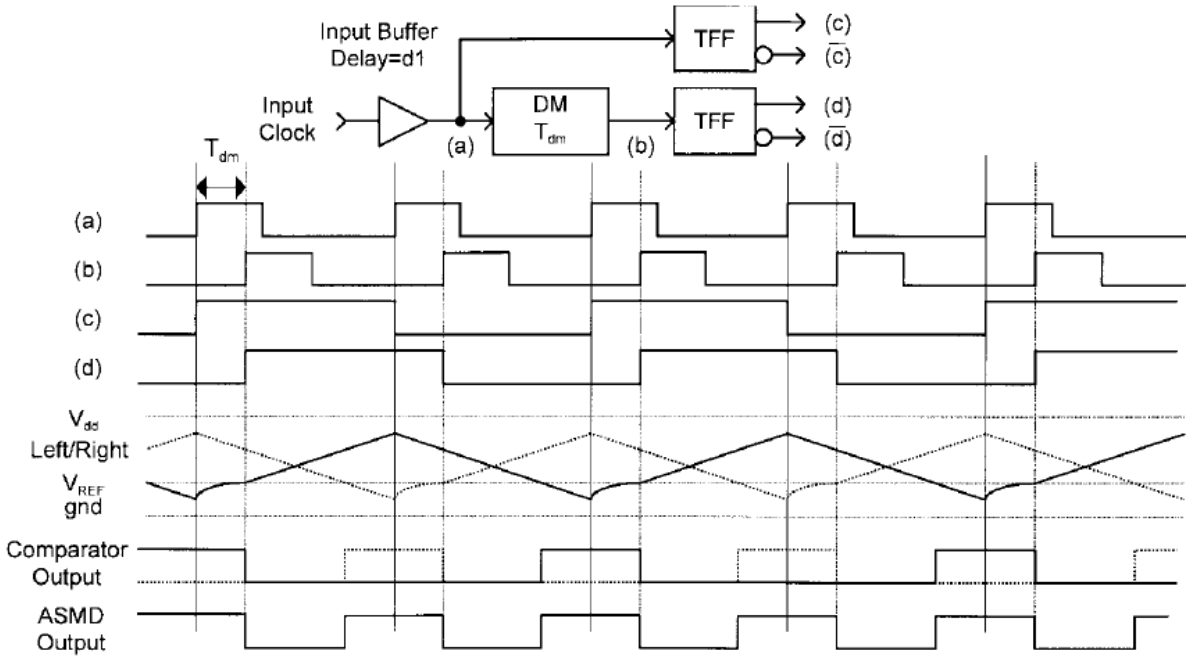
AMSD Timing Diagram



Operation of ASMD (continued)

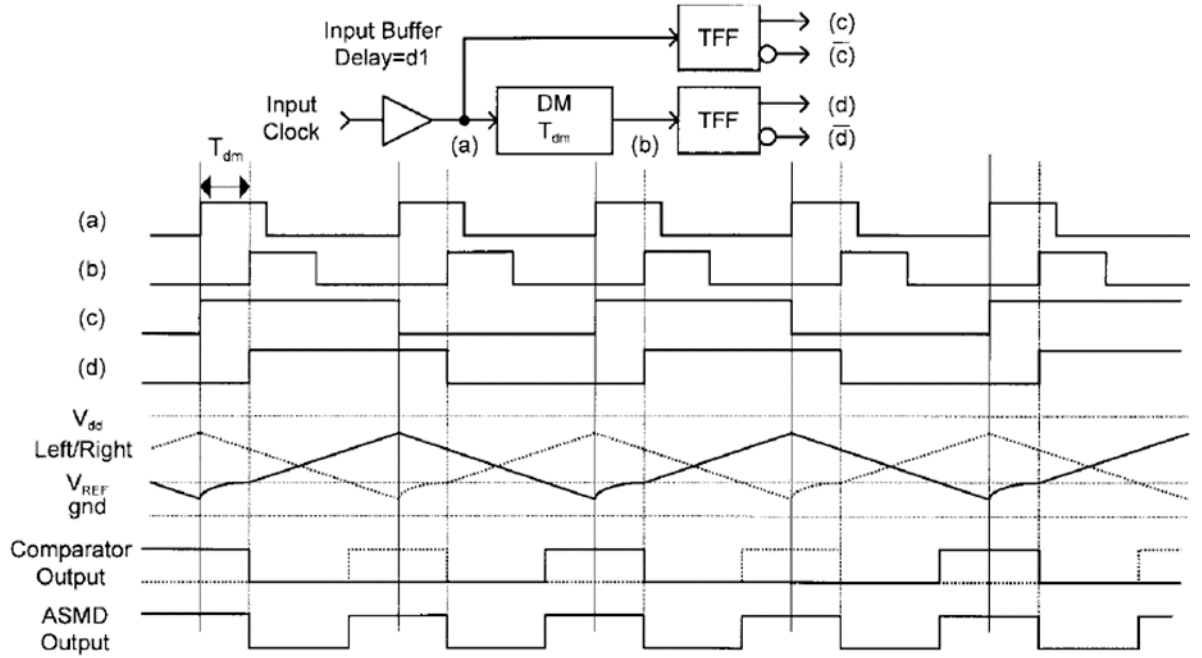
- Once both c and d are high the voltages on the left side are pumped up to Vdd.
- The same happens to the right side when c and d are both low.
- Looking at the timing diagram again we see that when the left voltage crosses Vref the output goes high and then when it crosses again it goes low for the comparator and ASMD.
- This process repeats itself for the rest of the clock period.

AMSD Timing Diagram



Operation of ASMD (continued)

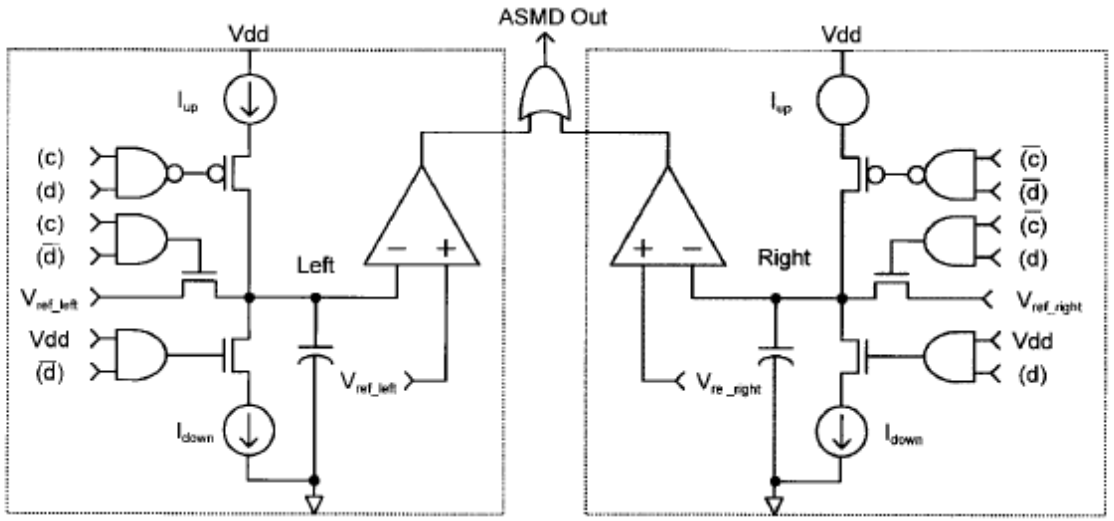
- If c goes low, then the voltage on the left side is being discharged to ground and the same can be side if c is high then the right side is discharged.
- The time that it takes the left and right voltage to discharge to Vref and then charged to Vref is used to create the pulse of the ASMD output which is the generated output clock.



ASMD Circuit

- The AMSD circuit is comprised of the CP, comparator, AND gates, NAND gates, PMOSs, NMOSs and capacitors.
- The AND along with the NAND gates help control the logic of the circuit with when to pump, discharge, or equalize the voltage on the left and right side of the comparators. While the PMOSs and NMOSs are used as switches to control the flow of current from the capacitors.
- In order to implement the CP and comparator different circuit designs are needed then what is seen here which we'll be discussed next slides.

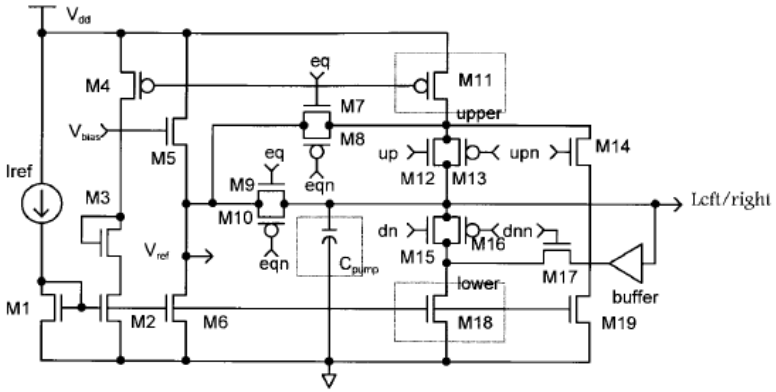
ASMD CP and Comparator Circuit



ASMD Circuit (continued)

- The CP circuit works by having the transistors M1–M4, M11, and M18 control the pumping of the current sources. The capacitor Cpump can equalize to Vref and charge up and down to make the signal go left or right. To reduce voltage spike when the transistors switch, M7, M8, and the buffer are used to initialize the upper and lower nodes to known voltages.
- The value of Cpump and the current level are determined by the maximum and minimum charging time.

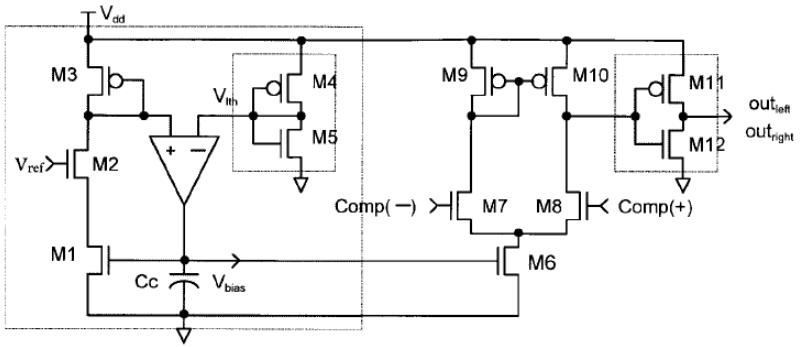
CP Implementation



ASMD Circuit (continued)

- The comparator for ASMD must have small conversion delay and high gain to generate an output clock pulse.
- To achieve this a single stage differential pair and CMOS inverter are used for a high gain stage. The single-ended output voltage of the differential stage is used as the logical threshold voltages of M3 and M4, when the inputs of the comparator cross.
- The negative feedback of the op-amp helps deal with the effects of process and operating condition variations.

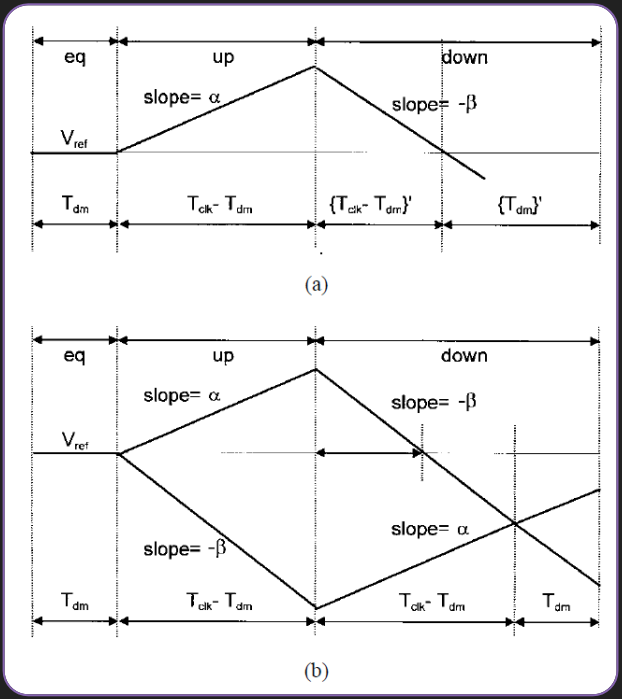
Comparator Implementation



ASMD Design

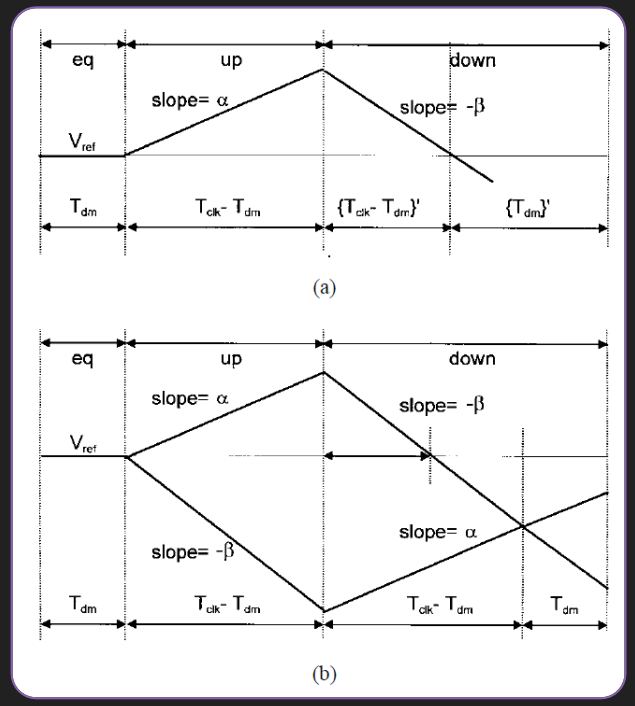
- When designing an ASMD there are only a few things to account for one of them is the frequency the ASMD will operate at.
- Next is the value of the pumping current Ipump that we'll want to use in the design.
- Next is the value of the capacitors for the left and right side of the comparators which can be solved with the equation C = (Ipump*Tck)/ VDD.
- For example, let's say we want to design an ASMD that operates at 200 MHz (Tck = 5 ns) with a VDD of 1 V and Ipump of 10 uA.
- Using the formula C = (10 uA* 5 ns)/ 1 V = 50 fF
- We can also figure out the charging rate for the capacitor with all the information given where dv/dt = Ipump/C = 250 mV/ 1ns which is measured by the circuit and used to create the length of the pulse for the output of the AMSD.

ASMD Dual Pumping Scheme



- So far, the we have been covering an ASMD with a single pumping scheme and there are drawbacks the ASMD suffers from when using it ((a) is the single pumping scheme and (b) is the dual pumping scheme).
- A single pumping scheme suffers from matching issues from the NMOS and PMOS in the current mirror of the charge pump and PVT variations.
- To fix these issues we can implement an ASMD with a dual pumping scheme meaning two charge pumps per comparator.

ASMD Dual Pumping Scheme (continued)



- It uses upper and lower triangular waveforms rather than one and a reference voltage Vref. The ASMD output is generated using these two waveforms as inputs to the comparator.
- The operation of the dual pumping scheme is during equalization, the voltages of two waveforms are initialized to Vref. Then, during the charging phase, one waveform, we'll call A, is charging up and another waveform , B, is charging down. The opposite is true during discharging, as A goes down and B goes up, and a crossing point is made.
- Using the symmetry of the waveform, the crossing time of two waveforms always coincides to the value of (Tck – Tdm), regardless of the levels of two current sources.

ASMD Dual Pumping Scheme (continued)

$$\Delta t_{\text{dual}} = \frac{(\Delta\alpha + \Delta\beta) \cdot \{T_{\text{CLK}} - T_{\text{dm}}\}}{(\alpha + \beta + \Delta\alpha + \Delta\beta)}$$
$$\Delta t_{\text{single}} = \frac{(\beta + \Delta\beta - \alpha) \cdot \{T_{\text{CLK}} - T_{\text{dm}}\}}{(\beta + \Delta\beta)}.$$

- We can see how these schemes affect the timing behavior by considering the current deviation due to a drain-source voltage dependency. By defining a and β as the charging slopes of A and B during charging. The output resistance of a MOS transistor causes the discharging slopes to become α+Δα and β+Δβ. The amount of time shift can be expressed ,for dual pumping and single pumping schemes, in the equations to the side.
- We can see the improvement that the dual scheme provides as the time shift with a single pumping scheme depends on the absolute number of current errors, while in a dual pumping scheme it depends only on relative errors, which means it is more tolerant to device mismatches.

ASMD Benefits and Drawbacks

Benefits

- No quantization error
- Short lock time
- Accepts input clocks with a duty cycle equal to or greater than 50%.
- Can be used at lower frequencies since layout size is not dependent on the frequency.
- Tolerant to device mismatches (Dual pump scheme).

Drawbacks

- Requires a bias circuit for the charge pump.
- Consumes more power due to comparator and charge pump.
- Timing mismatches from NMOS and PMOS in the charge pump (Single pump scheme).
- Circuit can be affected by PVT variations (Single pump scheme).

References

- Tu, Y. H., Cheng, K. H., Lin, Y. A., & Huang, H. Y. (2015). A Synchronous Mirror Delay with Duty-Cycle Tunable Technology. *2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems*, 79–82. https://doi.org/10.1109/ddecs.2015.29
- Kuo-Hsing Cheng, Chen-Lung Wu, Yu-Lung Lo, & Chia-Wei Su. (2005). A Phase-Detect Synchronous Mirror Delay for Clock Skew-Compensation Circuits. *2005 IEEE International Symposium on Circuits and Systems*, 1070–1073. https://doi.org/10.1109/iscas.2005.1464777
- Hung, C. L., Wu, C. L., & Cheng, K. H. (2006). Arbitrary Duty Cycle Synchronous Mirror Delay Circuits Design. *2006 IEEE Asian Solid-State Circuits Conference*, 283–286. https://doi.org/10.1109/asscc.2006.357906
- Daeyun Shim, Dong-Yun Lee, Sanghun Jung, Chang-Hyun Kim, & Wonchan Kim. (1999). An analog synchronous mirror delay for high-speed DRAM application. *IEEE Journal of Solid-State Circuits*, *34*(4), 484–493. https://doi.org/10.1109/4.753681
- Chae, J. S., Kim, D., & Kim, D. M. (2000). Wide range single-way-pumping synchronous mirror delay. *Electronics Letters*, *36*(11), 939. https://doi.org/10.1049/el:20000711
- Baker, J. R. (2019). *CMOS: Circuit Design, Layout, and Simulation (IEEE Press Series on Microelectronic Systems)* (4th ed.). Wiley-IEEE Press.