Getting Started with WinLASI:

Whilst this document is not intended to teach you how to do IC design, nor is it intended to replace the LASI Help files available in each tool menu, it should however, allow you "to get up and running" with relative ease. Working through this document will take about 2 days.

When you are finished you should be quite comfortable with using WinLasi and be able to carry through a basic Analogue Full-custom Design Flow.

Contents:

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1. Setting up WinLASI (and WinSPICE3)

Download WinLASI and WinSPICE3 from:

http://cmosedu.com/cmos1/winlasi/winlasi.htm
http://www.willingham2.freeserve.co.uk/winspice.html

and follow the setup instructions given on those sites. Also read WinLASI update info at:

http://members.aol.com/lasicad/

These programs are provided free of charge to private individuals. If you intend to use these programs for commercial purposes please pay the licensing fees. They are extremely good value for money, but will only remain so if we all support the people who have given so much of their time to developing these programs for us to use.

[My Documents] [Tools] [Folder Options] [File Types] [New] enter .cir [OK] [Change] [Other] search for winspice3.exe (To be found in C:\Program Files\WinSpice\ in my setup) accept and close.

Repeat setup for WinSPICE to read .tlc .bp6 and .cl6 files.

Setup WordPAD (in C:\Program Files\Windows NT\Accessories) to read .rpt .hdr .ftr .ldm .nod and .usf files.

If you decide to run more than one version of WinLASI (eg Version 6.2, version 6.3.2.2 and version 7.0.0.0 Beta) you may choose to set up V7 to open .tlc and V6.3 to read .bp6 and version 6.2 to read .cl6 files.

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2. Setting up a new design

How to start a new design is not immediately obvious in WinLASI: if a new directory is created, then a .tlc file copied into it using Explorer it will be found that the layouts will come up with lines only. Sometimes when downloading new examples you will find that the layers do not appear.

To correctly copy the setup files, or to "install" the layer file correctly, use explorer, then go to a library which contains the correct technology for your design [eg the WClib library) pick the highest level cell to be copied [eg Top.bp6] open with Wlasi.

Then use:

[Sys] [Clone]

enter the path to the new directory to be created, eg:

E:\Documents and Settings\All Users\Documents\WinLASI\SCRATCH\Invertor

TIP: Click in the "Address" box in Explorer to select the path the select [Edit] [Copy,] the click in the "path" box in the Clone window and press cntrl+c. This will save re-typing the whole path.

Add any new directory branch to the path.

-if the directory already exists you will get the message "directory exists", when you pick [OK], ignore this, you will see that a new Lasi6.usf file has appeared in the target directory.

Leave the Lasi window on the source directory open, go to the target directory and select the .usf file, open a new lasi window. This will be empty and you should see a Cells6.dbd file appear in the target directory.

In the source (Lasi) window, pick [List] then choose an example cell to be copied over (eg Invf101.bp6). Choose [TLCout] [Browse] then locate the target library. Type in the cell name (INVF101) into the filename box pick [Open]. You should now see the TLCout Setup window with the correct destination path and cellname in it. Pick [OK] [Yes] [OK] in response to the windows which pop up.

You should now see four files in the target directory; a {layers}.tlc and a Invf101.tlc file should have appreared.

In the target Lasi window, choose [TLCin] [Browse] locate the destination directory (ie the target directory above) when found, you should see just the two .tlc files above. Pick Invf101.tlc [Open] [OK] the invertor cell should now appear correctly (ie the polygons are "filled" rather than "outlines") in the target Lasi window.

You should now see nine files in hte destination directory; the five new files are: Invf101.bp6 Cellbkup.bp6 Cellbkup.cl6 Mainbkup.bp6 Mainbkup.cl6

Repeat the process to copy over the schematic .tlc file, Invf101_sch.tlc.

There should now be eighteen files in the target directory. Invf101_sch.bp6 Invf101_sch.cl6 Nmos_sch.tlc Pmos_sch.tlc Nmos_sch.bp6 Pmos_sch.bp6 Gnd_sch.tlc Gnd_sch.bp6 have now appeared in the directory.

TIP: move the browse window when copying over the cell to reveal the cell name. Use "fit" in the main Lasi window to see the schematic file.

Close the source Lasi Window. You should now be ready to look at LasiCkt and then LasiDRC.

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3. Setting up netlist extraction from schematics using LasiCKT

Choose the appropriate .bp6 file (eg Invf101_sch.bp6 in the above target directory) open with Lasi, then choose [Sys] [LasiCKT] [Setup] [List] choose INVF101_SCH ignore Header, Footer and Alias files for the moment.

Return to the schematic window select [layr] in Menu 1, you will see a list of all of the layers with one checked (probably layer 1 ARRW). Note the layer numbers for NTXT CTXT DTXT PTXT (probably 4, 5, 6 and 7).

Go to the Compile Setup window and enter these numbers into the Node, Connector, Device and Parameter text boxes respectively:

```
Special Text Layers:

Real Node Text Layer 4        Device Name Text Layer 6
Connector Text Layer 5        Parameter Text Layer   7
```

```
Options:

[v]Report Floating Cells        [ ]Report Virtual Nodes
[v]Report Multiple Connections  [v]Report Counts
```

```
               Rules ( ) Circuit (o) Schematic]

Name of Error File: Lasickt.rpt            [OK]
```

Next we have to set up the interlayer connectivity. This is done with the Trace table: [Sys] [LasiCKT] [Trace]

Go back to the schematic window, click-on [Get] then select some of the blue interconnecting lines on the schematic, then click-on [Info]. There will be a layer reported in that box. For this example it is layr=MET1(49)

Enter 49 in the Conductor 2 box in the Trace Table window. [OK] [Go]

- the extraction routine should run, then report:
"Completed ...0 Errors 0 Warnings"

- if you get a lot of errors and warnings (8 Errors) for this example, then you have not entered the correct layer in the step above. Notice that you can enter this number on any conductor layer and the netlist extraction from the schematic will still work. However when we get to the netlist extraction from layout, this will need to be entered into the correct conductor layer. some schematics may use another layer (possibly layer 3 SCHM) to avoid this complication and possible area for making errors.

Note: there are now 22 files in this directory: Invf101_sch.cir Invf101_sch.nod Lasickt.rpt LasiCkt.usf have just appeared.

Choose [Read] [Browse] then locate the target directory and

Invf101_sch.cir [Open] [OK]. You should then see a SPICE netlist as follows:

```
*** SPICE Circuit File of INVF101_SCH made by LASICKT 08/10/02 16:03:28

*MAIN INVF101_SCH IN OUT
M1 OUT IN VDD VDD CMOSPB L=2u W=13u
M2 OUT IN 0 0 CMOSNB L=2u W=4u
.END
```

Now we shall return to the header and footer files: copy the following into two separate text files, then save the first as Invf101.hdr, the second as Invf101.ftr.

```
************************* Invf101 Test-Bench *************************

  Vdd  VDD 0 2V AC 0
  Vcm  A   0 1V AC 0

***************************** Input Drive ****************************
*    NB V2=Vdd                 V1  V2  td   tr   tf    Pw    Per
*                               |   |   |    |    |     |     |
  Vdm In A DC 0 AC 1 PULSE(-0.3 0.3  0ns  1ns  1ns 100ns 200ns)

************************* End of Test-Bench **************************



************************* Invf101 Footer File ************************
************************* Library Definition *************************
Level 2 model nchan model for Orbit CN20
.MODEL CMOSNB NMOS LEVEL=2 PHI=0.6000 TOX=4.3500E-08 XJ=0.200000U TPG=1
+ VTO=0.8756 DELTA=8.5650E+00 LD=2.3950E-07 KP=4.5494E-05
+ UO=573.1 UEXP=1.5920E-01 UCRIT=5.9160E+04 RSH=1.0310E+01
+ GAMMA=0.4179 NSUB=3.3160E+15 NFS=8.1800E+12 VMAX=6.0280E+04
+ LAMBDA=2.9330E-02 CGDO=2.8518E-10 CGSO=2.8518E-10 CGBO=4.0921E-10
+ CJ=1.0375E-04 MJ=0.6604 CJSW=2.1694E-10 MJSW=0.178543 PB=0.800000

* Level 2 model pchan model for Orbit CN20
.MODEL CMOSPB PMOS LEVEL=2 PHI=0.6000 TOX=4.3500E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8889 DELTA=4.8720E+00 LD=2.9230E-07 KP=1.5035E-05
+ UO=189.4 UEXP=2.7910E-01 UCRIT=9.5670E+04 RSH=1.8180E+01
+ GAMMA=0.7327 NSUB=1.0190E+16 NFS=6.1500E+12 VMAX=9.9990E+05
+ LAMBDA=4.2290E-02 CGDO=3.4805E-10 CGSO=3.4805E-10 CGBO=4.0305E-10
+ CJ=3.2456E-04 MJ=0.6044 CJSW=2.5430E-10 MJSW=0.244194 PB=0.800000

***************************** Simulations ****************************
  .OP
  .DC Vdm -0.3 0.3 0.5m
  .AC DEC 11 1k 1000MEG
* .NOISE V(out) Vdd DEC 11 1 10MEG
  .TRAN 0.2n 3u UIC

************************ Commands for Spice3 *************************
.OPTIONS METHOD=GEAR ITL5=0  RELTOL=0.001  ABSTOL=1n VNTOL=1m
*#destroy all
*#run
.CONTROL
```

```
    where
.ENDC

********* SPICE3 & NUTMEG Commands, run from within WinSPICE3 *********
* Note to switch command on:  *#PLOT ...
*      to switch command off: * PLOT ...
*************************************************************************
*#PLOT  dc1.V(out)#branch
*#PLOT  db(ac1.v(out)) ph(ac1.v(out))
* PLOT mag(ac1.v(out)) ph(ac1.v(out))
* PLOT I(Vdd)
*#PLOT V(In) V(out)
* PLOT onoise loglog
********************** End of Invf101 Footer File ********************
```

NOTE: the device Models used here are simple ones which allow simulations to run. Ideally level 8 (level 49) models as provided from the foundary should be used, however to do so would require us to write the area, periphery and resistance rules for the layout based on the width and length of the devices to ensure junction cappacitances and drain and source resistances are correctly extracted. By using the Level 2 models we can avoid that issue for the moment. We will return to this later.

Go To the Compile Setup window in [Sys] [LasiCKT] [Setup] and enter the header file as Invf101.hdr the footer file as Invf101.ftr [OK] Click on [GO] to create the netlist which should be ready for simulation. If you have WinSPICE3 set up, you can just locate the Invf101_sch.cir file and double click on it and the simulation runs.

You should then see three plots, the first is the input/output DC transfer function, the second is the open loop AC gain and phase, the third is the transient response.

TIP: always add a <return> at the end of the header and footer files, otherwise the compiler joins the next line and causes and error in SPICE.

You should now have 24 files in this directory.

---

4. Setting up netlist extraction from layouts using LasiCKT

The original setup files for WinLASI were for SCNA (Scalable CMOS N-well Analog) technology with a lambda of 1.0. Unfortunately this technology (Orbit's 2.0 um CMOS) is no longer available, so we have to modify the default files to set them up for a new technology. Presently this is SCN3M_SUBM (SCalable N-well 3 Metal layer SUBMicron features) details can be found at:

http://www.mosis.org/Technical/Designsupport/mosis-design-example.html

Fortunately we can "re-use" the earlier layout libraries with a Lambda scaling of 0.30. This variant of SCMOS corresponds to the Agilent/HP 0.50um CMOS process. This allows us to reuse the typical N91B SPICE models from the web site in our simulations.

Note: these have not been used in the above footer file.

Choose the appropriate .bp6 file (eg Invf101.bp6 in the above target directory) open with Lasi, then choose [Sys] [LasiCKT] [Setup] [List] choose INVF101, leave Header, Footer and Alias files blank for the moment. Choose (o) Circuit Rules [OK]. Go to the Trace Table [Trace] Enter the following:

```
Conductor 8
   ....
Conductor 5   51        M3
Insulator 4   50        Via2
Conductor 4   51        M2
Insulator 3   50        Via1
Conductor 3   49        M1
Insulator 2   25        Contact (poly or active)
Conductor 2   56        Poly2
Insulator 1   47  48    Poly2 Contact, Active Contact
Conductor 1   46        Poly1
```

These are the interconnect layers referred to in "CMOS Circuit Design, Layout and Simulation" page 157, as defined for this process. Also see NEWLASICKT.pdf

Ignore the capacitances in the Trace Table for the moment, we shall return to these later on.

Add the following cellnames to the Smash List under [Smash]:

```
PAD
VIA
CONTACT
SFRAME
```

TIP: Layers used in a cell maybe checked with: [Sys] [Show] [List] then pick the cell of interest by double clicking on it, then [OK] by scrolling down the table presented you can see how many boxes, paths or text labels have been added on each layer. For our example here, there are:

```
0 boxes and 0 paths and 2 text entries on layer 5  (CTXT)
8 boxes and 8 paths and 0 text entries on layer 25 (CONT)
0 boxes and 1 path  and 0 text entries on layer 42 (NWEL)
1 box   and 3 paths and 0 text entries on layer 43 (ACTV)
1 box   and 1 path  and 0 text entries on layer 44 (PSEL)
1 box   and 1 path  and 0 text entries on layer 45 (NSEL)
0 boxes and 1 path  and 0 text entries on layer 46 (POL1)
0 boxes and 4 path  and 0 text entries on layer 49 (MET1)
2 boxes and 0 paths and 0 text entries on layer 50 (VIA1)
2 boxes and 0 paths and 0 text entries on layer 51 (MET2)
```

Layer tables for each technology can be found in the Form.dbd file for this technology the file looks like this:

```
; FORM.DBD for SCN3M_SUBM design rules, based on original file by
; Aaron Huntsinger and Jake Baker, 1996
; Modified for Agilent/HP 0.5um Process (HP_AMOS14TB) SLFH 11 Aug 02.

layer=arrw  1     ;layer used to draw arrows in schematics
layer=otln  2     ;Cell outline layer
layer=schm  3     ;Schematic layer used for drawing circuit schematics
layer=ntxt  4     ;used to label nodes for LASI to SPICE list, LASICKT
layer=ctxt  5     ;labels contacts so LASICKT knows order, i.e., D G S
layer=dtxt  6     ;gives device number such as M1 or M55 etc.
layer=ptxt  7     ;used to specify part type, model size etc.

layer=cont 25     ;contact
layer=pads 26     ;pads
layer=sblk 29     ;salicide block (additional for HP_AMOS15TB)
layer=pwel 41     ;p-well            (Not used in HP_AMOS14TB)
layer=nwel 42     ;n-well
layer=actv 43     ;active
layer=psel 44     ;pselect (or P+ diffusion)
layer=nsel 45     ;nselect (or N+ diffusion)
layer=pol1 46     ;poly 1
layer=pcon 47     ;poly contact   (additional for HP_AMOS15TB)
layer=acon 48     ;active contact (additional for HP_AMOS15TB)
layer=met1 49     ;metal 1
layer=via1 50     ;via connection between metals 1 and 2 (contact cut)
layer=met2 51     ;metal 2
layer=ovgl 52     ;overglass; cut openings for pads in top passivation
layer=pol2 56     ;poly 2            (Not used in HP_AMOS14TB)
layer=pbas 58     ;pbase             (Not used in HP_AMOS14TB)
layer=cwel 59     ;cap well          (Not used in HP_AMOS14TB)
layer=via2 61     ;via 2, metal2 to metal3 (contact cut)
layer=met3 62     ;metal 3
```

The layers labelled (not used) are legacy layers from earlier designs and probably should be left in to allow you to view any invalid boxes or paths on those layers. Layers labelled (additional) have been added to the earlier technology file. [View] will allow you to select the "All layer" mode; follow with [Draw] to see layers selected.

Copy this text to a file named Form.dbd and save it in the target directory. You should now be able to read this file by clicking on [Read] in the layout window, then scrolling down the "File to Read" menu then double clicking on FORM.DBD [OK].

You should now have 25 files in your target directory.

Next go to [Menu2] [Set] [Layers] then check that all the layers are present add/delete as necessary to match the above table, edit as necessary [Save] [OK].

Now you are set to try extracting a netlist from the target layout cell. First you have to create a second rank cell into which you can place the invertor cell to extract the subcircuit for the Invf101 layout. As the original layout has been generated for use with a digital simulator (which uses U-type primitives) you will have to create the text to be extracted from the layout.

We are going to generate a new cell from an existing library.

[Cell] double click Invf101(1) [OK]. Click [Save] then type "Invertor" in the cellname box [OK]. [Sys] [ReRank] [List] double click Invertor(1) [OK] enter 2 in New Rank box [OK].

Return to schematic window [Cell] double click Invertor(2) [OK].

You should now have 27 files in the directory; Invertor.bp6 and Invertor.cl6 have just appeared.

Now comes the interesting part - open Invf101 as PMOS13W2L and as NMOS2W6L. Switch to each of these cells and edit them down to just the PMOS and NMOs parts only, add connector text for DGSB on the PMOS and DGS on the NMOS. Return to Invf101 and remove the parts relating to the NMOS and PMOS devices; replacing them with the PMOS6W2U and NMOS4W2L rank 1 cells. Remember to add a Contact (25) and covering M1 (49) box inside the n-well of the PMOS rank 1 cell, then connet M1 in the rank 2 Invertor cell to VDD. Add Device and parameter text over the PMOS and NMOS cells in the rank 2 Invertor cell.

[Sys] [LasiCKT] [Setup] [List] select INVERTOR. Remove the header and footer file names for now [OK]. [GO] then [OK] on the error box that appears. [Read] select LasiCKY.rpt [OK]. When you have solved all the problems you have created and in the process learnt how to use the layout editor, you should see a "clean" error file like this:

```
*** Compile Error List for INVERTOR made by LASICKT 08/14/02 17:22:45

[MAIN CIRCUIT] INVERTOR
Counts:             Nodes                       Connectors
Devices (Real Virtual Symbol Total)(Count  Real Virtual Symbol Total)
     2     3       0      0     3      7     7       0      0     7

Completed ... 0 Warnings  0 Errors

Finished: 08/14/02 17:22:50
```

You should also get a SPICE netlist as follows:

```
*** SPICE Circuit File of INVERTOR made by LASICKT 08/18/02 22:29:53

*MAIN INVERTOR VSS VDD In Out
MN1 Out In VSS VSS NMOS W=4u L=2u
MP1 Out In VDD VDD PMOS W=13u L=2u
.END
```

TIP: Move the placement of the text around until it is read correctly into the netlist for both the subcircuit header as well as the device nodes.

Note: You will have to add an N+ Implant with an Active insert inside the N-well of the PMOS and a P+ Implant with an active insert near the NMOS device to connect the Tub and Sub to Vdd and Vss respectively. These have been missed on the Invf101 cell as they were drawn at a higher level in the CMOS library. For Analogue designs it is "good practice" to make the body connections for all the MOS within the cell, locally.

You should now have at least 31 files in this directory; the new files are: PMOS13W2L.bp6, NMOS4W2L.bp6, Invertor.nod and Invertor.cir. An odd Loadbkup.tlc file may have appeared making the file count 32.

To tidy up: [Sys] [Kill] [List} choose INVF101(1) [OK] leaving 31 files.

---

5. Setting up Layout Versus Schematic checking using LasiCKT

Start WinLASI in the above Invertor directory. [Sys] [LasiCKT] [Comp]

then enter:

```
 First Node List File: Invertor.nod
Second Node List File: Invf101.nod
 Base Name of Circuit: Invertor
   Name of Error File: Noderror.rpt
```

[Compare]

You will get the report: "Nodelist of INVERTOR is not in Invf101_sch.nod"

If you open the two files you will see that the subcircuit name is different, edit [INV101_SCH] to [INVEERTOR_SCH] in the Invf101_sch.nod file, then save it.

[Compare] now you will get a report like this:

```
*** Node Compare Error List made by LASICKT on 08/18/02 23:05:51

Comparing Invertor.nod to Invf101_sch.nod
Connection MN1.2 on Node In: is not on expected Node ?
Connection MN1.1 on Node Out: is not on expected Node ?
Connection MP1.3 on Node VDD: is not on expected Node ?
Connection MN1.3 on Node VSS: is not on expected Node ?
Comparing Invf101_sch.nod to Invertor.nod
Connection M2.3 on Node 0: is not on expected Node ?
Connection M1.2 on Node IN: is not on expected Node ?
Connection M1.1 on Node OUT: is not on expected Node ?
Connection M1.3 on Node VDD: is not on expected Node ?

Finished ... 8 Errors
```

Which is sort of obvious as the two circuits really are not the same ...

You wil find you now have 33 files in the directory. A file called Noderror.rpt has appeared as may have a file called Undobkup.tlc. Noderror.rpt is the example above.

Load Invf101_sch and save as Invertor_sch
Load NMOS_sch and save as PMOS13W2L_sch
Load PMOS_sch and save as NMOS4W2L_sch
Kill NMOS_sch, PMOS_sch, Invf101_sch and Gnd_sch.

When you load Invertor_sch agian you will find the sub cells missing. Re-place PMOS13W2L_sch and NMOS4W2L_sch on the Invertor Schematic and edit it until you get a clean LVS report.

Remember to change the connector numbering sequence for Vss, Vdd, In and Out nodes. Change Device names to MP1 amd MN1, change parameters

to "PMOS W=13u L=2u" and "NMOS W=4u L=2u", relabel what was Gnd to Vss.
Connect the body nodes to Vdd and Vss.

[Sys] [LasiCKT]

Change the files to be compared:

 First Node List File: Invertor.nod
Second Node List File: Invertor_sch.nod
 Base Name of Circuit: Invertor
   Name of Error File: Noderror.rpt

[Compare] should produce the Noderror.rpt file:

*** Node Compare Error List made by LASICKT on 08/18/02 23:58:02

Comparing Invertor.nod to Invertor_sch.nod
Comparing Invertor_sch.nod to Invertor.nod

Finished ... 0 Errors

Edit Invf101.ftr and Invf101.hdr to Invertor.hdr and Invertor.ftr
Remove all of the Invt101.xxx files left in the directory, as well as
the Gnd_sch.tlc NMOS_sch.tlc and PMOS_sch.tlc files.

You should now have 27 files in the directory, Invertor_sch.bp6
Invertor_sch.cl6 Invertor_sch.cir and Invertor_sch.nod have appeared.

You should by now be quite comfortable with using the schematic editor
and layout editors.

To prepare for the next section, re-run LasiCKT for both Invertor and
Invertor_sch including Invertor.hdr and Invertor.ftr in their .cir
files.

Remember to edit the Footer file to change the model names from CMOSNB
to NMOS and CMOSPB to PMOS. Also remember to add the line
"Rss VSS 0 1u" to the header file to replace the internal Ground
connection removed above.

Double click on both .cir files to simulate (if you have WinLASI setup
to do so) compare the simulated results. They should be identical.

---

6. Setting up Capacitance extraction using LasiCKT

Once you have a schematic and layout extraction setup to run in spice, you can set up the parasitic capacitance extraction.

from the layout window [Sys] [LasiCKT] [Setup] choose Invertor and circuit rules. [Trace] then enter the following values:

			C2Gnd	C2L+1	C2L+2	C2L+3	C2L+4
Conductor 5	51		0.011				
Insulator 4	50			0.042			
Conductor 4	51		0.016		0.015		
Insulator 3	50			0.042		0	
Conductor 3	49		0.031		0		0.010
Insulator 2	25			0		0.017	
Conductor 2	56		0		0.059		
Insulator 1	47	48		0			
Conductor 1	46		0.098				

click the (o)fF "button"

TIP: WinSPICE3 does not recognise aF.

Check the "[v] Node to Gnd Caps" box
and the "[v] Node to Node Caps" box. [OK]

Edit Invertor.hdr adding the following line:

```
Rin A B 1k
```

then edit the common mode source to say:

```
Vcm  B   0 1V AC 0
```

re-netlist both Invertor.cir and Invertor_sch.cir, Double click on Invertor.cir and on Invertor_sch.cir in the target directory to simulate. Compare the results, you will see a slight difference:

Invertor_sch (the ideal) will have a bandwidth of about 140Mz and a risetime of around 3ns, whereas Inveror (with parasitics) will have a bandwidth of about 100MHz and a rise time of about 5ns.

TIP: use version 6.2 or 7.0 for extracting the node to node capacitances, for some reason it does not work in version 6.3.2.2

To use version 7 you will have to do a TLCout from one of the version 6 LASIs. Once you have used version 7 you will have 33 files in the directory, the new files are: Lasi7.usf Cells7.dbd Swap.bpv Invertor.tlc Nmos4w2l.tlc and Pmos13w2l.tlc

TIP: values for N91B process to enter into theTrace Table can be obtained from:

www.mosis.org/Technical/Designsupport/mosis-design-example.html#Prelated

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Setting up 3D viewer using LasiDRC:

Once a layout is available [SYS] [Lasi3D] [Setup] enter layers into the Layer List:

1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
46	**47**	**56**	**25**	**49**	**50**	**51**	**61**
9	**10**	**11**	**12**	**13**	**14**	**15**	**16**
62							

Then Browse for Inveror.tlc [OK] [Go]

Return to the main Layout window, [TLCin] [Brwse]pick Invertor_3D.tlc [Open] [Ok] [Ok]. You should see an angled isometric 3D plot of the layers in just the invertor cell. Lower rank cells are not shown.

There are now 37 file in the target directory, the four new files are Lasi3D.usf Invertor_3D.tlc Invertor_3d.bp6 and Invertor_3d.cl6

---

7. Setting up Design Rule Checks using LasiDRC

From the layout window [Sys] [LasiDRC] [Setup] [List]
choose "Invertor" [OK] [Browse] then search for Mosissubm.drc (in my setup it is in the MOSIS directory). For older versions you will have to use the older rules to be found in the WMOSIS directory and will be called Mosis.drc

[Open] [Ok] [Go] [Ok] [Read] pick LasiDRC.rpt.

TIP: if this is the first time running version 6.3.2.2, you will have to add the full path to the reader box to avoid the "Cant find Reader Program" error message. In my setup it is at C:\WINNT\notepad.exe
you should then see a report like this:

*** LASI Design Rule Check Flag Report

Cell: INVERTOR
Check 1: 1.1 Well width >=10 lam (1)
Date: 08/21/02 Time: 12:31:36
Resolution= 1um Distance= 10um ScaleRatio= 1 MapSize= 1
Area(s) Flagged:

Completed ... 0 Total Flags

Finished: 08/21/02 12:31:37

[Setup] enter 102 in the "Finish Check [ ]" box, select [Fit} to fit DRC area to cell selected [OK] [Go] ..... [OK]
[Read] pick LasiDRC.rpt [OK]

Examine the errors reported. What they are will depend upon how well you drew the Invertor layout above (Mine gave three errors). The error messages will appear under the line "Area(s) Flagged: " (see above listing)

WARNING: cells such those in the "CMOS circuits" directory were written for the Mosis.drc rules in the WMOSIS library. They will fail some of the MosisSubm.drc rules used here, so the cell(s) will need editing accordingly.

The messages I got were:

Check 12:
Area= Zoom -36.65 -3.7 475.35 316.3 Map= INVERTOR_12_1.PCX

Check 15:
Area= Zoom -36.65 -3.7 475.35 316.3 Map= INVERTOR_15_1.PCX

Check 25:
Area= Zoom -34.65 -1.7 477.35 318.3 Map= INVERTOR_25_1.PCX

TIP: use [Edit] [Find] then enter the word "zoom" in hte Notepad report will assist in finding which rules have been compromised. You can of

course go to that area of the layout to see what the object is.

We now have 42 files in the directory, the new ones are:
LasiDrc.usf Lasidrc.rpt and the design rule "error" files
Invertor_12_1.pcx Invertor_15_1.pcx Invertor_25_1.pcx

In the LasiDRC window, [Sys] [LasiDRC] pick [Map] you will then see a list of .pcx files (for me those three listed above). Pick one [Open].

You will see a window with simplified representations of the cell(s) being checked, the error are highlighted in white, the specific error here is select width is less than 4 lambda and occurs in both NMOSW4L2 and PMOS13W2L. You will notice that in the Map window, next to the check number there will be a line of text telling you the rule file number and short descripton of the rule being violated (for this example it is "4.4 Minimum select overlap and spacing ...".

To help understand the error, there are a number of Rulexx.tlc files in the MOSIS directory. Start by loading AllMOSIS.tlc. This is a Rank 2 cell which reads all the Rulexx.tlc files as Rank 1 cells. Scroll around until you locate (Check 12) which is to be found in (Rule4.tlc) [List] double click Rule4(1) [Fit]

Compare this layout with the earlier one you have made.

TIP: to make the (n-select) clear go to [Ldrw] check "[v]NSEL 45" [OK] Sdrw will return the drawing to all layers.

(In our example, we had to move the tub tie away from the active areas on our MOS devices, as they were too close)

TIP: to save time when checking for one rule, enter its number in both the start and finish boxes.

TIP: do not rely on the pcx files appearing either through map or in the directory to flag the instance of an error. For instance check 12 above will give an error in LasiDRC.rpt, but does not generate a pcx file for the n-select and p-select boxes in the NMOS device, but does for the PMOS device.

Once you have located and edited the errors, check the "[v]Remove old PCX file" box (only available on version 6.3.2.2 or later). Re-run the DRC on all 102 checks. Verify that the word "zoom" does not appear in the LasiDRC.rpt file.

By the time you have got to here, you will have found that to meet the new design rules, you will have had to either make the active of the PMOS cell larger (thereby requiring a renaming of the cell) or that only two contacts can be fitted into the active area available.

You should now have 39 files in he directory with no PCX files once the cell(s) is (are) "DRC clean".

NOTE: it is "good practice" to re-extract the netlist from the layout and do a netlist compare whith the schematic, then re-run the simulation on the extracted circuit just to ensure there have been no compromising changes made during the DRC corrections.

---

8. Setting up a "TapeOut" from WinLASI using TLC2GDS

It is strongly recommended that you read the help files for TLC2GDS first.

[Sys] [TLS2GDS] [Help] Read it.

[Setup] enter the following ....

```
TLC File Name [Invertor.tlc      ]
GDS File Name [Invertor.gds      ]
--Layer Options-------------------------------------------------------
TLC Layer Filter (1-256) [25 26 29 41-52 56 58 59 61 62              ]
Layer Datatype Map File  [                                           ]
----------------------------------------------------------------------
GDS Library name        [DEFAULT.DB] Scale Unit LSB Correction [0     ]
GDS Units per Phys Unit [1000      ] Lambda Lenght in um [1.          ]
Default Path width      [0         ]
--Conversion Options--------------------------------------------------
 [ ]Convert Text                     [ ]Lowercase Cell Names
 [v]Check for Proper GDS IC Protocol  [v]Sort Cells in Ascending Rank
----------------------------------------------------------------------
             Report File Name [Tlc2gds.rpt   ]        [OK]
```

You will now have 40 files in the directory; Tlc2Gds.usf has just appeared.

[click [Go] in the TLC2GDS window. Reply yes to "Create Invertor.ldm file?" and yes to all of the "Map to GDS Layer [xx]" queries.

You will now have 43 files in the direcory; the new files are: Invertor.gds Invertor.ldm Tlc2gds.rpt

You should not get any conversion errors; if you do see the TLC2GDS help files for explanations.

Note the presence of Invertor.ldm   If you need to alter the layer map for a new process, erase this file, re-run the convertor, then put new numbers in the "Map to GDS Layer [ ]" box for each layer you wish to move.

The Layer Data Map should look like this:

```
*LDM built from Invertor.tlc
25,0,25
43,0,43
44,0,44
49,0,49
46,0,46
45,0,45
42,0,42
51,0,51
50,0,50
47,0,47
```

[Read]

- If this is the first time running version Tlc2gds 7, you will have to add the full path to the reader box to avoid the "Cant find Reader Program" error message.

In my setup it is at C:\WINNT\notepad.exe

[OK] to see a report like this:

```
*** TLC to GDS Conversion Report 08/22/02  12:08:55

GDS File Name: Invertor.tlc
GDS Library Drawing Name: DEFAULT.DB
GDS Scale: 1000 per um
LASI Scale: 20 per um
Rescale Ratio: 50
Lambda: 1um
Filtered Layers: 25 26 29 41-52 56 58 59 61 62

Structure                      Boundaries  Paths       Text        Srefs
-------------------------------------------------------------------------
PMOS13W2L                          20          0           0           0
NMOS4W2L                           13          0           0           0
Duplicate Vertex Removed at X=10 Y=48 L=46
Duplicate Vertex Removed at X=10 Y=48 L=46
Duplicate Vertex Removed at X=9 Y=11 L=46
Duplicate Vertex Removed at X=7 Y=11 L=46
Duplicate Vertex Removed at X=6 Y=48 L=46
Duplicate Vertex Removed at X=6 Y=48 L=46
Duplicate Vertex Removed at X=13 Y=49 L=49
Duplicate Vertex Removed at X=13 Y=49 L=49
INVERTOR                           13          0           0           2

Completed ... 3346 Bytes in GDS File
```

The resulting output file should now be in "Camera ready" GDSII format. If the file was for a whole chip, them we would have just created the "database" ready for "TapeOut".

However this was only for our Invertor example. To verify it we have to use the GDS2TLC convertor ....

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9. Reading a GDSII file into WinLASI using GDS2TLC

From the Layout window [Sys} [GDS2TLC] [Help] read the files.

To view the new tlc files and compare them to he originals, we need to create a subdirectory. Remember to "clone" the new directory to get the layer information; from the target directoy:

[Sys] [Clone] write Temporary in the "Full Path of New Folder[ ]" box [OK]

TIP: use a WinLASI6 version to do this - Version 7 does not seem to write the layer file correctly ...

Check the new directory has one file in it: lasi6.usf

[Sys} [GDS2TLC] [Setup] enter the following ....

```
GDS File Name              [Invertor.gds        ]
Path of all TLC Cell Files [Path* (- see below) ]
--Layer Options-----------------------------------------------------
Layer Datatype Map File  [Invertor.ldm                              ]
TLC Layer Filter (1-256) [25 26 29 41-52 56 58 59 61 62             ]
-------------------------------------------------------------------

    Physical Units [um     ]   LASI units per Phys Unit [Scale**    ]

--Conversion Options------------------------------------------------
[v]Convert GDS Text    [v]Replace old TLC Files  [ ]Omit Layers Record
[v]Check for Open Poly [v]Use Default Opt. Recds [ ]Write Layers TLD
[v]Convert Boundaries to  Boxes                  [ ]Write Names File
-------------------------------------------------------------------
             Report File Name [Gds2tlc.rpt   ]        [OK]
```

*Path = E:\Documents and Settings\All Users\Documents\WinLASI\SCRATCH \Invertor\Temporary\
**Scale = 20 Lasi Units/Phys Unit; look in [Sys] [Scale].

Notice that we have used a sub-directory of the target directory, to prevent the original .tlc files from being overwritten.

[Go]

There are now 45 files plus the "Temporary" sub-directory in the target direcory with 3 files in the sub-directory. The new files are: Gds2Tlc.usf Gds2tlc.rpt and in the sub-direcory:
Invertor.tlc Pmos13w2l.tlc and Nmos4w2l.tlc

Go to the Temporary directory and double click on Invertor.tlc

The invertor layout should come up. It will initially appear "odd" - this is because the text is missing. REsize the two layout windows you now have open, on shoould be on the Invertor cell in he target

director, then other on the Invertor in the temporary sub-directly. Compare the two layouts - text apart, they should be identical apart from where the conversion to GDSII format has removed vertices etc.

TIP: only read in the new tlc files with version 7. Version 6 seems to pick up old versions of the layout (for my example, the pre-DRC versions of the layout).

Check that the sizes of the two layouts are the same; for example the vias should be 4lambda across. If not go back and check the value of scale above with the numer of LASI Units per Physical Unit entered in GDS2TLC window above.

Do an [Export] etc to produce the {layers}.tlc file.

You should now have 17 files in the temporary directory: {layers}.tlc Cells6.dbd Invertor.bp6 Invertor.cl6 Cells7.dbd Lasi7.usf Loadbkup.tlc Swap.bpv Undobkup.tlc Cellbkup.bp6 Cellbkup.cl6 Mainbkup.bp6 Mainbkup.cl6 have been added to lasi6.usf Invertor.tlc Pmos13w2l.tlc and Nmos4w2l.tlc already there. The target directory should still have 45 files in it.

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