ESD PADS for MOSIS Submicron design rules using On's C5 process

λ = 300 nm

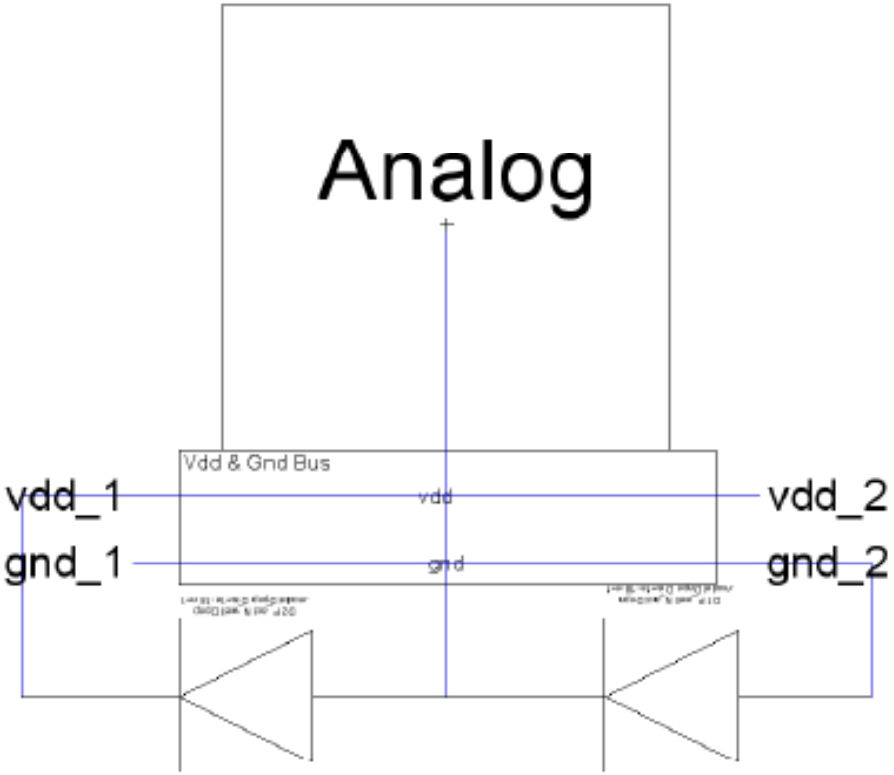
Technology code: SCN3ME_SUBM

Electric Technology: mocmos (submicron)

List of pads

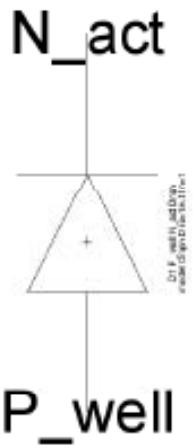
- Analog pad
- Digital Input/Output (Bidirectional) pad
- VDD pad
- GND pad

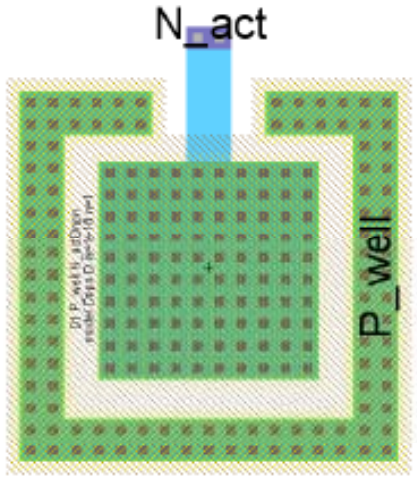
Analog Pad



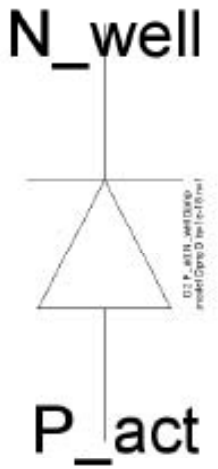
The pad contains diodes for ESD (Electrostatic Discharge) Protection. When the pad gets voltage higher than VDD, the P_act to Nwell diode turns on and supplies the extra voltage to vdd source. Similarly if the pad gets voltage lower than ground (negative voltage), the N_act to Pwell diode turns on supplying the negative voltage to the ground. Both the diodes protect the pad from damages.

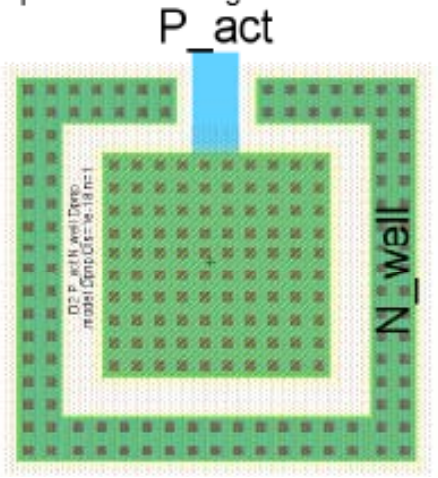
ESD diodes and Layout





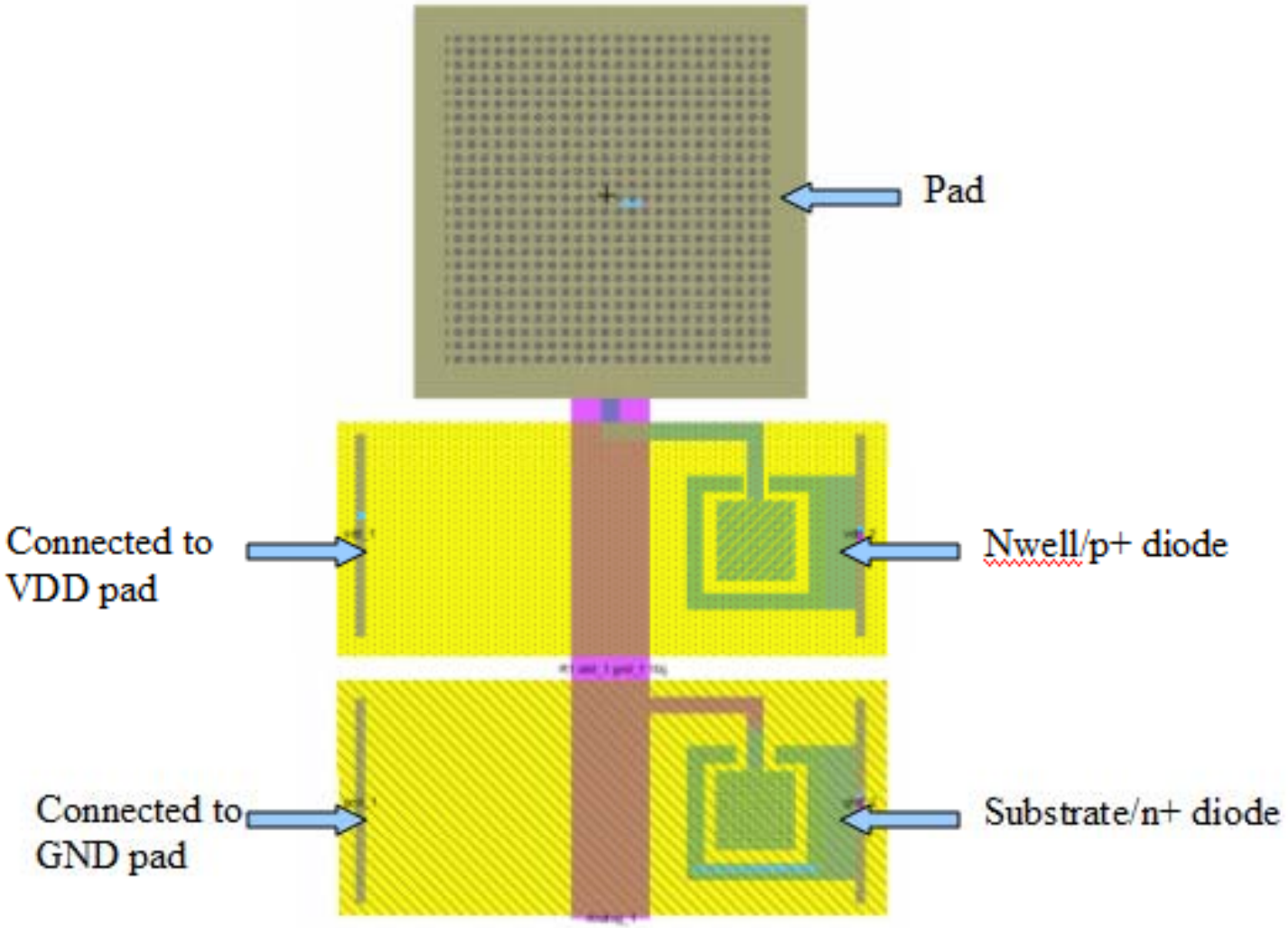
N_act is connected to pad and p_well is connected to ground. If the voltage on pad goes below ground (0 volt) the diode turns on and drives the negative voltage to ground preventing the pad from damage.



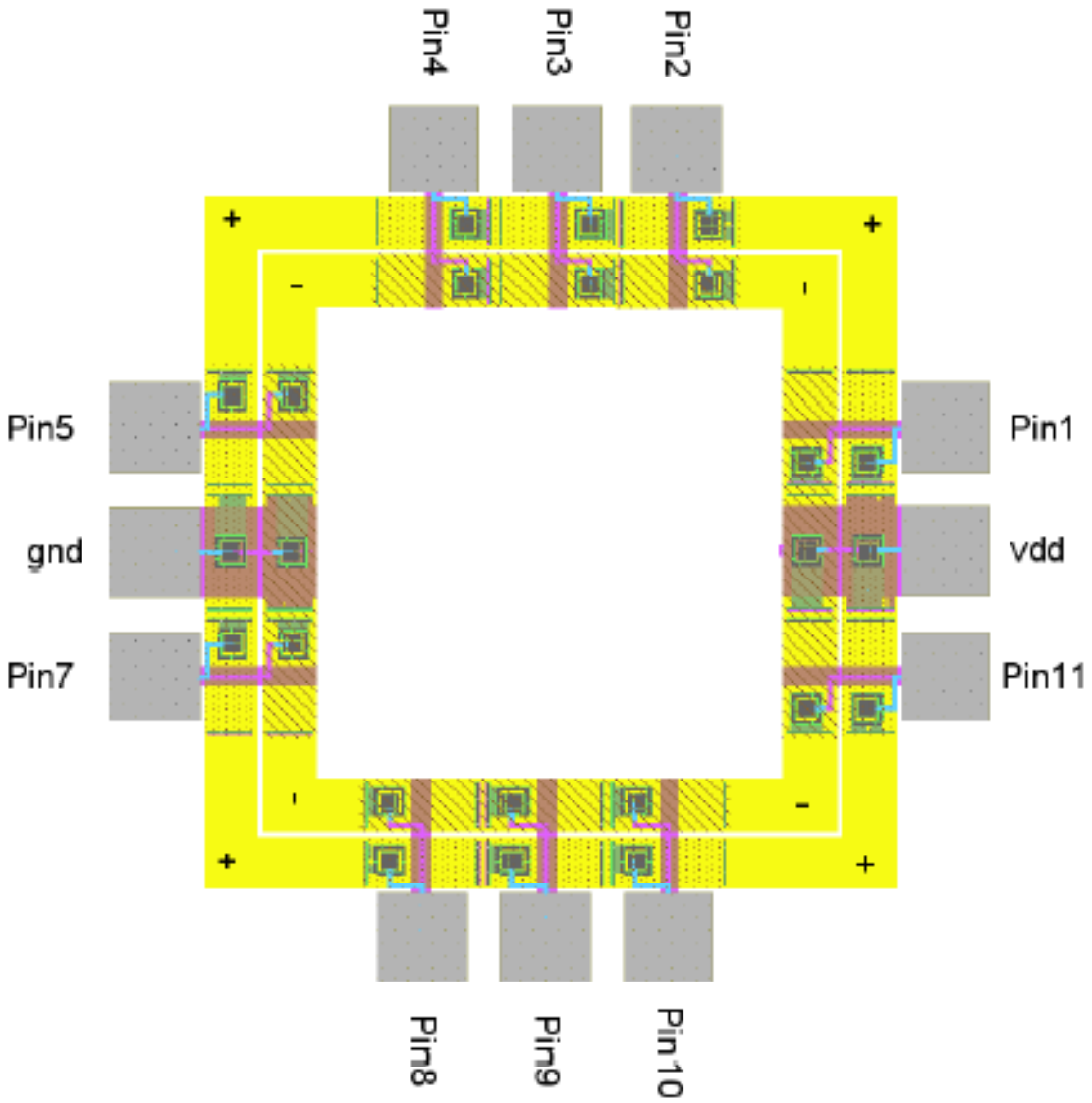


P_act is connected to pad and n_well is connected to power. If the voltage on pad goes above vdd (5 volt) the diode turns on and drives the extra voltage to power preventing the pad from damage.

Analog Pad Layout

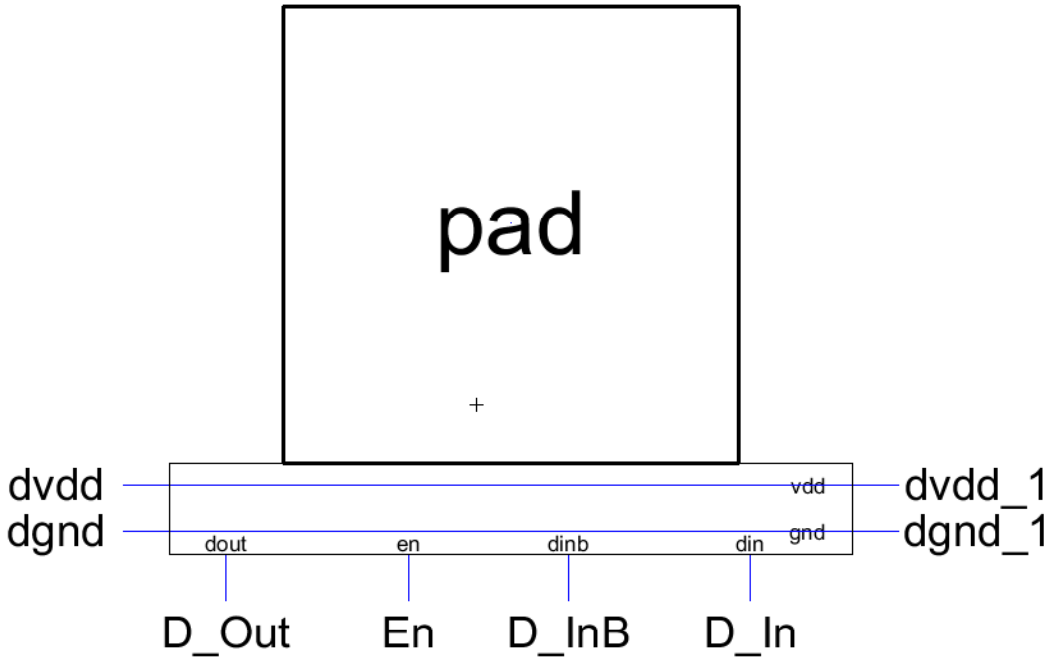


Example of a 12 pin Analog Chip Layout using Analog pads

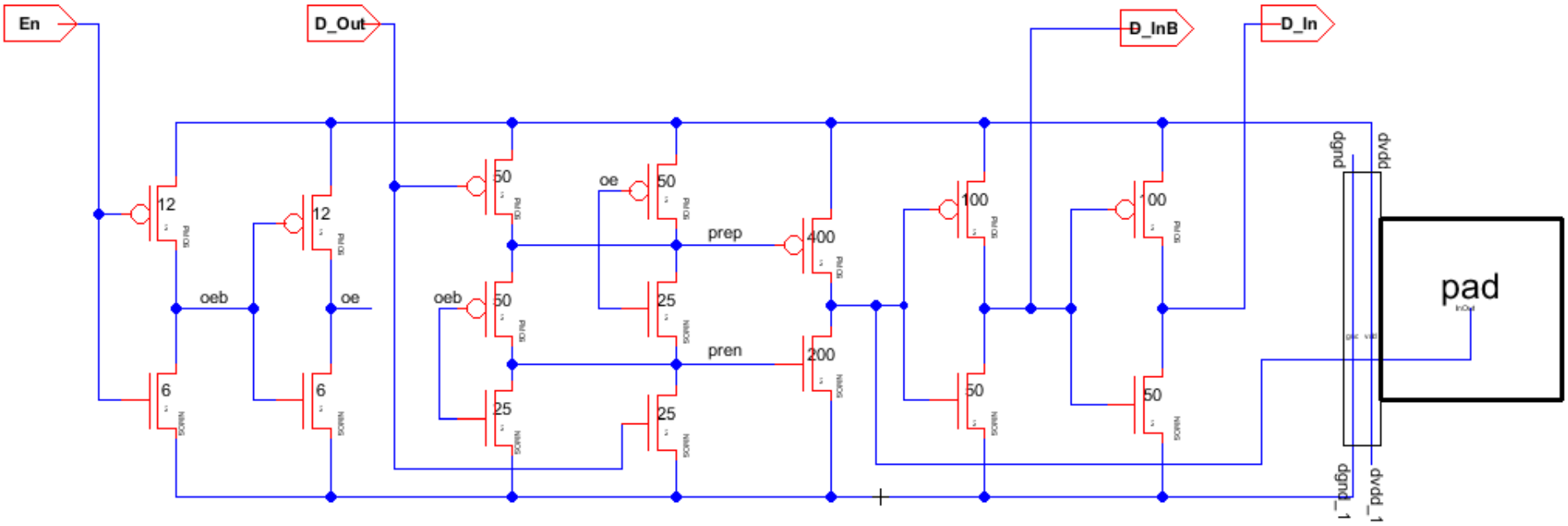


Digital Input/Output (Bidirectional) Pad

- The digital pad contains a bidirectional circuit. It can be used either as an **input** pad to drive the on-chip circuitry or as an **output** pad to drive a signal off-chip. It is also known as a bidirectional pad.

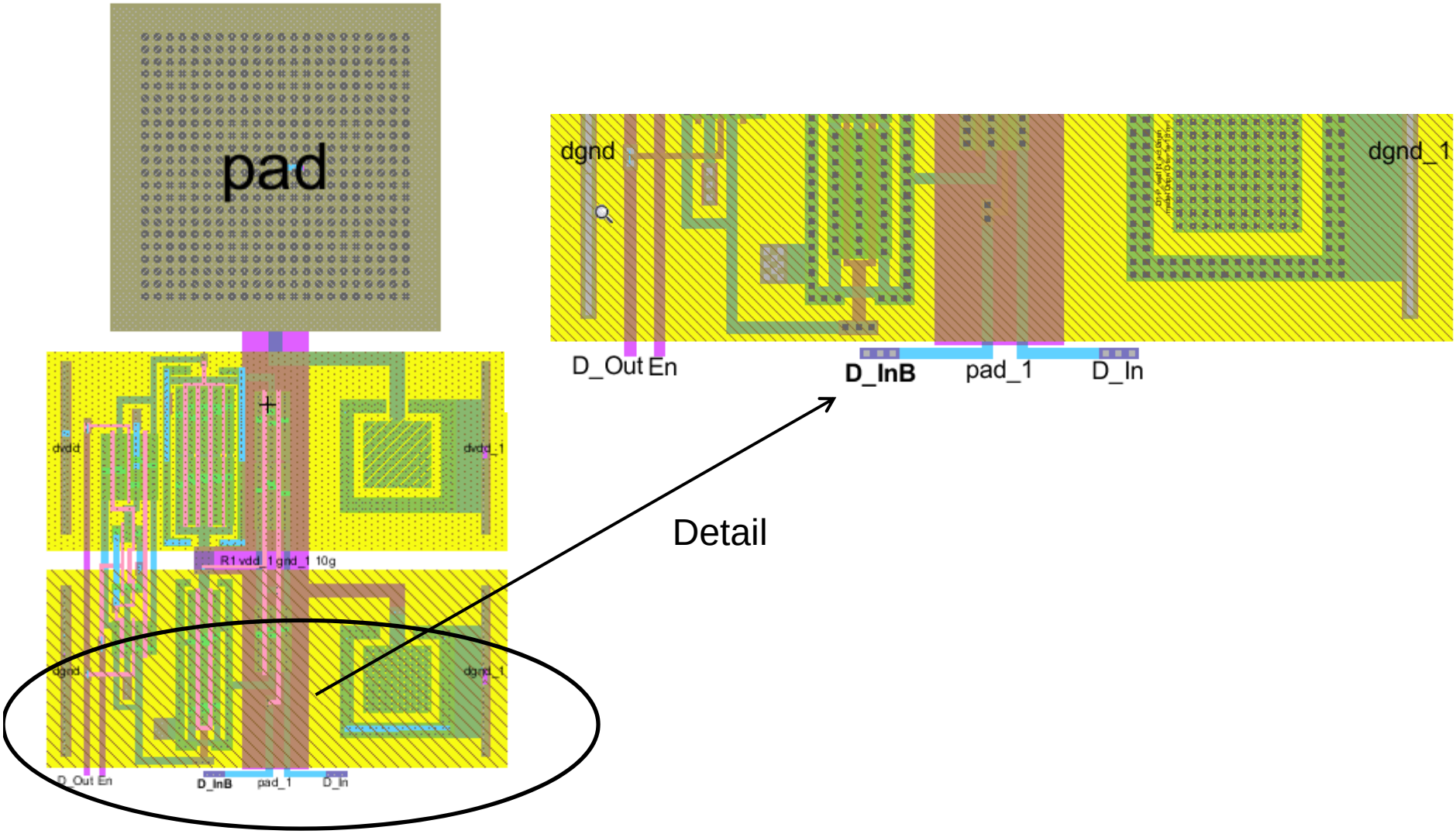


Bidirectional Circuit

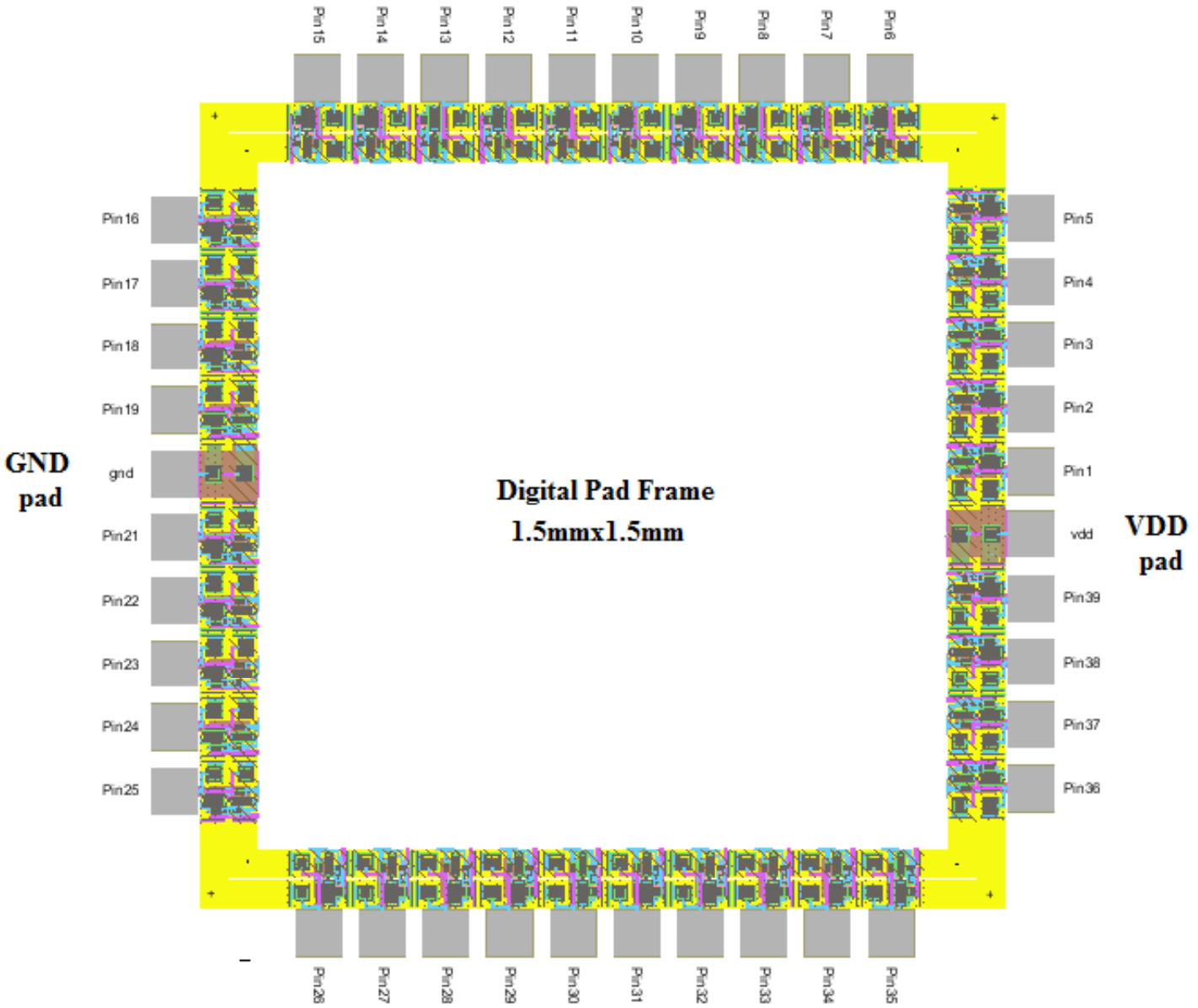


- The bidirectional circuit has five signals: D_Out, En, D_In, D_InB, and pad. Pad is the bonding pad that is wire-bonded to the package (so it can have a pin or signal name).
- For use as an **output pad** En is driven to VDD and the on-chip signal is connected to D_out. Signals D_InB and D_In are unused.
- For use as an **input pad** En is driven to ground and D_In, and its complement D_InB, are the signals coming on-chip from the pad.

Digital I/O Pad Layout

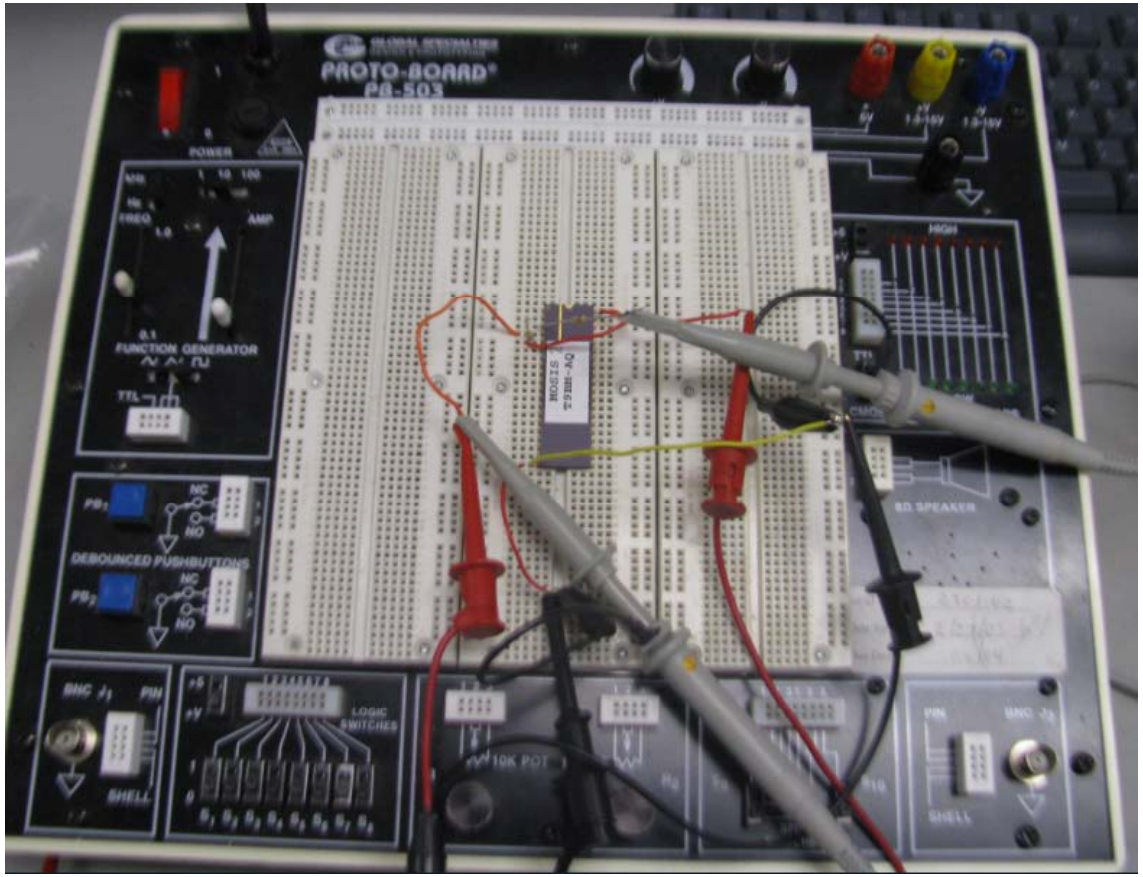


40 Pin - Digital Pad Frame Layout

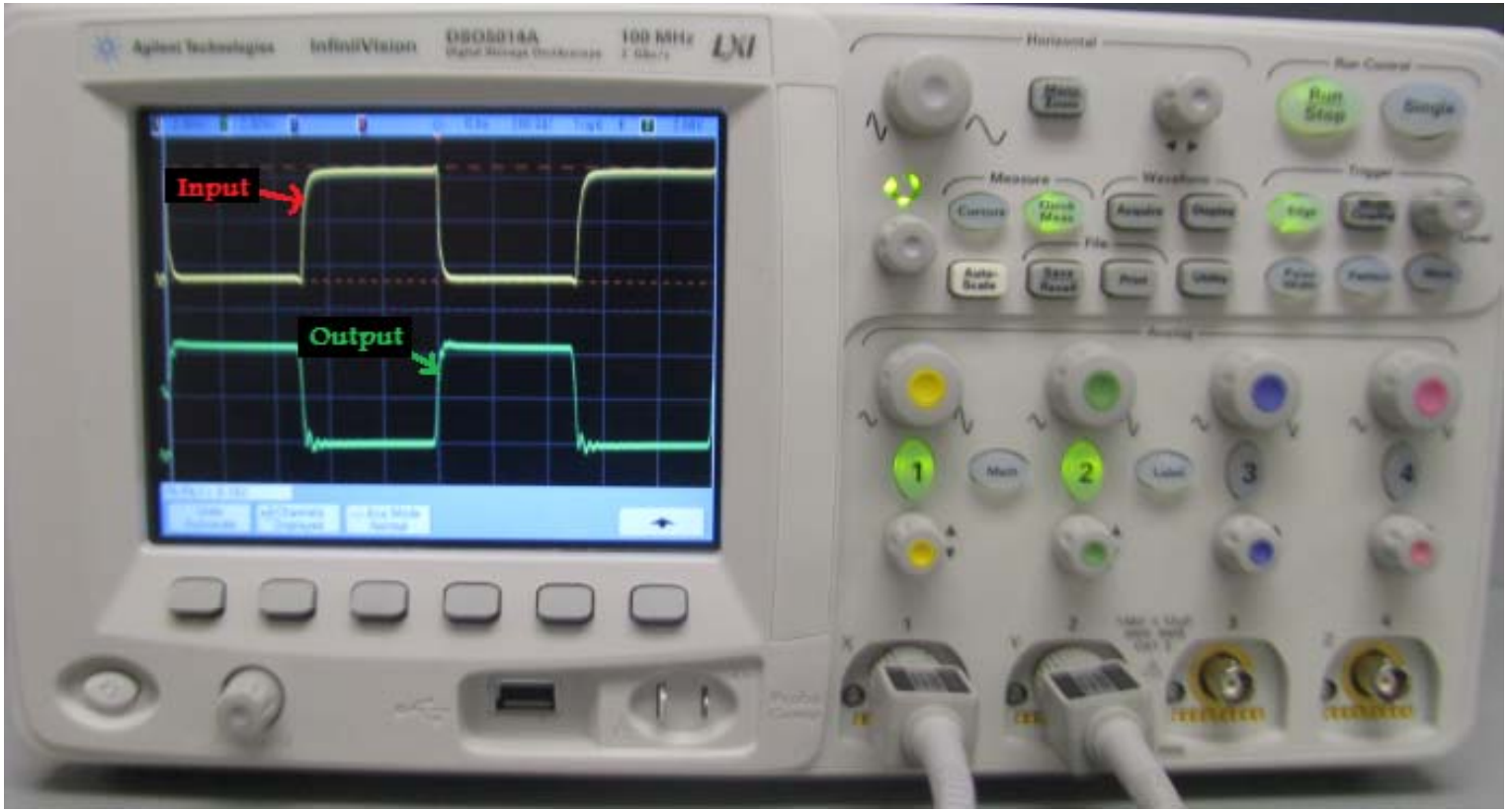


Simulation Results of Digital Chip

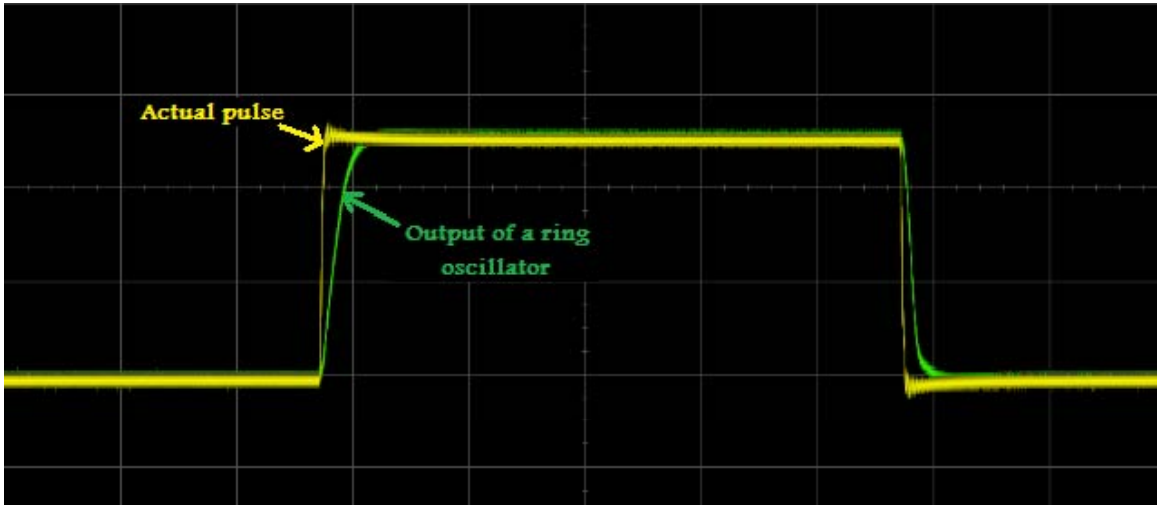
- A 40 pin Digital chip containing digital pads was fabricated using On's C5 process with lambda = 300nm.
- A 21 stage ring oscillator, 2 to 1 multiplexer and 2 input nand gate were used to check the operation of the pads.
- The set up to test the chip is shown in the following picture.



- The following scope shot shows the result of a 2 input nand gate. One input of the nand gate was tied to vdd (5 volts) and a pulse was given on the second input. The output is an inverted pulse with the same period as the input.



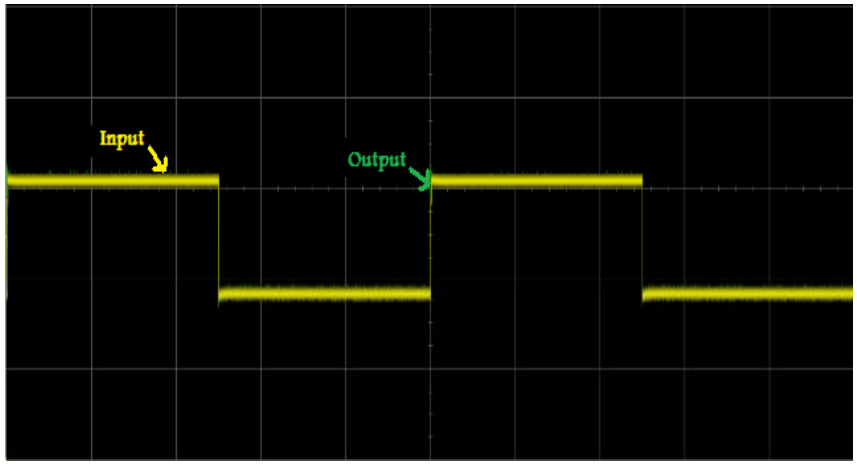
Output of a 21 stage ring oscillator



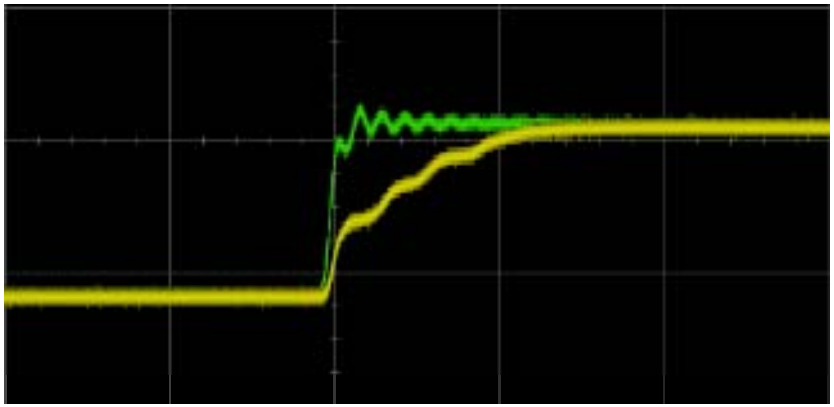
Zoomed view of output pulse, 10 ns/div

Simulation Results of Analog Chip

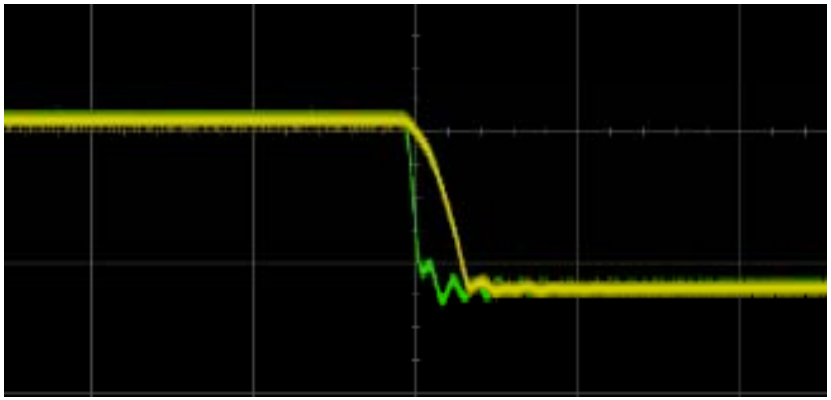
- A 40 pin Analog chip containing analog pads was fabricated using On's C5 process with lambda = 300nm.
- Four different topologies of two stage op-amps are used to test the performance of the chip.



Output of a two stage op-amp, 10 ns/div.



Zoomed view of Rising edge



Zoomed view of Falling edge

Conclusion

- The analog pads use simple diodes for ESD protection. The diodes provide little loading compared to the off-chip load.
- The digital pads include input/output buffers and can operate at > 30 MHz clock rates.
- The pads can be used with the Electric VLSI Design system for general analog and digital design using the MOSIS SUBM design rules with scale (lambda) = 300 nm.