#### Jones, Janice E Civ USAF AETC AFIT/ENG

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88 ABW has completed the review process for your case on 17 Jul 2012:

Subject: Integrated Circuit Design CAD Tool Information (Course Description)

Originator Reference Number: AFITENG141 Case Reviewer: William Huntington Case Number: 88ABW-2012-3988

The material was assigned a clearance of CLEARED on 17 Jul 2012. This email serves as the official notice of the disposition of this case. If you have additional questions, contact the Review Manager for your case, William Huntington, william.huntington@wpafb.af.mil.

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#### **Integrated Circuit Design CAD Tool Information**

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This work contains common CAD tool information used for the courses EENG653, EENG695, and EENG795. It has been adapted from similar material used at Tufts, Columbia, University of Virginia, and University of Utah. The Linux material is provided by the University of Surrey (UK) and O'Reilly.

Questions or comments for improvements on this document should be sent to <u>mary.lanzerotti@afit.edu</u>. Cadence is a trademark of Cadence Design Systems, Inc., 2655 Seely Avenue, San Jose, CA 95134

Permissions to use materials have been generously given by the following individuals. Thank you to all of them.

Kenneth Shepard, Columbia University

Jan Van der Spiegel, University of Pennsylvania

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Mircea Stan, University of Virginia

# **Integrated Circuit Design CAD Tool Information**

# **Table of Contents**

1.	General Information and Linux Account Information	3
2.	Guidelines for Working in the VLSI CAD Lab	4
3.	A Beginner's Guide to the Unix and Linux Operating System	5
4.	Linux Quick Reference: O'Reilly (www.oreilly.com)	9
5.	Setting up Firefox	11
6.	Setting up Secure Shell (SSH)	14
7.	Screen Capture of Images with The GIMP	17
8.	Printing and Plotting	19
9.	Setting up the Linux Environment and Getting Started with Cadence 6.1.5	23
10.	Sending Email from Linux	37
11.	Inverter: Creating a Library	
12.	Inverter: Creating a Schematic	40
13.	Inverter: Creating a Symbol	54
14.	Inverter: Performing a Spectre Simulation on a Schematic	59
15.	Inverter: Creating a Layout	
16.	Inverter: Running Design Rule Check (DRC)	120
17.	Inverter: Running Extraction	124
18.	Inverter: Running Layout Versus Schematic (LVS)	131
19.	Inverter: Running Extracted-Layout Simulation	136
20.	Inverter: Simulation with NC-Verilog	142
21.	nFET: Generating I-V Curves for an nFET	155
22.	nFET: Parametric Simulation of I-V Curves (nFET)	185
23.	Inverter: Generating a Voltage Transfer Curve (VTC) of an Inverter	203
24.	Inverter Chain: Creating an Inverter Chain	228
25.	Ring Oscillator	244
26.	Ring Oscillator: Learning to Use the Calculator	258
27.	Parameterized Inverter Chain: Delay of Inverter Chain	
28.	Parameterized Inverter Chain: More Use of the Calculator	318
29.	Parameterized Inverter Chain: Parametric Analysis of the Delay of an Inve	erter
Cha	ain	322
30.	The End	336

## **Integrated Circuit Design CAD Tool Information**

# **Integrated Circuit Design CAD Tool Information**

# 1. General Information and Linux Account Information

- **a.** Modern industrial integrated-circuit-design CAD tools will be an integral part of this course. All students in the courses must have access to the CAD tool setup at AFIT. This page contains relevant administrative information for all you need to do to get started with these tools.
- **b.** Read the following:
  - i. You will use the Linux workstations in the VLSI CAD Lab (Building 640, Room 332)
  - ii. You need an active login ID
- **c.** Prior to the first class, I will collect a list of student names in the class and send the list to the AFIT Help Desk (helpdesk@afit.edu). I will request that the AFIT Help Desk set up the computer accounts.
- **d.** All students should look for an email messages from either Mr. David Doak or Mr. Donald Bodle with your Linux account information and requesting that you stop by the SC Help Desk ("SC") to set your password.

Following the first lecture, after you receive this email, all students should go to the SC Help Desk and ask for "Unix Help." You will be redirected to another section of SC to Mr. Doak or to Mr. Bodle who will show you how to set your Linux password.

**e.** As soon as you have your password, you are able to start these labs and can log in to the VLSI Linux machines in the VLSI CAD Lab.

After the first week of class, any problems with login access to the machines should be addressed to Mr. David Doak: helpdesk@afit.edu, the AFIT Systems Administrator.

#### **Integrated Circuit Design CAD Tool Information**

#### 2. Guidelines for Working in the VLSI CAD Lab

- **a.** The VLSI CAD Lab is maintained by the Electrical and Computer Engineering Department.
- **b.** Do not bring any friends/visitors to the lab and let them use the machines on your account. These are not public machines.
- **c.** Food and drinks are allowed, BUT you must be VERY careful and clean up after yourself.
- **d.** The quota for each student is 20 GB. Please keep only relevant files in your home.
- **e.** Do NOT fire huge printing jobs at the lab printer. Printers are for your convenience and printing anything other than HW or project files is NOT permitted. Also, do not try to print tool documentation. Such files are hundreds of pages.
- **f.** Do NOT reboot the machines. Contact system administrators in case the machine hangs or freezes
- g. System Administrator: Mr. David Doak: <u>helpdesk@afit.edu</u>
- **h.** We encourage doing your homework and projects in Building 640, Room 332. This allows the professor and System Administrator to do a walk-through and help you. It also allows you to help each other.
- i. All paths for CAD tools should be automatically set.

#### **Integrated Circuit Design CAD Tool Information**

#### 3. A Beginner's Guide to the Unix and Linux Operating System

- **a.** Linux is a Unix-like operating system.
- b. If you are not familiar with Unix and Linux, the following link provides a beginner's guide to the Unix and Linux operating system. Eight tutorials cover the basics of UNIX/Linux commands. These tutorials and summaries below were developed by <u>M.Stonebank@surrey.ac.uk</u>. They are reproduced here for your reference during these tutorials.
- **c.** The link is: <u>http://www.ee.surrey.ac.uk/Teaching/Unix</u>
- **d.** Introduction to the UNIX Operating System
- **e.** Tutorial One Summary

Command	Meaning
ls	list files and directories
ls –a	list all files and directories
mkdir	make a directory
cd directory	change to named directory
cd	change to home-directory
cd ~	change to home-directory
cd	change to parent directory
pwd	display the path of the current directory

# **Integrated Circuit Design CAD Tool Information**

**f.** Tutorial Two Summary

Command	Meaning	
cp file1 file2	copy file1 and call it file2	
mv file1 file2	move or rename file1 to file2	
rm <i>file</i>	remove a file	
rmdir directory	remove a directory	
cat <i>file</i>	display a file	
less file	display a file a page at a time	
head <i>file</i>	display the first few lines of a file	
tail <i>file</i>	display the last few lines of a file	
grep 'keyword' file	search a file for keywords	
wc file	count number o	
	lines/words/characters in file	

**g.** Tutorial Three Summary

Command	Meaning
command > <i>file</i>	redirect standard output to a file
command >> file	append standard output to a file
command < file	redirect standard input from a file
command1	pipe the output of command1 to the
command2	input of command2
cat file1 file2 > file0	concatenate file1 and file2 to file0
sort	sort data
who	list users currently logged in

# **Integrated Circuit Design CAD Tool Information**

**h.** Tutorial Four Summary

Command	Meaning			
*	match any number of characters			
?	match one character			
man <i>command</i>	read the online manual page for a			
	command			
whatis command	brief description of a command			
apropos keyword	match commands with keyword in their			
	man pages			

**i.** Tutorial Five Summary

Command	Meaning		
ls –lag	list access rights for all files		
chmod [options]	change access rights for named file		
file			
command &	run command in background		
^C	kill the job running in the foreground		
^Z	suspend the job running in the		
	foreground		
bg	background the suspended job		
jobs	list current jobs		
fg %1	foreground job number 1		
kill %1	kill job number 1		
ps	list current processes		
kill 26152	kill process number 26152		

### **Integrated Circuit Design CAD Tool Information**

j. Tutorial Six Summary

<b>Other Useful UNIX</b>	Meaning		
Commands			
quota	disk space on the file system		
df	space left		
du	number of kilobytes in each		
	subdirectory		
gzip	reduces file size		
zcat	reads gzipped file		
file	classifies the named files		
diff	compares two files and displays the		
	differences		
find	searches through directories for files		
	and directories for attribute		
History	C shell keeps an ordered list of all		
	entered commands		

**k.** Tutorial Seven Summary

Command	Meaning
make	Manage large programs or groups of
	programs
makefile	Set of compile rules in a text file

**l.** Tutorial Eight Summary

Variables	Meaning			
UNIX variables	A way to p	A way to pass information from the shell		
	to program	to programs		
Environment	Set by the	Set by the setenv command		
variables				
Shell variables	\$history,	\$cwd,	\$HOME,	\$PATH,
	\$prompt; % set   less			

# **Integrated Circuit Design CAD Tool Information**

# 4. Linux Quick Reference: O'Reilly (<u>www.oreilly.com</u>)

**a.** Some Useful Commands

	inux Quicl	<b>c Refe</b> L COMM	erence ANDS
Commond	Tack	Commond	Task
Commanu	Idak	Commanu	Idak
File/Directo	ry Basics	File Locatio	n
ls	List files	find	Locate files
ср	Copy files	slocate	Locate files via index
mv	Rename files	which	Locate commands
rm	Delete files	whereis	Locate standard files
In	Link files	File Text M	anipulation
cd	Change directory	aren	Search text for matching
pwd	Print current directory name	3.05	lines
mkdir	Create directory	cut	Extract columns
rmdir	Delete directory	paste	Appena columns
e1. 16. 1		tr	Translate characters
File viewing	]	sort	Sort lines
cat	view files	uniq	Locate Identical lines
less	Page through files	tee	to stdout simultaneously
nead	view file beginning		to stable similaritaneously
tall	view file ending	File Compr	ession
ni od	Number lines View binary data	gzip	Compress files (GNU Zip)
xxd	View binary data	compress	Compress files (Unix)
gv	View Postscript/PDF files	bzip2	Compress files (BZip2)
xdvi	View TeX DVI files	zip	Compress files (Windows Zip)
<b>File Creatio</b>	n and Editing		(
emacs	Text editor	File Compa	rison
vim	Text editor	diff	Compare files line by line
umask	Set default file	comm	Compare sorted files
	protections	cmp	Compare files byte
soffice	Edit Word/Excel/ PowerPoint docs	md5sum	Compute checksums
abiword	Edit Word documents	Disks and D	ile evet eme
gnumeric	Edit Excel documents	DISKS and F	Chow free disk space
File Dreport	ine	ui macunt	Show nee usk space
rite Propert	Display file attributes	foold	Wake a disk accessible
SLOL	Count bates (verde (lines)	ISUK	Check a disk for entris
wu	Count bytes/words/intes	Syric	FIUSH UISK CACHES
au file	Measure disk usage	Backups an	d Remote Storage
touch	Change file timestamos	mt	Control a tape drive
chowen	Change file owner	dump	Back up a disk
abaro	Change file group	restore	Restore a dump
chmod	Change file protections	tar	Read/write tape archives
abottr	Change nie protections	cdrecord	Burn a CD
unaur	attributes	rsync	Mirror a set of files
lsattr	List advanced file attributes		

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#### **Integrated Circuit Design CAD Tool Information**

#### **b.** Some Useful Commands

#### **Linux Quick Reference** SOME USEFUL COMMANDS

Command

Networking

ssh

telnet

scp

sftp

ftp

mutt

mail

lynx

wget

mozilla

evolution

Task

Securely log into remote hosts

Log into remote hosts

Securely copy files

Securely copy files

Copy files between hosts GUI email client

Text-based email client

Text-only web browser

Retrieve web pages

Minimal email client

Web browser

to disk

between hosts

between hosts

#### Command Task

Printing	
lpr	Print files
lpq	View print queue
lprm	Remove print jobs

#### **Spelling Operations**

look	Look up spelling
aspell	Check spelling interactively
spell	Check spelling in batch

#### Pr

Processes	
ps	List all processes
w	List users' processes
uptime	View the system load
top	Monitor processes
xload	Monitor system load
free	Display free memory
kill	Terminate processes
nice	Set process priorities
reniœ	Change process priorities

#### Scheduling lobs

Wait for some time
Run programs at set intervals
Schedule a job
Schedule repeated jobs

#### Hosts

uname	Print system information
hostname	Print the system's hostname
ifconfig	Set/display network information
host	Look up DNS
whois	Look up domain registrants
ping	Check if host is reachable
traceroute	View network path to

www.oreilly.com

traceroute a host





Excerpted from Linux Pocket Reference

#### **Integrated Circuit Design CAD Tool Information**

#### 5. Setting up Firefox

**a.** In this step you will set up the Proxies for Firefox. Open a Firefox window as shown below.



#### **Integrated Circuit Design CAD Tool Information**

**b.** In the banner at the top of the Firefox window, select 'Edit  $\rightarrow$  Preferences" and click on the 'Advanced' button and then the 'Network' tab. The 'Firefox Preferences' window will appear as shown in the image below.

3		Firefox Pref	erences			_ D X		
General Tabs	Content	Applications	Privacy	Security	Sync			
General Network	Update Er	cryption	They	Security	Sync	Advanced		
Connection Configure how	Firefox cor	nnects to the In	ternet		(	😤 S <u>e</u> ttings		
Offline Storage	urrently us	ing 57.8 MB of	disk snace	2	G	Clear Now		
<u>Override</u> aut	omatic ca	the managem	ent	-				
Limit cache	to 102	24 📩 MB of sp	ace	-	ſ	Fucentians		
The following w	n a website vebsites ha	e asks to store (	data for of for offline	use:	L	Exceptions		
Remove								
🚱 <u>H</u> elp						X Close		

#### **Integrated Circuit Design CAD Tool Information**

**c.** In the 'Firefox Preferences' window, select 'Settings.' The 'Connection Settings' window will appear. Select 'Manual proxy configurations" button as shown, with HTTP Proxy: 129.92.252.3 Port: 8080; SSL Proxy: 129.92.252.3 Port: 8080; No Proxy for: localhost, 127.0.0.1, .afit.edu. Then click OK in this window and close the Firefox preferences window.

8	Connection Settings		×					
Configure Proxies to Access the Internet								
O No proxy								
○ Auto-detect proxy settings for this net <u>w</u> ork								
○ <u>U</u> se system pro	oxy settings							
ၜ <u></u> Manual proxy င	onfiguration:							
HTTP Pro <u>x</u> y:	129.92.252.3	Port:	8080					
	Use this proxy server for all	protoco	ols					
SS <u>L</u> Proxy:	129.92.252.3	P <u>o</u> rt:	8080					
ETP Proxy:		Po <u>r</u> t:	0					
SO <u>C</u> KS Host:		Por <u>t</u> :	0					
	○ SOC <u>K</u> S v4							
<u>N</u> o Proxy for:	localhost, 127.0.0.1, .afit.edu							
	Example: .mozilla.org, .net.nz,	192.16	8.1.0/24					
○ <u>A</u> utomatic prox	y configuration URL:							
			Reload					
🔀 <u>H</u> elp 🛛 🗶 Cancel 🗳 ОК								

## d. You should now be able to access the internet.

#### **Integrated Circuit Design CAD Tool Information**

#### 6. Setting up Secure Shell (SSH)

- **a.** On your Windows machine, go to the Start menu and click on "All Programs." Move the cursor to the "SSH Secure Shell" folder, open it, right click on the "Secure File Transfer Client" and then Pin to Taskbar.
- **b.** Open the SSH Secure File Transfer Client (now pinned on your taskbar).
- **c.** In the "SSH Secure File Transfer Client," click on the "Profiles" button (it looks like a yellow folder) and press "Add Profile." The "Add Profile" window will open, and enter "telemark" in the profile name field as shown below. Then click "Add to Profiles."



#### **Integrated Circuit Design CAD Tool Information**

**d.** Then click on "Profiles" again and click "Edit Profiles." The Profiles window will appear. In this window, under the "Connection" tab, set "Host name:" to "telemark" and "User name:" to your Linux username (e.g. your first initial followed by your last name). The Port number should already be set to "22" as shown in the image below.

Profiles			
Profiles Quick Connect Profiles Profile Name Mary Profile Name Mary Profile NameMary defaultstp m telemark	Colors       Tunnelin         Connection       Ciple         Configure protocol setting upon next login.       Specify * as the host naminformation when the profit         Host name:       tele         User name:       mix         Port number:       22         Encryption algorithm:       MAC algorithm:         Compression:       Terminal answerback:         Connect through fir       Request tunnels or	ng File Transfer her List Authentication s for the connection. New setting is for the user name to be promp ile is chosen for connecting. emark anzero (Default> (Default> (None> vt100 vt100 verwall nly (disable terminal)	Favorite Folders Keyboard ngs will take effect ited for the
		ΟΚ	Cancel

**e.** Press OK on the "Profiles" window.

- **f.** Now in the "SSH Secure File Transfer" window, click on "Profiles" again and select 'telemark.' Select 'yes' and then click 'OK' on the two windows that appear. Then enter your Linux password in the "Enter Password" window that appears. Click OK after entering your password.
- **g.** In the "SSH Secure File Transfer" window, the left side is your Windows information (click on the pulldown to find the various drives, such as the I: drive). Click on "Computer" and your home directory is located with your Windows username. On the right side is your Linux information. You can navigate to where you have saved the files you want to transfer.
- h. When you find the files on the Linux (right) side that you want to transfer to Windows, you will click on the files using 'SHIFT and CNTL" to select multiple files. Then drag the selected files to the Windows side and drop into your desired directory.
- i. You can keep this "SSH Secure File Transfer" window open.
- **j.** Use the 'Refresh' (circular arrows) button if you save a new file on Linux.

#### **Integrated Circuit Design CAD Tool Information**

## 7. Screen Capture of Images with The GIMP

a. To launch Gimp, move your cursor to the upper-left hand corner of the screen (Linux). Select "Applications → Graphics → The GIMP". The GIMP graphical user interface will appear as shown in the figure below.



- b. On The GIMP GUI, select "File → Acquire → Screen shot." In the Screen Shot window, select "a Single Window" and "1 second delay." Then click Grab.
- **c.** Then click on the window that you wish to save. A Gimp.tif window will appear.
- **d.** Save your window in .tif format with your desired filename in one of your directories. You may also save in other file formats (.tif is preferred; .ps and .eps formats are preferred in LaTex documents; in this document, .tif files are used for the screenshots of Cadence windows).

#### **Integrated Circuit Design CAD Tool Information**

#### 8. Printing and Plotting

a. To print a Virtuoso ® Visualization & Analysis window, select "File → Print → Print to File (postscript)". A "Print" window will appear. Enter the name of your desired output file in the window. GIMP is able to read ps files generated from a print from the Visualization & Analysis window as shown below.



- **b.** To print an entire schematic in a Virtuoso window (Schematic, Layout, Extracted view), select "File  $\rightarrow$  Print  $\rightarrow$  Plot Options" and fill in the print window. You may send the output to your AFIT email account: <u>mary.lanzerotti@afit.edu</u> and the file to <filename.ps> which will be written in your working directory, such as \$HOME/cadence/ncsu-cdk-1.6.0.utah folder. Kghostview is able to read multi-page postscript files generated from a Virtuoso Schematic winder. To start Kghostview, in the Linux screen, click on the menu bar: "Applications  $\rightarrow$  Graphics  $\rightarrow$  KGhostView  $\rightarrow$  File  $\rightarrow$  Open." Then point the window to your printed file, which should be in your home directory. Printing with the header information selected will produce a document such as the schematic shown below (two pages).
- **c.** To print a portion of a schematic, select "File  $\rightarrow$  Print  $\rightarrow$  Plot Options" and fill in the print window using the appropriate coordinates of your plot (lower left and upper right coordinates) in the "Area to Plot" field. Be sure to add extra space if you would like to see extra space around the boundary of your plot.

**Integrated Circuit Design CAD Tool Information** 

USEA:mlanzero DATE:Thu Apr 2611:46:47 2012 PLOT SIZE:5.12 x 9.64 Inches Library: EENG653Tutorial Cell: IVcurves View: schematic Plot Area: ((-1.7125 - 5.25)(2.275 2.2625))



#### **Integrated Circuit Design CAD Tool Information**

# 9. Setting up the Linux Environment and Getting Started with Cadence 6.1.5.

- **a.** You should already have contacted Mr. David Doak (david.doak@afit.edu) and have a Linux email userid and Linux password
- **b.** Log in to a Linux machine
- **c.** Open a terminal window (right click with the mouse)

					mlanzero@vlsilab05:~		X)
<u>F</u> ile	<u>E</u> dit	<u>V</u> iew	<u>T</u> erminal	Ta <u>b</u> s	<u>H</u> elp		
[mla	nzero	@vlsi]	lab05 ~]\$			-	
							≡
						l	-

### **Integrated Circuit Design CAD Tool Information**

#### **d.** At the command line in this window, type: cp /apps/vlsi/etc/cshrc .cshrc

						mlanzero@vlsifac01:~	
<u>F</u> ile	<u>E</u> dit	<u>V</u> iew	<u>T</u> ermi	nal	Ta <u>b</u> s	Help	
[mla	nzero	@vlsi1	fac01	~]\$	pwd		<u></u>
/hom	e/afi	ten3/1	fac/ml	anze	ero		
[mta [mla	nzero nzero	@vlsi @vlsi1	fac01	~]\$ ~]\$	ср 73	apps/vtsi/etc/csnrc .csnrc	
							~

# **Integrated Circuit Design CAD Tool Information**

# **e.** To verify the copy command, type more .cshrc

	mlanzero@vlsilab05:~	
<u>F</u> ile <u>E</u> o	dit <u>V</u> iew <u>T</u> erminal Ta <u>b</u> s <u>H</u> elp	
[mlanze /home/a [mlanze [mlanze # #	ero@vlsilab05 ~]\$ pwd afiten3/fac/mlanzero ero@vlsilab05 ~]\$ cp /apps/vlsi/etc/cshrc ./cshrc ero@vlsilab05 ~]\$ more .cshrc .cshrc	
# # # #	input) commands should be used in this file. Any interactive command placed in this file could cause problems with command like "rsh" on this system.	
# # #	If you want the backspace key on the sun workstations to work in the crttool, uncomment the following line (it may break other things though).	
# # # #	DO NOT MOVE, CHANGE, ADD, OR DELETE THE FOLLOWING LINES. They are part of our system set-up that allows us to keep your login environment updated. vvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvv	=
	set SystemCshrc = /etc/csh.cshrc set SystemLogin = /etc/csh.login set VLSIAlias = /apps/vlsi/etc/aliases	
More	1f ( -e \$SystemCshrc ) then (65%)	



#### **Integrated Circuit Design CAD Tool Information**

### f. At the command line in the same window, type: /bin/csh

mlanzero@vlsilab05:~	
<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>T</u> erminal Ta <u>b</u> s <u>H</u> elp	
[mlanzero@vlsilab05 ~]\$ pwd	<u></u>
/home/afiten3/fac/mlanzero	
[mlanzero@vlsilab05 ~]\$ cp /apps/vlsi/etc/csnrc ./csnrc	
#	
<pre># NOTICE: Only non-interactive (commands that do not need keyboard</pre>	
<pre># input) commands should be used in this file. Any</pre>	
# Interactive command placed in this file could cause	
# problems with command tike rsh on this system.	
# If you want the backspace key on the sun workstations to work	
# in the crttool, uncomment the following line (it may break other	
<pre># things though).</pre>	
# set CrttoolBackspace	
# DO NOT MOVE, CHANGE, ADD, OR DELETE THE FOLLOWING LINES. They	
# are part of our system set-up that allows us to keep your login	=
<pre># environment updated.</pre>	
#	
<pre>set SystemCshrc = /etc/csh.cshrc</pre>	
<pre>set SystemLogin = /etc/csh.login</pre>	
set VLSIAlias = /apps/vlsi/etc/aliases	
if ( -e \$SystemCshrc ) then	
[mlanzero@vlsilab05 ~]\$ /bin/csh	
[mlanzero@vlsilab05 ~]\$	

# **Integrated Circuit Design CAD Tool Information**

# **g.** At the command line in the same window, type: add\_cadence

File Edit View Terminal Tabs Help				
[mlanzero@vlsilab05 ~]\$ pwd	Â			
/home/afiten3/fac/mlanzero				
mlanzero@vlsilab05 ~]\$ cp /apps/vlsi/etc/cshrc ./cshrc				
# .cshrc				
#				
<pre># NOTICE: Only non-interactive (commands that do not need keyboard</pre>				
<pre># Input) commands should be used in this file. Any # interactive command placed in this file could cause</pre>				
<pre># problems with command like "rsh" on this system.</pre>				
#				
# If you want the backspace key on the sun workstations to work				
<pre># In the crttool, uncomment the following line (it may break other # things though)</pre>				
* chings chough).				
# set CrttoolBackspace				
# are part of our system set-up that allows us to keep your login	=			
# environment updated.				
# *************************************				
set SystemCshrc = /etc/csh.cshrc				
set SystemLogin = /etc/csh.login				
set VLSIAlias = /apps/vlsi/etc/aliases				
if ( -e \$SystemCshrc ) then				
[mlanzero@vlsilab05 ~]\$ /bin/csh				
[mlanzero@vlsilab05 ~]\$ add_cadence				
[mlanzero@vlsilab05 ~]\$ which add_cadence				
add_cadence: allased to source /apps/vls1/etc/setup_cadence.csn				
	-			

-	mianzero@visifac01 _ 🗆	x
	#!/bin/csh -f	
	setenv CADHOME /apps/vlsi/Cadence ###################################	
	# Master IC Cad flow including schematic capture, simulation, layout,	
	# and Verification. ####################################	
	setenv LANG C #++++++++++++++++++++++++++++++++++++	
	# IC Schematic Entry, Simulation, Layout, # Verification (Diva) #++++++++++++++++++++++++++++++++++++	
	setenv CDS \$CADHOME/IC615	
	<pre># Some of these variables are used by various other tools. # Set them to be safe setenv CDSDIR \$CDS setenv CDSHOME \$CDS setenv CADENCE_DIR \$CDS setenv CDS_INST_DIR \$CDS</pre>	
	# Cadence uses a setup.loc file to help setup third party tools # like Golden Gate and RFDE. This environment variable will be used # to guide the search. #setenv CDS_SITE /data/cadtools/cds/cdssetup	
	# Set Spectre defaults and netlisting mode setenv CDS_Netlisting_Mode Analog setenv SPECTRE_DEFAULTS -E	
	# This environment variable enables Spectre HB setenv CDS_SPECTRERF_FBENABLE 1	
	# Turn on the Palette feature. LSW no longer works, but many new features available setenv CDS_USE_PALETTE	
	<pre># Support for 64-bit executables, when available if (`uname -p` == x86_64) then setenv CDS_AUT0_64BIT ALL endif</pre>	
	setenv PATH \$CDSDIR/bin:\$CDSDIR/tools/dfII/bin:\$CDSDIR/tools/bin:\$CDSDIR/tools/plot/bin:\${PATH}	
	#+++++++++++++++++++++++++++++++++++++	
	# # These executables should be on the PATH after DFII executables #++++++++++++++++++++++++++++++++++++	
	setenv PATH \${PATH}:\$ASSURAHOME/bin:\$ASSURAHOME/tools/bin:\$ASSURAHOME/tools/assura/bin	
	#+++++++++++++++++++++++++++++++++++++	
	<pre># Note: QRC Must appear in the PATH before Assura execuatbles. #++++++++++++++++++++++++++++++++++++</pre>	



#### **Integrated Circuit Design CAD Tool Information**

# **h.** To verify that the executable is in the path, type: which virtuoso

	mlanzero@vlsilab05:~			
<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>T</u> erminal Ta <u>l</u>	<u>b</u> s <u>H</u> elp			
[mlanzero@vlsilab05 ~]\$ pw	/d	<b></b>		
/home/afiten3/fac/mlanzero	)			
mlanzero@vlsilab05 ~]\$ cp /apps/vlsi/etc/csnrc ./csnrc mlanzero@vlsilab05 ~l\$ more .cshrc				
# .cshrc				
#				
# NOTICE: Only non-1	Interactive (commands that do not need keyboard			
# interactiv	/e command placed in this file could cause			
# problems w	vith command like "rsh" on this system.			
#				
# If you want the ba	ackspace key on the sun workstations to work			
<pre># things though).</pre>	comment the following time (it may break other			
5 5 .				
# set CrttoolBackspa	ace			
# DO NOT MOVE. CHANG	SE. ADD. OR DELETE THE FOLLOWING LINES. They			
# are part of our sy	/stem set-up that allows us to keep your login	=		
# environment update	ed.			
# \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~			
set SystemCshrc =	/etc/csh.cshrc			
set SystemLogin =	/etc/csh.login			
set VLSIAlias = /a	apps/vlsi/etc/aliases			
if ( -e \$SystemCsh	nrc ) then			
[mlanzero@vlsilab05 ~]\$ /b	pin/csh			
[mlanzero@vlsilab05 ~]\$ ad	ld_cadence			
[mlanzero@vls1lab05 ~]\$ wh	nich add_cadence			
[mlanzero@vlsilab05 ~]\$ wh	hich virtuoso			
/apps/vlsi/Cadence/IC615/b	pin/virtuoso			
[mlanzero@vlsilab05 ~]\$				
		~		

# **Integrated Circuit Design CAD Tool Information**

i. Type:

use\_ncsucdk

	mianzero@visilab05:~		
<u>F</u> ile	Edit View Terminal Tabs Help		
# # # #	NOTICE: Only non-interactive (commands that do not need keyboard input) commands should be used in this file. Any interactive command placed in this file could cause problems with command like "rsh" on this system. If you want the backspace key on the sun workstations to work		
# #	In the critical, uncomment the following line (if may break other things though).		
# # #	DO NOT MOVE, CHANGE, ADD, OR DELETE THE FOLLOWING LINES. They are part of our system set-up that allows us to keep your login environment updated. vvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvv		
	<pre>set SystemCshrc = /etc/csh.cshrc set SystemLogin = /etc/csh.login set VLSIAlias = /apps/vlsi/etc/aliases if (</pre>		
[mla	nzero@vlsilab05 ~]\$ /bin/csh	=	
[mla [mla	nzero@vlsilab05 ~]\$ add_cadence		
add_	cadence: aliased to source /apps/vlsi/etc/setup_cadence.csh		
[mla	mlanzero@vlsilab05_~]\$ which virtuoso		
/app [mla [1]	s/Vts//Cadence/1ts/pin/Virtusso nzero@vlsilab05 ~]\$ use_ncsucdk 8986		
[mla	nzero@vlsilab05 ~]\$ which use_ncsucdk ncsucdk:aliased to source /apps/vlsi/etc/ncsu-cdk-1 6 0 beta csb:		
n/cs	xterm -fg white -bg royalblue -fn 9x15 -sl 1000 -geometry 100x35 -title mlanzero@vlsilab05 /bi h &; cd		
[mla use_ [mla	lanzero@vlsilab05 ~]\$ which use_ncsucdk e_ncsucdk: aliased to source /apps/vlsi/etc/ncsu-cdk-1.6.0.beta.csh; xterm -fg white -bg royalblue -fn 9x15 -sl 1000 -geometry 100x35 -title mlanzero@vlsilab05 /bin/csh &; cd lanzero@vlsilab05 ~]\$		

```
_ = ×
                                                         mlanzero@vlsifac01
FreePDK Setup Script
    2/23/2008 by Rhett Davis (rhett_davis@ncsu.edu)
#
#
# Set the PDK_DIR variable to the root directory of the FreePDK distribution
setenv PDK_DIR /apps/vlsi/ncsu-cdk-1.6.0.beta
setenv PDK_HOME ~/cadence/ncsu-cdk-1.6.0.beta
# Set CDSHOME to the root directory of the Cadence ICOA installatio
#setenv CDSHOME /afs/eos/dist/cadence2008/ic
if !(-d ${PDK_HOME} ) then
mkdir -p $PDK_HOME
cd ${PDK_HOME}
if !(-f ${PWD}/.cdsinit ) then
cp ${PDK_DIR}/cdssetup/cdsinit ${PWD}/.cdsinit
if !(-f ${PWD}/.cdsenv ) then
cp ${PDK_DIR}/cdssetup/cdsenv ${PWD}/.cdsenv
endif
if !( -f ${PWD}/cds.lib ) then
cp ${PDK_DIR}/cdssetup/cds.lib ${PWD}/cds.lib
endif
if !( -f ${PWD}/display.drf ) then
cp ${PDK_DIR}/cdssetup/display.drf ${PWD}/display.drf
if !( -f ${PWD}/lib.defs ) then
cp ${PDK_DIR}/cdssetup/lib.defs ${PWD}/lib.defs
setenv CDS_SITE ${PDK_DIR}
setenv CDK_DIR ${CDS_SITE}
setenv USE_NCSU_CDK
(END)
```
### **Integrated Circuit Design CAD Tool Information**

# **j.** In the blue window that appears, type: virtuoso –log ./CDS\_lab.log &



# **Integrated Circuit Design CAD Tool Information**

**k.** The CIW for Virtuoso **(B)** 6.1.5-64b will appear with the log file indicated in the banner at the top of the window.

Virtuoso® 6.1.5-64b - Log: /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/CDS_03162012.log	
File Iools Options Help	cādence
COPYRIGHT © 1992-2011 CADENCE DESIGN SYSTEMS INC. ALL RIGHTS RESERVED. © 1992-2011 UNIX SYSTEMS Laboratories INC., Reproduced with permission. This Cadence Design Systems program and online documentation are This Cadence Design Systems program and online documentation are	
as autorized in a license agreement controlling such use and disclosure.	
Us/reproducton/dislocations worlde (short rough) set forth as FAR 1525.227-19 or its equivalent. Program: 0(*)SDDS: wirlowso version 6.1.5-64b 09/07/2011 01:07 (sjfd1342) \$ Sub version: sub-version IC6.1.5-64b.500.6 (64-bit addresses) Loading qe/we ext	
Loading membhilder cxt Loading schWiew cxt Loading selectSv cxt Loading LVS cxt Loading LVS cxt	
Loading xUII.cxt Loading whol.cxt Loading seismic.cxt Loading c.cxt	
Loading ams.cxt Wirtupse Tramswork License (111) was checked out successfully. Total checkout time was 0.07s. Loading NOSU CDK 1.5.1 customizations Loading vars from /apps/vlsi/nosu-cdk-1.6.0.beta/cdssetup/cdsenv for tool adle Loading vars from /apps/vlsi/nosu-cdk-1.6.0.beta/cdssetup/cdsenv for tool asimenv *WARNING* env5etVal: Can't set the value of variable 'width', in tool   natting   asimeny plottion' = it has not here registered	
<pre>*WARNING* envSetVal. Cont set the value of variable 'height'.</pre>	
Done loading NOSU_CDK customizations.	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
1 > M:	B:

# **Integrated Circuit Design CAD Tool Information**

**I.** The Library Manager will also appear indicating the run directory in the banner at the top of the window.

Library Manager: Directoryro/cadence/ncsu-cdk-1.6.0.beta	×
<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>D</u> esign Manager <u>H</u> elp	cādence
Show Categories       Show Files         Library       Cell         EEN6695       State of the state of	
Messages	
Log file is "/home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/libManager.log". Loading NCSU Library Manager customizationsdone.	

# **Integrated Circuit Design CAD Tool Information**

# **10.** Sending Email from Linux

- a. Step 1
  - i. Open a blue Linux terminal by typing the following command in a white terminal (Right click in the Linux desktop and select 'open terminal').
  - ii. Type 'use\_ncsucdk'.
- **b.** Step 2
  - i. Type mail <user\_email address> in the blue window that appears, and then hit 'Enter'.
  - ii. Example: mail mary.lanzerotti@afit.edu and hit 'Enter.'
- **c.** Step 3
  - i. Copy and paste your link or other ascii information into the message space.
- d. Step 4
  - i. Hit Return and on the blank line at the bottom of your note, type '.'
- **e.** Step 5
  - i. Add any other email addresses in the cc: line
  - ii. Otherwise hit 'Return.'
- **f.** The email is sent.

### **Integrated Circuit Design CAD Tool Information**

### **11.** Inverter: Creating a Library

- **a.** Now you will create a library to store your circuit designs. Every library will be associated with a foundry-supplied technology file. For this laboratory, the technology file is supplied in the NCSU Design Kit.
- b. In the CIW or Library Manager window, click with the mouse on File → New → Library to obtain the following window. Complete the two fields for Name: and Path. The Name of your Library is 'LibName'. Your Path should be <Your Working Directory/LibName>. In the example shown below for the course EENG653, 'Name' is set to 'EENG653.' The working directory is '/home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta.'

	Create Library	×
Library		
Name:	EENG653	
Path:	/home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/EENG653	
Technol If this li Otherw Choose	brary will not contain physical design (i.e., layout) data you do not need a tech library. vise, you must either attach to an existing tech library or compile one. e option: No tech library needed Attach to existing tech library> AMI 0.60u C5N (3M, 2P, high-res)	
Misc. –	I/O Pad Type: 💿 Perimeter 🔾 Area array	
	OK Cancel Apply Help	p

# **Integrated Circuit Design CAD Tool Information**

**c.** Now you will see EENG653 appear in the Library Manager Window in the list of libraries on the left-hand side.

Library Manager: Directoryro/cadence/ncsu-cdk-1.6.0.1	eta 🛛 🔍
<u>File Edit View D</u> esign Manager <u>H</u> elp	cādence
Show Categories       Show Files         Library       Cell         EENG653       EENG695         NCSU_Analog_Parts       NCSU_Digital_Parts         NCSU_TechLib_ami06       NCSU_TechLib_ami06         NCSU_TechLib_smc02       NCSU_TechLib_tsmc02         NCSU_TechLib_tsmc02d       NCSU_TechLib_tsmc03d         NCSU_TechLib_tsmc03d       NCSU_TechLib_tsmc03d         NCSU_TechLib_tsmc03d       NCSU_TechLib_tsmc04_4M2P         basic       cdsDefTechLib         dave       Librate	View
Messages Log file is "/home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/libManager.log". Loading NCSU Library Manager customizationsdone.	

**d.** Now you have completed the task of creating a new empty Library.

# **Integrated Circuit Design CAD Tool Information**

### **12.** Inverter: Creating a Schematic

- **a.** Now you can create a Schematic in the library. To create a schematic, highlight the library EENG653 in the Library Manager.
- b. Click in the Library Manager Window with the mouse on the File → New → Cell View. Another window will appear as shown below with "New File" in the banner at the top of the window. Fill in the fields for Cell as 'inverter' and View as 'schematic.'



**c.** Click OK in the "New File" form.

### **Integrated Circuit Design CAD Tool Information**

**d.** A new Schematic window will appear with the title "Virtuoso Schematic Editor L Editing: EENG 653 inverter schematic" in the banner at the top of the window.



# **Integrated Circuit Design CAD Tool Information**

**e.** Now you are going to insert instances of devices into this Schematic Window in order to create an inverter shown below.



# Integrated Circuit Design CAD Tool Information

**f.** The first instance you will insert is an nfet. Click on the Schematic Window and type 'i' in the window. Two new Windows will appear. The Component Browser window and Add Instance browser are shown below:

Component Brows 🗕 🗆 🗙
Commands <u>H</u> elp <b>cādence</b>
Library NCSU_Analog_Parts Flatten Filter * Go up 1 level) Thesim
nbsim nbsim4 njfet nmes nmes4 nmos nmos4 nmos4_hv nmos_hv nmos_hv npn usernon
N_Transistors
4 HelpAction

# **Integrated Circuit Design CAD Tool Information**

	Add I	nstance 🗙						
Library	NCSU_Analog_Parts	Browse						
Cell	nmos4							
View	symbol							
Names								
🗹 Add Win	e Stubs at:							
	🔾 all terminals 🖲 r	egistered terminals only 📃						
Array	Rows 1	Columns 1						
	🖹 Rotate 🛛 🕼 Si	deways 🛛 🔫 Upside Down						
Model nar	ne	ami06N						
Model Typ	00	🖲 system 🔾 user						
Multiplier		1						
Fingers		1						
Width (grid	t units)	10						
Width		1.5u M						
Width (min	imum)	1.5u M						
Length (gr	id units)	4						
Length		600n M						
Length (mi	inimum)	600n M						
Drain diffu	sion area	2.25e-12						
Source dif	fusion area	2.25e-12						
Drain diffu	sion perimeter	6u M						
Source dif	fusion perimeter	6u M						
Drain diffu	sion res squares							
Source dif	fusion res squares							
Virtuoso-X	(L layout cell							
Drain diffu	sion length							
Source dif	fusion length							
Temp rise	from ambient							
Estimated	operating region	sat 🔽						
	Hide Cancel Defaults Help							

### **Integrated Circuit Design CAD Tool Information**

- g. In the Component Browser Window, select NCSU\_Analog\_Parts → N\_Transistors → nmos4, which will select a four-terminal nfet in the Add Instance Window. Fill in the fields in the Add Instance Window as shown in the Window above. Note that you have the ability to change the values of the channel width ('Width'), channel length ('Length'), and number of fingers ('Fingers') in the Add Instance Window.
- **h.** Click with the left mouse button in the Schematic Window in order to place one instance of the nfet in the Schematic Window.
- i. Press 'ESC' to cancel the placement of any additional nfets.
- **j.** If you wish to go back and change the properties ('Width', 'Length', 'Fingers') of the nfet that you just placed, click with the mouse on the instance to highlight it. Then type 'q'. Another form will appear to allow you to edit the object properties.
- **k.** The next instance you will insert is a pfet. Click on the Schematic Window and type 'i' in the window. Two Windows will appear.

### **Integrated Circuit Design CAD Tool Information**

I. In the Component Browser Window, select NCSU\_Analog\_Parts → p\_Transistors → pmos4, which will select a four-terminal pfet in the Add Instance Window. Fill in the fields in the Add Instance Window as shown in the Window above. Note that you have the ability to change the values of the channel width ('Width'), channel length ('Length'), and number of fingers ('Fingers') in the Add Instance Window.

	Add I	nstance 🗙								
Library	Library NCSU_Analog_Parts									
Cell	pmos4									
View	symbol.									
Names										
iiW bbA 🔽	Add Wire Stuke at									
	all terminals 💿 registered terminals only									
Array	Array Rows 1 Columns 1									
	🕰 Rotate 📄 🛛 🗥 Si	deways 🛛 🗲 Upside Down								
Model na	me	amill6P								
Model Ty	pe	🖲 system 🔾 user								
Multiplier		1								
Fingers		1								
Width (gri	d units)	10								
Width		1.5u M								
Width (mir	nimum)	1.5u M								
Length (g	rid units)	4								
Length		600n M								
Length (m	inimum)	600n M								
Drain diffu	ision area	2.25e-12								
Source di	ffusion area	2.25e-12								
Drain diffu	ision perimeter	6u M								
Source di	ffusion perimeter	6u M								
Drain diffu	ision res squares									
Source di	ffusion res squares									
Virtuoso-)	<l cell<="" layout="" td=""><td></td></l>									
Drain diffu	ision length									
Source di	ffusion length									
Temp rise	from ambient									
Estimated	Estimated operating region 🛛 sat 🧧									
Hide Cancel Defaults Help										

# **Integrated Circuit Design CAD Tool Information**

**m.** Click with the left mouse button in the Schematic Window in order to place one instance of the pfet in the Schematic Window. Place the pfet above the nfet as shown in the inverter schematic.

Virtuoso® Schematic Editor L Editing: EENG653 inverter schematic															IX															
<u>L</u> aunch <u>F</u> ile <u>E</u> dit	<u>V</u> iew	<u>C</u> reat	te (	Chec <u>k</u>	0	ption	5 <u>M</u>	igrate	e 7	<u>∦</u> ind	ow	NC	SU	<u>H</u> e	lp													cāc	l e n	ce
	] ∥ ∯	÷C			×		Ţ		1	\$	¢	4	2.	T	î.	тŤ			Q	۲	F		망	5	1	1	abo	1		È
	6	Works	spac	e: Ba	isic				-	Ę	1	-		13	٦Ŀ	1	3 -	R	T,		8	Q	r Se	arcl	1			•		
Navigator	? 🗗	×					•				•	•		•					•	•		•		•	•		•		•	- Î
T Default																														
Q Search		-																												
Name		<u>,</u>																												
inverter																														•
P0 (pmos4)																														•
																														•
																្នៃ	بر لے الے	19 niØ6P												•
															•	-9t	Ŵ	=1.	5u											•
																	`  ≐ ■m	=6Ø! :1	Øn											•
																														·
																- I F		0 niØ6t	J											
Property Editor		<u> </u>															W	=1	5u.											
																	- <b> </b>  =	=6Ø! •1	Øn											
																														•
																														•
	Pt(t)									M: e	chH	iMe		Popl	InA											В- 1	odd	a Dra	NZ MA	nde.
2(5) Point at starting	point fo	r the r	route	erors	nap	to dia	amon	d usi	ng t	the "	s" ke	ey.	4961	-040	-040											1. 1	Omd:	Wire	Sel	: 0

### **Integrated Circuit Design CAD Tool Information**

- **n.** Press 'ESC' to cancel the placement of any additional pfets.
- **o.** If you wish to go back and change the properties ('Width', 'Length', 'Fingers') of the pfet that you just placed, click with the mouse on the instance to highlight it. Then type 'q'. Another form will appear to allow you to edit the object properties.
- p. Now you will create wires to connect the two devices. Click on the Schematic window. In the Schematic window, type 'w' and click with the left mouse button at the location you wish to add the wire. The wire will be blue. Move the mouse to the final location of the wire. Double-click with the mouse at the final location to finish adding the wire. Press 'ESC' to stop adding the wire.

# **Integrated Circuit Design CAD Tool Information**

**q.** Add wires to the Schematic window so that the design looks like the image shown below.



# **Integrated Circuit Design CAD Tool Information**

**r.** Now you will add pins to the schematic. Click on the Schematic Editor window. In the Schematic Editor window, type 'p', and an Add Pin window will appear as shown in the image below.

		Add Pin	×						
Pin Names	Vin								
Direction	input	Bus Expansion	🖲 off 🔾 on						
Usage	schematic	Placement	🖲 single 🔾 multiple						
Signal Type	signal								
Attach Net Expression: 💿 No 🔾 Yes									
Property Name									
Default Net Name									
Font Height	0.0625	Font Style	stick -						
🔼 Rotate	▲ Sideways	🗧 Upside Down	Show Sensitivity >>						
		Hide Canc	el Defaults Help						

### **Integrated Circuit Design CAD Tool Information**

- **s.** In the Add Pin window, fill in the field "Pin Names" with 'Vin' and for the "Direction" pulldown, select 'input'. Move the mouse to the location on the wire where you will add the pin, and click with the left mouse button to place the pin. Make sure you click the mouse button on the wire so that the pin is connected to the wire.
- t. In the Add Pin window, fill in the field "Pin Names" with 'Vout' and for the "Direction" pulldown, select 'output'. Move the mouse to the location on the wire where you will add the pin, and click with the left mouse button to place the pin. Make sure you click the mouse button on the wire so that the pin is connected to the wire.
- **u.** In the Add Pin window, fill in the field "Pin Names" with 'VDD' and for the "Direction" pulldown, select 'inputoutput'. Move the mouse to the location on the wire where you will add the pin, and click with the left mouse button to place the pin. Make sure you click the mouse button on the wire so that the pin is connected to the wire.
- v. In the Add Pin window, fill in the field "Pin Names" with 'GND' and for the "Direction" pulldown, select 'inputoutput'. Move the mouse to the location on the wire where you will add the pin, and click with the left mouse button to place the pin. Make sure you click the mouse button on the wire so that the pin is connected to the wire.

# **Integrated Circuit Design CAD Tool Information**

**w.** The inverter in the Schematic window will look like the image below.



**x.** Now you have finished the task of creating an inverter schematic.

# **Integrated Circuit Design CAD Tool Information**

**y.** Here is a Quick Reference of commands.

Command Quick Reference							
Command	Function						
i	Add instance						
р	Add pin						
q	Edit properties						
W	Add wire						
f	Fit schematic within your schematic window						
1	Label a wire						
m	Move an object						
DEL	Delete an object						
ESC	Terminate any of the operations in the schematic						
	window						
Up	Up arrow moves up in a schematic window						
Down	Down arrow moves down in a schematic window						

### **Integrated Circuit Design CAD Tool Information**

### 13. Inverter: Creating a Symbol

- **a.** A symbol is a representation of a schematic. Symbols are instantiated in higher-level schematics in order to create hierarchical schematics that represent more complex designs.
- **b.** You will now create a symbol of the inverter that you designed in the previous section.
- c. Click on the Schematic Window. In the Schematic Window, click 'Create → Cellview → From Cellview'. Fill in the Fields for 'Library Name' as "EENG653" and 'Cell Name' as 'inverter' as shown in the image.

	Cellview From Cellview	X)
Library Name	EENG653 Browse	
Cell Name	inverter	
From View Name	schematic 🔽	
To View Name	symbol	
Tool / Data Type	schematicSymbol 🧧	
		_
Display Cellview		
Edit Options		
	OK Cancel Defaults Apply Help	

# **Integrated Circuit Design CAD Tool Information**

**d.** In the Symbol Generation Options Window, select the location of the pins as shown in the schematic, as represented in the image shown below.

	Symb	ol Gener	ation Optio	ns	×
Library Name		Cell Name		View Name	
EENG653	ii	nverter		symbol	
Pin Specificatio	ons				Attributes
Left Pins	Vin				List
Right Pins	Vout				List
Top Pins	VDD				List
Bottom Pins	GND				List
Exclude Inherit	ed Connection Pins:				
🖲 None 🔾	All 🔾 Only these:				
Load/Save 🗌	Edit Attribute	s 🔲	Edit Labels	Edit Pro	operties 🔲
			01	Cancel Ap	ply Help

### **Integrated Circuit Design CAD Tool Information**

**e.** After selecting the pins, click the 'OK' button on the Symbol Generation Options window. A Symbol Editor window will appear as shown in this figure.



# **Integrated Circuit Design CAD Tool Information**

**f.** Click in the Symbol Editor window and make the changes to the partName to 'Inverter' and instanceName to 'Inv' to match the image shown below.

<b>\$</b>	Virtuoso	o® Syn	nbol Edi	tor L E	diting	J: EEN	G653	invert	er syn	nbol				
Launch <u>F</u> ile <u>E</u> dit <u>V</u> iew <u>C</u> re	eate Chec <u>k</u>	Option	s <u>W</u> indow	/ <u>H</u> elp									c ā d	ence
1 🗅 🗁 🕢 🖬 🛛	0 💷 🖇	۵ ک	T⁄ 🖻	) 🥎	¢т	т т		Q	Q 🚱					
🔾 🕶 💭 🐨 🗍    Wo	irkspace: Ba	sic		- 5	-		ABC 🚽		<b>-</b>	) /				
Navigator ? 🗗 🗙					Â						<u>^</u>			
T Default	· ·													
🔍 Search 📃 🔻														
Name 🔺														
-1 GND						_								
1. VDD	•													
1 Vout 														
		. [								-Inv				
>>=> Vin:P0 >=> Vout:P1														
	•													
	· •				Inv	/Art/	or i							
					1110									
Property Editor														
	•	. L												
	· ·													
mouse L: mouseAddPt(t)				M: so	:hHiMou	usePonl	ln∩					R: si	chCmd	Dation∩
3(6) Click on text to edit or pres	s ESC to car	ncel.										Cmc	l: Text	Sel: 0

### **Integrated Circuit Design CAD Tool Information**

- **g.** If you have extra time, you can manipulate the Symbol view to turn the rectangle into a triangle to represent the inverter. Use the menu (with the arrow pointing to the red back-wards L-shape) at the top of the Symbol Editor window to manipulate the geometry of your symbol. It is considered good design practice to create symbols of standard cells with the same size.
- **h.** Now you have completed the task of creating a Symbol from a Schematic.

# **Integrated Circuit Design CAD Tool Information**

### **14.** Inverter: Performing a Spectre Simulation on a Schematic

- **a.** You are now going to create another Cell View to test the inverter that you created in the previous section. You are going to perform DC and transient (time-dependent) simulations on the inverter. In this laboratory, you are going to use Cadence spectre to perform the simulations.
- **b.** Create a new schematic Cell View called 'inv\_test' in your EENG653 library, as shown in the figure below.

Library Mana	ger: Directoryro/cadence/ncsu-cdk-1.6.0.beta	
<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>D</u> esign Manager <u>H</u> elp		cādence
Show Categories Show Files  Library  EENG653  EENG653 EENG653 NCSU_Analog_Parts NCSU_TechLib_ami06 NCSU_TechLib_ami06 NCSU_TechLib_ismc02 NCSU_TechLib_tsmc02 NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03d NCSU_TechLib_tsmc04_4M2P basic cdsDefTechLib dave	Cell Viev Inv_test Inverter	/iew A Lock Size
Messages Log file is "/home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1 Loading NCSU Library Manager customizationsdone.	.6.0.beta/libManager.log".	

# **Integrated Circuit Design CAD Tool Information**

**c.** Open a schematic window for 'inv\_test' as shown in the figure below.

Virtuoso® Schematic Editor L Editing: EENG653 inv_test schematic							
Launch <u>F</u> ile <u>E</u> dit <u>V</u> iew <u>C</u> n	eate Chec <u>k</u> O <u>p</u> ti	ions <u>M</u> igrate <u>W</u> ir	ndow NCSU <u>H</u> elp				cādence
🗅 🗁 🛃 🕞    ♣	0 🖾 🗙 🤇	D Ty 🖬 🥱		<b>T</b>    Q Q	् 🔣 🎼 १	1, 🚈 🗝 🗄	
₩c • ○ • ○ 6	orkspace: Basic	-	l 🖪 💽 🏹	5 14 - 15 Th	🔹 🗐 🔍 Search	<b>~</b>	
Navigator ? 🗗 🗙							
🍸 Default							
🔍 Search 🔽 🗸							
Name 🛆							
陓 inv_test							
							• • • • • •
							• • • • • •
Property Editor ? B X							• • • • • •
							• • • • • •
mouse L: showClickInfo()			M: schHi	MousePopUp()		R: so	chHiMousePopUp()
6(9) >							Cmd: Sel: 0

### **Integrated Circuit Design CAD Tool Information**

**d.** Create an instance of your inverter in the Schematic window. This inverter is the one that you created in the previous section. To create this inverter, click on the 'inv\_test' Schematic Window and type 'i'. Then select 'EENG653  $\rightarrow$  inverter  $\rightarrow$  symbol' and place the symbol in the 'inv\_test' Schematic window as shown in the figure below.

	Add Instance	×
Library	EENG653 Browse	
Cell	inverter	
View	symbol	
Names		
🗹 Add Wir	e Stubs at:	
	all terminals • registered terminals only	
Array	Rows 1 Columns 1	
	🖹 Rotate 📄 🕢 🕼 Sideways 🖯 🥞 Upside Down	
	Hide Cancel Defaults Hel	p

### **Integrated Circuit Design CAD Tool Information**

e. Now create two instances of voltage sources. First you will add a pulsed voltage source. Click on the 'inv\_test' schematic window. Type 'I' in the window. Then select 'NCSU\_Analog\_Parts → Voltage\_Sources → Vpulse' and place the instance in the 'inv\_test' schematic as shown in the image below. Type "ESC".



# **Integrated Circuit Design CAD Tool Information**

**f.** Now you will edit the object properties of Vpulse as shown in the image below. For example, set 'Voltage 2' equal to 5V.

Apply To Only curre	nt 🔽 instance 🔽	
Show 🗌 system	🖌 user 🖌 CDF	
Browse	Reset Instance Labels Display	
Property	Value	Display
Library Name	NCSU_Analog_Parts	off 🔽
Cell Name	rpulse	off 🔽
View Name	symbol	off 🔽
Instance Name	10	off 🔽
(	Add Delete Modify	)
User Property	Master Value Local Value	Display
Ivsignore	TRUE	off 🔽
CDF Parameter	Value	Display
AC magnitude		off 🔽
AC phase		off 🔽
Voltage 1	0 V	off 🔽
Voltage 2	5 V	off 🔽
Delay time		off 🔽
Rise time	100n s	off 🔽
Fall time	100n s	off 🔽
Pulse width	lu s	off 🔽
Period	2u s	off 🔽
DC voltage		off 🔽
Noise file name		off 🔽
Number of noise/freq pairs	0	off 🔽
Temperature coefficient 1		off 🔽
Temperature coefficient 2		off 🔽
Nominal temperature		off 🔽

### **Integrated Circuit Design CAD Tool Information**

**g.** Now you will add a DC voltage source. Click on the 'inv\_test' schematic window. Type 'I' in the window. Then select 'NCSU\_Analog\_Parts  $\rightarrow$  Voltage Sources  $\rightarrow$  VDC' and place the instance in the 'inv\_test' schematic as shown in the 'inv\_test' schematic image above. Type "ESC". Set the voltage source equal to 3V by editing the properties with 'a'.

	Edit Object Properties	×					
Apply To Only curr	rent 🔽 instance 🔽						
Show system V user V CDF							
2 0,000							
Browse	Reset Instance Labels Display						
Property	Value	Display					
Library Name	NCSU_Analog_Parts	off 🔽					
Cell Name	vdc	off 🔽					
View Name	symbol	off 🔽					
Instance Name	off 🔽						
	Add Delete Modify						
User Property	Master Value Local Value	Display					
Ivsignore	TRUE	off					
CDF Parameter	Value	Display					
AC magnitude		off 🔽					
AC phase		off 🔽					
DC voltage	3 4	off 🔽					
Noise file name		off 🔽					
Number of noise/freq pairs	0	off 🔽					
Temperature coefficient 1		off 🔽					
		off 🔽					
Temperature coefficient 2							

### **Integrated Circuit Design CAD Tool Information**

- **h.** Now you will add a capacitor. Click on the 'inv\_test' schematic window. Type 'I' in the window. Then select 'NCSU\_Analog\_Parts  $\rightarrow$  R\_L\_C  $\rightarrow$  cap' and place the instance in the 'inv\_test' schematic as shown above.
- **i.** Now connect these components with wires. Click on the 'inv\_test' schematic window. Type 'w' in the window and add wires to connect the components as shown in the 'inv\_test' schematic.

#### **Integrated Circuit Design CAD Tool Information**

**j.** Label the ground and supply wires as shown in the 'inv\_test' schematic by adding a wire name. To add a wire name and thereby label a wire, click on the wire and then type 'l' in the schematic. Type the desired name of the wire. This example shown the label for the wire called 'vdd!'. The use of the '!' indicates that this name is a global wire in the circuit. Two examples of global wires are 'vdd!' and 'gnd!' in your schematic. With the use of '!', you do not need to have separate pins for the supply terminals of each cell, and it is therefore convenient to use 'vdd!' and 'gnd!' to simplify the circuit.

	Add V	Vire Name		X
Wire Name	Net Expression			
Names	vdd!			
Font Height	0.0625	Bus Expansion	🖲 off 🔾 on	
Font Style	stick 🔽	Placement	🖲 single 🔾 multiple	
Justification	lowerCenter	Purpose	🖲 label 🔾 alias	
Entry Style	fixed offset 🔽	Bundle Display	🖲 horizontal 🔾 vertic	al
		Sh	ow Offset Defaults	
A Rotate				
		Hide Ca	ncel Defaults He	p

### **Integrated Circuit Design CAD Tool Information**

**k.** Label the net that is input to the inverter as 'InputNet' and the net that is output from the inverter as 'OutputNet' as shown in the schematic below. Now you have labeled all of the nets.



### **Integrated Circuit Design CAD Tool Information**

 Now you will Check and Save your schematic. Click on the schematic editor for your 'inv\_test' schematic. Select 'File → Check & Save.' The Check & Save should run without errors, as indicated in the log file in the CIW as shown in the image below.

C	Virtuoso® 6.1.5-64b - Log: /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/CDS_03162012.log	_ 🗆 🗙
File <u>T</u> ools <u>O</u> ptions <u>H</u> el	p	cādence
*WARNING* hiDeleteForm *WARNING* hiDeleteForm (etting schematic prope *WARNING* hiDeleteForm *WARNING* hiDeleteForm Symbol (invester symbol Symbol (invester symbol NG* (SGM-1061): Comple Adding OB* information Adding base cell of Adding base cell of HiDeleteForm *WARNING* hiDeleteForm *WARNING* hiDeleteForm	: Cannot delete a form that is mapped or from within the form's callback (_schHiSaveAsForm) : Ould not delete a form that is mapped or from within the form's callback (_schHiSaveAsForm) : Cannot delete a form that is mapped or from within the form's callback (_schHiSaveAsForm) : Ould not delete a faready created form _schHiSaveAsForm Or bagdetting schematic propert bag 1) generated and saved in library FERNOSS3 ted generating design in library FERNOSS3 as "inverter" "symbol".  DF parameter information PF simulation information PF ashultion information P label display information E label te a form that is mapped or from within the form's callback (_schHiSaveAsForm) : Ould not delete a freedy created form _schHiSaveAsForm	
Library Manager new cel	llview request for library "EEN0653".	
Library Manager new cel Getting schematic prope Getting schematic prope Getting schematic prope Getting schematic prope	llviev request for cell "EENG653 inverter". ert bag ert bag ert bag	
Library Manager new cel Getting schematic prope	llview request for cell "EEN0653 inverter". ert bag	
vdd (instance "I1", lib	brary "NGSU_Analog_Parts")	
wire drawing -> boundir	ng box: (0.62,-2.94) (0.62,-2.38)	
wire drawing -> boundir *WARNING* hiDeleteForm *WARNING* hiCreateForm Getting schematic prope	ng box: (-0.38,1.06) (-0.38,1.62) : Damot delste a form that is mapped or from within the form's callback (_schHiSaveAsForm) : Could not delste already created form _schHiSaveAsForm ert bag0etting schematic propert bag	
vdc (instance "V1", lib	brary "NGSU_Analog_Parts")	-
vpulse (instance "VO", INFO (SCH-1170): Extrac INFO (SCH-1426): Schema Getting schematic prope	library "NOSU_Analog_Perts") ting "inv_test schematic" sic check completed with no errors. ert bagGetting schematic propert bagINFO (SCH-1181): "EENG653 inv_test schematic" saved.	
		8
mouse L: showClickInfo0	markinusePoolin∂	B: schHiMousePopl Ip0
1		

### **Integrated Circuit Design CAD Tool Information**

**m.** Now you will start the Spectre simulator. In the 'inv\_test' schematic, click on 'Launch  $\rightarrow$  ADE L' and click on 'Yes' to check out a license. One new window will appear with the title Virtuoso B Analog Design Environment in the banner at the top of the window as shown below.

ADE L CO	/irtuos	o® Anal	og Desig	n Envir	onment (1	L) - EEN	IG653	inv_te	st sch	ematic		
Session	Setup	Analyses	Variables	Outputs	Simulation	Results	Tools	Help			cāden	ce
III 27		_	_	_	_	_		_		_	_	
Design V	ariables			An	alyses	1					? 🖥 🗙	
N	ame	V	alue	T    ''	/pe   Enable	!		Argun	nents			Trans
												1
												>⊜→ >⊜→
												×
				Ou	itputs						? 🖥 🗙	0
					Name/Signa	l/Expr	Valu	ie   Plot	Save	Save C	ptions	M
												<u>V</u> V
				U		_						
>				Plot	after simulati	on: Auto		Plotti	ng mode	e: Replace	<b>_</b>	
mouse L	.:				M:							R:
7(10) PI	ot Outpu	ts					Status	Ready	T=27	C Simu	ilator: spec	tre
#### **Integrated Circuit Design CAD Tool Information**

n. A second window may also appear titled 'Virtuoso ® Visualization & Analysis XL' window as shown below. If this window does not appear, it will show up later when you are plotting the waveforms from your schematic. (As a heads up, this will involve running a simulation and then selecting 'ADE→Results→Direct Plot→Transient Signal' after which the window will appear).



#### **Integrated Circuit Design CAD Tool Information**

**o.** In the Virtuoso (a) Analog Design Environment 'inv\_test' schematic window, click 'Setup  $\rightarrow$  Simulator/Directory/Host' and select 'spectre' as the simulator in the window that appears. Then click 'OK' in the 'Choosing Simulator/Directory/Host' window. The field for the Project Directory specifies the location where all the simulation files are written. Files in this directory should be removed regularly so that you have enough space for your simulations.

🔲 Choosing Sir	nulator/Directory/Host Virtuoso® Analog Desi 🗙
Simulator	spectre
Project Directory	<pre>~/cadence/ncsu-cdk-1.6.0.beta</pre>
Host Mode	🥑 local 🔾 remote 🔾 distributed
Host	
Remote Directory	
	OK Cancel Defaults Apply Help

## **Integrated Circuit Design CAD Tool Information**

- - i. /apps/vlsi/ncsu-cdk-
    - 1.6.0.beta/models/spectre/nom/ami06N.m
  - ii. /apps/vlsi/ncsu-cdk-
    - 1.6.0.beta/models/spectre/nom/ami06P.m

spectre0: Model Library Setup	×
Model File ⊡ Global Model Files Mapps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m Mapps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m Click here to add model file>	Section
ОК	Cancel Apply Help

#### **Integrated Circuit Design CAD Tool Information**

**q.** Now you will save these settings. In the Virtuoso ® Analog Design Environment, click on 'Session → Save State' and a window will appear. This window is the 'Saving State' window shown below. Each time you run the simulation, you can load the previous session so you do not need to load the model paths again.

Saving Stat	e Virtuo	so® Analog Desigr	n Environment	(L) ×
Save State Option	۲	) Directory 🔾 Cellview		
Directory Options				
State Save Directory	~/.artis	t_states		Browse
Save As	state1			
Existing States				
Cellview Options				
Library	EENG653	•		
Cell	inv_test	Browse	4	
State	spectre_s	tate1 -		
What to Save				
			Select All Clea	r All
🗹 Analyses		🗹 Variables	🗹 Outputs	
🗹 Model Setup		Simulation Files	🗹 Environment O	ptions
✓ Simulator Option:	3	Convergence Setup	☑ Waveform Setu	р
✓ Graphical Stimuli		Conditions Setup	✓ Results Display	/ Setup
Device Checking     Turba and Paradi	j Setup itis Roduction	MDL Control Sotup	Cosimulation C	ptions
<ul> <li>Parameterization</li> </ul>	Setup	<ul> <li>Moc control setup</li> </ul>	<ul> <li>Distributed FI0</li> </ul>	cessing
			K Cancel A	pply Help

#### **Integrated Circuit Design CAD Tool Information**

**r.** Now you are going to do a DC analysis and a transient (timedependent) analysis of your inverter. To select the DC analysis type, in the Virtuoso (a) Analog Design Environment window, click on 'Analyses  $\rightarrow$  Choose', and a 'Choosing Analyses' window will appear as shown in the image below. In the 'Choosing Analyses' window select the 'dc' radio button and click the box for 'Save DC Operating Point'.

🗖 Choosin	g Analys	es Vir	tuoso® Ai	nalog Design E 🗙			
Analysis	🔾 tran	🖲 dc	🔾 ac	🔾 noise			
	🔾 xf	🔾 sens	🔾 dcmatch	🔾 stb			
	🔾 pz	🔾 sp	🔾 envlp	🔾 pss			
	🔾 pac	🔾 pstb	🔾 pnoise	🔾 pxf			
	🔾 psp	🔾 qpss	🔾 qpac	🔾 qpnoise			
	🔾 qpxf	🔾 qpsp	🔾 hb	🔾 hbac			
	🔾 hbnoise	e					
		DC Ana	lysis				
Save DC O	perating Poi	nt 🔽					
Hysteresis S	Sweep						
Sweep Va	Sweep Variable						
lemper	ature						
Design	Variable 	*					
	nent Parame Devemeter	ler					
	Parameter						
Enabled ⊻				Options			
	0	Canc	el Default	ts Apply Help			

#### **Integrated Circuit Design CAD Tool Information**

**s.** To select the Transient analysis type, in the Virtuoso  $\mathbb{R}$  Analog Design Environment window, click on 'Analyses  $\rightarrow$  Choose', and a 'Choosing Analyses' window will appear as shown in the image below. In the 'Choosing Analyses' window select the 'tran' radio button and set the field 'Stop Time' equal to 10 microseconds (10  $\mathbb{Z}$ s).

🗖 Choosin	g Analys	es Vir	tuoso® A	nalog Design E 🗙	
Analysis	🖲 tran	🔾 dc	🔾 ac	🔾 noise	
	⊖ ×ſ	🔾 sens	🔾 dcmatch	🔾 stb	
	🔾 pz	🔾 sp	🔾 envlp	🔾 pss	
	🔾 pac	🔾 pstb	🔾 pnoise	⊖ p×f	
	🔾 psp	🔾 qpss	🔾 qpac	🔾 qpnoise	
	🔾 qpxf	🔾 qpsp	🔾 hb	🔾 hbac	
	🔾 hbnoise	!			
		Transient /	Analysis		
Stop Time	10u				
Accuracy	Defaults (err	preset)			
Conse	rvative 🗹 i	noderate	📃 liberal		
🔲 Transier	Transient Noise				
Dynamic Parameter					
Enabled ⊻				Options	
	0	Cano	el Defaul	ts Apply Help	

#### **Integrated Circuit Design CAD Tool Information**

Virtuoso® 6.1.5-64b - Log: /home/afiten3/fac/mianzero/cadence/ncsu-cdk-1.6.0.beta/CDS_03162012.log	
File Tools Options Help	cādence
<pre>generate netlist Loading spectreinl.cxt Loading spectreinl.cxt Initializing the control file using cp:</pre>	Â
End metlisting Mar 16 18:52:06 2012 ERROR (OSSENL-514): Netlisting failed due to errors reported before. Netlist may be corrupt or may not be produced at all. Fix reported errors and netlist again. Loading devCheck.cxt INPO (SCH-1426): Schematic check completed with no errors. Getting schematic propert bagGetling schematic propert bagINFO (SCH-1101): "EEN0653 inverter schematic" INPO (SCH-1426): Schematic check completed with no errors. Getting schematic propert bagGetling schematic propert bagINFO (SCH-1101): "EEN0653 inverter schematic" INPO (SCH-1426): Schematic check completed with no errors. Getting schematic propert bagGetling schematic propert bagINFO (SCH-1181): "EEN0653 inv_test schematic" Schematic propert bagGetling schematic propert bagINFO (SCH-1181): "EEN0653 inv_test schematic" Bejon / Action / home/Afiten3/Fac/Alanzero/cadence/ncsu-cdk-1.6.0.beta/inv_test/spectre/schematic/psf. Bejon Incremental. Netlisting Mar 16 18:52:48 2012 NetListing Statistics:	
Number of components: 6 Elapsed time: 1.0s (6.00/s) Errors: 0 Warnings: 0 successful. compose simulator input file successful. start simulator. if needed successful. Loading paraplet.ctt simulate INFO (ADE-3071): Simulation completed successfully. reading simulation data successful.	
Image:	R:

#### **Integrated Circuit Design CAD Tool Information**

u. Now you can visualize the simulation results. To see the results of the DC analysis, in the Virtuoso 
 ® Analog Design Environment, click on 'Results →Annotate →DC Node Voltages'. The results will be displayed in the schematic window with circuits.



#### **Integrated Circuit Design CAD Tool Information**

v. To see the results of the transient analysis, in the Virtuoso ® Analog Design Environment, click on 'Results →Annotate →Transient Node Voltages'. Your cursor will move to the schematic window. To visualize the time-dependent values of the voltages on nets, click on the 'InputNet' and 'OutputNet' wires. The nets will become red and pink dashes after you click on them. (To visualize time-dependent values of current, click on nodes.)



#### **Integrated Circuit Design CAD Tool Information**

**w.** After you have selected the wires, and they have become dashed, click 'ESC' in the window. A new Virtuoso ® Visualization & Analysis XL window appears as shown here. (Remember, this window may have appeared earlier as mentioned previously).

NN .	Virtuoso (R) Visualizatio	on & Analysis XL		
<u>File Edit View G</u> raph <u>A</u> xis <u>T</u> race <u>M</u> arker	M <u>e</u> asurements T <u>o</u> ols <u>W</u> indow <u>B</u> rov	vser <u>H</u> elp		cādence
📕 🥱 🦿 🐕 🗋 💼 🗶 🛛 Layout: Auto	Subwindows:ient Response	e 🔽 🛛 Workspace: Classic	- 🖬 🚭	
I 🖸 🔍 🍳 🝳 🔹 I 🖉	I 🕨 🕖 I 🗮 🍈 🛣			
EENG653 inv_test schematic				
Transient Response				
Name				<u>}</u>     >
VT("/InputNet") 6				
5 -				
4 -1				
3 -				
8				
× 1				
1 -				
o 7				
0.0	2.5	5.0	7.5	10
		time (us)		
8(13) plot new graph subwindow				

#### **Integrated Circuit Design CAD Tool Information**

x. As mentioned previously, a second method to display the 'InputNet' and 'OutputNet' waveforms is to select 'ADE→Results→Direct Plot→Transient Signal.' Then on the Schematic, click on the 'InputNet' and 'OutputNet' and then click ESC. The waveforms will appear as shown in the plot above in the Visualization & Analysis XL window.

# **Integrated Circuit Design CAD Tool Information**

**y.** The spectre.out file that lists the output log file for the spectre simulator is shown below (divided into two parts for clarity).

C	/home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/inv_test/spectre/schematic/psf/spectre.out	
<u>F</u> ile <u>H</u> elp	cāder	nce
Cadence (R) V Version 10.1. Copyright (C)	irtuoso (R) Spectre (R) Circuit Simulator 1.218 inr14 64bit 5 Sep 2011 1999-2010 Cademace Design Systems, Inc. All rights reserved worldwide. Cadence, Wirtuoso and Spectre are registered trademarks of	Ca
Protected by 5,610 6,088 6,349 6,778 7,085	U 8, Paranta. 847, 5,700.436; 5,812,431; 5,859,785; 5,949,992; 5,967,238; 5533,6,101,323; 6,151,698; 6,181,754, 6,250,176; 6,279,964 272; 6,374,390; 6,439,849; 6,504,885; 6,618,437, 6,538,839, 0255, 6,822,586; 6,851,097; 6,926,066; 7,024,652; 7,035,782; 700,71,43,821; 7,439,240; 7,571,401.	
Includes RSA User: mlanzer Memory avail CPU Type: Int Pro	Display         Constraint         Constraint <thconstraint< th="">         Constraint         Constraint&lt;</thconstraint<>	H
Simulating `i Environment v SPECTRE D Command line: /apps/vls input +npss +lqti spectre pid =	put.scs' on vlsilab05 at 6.52.51 PM. Fri Mar 16, 2012 (process id: 9966). ariable: grAULTS-E //cdance.ofMSIM101/tools lnx85/spectre/bin/6dbit/spectre \ .scs =sechars =log/psf/spectre.out =inter=mpsc \ .scs =sechars = log/psf/spectre.out = inter=mpsc \ meeut 900 = maxw 5 =maxm 5	
Loading /apps Loading /apps Loading /apps Loading /apps	Vpis/Cadence/MSIMIO/Looll 1006/cm/11b/CAbir/5.071binfineen_sh.so Vpis/Cadence/MSIMIO/Looll 1006/cm/11b/CAbir/5.071binping-sh.so Vpis/Cadence/MSIMIO/Looll 1006/cm/11b/CAbir/5.071binping-sh.so	
Time for NDB Time accumula Peak resident	Parsing, CPU = 90, 985 ms, elapsed = 2, 19821 s. ted: CPE = 90 985 ms, elapsed = 2, 19821 s. memory used = 34,1 M5ytes.	l
Time for Elab Time accumula Peak resident	oration, 020 = 16.998 ms, elapsed = 57.3261 ms. ted: 029 = 107.988 ms, elapsed = 2.25568 s. memory used = 38.1 Mbytes.	l
Time for EDB Time accumula Peak resident	Visiting: CPU = 0 s. etagosed = 20.493 ms. tod: CPU = 107 NoS ms. etagosed = 2.27629 s. memory used = 38.4 Mbytes.	l
Circuit inven b cap v	tory nodes 3 simJy3 2 scitor 1 source 2	l
Tine for pars Tine accunula Peak resident	ing: CPU = 2 ms, elapsed = 28.204 ms bed: CPU = 109 983 ms, elapsed = 2.30459 s. menory used = 39.1 Mbytes.	I
Entering remo Warning from	te command mode using NPSC service (spectre, ipi, v0.0, spectre0_9104_1, ). spectre.	ł
WAÉNING (	SPECTRE-16707): Only tran supports psfxl format, result of other analyses will be in psfbin format.	ł
Inportant par reltol = abstol(Y) ubstol(I) temp = 27 tompeffec gmindc = Convergence a Total time re Time accumula Peak resident	<pre>**** Subject Control Cont</pre>	
dc0pInfo: wri	ting operating point information to rawfile.	
<pre>**************** Transient Ana ************ Important par start = 0 outputsta stop = 10 step = 10 navstep = ic = all useprevic</pre>	yusi 'tran' time = (0 s -> 10 us) meter values: * t = 0 s us 200 ns =	

# **Integrated Circuit Design CAD Tool Information**

**z.** The second part of the spectre.out file that lists the output log file for the spectre simulator is shown below (divided into two parts for clarity).

C	/home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/inv_test/spectre/schematic/psf/spectre.out	
<u>E</u> ile J	Helb	cādence
		<u></u>
Time f	or parsing: CPU = 2 ms, elapsed = 28.204 ms. ccumulated: CPU = 109.983 ms, elapsed = 2.30459 s.	
Peak r	esident memory used = 39.1 Mbytes.	
Warnin	ng remote command mode doing miso service (species, ipi, vo.o, species_ion_i, ). ng from spectre.	
NY.	ÍNNNG (SÞECTRE-16707): Only tran supports psfxl format, result of other analyses will be in psfbin format.	
******	*******	
****** Import	ant parameter values:	
re ab	ltol = 1e-03 $stol(\Psi) = 1 u\Psi$	
te:	stou(1) = 1 pn mp = 27 C ms = 27 C	
te: gn	mpeffects = all indc = 1 pS	
Conver Total	gence achieved in 12 iterations. time required for dc analysis 'dcOp': CPU = 1 ms, elapsed = 19.1212 ms.	
Peak r	ccumulaced: GPU = 110.903 m8, elapsed = 2.33424 8. esident memory used = 39.7 Mbytes.	
dc0pIn	fo: writing operating point information to rawfile.	
Transi	ent Analysis `tran': time = (0 s -> 10 us)	
Import	ant parameter values: art = 0 s	
ou st	tputstart = 0 s op = 10 us	
st na	rop = 10 ns ratep = 200 ns 	
us sk	previc = no ipdc = no	
re ab	ltol = 1e-03 stol(W) = 1 uW	
te:	stou(1) = 1 pn mp = 27 C on = 27 C	=
ter	mpeffects = all rpreset = moderate	
ne lt	thod = traponly eratio = 3.5	
CTR CTR	ine = Sigglobal	
tr	an: time = 304.1 ns (3.04 %), step = 100.9 ns (1.01 %)	
tr	an: time = 904.1 ns (9.04 %), step = 200 ns (2 %) an: time = 1.255 us (12.6 %), step = 5.287 ns (52.9 m%) ma time = 1.940 us (19.5 %) step = 50.287 ns (52.9 m%)	
tr	an: time = 2.271 us (22.7 %), step = 84.51 ns (845 m%) an: time = 2.241 us (22.7 %), step = 84.51 ns (845 m%) an: time = 2.64 us (28.4 %), step = 200 ns (2 %)	
tr	an: time = 3.25 us (32.5 %), step = 8.532 ns (85.3 m%) an: time = 3.852 us (38.5 %), step = 147.6 ns (1.48 %)	
tr	an: time = 4.28 us (42.8%), step = 88.78 ns (888 m%) an: time = 4.857 us (48.6%), step = 200 ns (2%) The time = 52 us (25.5%) = time = 8.666 ms (26.5%)	$\cup$
tr	and the set of the se	
tr	an: time = 6.897 us (69 %), step = 200 ns (2 %) an: time = 7.251 us (72.5 %), step = 2.748 ns (27.5 m%)	
tr	an: time = 7.839 us (78.4 %), step = 160.9 ns (1.61 %) an: time = 8.295 us (82.9 %), step = 96.33 ns (963 m%)	
tr	an: time = 9.823 us (92.6 %), step = 10.21 ns (102 m%) an: time = 9.823 us (92.6 %), step = 200 ns (2 %)	
Number	of accepted tran steps = 284	
Notice	from spectre during transient analysis 'tran'. apezoidal ringing is detected during tran analysis. Please use method+trap for better results and performance.	
Initia	l condition solution time: CPU = 0 s, elapsed = 70.0951 us.	
Total Time a	time required for tran analysis 'tran': CPU = 11.999 ns. elapsed = 30.966 ns. coumlated: CPU = 124.98 ns. elapsed = 2.39521 s.	
Peak r	esident nemory used = 40.6 Mbytes.	
nodelP	imeor: writing operating point information to rawfile. arameter: writing model parameter values to rawfile. t: writing instance parameter values to rawfile.	
design	Parameter' writing output parameter values to rawfile. ParamVals: writing netlist parameters to rawfile.	
primit	ives: writing primitives to rawfile. s: writing subcircuits to rawfile.	
11 He	IpAction	
	· · · · · · · · · · · · · · · · · · ·	

# **Integrated Circuit Design CAD Tool Information**

**aa.** Click on the input waveform in the "Virtuoso Visualization & Analysis XL" window to display the waveform as a dashed, bold line as shown in the image below.

NN		Virtuoso (R) Vis	sualization & Anal	ysis XL		
<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>G</u> rap	ih <u>A</u> xis <u>T</u> race <u>M</u> arker	M <u>e</u> asurements T <u>o</u> ols <u>W</u> ii	ndow <u>B</u> rowser <u>H</u> elp			cādence
I 🥱 🦿 🎽 🗋	💼 🗙 🛛 Layout: Auto	Subwindows:ie	nt Response 🔽 🛛 Wo	rkspace: Classic		
	»	N 🕐   Aug 📣				
EENG653 inv_tes	t schematic 🛛					
Transient Response						
Name	<					
VT("/InputNet")	6 7					
	5	;;	[			
	4 -					
	s i					
	>					
	2 -					
	1 -					
	o -					
	0.0	2.5		5.0	7.5	10
			tim	e (us)		
mouse L: 33(88) Calculator			M:			R:

#### **Integrated Circuit Design CAD Tool Information**

**bb.** Right-click on the bold dashed line (the input waveform) and select "Table → New Window." Notice when you move the cursor over the dashed line, the (x, y) coordinates of the waveform are displayed. The table below shows all coordinates.

Ite         Yiew         Tools         Help           ImputNet	irtuoso (R) Vis	sualization & Analysis XL Table 📃 🗆
InputNet         Image           100         00           2.029E-9         100           3.0007E-9         100           2.029E-9         100           3.0007E-9         100           2.209E-9         100           2.209E-9         100           2.209E-9         100           2.209E-9         11           2.209E-9         133           2.209E-9         133           2.209E-9         133           3.07E-9         15           3.007E-9         15           3.007E-9         2.4           3.007E-9         2.4           5.005E-9         3.0           6.634E-9         3.1           7.038E-9         3.3           7.038E-9         3.3           7.038E-9         3.6           7.031E-9         5.6           1004E-9         4.1           2.9104E-9         5.6           1002E-9         5.6           102E-9         5.6           1037E-9         5.6           110387E-9         5.6           110387E-9         5.6           110387E-9         5.6      <	lp	cādence
ImputNet         ImputNet           0.0         0.0           2.029:-9         100           3.603E-9         110           2.029:-9         100           3.603E-9         11           2.624E-9         1.3           3.7.51E-9         1.3           3.7.51E-9         1.3           3.7.51E-9         1.3           3.7.51E-9         1.3           3.0.7E-9         1.5           3.0.7E-9         1.5           3.5046E-9         2.2           5.645E-9         3.3           7.560.25E-9         3.5           7.36E-9         3.5           7.36E-9         3.5           7.36E-9         3.5           7.36E-9         3.6           7.736E-9         3.6           7.736E-9         3.6           7.736E-9         3.6           7.736E-9         5.6           1.100E-6         5.6           1.100E-6         5.6           1.100E-6         5.6           1.100E-6         5.6           1.100E-6         5.6           1.100E-6         6.7           1.100E-6         6.7     <		
InputNet         ImputNet         ImputNet           10.0         0.0         0.0           2.2029E-9         0.0         0.0           3.603E-9         10         0.0           4.6470E-9         3.2         10.0           1.21E-9         61         2.308E-9         11.3           2.2751E-9         1.3         3.007E-9         1.8           2.20454-9         1.3         3.007E-9         1.8           2.20454-9         1.3         3.007E-9         1.8           2.2044-06-9         2.2         3.046E-9         2.5           2.5046E-9         2.6         6.034E-9         3.6           2.6045E-9         3.6         6.034E-9         3.5           2.6045E-9         3.6         6.034E-9         3.6           2.7058E-9         3.6         6.034E-9         3.6           2.7045E-9         5.6         5.6         5.6           3.1007E-9         5.6         5.6         5.6           3.1007E-9         5.6         5.6         5.7           3.1007E-9         5.6         5.7         5.7           3.1007E-9         5.6         5.7         5.7           3.1007E-9		
InputNet         Imm (s)           time (s)         1           0.0         0.0           2.028E-9         10           3.003E-9         10           4.6470E-9         32           2.236BE-9         1.1           2.242E-9         1.3           3.007E-9         1.5           3.907E-9         1.5           3.907E-9         1.5           3.907E-9         1.5           3.907E-9         1.5           3.907E-9         1.5           3.519E-9         2.7           3.5046E-9         2.5           6.634E-9         3.3           7.656E-9         3.6           7.033E-9         3.5           7.733E-9         3.5           7.733E-9         5.6           1.004E-9         4.1           2.9104E-9         4.1           2.9104E-9         5.6           1.001E-9         5.6           1.001E-9         5.6           1.001E-9         5.6           1.0101E-9         5.6           1.0101E-8         5.6           1.0101E-8         5.6           1.1010E-6         5.6     <	8	
Ilme (s)           0.0         0.0           2.028E-9         0.0           3.603E-9         10           3.603E-9         10           2.360E-9         10           2.360E-9         11           7.2624E-9         13           3.007E-9         18           3.007E-9         15           3.307E-9         15           3.307E-9         15           3.307E-9         15           2.426E-9         2.7           3.90E-9         2.7           5.046E-9         2.7           5.045E-9         2.7           5.045E-9         3.3           7.033E-9         3.5           9.738E-9         3.6           9.738E-9         3.6           9.738E-9         5.6           1004E-9         4.1           2.9104E-9         5.6           1004E-9         5.6           1004E-9         5.6           10316-9         5.6           10316-9         5.6           10316-9         5.6           10316-9         5.6           10316-9         5.6           113176-6		
0.0         0.0           1.0.0         0.0           2.028-9         10           3.303E-9         10           2.2028-9         10           2.2028-9         13           2.251E-9         13           2.251E-9         13           3.007E-9         13           3.519E-9         17           3.5025E-9         33           6.634E-9         33           7.56625E-9         36           7.738E-9         56           7.738E-9         56           7.738E-9         56           1.000E-9         56           1.000E-9         56           1.108E-9         56           1.108E-9         56           1.108E-9         56           1.108E-6         16           1.108E-6         16           1.108E-6         16           1.108E-6         16           1.108E-6 <th>InputNet (V)</th> <th></th>	InputNet (V)	
2         1.262-3         1.603           3.603-9         1.64         6.470E-9         3.2           3.603-9         1.64         6.470E-9         3.2           1.21E-9         1.1         3.2         3.2         1.1           2.64E-9         1.1         3.3         3.07E-9         1.5           3.309E-9         1.8         3.309E-9         1.8           3.309E-9         1.9         2.4         4.6           3.539E-9         2.7         1.7         3.939E-9         2.5           4.4.26E-9         2.5         5.60.25E-9         3.6         6.34E-9         3.5           5.60.25E-9         3.6         6.34E-9         3.5         7.86E-9         3.5           7.646E-9         2.5         3.7         7.86E-9         3.6         7.33E-9         3.5           7.7.34E-9         5.6         5.05         7.6         5.6         5.05 <td< td=""><th>01 55 2</th><td></td></td<>	01 55 2	
0.400-5         0.200-5           0.4700-9         0.2           0.2121-9         0.1           0.2368-9         1.1           2.2424-9         1.3           0.307-9         1.8           0.3519-9         1.9           2.4426-9         2.3           0.3519-9         1.9           2.4428-9         2.3           5.5046-9         2.5           5.5046-9         2.5           5.6025E-9         3.0           7.6556E-9         3.1           7.6556E-9         3.2           7.733E-9         3.8           9.7338E-9         3.8           9.7338E-9         3.8           9.7338E-9         3.8           9.7338E-9         3.8           9.7338E-9         3.8           9.7338E-9         3.8           9.7838E-9         4.1           2.9104E-9         5.6           1000E-9         5.6           10316-9         5.6           110316-9         5.6           110316-9         5.6           110316-9         5.6           110316-6         5.6           110100E-6         5.6 </td <th>01.5E-3 80.1E-3</th> <td></td>	01.5E-3 80.1E-3	
12.21E-9         6           12.21E-9         6           28.24E-9         1.3           3 27.51E-9         1.3           3 3007E-9         1.7           3 900F-9         1.7           3 900F-9         1.7           3 900F-9         1.7           3 900F-9         1.8           3 519E-9         1.7           3 900F-9         2.2           5 046E-9         2.2           5 045E-9         3.6           6 634E-9         3.8           7 033E-9         3.6           7 7.36E-9         3.6           0 70.37E-9         5.6           0 70.75F-9         5.6           1000E-9         5.6           1000E-9         5.6           1000E-9         5.6           1000E-9         5.6           1000E-9         5.6           1010E-6         5.6           1100E-6         7.6 <tr< td=""><th>323.5E-3</th><td></td></tr<>	323.5E-3	
a         23.86E-9         1.1           a         25.86E-9         1.3           a         27.51E-9         1.3           a         30.07E-9         1.8           a         30.07E-9         1.8           a         30.07E-9         1.8           a         30.07E-9         1.7           a         30.07E-9         1.7           a         30.07E-9         2.5           a         50.46E-9         2.2           a         50.30E-9         2.6           b         60.34E-9         3.6           a         7.30E-9         3.6           a         7.30E-9         3.6           a         7.30E-9         5.6           a         7.30E-9         5.6           a         100.00E-9         5.6           a         100.00E-9         5.6           a         100.00E-9         5.6           a         100.00E-9         5.6           a         17.47E-9         5.6           a         17.47E-9         5.6           a         17.47E-9         5.6           a         17.47E-6         1.7	610.3E-3	
$\begin{array}{c} 2 & 2 & 2 & 2 & 4 & 4 & -9 & 1 & 3 \\ 2 & 2 & 7 & 5 & 1 & -9 & 1 & 3 \\ 3 & 3 & 0 & 7 & -9 & 1 & 9 & 1 \\ 3 & 3 & 0 & 7 & -9 & 1 & 9 & 1 \\ 3 & 3 & 0 & 7 & -9 & 1 & 9 & 1 \\ 2 & 4 & 2 & 6 & -9 & 2 & 2 & 1 \\ 5 & 5 & 0 & 2 & 6 & -9 & 2 & 2 \\ 5 & 5 & 0 & 2 & 5 & -9 & 2 & 7 \\ 5 & 0 & 2 & 5 & -9 & 2 & 7 \\ 5 & 0 & 2 & 5 & -9 & 3 & 3 & 5 \\ 7 & 0 & 5 & 6 & -3 & 3 & 3 & 5 \\ 7 & 0 & 5 & 6 & -3 & 3 & 3 & 5 \\ 7 & 0 & 5 & 6 & -3 & 3 & 3 & 5 \\ 7 & 0 & 5 & 6 & -3 & 3 & 3 & 5 \\ 7 & 0 & 5 & 6 & -3 & 3 & 3 & 5 \\ 7 & 0 & 5 & 6 & -3 & 3 & 3 & 5 \\ 7 & 0 & 5 & 6 & -3 & 3 & 3 & 5 \\ 7 & 0 & 5 & 0 & 2 & 5 & -9 & 5 & 6 \\ 7 & 10 & 0 & -9 & 5 & 6 & 5 \\ 1 & 0 & 0 & 1 & -9 & 4 & 4 \\ 2 & 9 & 1 & 0 & 0 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 4 & 4 \\ 2 & 9 & 1 & 0 & 0 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 5 & 6 \\ 1 & 10 & 0 & 1 & -9 & 5 & 6 \\ 1 & 11 & 0 & 1 & -6 & 1 & 7 \\ 1 & 11 & 0 & 1 & -6 & 1 & 7 \\ 1 & 11 & 0 & 1 & -6 & 1 & 7 \\ 1 & 11 & 0 & 0 & -6 & 0 & 0 \\ 1 & 1 & 2 & 0 & 0 & -6 & 0 & 0 \\ 1 & 1 & 2 & 0 & 0 & -6 & 0 & 0 \\ 1 & 1 & 0 & 0 & -6 & 0 & 0 \\ 1 & 1 & 0 & 0 & -6 & 0 & 0 \\ 1 & 1 & 0 & 0 & -6 & 0 & 0 \\ 1 & 1 & 0 & 0 & -6 & 0 & 0 \\ 1 & 1 & 0 & 0 & -6 & 0 & 0 \\ 1 & 1 & 0 & 0 & -6 & 0 & 0 \\ 1 & 1 & 0 & 0 & -6 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & -5 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & -5 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 &$	.184	
2         3.017-5         1.5           3.007-5         1.5           3.007-5         1.5           3.307-5         1.5           3.307-5         1.7           3.307-5         1.7           3.307-5         1.7           3.307-5         2.7           5.046E-9         2.7           5.046E-9         2.7           5.046E-9         2.7           5.046E-9         2.7           5.046E-9         3.1           7.036E-9         3.8           7.036E-9         3.8           7.037-9         3.8           9.738E-9         3.6           0.70.11E-9         3.6           1.000E-9         5.6           1.004E-9         4.1           2.104E-9         5.6           1.105E-9         5.6           1.105E-9         5.6           1.105E-9         5.6           1.106E-6         4.5           1.107E-6         5.6           1.108E-6         1.8           1.108E-6         1.8           1.108E-6         1.8           1.108E-6         1.8           1.108E-6         1.8 </td <th>.312</th> <td></td>	.312	
38.19E-3         1.7.           39.30E-3         1.7.           39.30E-3         1.7.           39.30E-3         1.7.           39.30E-3         1.7.           39.30E-3         1.7.           39.30E-3         2.2.           35.442E-3         2.2.           56.35E-3         3.6.           66.34E-3         3.3.           7.36E-3         3.6.           7.36E-3         3.6.           7.36E-3         3.6.           31.00E-3         5.6.           31.00E-3         5.6.           31.00E-3         5.6.           31.00E-3         5.6.           31.00E-3         5.6.           31.00E-5         5.6.           31.00E-5         5.6.           31.00E-5         5.6.           31.00E-5         5.6.           31.10E-6         5.6.           31.10E-6         5.6.           31.10E-6         5.6.           31.10E-6         5.6.           31.10E-6         5.6.           31.10E-6         7.6.           31.10E-6         7.6.           31.10E-6         7.6.           31.10E-6	.376	
39.00-9         1           24.426E-9         2           55.46E-9         2           55.46E-9         2           55.46E-9         2           55.025E-9         3           66.34E-9         3           76.36E-9         3           70.32E-9         3           97.33E-9         3           97.34E-9         3           97.34E-9         3           97.34E-9         5           97.34E-9         5           1000E-9         5           29.04E-9         5           29.04E-9         5           29.04E-9         5           29.04E-9         5           20.02E-9         5           2105E-9         5           2105E-9         5           2105E-9         5           2137E-9         5           2147E-9         5           2174E-6         3           2174E-6         1           2174E-6         1           2174E-6         1           2174E-6         1           2174E-6         1           2174E-6         1	.760	
2 44.26E-9 2.2 3 50.46E-9 2.2 4 55.93E-9 2.7 5 60.25E-9 3.7 7 60.56E-9 3.7 7 0.35E-9 3.7 9 7.33E-9 3.5 9 7.34E-9 4.1 2 91.04E-9 4.5 100.E-9 5.5 100.E-9 5.5 109.E-9 5.5 109.E-9 5.5 109.E-9 5.5 129.4E-9 5.5 11.10E-6 4.5 11.10E-6 4.5	.995	
3         3         54.86E-9         2           4         55.93E-9         3         3           5         60.25E-9         3         3           6         5.34E-9         3         3           7         365.6E-9         3         3           7         73.8E-9         3         3           73.8E-9         3         3         3           73.8E-9         3         8         3           97.38E-9         3         8         3           97.38E-9         3         8         3           97.38E-9         5         10         7           103.4E-9         4         1         1         1           104.9         5         1         5         1           1100.0E-9         5         6         1         5           1158.4E-9         5         1         1         6           1130.7E-9         5         5         1         1         6           1100.7E-6         4         1         6         1         6           1100.7E-6         4         1         1         6         1         6 <t< td=""><th>2.214</th><td></td></t<>	2.214	
4         30.30E-3         2.5           6         60.25E-3         3.6           6         60.25E-3         3.6           7         60.56E-9         3.3           7         303E-9         3.8           9         7.30E-9         3.6           100.0E-9         5.6         105.7E-9           2         91.04E-9         4.5           3         100.0E-9         5.6           102.0E-9         5.6           103.0E-9         5.6           104.0E-9         5.6           124.9E-9         5.6           136.7E-9         5.6           1376.7E-9         5.6           1376.7E-9         5.6           1376.7E-9         5.6           1376.7E-9         5.6           1100E-6         5.6           1100E-6         5.6           1100E-6         6.6           1100E-6         1.8           1140E-6         2.1 <td< td=""><th>2.523</th><td></td></td<>	2.523	
0         0.000-5         0.000-5           0         0.000-5         0.000-5 <td< td=""><th>3.013</th><td></td></td<>	3.013	
66.56E-9         3           70.36E-9         3           73.36E-9         3           73.36E-9         3           73.36E-9         3           97.36E-9         3           97.36E-9         3           97.36E-9         3           97.36E-9         3           97.36E-9         3           97.36E-9         3           100.0E-9         5           1100.0E-9         5           1100.0E-9         5           1150.0E-9         5           1250.0E-9         5           1260.0E-9         5           1210.0E-9         5           130.7E-9         5           130.7E-9         5           130.7E-9         5           130.7E-9         5           1100E-6         4           1100E-6         4           1100E-6         1           1110E-6         1           1110E-6         1           1110BE-6         1           1110BE-6         1           1110BE-6         1           1110BE-6         1           1110BE-6         1     <	3.167	
8         70.33E-9         3           9         73.38E-9         3           9         73.88E-9         3           0         74.11E-9         3           1         0.74.11E-9         3           1         0.000E-9         5           1         10.00E-9         5           1         10.20E-9         5           1         115.8E-9         5           1         115.8E-9         5           1         116.7E-9         5           1         116.7E-9         5           1         1100E-6         5           1         1100E-6         5           1         1100E-6         5           1         1100E-6         5           1         1103E-6         1           1         1149E-6         1           1         1149E-6         1           1         1149E-6         1           1         1130E-6 <th>3.328</th> <td></td>	3.328	
3         73.88E-9         3.8           1         0.341E-9         4.1           2         91.04E-9         4.1           2         91.04E-9         4.1           2         91.04E-9         4.1           2         91.04E-9         5.6           100.0E-9         5.6           101.0E-5         5.6           101.0E-6         5.6           101.0E-6         5.6           101.0E-6         5.6           101.0E-6         5.6           11.00E-6         5.6           11.10BE-6         1.6           11.10BE-6         1.6           11.10BE-6         1.6           11.10BE-6         1.6           11.10BE-6         1.6           11.10BE-6         1.6           11.20E-6         0.0           12.20E-6         0.0	3.517	
w         no.11E-3         43           18.341E-9         4.1           29.104E-9         4.1           29.104E-9         4.1           100.05-9         5.6           1575-9         5.6           1057E-9         5.6           1158E-9         5.1           1158E-9         5.6           1157F-9         5.6           1157F-9         5.6           1157F-9         5.6           1157F-9         5.6           1168F-9         5.6           1178F-9         5.6           1187F-9         5.6           1108F-6         4.8           1108F-6         4.8           1108F-6         1.8           1149F-6         2.8           1149F-6         1.6           1174F-6         1.6           1174F-6         1.6           1174F-6         1.6           1198F-6         1.8           1198F-6         1.8           1198F-6         1.8           1198F-6         1.2           1200F-6         0.0           1200F-6         0.0           1200F-6         0.0	3.694	
2         91.045-3         91.04           31.00.0E-3         5.6           31.00.0E-3         5.6           10.91E-3         5.6           10.91E-3         5.6           10.91E-3         5.6           10.91E-3         5.6           10.91E-3         5.6           11.95E-3         5.6           12.91E-3         5.6           13.167E-3         5.6           13.167E-3         5.6           13.167E-3         5.6           13.167E-3         5.6           13.167E-3         5.6           13.108E-6         5.6           11.108E-6         5.6           11.108E-6         1.6           11.201E-6         0.6 <t< td=""><th>171</th><td></td></t<>	171	
3         100.0E-9         5.           4         102.0E-9         5.           4         102.0E-9         5.           5         105.7E-9         5.           5         105.7E-9         5.           5         105.7E-9         5.           10         115.8E-9         5.           11         15.8E-9         5.           12         13.7E-9         5.           21         13.7E-9         5.           21         13.7E-9         5.           21         17.7E-9         5.           21         17.7E-9         5.           21         17.7E-9         5.           21         17.7E-7         5.           21         17.7E-7         5.           21         17.7E-7         5.           21         1.10E-6         4.           21         1.10E-6         1.           21         1.149E-6         1.           21         1.149E-6         1.           21         1.10E-6         1.           21         1.10E-6         1.           21         1.10E-6         1.           21 </td <th>1.552</th> <td></td>	1.552	
41         102.0E-9         5.6           51         105.7E-9         5.6           51         105.7E-9         5.6           51         105.7E-9         5.6           115.0E-9         5.6         109.1E-9         5.6           115.0E-9         5.6         109.1E-9         5.6           115.0E-9         5.6         109.1E-9         5.6           110.0E-6         5.6         109.210.5E-9         5.6           110.0E-6         5.6         109.108E-8         5.6           110.0E-6         4.5         10.108E-6         4.5           11.10E-6         1.6         1.108E-6         1.8           11.10E-6         1.8         1.108E-6         1.8           11.10E-6         1.8         1.108E-6         1.8           11.10E-6         1.6         1.2         1.2         1.2           11.10E-6         1.6         1.2         1.2         1.2         1.2           11.10E-6         1.8         1.108E-6         1.8         1.108E-6         1.2         1.2         1.2         1.2         1.2         1.2         1.2         1.2         1.2         1.2         1.2         1.2         1.2<	5.000	
$\begin{array}{c} {\bf 5}_{\bf 1} 105.7E-9 & {\bf 5}_{\bf 1} \\ {\bf 109} 1E-9 & {\bf 5}_{\bf 1} \\ {\bf 109} 1E-9 & {\bf 5}_{\bf 1} \\ {\bf 119} 156.4E-9 & {\bf 5}_{\bf 1} \\ {\bf 31} 167.E-9 & {\bf 5}_{\bf 1} \\ {\bf 31} 167.E-9 & {\bf 5}_{\bf 1} \\ {\bf 31} 107.E-9 & {\bf 5}_{\bf 1} \\ {\bf 31} 100E-6 & {\bf 5}_{\bf 1} \\ {\bf 31} 100E-6 & {\bf 5}_{\bf 1} \\ {\bf 31} 100E-6 & {\bf 5}_{\bf 1} \\ {\bf 31} 110E-6 & {\bf 3}_{\bf 2} \\ {\bf 31} 1149E-6 & {\bf 2}_{\bf 2} \\ {\bf 31} 1149E-6 & {\bf 1}_{\bf 3} \\ {\bf 31} 1167E-6 & {\bf 1}_{\bf 3} \\ {\bf 31} 1169E-6 & {\bf 1}_{\bf 3} \\ {\bf 31} 1189E-6 & {\bf 37} \\ {\bf 31} 139E-6 & {\bf 37} \\ {\bf 31} 139E-6 & {\bf 37} \\ {\bf 31} 139E-6 & {\bf 0}_{\bf 0} \\ {\bf 31} 20E-6 & {\bf 0}_{\bf 0} \\ {\bf 31} 39BE-6 & {\bf 0}_{\bf 0} \\ {\bf 31} 20BE-6 & {\bf 0}_{\bf 0} \\ {\bf 31} 20BE-6 & {\bf 0}_{\bf 0} \\ {\bf 0}_{\bf 15} 3BE-6 & {\bf 0}_{\bf 0} \\ {\bf 0}_{\bf 15} 3BE-6 & {\bf 0}_{\bf 0} \\ {\bf 0}_{\bf 15} 20E-6 & {\bf 0}_{\bf 0} \\ {\bf 0}_{\bf 15} 20E-6 & {\bf 0}_{\bf 0} \\ {\bf 0}_{\bf 15} 20E-6 & {\bf 0}_{\bf 0} \\ {\bf 0}_{\bf 15} 20E-6 & {\bf 0}_{\bf 0} \\ {\bf 0}_{\bf 15} 20E-6 & {\bf 0}_{\bf 0} \\ {\bf 0}_{\bf 15} 20E-6 & {\bf 0}_{\bf 0} \\ {\bf 0}_{\bf 15} 20E-6 & {\bf 0}_{\bf 0} \\ {\bf 0}_{\bf 15} 20E-6 & {\bf 0}_{\bf 0} \\ {\bf 0}_{\bf 15} 20E-6 & {\bf 0}_{\bf 0} \\ {\bf 0}_{\bf 15} 20E-6 & {\bf 0}_{\bf 0} \\ {\bf 0}_{\bf 2} 200E-6 & {\bf 0}_{\bf 0} \\ {\bf 0}_{\bf 2} 200E-6 & {\bf 0}_{\bf 0} \\ {\bf 0}_{\bf 2} 200E-6 & {\bf 0}_{\bf 0} \\ {\bf 0}_{\bf 2} 200E-6 & {\bf 0}_{\bf 0} \\ {\bf 0}_{\bf 1} 20E-6 & {\bf 0}_{\bf 0} \\ {\bf 0}_{\bf 1} 20E-6 & {\bf 0$	5.000	
$\begin{array}{c} \hline 0 & 0 & 0 & 0 & 0 \\ \hline 0 & 10 & 0 & 0 & 0 \\ \hline 1 & 115 & 0 & -5 & 5 & 0 \\ \hline 1 & 115 & 0 & -5 & 5 & 0 \\ \hline 1 & 10 & 0 & 5 & 0 & 0 \\ \hline 1 & 10 & 0 & 5 & 0 & 0 \\ \hline 1 & 10 & 0 & 5 & 0 & 0 \\ \hline 1 & 10 & 0 & 5 & 0 & 0 \\ \hline 1 & 10 & 0 & -5 & 0 & 0 \\ \hline 1 & 10 & 0 & -6 & 0 & 0 \\ \hline 1 & 10 & 0 & -6 & 0 & 0 \\ \hline 1 & 10 & 0 & -6 & 0 & 0 \\ \hline 1 & 10 & 0 & -6 & 0 & 0 \\ \hline 1 & 10 & 0 & -6 & 0 & 0 \\ \hline 1 & 10 & 0 & -6 & 0 & 0 \\ \hline 1 & 10 & 0 & -6 & 0 & 0 \\ \hline 1 & 10 & 0 & -6 & 0 & 0 \\ \hline 1 & 11 & 0 & 0 & -6 & 0 & 0 \\ \hline 1 & 11 & 0 & 0 & -6 & 0 & 0 \\ \hline 1 & 11 & 0 & 0 & -6 & 0 & 0 \\ \hline 1 & 11 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 11 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 11 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 11 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 11 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 11 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 12 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \hline 1 &$	5.000	
1294E-3         5           1564E-3         5           1564E-3         5           1564E-3         5           1675         5           1787E-3         5           1710E-5         5           1712E-6         3           1714E-6         2           1748E-6         1.5           17147E-6         1.6           17182E-6         1.6           17182E-6         1.6           17182E-6         1.7           17192E-6         1.7           17192E-6         1.6           17192E-6         1.6           17192E-6         1.0           17192E-6         1.0           1702E-6         1.0           1100E-6         0.0           1200E-6         0.0           1200E-6         0.0           1200E-6         0.0           1200E-6         0.0	5.000	
19         156.4E-9         5.           12         210.5E-9         5.           13         7E-9         5.           13         7E-9         5.           13         7E-9         5.           16         7E-9         5.           17         7E-9         5.           1100E-6         5.         5.           1100E-6         5.         5.           1110E-6         2.         5.           1141E-6         2.         5.           11414E-6         1.         5.           11414E-6         1.         5.           1174E-6         1.         5.           1190E-6         1.         2.           1202E-6         0.         6.           1202E-6         0.         6.           1202E-6         0.         6.           1202E-6         0.         6.           1302E-6	5.000	
10         210/5E-9         5.6           1310         7E-9         5.6           2         518/7E-9         5.6           2         518/7E-9         5.6           2         518/7E-9         5.6           3         716/7E-9         5.6           5         1100E-6         5.8           6         11410E-6         4.8           7         1120E-6         3.8           11414E-6         2.5         1100E-6           11169E-6         1.8         1.1169E-6           2         1174E-6         1.3           3         1.70E-6         1.7           11108E-6         1.8         1.1169E-6           11108E-6         1.9         1.1169E-6           11108E-6         1.7         1.139E-6           11190E-6         1.2         1.139E-6           11201E-6         0.0         1.201E-6         0.0           1201E-6         0.0         1.201E-6         0.0           1201E-6         0.0         1.201E-6         0.0           1201E-6         0.0         1.201E-6         0.0           1201E-6         0.0         1.201E-6         0.0 <th>5.000</th> <td></td>	5.000	
13         13         17.F-9         5.6           25         71.7F-9         5.6         13         71.87F-9         5.6           13         71.77F-9         5.6         5.7         5.7         5.7           13         71.77F-9         5.6         5.7         5.7         5.7         5.7           13         71.77F-9         5.6         5.0         5.7         5.7         5.7           11         11.10F-6         5.0         5.7	5.000	
2         310/2-3         31           37         716/7-9         5.6           4         916/7-9         5.6           1         100E-6         4.5           1         110E-6         5.6           1         100E-6         4.5           1         1120E-6         3.3           1         1141E-6         2.5           1         149E-6         1.5           1         1163E-6         1.6           1         1169E-6         1.6           1         1169E-6         1.6           1         1174E-6         1.6           1         1174E-6         1.6           1         1174E-6         1.6           1         1196E-6         16           1         1196E-6         10           1         1196E-6         10           1         120E-6         0.0           1         120E-6         0.0           1         120E-6         0.0           1         139E-6         0.0           1         139E-6         0.0           1         139E-6         0.0           1         1	5.000	
918.7E-9         5 0.           918.7E-9         5 0.           5 1.100E-6         5.0.           1.100E-6         4.5.           1.100E-6         3.3.           1.141E-6         2.5.           0.163E-6         1.6.           1.169E-6         1.5.           1.174E-6         1.6.           1.174E-6         1.6.           1.174E-6         1.6.           1.174E-6         1.7.           1.194E-6         1.7.           1.194E-6         1.7.           1.194E-6         0.0.           1.194E-6         0.0.           1.204E-6         0.0.           1.338E-6 <th>5.000</th> <td></td>	5.000	
S1 1100E-6         5           S1 1100E-6         4           S1 110E-6         3.5           S1 141E-6         2.5           S1 141E-6         2.5           S1 141E-6         2.5           S1 141E-6         2.5           S1 168E-6         1.6           S1 174E-6         1.3           S1 174E-6         1.3           S1 174E-6         1.3           S1 174E-6         1.3           S1 174E-6         1.6           S1 174E-6         1.7           S1 1130E-6         16           S1 1130E-6         17           S1 130E-6         10           S1 130E-6         10           S1 120E-6         0.0           S1 130BE-6	5.000	
108-16         4.5           1120E-6         4.5           1141E-6         2.5           1149E-6         2.5           1149E-6         1.6           1149E-6         1.6           1149E-6         1.6           1149E-6         1.6           1149E-6         1.6           1149E-6         1.6           1174E-6         1.6           1174E-6         1.6           1174E-6         1.6           1174E-6         1.6           1184E-6         1.6           1190E-6         1.7           1193E-6         1.6           1120E-6         0.0           1120E-6         0.0           1120E-6         0.0           1120E-6         0.0           1120E-6         0.0           1120E-6         0.0           120E-6         0.0           120E-6         0.0           120E-6         0.0           1226E-6         0.0           1238E-6         0.0           1338E-6         0.0           1733E-6         0.0           1200E-76         0.3           2007E-76 <th>5.000</th> <td></td>	5.000	
1/12UE-16         2.3           1.141E-6         2.5           1.143E-6         2.5           1.143E-6         1.6           1.163E-6         1.6           1.163E-6         1.6           1.174E-6         1.6           1.174E-6         1.6           1.174E-6         1.6           1.174E-6         1.6           1.174E-6         1.7           1.174E-6         1.7           1.174E-6         1.7           1.174E-6         1.7           1.196E-6         1.8           1.196E-6         1.6           1.196E-6         0.0           1.202E-6         0.0           1.203E-6         0.0           1.203E-6         0.0           1.393E-6         0.0           1.1733E-6         0.0           1.1733E-6         0.0           1.203E-76         0.0           2.1037E-76         0.0	1.579	
1.149E-6         2.5           1.168E-6         1.6           1.168E-6         1.6           1.168E-6         1.6           1.178E-6         1.6           1.178E-6         1.6           1.178E-6         1.6           1.178E-6         1.6           1.178E-6         1.7           1.178E-6         1.7           1.178E-6         1.7           1.190E-6         49           1.190E-6         0.0           1.190E-6         0.0           1.200E-6         0.0           1.308E-6         0.0           1.793E-6         0.0           1.793E-6         0.0           1.209E-6         0.0	936	
0         11.63E-6         1.6           1         1.169E-6         1.5           2         1.774E-6         1.3           3         1.778E-6         1.6           3         1.778E-6         1.6           3         1.778E-6         1.6           3         1.778E-6         1.7           4         1.184E-6         81           5         1.167E-6         67           7         1.193E-6         37           8         1.196E-6         16           9         1.196E-6         0.6           1         1.201E-6         0.6           1         2.002E-6         0.6           3         1.205E-6         0.6           3         1.235E-6         0.6           1.339E-6         0.6           1.339E-6         0.6           1.733E-6         0.6           2.007E-6         0.3           2.007E-6         0.3	2.569	
11.169E-6         15.8           21.174E-6         13.3           31.176E-6         1.0           41.104E-6         16.6           51.187E-6         17.6           17.193E-6         17.6           17.193E-6         17.7           11.196E-6         16.7           11.196E-6         16.7           11.196E-6         16.7           11.196E-6         10.0           11.201E-6         0.0           11.202E-6         0.0           12.1203E-6         0.0           12.1204E-6         0.0           13.1204E-6         0.0           13.1304E-6         0.0           13.1394E-6         0.0           14.7934E-6         0.0           13.200E-6         0.0           13.200E-76         0.0           2.0007E-76         33	.835	
2         1.744-6         1.3           3         1.746-6         1.6           4         1.184E-6         61           5         1.877-6         6.7           1.139E-6         49         7           1.139E-6         18         1.139E-6           1.139E-6         18         1.139E-6           1.139E-6         12         1.201E-6         0.6           1.201E-6         0.6         1.202E-6         0.6           1.202E-6         0.6         1.302E-6         0.6           1.302E-6         0.6         1.302E-6         0.6           1.338E-6         0.6         1.733E-6         0.6           1.733E-6         0.6         1.203E-6         0.6           1.733E-6         0.6         1.203E-6         0.6           1.733E-6         0.7         2.207E-6         0.7           1.733E-7         0.7         1.207E-6	.557	
1.1706         1.1           1.184E-6         61           1.187E-6         67           1.190E-6         67           1.193E-6         37           1.195E-6         77           1.195E-6         37           1.195E-6         92           1.201E-6         0.2           1.201E-6         0.0           1.251E-6         0.0           1.398E-6         0.0           1.793E-6         0.0           1.201E-6         0.0           1.201E-6         0.0           1.398E-6         0.0           2.007E-6         0.3           2.007E-6         33	.322	
1.187E-6         67           1.190E-6         67           1.193E-6         67           1.193E-6         18           1.193E-6         18           1.195E-6         18           1.195E-6         10           1.101E-6         0.0           1.205E-6         0.0           1.236E-6         0.0           1.338E-6         0.0           1.733E-6         0.0           1.1733E-6         0.0           2.1897E-6         0.0           2.000E-76         0.3           2.000E-76         33	310.7E=3	
B         1190E-6         43           7         1.193E-6         37           1.196E-6         18           1.196E-6         18           1.196E-6         12           1.201E-6         0.0           1.300E-6         0.0           1.300E-6         0.0           1.300E-6         0.0           1.330E-6         0.0           1.733E-6         0.0           1.739E-6         0.0           1.739E-6         0.0           2.000E-6         0.0           2.000E-6         0.3	573.7E-3	
7         1138E-6         37           1138E-6         32           1138E-6         18           1120E-6         0.2           120DE-6         0.0           130DE-6         0.0           130DE-6         0.0           130DE-6         0.0           173DE-6         0.0           173DE-6         0.0           120DE-6         0.0           120DE-6         0.0           120DE-6         0.0           120DE-6         0.0           20DE-6         0.0           20DE-6         33	198.9E-3	
198-198E-6         18           198E-6         92           1200E-6         92           1200E-6         0.0           1201E-6         0.0           1201E-6         0.0           1201E-6         0.0           1201E-6         0.0           1201E-6         0.0           1201E-6         0.0           12126E-6         0.0           1226E-6         0.0           1226E-6         0.0           1238E-6         0.0           1338E-6         0.0           1733E-6         0.0           1738E-6         0.0           1738E-6         0.0           21897E-6         0.0           21907E-6         0.3           2000F-8         333	371.5E-3	
1.100E-0         322           1.200E-6         0.0           1.201E-6         0.0           1.201E-6         0.0           1.205E-6         0.0           1.205E-6         0.0           1.215E-6         0.0           1.215E-6         0.0           1.215E-6         0.0           1.215E-6         0.0           1.300E-6         0.0           1.330E-6         0.0           1.339E-6         0.0           1.733E-6         0.0           2.1897E-6         0.0           3.200E-6         0.0           3.200E-6         0.0	85.8E-3	
1.201E-6         0.0           12.203E-6         0.0           12.205E-6         0.0           13.300E-6         0.0           1.330E-6         0.0           1.330E-6         0.0           1.330E-6         0.0           2.1397E-6         0.0           2.000E-6         0.0           2.000E-6         3.3	1.0	
21 203E-6         0.0           31 205E-6         0.0           41 2205E-6         0.0           51 224E-6         0.0           51 224E-6         0.0           1251E-6         0.0           1251E-6         0.0           13 1251E-6         0.0           13 1351E-6         0.0           11 1793E-6         0.0           12 1793E-6         0.0           12 1793E-6         0.0           12 1793E-6         0.0           21 200E-6         0.0           21 200E-6         0.0           200DE-6         33		
31         2.05E-6         0.0           41         1.206E-6         0.0           51         1.214E-6         0.0           16         1.226E-6         0.0           13.121E-6         0.0         0.0           13.30E-6         0.0         0.0           13.30E-6         0.0         0.1           11.733E-6         0.0         0.2           12.89F-6         0.0         0.3           2.000E-6         0.0         3           3.200E-6         0.0         0.3	).0	
1.208E-6         0.0           1.214E-6         0.0           1.226E-6         0.0           1.251E-6         0.0           1.306E-6         0.0           1.396E-6         0.0           1.398E-6         0.0           1.733E-6         0.0           2.897E-6         0.0           3.200E-6         0.0           4.200E-6         0.0           4.200E-6         0.0           4.200E-6         0.0           4.200E-6         0.0	0.0	
1.2142-0         0.0           1.22142-0         0.0           1.251E-6         0.0           1.300E-6         0.0           1.398E-6         0.0           1.732E-6         0.0           1.732E-6         0.0           1.732E-6         0.0           2.1837E-6         0.0           2.000E-6         0.0           4.200E-6         0.0	J.U	
1.251 E 6         0.0           1.251 E 6         0.0           1.306E 6         0.0           1.398E 6         0.0           1.793E 6         0.0           1.897E 6         0.0           2.1897E 6         0.0           2.000E 6         0.0           3.2007E 6         0.3	10	
1.300E-6         0.0           1.398E-6         0.0           1.593E-6         0.0           1.793E-6         0.0           1.793E-6         0.0           2.897E-6         0.0           2.000E-6         0.0           4.2007E-6         33	).0	
1.396E-6         0.0           1.593E-6         0.0           1.593E-6         0.0           1.793E-6         0.0           1.2         1.897E-6         0.0           1.3         2.000E-6         0.0           1.4         2.007E-6         33	).0	
1.593E-6         0.0           1.793E-6         0.0           1.793E-6         0.0           1.2         1.897E-6         0.0           1.3         2.000E-6         0.0           1.4         2.007E-6         33	0.0	
1.7332-0 0.0 2 1.897E-6 0.0 3 2.000E-6 0.0 4 2.007E-6 33	J.U	
3 2.000E-6 0.0 4 2.007E-6 33	1.0	
4 2.007E-6 33	0.0	
	331.8E-3	
5 2.017E-6 84	341.3E-3	
aa ∠ 1126 E_6 1 3	3/3	

# **Integrated Circuit Design CAD Tool Information**

**cc.** Click on the output waveform in the "Virtuoso Visualization & Analysis XL" window to display the waveform as a dashed, bold line as shown in the image below.



#### **Integrated Circuit Design CAD Tool Information**

**dd.** Right click on the bold dashed line (the input waveform) and select "Table  $\rightarrow$  New Window." Notice when you move the cursor over the dashed line, the (x, y) coordinates of the waveform are displayed. The table below shows all coordinates.

N	Virtuoso (R)	visualization & Analysis XL Table	_ 🗆 🗙
<u>F</u> ile <u>V</u> iew <u>T</u> ools	<u>H</u> elp		cādence
time (c)			
1 0.0	3.000		Â
2 2.029E-9	3,000		
3 3.603E-9	3,000		
4 6.470E-9	3.000		
5 12.21E-9	3.001		
6 23.68E-9	2.973		
7 26.24E-9	2.955		
8 27.51E-9	2.941		
9 30.07E-9	2.902		
10 35.19E-9	2.758		
11 39.90E-9	2.497		
12 44.28E-9	2.127		
13 50.46E-9	1.440		
14 55.93E-9	760.6E-3		
15 60.25E-9	343.6E-3		
<u>16</u> 63.34E-9	173.6E-3		
<u>17</u> 66.56E-9	79.58E-3		
18 70.33E-9	29.70E-3		
<u>19</u> 73.88E-9	11.51E-3		
20 78.11E-9	3.611E-3		
21 83.41E-9	945.2E-6		
22 91.04E-9	372.9E-6		
23 100.0E-9	383.8E-6		
24 TUZ.UE-9	239.2E-b		
25 105.7E-9	70.40E-6		
26 103.1E-3	20.20E-0		
20 129 / E 9	-77.41E-3		
20 123.4E-3	-8 580E-9		
30_210.5E-9	24.48E-9		
31 318 7E-9	-2 787E-9		
32 518 7E-9	21.96E-9		
33 718.7E-9	-1.180E-9		
34 918.7E-9	20.45E-9		
35 1.100E-6	293.4E-12		
36 1.108E-6	-276.1E-6		
91 Click a property	to edit.		

# **Integrated Circuit Design CAD Tool Information**

- **ee.** From the information contained in the (x, y) tables obtained from the input waveform and the output waveform, values for the following quantities can be obtained:
  - i. For the falling transition of the input waveform
    - 1. Fall time (The time for the value of the waveform to fall from 90% to 10% of its maximum value, usually VDD, to GND).
    - 2. Delay (The time between when the value of the input waveform is halfway between its minimum and maximum values and when the value of the output waveform is halfway between its minimum and maximum values).
  - ii. For the rising transition of the input waveform
    - 1. Rise time (The time for the value of the waveform to rise from 10% to 90% of its maximum value, usually VDD, from GND).
    - 2. Delay
- **ff.** The value of the width of the inverter pfet can be changed so that it is double the width of the inverter nfet (a new value of the beta ratio). New values for the following quantities can be obtained and compared with the values in (ee).

**gg.**The value of the width of the inverter pfet can be changed so that it is triple the width of the inverter nfet (another new value of the beta ratio). New values for the following quantities can be obtained and compared with the values in (ee) and (ff).

# **Integrated Circuit Design CAD Tool Information**

- **hh.** The value of the output load (cap) can be changed to C = 10pF and to C = 100pF. For each case, calculate the Rise time, Fall time and delay for the rising transition and falling transition. Compare with results in (ee).
- **ii.** The value of the voltage driving the input net can be adjusted to 3V (to match the output net). Simulations can then be performed for the case in which the inverter pfet:
  - i. Takes on the initial value of the width.
    - 1. values for the following quantities can be obtained:
      - a. For the falling transition of the input waveform
        - i. Fall time
        - ii. Delay
      - b. For the rising transition of the input waveform
        - i. Rise time
        - ii. Delay
  - ii. Has twice the width of the inverter pfet
    - 1. values for the following quantities can be obtained:
      - a. For the falling transition of the input waveform
        - i. Fall time
        - ii. Delay
      - b. For the rising transition of the input waveform
        - i. Rise time
        - ii. Delay
  - iii. Has three times the width of the inverter pfet
    - 1. values for the following quantities can be obtained:
      - a. For the falling transition of the input waveform
        - i. Fall time
        - ii. Delay
      - b. For the rising transition of the input waveform
        - i. Rise time
        - ii. Delay
- **jj.** Now you have simulated your inverter.

# **Integrated Circuit Design CAD Tool Information**

# **15.** Inverter: Creating a Layout

**a.** In the Library Manager, highlight your library "EENG653" and the Cell "inverter." Then, click on "File  $\rightarrow$  New  $\rightarrow$  Cell View"

Library	Manager: Directoryro/cadence/ncsu-cdk-1.6.0.beta	
<u>File E</u> dit <u>V</u> iew <u>D</u> esign Manager <u>H</u> elp		cādence
Show Categories Show Files Library	Cell	View
EENG653	inverter	schematic
EENG653 NCSU_Analog_Parts NCSU_TechLib_ami06 NCSU_TechLib_ami16 NCSU_TechLib_p106 NCSU_TechLib_tsmc02 NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03d NCSU_TechLib_tsmc04_4M2P basic cdsDefTechLib megan	Inv_test Inverter	View         Lock         Size           schematic         29k           symbol         23k
Messages but was defined in libFile '/home/afiten3/fac/m Warning: The directory: '/home/afiten3/fac/m Warning: LIB EENG653 from File /home/afiten3/fac/m UB EENG653 from the same file (defined earlier.) Warning: The directory: '/home/afiten3/fac/mlanzero/cadence but was defined in libFile '/home/afiten3/fac/m Warning: The directory: '/home/afiten3/fac/mlanzero/cadence but was defined in libFile '/home/afiten3/fac/m	lanzero/cadence/ncsu-cdk-1.6.0.beta/cds.lib' for Lib 'EENG695'. //ncsu-cdk-1.6.0.beta/dave' does not exist lanzero/cadence/ncsu-cdk-1.6.0.beta/cds.lib' for Lib 'dave'. /cadence/ncsu-cdk-1.6.0.beta/cds.lib for lib 'dave'. //ncsu-cdk-1.6.0.beta/EENG695/EENG695' does not exist lanzero/cadence/ncsu-cdk-1.6.0.beta/cds.lib' for Lib 'EENG695'. //ncsu-cdk-1.6.0.beta/dave' does not exist lanzero/cadence/ncsu-cdk-1.6.0.beta/cds.lib' for Lib 'dave'.	

# **Integrated Circuit Design CAD Tool Information**

**b.** The window that appears is shown below. Fill in the field "View" with the word 'layout' and select "Type" as 'layout'. Then click 'OK'.

	New File
- File	
Library	EENG653
Cell	inverter
View	layout
Туре	layout 🔽
Application	
Open with	Layout L
🔲 Always use thi	s application for this type of file
Library path file	
mzero/cadence/	ncsu-cdk-1.6.0.beta/cds.lib
	OK Cancel Help

# **Integrated Circuit Design CAD Tool Information**

**c.** An empty layout window will appear in edit mode: "Virtuoso Layout Suite"

Virtuoso® Layout Suite L Editing: EENG653 inverter layout	_ 🗆 🗙
Launch Eile Edit <u>V</u> iew <u>C</u> reate Verlify Co <u>n</u> nectivity <u>O</u> ptions <u>T</u> ools <u>W</u> indow Ass <u>u</u> ra QRC Opti <u>m</u> ize NCSU <u>H</u> elp	cādence
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letat drawing VVIII	
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Rectangle 🥑 🗹 🔤	•
Objects Guides	· · · · · · · ·
Immouse L: showClickInfo() M: sevDirectPlot('sevSession1 'asiiPlotTranSignalCB) R: Lk+	liMousePopUp()
4(3) > Select nodes or terminals, press <esc> to finish selection</esc>	Cmd:

#### **Integrated Circuit Design CAD Tool Information**

**d.** Click on the layout window and create an instance of the nmos4 device by typing 'i' in the layout window. Click on the Browse button, and choose "NCSU\_TechLib\_ami06→nmos→layout" as shown in the Create Instance image below.

	Create Instance
Library	NCSU_TechLib_ami06 Browse
Cell	nnos
View	layout
Names	<b>I</b> 1
Mosaic	Rows 1 Columns 1
	Delta Y 2.7 Delta X 4.8
Halo	✓ Define Halo
Physical	Only 🗌
<u>الح</u>	Rotate 🖉 🕼 Sideways 🗧 Upside Down
Model na	me amiO6N
Model Ty	pe 💿 system 🔾 user 🔽
	Hide Cancel Defaults Help

# **Integrated Circuit Design CAD Tool Information**

**e.** Instantiate this layout for the nmos device in your layout.

Show Categories		
Library	Cell	View
NCSU_TechLib_ami06	nmos	layout
EENG653 NCSU_Analog_Parts NCSU_Digital_Parts NCSU_TechLib_ami06 NCSU_TechLib_ami16 NCSU_TechLib_tsmc02 NCSU_TechLib_tsmc02d NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03d NCSU_TechLib_tsmc04_4M2P avTech basic cdsDefTechLib megan	m1_elec m1_n m1_p m1_poly m2_m1 m3_m2 metal1 metal2 metal3 nactive nmos ntap nwell pactive pmos poly ptap	View A Lock Si layout
Close Fi	Iters Disp	lay) (Help)

# **Integrated Circuit Design CAD Tool Information**

**f.** Click on the layout window again. Type 'I' in the layout window and fill in the "Create Instance" window.

	Create Instance	X
Library	NCSU_TechLib_ami06 Browse	A
Cell	pmos	
View	layout	=
Names	12	=
Mosaic	Rows 1 Columns 1	
	Delta Y 4.8 Delta X 7.6	
Halo	Define Halo	
Physical	Only 🗌	
<u>الع</u>	Rotate 🖉 🕼 Sideways 🖉 Upside Down	
Model na	me ami06P	
Model Ty	pe 💿 system 🔾 user	7
	Hide Cancel Defaults Help	D

# **Integrated Circuit Design CAD Tool Information**

Library	y Browser - Create Instar	nce – 🗆 🗙
Library Show Categories Library NCSU_TechLib_ami06 EENG653 NCSU_Analog_Parts NCSU_Digital_Parts NCSU_TechLib_ami16 NCSU_TechLib_ami16 NCSU_TechLib_tsmc02 NCSU_TechLib_tsmc02 NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc04_4M2P avTech basic cdsDefTechLib megan	Prowser - Create Instar         Cell         pmosl         m1_elec         m1_p         m1_poly         m2_m1         m3_m2         metal1         metal2         metal3         nactive         nmos         ntap         nwell         pactive         pmos         poly	View layout View ^ Lock Si layout
Close	ilters Dis	play

**g.** Instantiate the layout of the pmos device in your layout.

#### **Integrated Circuit Design CAD Tool Information**

**h.** After instantiating one instance of the nmos layout and one instance of the pmos layout, your layout window "Virtuoso Layout Suite L Editing" will look like the image below.



# **Integrated Circuit Design CAD Tool Information**

**i.** Type 'shift-f' in the layout window, and the layers for the nmos device and pmos device will be visible as shown in this image.



# **Integrated Circuit Design CAD Tool Information**

**j.** To change the properties of the pmos device, highlight the device in your layout, and then type 'q'. The "Edit Instance Properties" window will appear.

	Edit I	nstance Properties	
ОКС;	ancel Apply is a	C Previous	Help
◆ Attribute →	🔆 Connectivity 🔶 Para	ameter 🕹 Property 👶 ROD 🕹 DEM	🔲 Coninon
Library	NCSU_TechLib_ami06	y	
Cell	pmoš		
View	layouti		
Origin: X	3.6	Y 2.55	
Name	IŽ	Rotation R0 -	
СөйТурө	none	Placement Status none 💷	
Cluster	None -	Halo	
Physical Crit	¥ 🗌		

# **Integrated Circuit Design CAD Tool Information**

**k.** In the "Edit Instance Properties" window, click the 'Parameter' radio button. The following window will appear.

	Edit Instance Properties	_ 🗆 🗙
OK Cancel Apply	Next Province	Help
Attribute	🔶 Parameter 🕹 Property 🕹 ROD 🕹 DFM	🗌 Convision
Model name	ami06Pį́	
Model Type	🔶 system 🕹 user	
Multiplier	1.	
Fingers	1 <u>.</u>	
Width (grid units)	10 <u>ĭ</u>	
Width	1.5ų	
Widih (naranaani)	1.5ų	
Length (grid units)	₫	
Length	600r <u>ě</u>	
Length (inlinium)	600r <u>i</u>	
Drain diffusion area	2.25e-12	
Source diffusion area	2.25e-12	
Drain diffusion perimeter	6યું	
Source diffusion perimeter	6યું	
Drain diffusion res squares	Y Y Y	
Source diffusion res squares	Y	
Virtuoso-XL layout cell	Y	
Drain diffusion length	Y	
Source diffusion length	Y ***	
Temp rise from ambient	Y *** **	
Estimated operating region	sat 💷	

# **Integrated Circuit Design CAD Tool Information**

**I.** The LSW (Layout Selection Window) can be separated from the Virtuoso Layout Suite window which then looks like the image below.

<b>1</b>					Vir	tuoso ®	Layout	Suite L E	diting: EEI	NG653 inve	rter layou	t					JX
Launch <u>File</u> Edit <u>V</u> iew <u>C</u>	<u>C</u> reate Ver	ify Co <u>n</u>	nectivity	<u>O</u> ptions	Tools	<u>W</u> indow	Ass <u>u</u> ra Q	RC Opti <u>m</u> i	ze NCSU .	Help						cāden	ce
🕞 🕞 🛛 🥱 🦿 🗍	• 🗘 🔟	× 1	<b>A</b> (1)	8	⊌ »	Q »	ab	<b>w</b> Wo	rkspace: Cla	ssic	- 5	-					
R - 2 - 2 - 2			»    (I	F)Select:0	) Sel(N)	:0 Sel(I):1	) D Sel(O):0	X:-6.750	0 Y:10.2000	dX:-11.400(	) dY:15.9000	Dist:19.5645	6 Cmd:Move				_
Objects ? 🖻 🗙								1									1
Object V S																	
🖨 Shapes 🛛 🗹 🗹	1.1																
- Donut V																	
– Label 🛛 🗹 🗹								•									
-Path 🗹 🗹																	.
-Polygon V																	
– Rectangle 🛛 🗹	1.1																
- Other Shapes 💆 💆																	
Fluid Guardring	•																
Mosaic 🗹 🗹																	.
Vias V																	
Fluid Shapes																	
- Fig Groups 🛛 📃 🗹																	
- P&R Boundaries																	
— Area Bound 👿 📋																	.
- Snap Bound 🗹 📃																	
El Soft Blocks	-																
∏ ⊢Pin 🗍																	
- P&R Bound								•									
🖻 Blockages 🛛 🖌 🖌																	.
- Halo Blocka 👿 💆																	
- Placement B ⊻ ⊻								· _									
- Fill Blockage																	
— Slot Blockage 📃 📃																	
🕀 Pin Blockage 🔽 🗹																	.
🗄 Screen Bloc 🗹 🗹																	
								·	· ·								
Objects Guides																	
=mouse L: Enter Point	au adu								M: Rotate 90						R	: Pop-up M	enu
4(5) Select the lighter to be mit	uveu.															Cuid: Mc	A.R.

# **Integrated Circuit Design CAD Tool Information**

**m.** The floating LSW lists the metal layers and via layers in this design. For example, metal1 is blue. Polysilicon is pink.

L	ayers.		8	9×
P	۱ V	V As	A R	1S
	pwell	drawing	-	-
7	All Va	lid Layer	s 🔽	(41)
	Used L	ayers Or	ily)	
Q	Searc	:h		-
	Laver	Purnose	a I V I	S
	pwell	drawing		V
	nwell	drawing	~	~
	active	drawing	~	~
	nact	drawing	<b>~</b>	~
	pact	drawing	✓	✓
	nsel	drawing	✓	✓
	psel	drawing	✓	✓
	poly	drawing	✓	✓
88	elec	drawing	✓	~
	met	drawing	✓	✓
	met	drawing	~	~
	met	drawing	~	~
	CC	drawing	<u> </u>	<u> </u>
	via	drawing	<u> </u>	<u> </u>
	viaz	drawing	<u>×</u>	<u> </u>
	giass	drawing	<u> </u>	<u> </u>
	nign	drawing	<u> </u>	<u> </u>
	nolno	drowing	<u> </u>	<u> </u>
	nad	drawing	-	÷.
R	text	drawing	-	÷.
	res id	drawing	Ē	÷.
	cap.	drawing	-	5
	dio id	drawing	-	Ū.
	pwell	net	~	2
F	nwell	net	~	~
F	active	net	~	~
	nact	net	~	~
	pact	net	<b>~</b>	✓
	high	net	✓	~
	poly	net	✓	✓
	elec	net	✓	✓
	met	net	✓	✓
	met	net	✓	✓
	met	net	~	✓
	CC	net	~	⊻
	via	net	~	⊻
	VIa2	net	⊻	<u>×</u>
	nign	pin	~	⊻
1				
L				
L				
<u> </u>				

# **Integrated Circuit Design CAD Tool Information**

**n.** Metal1 is highlighted in the LSW in the image below.

L	ayers		0	I X
F	V N	IV AS	Ń	18
	metal1	drawing	-	•
7	' All Va	lid Layers		
	Used L	avers Only	,	
	Seam	- · · ·		
	Louor	Durnoco	14	0
	pwell	drawing	V	<u> </u>
	nwell	drawing	v	2
	active	drawing	~	~
	nact	drawing	~	~
	pact	drawing	<b>v</b>	<b>v</b>
	nsel	drawing	~	~
	psel	drawing	✓	✓
	poly	drawing	✓	✓
**	elec	drawing	-	✓
	met	drawing	V	▼
	met	drawing	✓	~
$\square$	met	drawing	✓	✓
	CC	drawing	~	✓
	via	drawing	~	✓
	via2	drawing	~	~
	glass	drawing	~	~
	high	drawing	~	~
	noarc	drawing	<u> </u>	<u>×</u>
	noipe	drawing	<u> </u>	<u>×</u>
R	pau	drawing	<u> </u>	<u>×</u>
H	roc id	drowing	×	×.
20	can	drawing	×	×.
高	dio id	drowing		
EX	micell	net		
H	nwell	net	Ĵ.	Ĵ.
H	active	net	Ĵ.	Ĵ.
	nact	net	~	~
	pact	net	~	~
	high	net	-	~
	poly	net	~	~
	elec	net	✓	~
	met	net	•	~
	met	net	✓	✓
	met	net	✓	✓
	СС	net	✓	✓
	via	net	~	✓
	via2	net	✓	✓
	high	pin	✓	✓
1				
1				
1				
1				

#### **Integrated Circuit Design CAD Tool Information**

**o.** Now you will make connections on the metal layers between the nmos layout and pmos layout. Draw a polysilicon rectangle to connect the gate of the nmos device with the gate of the pmos device. Draw a metal1 rectangle to connect the drain/source region of one device with the drain/source region of the second device. Notice that the nmos device layout and the pmos device layout already contain the built-in active contacts between metal1 and polysilicon (the black vias).



# **Integrated Circuit Design CAD Tool Information**

**p.** Click on your layout window. Type 'i' and fill in the "Create Instance" window as shown below. Instantiate two instances of an 'ntap' in the layout.

	Create Instance	X			
Library	NCSU_TechLib_ami06 Browse	Â			
Cell	ntap				
View	layout				
Names	15				
Mosaic	Rows 1 Columns 1	-			
Halo	Define Halo	-			
Physical	Only 🔲				
<u>ا اک</u>	Rotate A Sideways Sideways				
Rows of c	ontacts 1	U			
Columns of contacts 1					
	Hide Cancel Defaults Hel	p)			

# **Integrated Circuit Design CAD Tool Information**

**q.** Locate the 'ntap' by clicking Browse and choosing "NCSU\_TechLib\_ami06  $\rightarrow$  ntap  $\rightarrow$  layout."

Library	Cell		~ View		
NCSU TechLib ami06	ntap	Tayo	ut		
EENG653 NCSU_Analog_Parts NCSU_Digital_Parts NCSU_TechLib_ami06 NCSU_TechLib_ami16 NCSU_TechLib_tsmc02 NCSU_TechLib_tsmc02d NCSU_TechLib_tsmc03d NCSU_TechLib_tsmc03d NCSU_TechLib_tsmc04_4M2P avTech basic cdsDefTechLib megan	active elec m1_elec m1_n m1_p m1_poly m2_m1 m3_m2 metal1 metal2 metal3 nactive nmos ntap nwell pactive pmos		View A Lock layout		
### **Integrated Circuit Design CAD Tool Information**

**r.** The ntaps will be positioned as shown in the image below. The bulk terminal for the pmos device is its nwell. The power supply layer should be overlapped with ntap using metal1 so that the bulk of the transistor is connected.



## **Integrated Circuit Design CAD Tool Information**

**s.** Now click on your layout and type 'I'. In the "Create Instance" window, fill in the form with "NCSU\_TechLib\_ami06  $\rightarrow$  ptap  $\rightarrow$  layout" as shown in the form below.

	Create Instance	×
Library	NCSU_TechLib_ami06 Browse	Â
Cell	ptap	
View	layout	
Names	I6	
Mosaic	Rows 1 Columns 1	-
	Delta Y 2.4 Delta X 2.4	≣
Halo	Define Halo	
Physical Only		
Rotate A Sideways		
Rows of contacts 1		
Columns of contacts		
	Hide Cancel Defaults Hel	p

# **Integrated Circuit Design CAD Tool Information**

**t.** The "Create Instance" form will appear as shown in the figure below.

🗖 Librar	y Browser - Create Instan	ce 💷 🗙
Show Categories		
Library	Cell	View
NCSU_TechLib_ami06	ptap	layout
NCSU_Analog_Parts NCSU_Digital_Parts NCSU_TechLib_ami06 NCSU_TechLib_ami16 NCSU_TechLib_hp06	m1_enec m1_n m1_p m1_poly m2_m1 m3_m2	layout
NCSU_TechLib_tsmc02 NCSU_TechLib_tsmc02d NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03d NCSU_TechLib_tsmc04_4M2P	metal1 metal2 metal3 nactive nmos	
avTech basic cdsDefTechLib megan	ntap nwell pactive pmos poly	
Close	ilters	lay Help

### **Integrated Circuit Design CAD Tool Information**

**u.** Instantiate two instances of 'ptap' as shown in the figure below. The 'ptap' serves as a bulk connection for the nmos device. The power supply layer should be overlapped with ptap using metal 1 so that the bulk of the transistor is connected.



## **Integrated Circuit Design CAD Tool Information**

**v.** Draw metal1 power rails as shown in the figure below. Click on your layout, select metal1 from the LSW, and select "Create  $\rightarrow$  Shape  $\rightarrow$  Rectangle."



### **Integrated Circuit Design CAD Tool Information**

**w.** Click on your layout and type 'I'. Select a via between metal1 and polysilicon, which is known as a 'm1\_poly' instance. Fill out the "Create Instance" window as shown below: "NCSU\_TechLib\_ami06  $\rightarrow$  m1\_poly  $\rightarrow$  layout."

	Create Instance	×
Library	NCSU_TechLib_ami06 Browse	Â
Cell	m1_poly	
View	layout	
Names	I7	
Mosaic	Rows 1 Columns 1 Delta Y 1.2 Delta X 1.2	
Halo	Define Halo	
Physical Only		
A Rotate A Sideways		
Rows of contacts 1		
Columns of contacts		
	Hide Cancel Defaults Help	

# **Integrated Circuit Design CAD Tool Information**

**x.** Select the "m1\_poly" instance as shown in the Library Browser. Instantiate two instances of "m1\_poly" vias at the input of your inverter.

Library	y Browser - Create I	nstance	
Show Categories Library	Cell	View	
NCSU_TechLib_ami06 EENG653 NCSU_Analog_Parts NCSU_Digital_Parts NCSU_TechLib_ami06 NCSU_TechLib_ami16 NCSU_TechLib_hp06 NCSU_TechLib_tsmc02 NCSU_TechLib_tsmc02d NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03d NCSU_TechLib_tsmc03d NCSU_TechLib_tsmc04 4M2P	m1_poly M1_ELEC M1_N M1_P M1_POLY M2_M1 M3_M2 NTAP active elec m1_elec m1_n	Iayout	Si
avTech basic cdsDefTechLib megan	m1_p m1_poly m2_m1 m3_m2 metal1 metal2	Display	Help

#### **Integrated Circuit Design CAD Tool Information**

**y.** Click on your layout and type 'I' in the layout. Create two instances of an "m2\_m1" via between metal2 and metal1. Fill in the "Create Instance" window with "NCSU\_TechLib\_ami06  $\rightarrow$  m2\_m1  $\rightarrow$  layout."

	Create Instance	<u>(</u> )
Library	NCSU_TechLib_ami06 Browse	
Cell	m2_m1	
View	layout	
Names	19	
Mosaic	Rows 1 Columns 1 Delta Y 1.2 Delta X 1.2	
Halo	Define Halo	
Physical Only		
A Rotate A Sideways		
Rows of contacts		
Columns (	of contacts 1 Hide Cancel Defaults Help	2

# **Integrated Circuit Design CAD Tool Information**

**z.** The "Library Browser" window for the m2\_m1 via will appear as shown in the figure below.

Library	Cell	h	View	
NCSU_TechLib_ami06	m2_m1		layout	
EENG653 NCSU_Analog_Parts NCSU_Digital_Parts NCSU_TechLib_ami06 NCSU_TechLib_ami16 NCSU_TechLib_hp06 NCSU_TechLib_tsmc02 NCSU_TechLib_tsmc02d NCSU_TechLib_tsmc03d NCSU_TechLib_tsmc03d NCSU_TechLib_tsmc04_4M2P avTech basic cdsDefTechLib megan	M1_ELEC M1_N M1_P M1_POLY M2_M1 M3_M2 NTAP active elec m1_elec m1_n m1_p m1_poly m2_m1 m3_m2 metal1 metal2		View A Loci	k :

### **Integrated Circuit Design CAD Tool Information**

**aa.** Position two instances of "m2\_m1" vias at the input of your inverter and two instances of "m2\_m1" vias at the output of your inverter, as shown in the image below. Also add m1 and m2 stripes at the input and output (as shown in the image) to cover the m2\_m1 vias.

Virtuoso@ Layout Suite L Editing: EENG653 inverter layout	_ • ×
Launch Eile Edit View Create Vertfy Connectivity Options Tools Window Assura GRC Optimize NCSU Help	cādence
🕂 🙀 🍘 🎕 🔍 🖓 🏰 🔲 🗰 (F)Select0 Sel(N):0 Sel(0):0 Sel(0):0 X:-7.8000 V:9.6000 dX:0.1500 dY:2.5500 Dist2.5544 Cmd:	
Objects ? 6 ×	
Object V S	
Polygon 🗹 🗹	
- Rectangle 🖌 M	
🛛 – Fluid Guardring 🕑 – La cala a c	
Fluid Shapes 🗹	
📙 Fig Groups 🔄 🖌	
- Area Bound 🗹 📋	
- Snap Bound 🖉 🔤	
P&R Bound	
- Halo Blocka 🗹 🗹 🖉 - A second se	
- Placement B 🗹 🗹	
B - Pin Blockage 🖌 🖌	
Objects Guides	
mouse L: showClickInfo) M: IeHiSearch()	R: _IxHiMousePopUp()
4(3) >	Cmd:

#### **Integrated Circuit Design CAD Tool Information**

**bb.** You will now create pins for "Vin" and "Vout". Click on your inverter layout and select "Create  $\rightarrow$  Pin". Fill in the windows as shown below to create these pins and place "Vin" pin at the input (I/O type is input) and "Vout" pin at the output (I/O type is output). These pins should be on the same metal layer as the metal they are connected to; their purpose, however, is 'pin' (pn) rather than 'drawing' purpose of the metal rectangle. Also create "VDD" and "GND" pins (set I/O type to be inputOutput) on the Create Shape Pin form for these pins. Be sure to check the box next to 'Display Terminal Name' to display the terminal name in the layout.

	Create Shape Pin	×
Connectivity	💿 strong 🔾 weak	
Terminal Names	Vin Physical Only	
📃 Keep First Nar	ne X Pitch 0 Y Pitch 0	
🗹 Display Termin	al Name Display Terminal Name Option	
🔲 Create as ROE	) Object	
Name	rect0	
Mode	💿 rectangle 🔾 dot 🔾 polygon 🔾 circle 🔾 auto pin	
I/O Type	💿 input 🔾 output 🔾 inputOutput 🔾 switch	
	🔾 jumper 🔾 unused 🔾 tristate	
Snap Mode	orthogonal 🔽	
Access Direction	🗹 Top 🔽 Bottom 🖌 Left 🖌 Right	
	🗹 Any 🔲 None	
	Hide Cancel He	lp

# **Integrated Circuit Design CAD Tool Information**

	Create Shape Pin	X
Connectivity	💿 strong 🔾 weak	
Terminal Names	Vout Physical Only	
🔲 Keep First Nar	ne X Pitch 0 Y Pitch 0	
🗹 Display Termir	al Name Display Terminal Name Option	
🔲 Create as ROE	) Object	
Name	rectO	
Mode	💿 rectangle 🔾 dot 🔾 polygon 🔾 circle 🔾 auto pin	
I/O Type	🔾 input 💿 output 🔾 inputOutput 🔾 switch	
	🔾 jumper 🔾 unused 🔾 tristate	
Snap Mode	orthogonal 🔽	
Access Direction	🗹 Top 🔽 Bottom 🗹 Left 🗹 Right	
	🗹 Any 🔲 None	
	Hide Cancel He	lp)

	Create Shape Pin 🗙
Connectivity	🖲 strong 🔾 weak
Terminal Names	gnd Physical Only
🔲 Keep First Nar	ne X Pitch 0 Y Pitch 0
🗹 Display Termir	al Name Display Terminal Name Option
🔲 Create as ROE	) Object
Name	rect0
Mode	● rectangle 🥥 dot 🔾 polygon 🔾 circle 🔾 auto pin
I/O Type	🔾 input 🔍 output 💿 inputOutput 🔾 switch
	🔾 jumper 🔾 unused 🔾 tristate
Snap Mode	orthogonal 🔽
Access Direction	🗹 Top 🗹 Bottom 🗹 Left 🗹 Right
	🗹 Any 🔲 None
	Hide Cancel Help

### **Integrated Circuit Design CAD Tool Information**

**cc.** Make sure to label the pins with the same name as in the schematic, namely "VDD," "GND," "Vin," and "Vout." You will need to separate the vias as shown in the layout below (the separation is required in order to pass Design Rule Checks – DRC – as discussed below in the next section).

After creating the "Vin" pin, highlight the pin and type 'Q.' In the 'Edit Rectangle Pin Properties' window, click on the 'Attribute' radio button. Set the 'Pin Name' to 'Vin' and set 'Terminal Name' to 'Vin.'

After creating the "Vout" pin, highlight the pin and type 'Q.' In the 'Edit Rectangle Pin Properties' window, click on the 'Attribute' radio button. Set the 'Pin Name' to 'Vout' and set 'Terminal Name' to 'Vout.'



# **Integrated Circuit Design CAD Tool Information**

Useful notkeys for Designing Custom Layouts		
m	Move	
Keyboard arrows: up,	Move around the layout screen	
down, left, right		
Ctrl/Shift z	Zoom in/out	
F2	Save the design	
ESC	Cancel the previous command	
Shift f	Reveal all mask layers within each instantiated layout	
	cell (metal layers and via layers)	
Cntl f	Hide the mask layers and display the red instance boxes	
	instead	
q	Properties	
р	Create a path (Paths are convenient for making	
	interconnections between I/O pins of a layout cell; be	
	sure to select the desired metal layer from the LSW first	
	before typing 'p').	
r	Create a rectangle	
Cntl p	Create a pin	
i	Instantiate a cell layout	
Hold down shift key	Select more than one mask layer simultaneously. (Use	
and click on each	cntl to deselect a particular layer)	
layer		
u	Undo	
С	Сору	
d	Delete	
S	Stretch	
k	Display the ruler (very helpful)	
Shift-k	Hide the ruler	

### **Integrated Circuit Design CAD Tool Information**

### 16. Inverter: Running Design Rule Check (DRC)

a. Now you will run Design Rule Check (DRC) on your layout. DRC is a software program that inspects your layout for violations of the design rules and inserts markers at locations where any design rule violations are found. To run DRC, click on your layout. From the banner at the top of the layout, select "Verify → DRC." The "DRC" window will appear. Check the boxes as shown, making sure to check the Rules Library checkbox and setting the field to "NCSU\_TechLib\_ami06" as shown in the two windows below (note that the name of the TechFile is long).

	DRC
Checking Method   flat Checking Limit	<ul> <li>hierarchical</li> <li>hier w/o optimization</li> <li>incremental</li> <li>by area</li> </ul>
Switch Names	Set Switches
Run-Specific Command File	
Inclusion Limit	1000 Limit Rule Errors 🔲 0
Join Nets With Same Name	Limit Run Errors
Echo Commands	⊻
Rules File	divaDRC.rul
Rules Library	MCSU_TechLib_am
Machine	● local ◯ remote Machine
Ignore Missing Cell Masters	
	OK Cancel Defaults Apply Help

# **Integrated Circuit Design CAD Tool Information**

	DRC X
Checking Method 💿 flat	◯ hierarchical ◯ hier w/o optimization
Checking Limit 💿 full	🔾 incremental 🔾 by area
Coordi	nate Sel by Cursor
Switch Names	Set Switches
Run-Specific Command File	
Inclusion Limit	1000 Limit Rule Errors 🔲 0
Join Nets With Same Name	Limit Run Errors
Echo Commands	
Rules File	divaDRC.rul
Rules Library	☑ U_TechLib_ami06
Machine	🖲 local 🔾 remote 🛛 Machine
Ignore Missing Cell Masters	
	OK Cancel Defaults Apply Help

# **Integrated Circuit Design CAD Tool Information**

**b.** Click "OK" in the DRC window. "DRC" will run, and if it completes successfully, the log file in the CIW will report "Total errors found: 0" as shown in the window below.

C	Virtuoso© 6.1.5-64b - Log: /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/CDS.09APR2012a.log	
File <u>T</u> ools <u>O</u> p	ns <u>H</u> elp	cādence
executing: drc executing: drc executing: sav executing: drc drc executing: sav executing: sav executing: drc executing: drc executing: drc executing: drc executing: sav executing: drc drc drc drc drc drc drc drc drc drc	<pre>ia2 (area &gt; ((lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1))) etal3Edge via2Edge (enc &lt; (lambda * 1.0)) errMesg) etal3Edge (width &lt; (lambda * 5.0)) errMesg) etal3Edge (sep &lt; (lambda * 3.0)) errMesg) etal3Edge (sep &lt; (lambda * 3.0)) errMesg) etal3Edge (sep &lt; (lambda * 3.0)) errMesg) ighresEdge (vidth &lt; (lambda * 4.0)) errMesg) ighresEdge (sep &lt; (lambda * 4.0)) errMesg) ighresEdge (sep &lt; (lambda * 2.0)) errMesg) ighresEdge ceEdge (sep &lt; (lambda * 2.0)) errMesg) ighresEdge schiveEdge (sep &lt; (lambda * 2.0)) errMesg) ighresEdge schiveEdge (sep &lt; (lambda * 2.0)) errMesg) ighresEdge schiveEdge (sep &lt; (lambda * 2.0)) errMesg) ighresEdge gendeEtdge(geonAndNot(elec genoButting(elec elecHighres))) (sep &lt; ( erived(genaButting(elecHighres mell) * (SCMOS Rule 27.6) resistor must be outside w erived(genaButting(elecHighres active) * (SCMOS Rule 27.6) resistor must be outside w erived(genaButting(elecHighres active) * (SCMOS Rule 27.6) resistor must be outside w erived(genaButting(elecHighres active) * (SCMOS Rule 27.6) resistor must be outside w erived(genaButting(elecHighres des 1.0)) errMesg) lecHighresEdge (sep &lt; (lambda * 7.0)) errMesg) lecHighresEdge (sep &lt; (lambda * 7.0)) errMesg) Mon Apr 9 16:47:57 2012 Mon Apr 9 16:47:57 2012 0:00:00 TOTAL THE = 00:00:00 ary of rule violations for cell *inverter layout" ******** found: 0</pre>	0
mouse L: showC	xkinfo() M: leHiSave()	R: _IxHiMousePopUp()
1 >		

### **Integrated Circuit Design CAD Tool Information**

- **c.** If there are errors in the layout as identified by "DRC," the errors will be identified with white markers in the layout. To see these errors, click on the layout window. Then, click on "Verify  $\rightarrow$  Markers  $\rightarrow$  Find" to look at the errors.
- **d.** Correct the errors and re-run "DRC." Proceed to the next step, Extraction, only after "DRC" passes with no errors.
- **e.** You have now completed Design Rule Check.

### **Integrated Circuit Design CAD Tool Information**

### **17.** Inverter: Running Extraction

a. In this step, you will run extraction to extract circuit models from your layout. Click on your layout. Then select "Verify → Extract" from the banner. The "Extractor" window will appear as shown below in the two images. Note that the Rules library field should be set to "NCSU\_TechLib\_ami06." (note that the 'Rules Library' window in each image is slightly different because the name is too long for the field width).

In the 'Extractor' form, click on 'Set Switches,' and a window titled 'Set Switches' will appear as shown in the third image below (next page). In the 'Set Switches' window, select 'Extract\_parasitic\_caps' which will highlight this text as shown in the image. Click 'OK' in the 'Set Switches' window.

	Extractor
Extract Method 💿 flat	: 🔾 macro cell 🔾 full hier 🔾 incremental hier
View Names Extracted	extracted Excell excell
Switch Names	Extract_parasitic_caps Set Switches
Run-Specific Command File	
Inclusion Limit	1000 Limit Rule Errors 🔲 0
Join Nets With Same Name	Limit Run Errors D
Echo Commands	
Rules File	divaEXT.rul
Rules Library	NCSU_TechLib_am
Machine	● local ⊖ remote Machine
Ignore Missing Cell Masters	
	OK Cancel Defaults Apply Help

# **Integrated Circuit Design CAD Tool Information**

	Extractor	X
Extract Method 💿 fla	t $\bigcirc$ macro cell $\bigcirc$ full hier $\bigcirc$ incremental hier	
View Names Extracted	extracted Excell excell	
Switch Names	Extract_parasitic_caps Set Switches	
Run-Specific Command File		
Inclusion Limit	1000 Limit Rule Errors 🔲 0	
Join Nets With Same Name	Limit Run Errors	
Echo Commands	⊻	
Rules File	divaEXT.rul	
Rules Library	U_TechLib_ami06	
Machine	● local	
Ignore Missing Cell Masters		
	OK Cancel Defaults Apply He	p

Set Switches(Ctrl+mouse for multiple) X
Extract_parasitic_caps
Keep_labels_in_extracted_view
Layer_convert_[np]active_to_active
Layer_convert_active_to_[np]active
Layer_create_nselect_around_nactive
Layer_create_pselect_around_pactive
Layer_create_select_around_field_poly
use_ord_moscap_extraction
OK Cancel Help

# **Integrated Circuit Design CAD Tool Information**

- **b.** Click "OK" on the Extractor form.
- **c.** After Extraction runs, the log file in the CIW will report any errors. If there are no errors, the log file will report that "Total errors found: 0" as shown in the image below.

Č Virtuoso® 6.1.5-64b - Log: /home/a	fiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/CDS.09APR2012a.log	_ 🗆 🗙
File Tools Options Help		cādence
executing: saveInterconnect((nDiff "active"))		
executing: saveInterconnect((polu "polu"))		
executing: saveInterconnect((metall "metall"))		
executing: saveInterconnect((nObmicContact "cc"))		
executing: saveInterconnect((pOhmicContact "cc"))		
executing: saveInterconnect((nDiffContact "cc"))		
executing: saveInterconnect((pDiffContact "cc"))		
executing: saveInterconnect((cp "cc"))		
executing: saveInterconnect((metal2 "metal2"))		
executing: saveInterconnect((via "via"))		
executing: saveInterconnect((metal3 "metal3"))		
executing: saveInterconnect((via2 "via2"))		
executing: saveInterconnect((nweILRes "res_id"))		
executing: saveInterconnect((polyNes "res_id"))		
executing: saveInterconnect((eleckes "res_1d"))		
executing: saveInterconnect((erechightes res_id)))		
executing: saveberived(metal1 ( metal1 "net") cell view)		
executing: saveDerived(wecais ( metais ( metais ) cell view)		
executing: saveDerived(metal3 ("metal3" "met") cell view)		
executing: saveDerived(via2 ("via2" "net") cell view)		
Extraction started Mon Apr 9 16:56:04 2012		
completed Mon Apr 9 16:56:05 2012		
CPU TIME = 00:00:00 TOTAL TIME = 00:00:01		
********* Summary of rule violations for cell "inverter layout"	****	
Total errors found: O		
saving rep EENG653/inverter/extracted		
Getting Layout propert bagGetting Layout propert bag		
t		
mouse L: showClickInfo()	M: setExtForm()	R: _IxHiMousePopUp()
1 >		

## **Integrated Circuit Design CAD Tool Information**

**d.** The 'extracted' view will appear in the Library Manager for the layout as shown in the image below. Note that your layout for the cell 'inverter' in the library 'EENG653' now contains four cellviews: an 'extracted' view, a 'layout' view, a 'schematic' view, and a 'symbol' view.

Library	Manager: Directoryro/cadence/ncsu-cdk-1.6.0.	beta	
<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>D</u> esign Manager <u>H</u> elp			cādence
Show Categories Show Files Ubrary	Cell	View	
EENG653	inverter	extracted	
EENG653 NCSU_Analog_Parts NCSU_Digital_Parts NCSU_TechLib_ami06 NCSU_TechLib_ami06 NCSU_TechLib_tsmc02 NCSU_TechLib_tsmc02d NCSU_TechLib_tsmc03d NCSU_TechLib_tsmc03d NCSU_TechLib_tsmc04_4M2P avTech basic cdsDefTechLib megan	inv_test inverter zpcellSCRATCHYdjrGN227202	View Lock extracted Schematic symbol United Stresses Symbol	Size 29k 29k 29k 23k
Messages         Log file is "/home/aften3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/dblbManager.log".         Loading NCSU Library Manager customizationsdone.         Warning: LIB EENG653 from File /home/aften3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/cds.lib Line 19 redefines         LIB EENG653 from File /home/aften3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/cds.lib Line 19 redefines         but was defined in libFile /home/aften3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/cds.lib Line 19 redefines         but was defined in libFile /home/aften3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/cds.lib' for Lib 'EENG695'.         Warning: The directory: 'home/aften3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/cds.lib' for Lib 'EENG695'.         Warning: The directory: 'home/aften3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/cds.lib' for Lib 'dave'.         Warning: IB EENG653 from File /home/aften3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/cds.lib' for Lib 'dave'.         Warning: LIB EENG653 from File /home/aften3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/cds.lib' for Lib 'dave'.         Warning: LIB EENG653 from File /home/aften3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/cds.lib' for Lib 'dave'.         Warning: LIB EENG655 from File /home/aften3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/cds.lib Line 19 redefines         Warning: LIB EENG655       Tom File /home/aften3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/cds.lib Line 19 redefines			

### **Integrated Circuit Design CAD Tool Information**

**e.** Double-click on the 'extracted' view to open it and obtain the image shown below. Notice the pins: VDD, GND, Vin, and Vout. Outlines are shown for the metal layers: polysilicon, metal1, metal2, vias, and wells. The outlines show the connectivity of the circuit (the shapes are merged together to show the shapes that are electrically connected).



# **Integrated Circuit Design CAD Tool Information**

**f.** You can click on the 'Vin' pin and obtain the image shown below. Notice that all shapes connected to 'Vin' are highlighted in white.

<b>M</b>	Virtuoso® Layout Suite L Editing: EENG653 inverter extracted	_ <b>_ X</b>
Launch <u>F</u> ile <u>E</u> dit <u>V</u> iew <u>C</u> re	reate Verify Co <u>n</u> nectivity <u>O</u> ptions <u>T</u> ools <u>W</u> indow Ass <u>u</u> ra QRC Opti <u>m</u> ize NCSU <u>H</u> elp	cādence
🗈 🖯 🗠 🤞	• 🗅 💷 🗶 💤 🛈 ⊨   🕹 »   🔍 »   🎝 🚈 »   Workspace: Classic 🗾 🗣 🗔	
🖳 🔩 🍰 🎕 🖓 4	실 🖳 🛄 👘 🕐 📗 (F)Select:1 Sel(N):1 Sel(I):0 Sel(O):1   X:-4.5000 Y:9.4500 dX:-17.4000 dY:10.3500 Dist20.2456	Cmd:
Layers ? 🗗 🗙		l l
AV NV AS NS		
📓 metal1 drawing 🔽 👻		
🍸 All Valid Layers 🗧 🔌		
Used Layers Only		
🔍 Search 🔽 🔻		
🔨 Layer Purpose V S 🔼		
met drawing 🗹 🗹	· · · · · · · · · · · · · · · · · · ·	<b>-</b>
📝 met drawing 🔽 🗹	· · · · · · · · · · · · · · · · · · ·	
🚺 CC drawing 🗹 🗹		
🗱 via2 drawing 🗹 🗹		
ingh drawing 🗹 🗹		
🔀 nodrc drawing 🗹 🗹 📄		
🛃 holpe drawing 👱 👱		
🔲 text drawing 🗹 🗹		
🚛 res_id drawing 🗹 🗹		
🚮 dio_id drawing 🗹 🗹		
nwell net 🗹 🗹		
🗖 active net 🛛 🗹		
nact net		
Objects ? 🗗 🗙		
Object V S 🛆		
- Circle/Elli 🗹 🗹		
Donut 🗹 🗹		
Path V		
- PathSeg 🗹 🗹		
Rectangle 🗹 🗹 🚽		
Objects Guides		
mouse L: showClickInfo()	M: hiZoomAbsoluteScale(hiGetCurrentWindow() 0.9) R:	_IxHiMousePopUp()
6(11) >		Cmd:

# **Integrated Circuit Design CAD Tool Information**

**g.** You can also click on the 'Vout' pin and obtain the image shown below. Notice that all shapes connected to 'Vout' are highlighted in white.



**h.** You have now completed Extraction of your layout.

## **Integrated Circuit Design CAD Tool Information**

### **18.** Inverter: Running Layout Versus Schematic (LVS)

**a.** Now you will compare your layout with your schematic. Ideally, the connectivity in the layout will match the connectivity in the schematic. Running the software tool "LVS" will help you to verify if the netlist of your layout does match the netlist of your schematic. First, click on your layout. From the banner at the top of the layout, select "Verify  $\rightarrow$  LVS." The "Artist LVS" window will appear as shown in the image below. Fill in the fields as shown in the image.

C Artist LVS – 🗆			
Commands <u>H</u> elp cādenc			
Run Directory	L¥S	Browse	
Create Netlist Library	✓ schematic ✓ extracted EENG653 EENG653		
Cell	inverter inverter		
View	schematic extracted		
	Browse Sel by Cursor Browse S	el by Cursor	
Rules File	divaLVS.rul	Browse	
Rules Library	NCSU_TechLib_ami06		
LVS Options	LVS Options  Rewiring  Device Fixing Create Cross Reference  Terminals		
Correspondence	File 🗌 🔤 Ivs_corr_file	Create	
Switch Names			
Priority 0	Run background		
Run	Run Output Error Display Monitor Info		
Backannotate Parasitic Probe Build Analog Build Mixed			
12 HelpAction			

# **Integrated Circuit Design CAD Tool Information**

**b.** LVS will now run and compare the connectivity in the layout cellview (in the image below) with your schematic.



### **Integrated Circuit Design CAD Tool Information**

**c.** When LVS completes, and if the net-lists match, a window will appear showing that "The LVS job has completed. The net-lists match," and the window will provide the path to the Run Directory.



### **Integrated Circuit Design CAD Tool Information**

**d.** After running "LVS," the CIW will report the si.out file (log file for the LVS run) as shown in the image below. Notice that when LVS passes, the si.out file indicates that "The net-lists match."

C		/home/a	fiten3/fac/	mlanzero/o	adence/ncsu-cdk-1.6.0.beta/LVS/si.out	>
<u>F</u> ile <u>H</u> elp						cādence
Net swappi Using term Compiling	ng is enabled Ninal names as Diva LVS rule	l. 3 correspon 35	dence point	s.		
Net-li	st summary fo	or /home/af	iten3/fac/m	lanzero/cade	ence/ncsu-cdk-1.6.0.beta/LVS/layout/netlis	st
cou	unt 4		nets			
	1		pmos nmos			
Net-li	st summary fo	or /home/af	iten3/fac/m	lanzero/cade	ence/ncsu-cdk-1.6.0.beta/LVS/schematic/net	clist
cou	unt 4		nets			
	4		pmos			
	-		10100			
Termir NO	N3	lence point	8			
N3 N1	N2 N0	VDD Vin				
Devices in	nt the rules bu	t not in t	he netlist:			
ca	p nfet pfet r	unos4 pmos4				
The net-li	sts match.					
	up matched		Layou	it schemati instances	c	
	rewired		0	0 0	0	=
	pruned active			0 2	0	
	total			2	2	
	un-matched		0	nets 0	0	
	pruned			0	0	
	total			4	4	
	un-matched		0	terminals O		
	matched but different t	ype		1	1	
	COURT			4	7	
Probe file	es from /home,	/afiten3/fa	c/mlanzero/	cadence/ncsi	u-cdk-1.6.0.beta/LVS/schematic	
devbad.out						
mergenet o	ut.					
termbad.ou	it:					
? Terminal	. Vout's type	in the sch	ematic: inp	ut, in the l	Layout: output	
prunenet.c	out:					
audit out	JUC:					
Probe file	es from /home,	/afiten3/fa	c/mlanzero/	cadence/ncsi	u-cdk-1.6.0.beta/LVS/layout	
devbad.out						
netoad.out	ant.					
termbad.ou	it:					
? Terminal	. Vout's type	in the lay	out: output	, in the sch	nematic: input	
prunenet.c	out:					
prunedev. o	out:					
auure. oue:						
16						F

## **Integrated Circuit Design CAD Tool Information**

**e.** If errors are found by LVS, a window "Artist LVS Error Display," can be used to identify the error markers.

Artist LVS Error Display
Display First Next Prev Last
Error Color hilite dg
All       ✓       Unmatched       ✓       nets       ✓       parameters       ✓       terminals         All       ✓       Pruned       ✓       nets       ✓       instances         None       Omeged       ✓       nets       Net Display Limit       100
OK Cancel Explain Clear Display Probe Form Help

**f.** Fix any errors that may exist in the layout. Re-run LVS until no errors are reported. If LVS passes with no errors, you have now completed LVS.

# **Integrated Circuit Design CAD Tool Information**

# **19.** Inverter: Running Extracted-Layout Simulation

- **a.** Now you will simulate your design using the extracted capacitances that you obtained during the "Extraction" step. The extraction cellview will change as the layout changes, and a post-layout simulation will indicate how the layout of your inverter will perform compared with your idealized schematic (your schematic does not contain any parasitic capacitances). The procedure that you will use is the same as the procedure for simulating the schematic view (described in a previous step).
- **b.** Open your library "EENG653" cell "inv\_test" cellview "schematic" from the Library Manager as shown below.



# **Integrated Circuit Design CAD Tool Information**

**c.** Click on the schematic window. Using the banner at the top of the schematic window, click on "Launch  $\rightarrow$  ADE L" to bring up the 'Virtuoso Analog Design Environment' window shown below.

👫 Virtuoso® Analog Design E	nvironment (1) - EENG653 inv_test schematic
Session Setup Analyses Variables Ou	tputs Simulation Results Tools Help cadence
27	
Design Variables Name Value	Analyses ? Type Enable Arguments  Arguments  Acc Type  Acc Type Acc Ty
>	Name/Signal/Expr   Value   Plot   Save   Save Options   M Plot after simulation: Auto Plotting mode: Replace R
5(6) Environment	Status: Ready   T=27 C   Simulator: spectre

### **Integrated Circuit Design CAD Tool Information**

- **d.** Now we will set up to display the simulation results for your schematic and for your extracted view in the same window. The first step is to first simulate your schematic with DC mode and transient mode options as before and display your results in the display window. (Be sure to follow all of the steps involved in setting up a simulation that were shown in previous sections).
- e. Click on the "Virtuoso Analog Design Environment" window for your "EENG653 inv\_test schematic". On the banner at the top of the window, select "Setup → Environment," and a window named "Environment Options" will appear as shown in the image below. In the 'Switch View List' in the 'Environment Options' window, add 'extracted' between 'cmos.sch' and 'schematic' so that the field appears as shown in the image.

Environment Options			
Switch View List	spectre cmos_sch cmos.sch extracted schematic veriloga		
Stop View List	spectre		
Parameter Range Checking File			
Print Comments			
userCmdLineOption			
Automatic output log	⊻		
savestate(ss):			
recover(rec):			
Run with 64 bit binary			
Using colon as Term Delimiter			
	OK Cancel Defaults Apply Help		

### **Integrated Circuit Design CAD Tool Information**

**f.** Open the "Environment Options" window and resimulate with your extracted view as shown in the image in (e) (above). In the "Virtuoso Analog Design Environment" window for your "EE653 inv\_test schematic", select the "Append" radio button next to the "Plotting mode" at the lower right-hand corner of the form.

🚪 Virtuos	o® Analog Desig	n Environment (2) - EENG653 inv_test schematic	
Session Setup	Analyses Variables	Outputs Simulation Results Tools Help	cādence
III 27 I			
Design Variables	Value	Analyses       Type     Enable     Arguments       1     tran     ✓     0     10u       2     dc     ✓     t	
		Outputs Name/Signal/Expr   Value   Plot   Save   Save C	Pptions
> Immouse L: 12(20) Transient	Signal	Plot after simulation: Auto Plotting mode: Append M: Status: Ready   T=27 C   Simu	R:

### **Integrated Circuit Design CAD Tool Information**

**g.** When you append the results of the extracted simulation to the results of the schematic simulation, the results will be shown together, as shown in the image below where the waveforms show that the simulations match well (Note that you can measure waveforms with the cursor in the window):



## **Integrated Circuit Design CAD Tool Information**

**h.** Now you have simulated your schematic view and your extracted view of your inverter. For a layout with a lot of extra wire (extra metal layer), the simulation of the extracted view will not closely match the simulation of the schematic view.
### **Integrated Circuit Design CAD Tool Information**

### 20. Inverter: Simulation with NC-Verilog

- **a.** You will now learn to perform digital logic design in the Cadence environment with a software tool called "NC-Verilog." "NC-Verilog" performs logic design at the functional level, such as logic design of your inverter. In this section, you will create a verilog file for your inverter design and will simulate the function of this inverter using Cadence.
- **b.** First, open the Library Manager. Select your library "EENG653", the cellname "inverter" and viewname "schematic" as shown in the image below.

Library Mai	nager: Directoryro/cadence/ncsu-cdk-1.6.0.beta	
<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>D</u> esign Manager <u>H</u> elp		cā den ce
Show Categories Show Files  Ubrary  EENG653  FenG653  NCSU_PachLib_ami06 NCSU_TechLib_ami06 NCSU_TechLib_ami06 NCSU_TechLib_hp06 NCSU_TechLib_tsmc02 NCSU_TechLib_tsmc02d NCSU_TechLib_tsmc03d NCSU_TechLib_tsmc03d NCSU_TechLib_tsmc04_4M2P avTech basic cdsDefTechLib megan	Cell Inv_test Inv_test Inverter	View       schematic       View     Lock       extracted     2       functional     11       layout     3       schematic     mlanzero@vlsifac01       symbol     2
Messages Log file is "/home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.f Loading NCSU Library Manager customizationsdone. Deleting view "functional" from cell "inverter" in library "EEN Deleted cellview 'EENG653/inverter/functional' Deletion of 1 Deleting view "function" from cell "inverter" in library "EENG6 Deleted cellview 'EENG653/inverter/function'.Deletion of 1 vi	3.0.beta/libManager.log". 3653". view done. 353". ew done.	

## **Integrated Circuit Design CAD Tool Information**

**c.** Open the schematic. The "Virtuoso Schematic Editor" window will display your schematic as shown in the image below.



### **Integrated Circuit Design CAD Tool Information**

**d.** Click on your schematic. At the banner of the schematic, select "Launch  $\rightarrow$  Simulation  $\rightarrow$  NC-Verilog" which will launch the "Virtuoso Verilog Environment for NC-Verilog Integration" window shown in the image below.

10	Virtuoso®	Verilog Env	vironment for N	IC-Verilog li	ntegration	
<u>C</u> ommar	nds <u>S</u> etup <u>R</u> esults j	<u>H</u> elp				cādence
III Status:	SimVision Launched					
_	Run Directory					
	/home/afiten3/fac	/mlanzero/ca	dence/ncsu-cdk-1	6.0.beta/in	verter_run1	
<u>z</u>	- Top Level Design-					
*C	Library		Cell		View	
	EENG653		inverter		schematic	
			Browse		Hierarchy I	Editor
	Simulation Mode — Batch					
	<ul> <li>Interactive</li> </ul>	(Choose S	Steps):			
		🗹 Comp	pile 🗹	Elaborate	🗹 Simula	te
-0-						
ч <sup>_</sup> Гч						
www.						
15 Initia	lize Design					

### **Integrated Circuit Design CAD Tool Information**

e. On the "Virtuoso Verilog Environment for NC-Verilog Integration" form, select "Setup → Record Signals." The window "Record Signals Setup" will appear as shown in the image below. Complete this form, change the depth of '1' to a depth of '100,' click "All" and click "OK" on the form. (It is reported that this is a bug in Cadence.)

If this step does not work the first time, click "Initialize Design" (the runner on the left-hand side of the window) in the "Virtuoso Verilog Environment for NC-Verilog Integration" window. Then click on "Setup  $\rightarrow$  Record Signals" and follow the previous steps in (e).



- **f.** In the "Virtuoso Verilog Environment for NC-Verilog Integration" window, click "Initialize Design" (the runner on the left-hand side of the window.
- **g.** Then in the "Virtuoso Verilog Environment for NC-Verilog Integration" window, click "Generate Netlist" (the three boxes with checks on the left-hand side of the window. Each time that you change your design, you need to re-netlist it.
- h. In the "Virtuoso Verilog Environment for NC-Verilog Integration" window, click "Commands → Edit TestFixture," and the "Edit Test Fixture" window will appear as shown in the image below.

Edit Test Fixture
TestBench
File Name eta/inverter_run1/testfixture.template 🚽 📝 🕒 🗶
Set Selected File As TestBench Check Syntax
Stimulus
File Name beta/inverter_run1/testfixture.verilog 🔽 🦲 😰 🗱
Set Selected File As Stimulus Check Syntax
OK Cancel Defaults Apply Help

# **Integrated Circuit Design CAD Tool Information**

**i.** You may view the testfixture.template file. Emacs is one editor that can be used to edit the file as shown in the images below.

ſ	mlanzero@visifac01	
	<pre>[mlanzero@vlsifac01 ncsu-cdk-1.6.0.beta]\$ ls CDS.09APR2012.log CDS.10APR2012b.log LVS inv_test libManager.log CDS.09APR2012.log CDS.10APR2012c.log LVS inv_test libManager.log.cdslck CDS.10APR2012.log CDS.11APR2012.log cds.lib inverter_run1 megan CDS.10APR2012a.log CDS.11APR2012.log.cdslck cds.lib lib.defs mycds.lib [mlanzero@vlsifac01 ncsu-cdk-1.6.0.beta]\$ cd inverter_run1</pre>	
	<pre>Intal2eroevisifac01 inverter_runifs is INCA_libs ihn! raw si.foregnd.log testfixture.verilog control map shm.db simout.tmp testfixture.verilog~ hdJFileeDir ncxlmode.key si.env testfixture.template verilog.inpfiles [mlanzero@vlsifac01 inverter_runi]\$ pwd /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/inverter_run1 [mlanzero@vlsifac01 inverter_runi]\$ emacs testfixture.template &amp; [11 24383</pre>	
	[mlanzero@vlsifac01 inverter_run1]\$ [	

emacs@visifac01.afit.edu	. 🗆 🗙
File Edit Options Buffers Tools Help	
0 11 × 11 12 1 × 11 12 12 12 12 12 12 12 12 12 12 12 12	
<pre>     U timescale ins / ins     nodule test;     vire Vout;     vire Vout;     vire 00D, VDD;     reg Vin;     reg i_OND, io_VDD;     // Inout assignments     ods_mlias_inst1(VDD, io_VDD);     ids_mlias_inst2(OND, io_NDD);     inverter top(Vout, GND, VDD, Vin);     'ifdef verilog     '//please enter any additional verilog stimulus in the /home/sfiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/inverter_runl/testfixture.verilog file     ''home/sfiten3/fac/alanzero/cadence/ncsu-cdk-1.6.0.beta/inverter_runl/testfixture.verilog"     'endif     endmodule </pre>	
<pre>↓ // //</pre>	
耳 For information about the GNU Project and its goals, type C-h C-p.	

# **Integrated Circuit Design CAD Tool Information**

**j.** You may view the testfixture.verilog file. Emacs is one editor that can be used to edit the file as shown in the image below.

mianzero@visifac01	_ 🗆 🗙
<pre>[mlanzero@vlsifac01 ncsu-cdk-1.6.0.beta]\$ ls CDS.09APR2012.log CDS.10APR2012b.log EENG653 display.drf libManager. CDS.09APR2012.log CDS.10APR2012c.log LVS inv_test libManager. CDS.10APR2012.log CDS.11APR2012.log cds.lib inverter_run1 megan CDS.10APR2012.log CDS.11APR2012.log cds.lib lib.defs mycds.lib [nlanzero@vlsifac01 ncsu-cdk-1.6.0.beta]\$ cd inverter_run1</pre>	.log .log.cdslck
INCA_libs incl read si.foregnd.log testfixture.verilog control map sin.db simout.tmp testfixture.verilog" hdlFileSDir ncxImode.key si.env testfixture.template verilog.inpfiles [mlanzero@vlsifac01 inverter_run1]\$ pwd /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/inverter_run1 [nlanzero@vlsifac01 inverter_run1]\$ emacs testfixture.verilog &	
[1] 24425 [mlanzero@vlsifac01 inverter_run1]\$ [	

# **Integrated Circuit Design CAD Tool Information**

**k.** Edit the testfixture.verilog file so that it matches the file shown in the image below.

emacs@vlsifac01.afit.edu
File Edit Options Buffers Tools Help
♥ ♥ × ● Ø > ★ № Ø Q ≤ Ø ?
Verilog stimulus file. // Verilog stimulus file. // Please do not create a module in this file.
// Default verilog stimulus.
initial begin
Vin = 1'b0; io_GND = 1'b0; io_VDD = 1'b1;
#25 Vin = 1'b1; #35 Vin = 1'b0; #75 Vin = 1'b1;
end
-: testfixture.verilog (Fundamental)L1All
For information about the GNU Project and its goals, type C-h C-p.

### **Integrated Circuit Design CAD Tool Information**

 Then click 'Simulate' on the "Virtuoso Verilog Environment for NC-Verilog Integration (the third button on the left-hand side of the form showing an input waveform, a block diagram, and an output waveform). Two windows will appear: "Design Browser 1 – SimVision" and "Console – SimVision" as shown below.



Console - SimVision	
<u>F</u> ile <u>E</u> dit <u>V</u> iew Sim <u>u</u> lation <u>W</u> indows <u>H</u> elp	cādence <sup>°</sup>
🛛 🍄 🦭 🕅 🛍 🗶 🗍 Text Search: 🔽 🛍 👘	
▶ • 🛄 🔣 📔 💾 🛄 🗰 2 135ns + 3 💽	🔕 🐠 💷
<pre>ncsim&gt; ncsim&gt; source /apps/vlsi/Cadence/INCISIV102/tools/inca/files/ncsimrc ncsim&gt; database -open shmWave -shm -default -into shm.db Created default SHM database shmWave ncsim&gt; probe -create -shm test -all -depth 1 Created probe 1 ncsim&gt; run ncsim&gt;</pre>	
SimVision simulator	]

### **Integrated Circuit Design CAD Tool Information**

m. In the "Design Brower 1 – Sim Vision" window, click on 'test' and then select the nodes in the 'Objects' window on the right-hand side of the window. Select the nodes so that they turn yellow: "GND," "VDD," "Vin," "Vout," "io\_GND," and "io\_VDD." Right-click on the yellow nodes and select "Send to waveform window." A new window, "Waveform 1 – SimVision" window will appear as shown in the image below.



### **Integrated Circuit Design CAD Tool Information**

**n.** In the "Waveform 1 – SimVision" window, click on the blue 'Run' button (the blue button with the white arrow pointing to the right). The waveforms for the nodes will appear as shown in green. Notice that the "Vin" signal transitions from  $0 \rightarrow 1$  at 25ns as you specified in the testfixture.verilog file. Also notice that the "Vin" signal transitions from  $1 \rightarrow 0$  at 60ns as you specified in the textfixture.verilog file (that is, it transitions 35 ns after the first transition). Finally, notice that the "Vin" signal transitions from  $0 \rightarrow 1$  again at 135 ns (75 ns after the previous transition), as you specified in the testfixture.verilog file.



- **o.** Notice that in the "Waveform 1 SimVision" window, the "Vout" node is the 'not' of the "Vin" node. This behavior is expected for an inverter.
- **p.** You have now completed the step of running NC-Verilog on an inverter schematic.
- **q.** Note that each time you want to re-run the simulation, you must close SimVision, re-netlist, and click the simulate button again.

# **Integrated Circuit Design CAD Tool Information**

### 21. nFET: Generating I-V Curves for an nFET

**a.** You are now going to generate I-V curves for an nFET with technology AMI 060u C5N (3M, 2P, high-res). Open the Library Manager and create a new library called "EENG653Tutorial" as shown in the image below.

🗆 Library Mana	ger: Directoryro/cadence/ncsu-cdk-1.6.0.beta	
<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>D</u> esign Manager <u>H</u> elp		cādence
Show Categories       Show Files         Library         EENG653Tutorial         EENG653Tutorial         NCSU_Analog_Parts         NCSU_Digital_Parts         NCSU_TechLib_ami06         NCSU_TechLib_ami06         NCSU_TechLib_smc02         NCSU_TechLib_ismc02d         NCSU_TechLib_ismc03d         NCSU_TechLib_ismc03d         NCSU_TechLib_ismc04_4M2P         avTech         basic         cdsDefTechLib         megan	Cell View View IVcurves IVcurv	Lock Size
Messages Log file is "/home/afiten3/fac/mlanzero/cadence/ncsu-cdk-Loading NCSU Library Manager customizationsdone.	-1.6.0.beta/libManager.log*.	

### **Integrated Circuit Design CAD Tool Information**

b. In the Library Manager, click on "File → New → Library" to open the "Create Library" window and complete it as shown. Attach the new library to existing technology library "AMI 0.60u C5N (3M, 2P, highres)." Then click "OK."

	Create Library	×
Library		
Name:	EENG653Tutorial	
Path:		
Technol	ogy Library	
lf this li Otherw Choose	brary will not contain physical design (i.e., layout) data you do not need a tech library. rise, you must either attach to an existing tech library or compile one. e option:	
0	No tech library needed	
۲	Attach to existing tech library> AMI 0.60u C5N (3M, 2P, high-res)	
	Compile tech library	
Misc		
	I/O Pad Type: 💿 Perimeter 🔾 Area array	
	OK Cancel Apply H	lelp

### **Integrated Circuit Design CAD Tool Information**

c. The library "EENG653Tutorial" should now appear in the Library Manager. You are now going to open a new schematic. Click on the Library Manager. Select the library "EENG653Tutorial" and then click "File → New → Cell View" and complete the "New File" window that appears below. Set "Cell" to "Ivcurves" and "View" to "schematic." Then click "OK."

	New File X
File	
Library	EENG653Tutorial
Cell	IVcurves
View	schematic
Туре	schematic 🔽
Application	
Open with	Schematics L
🔲 Always use th	is application for this type of file
Library path file	
mzero/cadence,	/ncsu-cdk-1.6.0.beta/cds.lib
	OK Cancel Help

### **Integrated Circuit Design CAD Tool Information**

**d.** Now you will see the schematic editing window. Spend some time analyzing the window. On the left side, you will see shortcuts to commonly-used commands such as: placing component instances (it looks like an IC), drawing wires, placing ports, stretching, copying, zooming in and out, saving, and so on. If you pass the mouse pointer on top of the buttons you will see short pop-up help messages. You also have access to these commands (and others) from the menu. It is not possible in this tutorial to explain all the functionality of Virtuoso Schematic so you are strongly encouraged to read the on-line user manuals (select "Help").

### **Integrated Circuit Design CAD Tool Information**

e. You will now generate a schematic which will be used to generate and plot I-V curves. Click 'I' in the schematic editor window to bring up the "Component Browser" and "Add Instance" windows as shown below. Select "NCSU\_Analog\_Parts → N\_Transistors → nmos4."

Component Brows 🗕 🗆 🗙
Commands <u>H</u> elp <b>cādence</b>
Library NCSU_Analog_Parts Flatten Filter * (Go up 1 level) nbsim nbsim4 njfet nmes nmes4 nmos4 nmos4_hv nmos_hv npn
N_Transistors

## **Integrated Circuit Design CAD Tool Information**

**f.** These choices will automatically fill in the other pop-up window, called the "Add Instance" window (You could have also filled in this window directly).

Now move the mouse over the Virtuoso Schematic window, and you will see an 'outline' (or ghost) of the transistor. You can move, rotate, and/or flip this outline until the transistor is in the desired orientation; when you are satisfied that the transistor is oriented correctly, you can click on the left-mouse button to place the transistor in the schematic.

It is possible to place the transistors one at a time, but it is easier to place several transistors at one time as long as you know in advance the required number.

In this case, you need five transistors, so select 5 rows and 1 column in the "Add Instance" window as shown in the image on the next page.

It is a good idea to save your design from time to time in case the system crashes.

	Add I	nstance	X
Library	NCSU_Analog_Parts	Brow	vse
Cell	nmos4		
View	symbol		
Names			
🖌 Add Wir	o Stube at:		
	🔾 all terminals 🧕 n	egistered terminals only	
Array	Rows 5	Columns 1	
	🖹 Rotate 📄 🛛 🕼 Si	deways ) 🥞 Upside Dov	vn
			-
Model nar	ne	amiO6N	
Model Typ	)e	<ul> <li>svstem Q user</li> </ul>	
Multiplier		1	
Fingers		1	-
Width (grid	d units)	10	
Width		1.5u M	1
Width (min	iimum)	1.5u M	1
Length (gr	id units)	4	
Length		600n M	1
Length (mi	inimum)	600n M	1
Drain diffu	sion area	2.25e-12	
Source dif	fusion area	2.25e-12	
Drain diffu	sion perimeter	6u M	
Source dif	ffusion perimeter	6u M	
Drain diffu	sion res squares		
Source diffusion res squares			
Virtuoso-XL layout cell			
Drain diffusion length			
Source diffusion length			
Temp rise from ambient			
Estimated operating region			
Hide Cancel Defaults Help			

### **Integrated Circuit Design CAD Tool Information**

g. Now you can place the five transistors by clicking on the left mouse button for the first transistor and then moving the mouse vertically downward and clicking again. Do these five clicks now. If you make mistakes, you can always go to "Edit → Undo" and try again. You can press the ESC key on the keyboard to get out of the place instance mode, or you can keep placing other parts.

You can also move parts and delete parts. Please explore the different editing functions.

# **Integrated Circuit Design CAD Tool Information**

**h.** The schematic that you are building is shown below.



### **Integrated Circuit Design CAD Tool Information**

**i.** Now you need to add ports, wires, and the power supply. First, add ground by clicking 'I' again and then choosing "Supply-Nets" and then 'gnd' in the Component Browser window. Place one gnd below the five transistors as shown in the image on the previous page.

Component Brows _ 🗆 🗙
Commands <u>H</u> elp <b>cādence</b>
Library NCSU_Analog_Parts Flatten Filter *
(Go up 1 level) gnd gnda gndd oscport powerSupply vcc vcca vccd vdd vdd
Supply_Nets
12 HelpAction

	Add Instance	×
Library	NCSU_Analog_Parts	Browse
Cell	gnd	
View	symbol	
Names		
🗹 Add Wii	e Stubs at: Q all terminals	only
Array	Rows 1 Columns	1
	😫 Rotate 🔰 🕼 Sideways 🛛 🥞 Upsi	de Down
	Hide Cancel De	faults Help

**j.** Now add wires by typing 'w' in the schematic to connect all the transistor sources and transistor bodies to ground.

### **Integrated Circuit Design CAD Tool Information**

**k.** Now add six DC voltage sources, one for VDS and one for each VGS. The DC voltage sources are in the "Voltage\_Sources" directory with the name 'vdc.' Remember to save your design. More information about adding the six DC voltage sources are in the next step. The first one should be added with the windows shown below.

Component Brows _ 🗆 🗙
Commands <u>H</u> elp <b>cādence</b>
Library NCSU_Analog_Parts Flatten Filter *
(Go up 1 level) ccvs vcvs vdc vexp vpulse vpwl vpwlf vsin
Voltage_Sources
11 HelpAction

	Add	l Instance	X
Library	NCSU_Analog_Part	ts	Browse
Cell	vdc		
View	symbol		
Names			
Add Wire Stubs at:			
Array	Rows 1	L Columns	1
	🖹 Rotate 📄 🚺	Sideways 🛛 🚄 Ups	ide Down
AC magni	tude		
AC phase			
DC voltag	e	5 V	
Noise file	name		
Number of noise/freq pairs		0	
Temperature coefficient 1			
Temperature coefficient 2			
Nominal te	emperature		
	•	Hide Cancel De	efaults Help

- **I.** Now connect the DC voltage sources with wires to the transistors. As you place each vdc source (you can place them one after the other, no need to click on 'instance' in between), change the VGS power supplies to be 5 V, 4 V, 3 V, 2 V, and 1 V respectively, by inserting the appropriate value for the DC voltage property. The form on the previous page has 5 V inserted, for example, in the "DC voltage" field.
- **m.** You now need to add five more 'dummy' voltage sources (each with a value of 0 V) so that you can plot the current in each transistor (it seems from existing tutorials that there is a bug with the transistor models right now, and the transistor currents cannot be plotted directly). Add the five 'dummy' '0 V' sources in series with the drains, and a voltage source vdc of '5 V' for VDS. Press the ESC key to exit from the 'Add Instance' mode. In case you make a mistake, you can perform 'Edit  $\rightarrow$  Undo', or you can correct the mistake by some form of editing. For example, if you typed the wrong value for the DC voltage source for 'vdc', you can change the value later by first selecting the instance (click on it in the schematic) and then type 'q' (or "Edit  $\rightarrow$  Properties  $\rightarrow$  Objects"). Then, a pop-up window will appear where you can change the field, as shown in the image below.

Apply To only cur	rent 🔽 instance 🔽	
Show 🗌 syste	m 🗹 user 🗹 CDF	
Browse	Reset Instance Labels Display	
Property	Value	Display
Library Name	NCSU_Analog_Parts	off 🔽
Cell Name	vdc	off 🔽
View Name	symbol	off 🔽
Instance Name	¥10	off 🔽
lvslgnore	TRUE	off 🔽
AC magnitude	value	off 🗖
AC magnitude		off 🔽
DC voltage	5 ¥	off 🔽
Noise file name		off 🔽
Number of noise/freq pairs	0	off 🔽
Temperature coefficient 1		off 🔽
		off 🔽
Temperature coefficient 2		



- **o.** Now you need to check and save your design. In the Schematic window, select "File  $\rightarrow$  Check & Save." Make sure to read the log file reported in the CIW window to be sure that Check & Save completed with no errors. There should be no errors and no warnings. If there are any errors and/or any warnings, you will need to fix them in the schematic. After fixing any errors and/or warnings, you will need to Check & Save the schematic again. You will need to Check & Save the schematic each time you make changes to the schematic.
- **p.** Assuming there are no errors, and that the design passed Check & Save, you can now proceed to the simulation step.

# **Integrated Circuit Design CAD Tool Information**

**q.** In the Virtuoso Schematic window, click on "Launch  $\rightarrow$  ADE L" to launch the Virtuoso Analog Design Environment window as shown in the image below.

👫 Virtuoso® Analog Design Envi	ironment (1) - EENG653Tutorial IVcurves schem	natic 💶 🗙
Session Setup Analyses Variables C	Dutputs Simulation Results Tools Help	cādence
III 27		
Design Variables	Analyses	? 🗗 🗙 🚃
Name Value	Type Enable Arguments	ODC
		61
		×
	Outputs	7 8 × 👩
	Name/Signal/Expr   Value   Plot   Save   Save	Options
		<u>V</u> (*
	J	
>	Plot after simulation: Auto Plotting mode: Replace	e 🔽
mouse L:	M:	R:
2(5) Save State	Status: Ready   T=27 C   Simulator: spectre	State: tmpstate 📘

### **Integrated Circuit Design CAD Tool Information**

r. First you need to choose the simulator. In the Analog Design Environment window, select "Setup → Simulator/Directory/Host" and the window below will appear. This window is "Choosing Simulator/Directory/Host" window. Choose 'spectre' in the Simulator pull-down menu and then click OK.

🗖 Choosing Simulator/Directory/Host Virtuoso® Analog Desi 🗙		
Simulator	spectre	
Project Directory	afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta 🛄	
Host Mode	🖲 local 🔾 remote 🥥 distributed	
Host		
Remote Directory		
	OK Cancel Defaults Apply Help	

- S. Next you will choose model libraries. Click on the Virtuoso Analog Design Environment window and select "Setup → Model Libraries." Select the following paths in the "spectre0: Model Library Setup" window. These are the paths to the model for the NMOS device and the PMOS device:
  - i. /apps/vlsi/ncsu-cdk-
    - 1.6.0.beta/models/spectre/nom/ami06N.m
  - ii. /apps/vlsi/ncsu-cdk-
    - 1.6.0.beta/models/spectre/nom/ami06P.m
  - iii. Then click OK.



### **Integrated Circuit Design CAD Tool Information**

t. Now you will choose the type of simulation. Click on the Virtuoso Analog Design Environment window. Select "Analyses → Choose" and the window below will appear. This is the "Choosing Analyses" window. You are doing a DC sweep, so click on the 'dc' radio button, and then click on 'Component Parameter' check-box. Then click on the VDS component in the Schematic window and choose dc in the Select Component Parameter pop-up window and click 'OK'.

Choosin	ng Analyse	es Vir	tuoso® A	nalog Design E	X
Analysis	🔾 tran	🖲 dc	🔾 ac	🔾 noise	
	🔾 xf	🔾 sens	🔾 dcmatch	🔾 stb	
	🔾 pz	🔾 sp	🔾 envlp	🔾 pss	
	🔾 pac	🔾 pstb	🔾 pnoise	🔾 pxf	
	🔾 psp	🔾 qpss	🔾 qpac	🔾 qpnoise	
	🔾 dbxt	🔾 dbsb	🔾 hb	🔾 hbac	
	🔾 hbnoise				_
		DC Ana	alysis		
Save DC O	perating Poir	nt 📃			
Hysteresis	Sweep				
Sweep Va	riable	_			
🗌 Temper	rature	Co	mponent Nan	ne /V10	
🔲 Design	Variable	$\subset$	Select	Component	
🗹 Compo	nent Parame	ter Pai	rameter Name	e dc	
🔲 Model	Parameter				
					31
Sweep Ra	nge				
Start-S	top g	Start 0		Ston 🖪	
Center	-Span				
Sweep Ty	pe				
Automatic					
Add Specifi	ic Points 📃				
Enabled 🖌	1			Options	
	ОК	Cano	el Defaul	ts Apply Help	

### **Integrated Circuit Design CAD Tool Information**

	Select Comp	onent Parameter 🛛 🗙
type	srcType	"Source type"
dc	vdc	"DC voltage"
mag	acm	"AC magnitude"
phase	acp	"AC phase"
tc1	tc1	"Temperature coefficient
tc2	tc2	"Temperature coefficient
tnom	tnom	"Nominal temperature"
$\triangleleft$		
		OK Cancel Help

u. Then, back in the "Choosing Analyses" window, set Start to '0' and set Stop to '5'. Set the 'Sweep Type' to 'Automatic.' Setting the sweep type to automatic will do a dc sweep of VDS from 0 V to 5 V. Then click 'OK' in the "Choosing Analyses" window.

### **Integrated Circuit Design CAD Tool Information**

v. Click on the "Virtuoso Analog Design Environment" window. Select "Outputs → Save All" which will bring up the 'Save Options' form shown below. In this form, select 'allpub' for signals to save (the default). In general, you will want to save only a subset of signals so that you save computing resources, but this schematic is small enough that it is OK to save all the signals. Click "OK" in the 'Save Options" form.

	Save Options X
Select signals to output (save)	🗌 none 🔲 selected 🛄 lvlpub 🛄 lvl 🕑 allpub 🛄 all
Select power signals to output (pwr)	🗌 none 🔲 total 🛄 devices 🛄 subckts 🛄 all
Set level of subcircuit to output (nestIvI)	
Select device currents (currents)	🔄 selected 🔲 nonlinear 🛄 all
Set subcircuit probe level (subcktprobelvl)	
Select AC terminal currents (useprobes)	🗆 yes 🔲 no
Select AHDL variables (saveahdlvars)	selected all
Save model parameters info	⊻
Save elements info	⊻
Save output parameters info	⊻
Save primitives parameters info	⊻
Save subckt parameters info	⊻
Save asserts info	
Save extreme info	
Output Format	🔄 sst2 🔛 psf 🔄 psf with floats 🕑 psfxl
Use Fast Viewing Extensions	
	OK Cancel Defaults Apply Help

# **Integrated Circuit Design CAD Tool Information**

w. Now you are ready to simulate your schematic. In the "Virtuoso Analog Design Environment" window, click on "Simulation → Netlist → Create raw" to create the netlist.
#### **Integrated Circuit Design CAD Tool Information**

x. Now you are ready to run the simulation. Click on the "Virtuoso Analog Design Environment" window. Click on "Simulation → Run." The CIW reports a successful simulation, and the file below will appear. This file will appear in the case that there are no errors.

In case you have errors, you will need to go back and correct them. This process can be tricky. You may need to do to "Simulation  $\rightarrow$  Netlist" and "Simulation  $\rightarrow$  Run" each time you change the schematic.

Note: Each time you change the schematic, you will need to do a Check & Save.

# **Integrated Circuit Design CAD Tool Information**

Č /ho	me/afiten3/fac/mla	nzero/ca	dence/r	ncsu-cdk-1.6	.0.beta/ _	=)(×
<u>F</u> ile	<u>H</u> elp				c ā d e n	ce
Loadiı Loadiı Loadiı Loadiı	ig /apps/vlsi/Cadence ig /apps/vlsi/Cadence ng /apps/vlsi/Cadence ng /apps/vlsi/Cadence	/MMSIM101 /MMSIM101 /MMSIM101 /MMSIM101	/tools.l /tools.l /tools.l /tools.l	nx86/cmi/lib/ nx86/cmi/lib/ nx86/cmi/lib/ nx86/cmi/lib/	64bit/5.0/li) 64bit/5.0/li) 64bit/5.0/li) 64bit/5.0/li)	biı^ bpl bsj
Time : Time : Peak :	For NDB Parsing: CPU accumulated: CPU = 65 cesident memory used	= 65.989 m .989 ms, = 34.1 Mb;	ms, elap elapsed ytes.	sed = 128.782 = 128.782 ms.	ms.	l
Time : Time : Peak :	for Elaboration: CPU accumulated: CPU = 80 cesident memory used	= 14.998 n .987 ms, = 38.1 Mb;	ms, elap elapsed ytes.	sed = 23.0691 = 153.077 ms.	ms.	l
Time : Time : Peak :	for EDB Visiting: CPU accumulated: CPU = 81 cesident memory used	( = 999 us. 986 ms, = 38.3 Mb;	, elapse elapsed ytes.	d = 1.13297 m = 154.315 ms.	3.	l
Circu:	it inventory: nodes 11 bsim3v3 5 vsource 11					
Time : Time : Peak :	for parsing: CPU = 1 accumulated: CPU = 82 resident memory used	ms, elaps .986 ms, = 39 Mbyt	ed = 3.2 elapsed es.	2294 ms. = 157.633 ms.		
Enter:	ing remote command mo	de using 1	MPSC ser	vice (spectre	, ipi, v0.0,	3)
Warnı) Wi	ng from spectre. ARNING (SPECTRE-16707	): Only t	ran supp	orts psfxl fo	rmat, result	0:
DC An +***** Import	alysis `dc': V10:dc = ************************************	++++++++++ (0 ∇ -> ! +++++++++++	**** 5 ♥) ****			=
න් ව tr	ostol(V) = 1 uV ostol(I) = 1 pA emp = 27 C					
ti ti	nom = 27 C empeffects = all mindc = 1 mS					
đi di	:: dc = 200 m∀ :: dc = 300 m∀ :: dc = 400 m₩	(4 %), (6 %), (0 %)	step = 1 step = 1	00 m∀ 00 m∀ 00 mV	(2 %) (2 %)	
di di	s: dc = 400 m♥ s: dc = 500 m♥ s: dc = 600 m♥	(10 %), (12 %),	step = 1 step = 1 step = 1	00 mV 00 mV 00 mV	(2 %) (2 %) (2 %)	
dı dı dı	o: dc = 700 m∀ o: dc = 800 m∀ o: dc = 900 m∀	(14 %), : (16 %), : (18 %), :	step = 1 step = 1 step = 1	UU m∀ 00 m∀ 00 m∀	(2 %) (2 %) (2 %)	
di di	c: dc = 1 V c: dc = 1.1 V	(20 %), (22 %),	step = 1 step = 1	00 m∀ 00 m∀	(2 %) (2 %)	
di di di	s: dc = 1.2 ∀ s: dc = 1.3 ∀ s: dc = 1.4 ∀	(24 %), (26 %), (28 %),	step = 1 step = 1 step = 1	00 m¥ 00 m¥	(2 %) (2 %) (2 %)	
di di	o: dc = 1.5 ♥ c: dc = 1.6 ♥	(30 %), : (32 %), :	step = 1 step = 1	00 m∀ 00 m∀ 00	(2 %) (2 %)	
di di	p: dc = 1.7 V p: dc = 1.8 V p: dc = 1.9 V	(34 ≉), : (36 %), : (38 %), :	step = 1 step = 1 step = 1	00 m¥ 00 m¥	(2 %) (2 %) (2 %)	
di di	b: dc = 2 ♥ b: dc = 2.1 ♥	(40 %), (42 %),	step = 1 step = 1	00 m∀ 00 m∀	(2 %) (2 %)	
dı dı dı	o: dc = 2.2 ¥ o: dc = 2.3 ¥ o: dc = 2.4 ¥	(44 %), (46 %), (48 %),	step = 1 step = 1 step = 1	UU m∀ 00 m∀ 00 m∀	(2 %) (2 %) (2 %)	
di di	o: dc = 2.5 ♥ c: dc = 2.6 ♥	(50 %), (52 %),	step = 1 step = 1	00 m¥ 00 m¥	(2 %) (2 %)	
dı dı dı	o: de = 2.7 ♥ o: de = 2.8 ♥ o: de = 2.9 ♥	(54 %), (56 %), (58 %),	step = 1 step = 1 step = 1	UU m∀ 00 m∀ 00 m∀	(2 %) (2 %) (2 %)	
di di	c: dc = 3 V c: dc = 3.1 V	(60 %), (62 %),	step = 1 step = 1	00 m¥ 00 m¥	(2 %) (2 %)	
di di di	5: dc = 3.2 ♥ 5: dc = 3.3 ♥ 5: dc = 3.4 ♥	(64 %), : (66 %), : (68 %)	step = 1 step = 1	00 m∀ 00 m∀ 00 mV	(2 %) (2 %) (2 %)	
di di	5: dc = 3.5 ¥ 5: dc = 3.6 ¥	(70 %), (72 %),	step = 1 step = 1 step = 1	00 mV 00 mV	(2 %) (2 %) (2 %)	
di di	s: dc = 3.7 ♥ s: dc = 3.8 ♥ s: dc = 2.0 ♥	(74 %), (76 %), (70 %)	step = 1 step = 1	00 m¥ 00 m¥ 00 m¥	(2 %) (2 %) (2 %)	
di di	5: dc = 3.9 V 5: dc = 4 V 5: dc = 4.1 V	(70 ≼), (80 %), (82 %),	step = 1 step = 1 step = 1	00 m¥ 00 m¥	(2 %) (2 %) (2 %)	
di di	c: dc = 4.2 ♥ c: dc = 4.3 ♥	(84 %), (86 %),	step = 1 step = 1	00 m∀ 00 m∀	(2 %) (2 %)	
di di	s: ac = 4.4 ∀ s: dc = 4.5 ∀ s: dc = 4.6 ∀	(88 %), : (90 %), : (92 %), :	step = 1 step = 1 step = 1	00 m¥ 00 m¥	(2 %) (2 %) (2 %)	
di di	c: dc = 4.7 ♥ c: dc = 4.8 ♥	(94 %), (96 %),	step = 1 step = 1	00 m∀ 00 m∀ 00 m∀	(2 %) (2 %)	
dı dı Total	<pre> ac = 4.9 ♥ &gt;: dc = 5 ♥ time required for dc</pre>	(30 ≼), (100 %), analysis	step = 1 `dc': C	00 mV 00 mV PU = 8.999 ms	(2 %) (2 %) , elapsed = 1	10
Time : Peak :	accumulated: CPU = 91 resident memory used	.985 ms, = 39.8 Mb	elapsed ytes.	= 1.44215 s.	-	
modell elemen	arameter: writing mo nt: writing instance	del param parameter	eter val values	ues to rawfil to rawfile.	e.	
outpu desig primi subck	:Parameter: writing o :ParamVals: writing n sives: writing primit ts: writing subcircui	utput par etlist pa ives to r ts to raw	ameter v rameters awfile. file.	alues to rawf to rawfile.	ile.	
< 7 Ho	InAction					
, ne	priotion					

# **Integrated Circuit Design CAD Tool Information**

Virtuoso® 6.1.5-64b - Log: /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/CDS.24april2012.log
File Tools Options Help cadence
wire drawing -> bounding box: (-1.75,0.94) (-1.12,0.94)
<pre>wire drawing -&gt; bounding box: (-1.50.04) (-1.12.0.94) Wiff (GSU-117) Extracting 'Theuress submatic' Warning: Pin 'T' on instance 'N'': floating input/output Warning: Pin 'T' on instance 'N'': floating input/output Warning: Pin 'T' on instance 'N': floating input/output Warning: Pin 'TUS' on instance 'N': floating input/output Warning: Pin 'TUS' on instance 'N': floating input/output. Warning: Pin 'TUS' on instance''''''''''''''''''''''''''''''''''''</pre>
Copying Spectre source file 'spectre.im' Copying Spectre command file 'spectre.im' Begin Incremental Netlisting Apr 25 13:06:02 2012 End netlisting Apr 25 13:06:02 2012
Number of components: 16 Elapsed time: 2.0s (8.00/s) Errors: 0 Warnings: 0 successful. compose simulator input file Loading devCheck.cxt successful. Pelete psf data in /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/IVcurves/spectre/schematic/psf. generate netList
<pre>begin incremental wetlisting Apr 25 13:05:22 2012 End netlisting Apr 25 13:06:22 2012 The netlist is up to date. Time taken to compare the design with netlist: 0.0ssuccessful. compose simulator input filesuccessful. Loading paraplot.ext simulate INFO (ADE-SOT1): Simulation completed successfully. reading simulation datsuccessfulsucce</pre>
Image: Non-Select component         M:         R

#### **Integrated Circuit Design CAD Tool Information**

y. If there are no errors in the simulation, you are now able to plot the simulation results. Click on the "Virtuoso Analog Design Environment" window. Select "Results → Direct Plot → DC" which will pop-up your schematic window. Now you have to click on the signals that you want to see. Since this is a DC-sweep, you want to see the drain currents into the five transistors. In order to see these, you have to click on the small red square at "+" terminal of each of the dummy power supplies in series with each drain. Make sure you click on the red square (the pin) which means current, versus any other part which means net, or voltage. Click on all five (5) power supplies. If you are clicking correctly on the pins, a circle (in color) should appear around each chosen pin as shown in the figure below. Note that the circle around each pin will be a different color.

# **Integrated Circuit Design CAD Tool Information**



# **Integrated Circuit Design CAD Tool Information**

**z.** Now you can press on the 'ESC' key to finish choosing the signals. You should finally get the desired simulation results, five IV-curves.



# **Integrated Circuit Design CAD Tool Information**

aa. It is a good idea to save the state of your simulation before you exit the simulation window. You can save the state of your simulation by clicking on the "Virtuoso Analog Design Environment" window. Then click on "Session → Save state" which will bring up the "Saving State" window shown in the image below. This will be helpful if you want to redo any of the simulations without having to re-enter everything from scratch.

	Saving State	Virtuo	so® Analog Desig	n Environment	: (1) X
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Directo	ory Options				
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	Save As	state1			
E	Existing States	state-iv	curves		
- Cellvie	w Options				
1	_ibrary	EENG653T	utorial 👻		
0	Cell	IVcurves	Brows	e	
	State	spectre_s	tatel -		
~ Descri	ption				
None	<u>.</u>				( III )>
$\triangleleft$			11111		
⊂What t	o Save				
				Select All Clea	r All
⊻	Analyses		🗹 Variables	🗹 Outputs	
⊻	Model Setup		🗹 Simulation Files	🗹 Environment O	ptions
<b>V</b>	Simulator Options		🗹 Convergence Setup	🗹 Waveform Setu	lb
<b>V</b>	Graphical Stimuli		🗹 Conditions Setup	🗹 Results Display	y Setup
<b>V</b>	Device Checking :	Setup	🗹 RelXpert Setup	🗹 Cosimulation C	Options
<ul> <li>✓</li> <li>✓</li> </ul>	Turbo and Parasiti Parameterization S	c Reduction etup	✓ MDL Control Setup	🗹 Distributed Pro	cessing
				Cancel A	Apply Help

**bb.** You have now saved the state of your simulation of five IV-curves.

# **Integrated Circuit Design CAD Tool Information**

# 22. nFET: Parametric Simulation of I-V Curves (nFET)

**a.** You will now learn another way to perform the same type of simulation as in the previous section. The idea behind this section is to show another choice about how to achieve the same result within the Cadence Design tool framework. To review, in the previous section, you used multiple devices (five devices) to obtain the five IV curves. You are now going to achieve the same results (and expand to ten IV curves) by using a single transistor for which you will change the voltage VGS.

Close the Analog Environment and the IV curves schematic, now you will start another schematic that you will call "IVparam."

Instead of starting with a new schematic window, you will start from your IVcurves schematic that you made in the previous section.

Open the Library Manager as shown in the figure below. Click on the Library Manager window, and in the window, select the IVcurve cellView and choose "Copy."

# **Integrated Circuit Design CAD Tool Information**

Library Manager:	Directoryro/cadence/	ncsu-cdk-1.6.0.beta	
<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>D</u> esign Manager <u>H</u> elp			cādenc
Show Categories Show Files Library	Cell	View	
EENG653Tutorial	 IVcurves		
EENG653 EENG653 NCSU_Analog_Parts NCSU_Digital_Parts NCSU_TechLib_ami06 NCSU_TechLib_tami16 NCSU_TechLib_tsmc02 NCSU_TechLib_tsmc02 NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03d NCSU_TechLib_tsmc04_4M2P avTech basic cdeDeffechLib	IVcurves IVparam	View <u>  Lock</u> schematic	Size
Messages Log file is "/home/afiten3/fac/mlanzero/ca Loading NCSU Library Manager customiz Beginning simple copy to library "EENG65 Processing files to be copied	dence/ncsu-cdk-1.6.0.beta/libMar ationsdone. 53Tutorial".	nager.log".	
	IIII		

# **Integrated Circuit Design CAD Tool Information**

**b.** The "Copy Cell" window will appear as shown in the image below. Complete the "Copy Cell" window as shown with the name of the new cell as "IVparam."

		Copy Cell	×
From-			h
Library	EENG653Tutorial		
Cell	IVcurves		
_То			5
Library	EENG653Tutorial		
Cell	IVparam	]	
Options			ĥ
Copy	y Hierarchical		
×	Skip Libraries	NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03d NCSU TechLib tsmc04 4M2P avTech	
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🗹 Copy	/ All Views		
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🖌 🖌 Re	e-reference customv	/iaDefs	
🖉 Cł	neck existence in te	chnology database	
🗌 Add	To Category	Cells *	J
ОК	Apply	Cancel	_

## **Integrated Circuit Design CAD Tool Information**

c. After copying to the new cell "IVparam," click on the "IVparam" cell and then double-click on the schematic view of this cell. A schematic should appear which is identical to the "IVcurves" schematic that you made in the previous section. You are now going to delete the bottom four transistors and their connections, as well as the bottom four VGS and dummy power supplies. You may use "Edit → Delete," or clicking and using the mouse button to select regions of the schematic to delete, and then clicking the delete button. You may also click 'd' to delete.

Now you will change the value of the VGS power supply to "parameter" as shown in the figure below. Note that the value "parameter" will be a variable that you will set later in this section. For now, change the value to the word "parameter."

Finally, move the symbol for 'gnd' upwards in the schematic and reconnect it to the rest of the schematic, as shown in the image below.

Your final schematic should look like the image below.

# **Integrated Circuit Design CAD Tool Information**



# **Integrated Circuit Design CAD Tool Information**

**d.** Remember to "Check & Save" your schematic. Look in the CIW to make sure that your schematic checks & saves without any errors.

C Virtuoso® 6.1.5-64b - Log: /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/CDS.1May2012.log	_ 🗆 🗙
File <u>T</u> ools <u>O</u> ptions <u>H</u> elp	cādence
wire drawing -> net: "gnd!" bounding box: (-1.50,-0.50) (-1.50,0.94)	
vdc (instance "VO", library "NCSU_Analog_Parts")	
Loading Layers.cxt Loading cdf.cxt	
INFO (SCH-1170): Extracting "IVparam schematic" Warning: Solder dot on cross over at ( -0.2500, 0.9375 )	
INFO (SCH-1172): There were 0 errors and 1 warning found in "EENG653Tutorial IVparam schematic".	
Getting schematic propert baggetting schematic propert baginru (SCH-1181): "ELMGESJUtorial lyparam schematic" saved.	
wire drawing -> net: "gnd!" bounding box: (-0.25,0.94) (1.69,0.94)	
wire drawing -> net: "gnd!" bounding box: (-0.25,0.94) (1.69,0.94)	
INFO (SCH-1170): Extracting "IVparam schematic"	
INFO (SCH-1426): Schematic check completed with no errors. Getting schematic proper bagdetting schematic propert bagdNFO (SCH-1181): "EEN0653Tutorial IVparam schematic" saved.	
Loading avv. cxt	
Immouse L: M:	R:
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# **Integrated Circuit Design CAD Tool Information**

 e. Now Click on the "IVparam" schematic and select "Launch → ADE L" to bring up the Analog Design Environment window as shown below.

👫 Virtuo	oso®	Analog D	esign En	vironm	ent (1) -	EENG65	i 3Tuto	rial IVparam	schematic 🗕	.ox
Session	Setup	Analyses	Variables	Outputs	Simulation	Results	Tools	Help	c ā d e	ence
IIII 27	1									
Design Va	ariables			An	alyses		_		?5	×
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mouse L:				_	M:					R:
2(3) DC					Status: Read	y   T=27	C   Si	mulator: spectre	State: state-ivc	urves 📘

# **Integrated Circuit Design CAD Tool Information**

f. In the Analog Design Environment window, select "Setup → Simulator/Directory/Host" and choose Spectre as your simulator. Select "OK."

🗆 Choosing Si	mulator/Directory/Host Virtuoso® Analog Desi 🗙
Simulator	spectre
Project Directory	afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta
Host Mode	💿 local 🔾 remote 🥥 distributed
Host	
Remote Directory	
	OK Cancel Defaults Apply Help

#### **Integrated Circuit Design CAD Tool Information**

g. Now you will load the state that you saved in the previous session. In the Analog Design Environment window, select "Session → Load State" which brings up the "Loading State" window shown below. Select "IVcurves" as your cell and select the state name that you saved in the previous section as shown.

Loading Sta	ite Virtua	oso® Analog De	sign Environment	(1) X
Load State Option	۲	) Directory 🔾 Cellvia	ew.	
- Directory Options				
State Load Directory	w/ artist	- 0+3+20		Browse
	CENCRE2T			
Library	EENG0551	utonal		
Cell	Ivcurves			
Simulator	spectre			
State Name	state-1vo	urves		Delete State
Cellview Options				
Library	EENG653T	utorial	•	
Cell	IVparam	Simul	ator	
State		• Bi	rowse Delete St	ate
- Description				
None		IIII		
What to Load				
			Select All Clear	AII
🗹 Analyses		🗹 Variables	🗹 Outputs	
🗹 Model Setup		✓ Simulation Files	🗹 Environment Op	otions
Simulator Option	s	✓ Convergence Set	up 🗹 Waveform Setuj	0
Graphical Stimul		Conditions Setup	🔲 Results Display	Setup
Device Checking	g Setup Wa Bashuati	RelXpert Setup	Cosimulation O	ptions
Iurbo and Paras     Parameterization	Sotup	MDL Control Setu	ip 🔄 Distributed Proc	cessing
	Setup		OK Cancel A	nnly Help

#### **Integrated Circuit Design CAD Tool Information**

h. Now you will edit the design variable "parameter" that you set in your "IVcurves" schematic. Click first on the Virtuoso Analog Design Environment window. Then click on "Variables → Edit" which will bring up the "Editing Design Variables" window shown below. In this window, set "Name" to "parameter" and "Value" to "5." Click on "Add" that will move the word "parameter" to the right-hand side of the form under the "Name" column and will move the value '5' to the right-hand side under the "Value" column.

🗖 Editing D	esign Variables Virtuoso	Analog Desig	jn Environmen 🗙
	Selected Variable	Design Variables	
		_ Name	Value
Name	parameter	1 parameter	5
Value (Expr)	5		
Add Dele Next Cle	ar Find		
Cellview Variab	oles Copy From Copy To		
	OK Cancel Appl	y) Apply & Run 3	Simulation Help

# **Integrated Circuit Design CAD Tool Information**

 Now you can netlist your "IVcurves" schematic. Click on the Virtuoso Analog Design Environment window. Select "Simulation →Netlist → Create Raw" which will netlist your schematic as shown in the image below.

C /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/ _ 🗆 🗙
Eile Help cādence
<pre>// Generated for: spectre // Generated on: May 1 12:48:18 2012 // Design library name: EEN6653Tutorial // Design view name: schematic simulator lang=spectre global 0 parameters parameter=5 include "/apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m" include "/apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m" // Library name: EEN6653Tutorial // Cell name: NPParam // View name: schematic NO (net11 net12 0 0) am106N w=1.5u 1=600n as=2.25e-12 ad=2.25e-12 ps=6</pre>
6

# **Integrated Circuit Design CAD Tool Information**

**j.** Inspect the CIW to make sure that your netlist was created OK.

C Virtuoso® 6.1.5-64b - Log: /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/CDS.1May2012.log	X
File <u>T</u> ools <u>O</u> ptions <u>H</u> elp	cādence
<pre>*TNF0* (icLic-25) License Analog_Design_Environment_XL ("95210") was used to run ADE L. Loading spectrei.ext Loading relXpert.ext Loading devCheck.ext generate netlist Loading spectreinl.ext Loading sectore.nct Initializing the control file using cp: cp /apps/vlsi/Cadence/ID615/tools.lnx86/dfII/etc/si/control.spectre /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/IVparam/spectre/sc Copying Spectre source file 'spectre.inp' Copying Spectre command file 'spectre.inp' Begin Incremental Netlisting May 1 12:48:18 2012 Fod netlisting May 1 12:48:18 2012</pre>	∧
<pre>Ind netlsting May 1 12:49:18 2012 Netlisting Statistics:             Number of components: 4             Elapsed time: 0.0s Errors: 0 Warnings: 0            successful. compose simulator input file            successful. Loading paraplot.ext Loading bariefle.rt </pre>	
Loading Msglandler.cxt Loading UltraSim.cxt Loading AMSOSS.cxt Loading AMS.cxt	=
Delete psf data in /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/IVparam/spectre/schematic/psf. Writing simulator output to file "/home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/IVparam/spectre/schematic/netlist/paraplot-sim-out". 5 parametric simulations remaining. Setting parameter = 1 Begin Incremental Netlisting May 1 12:49:11 2012 End netlisting May 1 12:49:11 2012	
The netlist is up to date. Time taken to compare the design with netlist: 0.0s The 2021 Simulation completed concentrations.	
mouse L: M:	R:
1 Click a property to edit.	

#### **Integrated Circuit Design CAD Tool Information**

k. Now you will set up the parametric simulation. Click on the Virtuoso Analog Design Environment window. In this window, select "Tools → Parametric Analysis," and the "Parametric Analysis" window will appear as shown below. In this window, set "Variable" to 'parameter', "Value" to '5', "From" to '1', "To" to '5', and "Total Steps" to '10'. The value of '10' will give you 10 IV-curves with one parametric simulation (To duplicate the results of the previous section, set "Total Steps" to '5'). Here, 10 is suggested so you can see the ease with which multiple simulations can be performed.

Parametric Analysis - spectre(0): EENG653Tutorial IVparam schematic						
Eile <u>A</u> nalysis <u>H</u> elp	cādence					
■ Parametric Simulation Completed.						
🖻 🔚 😓 🛹 🛪 💿 📀 📝 🎹 🚽 Run Mode: Sweeps & Ranges 🔽 🕟 🙆 💷						
Variable   Value   Sweep?   Range Type   From   To   Step Mode   Total Steps   Inclusion List   Ex	clusion List					
parameter 5 🖌 From/To 1 5 Auto 10						
100%						
successiui.	,					
Info: Parametric Simulation Completed						
7 HelpAction						

## **Integrated Circuit Design CAD Tool Information**

 Now you will perform the parametric simulation. Click on the "Parametric Analysis" window. Select "Analysis → Start All." The window will appear as shown in the image below.

Parametric Analysis - spectre(0): EENG653Tutorial IVparam schematic						
Eile Analysis Help	dence					
■ Parametric Simulation Completed.						
🖻 🔲 🖳 🚛 🗶 🕥 🖓 🎹 🚽 Run Mode: Sweeps & Ranges 🔽 🙆 🍈 💷						
Variable Value Sween? Range Tune From To Sten Mode Total Stars Inclusion List Exclusion List						
parameter 5 S From/To 1 5 Auto 10						
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Info: Persmetric Simulation Completed	Ē					

# **Integrated Circuit Design CAD Tool Information**

**m.** The Virtuoso Analog Design Environment will look like the image below.

📱 Virtuo	so® /	Analog D	esign En	vironn	nent (1)	- EENC	653	Tutor	ial IVpara	m sch	ematic 🗕	
Session	Setup	Analyses	Variables	Outputs	: Simulatio	in Resu	lts T	ools	Help		cāder	nce
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Design Va	riables			A	nalyses						? 🖥 X	
_ Na	ıme	L V	alue	1 d	Type   En C 🛛 🗸	able 0 5	i Auto	matic (	Arguments Start-Stop /V	10		ODC
<u>1</u> paramet	er	5		11								49
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> Results	inero	)/cadence/r	nosu-odk-1.	6.I Plo	t after simul	ation: 6	uto		Plotting mo	ode: Repl	ace 🔽	
immouse L:					1	VI:		- 1				R:
2(3) Stop					Status: Re	ady   T:	=27 (	C   Sir	nulator: spec	tre   Sta	te: state-ivcur	ves

# **Integrated Circuit Design CAD Tool Information**

**n.** Look at the CIW to make sure that the parametric simulation completed successfully, as shown in the image below.

C Virtuoso® 6.1.5-64b - Log: /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/CDS.1May2012.log	_ 🗆 🗙
File Tools Options Help	cādence
Writing simulator output to file "/home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/IVparam/spectre/schematic/netlist/paraplot-sim-out". 5 parametric simulations remaining. Setting parametre = 1 Begin Incremental Netlisting May 1 12:49:11 2012 End netlisting May 1 12:49:11 2012	
The netlist is up to date. Time taken to compare the design with netlist: 0.0s INFO (ADE-3071): Simulation completed successfully. INFO (ADE-3071): Simulation completed successfully. INFO (ADE-3071): Simulation completed successfully. INFO (ADE-3071): Simulation completed successfully. INFO (ADE-3071): Simulation completed successfully.	
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Immuse L:         M:           1         >	R:

#### **Integrated Circuit Design CAD Tool Information**

o. After the parametric simulation completes successfully, you are ready to look at the results of your simulation (the 10 IVcurves). Click on the "Virtuoso Analog Design Environment" window and select "Results → Direct Plot → DC." Then click on the terminal of the dummy supply in the drain of the transistor. After clicking the terminal, the terminal will then be surrounded by a circle, as shown in the image below (where the circle is red).



#### **Integrated Circuit Design CAD Tool Information**

p. Now click the "ESC" key. You will see a family of 10 IVcurves displayed in the "Virtuoso Visualization & Analysis XL" window as shown below. Count the number of IV curves; the figure below shows '10' IV curves.



**q.** You have now completed the parametric simulation tutorial.

# **Integrated Circuit Design CAD Tool Information**

# 23. Inverter: Generating a Voltage Transfer Curve (VTC) of an Inverter

**a.** In this tutorial, you will generate a voltage transfer curve (VTC) of an inverter. Open the Library Manager and select the EENG653 library that you created previously. Select the inverter schematic and open it with the schematic editor. The select the inv\_test schematic and open it with the schematic editor.

Library Manager:	Directoryro/cadence/ncsu-cdk-1.6.0.beta	
<u>File Edit V</u> iew <u>D</u> esign Manager <u>H</u> elp		cādence
☐ Show Categories ☐ Show Files	Cell View	)
EENG653	inverter schematic	
EENG653 EENG653Tutorial NCSU_Analog_Parts NCSU_Digital_Parts NCSU_TechLib_ami06 NCSU_TechLib_ami16 NCSU_TechLib_hp06 NCSU_TechLib_tsmc02 NCSU_TechLib_tsmc02	Inv_test Inv_test Inverter Inverter	A Lock d ic mlanzero@vlsifac01
NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03d NCSU_TechLib_tsmc04_4M2P avTech basic cdsDefTechLib megan		
Messages		
Deleting library "EENG653TutorialVTC". Deleted library 'EENG653TutorialVTC'.War but was defined in libFile '/h Delete of library "EENG653TutorialVTC" su Deletion of library done. Warning: The directory: '/home/afiten3/fac// but was defined in libFile '/h Warning: The directory: '/home/afiten3/fac// but was defined in libFile '/h	ning: The directory: '/home/afiten3/fac/mlanzero/cadence/ncs ome/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/cds.lil icceeded. mlanzero/cadence/ncsu-cdk-1.6.0.beta/EENG653TutorialVTC ome/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/cds.lil mlanzero/cadence/ncsu-cdk-1.6.0.beta/EENG653TutorialVTC ome/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/cds.lil	u-c o'ft 'da o'ft da o'ft

# **Integrated Circuit Design CAD Tool Information**

# **b.** Your inv\_test schematic will look like the image below.



# **Integrated Circuit Design CAD Tool Information**



# **c.** Your inverter schematic will look like the image below.

# **Integrated Circuit Design CAD Tool Information**

d. Click on the inv\_test schematic. Select "File → Check & Save" and check & save the schematic. If the schematic completes "Check & Save" successfully, the CIW will report that the "Schematic check completed with no errors," as shown in the image below. Make sure that your schematic completes "Check & Save successfully." Otherwise, you will need to fix your schematic and redo this step.

C Virtuoso® 6.1.5-64b - Log: /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/CDS.12May12.log	
File <u>T</u> ools <u>O</u> ptions <u>H</u> elp	cādence
Deleted library 'EENG653TutorialVTC'. INFO (SCH-1170): Extracting "inv_test schematic" INFO (SCH-1426): Schematic check completed with no errors. Getting schematic propert bagGetting schematic propert bagINFO (SCH-1181): "EENG653 inv_test schematic" saved. generate netlist Begin Incremental Netlisting May 12 14:22:35 2012 End netlisting May 12 14:22:35 2012	
Netlisting Statistics: Number of components: 4	
Elapsed time: 0.0s Errors: 0 Warnings: 0 successful. compose simulator input file successful. Belete psf data in /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/inv_test/spectre/schematic/psf. generate netlist Begin Incremental Netlisting May 12 14:22:44 2012 End netlisting May 12 14:22:44 2012	
The netlist is up to date. Time taken to compare the design with netlist: 0.0s successful. compose simulator input file successful. start simulator if needed	
_mmouse L: M: 1   >	R:

#### **Integrated Circuit Design CAD Tool Information**

 e. Click on the "EENG653 inv\_test schematic" and select "Launch → ADE L" to launch the Virtuoso Analog Design Environment. The Virtuoso Analog Design Environment window will appear as shown below. In the next steps, you will populate the 'Analyses' portion of this window.

	/irtuos	o® Anal	og Desig	n Envir	onment (4	I) - EEN	IG653	inv_test s	chematic	
Session	Setup	Analyses	Variables	Outputs	Simulation	Results	Tools	Help		cādence
III 27	]									
Design V	ariables			An	alyses					? 🗗 🗙 👘
Na	ıme	V	alue	1 1 dc	Type Enab	t 0 5 2	00m Lin	Arguments ear Step Size	Start-Stop /	VO
										*
				Ou	tputs		1 Maler		al David	? 🗗 🗙 💽
				Г	Name/Signa	.I/Expr	Valu	e  Plot  Sav	e  Save (	
							_			
> Result	s inro	/cadence/n	csu-cdk-1.6	.o. Plot	after simulati	on: Auto	<b></b>	Plotting mo	ode: Replace	
mouse L	:				M:					R:
19(43) S	ave Stat	te			State	is: Ready	T=27	C Simulat	tor: spectre	State: state1

# **Integrated Circuit Design CAD Tool Information**

 f. In the Virtuoso Analog Design Environment window, select "Setup
 → Simulator/Directory/Host." In the "Choosing Simulator/Directory/Host" window, select 'spectre' as the Simulator as shown in the image below.

🗆 Choosing Si	mulator/Directory/Host Virtuoso® Analog Desi 🗙
Simulator	spectre
Project Directory	afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta
Host Mode	🖲 local 🔾 remote 🔾 distributed
Host	
Remote Directory	
	OK Cancel Defaults Apply Help

#### **Integrated Circuit Design CAD Tool Information**

- g. Now you will set up the Model Libraries. In the Virtuoso Analog Design Environment window, select "Setup → Model Libraries." In the "Model Library Setup" window, point the Global Model Files to the models for the nmos4 and pmos4 in your schematic. The two paths that you need to add to your Global Model Files are shown in the image below and are:
  - i. /apps/vlsi/ncsu-cds-
    - 1.6.0.beta/models/spectre/nom/ami06N.m
  - ii. /apps/vlsi/ncsu-cds-1.6.0.beta/models/spectre/nom/ami06P.m

	spectre3: Model Library Setu	p	X
Global	Aodel File Model Files 'apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m 'apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m <click add="" file="" here="" model="" to=""></click>	Section	
,		OK Cancel Apply	Help

#### **Integrated Circuit Design CAD Tool Information**

h. Now click on the Virtuoso Analog Design Environment window and select "Analyses → Choose." In the "Choosing Analyses" window, select 'dc' because you will be doing a dc analysis. Select "Component Parameter," and enter the Component Name /V0 for the vpulse in the inv\_test schematic. Then click 'Select Component.'

🗆 Choosin	g Analys	es Vir	tuoso® A	nalog De	sign E 🗙
Analysis	🔾 tran	🖲 dc	🔾 ac	🔾 noise	
	🔾 xf	🔾 sens	🔾 dcmatch	🔾 stb	
	🔾 pz	🔾 sp	🔾 envlp	🔾 pss	
	🔾 pac	🔾 pstb	🔾 pnoise	🔾 pxf	
	🔾 psp	🔾 qpss	🔾 qpac	🔾 qpnoise	Э
	🔾 qpxf	🔾 qpsp	🔾 hb	🔾 hbac	
	🔾 hbnoise	9			
		DC An	alysis		
Save DC O Hysteresis S	perating Poi Sweep	nt 🗹			
Sweep Val	riable ature	Co	mponent Nar	ne ∕∀O	
Design	Variable	$\subset$	Select	t Component	
Compor	nent Parame Parameter	ter Pa	rameter Nami	e dc	
Sweep Rar	nge				
<ul> <li>Start-St</li> <li>Center-</li> </ul>	top •Span	Start 0	:	Stop 5	
Sweep Typ	)e	🖲 Ste	p Size	0.2	
Linear		🔾 Nur	nber of Steps	0.4	
Add Specifi	c Points 📃	1			
Enabled 🕑				Ор	tions
	01	Cano	el Defaul	lts Apply	Help

## **Integrated Circuit Design CAD Tool Information**

i. After clicking 'Select component,' the 'Select Component Parameter' window will appear as shown in the image below. Select the line 'dc vdc "DC voltage" ' with your cursor as shown in the image below, and then select 'OK."

If the 'Select Component Parameter' window does not appear, then go to your schematic and click on the vpulse instance which will bring up the 'Select Component Parameter' window as shown in the image below.

□ S	elect Comp	onent Parameter 🛛 🗙
type	srcType	"Source type"
dc	vdc	"DC voltage"
mag	acm	"AC magnitude"
phase	acp	"AC phase"
val0	v1	"Voltage 1"
val1	<b>v</b> 2	"Voltage 2"
period	per	"Period"
delay	td	"Delay time"
rise	tr	"Rise time"
fall	tf	"Fall time"
width	pw	"Pulse width"
tc1	tc1	"Temperature coefficient
tc2	tc2	"Temperature coefficient
tnom	tnom	"Nominal temperature"
1		
1		
1		
1		
1		
1		
<		
		OK Cancel Help

#### **Integrated Circuit Design CAD Tool Information**

**j.** Now return to the "Choosing Analyses" window. In this window the "Parameter Name" will now be set to 'dc.' Set 'Start' to '0' and 'Stop' to '5' as shown in the image below. Also select 'Sweep Type' to 'Linear' using the pull-down and set 'Step Size' to '0.2' as shown. Click 'Enabled' and select 'OK.'

🗖 Choosin	g Analys	es Vir	tuoso® A	nalog Design	EX
Analysis	🔾 tran	🖲 dc	🔾 ac	🔾 noise	
	🔾 xf	🔾 sens	🔾 dcmatch	🔾 stb	
	🔾 pz	🔾 sp	🔾 envlp	🔾 pss	
	🔾 pac	🔾 pstb	🔾 pnoise	🔾 pxf	
	🔾 psp	🔾 qpss	🔾 qpac	🔾 qpnoise	
	🔾 qpxf	🔾 qpsp	🔾 hb	🔾 hbac	
	🔾 hbnoise	e			
		DC An	alysis		
Save DC O Hysteresis S	perating Poi Sweep	nt 🗹			
Sweep Va	riable	Co	mponent Nam	ne /¥0	
🔲 Temper	ature	_	0-1	Common and	
📃 Design	Variable		Select	Component	
Compo Model	nent Parame Parameter	ter Pa	rameter Name	e dc	
Sweep Ra	nge				
<ul> <li>Start-S</li> <li>Center-</li> </ul>	top -Span	Start 0		Stop 5	
Sweep Ty	pe				
Linear		🖲 Ste	p Size	0.2	
		🔾 Nur	nber of Steps		
Add Specifi	c Points 🗌	1			
Enabled ⊻				Options	
	01	Cano	el Defaul	ts Apply H	elp

#### **Integrated Circuit Design CAD Tool Information**

k. Now click on the "Analog Design Environment" window. Select "Outputs → Save All." The "Save Options" window will appear as shown below. For 'Select signals to output (save),' select 'allpub.' For 'Select power signals to output (pwr),' select 'all.' Select the other options as shown, and then click 'OK.'

	Save Options X
Select signals to output (save)	🔄 none 🔲 selected 🛄 lvlpub 🛄 lvl 🕑 allpub 🛄 all
Select power signals to output (pwr)	🗌 none 🛄 total 🛄 devices 🛄 subckts ⊻ all
Set level of subcircuit to output (nestIvI)	
Select device currents (currents)	🔄 selected 🛄 nonlinear 🛄 all
Set subcircuit probe level (subcktprobelvl)	
Select AC terminal currents (useprobes)	🗌 yes 🔲 no
Select AHDL variables (saveahdlvars)	selected all
Save model parameters info	⊻
Save elements info	⊻
Save output parameters info	⊻
Save primitives parameters info	⊻
Save subckt parameters info	⊻
Save asserts info	
Save extreme info	
Output Format	🔄 sst2 🔛 psf 🛄 psf with floats 🗹 psf×l
Use Fast Viewing Extensions	
	OK Cancel Defaults Apply Help
# **Integrated Circuit Design CAD Tool Information**

 Now you can get ready for the simulation. Click on the Virtuoso Analog Design Environment window and select "Simulation → Netlist → Create Raw." The netlist will appear as shown in the image below.

(C) /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/inv_te	st/s_OX
<u>F</u> ile <u>H</u> elp	cādence
<pre>// Generated on: May 12 14:22:35 2012 // Design library name: EENG653 // Design cell name: inv_test // Design view name: schematic simulator lang=spectre global 0 vdd! include "/apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m" include "/apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m"</pre>	Â
<pre>// Library name: EENG653 // Cell name: inverter // View name: schematic subckt inverter GND VDD Vin Vout NO (Vout Vin GND GND) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u pd=6u m=1 region=sat PO (Vout Vin VDD VDD) ami06P w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u pd=6u m=1 region=sat ends inverter // End of subcircuit definition.</pre>	\ ≡ \
<pre>// Library name: EENG653 // Cell name: inv_test // View name: schematic IO (0 vdd! InputNet OutputNet) inverter VO (InputNet 0) vsource type=pulse val0=0 val1=5 period=2u rise=100n \ fall=100n width=1u V1 (vdd! 0) vsource type=dc dc=3 CO (OutputNet 0) capacitor c=1p m=1 simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=2' tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarr digits=5 cols=80 pivrel=1e-3 sensfile="/psf/sens.output" \ checklimitdest=psf dcOp dc write="spectre.dc" maxiters=150 maxsteps=10000 annotate=status dcOpInfo info what=oppoint where=rawfile dc dc dev=V0 param=dc start=0 stop=5 step=0.2 oppoint=rawfile maxiters= maxsteps=10000 annotate=status modelParameter info what=maters where=rawfile element info what=inst where=rawfile outputParameter info what=parameters where=rawfile primitives info what=primitives where=rawfile subckts info what=subckts where=rawfile save0ptions options save=allpub pwr=all</pre>	7 \ hs=5 \ =150 \
54	

# **Integrated Circuit Design CAD Tool Information**

**m.** Now click on the Virtuoso Analog Design Environment window and select "Simulation → Run." The simulation will run and appear as shown in the following two images.

/home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1,6,0,beta/inv_test/spectre/schematic/psf/spectre.out
Cadence (P) Virtuee (P) Exectre (P) Circuit Simulator
Version 10.1.1.218.isrl4 GAbit 5 Sep 2011 Copyright (c) 1989-2010 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, Virtuoso and Spectre are
Protected by U.S. Patents: 5,610, 047; 5,790, 436; 5,812,431; 5,859,785; 5,949,992; 5,987,238; 6,088,523; 6,101,323; 6,151,698; 6,181,754; 6,250,176; 6,278,064; 6,349,272; 6,374,309; 6,432,494; 6,504,485; 6,618,837; 6,636,839; 6,778,025; 6,632,356; 6,451,097; 6,926,626; 7,024,652; 7,035,782; 7,005,700; 7,143,021; 7,493,240; 7,571,401.
Includes RSA BSAFE(R) Cryptographic or Security Protocol Software from RSA Security, Inc.
User: alanzero Host: vlsifac11 HostII: 50815619 PID: 24948 Memory available 19.9984 0B physical: 25.2720 0B CPU Type: Intel(R) Xeon(R) CPU X5550 0 2.670Hz Processor PhysicalID Corell Prequency 0 0 1 2860.1 2 0 1 2660.1 3 0 8 2660.1 4 0 9 2660.1 5 0 10 2660.1
Simulating `input.ses' on vlsifac01 at 2:22:44 PM, Sat May 12, 2012 (process id: 24948). Environment variable: SPECTER DEFAULTS-E
<pre>/wmmatu line: /wpp3/vlsi/Cadence/MMSIH101/tools.lmx86/spectre/bin/64bit/spectre \ input scs +eschars +log _/psf/spectre.out +inter=mpsc \ +mpsession=spectre3_23422_13 - format psfxl -raw/psf \ +lqtimeout 900 -maxw 5 -maxn 5 spectre pid = 24348</pre>
Loading /apps/vlsi/Cadence/MMSIM101/tools.lrx86/cmi/lib/64bit/5.0/libinfineon_sh.so Loading /apps/vlsi/Cadence/MMSIM101/tools.lrx86/cmi/lib/64bit/5.0/libph1lips_bh.so Loading /apps/vlsi/Cadence/MMSIM101/tools.lrx86/cmi/lib/64bit/5.0/libstmodels_sh.so Loading /apps/vlsi/Cadence/MMSIM101/tools.lrx86/cmi/lib/64bit/5.0/libstmodels_sh.so
Time for NDB Parsing: CPU = 65,989 ms, elapsed = 109.553 ms. Time accumulated: CPU = 65,989 ms, elapsed = 109.553 ms. Peak resident memory used = 34.1 Mbytes.
Time for Elaboration: CPU = 15.997 ms, elapsed = 18.158 ms. Time accumulated: CPU = 81.986 ms, elapsed = 127.857 ms. Peak resident memory used = 38.2 Mbytes.
Time for EDB Visiting: CPU = 0 s, elapsed = 406.027 us. Time accumulated: CPU = 82.986 ms, elapsed = 128.394 ms. Peak resident memory used = 38.4 Mbytes.
Circuit inventory: nodes 3 bsisWa 2 copector 1 veource 2
Time for parsing: GPU = 2 ms, elapsed = 3.17502 ms. Time accumulated: CPU = 84,986 ms, elapsed = 131.676 ms. Peak resident memory used = 39.1 Mbytes.
Entering remote command mode using MPSC service (spectre, ipi, v0.0, spectre3_23422_19, ).
Warning from spectre. WARNING (SPECTRE-16707): Only tran supports psfxl format, result of other analyses will be in psfbin format.
<pre>transformation of the second sec</pre>
dcOpInfo: writing operating point information to rawfile.
$\label{eq:constraint} \begin{array}{l} & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & $
$\begin{array}{c} \text{temperiecs} = \text{all} \\ \text{gminde} = 1 \text{ pS} \\ \text{dc: dc} = 200 \text{ mV} & (4\%), \text{ step} = 200 \text{ mV} & (4\%) \\ \text{dc: dc} = 200 \text{ mV} & (4\%), \text{ step} = 200 \text{ mV} & (4\%) \\ \text{dc: dc} = 400 \text{ mV} & (12\%), \text{ step} = 200 \text{ mV} & (4\%) \\ \text{dc: dc} = 800 \text{ mV} & (15\%), \text{ step} = 200 \text{ mV} & (4\%) \\ \text{dc: dc} = 800 \text{ mV} & (15\%), \text{ step} = 200 \text{ mV} & (4\%) \\ \text{dc: dc} = 1.7 \text{ W} & (24\%), \text{ step} = 200 \text{ mV} & (4\%) \\ \text{dc: dc} = 1.2 \text{ W} & (24\%), \text{ step} = 200 \text{ mV} & (4\%) \\ \text{dc: dc} = 1.4 \text{ W} & (24\%), \text{ step} = 200 \text{ mV} & (4\%) \\ \end{array}$
55 HelpAction
and trade to a second se

# **Integrated Circuit Design CAD Tool Information**

**n.** This is the second half of the results of the simulation (see the image below).

( /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/inv_test/spectre/schematic/psf/spectr	e.out _ 🗆 🗙
Eile Help	cādence
Loading /apps/vlsi/Cadence/MMSIMI01/tools lnx86/cmi/lb/64bit/5 0/libaparam sh.so Loading /apps/vlsi/Cadence/MMSIM101/tools lnx86/cmi/lb/64bit/5.0/libstmodels_sh.so	<u>_</u>
Time for MDB Parsing: CPU = 65 980 ms, elapsed = 109.553 ms. Time accumulated: $CPU = 65.989$ ms, elapsed = 109.553 ms. Peek resident amency used = 34.1 Mbytes.	
Time for Elaboration: CPU = 15.997 ms, elapsed = 18 158 ms. Time accumulated: CPU = 81.986 ms, elapsed = 127.857 ms. Peak resident memory used = 38.2 Mbytes.	_
Time for EDB Visiting: CPU = 0 s, elapsed = 406.027 us. Time accumulated: CPU = 82.986 ms, elapsed = 120.394 ms. Peak resident memory used = 38.4 Mbytes.	- 1
Circuit inventory: nodes 3 bsináv3 2 cepseitor 1 vsource 2	
Time for parsing: CPU = 2 ms, elapsed = 3.17502 ms. Time accumulated: CPU = 84.996 ms, elapsed = 131.676 ms. Peak resident memory used = 39.1 Mbytes.	- 1
Entering remote command mode using MPSC service (spectre, ipi, v0.0, spectre3_23422_19, ).	
Warning from spectre. WARNING (SPECTRE-16707): Only tran supports psfxl format, result of other analyses will be in psfbin	format.
DC Analysis 'dcOp' Taportant parameter values: inhortant parameter values: inhort(V) = 1 uV abtol(V) = 1 uV inhort = 27 c tempeffects = all ourganide = 1 pS ourganide = 1 pS ourganide = 1 pS ourganide = 1 pS ourganide = 0 pS tempef = 0 pV = 0 pS set dc analysis for dc analysis dcOp' OPU = 2 ms, elapsed = 4.12297 ms. Time accumulated: CPU = 89.985 ms, elapsed = 33.513 ms.	÷
dcOpInfo: writing operating point information to rawfile.	
DC Analysis 'dc': V0.dc = $(0 \text{ V} \rightarrow 5 \text{ V})$ Important parameter values: relicit = 10 - 1 v mbricl(1) = 1 v temp = 27 c temp = 27 c temp = 27 c	
$ \begin{array}{c} \mbox{quark} quar$	
lateat time required for de analysis de : 620 = 3.999 ms, elapsed = 5.09662 ms. Time accumulated: CPU = 96.984 ms, elapsed = 363.96 ms. Peak resident memory used = 40.2 Mbytes.	
<pre>modelParameter: writing model parameter values to rawfile. element: writing instance parameter values to rawfile. outputParameter: writing output parameter values to rawfile. designParamVals: writing netlist parameters to rawfile. primatives: writing primatives to rawfile. subckts: writing subcircuits to rawfile.</pre>	
55 HelpAction	

#### **Integrated Circuit Design CAD Tool Information**

o. Now click on the Virtuoso Analog Design Environment window. You are going to generate a Voltage Transfer Curve for your schematic. Click on "Results → Annotate → DC Node Voltages." Then click on "Results → Direct Plot → DC." The "Virtuoso ® Visualization & Analysis XL" window will appear as shown below. It will be empty (blank).



# **Integrated Circuit Design CAD Tool Information**

p. In the Virtuoso Analog Design Environment window, select the nets for which you wish to display the voltages in the voltage tranfer curve. The two nets are the "InputNet" and the "OutputNet." Select these two nets by clicking on them, and the nets will become dashed lines as shown in the inv\_test schematic image shown below.



# **Integrated Circuit Design CAD Tool Information**

**q.** After clicking on the "InputNet" and "OutputNet," click the "ESC" key. The Voltage Transfer Curve will appear (that is, the output voltage as a function of the input voltage) in the Virtuoso Visualization & Analysis XL window as shown in the image below. In the image below, the VTC is indicated in red. The increasing input voltage is shown in pink. Note that these colors correspond to the colors of the dashed nets in the inv\_test schematic.



# **Integrated Circuit Design CAD Tool Information**

- r. Notice that the voltage transfer curve is not smooth; that is, there are points at the locations on the curve where the input voltage has taken a step; recall that you set the step size for this simulation to 0.2 (refer to the "Choosing Analyses" window in a previous step.
- **s.** Now you are going to generate a smooth Voltage Transfer Curve for your inv\_test schematic and inverter schematic. Return to the "Choosing Analyses" window and set the "Step Size" to 0.01 (that is, this is equivalent to 0.1 V) as shown in the image below. Click 'Apply' on the form.

🗖 Choosin	g Analys	es Vii	tuoso® A	nalog Desigi	n E 🗙
Analysis	<ul> <li>tran</li> <li>xf</li> <li>pz</li> <li>pac</li> <li>psp</li> <li>qpxf</li> <li>hbnoise</li> </ul>	<ul> <li>dc</li> <li>sens</li> <li>sp</li> <li>pstb</li> <li>qpss</li> <li>qpsp</li> </ul>	<ul> <li>ac</li> <li>dcmatch</li> <li>envlp</li> <li>pnoise</li> <li>qpac</li> <li>hb</li> </ul>	<ul> <li>noise</li> <li>stb</li> <li>pss</li> <li>pxf</li> <li>qpnoise</li> <li>hbac</li> </ul>	
Save DC O Hysteresis S Sweep Var Design	oerating Poi weep riable ature Variable	nt 🔽 Co	omponent Nar Selec	ne ∕⊽0 t Component	
Compor	hent Parame Parameter	ter Pa	rameter Nam	e dc	
<ul> <li>Start-St</li> <li>Center-</li> </ul>	op Span	Start 0		Stop 5	
Linear	De Pointe	● Ste ⊖ Nu	p Size mber of Steps	0.01	
Enabled 🕑		Can	cel Defau	Options Its Apply	3 Help

# **Integrated Circuit Design CAD Tool Information**

In the Virtuoso Analog Design Environment window, select
 "Simulation → Netlist → Raw." Then select "Simulation → Run."
 The simulation will look like the results shown in the image below.

(C) /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/inv_test/spectre/schematic/psf/spectre.out	
<u>F</u> ile <u>H</u> elp	cādence
*****	<u> </u>
DC Analysis `dcOp'	
<pre>Important parameter values: reltol = 1e-03 abstol(V) = 1 uV abstol(I) = 1 uV abstol(I) = 1 pA temp = 27 C tempeffects = all gmindc = 1 pS Convergence achieved in 12 iterations. Total time required for dc analysis `dcOp': CPU = 1 ms, elapsed = 5.99194 ms. Time accumulated: CPU = 204.968 ms, elapsed = 2.40676 ks (40m 6.8s). Peak resident memory used = 40.3 Mottes.</pre>	
dcOpInfo: writing operating point information to rawfile.	
*************************************	
Important parameter values: reltol = $1e-03$ abstol( $\forall$ ) = 1 uV abstol(1) = 1 pA temp = 27 C trom = 27 C	
gmindc = 1 pS	
$ \begin{array}{c} dc: dc = 130 \text{ mV} & (2.6 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 140 \text{ mV} & (2.8 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 150 \text{ mV} & (3 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 150 \text{ mV} & (3.2 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 170 \text{ mV} & (3.4 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 170 \text{ mV} & (3.4 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 190 \text{ mV} & (3.6 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 200 \text{ mV} & (3.8 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 200 \text{ mV} & (4.2 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 200 \text{ mV} & (4.2 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 200 \text{ mV} & (4.4 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 230 \text{ mV} & (4.4 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 230 \text{ mV} & (4.8 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 250 \text{ mV} & (4.8 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 250 \text{ mV} & (5 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 260 \text{ mV} & (5 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 260 \text{ mV} & (5 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 260 \text{ mV} & (5 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 260 \text{ mV} & (5 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 260 \text{ mV} & (5 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 260 \text{ mV} & (5 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 260 \text{ mV} & (5 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 260 \text{ mV} & (5 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 260 \text{ mV} & (5 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 260 \text{ mV} & (5 \$), \text{ step } = 10 \text{ mV} & (200 \$) \\ dc: dc = 260 \text{ mV} & (5 \$), \text{ step } 10 \text{ mV} & (200 \$) \\ dc: dc = 260 \text{ mV} & (5 \$), \text{ step } 10 \text{ mV} & (200 \$) \\ dc: dc = 260 \text{ mV} & (5 \$), \text{ step } 10 \text{ mV} & (200 \$) \\ dc: dc = 260 \text{ mV} & (5 \$$	

# **Integrated Circuit Design CAD Tool Information**

- **u.** Then select "Results  $\rightarrow$  Direct Plot  $\rightarrow$  DC."
- v. A blank "Virtuoso Visualization & Analysis XL" window will appear. In the inv\_test schematic window, select the "InputNet" and "OutputNet" which will become dashed lines. Then click the "ESC" key. Then the "Virtuoso Visualization & Analysis XL" window will appear with a smooth VTC as shown in the image below.



# **Integrated Circuit Design CAD Tool Information**

- w. Now you will investigate how the response of the Voltage Transfer Curve changes as you change the width of the devices. For example, change the width of the pfet in your inverter schematic to 3microns: w = 3um. Check and Save your inverter schematic and the inv\_test schematic.
- x. Now click on the Virtuoso Analog Design Environment window and select "Simulation → Netlist → Create Raw." Then select "Simulation → Run." Select "Results → Direct Plot → DC," then select "InputNet," "OutputNet," click "ESC." You will obtain an updated VTC in the Virtuoso Visualization & Analysis XL window as shown in the image below.



# **Integrated Circuit Design CAD Tool Information**

**y.** Now change the width of the pfet in your inverter schematic to 3\*1.5 microns: w = 4.5um. Check and Save your inverter schematic and the inv\_test schematic. Now click on the Virtuoso Analog Design Environment window and select "Simulation  $\rightarrow$  Netlist  $\rightarrow$  Create Raw." Then select "Simulation  $\rightarrow$  Run." Select "Results  $\rightarrow$  Direct Plot  $\rightarrow$  DC," then select "InputNet," "OutputNet," click "ESC." You will obtain an updated VTC in the Virtuoso Visualization & Analysis XL window as shown in the image below.



# **Integrated Circuit Design CAD Tool Information**

**z.** Now click on the VTC. It will become bold and dashed as shown in the image below.



#### **Integrated Circuit Design CAD Tool Information**

aa. Now right click with your mouse on the curve and select
"Table → New Window." A Virtuoso Visualization & Analysis XL
Table will appear with the values of the voltage on the InputNet and the values of the voltage on the OutputNet, where the voltage on the InputNet ranges from 0V to 5V as you specified in the simulation. The table looks like the image below.

N		Virtuoso (R)	visualization & Analysis XL Table	_ 🗆 🗙
<u>F</u> ile	e <u>V</u> iew <u>T</u> ools	<u>H</u> elp		cādence
Ŵ	OutputNet	$\mathbf{X}$		
	dc (V)	OutputNet (V)		<u> </u>
1	0.0	3.000		
_2	10.00E-3	3.000		
3	20.00E-3	3.000		
_4	30.00E-3	3.000		
_5	40.00E-3	3.000		
_6	50.00E-3	3.000		
	60.00E-3	3.000		
8	70.00E-3	3.000		
9	80.00E-3	3.000		
10	90.00E-3	3.000		
11	100.0E-3	3.000		
12	110.0E-3	3.000		
13	120.0E-3	3.000		
14	130.0E-3	3.000		
15	140.0E-3	3.000		
16	150.0E-3	3.000		
17	160.0E-3	3.000		
18	170.0E-3	3.000		
19	180.0E-3	3.000		
20	190.0E-3	3.000		
21	200.0E-3	3.000		
22	210.0E-3	3.000		
23	220.0E-3	3.000		
24	230.0E-3	3.000		
25	240.0E-3	3.000		
26	250.0E-3	3.000		
27	260.0E-3	3.000		
28	270.0E-3	3.000		
29	200.0E-3	3.000		
30	290.0E-3	3.000		
31	300.0E-3	3.000		
32	310.0E-3	3.000		
33	330.0E-3	3.000		
24	340.0E-3	3.000		
30	350.0E-3	3.000		
130	000.0E-0	0.000		
78				

# **Integrated Circuit Design CAD Tool Information**

**bb.** You can export this Table to a CSV file by clicking at the top banner of this window on "File → Save as CSV." The image below shows that this table is saved in the working directory with the name "VTC-table.csv."

( MR	Save	e As CSV	×
Look in: [	/home/afiten3/fac/mlanzero/cader	nce/ncsu-cdk-1.6.0.beta	<ul> <li></li></ul>
Computer mlanzero i ncsu-cdk-	Name EENG653 EENG653Tutorial inv_run1 inv_test inverter_run1_backup Vcurves IVcurves IVparam LVS megan	Size Type Folder Folder Folder Folder Folder Folder Folder Folder Folder Folder	Date Modified 9 Apr 20:48:44 1 May 22:48:02 13 Apr7:37:41 9 Apr 21:07:26 11 Apr4:59:58 25 Apr3:04:35 1 May 22:48:15 9 Apr 27:18:07 23 Mar3:50:28
File <u>n</u> ame: V Files of type: C	TC-table.csv (TC-table.csv)	Folder 7 KB csv File	12 May7:23:49 12 May7:23:49 Save ✓ Cancel

cc. You have now completed the voltage transfer curve (VTC) tutorial.

# **Integrated Circuit Design CAD Tool Information**

# 24. Inverter Chain: Creating an Inverter Chain

**a.** In this section, you will create a chain of 11 inverters. A chain of inverters is referred to as an *inverter chain*. The library 'EENG653' should still be in your library search path, as shown in the library manager below. Copy the 'inv\_test' cell to a new cell called 'invchain\_test' cell. Copy the 'inverter' cell to a new cell called 'invchain\_test' cell. Copy the 'inverter' cell to a new cell called 'invchain\_test' cell to inverter instantiated in the 'invchain\_test' cell to 'inv' from 'inverter.'

Library Manager	Directoryro/cadence/ncs	su-cdk-1.6.0.beta
<u>File E</u> dit <u>V</u> iew <u>D</u> esign Manager <u>H</u> elp		cādence
Show Categories Show Files Library EENG653 EENG653 EENG653Tutorial NCSU_Analog_Parts NCSU_Digital_Parts NCSU_TechLib_ami06 NCSU_TechLib_ami16 NCSU_TechLib_hp06 NCSU_TechLib_hp06 NCSU_TechLib_tsmc02 NCSU_TechLib_tsmc02d NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03d	Cell inv inv_test invchain_test inverter	View symbol View <u>Lock</u> extracted functional layout schematic mlanzero@vlsifac01 symbol mlanzero@vlsifac01
NCSU_TechLib_tsmc02d NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03d NCSU_TechLib_tsmc04_4M2P avTech basic cdsDefTechLib megan		
Messages Loading NCSU Library Manager customia Warning: The directory: '/home/afiten3/fac but was defined in libFile '/ Warning: The directory: '/home/afiten3/fac but was defined in libFile '/ Beginning simple copy to library "EENG6 Processing files to be copied Warning: The directory: '/home/afiten3/fac but was defined in libFile '/	ationsdone. c/mlanzero/cadence/ncsu-cdk-1.6.0.b 'home/afiten3/fac/mlanzero/cadence/r c/mlanzero/cadence/ncsu-cdk-1.6.0.b 'home/afiten3/fac/mlanzero/cadence/r 53". c/mlanzero/cadence/ncsu-cdk-1.6.0.b 'home/afiten3/fac/mlanzero/cadence/r	peta/EENG653TutorialVTC' do ncsu-cdk-1.6.0.beta/cds.lib' fo ncsu-cdk-1.6.0.beta/cds.lib' fo peta/EENG653TutorialVTC' do ncsu-cdk-1.6.0.beta/cds.lib' fo

# **Integrated Circuit Design CAD Tool Information**

**b.** Open the 'inv' symbol in the 'EENG653' library and edit it using the editing functions on the bar above the symbol (add green lines, a green circle, delete the green rectangle). You may edit the 'inv' symbol to create an inverter symbol that is similar to the one you are studying in this course.

We need this symbol in order to create a hierarchical schematic at the logic (gate) level of an inverter chain. We create a hierarchical schematic using symbols of lower-level schematics (in this case, we create a hierarchical schematic of an inverter chain using the symbol of an inverter).



# **Integrated Circuit Design CAD Tool Information**

**c.** The schematic of the 'inv' is shown in the image below. Note that this schematic shows a pfet with a width (4.5 um) that is three times as large as the width of the nfet (1.5 um).



#### **Integrated Circuit Design CAD Tool Information**

d. We now create a hierarchical schematic that uses the 'inv' symbol that you created. Go to the library manager and open the cell named 'invchain\_test'. Edit 'invchain\_test' by moving the load capacitor to the right and inserting 10 additional inverters, to create a chain of 11 total inverters. Connect the output of each inverter to the input of the next inverter using wires (review the hotkeys for these functions as reviewed in earlier sections). Connect the output of the last inverter to the load capacitor. Name each net (the nets in this example are called 'InputNet,' 'N1,' 'N2,' ... 'OutputNet.') If you make a mistake, you can always do 'Edit → Undo' and try again. Don't be afraid if you make mistakes, just Undo and start over. Connect each inverter to vdd! and gnd! as shown in the image. Check & Save your schematic and inspect the CIW to make sure that it is successful.



# **Integrated Circuit Design CAD Tool Information**

**e.** Zoom in on the inverter chain and inspect the voltage sources V1 and V2 to make sure they and the first inverter appear as shown in the image below.



# **Integrated Circuit Design CAD Tool Information**

**f.** Zoom out from the inverter chain, and the first six inverters are shown as in the image below.



# **Integrated Circuit Design CAD Tool Information**

**g.** The last seven inverters and the load capacitor are shown in the image below.



# **Integrated Circuit Design CAD Tool Information**

**h.** Zoom in on the eleventh inverter and the load capacitor in the 'invchain\_test' schematic, and it will look as shown in the image below.



# **Integrated Circuit Design CAD Tool Information**

i. Set up a transient simulation and a dc simulation using the Virtuoso Analog Design Environment. Use the same series of steps that you used in an earlier section, and refer to it if you forget some of the steps. As a reminder, be sure to point to the device models for the nfet and pfet; point to spectre as the simulator, choose trans and dc analyses; save all the outputs; generate a netlist; run the simulation. The transient simulation is set for 4 microseconds, as shown in the image below.

🚆 Virtuoso® Analog Design Environment (	2) - EENG653 invchain_test schematic
Session Setup Analyses Variables Outputs Simulation Results	Fools Help cādence
IIII 27 I	
Design Variables	Analyses ? 🗗 X
Name Value	Type     Enable     Arguments       1     tran     ✓     0 4u moderate       2     dc     ✓     t
	Outputs     Image: Save Options       Name/Signal/Expr     Value       Plot     Save       Save Options
>	Plot after simulation: Auto 🔽 Plotting mode: Replace 🔽
mouse L:	M: R:
4(7) Transient Signal	Status: Ready   T=27 C   Simulator: spectre   State: state09APR2012

# **Integrated Circuit Design CAD Tool Information**

# **j.** Inspect the CIW to make sure that the simulation completes successfully, as shown in the image below.

C Virtuoso® 6.1.5-64b - Log: /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/CDS.19May2012.log	
File Tools Options Help	cādence
*WARNING* (icLic-3) Could not get license Analog_Design_Environment_L	<u> </u>
*WARNING* (icLic-21) License Analog Design Environment_L (*95200") is not available to run ADE-L.	
Hypig to the solution of the interior interior particular (solution) instead.	
generate netlist	
Begin Incremental Netlisting May 19 09:53:38 2012	
End netlisting May 19 U9:53:38 2012	
The netlist is up to date.	
Time taken to compare the design with netlist: 0.0s	
successful.	
compose simulator input file successful	
start simulator if needed	
successful.	
simulate	
Inte (Intersort). Similation completed successfully.	_
successful.	
Immouse L: showClickInto() M: schHiMousePopUp()	R: schHiMousePopUp()
1   >	

# **Integrated Circuit Design CAD Tool Information**

**k.** The netlist for this inverter chain is shown in the image below.

(home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/invchain_test/spectre/schematic/netlist/input.sc	s _ 🗆 🗙
<u>E</u> ile <u>H</u> elp	cādence
<pre>// Generated for: spectre // Generated on: May 19 09:53:33 2012 // Design library name: EEN0653 // Design cell name: invchain test // Design view name: schematic simulator lang=spectre global 0 vdd! include "/apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m" include "/apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m"</pre>	
<pre>// Library name: EENG653 // Cell name: inv // View name: schematic subckt inv GND VDD Vin Vout N0 (Vout Vin GND) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 \ ps=6u pd=6u m=1 region=sat P0 (Vout Vin VDD VDD) ami06P w=4.5u l=600n as=6.75e-12 ad=6.75e-12 \ ps=12.0u pd=12.0u m=1 region=sat ends inv // End of subcircuit definition.</pre>	111
<pre>// Library name: EEN6653 // Cell name: invchain_test // View name: schematic V0 (InputWet 0) vsource type=pulse val0=0 val1=5 period=2u rise=100n \ fall=100n width=1u V1 (vdd! 0) vsource type=dc dc=5 C0 (OutputNet 0) capacitor c=1p m=1 I10 (0 vdd! N10 OutputNet) inv I9 (0 vdd! N10 OutputNet) inv I9 (0 vdd! N9 N10) inv I8 (0 vdd! N9 Ni) inv I7 (0 vdd! N7 N8) inv I7 (0 vdd! N7 N8) inv I6 (0 vdd! N6 N7) inv I5 (0 vdd! N6 N7) inv I3 (0 vdd! N4 N5) inv I3 (0 vdd! N1 N2) inv I1 (0 vdd! N1 N2) inv I1 (0 vdd! N1 N2) inv I1 (0 vdd! InputNet N1) inv simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \ trom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxvets=5 maxvetns=5 \ dimits=5 cols=80 njvel=1e=3 aensfile=".org", charter of cols=10 maxvets=5 maxve</pre>	
<pre>ingle observations for the original of the second for the sec</pre>	-

# **Integrated Circuit Design CAD Tool Information**

**I.** The simulation output file (upper half) is shown in the image below.

C /home/afiten3/fac/mianzero/cadence/ncsu-cdk-1.6.0.beta/invchain_test/spectre/schemati 💷
Eile Help cädence
Cadence (R) Virtuoso (R) Spectre (R) Circuit Simulator Version 10.1.218 isrl4 64bit 5 Sep 2011 Copyright (C) 1989-2010 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, Virtuoso a
Protected by U.S. Patents: 5,610,847; 5,790,436; 5,812,431; 5,859,785; 5,949,992; 5,987,238; 6,088,523; 6,101,233; 6,151,698; 6,181,754; 6,260,176; 6,278,964; 6,349,272; 6,374,390; 6,493,849; 6,504,885; 6,618,837; 6,636,839; 6,778,025; 6,832,358; 6,651,097; 6,928,626; 7,024,652; 7,035,782; 7,085,700; 7,143,021; 7,493,240; 7,571,401.
Includes RSA BSAFE(R) Cryptographic or Security Protocol Software from RSA Security, Inc. User: mlanzero Host: vlsifac01 HostD: SOBISC19 PID: 26726 Memory available: 19.9969 08 physical: 25.2702 08 CPU Type: Intel(R) Xeon(R) OPU x5650 0 2.670Hz Processor PhysicalD CoreID Frequency 0 0 0 2660.1 1 0 1 2660.1 2 0 2 2660.1 3 0 8 2650.1 4 0 9 2660.1
5 0 10 2000.1 Simulating `input.scs' on vlsifac01 at 9:53:38 AM, Sat May 19, 2012 (process id: 26726). Environment variable: SPEOTRE DEFAULTS-E Command line: /app/vlai/Cadence/AMSIM101/tools.lxv86/spectre/bin/64bit/spectre \ input.scs +escchars +log/psf/spectre.out +inter=mpsc \ +mpsession=spectre1_25786_10 -format psfxL -raw/psf \ spectre pid = 26726
Loading /apps/vlsi/Cadence/MMSIM101/tools.lxx86/cmi/lib/64bit/5.0/libinfineon_sh.so Loading /apps/vlsi/Cadence/MMSIM101/tools.lxx86/cmi/lib/64bit/5.0/libphlipe_sh.so Loading /apps/vlsi/Cadence/MMSIM101/tools.lxx86/cmi/lib/64bit/5.0/libstmodels_sh.so Loading /apps/vlsi/Cadence/MMSIM101/tools.lxx86/cmi/lib/64bit/5.0/libstmodels_sh.so
Time for NDB Parsing: CPU = 67,989 ms, elapsed = 111.119 ms. Time accumulated: CPU = 67,989 ms, elapsed = 111.119 ms. Peak resident memory used = 34.1 Mbytes.
Time for Elaboration: CPU = 17.996 ms, elapsed = 18.332 ms. Time accumulated: CPU = 85.985 ms, elapsed = 129.583 ms. Peak resident memory used = 37.8 Mbytes.
Time for EDB Visiting: CPU = 1 ms, elapsed = 661.135 us. Time accumulated: CPU = 86.985 ms, elapsed = 130.367 ms. Peak resident memory used = 38.1 Mbytes.
Circuit inventory: nodes 13 bsim3v3 22 capacitor 1 vsource 2
Time for parsing: CPU = 2 ms, elapsed = 3.21078 ms. Time accumulated: CPU = 88.985 ms, elapsed = 133.679 ms. Peak resident memory used = 38.8 Mbytes.
Entering remote command mode using MPSC service (spectre, ipi, v0.0, spectre1_25786_10, ).
Warning from spectre. WARNING (SPECTRE-16707): Only tran supports psfxl format, result of other analyses will be in psfbi
Transient Analysis 'trans: time = (0 s -> 4 us) Transient parameter velues: Important parameter velues: start = 0 s outputtart = 0 s stop = 4 us stop = 4 us maxstep = 80 ns ic = all useprevic = no skipdc = no reltol = 10 - uv abtol() = 1 - 03 abtol() = 1 - 03 abtol() = 1 - 04 trans = 27 C trans = 7 C transet = sull terprevet = sull terprevet = sull terprevet = sill erprevet = sull terprevet = sill erprevet = sull terprevet = sill erprevet = sill terprevet = sill erprevet = sill terprevet = sill erprevet = siglobal cmin = 0 F gmin = 1 pS
tran. time = 100 ns (2.5 %), step = 2.795 ns (69.9 m%) tran. time = 305.8 ns (7.65 %), step = 80 ns (2 %) tran. time = 545.8 ns (13.6 %), step = 80 ns (2 %) tran. time = 705.8 ns (17.6 %), step = 80 ns (2 %) tran. time = 945.8 ns (23.6 %), step = 80 ns (2 %) tran. time = 1.1 us (27.5 %), step = 74.17 ns (1.85 %) tran. time = 1.353 us (33.8 %), step = 74.92 ns (1.87 %)
Lu Halbwann

# **Integrated Circuit Design CAD Tool Information**

**m.** The simulation output file (lower half) is shown in the image below.

() /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/invchain_test/spectre/sche	emati 🗕 🗆 🗙
Elle Help	cādence
capacitor 1 trource 2	~
Time for parsing: CPU = 2 ms, elapsed = 3.21078 ms. Time accumulated: CPU = 88.985 ms, elapsed = 133.679 ms. Pesk resident memory used = 38.8 Mbytes.	- 1
Warning from spectre.	
<pre>Walling thus (percentering): Only tran supports pefxl format, result of other analyses will  Transient Analysis 'tran': time = (0 s -&gt; 4 us) Transient Analysis 'tran': time = (0 s -&gt; 4 us) Tuportant persenter values:     supputstatt = 0 s     stop = 4 us     stop = 4 us     stop = 4 ns     maxstep = 80 ns     ic = all     useprevic = no     skipkc = no     skipkc = no     skipkc = 1 uW     abstol(V) = 1 uW     abstol(V) = 1 uW     abstol(V) = 1 uW     abstol(V) = 1 uB     tempeffects = all     errpreset = noderate     method = trapenity     relref = sigglboal     cmin = 0 P     gmin = 1 pS </pre>	be in pefbi
$\begin{array}{c} \mbox{tran: time = 100 ns} & (2.5 \ \mbox{k}), \ \mbox{step = 2.795 ns} & (69.9 \ \mbox{m}\ \mbox{m}\ \mbox{m}\ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 545.8 ns} & (13.6 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 945.8 ns} & (17.6 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 945.8 ns} & (17.6 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 1.612 us} & (27.5 \ \mbox{k}), \ \mbox{step = 74 J2 ns} & (1.67 \ \mbox{k}) \\ \mbox{tran: time = 1.612 us} & (27.5 \ \mbox{k}), \ \mbox{step = 74 J2 ns} & (1.67 \ \mbox{k}) \\ \mbox{tran: time = 1.612 us} & (27.5 \ \mbox{k}), \ \mbox{step = 74 J2 ns} & (1.67 \ \mbox{k}) \\ \mbox{tran: time = 1.512 us} & (27.8 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 1.913 us} & (47.8 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 2.344 us} & (58.3 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 2.574 us} & (64.3 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 2.574 us} & (64.3 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 3.254 us} & (68.2 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 3.326 us} & (68.2 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 3.326 us} & (68.2 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 3.326 us} & (68.2 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 3.326 us} & (68.2 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 3.326 us} & (68.2 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 3.326 us} & (68.2 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 3.326 us} & (68.2 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 3.326 us} & (68.2 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 3.326 us} & (68.2 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 3.326 us} & (68.2 \ \mbox{k}), \ \mbox{step = 80 ns} & (2.8) \\ \mbox{tran: time = 3.326 us} & (68.2 \ \mbox{k})$	
Notice from spectre during transient analysis `tran'. Trapezoidal ringing is detected during tran analysis. Please use method-trap for better results and performance.	
Initial condition solution time: CPU = 2 ms, elapsed = 1.11485 ms. Intrinsic tran analysis time: CPU = 53.992 ms, elapsed = 59.1469 ms. Total time required for tran analysis 'tran': CPU = 57.992 ms, elapsed = 70.487 ms. Time accumulated: CPU = 148.977 ms, elapsed = 359.265 ms. Peak resident memory used = 40.1 Mbytes.	
finalTimeOP: writing operating point information to rawfile.	
<pre>0. Analysis 'doDy' DO Analysis 'doDy' '''''''''''''''''''''''''''''''''''</pre>	
<pre>booking. stacking opticating for a introduction to familie. booking opticating with model preserved values to trailie computParameter: writing output parameter values to rawfile. desingParameter: writing netList parameters to rawfile. primitives: writing primitives to rawfile. subckts: writing subcircuits to rawfile.</pre>	
20 HelpAction	

# **Integrated Circuit Design CAD Tool Information**

- n. After the simulation completes successfully, annotate the results and then perform a direct plot of the transient signals. The image below displays the waveforms of the transient signals 'InputNet,'
   'OutputNet,' and 'N5' near the time t = 1.1 microseconds to t = 1.2 microseconds. Values for the following quantities can be obtained for each inverter pair:
  - a. For the falling transition of the input waveform
    - i. Fall time
    - ii. Delay
  - b. For the rising transition of the input waveform





ii. Delay

# **Integrated Circuit Design CAD Tool Information**

**o.** The complete waveforms for 'InputNet,' 'OutputNet,' and 'N5' in the time range t = 0 microseconds to t = 4 microseconds are shown in the image below.



# **Integrated Circuit Design CAD Tool Information**

- **p.** You can now save the state for this simulation. Save the state as the name 'state-invchain.' You will load this state in the next section, when you create a ring oscillator. The procedure to save a state was discussed in the previous sections. Refer to the previous sections if you forget how to save the state of your simulation.
- **q.** You can now increase the value of the load capacitor. Values for the following quantities can be obtained for each value of the load capacitor for each inverter pair. Note that the values of the widths of the successive inverters may need to be increased in order to drive the load capacitor:
  - a. For the falling transition of the input waveform
    - i. Fall time
    - ii. Delay
  - b. For the rising transition of the input waveform
    - i. Rise time
    - ii. Delay
- **r.** You have now completed this section on the inverter chain.

# **Integrated Circuit Design CAD Tool Information**

# 25. Ring Oscillator

**a.** In this section, you will create and simulate a ring oscillator that is composed of 11 inverters. In the 'EENG653' library, copy the 'invchain\_test' cell to a new cell called 'ringoscillator\_test' as shown in the image below. Make sure that the 'inv' instantiated in the 'ringoscillator\_test' library still points to the 'inv' cell in the 'EENG653' library.

Library Manager: Directoryro/cadence/ncsu-cdk-1.6.0.beta		
<u>File Edit V</u> iew <u>D</u> esign Manager <u>H</u> elp		cādence
Show Categories       Show Files         Library         EENG653         EENG653Tutorial         NCSU_Analog_Parts         NCSU_Digital_Parts         NCSU_TechLib_ami06         NCSU_TechLib_hp06         NCSU_TechLib_tsmc02         NCSU_TechLib_tsmc03d         NCSU_TechLib_tsmc03d         NCSU_TechLib_tsmc03d         NCSU_TechLib_tsmc04_4M2P         avTech         basic         cdsDefTechLib         megan	Cell ringoscillator_test inv inv_test invchain_test inverter ringoscillator_test	View schematic View <u>Lock</u> Schematic mlanzero@vlsifac01
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# **Integrated Circuit Design CAD Tool Information**

b. Open the 'ringoscillator\_test' cell schematic and wire the 11 inverters into a ring as shown in the image below. You will need to delete the load capacitor. Note that the output node of the 11<sup>th</sup> inverter is connected to the input node of the first inverter as shown in the image.

Check & Save the schematic and make sure the check & save completes successfully by inspecting the CIW. Make sure there are no errors or warnings. If you have errors and/or warnings, go back and fix your schematic. Then, rerun Check & Save your schematic to make sure it completes successfully.



#### **Integrated Circuit Design CAD Tool Information**

**c.** When you are creating a hierarchical schematic that contains many levels of hierarchy, you may find it helpful to make modifications on different cells that are instantiated in the schematic without closing and opening different schematics. You can edit or read different cells through a process referred to as *traversing the hierarchy* of the schematic. You can traverse the hierarchy upwards, and you can also traverse the hierarchy downwards. The image below shows how to descend the hierarchy to read a cell in a lower level of the hierarchy (change the radio button to 'edit' if you want to edit the cell in the lower level of the hierarchy.)

For example, to make modifications to or to read the 'inv' schematic contained in the 'ringoscillator\_test' schematic, click on "Edit  $\rightarrow$  Hierarchy  $\rightarrow$  Descend Edit" or "Edit  $\rightarrow$  Hierarchy  $\rightarrow$  Descend Read." The 'Descend' window will appear as shown in the image below. Click OK in the window. The inverter should now appear. You can now edit it if you want; be sure to Check & Save after editing. This will change all instances of 'inv' schematic in your hierarchical schematics.



# **Integrated Circuit Design CAD Tool Information**

**d.** Now you will perform a transient simulation to learn about the operation of the ring oscillator. In the Virtuoso Schematic window, launch the Analog Design Environment (ADE). As in previous sections, you will need to set up the simulation: select the simulator (spectre), load the model files, choose a transient analysis (4 microseconds stop time; moderate accuracy default), choose a dc analysis, print all output signals (allpub), generate the netlist, and run the simulations. You may find it helpful to load the state of the 'state-invchain' that you saved in the previous section. Review the previous sections if you do not recall how to set up these simulations with spectre. Your Analog Design Environment window will appear as shown in the image below.

For large schematics, you will want to save only a few signals to speed up your simulations.

🖀 Virtuoso® Analog Design I	nvironment (3) - EENG653 ringoscillator_test s	schemat 🗕 🗆 🗙
Session Setup Analyses Variable	s Outputs Simulation Results Tools Help	cādence
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Design Variables	Analyses	? 🗗 🗙 🚃
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	Name/Signal/Expr   Value   Plot   Save   Si	ave Options
>	Plot after simulation: Auto Plotting mode: Re	place
mouse L:		R:
16(34) Save State	Status: Ready   T=27 C   Simulator: spectre   St	late: state-invchain 📗

#### **Integrated Circuit Design CAD Tool Information**

e. To help with convergence of the simulation of the ring oscillator, you will now set up an initial condition which is to initialize the input node to zero (0) at the left-mode inverter. Click on 'Simulation → Convergence Aids → Initial Condition.' A window entitled "Select Initial Condition Set' will appear.

	Select Initial Condition Set	X
Node Voltage		
Voltage	Node Set	
0	/inputNet	
1		
	OK Cancel Annly Delete Helr	
	Cancer (hppi) Delete (heik	

# **Integrated Circuit Design CAD Tool Information**

**f.** Then click on the left-most node in the schematic, as shown in the image below. The 'Select Initial Condition Set' window will show that the 'InputNet' voltage is set to '0.' Note that the net itself becomes highlighted in the 'ringoscillator\_test' schematic, and a large '0' is written on top of the net.


# **Integrated Circuit Design CAD Tool Information**

**g.** The left side of the 'ringoscillator\_test' schematic is shown in the image below after zooming in on the initial inverters.



# **Integrated Circuit Design CAD Tool Information**

**h.** The right side of the ring oscillator inverter chain is also shown in the image below after zooming in on the inverters. Notice the output (11<sup>th</sup>) inverter.



# **Integrated Circuit Design CAD Tool Information**

i. You can now generate the netlist and run the simulation. Launch the Visualization & Analysis XL tool and generate plots of the waveforms of the 'InputNet' and the following net (N1, in this case) as shown in the image below. In case there are errors, you will need to go back and correct the errors. You may need to do 'Simulation → Netlist' again if you change the schematic. Remember also that each time you change the schematic, you need to do a 'Check & Save.' You will be able to view the simulation results when there are no errors.



# **Integrated Circuit Design CAD Tool Information**

**j.** The netlist of this ring oscillator is shown in the image below.

c dero/cadence/ncsu-cdk-1.6.0.beta/ringoscillator_t	test/spe 💶 🗖 🗙
Eile Help	c <mark>ā</mark> d e n c e
<pre>// Generated for: spectre // Generated on: May 19 13:07:05 2012 // Design library name: EEN0653 // Design cell name: ringoscillator_test // Design view name: schematic simulator lang=spectre global 0 vdd! include "/apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m" include "/apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m"</pre>	Â
<pre>// Library name: EENG653 // Cell name: inv // View name: schematic subckt inv GND VDD Vin Vout NO (Vout Vin GND GND) amiO6N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 \         ps=6u pd-6u m=1 region=sat PO (Vout Vin VDD VDD) amiO6P w=4.5u l=600n as=6.75e-12 ad=6.75e-12 \         ps=12.0u pd=12.0u m=1 region=sat ends inv // End of subcircuit definition.</pre>	
<pre>// Library name: EEN0653 // Cell name: ringoscillator_test // View name: schematic V1 (vdd! 0) vsource type=dc dc=5 110 (0 vdd! N10 InputNet) inv I9 (0 vdd! N9 N10) inv I8 (0 vdd! N9 N10) inv I8 (0 vdd! N8 N9) inv I7 (0 vdd! N1 N8) inv I6 (0 vdd! N6 N7) inv I5 (0 vdd! N5 N6) inv I4 (0 vdd! N5 N6) inv I3 (0 vdd! N3 N4) inv I2 (0 vdd! N2 N3) inv I1 (0 vdd! N1 N2) inv I1 (0 vdd! Iavnet N1) inv</pre>	
<pre>is (o val inpute in ) inv is InputNet=0 simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \ tomm=27 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \ digits=5 cols=80 pivrel=1e-3 sensfile="/psf/sens.output" \ checklimitdest=psf tran tran stop=4u errpreset=moderate write="spectre.ic" \ writefinal="spectre.fc" annotate=status maxiters=5 finalTimeOP info what=oppoint where=rawfile dcOp dc write="spectre.fc" maxiters=150 maxsteps=10000 annotate=status dcOpInfo info what=oppoint where=rawfile modelParameter info what=models where=rawfile element info what=inst where=rawfile</pre>	
outputParameter info what=output where=rawfile designParamVals info what=parameters where=rawfile primitives info what=primitives where=rawfile subckts info what=subckts where=rawfile saveOptions options save=allpub	

# **Integrated Circuit Design CAD Tool Information**

**k.** The upper part of the file displaying the simulation run is shown in the image below.

Elle         Eddence           Enderse         (f) Virtusse (f) Spectre (f) Circuit Simulator           Version (0) 1: 203 srid 64bit - 5 Sep 2011           Dopright (0) 1989-2010 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, Virtusso and Spectre           Protected by US Patents         (f) Sep 2011           School Size 5: 101.233, 6: 101.233, 6: 101.754, 5: 200.1756, 5: 200.944;         (f) Sep 2011           School Size 5: 101.233, 6: 101.233, 6: 101.754, 5: 200.1756, 5: 200.100.2560.1           Simulating 'input ses' en vlsifac01 at 1:07:11 PM, Sat May 19, 2012 (process id: 27648).           Simulating 'input ses' en vlsifac01 at 1:07:11 PM, Sat May 19, 2012 (process id: 27648).           Simulating 'input ses' en vlsifac01 at 1:07:11 PM, Sat May 19, 2012 (process id: 27648).           Simulating 'input ses' en vlsif
<pre>Gadeca (D) Firtups (A) Spects (A) Circuit Simulator VeryFight (C) 1999-2010 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, Virtuoso and Spectre Protected by U.S. Petents:     S. Glinkar, 5.700, 445, 5.512, 441, 5.863, 786; 5.409, 992, 5.907, 238,     G. 430, 272; 6.214, 330; 6.430, 154, 5.817, 442, 5.801, 755, 5.700, 748,     G. 430, 272; 6.214, 330; 6.430, 144, 6.504, 855; 6.618, 637, 6.636, 639,     G. 705, 6.83, 5.85, 6.851, 977, 5.926, 6.53, 759, 7.656, 763, 759, 7.705, 7.057, 705, 7.143, 021, 7.493, 240, 7.571, 401. Includes RSA BSATE(N) Cryptographic or Security Protocol Software from RSA Security, Inc.     Use: malanero Rost: visifac01 HostID: SC015619 PID: 27648     Weary available: 19.445; 60 physical: 25.2792 08     CU Type: Intel(R) Xoon(R) CU</pre>
Protected by U.S. Patents: 5.088.523; 6.101.232; 6.512.431; 5.859.785, 5.949.992; 5.987.238; 6.088.523; 6.101.232; 6.512.688; 6.181.744; 6.280.176; 6.278.964; 6.382.721; 6.372.901; 6.423.091; 6.504.885; 6.518.807; 6.658.639; 6.778.025; 6.382.559; 6.612.071; 6.524.885; 6.518.807; 6.658.639; 6.778.025; 6.382.559; 6.612.17, 6.392.081; 7.571.401 Includes FAS BEAFE(8) Cryptographic or Security Protocol Software from RSA Security. Inc. User: mlanzero: Host: visifac01 HostID 26815619 PID: 27648 Hencry available: 13.9468; 00 physical: 25632 0.670Hz Urype: Processor PhysicalID CoreID Frequency 0 0 0 0 26601 1 0 0 1 26601 2 0 2 26601 3 0 0 2 26601 3 0 0 2 06601 5 0 10 26601 1 0 0 0 26601 2 0 0 26601 1 0 0 0 26601 1 0 0 0 26601 1 0 0 0 26601 1 0 0 0 26601 5 0 10 26601 5 0 10 26601 1 0 0 0 26601 1 0 0 0 26601 1 0 0 26601 1 0 0 0 26601 1 0 0 0 26601 5 0 0 10 2660 5 0 0 10 2600 5 0
<pre>Includes RSA ESAFE(R) Gryptographic or Security Protocol Software from RSA Security. Inc. User: mlanzero Host: vlsifac01 HostID: SO20150 PID: 27648 Heary available: 19.4455 08 physical: 25.2792 08 GPU Type: Intel(R) Koon(R) GPU X5650 # 2.670Hz Protessor PhysicalD CoreID Prequency 0 0 0 2660.1 1 0 1 2660.1 3 0 8 2660.1 3 0 8 2660.1 5 0 10 2660.1 Security Protocols 1: 0.711 PM, Sat May 19, 2012 (process id: 27648). Environment Variable: SPECTRE DEFAULTS=E Command Inte: //apps/vlsi/Cadence/MMSIM101/tools.lnx86/spectre/bin/64bit/Spectre \ 'thrimeout 900 =maxw 5 -maxoT. 'dot inte: //apps/vlsi/Cadence/MMSIM101/tools.lnx86/spectre/bin/64bit/Spectre \ 'thrimeout 900 =maxw 5 -maxoT. 'dot inte: //apps/vlsi/Cadence/MMSIM101/tools.lnx86/spectre/bin/64bit/S 0/libpinfineon sh.so Loading /apps/vlsi/Cadence/MMSIM101/tools.lnx86/smi/lib/64bit/S 0/libpinfineon sh.so Loading /apps/v</pre>
<pre>User: alametro Host: vlsifac01 HostD: Sc01519 PD: 27648 Mearyr aveniable: 19.4455 GB physical: 25.7522 GB GPU Type: Intel(N) Keen(N) GPU X5650 e 2.670Hz Processor PhysicalD CoreID Prequency 0 0 0 2660.1 1 0 0 2660.1 3 0 8 2660.1 4 0 9 2660.1 5 0 10 2660.1 Simulating 'input scs' on vlsifac01 at 1:07:11 PM, Sat May 19, 2012 (process id: 27648). Environment variable: SPECTRE DEFAULTS=-E Command Line: //apps/vlsi/Cadence/MMSIM101/tools.lnx86/spectre/bin/64bit/spectre \</pre>
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<pre>Loading /sps/vlsi/Cadence/MESINIO1/tools Inv85/cmi/lb/6bit/5 0/lbinfineon_sh.so Loading /sps/vlsi/Cadence/MESINIO1/tools Inv85/cmi/lb/6bit/5 0/lbsparsa_sh.so Loading /sps/vlsi/Cadence/MESINIO1/tools Inv85/cmi/lb/6bit/5 0/lbsparsa_sh.so Loading /sps/vlsi/Cadence/MESINIO1/tools Inv85/cmi/lb/6bit/5 0/lbsparsa_sh.so Time for NUE Parsing: OPU = 65.989 ms. elapsed = 111.107 ms. Peak resident menory used = 34.2 Mbytes. Time for Elaboration: OPU = 17.997 ms. elapsed = 129.649 ms. Peak resident menory used = 38.2 Mbytes. Time for Elaboration: OPU = 17.997 ms. elapsed = 129.649 ms. Peak resident menory used = 38.2 Mbytes. Time for EDE Visiting: OPU = 1 ms. elapsed = 642.061 us. Time nercumulated: OPU = 84.986 ms. elapsed = 130.413 ms. Peak resident menory used = 38.5 Mbytes. Circuit inventory:</pre>
<pre>Time for NDE Parsing: CPU = 65.989 ms, elapsed = 111.107 ms. Time accusulated: CPU = 65.989 ms, elapsed = 111.107 ms. Test resident memory used = 34.2 Mbytes. Time for Elaboration: CPU = 17.997 ms, elapsed = 129.649 ms. Peak resident memory used = 38.2 Mbytes. Time for EDE Visiting: CPU = 1 ms, elapsed = 642.061 us. Time accusulated: CPU = 84.986 ms, elapsed = 130.413 ms. Peak resident memory used = 38.5 Mbytes. Circuit inventory:</pre>
<pre>Time for Elaboration: GPU = 17.997 ms, elapsed = 18.4011 ms. Time accumulated: GPU = 83.966 ms, elapsed = 129.649 ms. Peak resident memory used = 38.2 Mbytes.</pre> Time for EDB Visiting: CPU = 1 ms, elapsed = 642 061 us. Time accumulated: CPU = 84.986 ms, elapsed = 130.413 ms. Peak resident memory used = 38.5 Mbytes. Circuit inventory: nodes 12 binavoz 12 vosurce 1 Time for parsing: CPU = 2 ms, elapsed = 2.75707 ms. Time accumulated: CPU = 86.986 ms, elapsed = 133.279 ms. Peak resident memory used = 39.2 Mbytes. Entering remote command mode using MPSC service (spectre, ipi, v0.0, spectre2_25786_11, ).
<pre>Time for EUB Visiting: CPU = 1 ms, elapsed = 642.061 us. Time accumulated: CPU = 84.986 ms, elapsed = 130.413 ms. Peak resident memory used = 35.8 Mbytes. Circuit inventory:</pre>
Circuit inventory: nodes 12 bsin393 22 vsource 1 Time for parsing: CPU = 2 ms, elapsed = 2.75707 ms. Time accumulated: CPU = 86.986 ms, elapsed = 133.279 ms. Peak resident menory used = 39.2 Moyts. Entering remote command mode using MPSC service (spectre, ipi, v0.0, spectre2_25786_11, ).
Time for parsing: CPU = 2 ms. elapsed = 2.75707 ms. Time accumulated: CPU = 26.966 ms. elapsed = 133.279 ms. Peak resident memory used = 39.2 Mbytes. Entering remote command mode using MPSC service (spectre, ipi, v0.0, spectre2_25786_11, ).
Entering remote command mode using MPSC service (spectre, ipi, v0.0, spectre2_25786_11, ).
Warning from spectre. WARNING (SPECTRE-16707): Only tran supports psfxl format, result of other analyses will be in psfbin format.
Transient Analysis 'tran': time = (0 s -> 4 us)
Notice from spectre during IO analysis, during transient analysis `tran'. There are 1 IO nodes defined. Notice from spectre during IO analysis, during transient analysis `tran'. Initial condition computed for node Ingulèt is in error by 1.12635 MV. Decrease `tforce' to reduce error in computed initial conditions. However, setting rforce too small may r
Important parameter values: start = 0 s outputstart = 0 s stop = 4 us stop = 4 us maxstep = 80 ns ic = all useprevic = no skipdc = no reltol = 1e-03 abstol(V) = 1 uW abstol(I) = 1 pA temp = 27 c tempeffects = moderate experiset = moderate method = tranonly method = tranonly tranonly method = tranonly method = tranon

# **Integrated Circuit Design CAD Tool Information**

**I.** The lower part of the file displaying the simulation run is shown in the image below.

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Eile Help	cādence
Transient Analysis `tran': time = (0 s> 4 us)	
Notice from spectre during IC analysis, during transient analysis 'tran'. There are 1 IO nodes defined. Notice from spectre during IC analysis, during transient analysis 'tran'. Initial condition computed for node InputNet is in error by 1.12635 mV. Decrease 'froce' to reduce error in computed initial conditions. However, setting rfo	rce too small may r
Important parameter values: start = 0 s otop = 4 us stop = 4 us maxtep = 80 ns ic = all ussprevi = no skipde = no reltol = 1e-03 abtol(1) = 1 µA temp = 27 0 tempeffects = all errpreset = moderate method = traponly lteratio = 3.5 relife = sigglobal otom = 1 pS	
$ \begin{array}{llllllllllllllllllllllllllllllllllll$	
Notice from spectre during transient analysis `tran'. Trapezoidal ringing is detected during tran analysis. Please use methodetrap for better results and performance.	
Initial condition solution time: CPU = 1 ms, elapsed = 1.23978 ms. Initial condition solution time: CPU = 17,4713 s, elapsed = 17,4954 s. Total time required for tran analysis tran': CPU = 17,4743 s, elapsed = 17.5022 s. Time accumulated: CPU = 17.6453 s, elapsed = 18.0591 s. Peak resident memory used = 86.8 Mbytes.	
<pre>finalTimeOP: writing operating point information to rawfile. ************************************</pre>	
nuckes: willing subcircuits to rawile.	
38 HelpAction	

# **Integrated Circuit Design CAD Tool Information**

**m.** You can display the waveforms separately by clicking on the left of the display window and selecting 'Plot to New Strip.'

These waveforms should show the desired results, namely periodic waveforms as we expect for a ring oscillator. You can determine the period of oscillation and measure the inverter delay.



# **Integrated Circuit Design CAD Tool Information**

n. You can recombine the waveforms into one set of axes by right clicking in the left section of the Visualization & Analysis window and selecting 'Combine All Analog Traces.' Your Visualization & Analysis XL window will look like the image below. It is a good idea to save your state, such as 'state-ringoscillator,' before exiting the simulator in the event that you would like to redo some of the simulations (then you can load a saved state).



**o.** Now you have simulated a ring oscillator.

# **Integrated Circuit Design CAD Tool Information**

# 26. Ring Oscillator: Learning to Use the Calculator

- **a.** In this section, you are going to learn how to use the Calculator in Cadence.
- **b.** The first example will be to show you how to measure the delay in the ring oscillator for the case in which the input waveform has a low-to-high transition (rising transition) and the output waveform therefore has a high-to-low transition (falling transition). You will measure the delay with the Cadence calculator.

#### **Integrated Circuit Design CAD Tool Information**

**c.** To open the Cadence Calculator, click on 'Tools  $\rightarrow$  Calculator' in the Analog Environment window, and the 'Calculator' window will appear as shown below. Spend some time to get familiar with the calculator (see Help and the online documents).

Wirtuoso (R) Visualization & Analysis XL calculator	_ <b>D</b> X
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In Context Results DB: /home/afiten3/SOCHE/kmantell/cadence/ncsu-cdk-1.6.0.beta/ringoscillator_test/spectre/schematic/psf	
Ovt       Ovf       Ovc       Ovs       O op       O var       O vn       O sp       O vswr       O hp       O zm         O it       O if       O is       O opt       O mp       O vn2       O zp       O yp       O gd       O data	
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Key         G         X           7         8         7           4         5         6           1         2         3	
Stack	Ð×
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PN       d2a       fallTime       harmonicFreq       peak       pzfliter       spectrumMeas         a2d       dBm       flip       histo       peakToPeak       riseTime       stddev         abs_jitter       delay       fourEval       iinteg       peakToPeak       riseTime       stagent         average       deriv       freq       integ       phaseMargin       ms Noise       thd         bandwidth       dft       freq_litter       intersect       phaseNoise       root       untyGainFreq         clip       dtbb       frequency       ipn       pow       rshift       value         compare       dnl       gainBwProd       ipn/Ri       prms       sample       xmax         compression/VRI       evmQAM       getAsciiWave Ishift       psd settlingTime       xmin         convolve       evmQApsk       groupDelay       overshoot       psddev       spectralPower         cross       eyeDiagram       harmonic       pavg       pzbode       spectrum       ymin	
Function Panel Expression Editor Memories	
8	

# **Integrated Circuit Design CAD Tool Information**

- **d.** The calculator works with a 'stack' (like some HP calculators) in which you first input one or more operands (waveforms), and then you perform an operation on them. After each operation, it is recommended that you clear the stack (clst). To view the stack, you have to enable it (click on the Display Stack).
- e. Now you will set up your waveforms in the Visualization & Analysis window to look like the ones in the image below. Notice that in this image, the waveform for the InputNet starts low and transitions to Vdd (a low-to-high transition, or rising edge). Notice also that in the image, the waveform for the output net (N1 for the case shown) starts high and transitions to 0 V (a high-to-low transition, or falling edge). This edge is referred to as the first edge, or 'edge 1.'



# **Integrated Circuit Design CAD Tool Information**

**f.** Now click on the 'Wave' radio button in the calculator window. Then click on the output waveform (the waveform with the low to high transition, in this case, N1) in the Visualization & Analysis XL window. (Be sure not to click on the wave name on the left-hand side; click instead on the waveform itself).



#### **Integrated Circuit Design CAD Tool Information**

**g.** A wave name should appear in the calculator window as shown in the image below. This image shows the wave name "N1" in the window. The syntax of the statement in the window, 'clipX,' refers to the zoomed-in portion of the waveform that you are displaying in the waveform window. The syntax of the two values in blue at the end of the statement refer to the start time and to end time of the zoomed-in portion of the viewing window that you selected in the Visualization & Analysis XL window.

W Virtuoso (R) Visualization & Analysis XL calculator	_ <b>_ X</b>
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In Context Results DB: /home/afiten3/SOCHE/kmantell/cadence/ncsu-cdk-1.6.0.beta/ringoscillator_test/spectre/schematic/psf	
O vt       O vf       O vdc       O vs       O op       O var       O vn       O sp       O vswr       O hp       O zm         O it       O if       O idc       O is       O opt       O mp       O vn2       O zp       O yp       O data	
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PN       d2a       fallTime       harmonicFreq       peak       pzfilter       spectrumMeas         a2d       dBm       flip       histo       peakToPeak       riseTime       stddev         abs_jitter       delay       fourEval       integ       period_jitter       ms       tangent         average       deriv       freq       integ       phaseMargin       msNoise       thd         bandwidth       dft       freq_itter       intersect       phaseNoise       tod       unityGainFreq         clip       dtbb       frequency       ipn       pow       rshift       value         compare       dnl       gainBwProd       ipn/YRI       prms       sample       xmax         compressionVRI       evmQAM       getAscilWave       Ishift       psdbb       slewRate       xval         convolve       evmQApk       groupDelay       overshoot       psddev       spectralPower       ymax         cross       eyeDiagram       harmonic       pavg       pzbode       spectrum       ymin	
Function Panel Expression Editor Memories	
8	

### **Integrated Circuit Design CAD Tool Information**

**h.** Now click on the input waveform wave (it transitions from low to high first). Be sure not to click on the name of the waveform on the left-hand side of the window. You are selecting the rising edge of this waveform, and it is edge 1 (in the zoomed-in portion of the waveform that you display in the window).



#### **Integrated Circuit Design CAD Tool Information**

i. Now check in the calculator to verify that the name of the first waveform (N1 in the case shown) has been pushed into the stack and brings the name of the input waveform into the calculator (InputNet in the case shown). Important: Note that the waveforms were entered in reverse order (the late first; then the early one); this is a feature of the stack operation of the calculator.

W Virtuoso (R) Visualization & Analysis XL calculator	_ <b>_ X</b>
Eile <u>T</u> ools <u>V</u> iew <u>O</u> ptions <u>C</u> onstants <u>H</u> elp	cādence
In Context Results DB: /home/afiten3/SOCHE/kmantell/cadence/ncsu-cdk-1.6.0.beta/ringoscillator_test/spectre/schematic/psf	
ovt ovf ovdc ovs op ovar ovn osp ovswr ohp ozm it oif oidc ois opp omp ovn2 ozp oyp ogd odata	
📗 Off O Family 🖲 Wave 🗹 Clip   🍢 🎣 Append 🔽 🎯   🗮	
Key         Image: Second system         ClipX ("/InputNet" ?result "tran") 126.9E-9 132.4E-9 [           7         8         9         /           4         5         6         *           1         2         3         -	
Stack	ē ×
Function Panel	ē ×
Special Functions	
PN       d2a       fallTime       harmonicFreq       peak       pzfilter       spectrumMeas         a2d       dBm       flip       histo       peakToPreak       riseTime       stddev         abs_jitter       delay       fourEval       integ       period_jitter       msettineg         average       deriv       freq       integ       phaseMargin       msNoise       thd         bandwidth       dft       freq_jitter       intersect       phaseMargin       unityGainFreq         clip       dthbb       frequency       ipn       pow       rshift       value         compare       dnl       gainBwProd       ipn/VRI       prms       sample       xmax         compressionVRI       evmQAM       getAscilWavg       Ishift       psdbb       slewRate       xval         convolve       evmQAM       getAscilWavg       Ishift       psdbb       slewRate       xval         cross       eyeDlagram       harmonic       pavg       pzbode       spectrum       ymin	
Function Panel Expression Editor Memories	
8 8	

#### **Integrated Circuit Design CAD Tool Information**

j. Now move the cursor to 'Special Functions' in the calculator window. Select 'delay'. Fill 2.5 as the threshold values (50% of Vdd = 2.5V since Vdd = 5V). Notice that in the 'delay' section, the name of your first waveform (N1 in this case) is listed as 'Signal2,' and the name of your second waveform (InputNet in this case) is listed as 'Signal1'. For Signal1, set the Edge Number equal to 1. For Signal2, set the Edge Number equal to 1. For Signal 1, set the Edge Type 1 to 'rising.' For Signal 2, set the Edge Type 2 to 'falling.' Then click 'OK'.

Wirtuoso (R) Visualization & Ana	lysis XL calculator
<u>Eile T</u> ools <u>V</u> iew <u>O</u> ptions <u>C</u> onstants <u>H</u> elp	cādence
In Context Results DB: /home/afiten3/SOCHE/kmantell/cadence/ncsu-cdk-1.6.0.beta/ringoscillate	or_test/spectre/schematic/psf
oit oif oidc ois opt omp ovn2 ozp ovp od odata	
I Off ⊂ Family ● Wave I ✓ Clip I A Append ■ 1 200 I =	
Key         Image: Second	
7 8 9 /	
4 5 6 *	
0 ± . + 🔺 💭 🔝 📴 🗐 🛍 🛛 🕷 🕷 🗮 📶 ME 有 🔗	¢
Stack	e ×
clipX(v("/N1" ?result "tran") 88.28E-9 93.79E-9 )	
(REEL)	
Function Panel	e ×
Special Functions	
delay	
Signal1 clipX(v("/inputNet" ?result "tran") 88.28E-9 93.79E-9 )	
Signal2 ClipX(v("/N1" ?result "tran") 88.28E-9 93.79E-9 )	
Threshold Value 1 2.5 Thr	eshold Value 2 2.5
Edge Number 1 1	dge Number 2 1
Edge Type 1 rising	Edge Type 2 [falling
	QK Apply Defaults Close Help
Function Panel Expression Editor Memories	
Successful evaluation	
8	

# **Integrated Circuit Design CAD Tool Information**

**k.** Notice the change in the calculator window. The entry has now been expanded to show the delay calculation expression.

Virtuoso (R) Visualization & Analysis XL calculator	_ 🗆 🗙
<u>Eile T</u> ools <u>V</u> iew <u>O</u> ptions <u>C</u> onstants <u>H</u> elp	cādence
In Context Results DB: /home/afiten3/SOCHE/kmantell/cadence/ncsu-cdk-1.6.0.beta/ringoscillator_test/spectre/schematic/psf	
ovt ovf ovdc ovs op ovar ovn osp ovswr ohp ozm oit oif oidc ois opt omp ovn2 ozp oyp ogd odata	
💭 Off 🔾 Family 🖲 Wave 🗹 Clip   🍌 🐖 Append 🔽 🍪   🗄	
Key         Image: Second	93.79E-9 ),
0 ± . + • 3 12 12 12 12 12 12 12 12 12 12 12 12 12	
Stack	5×
CipX(v("/InputNet" ?result "tran") 88.28E-9 93.79E-9 ) CipX(v("/N1" ?result "tran") 88.28E-9 93.79E-9 )	
Function Panel	a x
Special Functions	
PN       d2a       fallTime       harmonicFreq       peak       pzfilter       spectrumMeas         a2d       dBm       flip       histo       peakToPeak       riseTime       stddev         abs_jitter       delay       fourEval       iinteg       period_jitter       rms       tangent         average       deriv       freq       integ       phaseMargin       rmsNoise       thd         bandwidth       dft       freq_jitter       intersect       phaseNoise       root       unityGainFreq         clip       dftbb       frequency       ipn       pow       rshift       value         compare       dnl       gainMargin       loadpull       psd       settlingTime       xmin         compression       dutyCycle       gainMargin       loadpull       psd       settlingTime       xmin         convolve       evmQAM       getAsciiWave       Ishift       psdbb       slewRate       xval         cross       eyeDiagram       harmonic       pavg       pzbode       spectrulPower ymax	
Function Panel Expression Editor Memories	
8	

#### **Integrated Circuit Design CAD Tool Information**

**I.** Now click on the 'Evaluate' buffer (the icon to the left of 'Append' pulldown), and you will see a value for the rising delay (tpLH) for the inverter (in the ring oscillator). In the image below, the result of the delay calculation shows that the rising delay for edge 1 is 156.6 ps.

W Virtuoso (R) Visualization & Analysis XL calculator 💷 💌
Eile Tools View Options Constants Help cādence
In Context Results DB: /home/afiten3/SOCHE/kmantell/cadence/ncsu-cdk-1.6.0.beta/ringoscillator_test/spectre/schematic/psf
Ovt Ovf Ovdc Ovs Oop Ovar Ovn Osp Ovswr Ohp Ozm
li ⊂ if ⊂ idc ⊂ is ⊂ opt ⊂ mp ⊂ vn2 ⊂ zp ⊂ yp ⊂ gd ⊂ data
🕪 Off 🔾 Family 🖲 Wave 🗹 Clip   🍢 🐗 Append 🧧 🍪   🚍
Key 🖉 🗶 156.6E-12
7 8 9 /
4 5 6 *
1 2 3 -
0 ± . +
Stack ØX
delay(?wfl clipX(v("/InputNet" ?result "tran") 88.28E-9 33.79E-9 ), ?value1 2.5, ?edge1 "rising", ?nth1 1, ?td1 0.0, ?wf2 clipX(v("/N1" ?result "tran") 88.28E-9 33.79E-9 ), ?value2 2.5, ?edge2 "failing", ?nth2 1, ?td2 0.0, ?stop nil, ?multiple nil) clipX(v("/InputNet" ?result "tran") 88.28E-9 33.79E-9 ) clipX(v("/N1" ?result "tran") 88.28E-9 33.79E-9 )
Function Panel
Special Functions
PN d2a fallTime harmonicFreq peak pzfilter spectrumMeas a2d dBm flip histo peakToPeak riseTime stddev
abs_jitter delay fourEval linteg period_jitter ms tangent
bandwidth dft freq_jitter intersect phaseNoise root unityGainFreq
compare dnl gainBwProd ipnVRI prms sample xmax
compression outycycle gainwargin loadpuli psd settiing ime xmin compressionVRI evmGAM getAsciiWave Ishift psdbb slewRate xval
convolve evmQpsk groupDelay overshoot pstddev spectralPower ymax cross eyeDiagram harmonic pavg pzbode spectrum ymin
Function Panel Expression Editor Memories
8

# **Integrated Circuit Design CAD Tool Information**

**m.** The image below shows the zoomed-in section of a single transition. The input waveform is a rising edge (InputNet in this case), and the output waveform is a falling edge (N1 in this case). You can highlight both waveforms by holding the shift key and clicking on the two waveforms. This makes it easier to see whether the rise time of the InputNet is equal to the fall time of the output net (N1 in this case) and thus, the extent to which the inverter is balanced.



# **Integrated Circuit Design CAD Tool Information**

- **n.** Now you are going to measure the delay of the high-to-low transition for these two signals (tpHL).
- **o.** First, you can clear the 'Evaluate' buffer and clear the stack (clst) as shown in the image below.

W Virtuoso (R) Visualization & Analysis XL calculator	_ 🗆 🗙
Eile <u>T</u> ools <u>V</u> iew <u>O</u> ptions <u>C</u> onstants <u>H</u> elp	cādence
In Context Results DB: /home/afiten3/SOCHE/kmantell/cadence/ncsu-cdk-1.6.0.beta/ringoscillator_test/spectre/schematic/psf	
Ovt       Ovf       Ovdc       Ovs       O op       O var       O vn       O sp       O vswr       O hp       O zm         O it       O if       O is       O opt       O mp       O vn2       O zp       O yp       O gd       O data	
📗 Off O Family 🖲 Wave 🗹 Clip   🍢 🚛 Append 🔡 🍪   🗮	
Key         Image: Second	
0 ± . + A D 🗈 🔐 B9 🛍 8 🕷 🎬 ME 🖊 ME 🥠 🦿	
Stack	ē ×
Function Panel	e ×
Special Functions	
PN       d2a       fallTime       harmonicFreq       peak       pzfilter       spectrumMeas         a2d       dBm       flip       histo       peakToPeak       riseTime       stddev         abs_jitter       delay       fourEval       iinteg       period_jitter       rms       tangent         average       deriv       freq_integ       phaseMargin       msNoise       thd         bandwidth       dft       frequency       intersect       phaseNoise       root       unityGainFreq         clip       dftbb       frequency       ipnVRI       prms       sample       xmax         compression       dutyCycle       gainMargin       loadpull       psd       settlingTime       xmin         convolve       evmQpsk       groupDelay       overshoot       pstddev       xpectrum ymax         cross       eyeDiagram       harmonic       pavg       pzbode       spectrum ymin	
Function Panel Expression Editor Memories	
8	

# **Integrated Circuit Design CAD Tool Information**

- **p.** You will execute similar steps in this part of the exercise with the calculator.
- **q.** First make sure that your waveforms look like the ones shown in the Visualization & Analysis window (the same as for the previous set of steps to obtain the delay tpLH).



# **Integrated Circuit Design CAD Tool Information**

r. Now click on the 'Wave' radio button in the calculator window. Then click on the output waveform (the waveform with the low to high transition, in this case, N1) in the Visualization & Analysis XL window. (Be sure not to click on the wave name on the left-hand side; click instead on the waveform itself).



#### **Integrated Circuit Design CAD Tool Information**

**s.** A wave name should appear in the calculator window as shown in the image below. As before, this image shows the wave name "N1" in the window. The syntax of the statement in the window, 'clipX,' refers to the zoomed-in portion of the waveform that you are displaying in the waveform window. The syntax of the two values in blue at the end of the statement refer to the start time and to end time of the zoomed-in portion of the viewing window that you selected in the Visualization & Analysis XL window.

W Virtuoso (R) Visualization & Analysis XL calculator	_ <b>_ X</b>
Eile <u>T</u> ools <u>V</u> iew <u>O</u> ptions <u>C</u> onstants <u>H</u> elp	cādence
In Context Results DB: /home/afiten3/SOCHE/kmantell/cadence/ncsu-cdk-1.6.0.beta/ringoscillator_test/spectre/schematic/psf	
• vt         • vf         • vdc         • vs         • op         • var         • vn         • sp         • vswr         • hp         • zm           • it         • if         • idc         • is         • opt         • mp         • vn2         • zp         • yp         • gd         • data	
🛛 Off O Family 💿 Wave 🔽 Clip   🛼 🖏 Append 🔤 🍪   🗄	
Key         Image: Clipx w("/N1" ?result "tran") 126.9E-9 132.4E-9           7         8         9         /           4         5         6         *           1         2         3         -	
0 ± . + • 🞝 🗈 📴 🛍   🕬 🕸   🕬 Me / 🏪   6 %	
Stack	Ð×
Function Panel	ð×
Special Functions	
PN       d2a       fallTime       harmonicFreq       peak       pzfilter       spectrumMeas         a2d       dBm       flip       histo       peakToPeak       riseTime       stddev         abs_jitter       delay       fourEval       iinteg       period_jitter       rms       tangent         average       deriv       freq       iinteg       phaseMargin       rmsNoise       thd         bandwidth       dft       freq_iitter       intersect       phaseNoise       root       unityGainFreq         clip       dtbb       frequency       ipn       pow       rshift       value         compare       dnl       gainBwProd       ipn/Rin       prms       sample       xmax         compression/VRI       evmQAM       getAscilWave       Ishift       psdbb       slewRate       xval         convolve       evmQApsk       groupDelay       overshoot       psdbdv       spectralPower       ymax         cross       eyeDiagram       harmonic       pavg       pzbode       spectrum       ymin	
Function Panel Expression Editor Memories	
8 8	

# **Integrated Circuit Design CAD Tool Information**

t. Now click on the input waveform. Be sure not to click on the name of the waveform on the left-hand side of the window. You are selecting the first falling edge of this waveform, and it is edge 1 (in the zoomed-in portion of the waveform that you display in the window).



#### **Integrated Circuit Design CAD Tool Information**

**u.** Now check in the calculator to verify that the name of the first waveform (N1 in the case shown) has been pushed into the stack and brings the name of the input waveform into the calculator (InputNet in the case shown). Important: Note that the waveforms were entered in reverse order (the late first; then the early one); this is a feature of the stack operation of the calculator.

W Virtuoso (R) Visualization & Analysis XL calculator	_ <b>_ X</b>
Eile <u>T</u> ools <u>V</u> iew <u>O</u> ptions <u>C</u> onstants <u>H</u> elp	cādence
In Context Results DB: /home/afiten3/SOCHE/kmantell/cadence/ncsu-cdk-1.6.0.beta/ringoscillator_test/spectre/schematic/psf	
ort orf ordc ors op oran orn orn orn orn orn orn orn orn orn or	
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Key         Image: Clipx w("/InputNet" ?result "tran") 126.9E-9 132.4E-9           7         8         7           4         5         6           1         2         2	
0 ± . + • 📮 🛅 🎇 🙀 🕸 🗰 🦛 🏧 ME 🚰 ME	
Stack	ē ×
ClipX(v("/N1" ?result "tran") 126.9E-9 132.4E-9 )         Co         Co         Co         Co         Co	
Function Panel	ð ×
Special Functions 🧧 🔍	
PN       d2a       fallTime       harmonicFreq       peakToPeak       pzfilter       spectrumMeas         a2d       dBm       flip       histo       peakToPeak       riseTime       stdev         abs_jitter       delay       fourEval       intreg       period_jitter       msetmest       tadev         average       deriv       freq       integ       phaseMargin       msNoise       thd         bandwidth       dft       freq_jitter       intersect       phaseMargin       msNoise       thd         clip       dftbb       frequency       ipn       pow       rshift       value         compare       dnl       gainBwProd       ipn/VRI       prms       sample       xmin         compressionVRI       evmQAM       getAsciiWave       Ishdft       psdbb       slewRate       xval         convolve       evmQAM       getAsciiWave       Ishdft       psdbd       spectralPower ymax         cross       eyeDiagram       harmonic       pavg       pzbde       spectrum       ymin	
Function Panel Expression Editor Memories	_
8 8	

#### **Integrated Circuit Design CAD Tool Information**

v. Now move the cursor to 'Special Functions' in the calculator window. Select 'delay'. Fill 2.5 as the threshold values (50% of Vdd = 2.5V since Vdd = 5V). Notice that in the 'delay' section, the name of your first waveform (N1 in this case) is listed as 'Signal2,' and the name of your second waveform (InputNet in this case) is listed as 'Signal1'. For Signal1, set the Edge Number equal to 1. For Signal2, set the Edge Number equal to 1. For Signal2, set the Edge Number equal to 1. For Signal 2, set the Edge Type 2 to 'rising.' Then click 'OK.'



# **Integrated Circuit Design CAD Tool Information**

**w.** Notice the change in the calculator window. The entry has now been expanded to show the delay calculation expression.

Eile Tools View Options Constants Help Cadence						
In Context Results DB: /home/afiten3/SOCHE/kmantell/cadence/ncsu-cdk-1.6.0.beta/ringoscillator_test/spectre/schematic/psf						
Ovt       Ovf       Ovc       Ovs       Opp       Ovar       Ovn       Osp       Ovswr       Ohp       T         Oit       Oif       Oid       Osp       Ovar       Ovn       Osp       Ovswr       Ohp       T         Oit       Oif       Oisp       Ovar       Ovn       Osp       Ovswr       Ohp       T						
💭 Off O Family 🖲 Wave 🔽 Clip   🍌 🚛 Append 🔽 🦃 🔚						
Key       All       All       Comparison       Comp						
0 ± . + + 🞝 🛅 🔐 🛤 🛤 🏁 🎬 ME 🚰 ME						
Stack 8 ×						
ClipX(v("/inputNet" ?result "tran") 88.28E-9 93.79E-9 )						
CipX(V(7N1**?result tran*) 66.26E-9 33.73E-9 )						
mg						
Function Panel 8 ×						
Special Functions						
PN       d2a       fallTime       harmonicFreq       peak       pzfilter       spectrumiMeas         a2d       dBm       flip       histo       peakToPeak       riseTime       stoPiak         abs_jitter       delay       fourEval       iinleg       period_jitter       ms       tangent         average       deriv       freq       integ       phaseMargin       msNoise       thd         bandwidth       df       freq_iency       ipn       pow       rshift       value         compare       dnl       gainBwProd       ipnVRI       prms       sample       xmax         compression       dutyCycle       gainMargin       loadpull       psd       settlingTime       xmin         convolve       evmQAM       getAsctiWave       tshift       spectruPower ymax         cross       eyeDiagram       harmonic       pavg       pzbode       spectrum       ymin						
Function Panel Expression Editor Memories						
expression evaluation failed: delay(?wf1 clipX(v("/InputNet" ?result "tran") 58.02E-9 58.74E-9 ), ?value1 2.5, ?edge1 "falling", ?nth1 1, ?td1 0.0, ?wf2 clipX(v("/N1" ?result "tran") 58.02E-9 58.74t						

#### **Integrated Circuit Design CAD Tool Information**

**x.** Now click on the 'Evaluate' buffer (the icon to the left of 'Append' pulldown), and you will see a value for the falling delay (tpHL) for the inverter (in the ring oscillator). In the image below, the result of the delay calculation shows that the rising delay for edge 1 is 83.83 ps.

W Virtuoso (R) Visualization & Analysis XL calculator	
Eile <u>T</u> ools <u>V</u> iew <u>O</u> ptions <u>C</u> onstants <u>H</u> elp	cādence
In Context Results DB: /home/afiten3/SOCHE/kmantell/cadence/ncsu-cdk-1.6.0.beta/ringoscillator_test/spectre/schematic/psf	
ovt ovf ovdc ovs op ovar ovn osp ovswr ohp ozm it oif oidc ois opt omp ovn2 ozp oyp ogd odata	
📗 Off 🔾 Family 🖲 Wave 🖳 Clip   🏹 🐗 Append 🔡 🍪   🗐	
Key <b>B</b> X 83.83E-12	
7 8 9 /	
4 5 6 *	
1 2 3 -	
0 ± . + • 2 🗈 🔛 🕸 🛍 🕬 🛍 🕬 M M M	
Stack	Ð×
delay(?vrf1 clipX(v("/InputNet" ?result "tran") 88.28E-9 93.79E-9 ), ?value1 2.5, ?edge1 "falling", ?nth1 1, ?td1 0.0, ?vrf2 clipX(v("/N1" ?result "tran") 88.28E-9 93.79E-9 ), ?value1 2.5, ?edge1 "falling", ?nth1 1, ?td1 0.0, ?vrf2 clipX(v("/N1" ?result "tran") 88.28E-9 93.79E-9 ), clipX(v("/N1" ?result "tran") 88.28E-9 93.79E-9 )         Image: clipX(v("/N1" ?result "tran") 88.28E-9 93.79E-9 )	7value2 2.5,
Function Panel	
Special Functions	
PN       d2a       fallTime       harmonicFreq       peak       pzfilter       spectrumMeas         a2d       dBm       flip       histo       peakToPeak       riseTime       stddev         abs_jitter       delay       fourEval       iinteg       period_jitter       rms       tangent         average       deriv       freq_integ       phaseMargin       msNoise       thd         bandwidth       dft       frequency       intersect       phaseNoise       root       unityGainFreq         clip       dtbb       frequency       ipn VRI       prms       sample       xmax         compression       dutyCycle       gainMargin       loadpull       psd       settlingTime       xmin         compressionVRI       evmQAM       getAsciiWave       Ishift       psdbb       slewRate       xval         convolve       evmQpsk       groupDelay       overshoot       pzbddev       spectrum       ymin	
Function Panel Expression Editor Memories Successful evaluation	
8	

# **Integrated Circuit Design CAD Tool Information**

**y.** The image below shows the zoomed-in section of a single transition. The input waveform is a falling edge (InputNet in this case), and the output waveform is a rising edge (N1 in this case). You can highlight both waveforms by holding the shift key and clicking on the two waveforms. This makes it easier to see whether the fall time of the InputNet is equal to the rise time of the output net (N1 in this case) and thus, the extent to which the inverter is balanced for this transition.



# **Integrated Circuit Design CAD Tool Information**

- **z.** You can also measure the period of this ring oscillator.
- **aa.** You have now learned to use the calculator using your simulation of a ring oscillator.

# **Integrated Circuit Design CAD Tool Information**

# 27. Parameterized Inverter Chain: Delay of Inverter Chain

**a.** In this section, you are going to create a hierarchical schematic at the logic gate level by using symbols that represent lower-level schematics. When you create a hierarchical schematic, it may be necessary to use different gates that represent the same logic but have different transistor sizes (e.g. a 'weak' inverter and a 'strong' inverter) and different corresponding power levels. It is also desirable at times to be able to move easily from one technology to another (e.g., from 0.6 microns to 0.25 microns). In these cases, it is helpful to parameterize the sizes of the transistors in the schematics.

In this section, you will start with the schematic and symbol for the inverter that you created in a previous section (inv). You may want to review the previous sections and refresh your memory.

First, copy the existing inverter cell to four other cells named invx1, invx4, invx16, and Loadx64, respectively. These cells will be parameterized inverters; specifically, the cells will be a parameterized inverter with minimum size (x1), four times the minimum (x4), 16 times the minimum (x16), and a fixed load 64 times the minimum.

In order to copy the cells, first click on the 'EENG653' library, then on the inverter cell (such that they become highlighted). Then select 'Edit  $\rightarrow$  Copy,' and the 'Copy Cell' form will appear as shown in the image below. Complete the name of the new cell, as shown for the case of the 'invx1' cell. Make sure that 'Copy All Views' is selected. (If your inverter were to have contained additional schematics, then it would be important to select 'Copy Hierarchical' as well).

In this way, you should copy four more inverter cells in the 'EENG653' library (you could have also copied the cell into a different library.)

# **Integrated Circuit Design CAD Tool Information**

		Copy Cell	(
- From			
Library	EENG653		
Cell	inv		
То			
Library	EENG653		
Cell	invx1		
Options			
Copy	/ Hierarchical		
<b>V</b>	Skip Libraries	NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03d NCSU_TechLib_tsmc04_4M2P avTech (=)	
	Exact Hierarchy	basic cdsDefTechLib megan	
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📃 Upda	ate Instances:	Of Entire Library	
Datab	ase Integrity		
🔲 Re	-reference custom'	ViaDefs	
Cł	neck existence in te	echnology database	
🔲 Add	To Category	Cells ×	
ОК	Apply	Cancel Help	

### **Integrated Circuit Design CAD Tool Information**

**b.** Open the EENG653 invx1 schematic (to review, one way to do this is to click on the Library Manager window and then double-click on the schematic view in this window). You will now change the properties of the nmos4 and pmos4 to become *parameterized*. Recall that to change the properties of the nmos4, you click on the device (highlight it), and type 'q' (the hotkey).

Edit the properties for the nmos4:

- 1. Set the Width to 'Width';
- 2. Set the Length to 'Length'.

Edit the properties for the pmos4:

- 1. Set the Width to 'a\*Width';
- 2. Set the Length to 'Length'.

Replace the VDD pin with an instance of the 'vdd' symbol from the 'basic' library. Replace the GND pin with an instance of the 'gnd' symbol from the 'basic' library. You will be setting the values for ground and power at the top level of the hierarchy (this practice is helpful for more complicated schematics).

# **Integrated Circuit Design CAD Tool Information**



Your schematic will look like the image shown below.

This image shows a parameterized inverter. You have parameterized the width and length of each transistor. In this case, you have parameterized the length of the nmos4 and length of the pmos4 with the parameter 'Length,' (default value is 0.6 microns), the width of the nmos4 with the parameter 'Width,' (e.g., 1.5 microns base size) and the width of the pmos4 with the parameter 'a\*Width.' Note that the 'a' is used to change the ratio of the pmos4 width to the nmos4 width: PMOS/NMOS ratio.

# **Integrated Circuit Design CAD Tool Information**

When you instantiate this inverter schematic in a hierarchical schematic, you will be able to:

- 1. Keep the default values;
- 2. Change the default values to migrate to a new technology (such as changing 'Length' to 0.25 microns for a 0.25 micron CMOS technology);
- 3. Change the transistor sizes to create different transistor strengths for different inverters.

#### **Integrated Circuit Design CAD Tool Information**

**c.** Create a symbol for the invx1 schematic. In the EENG653 invx1 schematic, select "Create  $\rightarrow$  Cellview  $\rightarrow$  From Cellview". The form "Cellview From Cellview" will appear as shown in the image below. Fill in the form with Cell Name 'invx1', From View Name as 'schematic', To View Name as 'symbol'. Then click OK.

The "Create Cellview" window will appear when the invx1 symbol already exists. You can select 'Modify' to use the previous symbol (where you will delete the VDD and GND pins with green lines) or you can select 'Replace' and start over with a fresh symbol.

	Cellview From Cellview	×
Library Name	EENG653	Browse
Cell Name	invx1	
From View Name To View Name Tool / Data Type	schematic 🔽 symbol schematicSymbol 🔽	
Display Cellview	⊻	
Edit Options		
	OK Cancel Defaults	Apply Help


## **Integrated Circuit Design CAD Tool Information**

**d.** The invx1 symbol will look like the image shown below.



#### **Integrated Circuit Design CAD Tool Information**

**e.** Run Check and Save on the invx1 schematic. When you run Check and Save, the CIW will report that the invx1 "Schematic check completed with no errors." If there are errors, correct the schematic and/or symbol and re-run Check and Save. Be sure that Check and Save completes with no errors, as shown in the image below.

C Virtuoso® 6.1.5-64b - Log: /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/CDS.19May2012.log	X
File <u>T</u> ools <u>Options</u> <u>H</u> elp	cādence
successful. start simulator if needed successful. simulate INFO (ADE-3071): Simulation completed successfully. reading simulation data successful.	
<pre>wire drawing -&gt; net: "IN3" bounding box: (2.25,-0.06) (2.50,-0.06) *WARNING* (GE-2067): geGetEditCellView: There is no graphical edit environment assigned to window(151) because the window is not Make sure that your current window is a valid graphic editor window. If it is a valid graph editor window, contact customer service to investigate this issue. *WARNING* (GE-2067): geGetEditCellView: There is no graphical edit environment assigned to window(151) because the window is not Make sure that your current window is a valid graphic editor window. If it is a valid graph editor window, contact customer service to investigate this issue. *WARNING* (GE-2067): geGetEditCellView: There is no graphical edit environment assigned to window(151) because the window is not Make sure that your current window, contact customer service to investigate this issue. *WARNING* (GE-2067): geGetEditCellView: There is no graphical edit environment assigned to window(151) because the window is not Make sure that your current window, contact customer service to investigate this issue. *WARNING* (GE-2067): geGetEditCellView: There is no graphical edit environment assigned to window(151) because the window is not Make sure that your current window, contact customer service to investigate this issue. *WARNING* GEPropEag: Bad Library ID. Getting schematic propert bag Getting schematic propert bag</pre>	a graphic edi a graphic edi a graphic edi
vdd (instance "IO", library "basic") INFO (SCH-1170): Extracting "invxl schematic" INFO (SCH-1426): Schematic check completed with no errors. Getting schematic propert bagGetting schematic propert bagINFO (SCH-1181): "EENG653 invxl schematic" saved.	
Immouse L: showClickInto()         M: schHiMousePopUp()         R: sch           1         >	IHIMousePopUp()

## **Integrated Circuit Design CAD Tool Information**

**f.** Now you will *parameterize* the width and length for your additional inverters: invx4, invx16, and Loadx64.

#### Parameterizing transistor widths

For each inverter, change the length of each pmos4 and each nmos4 to the parameter 'Length'. Setting the length of each device to 'Length' is standard practice for the case of digital design in which transistor lengths are set to the minimum value (in this case, 0.6 microns) in order to achieve high performance.

## Parameterizing transistor lengths

For each inverter, set the widths according to the following:

- 1. invx4
  - a. pmos4 width: 'a\*b\*Width'
  - b. nmos4 width: 'b\*Width'
- 2. invx16
  - a. pmos4 width: 'a\*b\*b\*Width'
  - b. nmos4 width: 'b\*b\*Width'
- 3. Loadx64
  - a. pmos4 width: 'a\*c\*Width'
  - b. nmos4 width: 'c\*Width'

Notice that invx4 and invx16 are parameterized twice (with 'a' and 'b'). Notice that Loadx64 is parameterized twice (with 'a' and 'c') and is kept independent of parameter 'b' in order to compare the results of different choices of sizes for invx4 and invx16 when the inverter chain drives a fixed load (default value for 'c' is c = 64).

#### **Integrated Circuit Design CAD Tool Information**

For each of these inverters, replace the VDD pin with an instance of the 'vdd' symbol from the 'basic' library. Replace the GND pin with an instance of the 'gnd' symbol from the 'basic' library. You will be setting the values for ground and power at the top level of the hierarchy (this practice is helpful for complicated schematics).

Create a symbol for each inverter. Save the inverter symbol.

Check and Save each inverter. Make sure that the CIW reports that the Check and Save completed successfully.

## **Integrated Circuit Design CAD Tool Information**





## **Integrated Circuit Design CAD Tool Information**

**h.** The image below shows the invx4 symbol.



## **Integrated Circuit Design CAD Tool Information**



i. The image below shows the invx16 schematic.

## **Integrated Circuit Design CAD Tool Information**

**j.** The image below shows the invx16 symbol.



## **Integrated Circuit Design CAD Tool Information**



**k.** The image below shows the Loadx64 schematic.

## **Integrated Circuit Design CAD Tool Information**

₹-		Virtuo	so®	Sym	bol E	dito	r L Ed	liting:	EENG	553 Lo	adx64	symbo	ol				
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94(159) Delete																	Cmd: Sel: 0 📕

**I.** The image below shows the Loadx64 symbol.

#### **Integrated Circuit Design CAD Tool Information**

**m.** Now you will edit each of the symbols that correspond to the four inverter schematics to indicate their different characteristics. This revision is not necessary but it is a good design practice. Recall that to open the symbol, you can click on the Library Manager and then double-click on the symbol view of the invx1 inverter.

Select 'Edit  $\rightarrow$  Properties  $\rightarrow$  Objects' and then click on the green text of the symbol itself. Type the name of the symbol; the symbol should change to reflect the change. Save the symbol.

For the case of the invx1 symbol, change the text to 'invx1'. The image of the invx1 symbol is shown below.



## **Integrated Circuit Design CAD Tool Information**

**n.** Change the names in the symbols of the other inverters. The image below shows the symbol of the invx4 inverter.



## **Integrated Circuit Design CAD Tool Information**



**o.** The image below shows the symbol of the invx16 inverter.

## **Integrated Circuit Design CAD Tool Information**



**p.** The image below shows the symbol of the Loadx64 inverter.

### **Integrated Circuit Design CAD Tool Information**

**q.** Now you are going to create a hierarchical schematic of an inverter chain. In the schematic of the inverter chain, you will instantiate one instance of an invx1, one instance of an invx4, one instance of an invx16, and one instance of a Loadx64 inverter.

You can call the new hierarchical schematic, 'InvDelay.' Open the Library Manager and highlight the 'EENG653' library. Select 'File  $\rightarrow$  New  $\rightarrow$  CellView,' and the 'New File' form will appear as shown in the image below. Complete the form as shown in the image. The Cell name will be 'InvDelay,' and the View name will be 'schematic.'

	New File 🗙
- File	
Library	EENG653
Cell	InvDelay
View	schematic
Туре	schematic 🔽
Application	
Open with	Schematics L
🔲 Always use thi	is application for this type of file
Library path file	
mzero/cadence/	ncsu-cdk-1.6.0.beta/cds.lib
	OK Cancel Help

Then click 'OK' on the form.

## **Integrated Circuit Design CAD Tool Information**

**r.** After clicking 'OK,' an 'EENG653' 'InvDelay' schematic window will appear as shown in the image below.



#### **Integrated Circuit Design CAD Tool Information**

**s.** In the 'EENG653' 'InvDelay' 'schematic' window, instantiate four cascaded inverters comprised of an invx1 (one instance), invx4 (one instance), invx16 (one instance), and Loadx64 (one instance). Use the Component Browser form as shown in the image below.

Component Brows _ 🗆 🗙
Commands <u>H</u> elp <b>cādence</b>
Library basic Flatten Filter * (Go up 1 level) noConn onPageConn patch simNameState simState
Misc
62 HelpAction

## **Integrated Circuit Design CAD Tool Information**

**t.** Create an instance of the power supply, vdc, and set the values as shown in the image below. Set the DC voltage to 5 V.

	Edit Object Properties	X
Apply To Only curr	ent 🔽 instance 🔽	
Show Show		
Browse	Reset Instance Labels Display	
Property	Value	Display
Library Name	NCSU_Analog_Parts	off 🔽
Cell Name	vdc	off 🔽
View Name	symbol	off 🔽
Instance Name	¥1	off 🔽
	Add Delete Modify	
User Property	Master Value Local Value	Display
lvslgnore	TRUE	off 🔽
CDF Parameter	Value	Display
AC magnitude		off 🔽
AC phase		off 🔽
DC voltage	5 V	off 🔽
Noise file name		off 🔽
Number of noise/freq pairs	0	off 🔽
Temperature coefficient 1		off 🔽
Temperature coefficient 2		off 🔽
Nominal temperature		off 🔽
OK Canc	el Apply Defaults Previous	Next Help

## **Integrated Circuit Design CAD Tool Information**

**u.** Create an image of the voltage pulse, vpulse in the schematic. Set the values of the pulse as shown in the image below. Set Voltage 2 = 5 V; Rise time to 400ps; Fall time to 400ps; Pulse width to 1.6ns; and Period to 4ns.

🗆 Ed	it Object Properties	×
Apply To Only current	instance	
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CDF Parameter	Value	Display
AC magnitude		off 🔽
AC phase		off 🔽
Voltage 1	0 4	off 🔽
Voltage 2	5 ¥	off 🔽
Delay time		off 🔽
Rise time	400p s	off 🔽
Fall time	400p s	off 🔽
Pulse width	1.6n s	off 🔽
Period	4n s	off 🔽
DC voltage		off 🔽
Noise file name		off 🔽
Number of noise/freq pairs	0	off 🔽
Temperature coefficient 1		off 🔽
Temperature coefficient 2		off 🔽
Nominal temperature		off 🔽
OK Cancel	Apply Defaults Previous	Next Help

## **Integrated Circuit Design CAD Tool Information**

**v.** Add a noConn symbol to terminate the Loadx64 (final inverter) as shown in the image below.

	Edit Object Properties	×
Apply To only curr Show Show	rent 🔽 instance 🔽 m ⊻ user ⊻ CDF	
Browse	Reset Instance Labels Display	
Property	Value	Display
Library Name	basic	off
Cell Name	noConn	off 🔽
View Name	symbol	off 🔽
Instance Name	I13	off 🔽
User Property nIAction	Add Delete Modify Master Value Local Value ignore	Display off
OK Cano	el Apply Defaults Previous 1	Next Help

## **Integrated Circuit Design CAD Tool Information**

**w.** Let's review the creation of this inverter chain.

So far, you have instantiated four inverters, the vpulse symbol, vdc symbol, and the noConn symbol.

Now connect the vdc to vdd (a symbol from the 'basic' library) and gnd (a symbol from the 'basic' library). Connect the terminals with wires (blue).

Connect the vpulse to gnd and to the net "IN1". Use wires and wire labels.

Connect the input port 'IN' to the input of invx1, and label the input net "IN1". Use wires and the labeling tool.

Connect the output of invx1 to the input of invx4 with a wire.

Connect the output of the invx4 to the input of invx16 with a wire.

Connect the output of invx16 to the input of Loadx64 with a wire.

Label the wire between invx1 and invx4 as 'IN2'.

Label the wire between invx4 and invx16 as 'IN3'.

Label the wire between invx16 and Loadx64 as 'OUT'.

Connect the output of invx16 to the output pin labeled "OUT".

Connect the output of the Loadx64 inverter to the noConn.

## **Integrated Circuit Design CAD Tool Information**

The schematic of the EENG653 InvDelay (inverter chain) will appear as shown in the image below.



## **Integrated Circuit Design CAD Tool Information**

**x.** You have now constructed a schematic of an inverter chain and need to assign values to the widths and lengths of each of the transistors in each inverters (sometimes this process is referred to as *sizing* the transistors).

In this example, you will investigate the delay of the inverter chain for the case in which the fanout is 4 (FO = 4); theoretically, you could have constructed an inverter chain composed entirely of the same inverter, with each inverter driving four different inverters (FO4). In this example, you will use the new parameterized inverters. To achieve an FO4 inverter chain, you will assume that each inverter drives an inverter for which (1) the nfet width is four times the width of the driving nfet, and (2) the pfet width is four times the width of the driving pfet.

This means that you can keep the first inverter at the base *size*, make the second inverter *four times the size* of the first inverter, make the third inverter *16 times larger* than the first inverter, and the fourth inverter *64 times larger* than the first inverter. We can accomplish *this sizing of the inverter chain* by setting the parameter b = 4.

Note that if you want to generate an inverter chain with a different sizing, you just need to change the value of the parameter b. You can do this easily because you have already defined the parameter b in each inverter.

#### **Integrated Circuit Design CAD Tool Information**

Before setting up the simulation of the inverter chain, you will learn one additional skill that is useful in your work with schematic entry. This skill is the ability to *traverse the schematic hierarchy*.

In order to traverse the schematic hierarchy *in Read mode*, click on the EENG653 InvDelay schematic, and then select "Edit  $\rightarrow$  Hierarchy  $\rightarrow$  Descend Read." Then click on the instance – such as the first inverter - in which you wish to descend (without the ability to edit).

In order to traverse the schematic hierarchy *in Edit mode*, click on the EENG653 InvDelay schematic, and then select "Edit  $\rightarrow$  Hierarchy  $\rightarrow$  Descend Edit." Then click on the instance in which you wish to descend (with the ability to edit).

## **Integrated Circuit Design CAD Tool Information**

**y.** Before you simulate the inverter chain, there are a couple comments about the use of four inverters in the chain. Specifically, you will use the InvDelay schematic to determine the optimum value of the pmos to nmos ratio (that is, the value of the parameter a) for a given value of the parameter b. In this example, you will set the parameter b = 4 (for this FO4 inverter chain).

In this example, the role of the first inverter is to generate an input waveform that is more realistic; that is, the rise time and fall time are more realistic than the rise time and fall time of a waveform that is a simple step or piecewise linear (as for the waveform that is generated by vpulse).

The last inverter (Loadx64) is used only as a load, in this example.

Note that you are strongly recommended to use this type of approach when you estimate delays through simulation; do not drive inputs directly because the results may be unrealistic.

The two remaining inverters (invx4 and invx16) are used in the inverter chain so that you can measure both tpLH and tpHL.

#### Integrated Circuit Design CAD Tool Information

**z.** Now you will simulate the inverter chain, InvDelay. Click on the EENG653 InvDelay schematic and select "Launch  $\rightarrow$  ADE L". The Virtuoso Analog Design Environment will appear showing the correct library (EENG653), cell name (InvDelay), and view name (schematic).

Setup the simulation for spectre by clicking on the ADE environment window with 'Setup  $\rightarrow$  Simulator/Directory/Host' and select spectre in the "Choosing Simulator/Directory/Host" window that appears.

Select the correct model libraries by clicking on the ADE environment window with 'Setup  $\rightarrow$  Model Libraries" and choosing the following two model libraries in the "spectre6: Model Library Setup" window that appears:

- 1. /apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m
- /apps/vlsi/ncsu-cdk 1.6.0.beta/models/spectre/nom/ami06P.m

Select the transient simulation type by clicking on the ADE environment window with 'Analyses  $\rightarrow$  Choose' and selecting 'tran' in the "Choosing Analyses" window. In this window, set the "Stop Time" to 8n (type 8n in the window). Select 'moderate' as the Accuracy default. Make sure there is a 'check mark' in the radio button next to the word 'Enabled.' Then click OK.

Select all outputs by clicking on the ADE environment window with 'Outputs  $\rightarrow$  Save Options' and select 'allpub', 'Save model parameters info', 'Save elements info', 'Save output parameters info', 'Save primitives parameters info', 'Save subckt parameters info', and set 'Output format' to 'psfxl'. Then click 'OK' on the form.

The next settings you will need to make are to set the values of the parameters a, b, c, Length, and Width.

#### **Integrated Circuit Design CAD Tool Information**

You can set the values of each parameter by clicking on the ADE environment window with 'Variables  $\rightarrow$  Edit', which will produce the 'Editing Design Variables' window as shown in the image below. In the 'Name' dialog box, enter a, and in the 'Value (Expr)' dialog box, enter 2. Then click the 'Add' button. The parameter a with value 2 will move to the right-hand side of the form as shown in the list below under the name 'Design Variables.'

Editing D	esign Variables Virtuoso	® Ar	nalog Desig	n Environmen 🗙
	Selected Variable	Des	ign Variables	
			Name	Value
Name		1 a		2
Value (Expr)				
Add Dele Next Cle	ar Find			
Cellview Variat	oles Copy From Copy To			
	OK Cancel Appl	DC	Apply & Run S	Simulation Help

#### **Integrated Circuit Design CAD Tool Information**

**aa.** You can now enter the values for the parameters b, c, Length, and Width. Set the value of the parameter b to 4, the value of the parameter c to 64, the value of the parameter Length to 0.6 microns (0.6u), and the value of the parameter Width to 1.5 microns (1.5u). The list of design variables will now appear as shown in the image below.

🗖 Editing D	esign Variables Virtuoso	8	Analog Desi	gn Environmen 🗙
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Next Cle	ar Find			
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	Copy Fiom Copy To			
	OK Cancel App	ly)	Apply & Run	Simulation Help

#### **Integrated Circuit Design CAD Tool Information**

**bb.** You are now ready to simulate. Look again at the Virtuoso Analog Design Environment window. The list of design variables will appear on the left-hand side of the window, as shown in the image below. Note that the window also shows that the type of analysis is 'tran' (it is enabled).

ABE L CTI			Virt	uoso®	Analog De	esign Envir	onment	t (7) - EEN	IG653 Inv	Delay	schematic		_	. DX
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27														
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79(136)	Calculat	or									Status:	Ready   T=27	C Simulator: sp	ectre

#### **Integrated Circuit Design CAD Tool Information**

**cc.** Generate a netlist for your InvDelay inverter chain by clicking on the Virtuoso ADE window and selecting "Simulation  $\rightarrow$  Netlist  $\rightarrow$  Generate Raw.' A netlist window will appear as shown in the image below (the input.scs file).

<u>c</u> /	me/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/ 💶 🗅	٢
Eib	Help cādence	
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1		1
160		

## **Integrated Circuit Design CAD Tool Information**

**dd.** Now you can run the simulation by clicking on the ADE window and selecting "Simulation  $\rightarrow$  Run." A run window will appear as shown in the image below (spectre.out file).

Elle         Help         cādence           Cadence (R) Virtuoso (R) Spectre (R) Circuit Simulator         Cadence (R) Virtuoso (R) Spectre (R) Circuit Simulator           Version 10.1.1.218.isr14 64bit 5 Sep 2011         Coopyright (C) 1989-2010 Codence Design Systems, Inc. All rights reserved worldwide. Cadence, Virtuoso and Protected by U.S. Patents:         A           Protected by U.S. Patents:         5.610.847; 5.790.436; 5.812.431; 5.859,785; 5.949.992; 5.967.238; 6.349,429; 6.544,852; 6.349,222; 6.374,330; 6.493,449; 6.514,856; 6.618,837; 6.635,839; 6.736,452,652; 7.035,782; 7.055,702; 7.055,700; 7.143,021; 7.493,240; 7,571.401.           Includes RSA BSAFE(R) Cryptographic or Security Protocol Software from RSA Security, Inc.         User: malanzero           User: malanzero         Host: Usifac01         Host: S015519         P11: 6000           Meanry available:         19.5416 0B         physical: 25.2792 0B         C90 Type: Intel(R) Xeon(R) CPU
Cadence (R) Virtuoso (R) Spectre (R) Circuit Simulator Version 10.1.2.218.isr14 64bit 5 Sep 2011 Copyright (D) 1989-2010 Cadence Design Systems. Inc. All rights reserved worldwide. Cadence, Virtuoso and Protected by U.S. Patents: 5.610, 847. 5.790, 436. 5.912, 431. 5.859, 785. 5.949, 992. 5.987, 238, 6.082, 522. 6.101, 323. 6.151, 638. 6.181, 754. 6.260, 176. 6.278, 964, 6.249, 522. 6.103, 325. 6.151, 639. 6.613, 754. 6.260, 176. 6.638, 639, 6.780, 625. 6.33, 338, 6.651, 097. 6.928, 626. 7.1024, 652. 7.035, 782, 7.085, 700, 7.143, 021. 7.493, 240, 7, 571, 401. Includes RSA BSAFE(R) Cryptographic or Security Protocol Software from RSA Security, Inc. User: mlanzero Host: vlsifac01 HostD: S0815619 PD: 6000 Memory available: 19.5416 0B physical: 25.2792 0B CPU Type: Intel(R) Xeon(R) CPU
Protected by U.S. Patents: S. 610, 847, 5. 700, 436; 5, 812, 431; 5, 859, 785; 5, 949, 992; 5, 987, 238; 6, 088, 523; 6, 101, 323; 6, 151, 589; 6, 181, 754, 6, 250, 176; 6, 279, 964; 6, 349, 472; 6, 514, 349; 6, 543, 4894; 6, 554, 4895; 6, 618, 373; 6, 636, 839; 6, 778, 025; 6, 832, 358; 6, 651, 097; 6, 928, 626; 7, 024, 652; 7, 035, 782; 7, 085, 700; 7, 143, 021; 7, 493, 240; 7, 571, 401. Includes RSA BSAFE(R) Cryptographic or Security Protocol Software from RSA Security, Inc. User: mlanzero Host: vlsifac01 HostID: S50815619 PID: 6000 Memory available: 19. 5416 08 physical: 25, 2792 08 CVD Type: Intel(R) Xeon(R) CVD X5650 08 2, 67018
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User: mlanzero Host: vlsifac01 HostII: 50815619 PID: 6000 Memory available: 19.5416 6B physical: 25.2792 6B CVU Type: Intel(R) Xeon(R) CVU - X5550 8 2.670Hz
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Time for NDB Parsing: CPU = 63.989 ms, elapsed = 243.045 ms. Time accumulated: CPU = 63.989 ms, elapsed = 243.045 ms. Peak resident memory used = 34.1 MDytes.
Time for Elaboration: CPU = 14.998 ms, elapsed = 66.2849 ms. Time accumulated: CPU = 78.987 ms, elapsed = 309.452 ms. Peak resident memory used = 37.8 Mbytes.
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Circuit inventory: nodes 6 bsin393 8 vsource 2
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#### **Integrated Circuit Design CAD Tool Information**

**ee.** Remember that each time you change the schematic, you will need to do a Check and Save. If there are no errors in your simulation (look at the CIW to verify that the simulation completed with no errors), you may visualize the simulation results. Since this is a transient analysis, you will inspect voltage waveforms.

To visualize the simulation results, click on the ADE window and select 'Results  $\rightarrow$  Direct Plot  $\rightarrow$  Transient Signal'. A Virtuoso Visualization & Analysis XL window will appear. Click on the InvDelay schematic and select the signals IN1, IN2, IN3, and OUT. Then type 'ESC'. The waveforms will appear as shown in the image below (select one to highlight it).



## **Integrated Circuit Design CAD Tool Information**

# 28. Parameterized Inverter Chain: More Use of the Calculator

**a.** You can now measure the tpLH and tpHL for the second and third inverters with signals IN2 and IN3 (recall that the role of the first inverter is to generate the realistic waveform, and the fourth inverter is the load). To do this accurately, you are going to use the waveform calculator (you can also save the waveforms in a table, as explained earlier).

To open the waveform calculator, click on the ADE window. Then select 'Tools  $\rightarrow$  Calculator' which will open the calculator as shown in the image below.

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151	

#### Integrated Circuit Design CAD Tool Information

**b.** Get familiarized with the waveform calculator (also discussed previously). The calculator works with a 'stack' in which you first input a waveform (or more than one waveform) and then perform an operation. After each operation, it is recommended that you clear the stack. To view the stack, you have to enable it (click on the button 'Display Stack').

Now click on 'wave' in the calculator window. The toggle button should be selected next to the word 'wave'.

Now click on the IN3 waveform in the Virtuoso Visualization and Analysis XL window. A wave will be displayed in the calculator window.

Now click on the IN2 waveform in the Virtuoso Visualization & Analysis XL window. The first wave (for IN3) will appear in the stack, and the IN2 wave will appear in the calculator window.

Note that you have entered the waves in reverse order (the later wave first, then the early wave); this is a feature of the stack operation of the calculator.

Now click on 'Special Functions' at the bottom of the calculator. Click on 'delay'. In the 'delay' form that appears, fill in 2.5 as the threshold values (since 50% of Vdd = 5 V is 2.5 V); Set 'Edge Number 1' to 1; Set 'Edge Number 2' to 1; Set 'Edge Type 1' to either; Set 'Edge Type 2' to either; Then click OK.

Notice the change in the calculator window. There will be a long expression.

Now click the icon for the 'Evaluate buffer', and you will see the value of approximately 224ps appear in the calculator window, which represents tpLH for the second inverter with a fanout of 4 (you measured the delay from IN2 to IN3 in a transition going from

#### **Integrated Circuit Design CAD Tool Information**

low to high). Notice that the value in the calculator window shown above is 224.4E-12 which represents 224.4ps.

**c.** Clear the 'Evaluate buffer' and the stack. Now measure the value of tpHL for the second inverter. You will follow the same steps as for the previous calculation (of tpLH), except that you will set 'Edge Number 1' to 2 and 'Edge Number 2' to 2. The value for tpHL is approximately 221ps; (for the case of the image below, tpHL is 220.9ps.)



#### **Integrated Circuit Design CAD Tool Information**

**d.** The value of tpHL is slightly less than the value of tpLH, as expected because of the difference between the mobility of the electron and the mobility of the hole (the carriers in the nmos and the pmos). What is the ratio of the mobility of the electron and the hole? What is the value of the parameter a? Which is larger? Although the simulation results may suggest that the value of the width of the pmos device may need to be increased even larger (to what value?), you only need to do this (that is, increase the value) if you are mainly interested in producing an inverter with a symmetric voltage transfer curve (VTC) and with equal values of tpHL and tpLH (that is, tpHL = tpLH). If you are interested in propagation delay (the average of tpHL and tpLH), you may actually want to make them less symmetric to gain speed.

**e.** You have now simulated an inverter chain with FO4.
# **Integrated Circuit Design CAD Tool Information**

# 29. Parameterized Inverter Chain: Parametric Analysis of the Delay of an Inverter Chain

**a.** You will now determine the optimal ratio of the pmos width to the nmos width through simulation. In order to obtain the optimal value of the ratio, you will perform multiple simulations with different values for a, and you will determine the fastest solution. It is possible to perform these simulations manually. In this section you will learn how to perform the simulations automatically in the Cadence software.

# **Integrated Circuit Design CAD Tool Information**

b. Click on the 'Virtuoso Analog Design Environment' window for the EENG653 InvDelay schematic and select 'Tools → Parametric Analysis.' The 'Parametric Analysis' window will appear as shown in the image below.

Parametric Analysis - spectre(6): EENG653 InvDelay schematic		
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# **Integrated Circuit Design CAD Tool Information**

**c.** In the 'Parametric Analysis' window, type 'a' in the 'Variable' column. Type '1' in the 'From' column; type '4' in the 'To' column; select 'Linear Steps,' and set 'Step Size' to '0.2' as shown in the image below.

Parametric Analysis - spectre	6): EENG653 InvDelay schematic	
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# **Integrated Circuit Design CAD Tool Information**

**d.** In the 'Parametric Analysis' window, select 'Analysis → Start.' The simulations of your inverter chain will start to run, as indicated in the run window of the 'Parametric Analysis' window below.

Parametric Analysis - spectre(6): EENG653 InvDelay schematic	
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Compose simulator input file successful. simulate 13 parametric simulations remaining. 162 Start All	T

# **Integrated Circuit Design CAD Tool Information**

**e.** The CIW will also report that the simulations are running, as shown in the image below.

C Virtuoso® 6.1.5-64b - Log: /home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/CDS.19May2012.log	_ 🗆 🗙
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#### **Integrated Circuit Design CAD Tool Information**

f. When the simulations are completed, you can plot the waveforms. In the Virtuoso Analog Design Environment window, select 'Results → Direct Plot → Transient Signal.' Then move your mouse to the window showing the EENG653 InvDelay schematic and click on the 'IN2' net and the 'OUT' net. These two nets will become dashed lines and will become highlighted, as shown in the image below.



# **Integrated Circuit Design CAD Tool Information**

**g.** Then click 'ESC' in the EENG653 InvDelay schematic, and the Virtuoso Visualization & Analysis XL window will appear showing the 'IN2' waveform and the 'OUT' waveform for the duration of the simulations as shown below (click on the 'IN2' waveform and the 'OUT' waveform to see the left-most keys indicating the simulations with different values of the parameter 'a'). The image below shows the 'IN2' waveform with a = 1.0 highlighted in a red dashed line; this is the fastest high-to-low transition (and slowest low-to-high transition). Note that the values of the delays are similar for a=1 to a=3.



# **Integrated Circuit Design CAD Tool Information**

**h.** The image below shows the 'IN2' waveform with a = 4.0 highlighted in a blue dashed line.



# **Integrated Circuit Design CAD Tool Information**

**i.** The image below shows the 'OUT' waveform with a = 1.0 highlighted in a pink dashed line.



# **Integrated Circuit Design CAD Tool Information**

**j.** The image below shows the 'OUT' waveform with a = 4.0 highlighted in a peach dashed line.



# **Integrated Circuit Design CAD Tool Information**

**k.** If you zoom in on the low-to-high transition of 'IN2', you will see that the fastest transition is the case for which a = 4. The slowest transition is the case for which a = 1 (see the next image).



# **Integrated Circuit Design CAD Tool Information**

I. The slowest low-to-high transition for 'IN2' is the case for which the width of the pmos device is equal to the width of the nmos device (a = 1).



# **Integrated Circuit Design CAD Tool Information**

**m.** The image below shows the 'OUT' waveform with the fastest low-tohigh transition, for which a = 2.2 highlighted in a purple dashed line.



#### **Integrated Circuit Design CAD Tool Information**

**n.** The image below shows the 'OUT' waveform with the slowest low-to-high transition with a = 1.0 highlighted in a pink dashed line.



#### **Integrated Circuit Design CAD Tool Information**

o. It is a good idea to save your state before exiting the simulator in case you would like to redo some of the simulations; with a saved state, you can start by loading the state that you saved previously. To save the state, click on the Virtuoso Analog Design Environment window and select 'Session → Save State.' Then input the name that you would like to use for the state and click 'OK' on the form. For example, you can set the 'Save As' field to 'state-InvDelay-schematic.'

30. The End.