PROBLEM 2.1

For the layout seen in fir. 2.27 sketch the cross sectional views at the places indicated. Is there a parasitic pn junction in the layout?If so, where?Is there a parasitic bipolar transistor?If so,where?

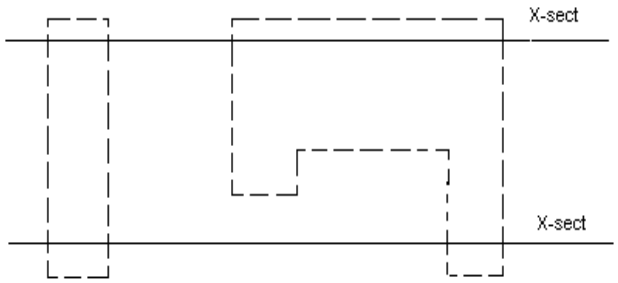
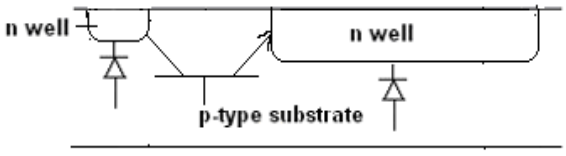
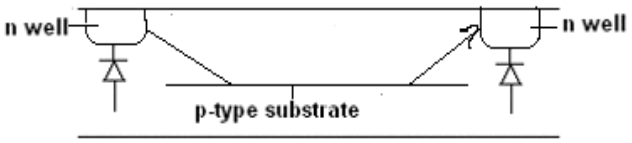


Figure 2.27 Layout used in problem 2.1

SOLUTION:

Cross-sectional view



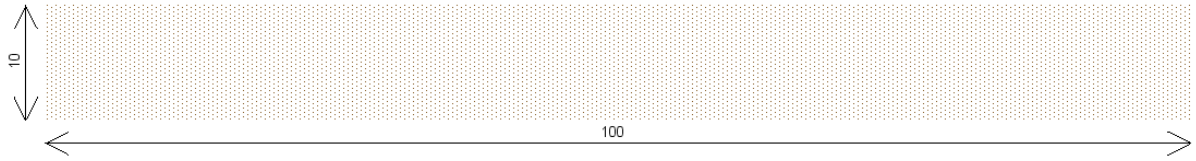


We have parasitic pn junctions and parasitic bipolar transistors.

Aruna Vadla

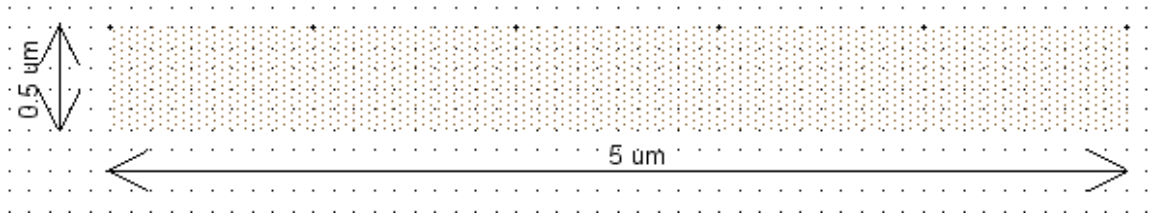
Problem (2.2): Sketch (or use a layout tool) the layout of an n-well box that measures 100 by 10. If the scale factor is 50 nm what is the actual size of the box after fabrication? What is the area before and after scaling ? Neglect lateral diffusion or any other fabrication imperfections.

Solution:
Layout of an n-well box that measures 100 by 10 is as below:



Scale factor = 50 nm,
So **actual size** of the box after fabrication = (100*50 nm) by (10*50 nm)
= 5 um by 0.5 um
Area of the box **before** scaling = 100 * 10 = 1000 sq. units
Area of the box **after** scaling = 5 um * 0.5 um = 2.5 (um^2)

Layout of an n-well box after scaling is as below:



Note: The distance between the two dark grids is 1um. So the n-well box size after scaling is 5 um by 0.5 um respectively.

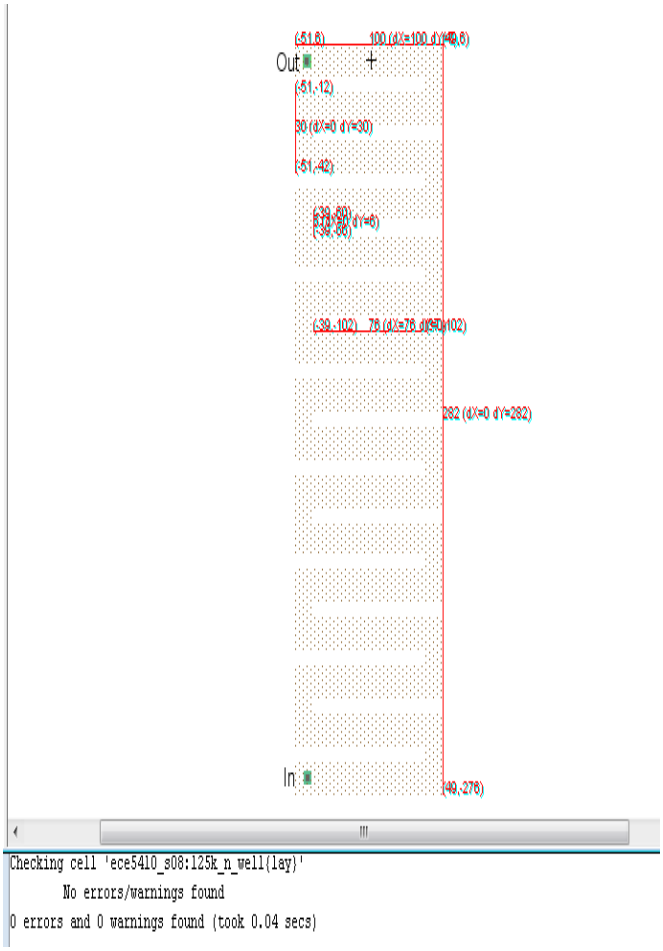
2.3 Lay out a nominally 250 kΩ resistor using the n-well in a serpentine pattern similar to what's seen in Fig. 2.28 Assume that the maximum length of a segment is 100 and the sheet resistance is 2kΩ/square. Design rule check the finished resistor. If the scale factor in the layout is 50nm, estimate the fabricated size of the resistor.

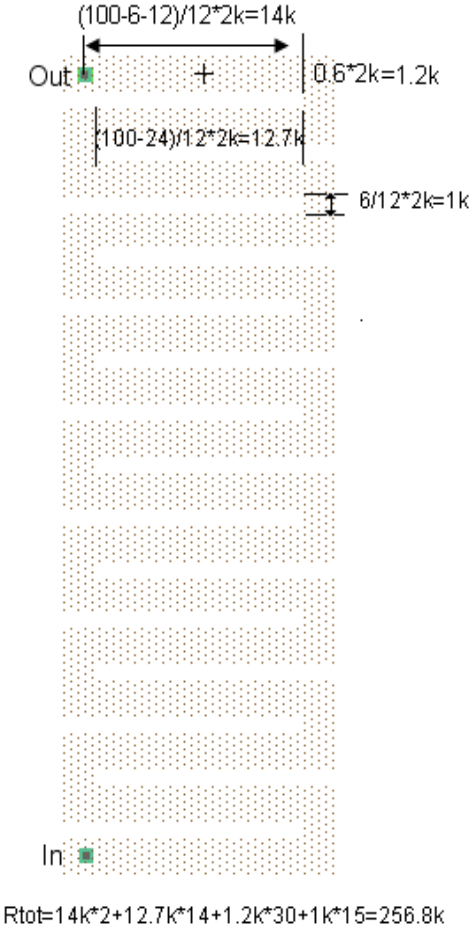
Solutions:

To begin with, we need to estimate how many segments with length of 100 are going to be used. Then space these segments with minimum distance specified by design rule (6 for N-well).

To lay out 250kΩ resistor, the number of single 100 segment with resistance of (100/12*2k=)16.7 kΩ are 250k/16.7k=15. (Minimum width for N-well is 12) Because the effective resistance for corners are only 0.6*2k, we need one more segment to compensate this loss.

The 250kΩ resistor using N-well material is laid out in Electric, and it passed the design rule check (DRC). Actual resistance for this N-well resistance is calculated on the right side of the figure below.





Assignment #3 Vinay Dindi

2.4) If the fabricated n-well depth, t, is 1um, then what are the minimum, typical, and maximum values of the n-well resistivity, *p*? Assume the measured sheet resistances (mimimum, typical and maximum) are 1.6, 2.0, and 2.2 kohm/square?

p=Sheet resistance[Rsq] * n-well depth
n-well depth = 1um

For Rsq=1.6kohm/sq, *p*=1.6k*1e-06= 1600 ohm um
For Rsq=2kohm/sq, *p*=2k*1e-06= 2000 ohm um
For Rsq=2.2kohm/sq, *p*=2.2k*1e-06= 2.200 ohm um

Problem 2.5

Question: Normally, the scale current of a pn junction is specified in terms of a scale current density, Js (A/ sq. m) and the width and length of a junction (i.e., Is = Js * L * W * scale * scale neglecting the side wall component). Estimate the scale current for the diode of Example 2.3 if Js = 1E-08 A per sq.m).

Solution: Is = Js * L * W * scale * scale
= (1E-08 A / sq m) * 100 * 100 * 1E-06 * 1E-06
= 1E -16 A.

Rahul Mhatre

2.6 Repeat problem 2.5 including the sidewall component ($I_s = J_s.L.W.scale^2 + J_s.(2L+2W).depth.scale$).

Solution

As seen in the problem statement, the equation for I_s is given as

$$I_s = Js.L.W.scale + J_s.\ (2L+2W).depth.scale^2 \qquad (2.3.1)$$

$$\text{Area component} = J_s.L.W.scale^2. \qquad (2.3.2)$$

$$\text{Perimeter component} = J_s.2.\ (L+W).\ depth.scale^2. \qquad (2.3.3)$$

Depth is given as 3um, Scale is 1um and J_s is 10^{-8} A/m^2. All we have to do is to calculate (2L+2W) for perimeter component and L.W for the area component. L and W are functions of layouts. Substituting all the length and width values in area components, we get,

L.W = 100*100
L.W = 1000 Grid units square.

Substituting the values of J_s, L.W and scale, in Equation (2.3.2), we get,

Area Component = 10^{-8} * 10000*10^{-12}
Area Component = 10^{-16} = 0.1fA

Substituting all the length and width values in perimeter components (Equation 2.3.3), we get,

2L + 2W = 200 + 200
2L + 2W = 400 Grid Units square.

Perimeter component = J_s * 400 * depth *scale.
Perimeter component = 10^{-8} * 400 * 3 * 10^{-6} * 10^{-6}
Perimeter component = 12 * 10^{-18} A.

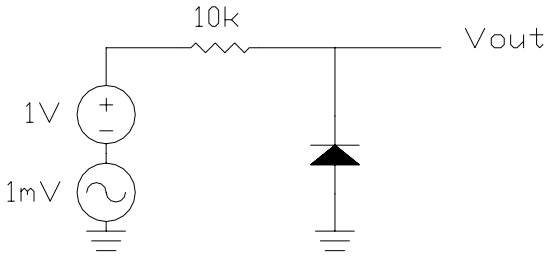
Therefore the total current is given as

I_s = Area component + Perimeter component
I_s = 0.1 fA +0.012 fA
I_s = 0.112 fA.

Justin Wood
EE 4/510
Problem 2.7

2.7) Using the diode of Example 2.3 in the circuit of Figure 2.29, estimate the frequency of the input signal when the AC component of Vout is 707μV (i.e. estimate the 3dB frequency of the $|\text{Vout/Vin}|$).

Figure 2.29



From Example 2.3

$$C_j = \frac{1.120\,pF}{(1-\left(\frac{V_D}{0.759}\right)^{0.33}}$$

$$V_D = -V_{OUT} \approx -1V - 0.000707V = -1.000707V$$

$$\therefore C_j = \frac{1.120\,pF}{(1-\left(\frac{-1.000707}{0.759}\right)^{0.33}} = 848\,fF$$

The transfer function is determined by using the voltage divider as shown below.

$$Vout = Vin\left(\frac{\frac{1}{j\omega C}}{R+\frac{1}{j\omega C}}\right)$$

$$\frac{Vout}{Vin} = \left(\frac{\frac{1}{j\omega C}}{R+\frac{1}{j\omega C}}\right)\left(\frac{j\omega C}{j\omega C}\right) = \frac{1}{j\omega CR+1}$$

$$Vout = Vin\left(\frac{\frac{1}{j\omega C}}{R+\frac{1}{j\omega C}}\right)$$

$$\frac{Vout}{Vin} = \left(\frac{\frac{1}{j\omega C}}{R+\frac{1}{j\omega C}}\right)\left(\frac{j\omega C}{j\omega C}\right) = \frac{1}{j\omega CR+1}$$

Substituting :

$Vout = 0.000707$

$Vin = 0.001$

$$\left|\frac{0.000707}{0.001}\right| = \left|\frac{1}{j\omega CR+1}\right|$$

$$0.707 = \left|\frac{1}{j\omega CR+1}\right|$$

$$\omega CR = 1$$

$$\omega = \frac{1}{CR} = \frac{1}{848e-15*10000} = 117924528 rad/s$$

$$f = \frac{\omega}{2\pi} = 18768271 Hz$$

or

$$-3dB = \left|\frac{Vout}{Vin}\right| = \left|\frac{1}{j\omega CR+1}\right|$$

$$-3dB = 20\log_{10} = \left|\frac{1}{j\omega CR+1}\right|$$

$$0.707 = \left|\frac{1}{j\omega CR+1}\right|$$

$$\omega CR = 1$$

$$\omega = \frac{1}{CR} = \frac{1}{848e-15*10000} = 117924528 rad/s$$

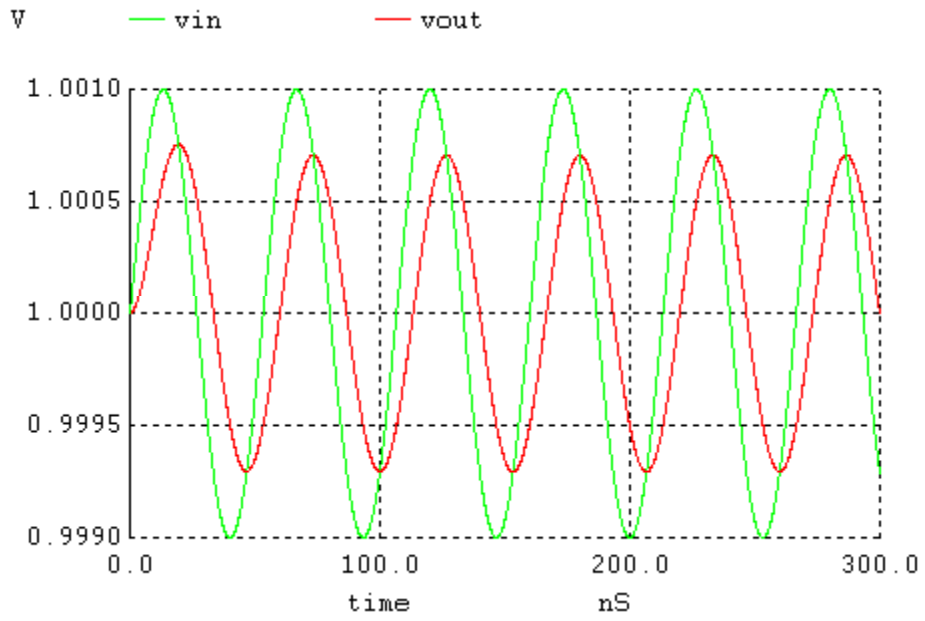
$$f = \frac{\omega}{2\pi} = 18768271 Hz$$

Rupa Balan

Q.2.8) Verify the answer given in problem 2.7 with SPICE.

The 3db frequency is approximately given by (1/2*pi*R*Cj).
From Ex 2.3 Cj0=1.12 pF
Cj (1V) = 0.8487 pF
Hence 3db frequency is approximately 18.76 MHz.
This frequency is used in the Spice netlist below
For WinSpice,
The netlist is

```
*** Question 2.8 ***
.control
destroy all
run
plot vout vin
.endc
D1 0 vout Dtrr
R1 vin vout 10k
Vin vin 0 DC 0 sin 1 1m 18.76meg
.Model Dtrr D is=1.0E-15 tt=10E-9 cj0=1.12E-12 vj=.759 m=0.33
.tran 100p 300n
.end
```



The waveforms for the transient analysis above are

As can be seen from Spice simulation, when frequency of input signal=18.76 MHz, vout varies from 1.000707V to 0.999293 V (i.e. ac component of vout varies from .000707V=707uv to -.000707V=- 707uv).
Hence 3 db frequency =18.76MHz.

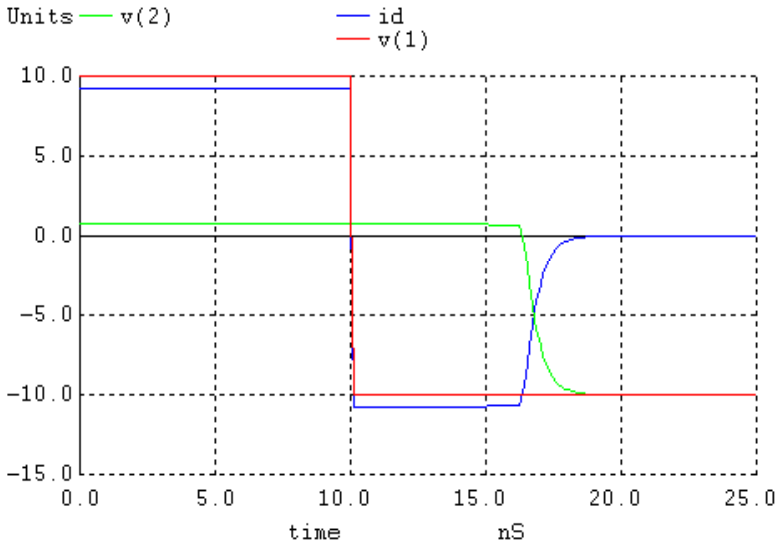
Problem 2.9.

Using SPICE, show that a diode can conduct from its cathode to its anode when the diode is forward biased.

Consider a circuit containing a resistance of 1k and a diode in series with a voltage source of pulse changing from +10v to –10v. The net list in winspice is shown below for this circuit. The graphs of the voltage across the diode V (2) and current are also shown below. A delay of 10ns is given to ensure equilibrium of the carriers in the diode. When the input voltage is suddenly changed to negative value, the diode cannot change its voltage immediately due to diffusion capacitance. But as the input voltage has changed its sign, the current through the resistor also changes accordingly while keeping the diode still in forward biased mode. The minority carriers in the diode diffuse to produce this reverse current. After they diffuse completely, the current becomes zero and then the diode is reverse biased. We can see in the graph that the diode is conducting current from cathode to anode (i.e. negative current) even though the diode is in forward mode between 10ns and 16ns.

Netlist

```
.control
destroy all
run
let id=-i(vin )*1k
plot v(1) v(2) id
.endc

D1 2 0 Dtrr
R1 1 2 1k
Vin 1 0 DC 0 pulse 10 -10 10n .1n .1n 20n 40n
.Model dtrr D is=1.0E-15 tt=10E-9 cjo=1E-12 vj=.7 m=0.33
.tran 100p 50n
.end
```



By Vehid Suljic

Problem 2.10

Estimate the delay through a 1 MEG resistor (10 by 2000) using the values given in Ex. 2.5. Verify the estimate with SPICE.

From Ex. 2.5 we have that (10 x 10) square's parameters are:

C = 5 fF and R = 5 kΩ and l = 2000/10 = 200

Now we can estimate the delay through the resistor,

$td = 0.35 \circ R \circ C \circ (l\text{^}2) \cong 350n\,\text{sec}$

Figure 1 shows WinSpice plot of Vin and Vout vs. time. From the plot we can see that our delay (Vout is at 50% of Vin = 500mV) is about 400 nsec which is close to what we calculated above.

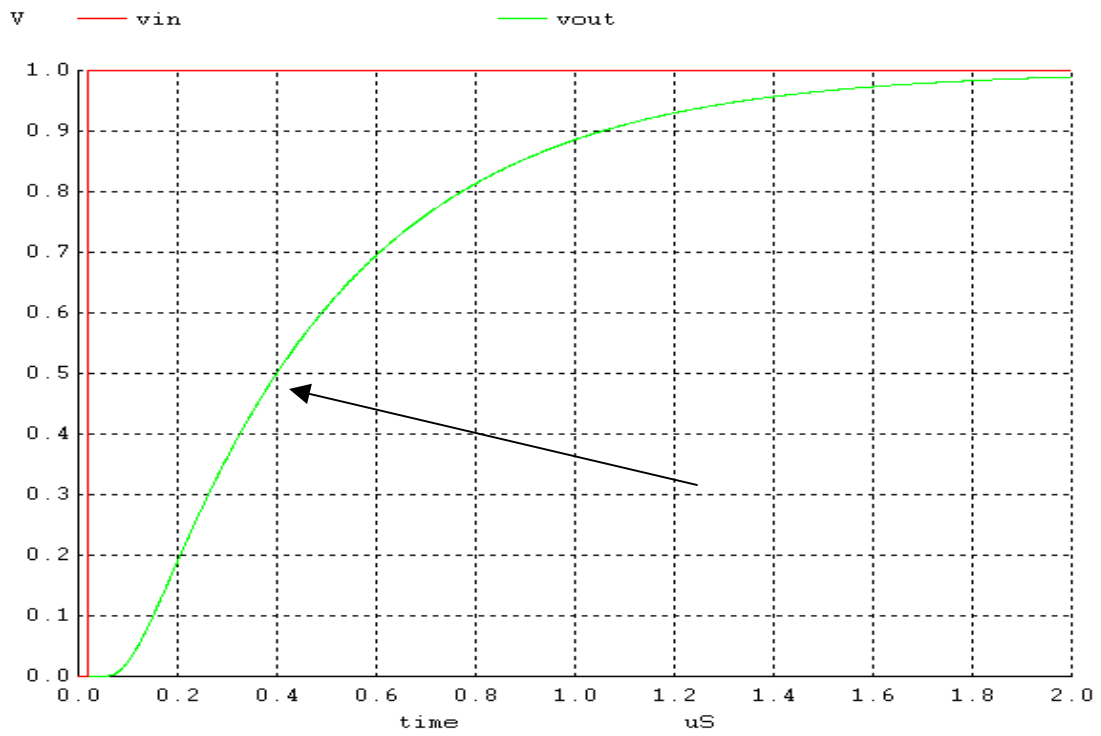


Figure 1. Spice simulation results for problem 2.10

*** Problem 2.10 top level netlist***

```
.control
destroy all
run
plot vin vout
.endc

.tran 1n 2u

O1      Vin     0       Vout    0       TRC
Rload   Vout    0       1G
Vin     vin     0       DC      0       pulse 0 1 20n 0

.model TRC    ltra      R=5k    C=5f    len=200

.end
```

Problem 2.11

Problem Statement:
If one end of the resistor in problem 2.10 is tied to +1V and the other end is tied to the substrate that is tied to ground, estimate the depletion capacitance (F/m^2) between the n-well and the substrate at the beginning, the middle, and the end of the resistor. Assume the resistance does not vary with position along the resistor and that the scale factor is 50nm, C_{jo}=25aF for a 10 by 10 square, m=.5, and V_{bi}=1.

Solution:

Cjo = 25aF per 10x10 square

A 10x10 square is: 10(50nm)x10(50nm) = $0.25(\mu m)^2$.

So $Cjo/m^2 = 25aF/0.25(\mu m)^2 = 100\mu F/m^2$

For V_d = 1V:

$$Cj = \frac{Cjo}{(1+ Vd/Vbi)^m}$$

$$Cj = \frac{100\mu F/m^2}{(1+ 1/1)^{.5}}$$

$$Cj = 70.7\mu F/m^2$$

For V_d = 0.5V:

$$Cj = \frac{Cjo}{(1+ Vd/Vbi)^m}$$

$$Cj = \frac{100\mu F/m^2}{(1+ 0.5/1)^{.5}}$$

$$Cj = 81.6\mu F/m^2$$

For V_d = 0V:

$$Cj = \frac{Cjo}{(1+ Vd/Vbi)^m}$$

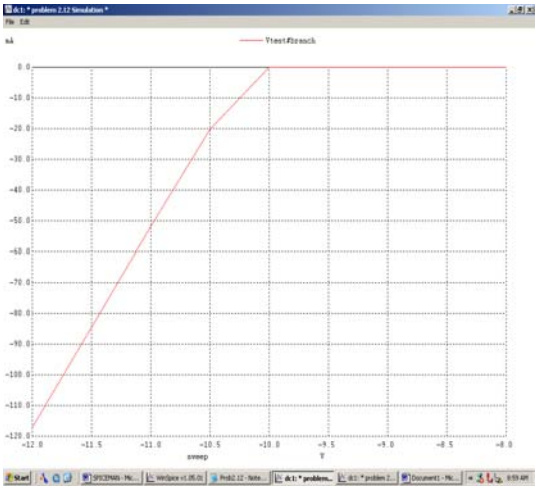
$$Cj = \frac{100\mu F/m^2}{(1+ 0/1)^{.5}}$$

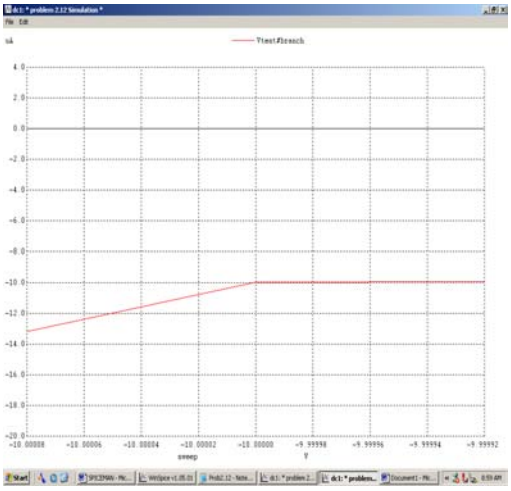
$$Cj = 100\mu F/m^2$$

2.12)
The Diode reverse breakdown voltage is the current that flows when $V_d < BV$ (breakdown voltage), is modeled in spice by
$I_D = IBV. e^{-(Vd+BV)/VT}$
Assuming 10μA of current flows when the junction starts to break down at 10V, simulate using spice DC sweep, the reverse breakdown characteristics of the diode.

//Netlist for Problem 2.12//

```
.control
destroy all
run
plot Vtest#branch
.endc

.DC Vin -8 -12 -0.5

Vin    1 0    DC 1 AC 0 0
R      1 2 15
D 3 0 DBreak
Vtest 2 3 0V

.Model DBreak D CJO=1E-12 BV=10 IBV=10E-6
.end
```





2.13 Repeat Ex 2.3 if the n-well/p-substrate diode is 50 square and the accepter doping concentration is changed to 10E15 atoms/cm3

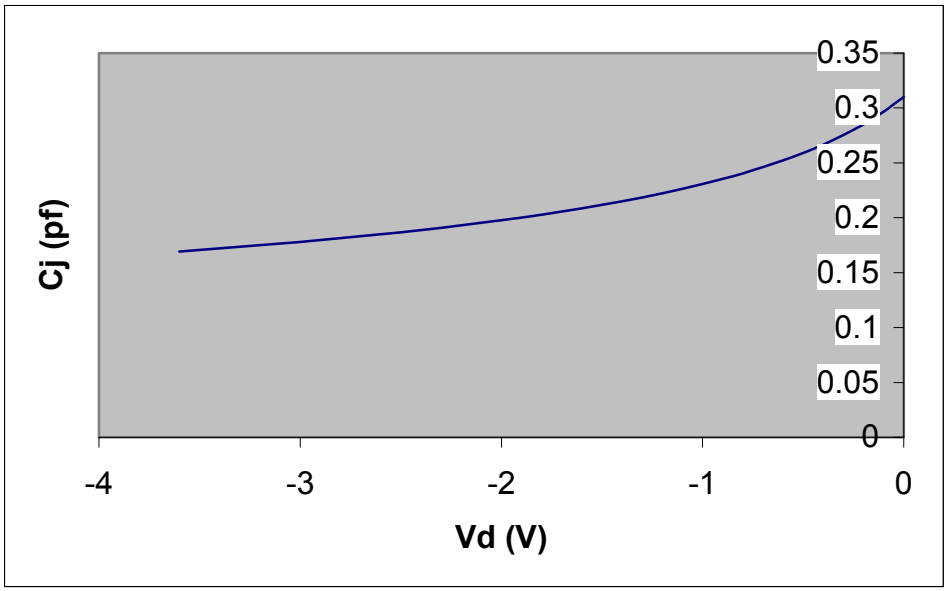
$$New V_{bi} = 26mV \ln \frac{10^{15} x 10^{17}}{(14.5x10^{9})^{2}} = 699mV$$

$$C_{j0b} = (100uF/um^{2})(1um^{2})(50)^{2} = 0.25pF$$

$$C_{j0s} = (100uF/um^{2})(1um^{2})3(4*50) = 60fF$$

$$Cj = \frac{0.25pF + 60fF}{(1 - \frac{V_d}{0.699})^{0.333}}$$

$$= \frac{0.31pF}{(1 - \frac{V_d}{0.699})^{0.333}}$$



KRISHNAMRAJU KURRA

2.14: Estimate the storage time, that is ,the time it takes to remove the stored charge ina diode, when T_T = 5 ns, V_F = 5V, V_R= -5V , C_{jo} = 0.5 pF and R = 1K. Verify the estimate using SPICE.

Given:

T_T = 5ns
V_F= 5V
V_R = -5V
C_{jo}= .5pF
R=1k

We have:

$t_s = T_T .\ln[(i_F-i_R)/(-i_R)]$

Where $i_F=V_F/R$ and $i_R=V_R/R$

Under forward bias the voltage drop across the diode = 0.7V

i_F = (5 - 0.7)/1K = 4.3 mA

When the diode is reversed biased, i_R= (-5-0.7)/1K = -5.7 mA

t_s = 5 ns . ln[(4.3 + 5.7)/ 5.7] = 2.81 ns

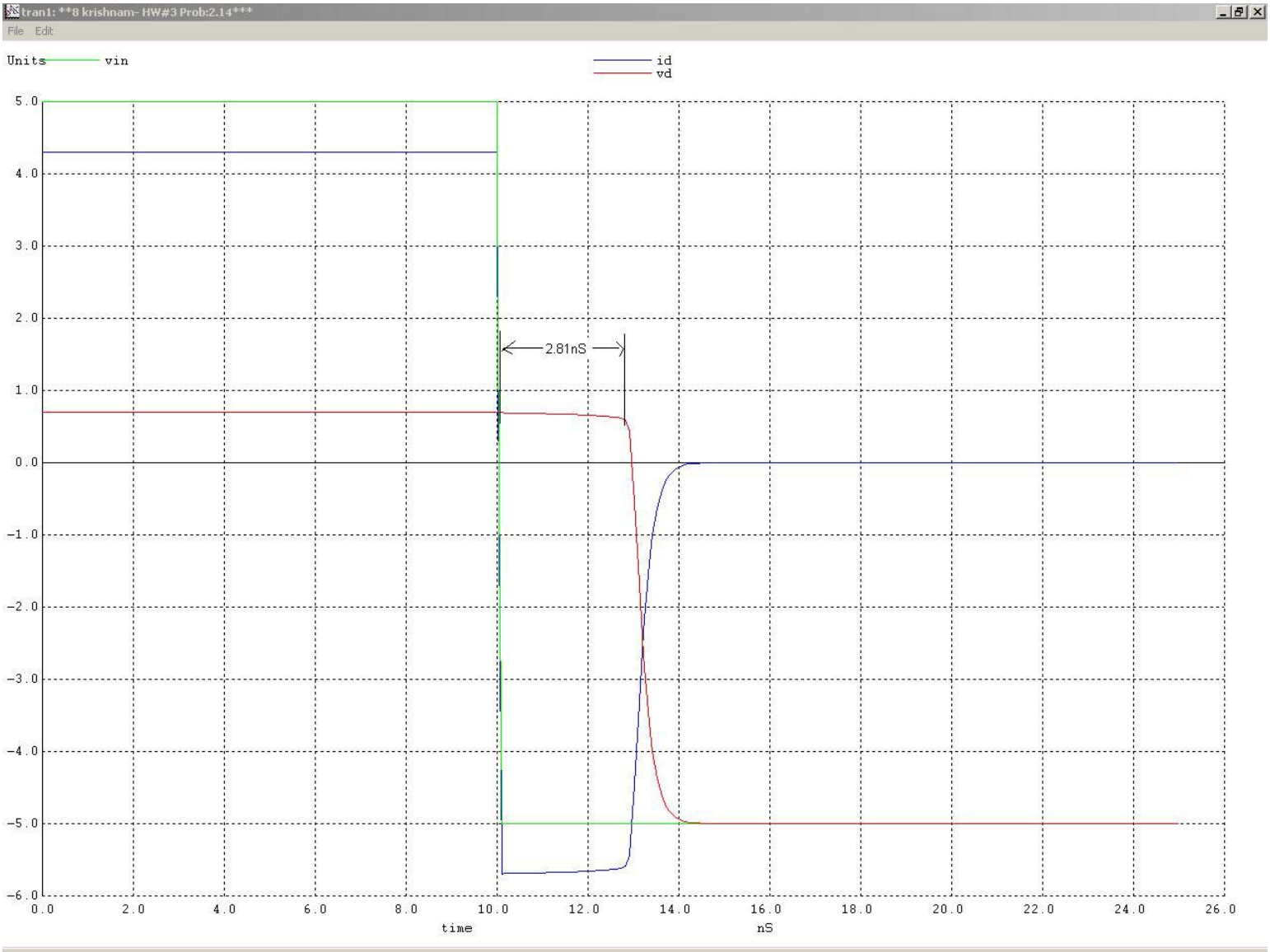
Therefore t_s = 2.81 ns

Verification using Winspice:

```
**8 krishnam- HW#3 Prob:2.14***

.control
destroy all
run
let id= -i(vin)*1k
plot vd vin id
.endc

.tran 100p 25n

D1      vd      0       dtrr
R1      Vin     vd      1k
Vin     vin     0       Dc      0       pulse 5 -5 10n .1n .1n 20n 40n
```

```
.Model Dtrr D tt=5E-9 cjo=5E-13
.end
```

Plot showing Vin, Vd, id:



Avani Falgun Trivedi

2.15 Repeat problem 2.14 if the resistor is increased to 10k. Comment on the difference in storage time between using a 1k and a 10k resistor. What dominates the increase the diode's reverse recovery time when using a 10k resistor instead of 1 1k resistor?

R=10k and from problem 2.14: $T_T = 5ns$, $V_F = 5V, V_R = -5V, C_{jo} = 0.5pF$

Diode storage time is $t_S = t_2 - t_1 = \tau_T \bullet \ln \frac{i_F - i_R}{-i_R}$ Where $\frac{V_F - 0.7}{R} = i_F$ and $\frac{V_R - 0.7}{R} = i_R$

Under forward bias condition, i_F = (5-0.7)/10k = 430uA

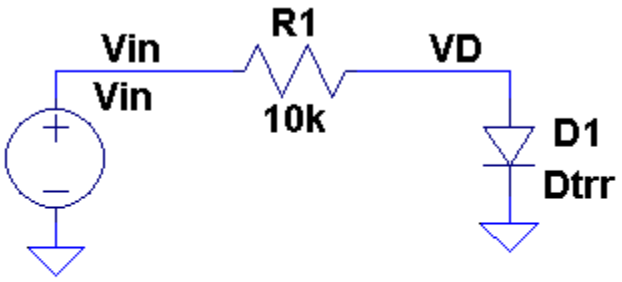
When diode is reverse biased, i_R = (-5-0.7)/10k = -570uA

Which gives diode storage time = t_S = 5 ns. ln [(430 + 570)/ 570] = 2.81ns

Diode storage time is the same when using 1k or 10k resistor value. It doesn't depend on resistor value.

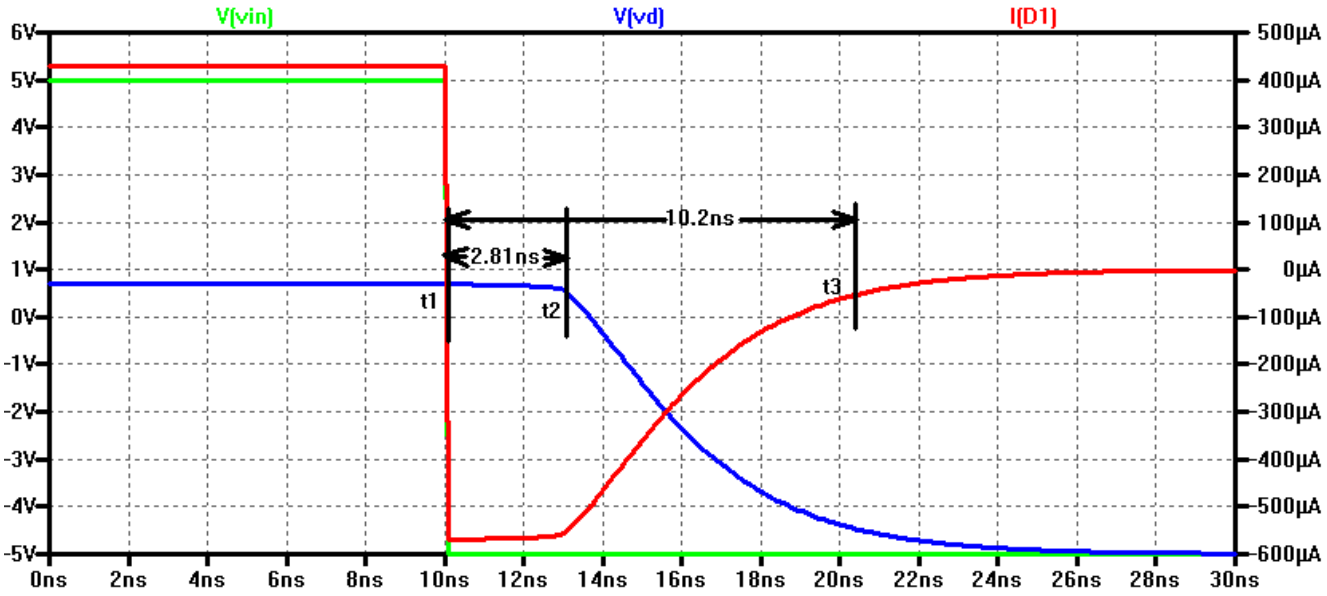
Diode's reverse recovery time is $t_{rr} = t_3 - t_1$ where t_3 is the time when current in the diode becomes 10% of $\frac{V_R - 0.7}{R}$.

Verification using LTSpice:




```
PULSE(5 -5 10n 0.1n 0.1n 20n 40n)
.tran 30n
.model Dtrr D is=1e-15 tt=5E-9 cj0=5e-13 vj=0.7 m=0.33
```

Avani Falgun Trivedi



From the above plot when current in the diode is = 0.01(-570uA)= -57uA, which gives t_3 = 20.20ns. Hence t_{rr} = 10.2ns.

When t > t_2, the diode-depletion capacitance is charged through R until the current in the circuit goes to zero, time t_3 depends on the resistor value. So resistor value dominates in increases the diode's reverse recovery time when using 10k resistor instead of 1k resistor.