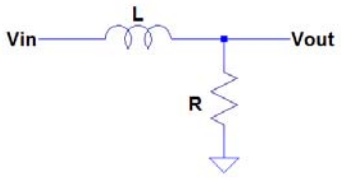
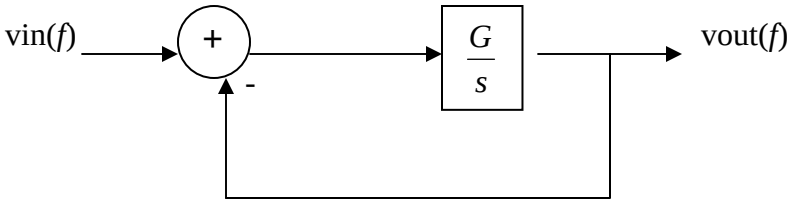
Lincoln Bollschweiler

3.1) Resketch Fig. 3.2 for the following circuit.



There is no change that needs to be made to the sketch of Fig. 3.2 for this implementation of a first order lowpass filter. Fig. 3.2 was constructed with an RC lowpass filter. Both can be considered passive integrators. The only difference is that, for the RC filter, G = 1/(RC) where as for the LR filter G = R/L.

For completeness, Fig. 3.2 is resketched, as the problem requests.



The derivation of the transfer function from the schematic is as follows:

$$V_{out} = \frac{V_{in} \cdot R}{R + j\omega L} \Rightarrow \frac{V_{out}}{V_{in}} = \frac{1}{1 + j\omega L/R} = \frac{1}{1 + s/G}, \quad G = R/L.$$

The derivation of the transfer function from the block diagram is as follows:

$$V_{out} = (V_{in} - V_{out})G/s \Rightarrow V_{out}\left(1 + G/s\right) = V_{in} \cdot G/s \Rightarrow \frac{V_{out}}{V_{in}} = \frac{G/s}{1 + G/s}\frac{\left(s/G\right)}{\left(s/G\right)} = \frac{1}{1 + s/G}.$$

One can see the two solutions for V_{out}/V_{in} are consistent.

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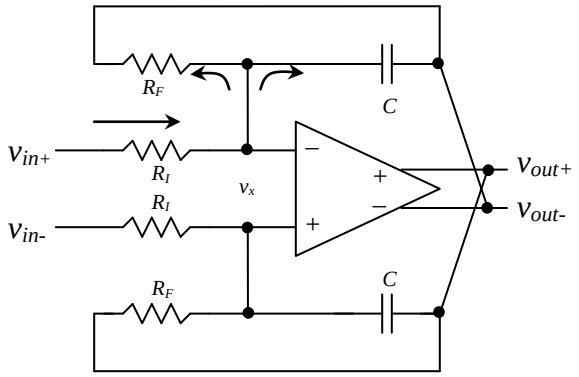
3.2 *Show that Eq. (3.6) is still valid if the circuit's inputs and outputs are referenced to the common-mode voltage, V_{CM}. (The op-amp inputs should also be at V_{CM}.)*

Below is equation 3.6:

$$\frac{v_{in}}{R_I} - \frac{v_{out}}{R_F} = \frac{v_{out}}{1/sC}$$

This equation was derived from the fully differential continuous time integrator (CAI) seen on page 75, figure 3.4.



F-1 Implementation of a first-order low-pass filter using a CAI.

F-1 has several additions which are not shown in figure 3.4. The current flow directions shown in F-1 were arbitrarily chosen, and the v_x voltage is labeled for completeness. Please realize that the op-amp will try and keep the v_x nodes equal. F-1 shows how, for an analog integrator, your positive input goes to the negative terminal of the op-amp, also note that I explicitly drew how we feedback the inverse output to the input of the op-amp. If we didn't inverse the feedback signal our transfer function would only have a 180° phase shift, but the magnitude would be unchanged.

To solve this problem we will use Kirchhoff's Current Law to determine the transfer function of the circuit seen in F-1. Let's reference the input voltages and output voltages to the common mode voltage (V_{CM}):

$$v_{INP} = V_{CM} + v_{inp}$$

$$v_{INM} = V_{CM} + v_{inm}$$

$$v_{OUTP} = V_{CM} + v_{outp}$$

$$v_{OUTM} = V_{CM} + v_{outm}$$

We are denoting the input and output voltages have a DC component, V_{CM}, along with a varying voltage (often a small signal, or sinewave), $v_{in/out}$, which can be positive or negative w.r.t. V_{CM}. Writing KCL:

$$\frac{v_{INP} - v_X}{R_I} = \frac{v_X - v_{OUTM}}{R_F} + \frac{v_X - v_{OUTM}}{1/sC}$$

$$\frac{v_{INM} - v_X}{R_I} = \frac{v_X - v_{OUTP}}{R_F} + \frac{v_X - v_{OUTP}}{1/sC}$$

Subtracting the two equations to get the fully differential input and output voltages:

$$\frac{v_{INP} - v_X}{R_I} - \frac{v_{INM} - v_X}{R_I} = \frac{v_X - v_{OUTM}}{R_F} + \frac{v_X - v_{OUTM}}{1/sC} - \frac{v_X - v_{OUTP}}{R_F} - \frac{v_X - v_{OUTP}}{1/sC}$$

After organizing the terms we can see that the v_x terms cancel out:

$$\frac{v_{INP} - v_{INM} - v_X + v_X}{R_I} = \frac{v_X - v_{OUTM}}{R_F} - \frac{v_X - v_{OUTP}}{R_F} + \frac{v_X - v_{OUTM}}{1/sC} - \frac{v_X - v_{OUTP}}{1/sC}$$

$$\frac{v_{INP} - v_{INM}}{R_I} = \frac{v_{OUTP} - v_{OUTM}}{R_F} + \frac{v_{OUTP} - v_{OUTM}}{1/sC}$$

We normally leave out the v_x terms to simplify the equations, but we left them in to ensure understanding of what we are doing. We can expand the voltages and show their reference to V_{CM}:

$$\frac{V_{CM} + v_{inp} - V_{CM} - v_{inm}}{R_I} = \frac{V_{CM} + v_{outp} - V_{CM} - v_{outm}}{R_F} + \frac{V_{CM} + v_{outp} - V_{CM} - v_{outm}}{1/sC}$$

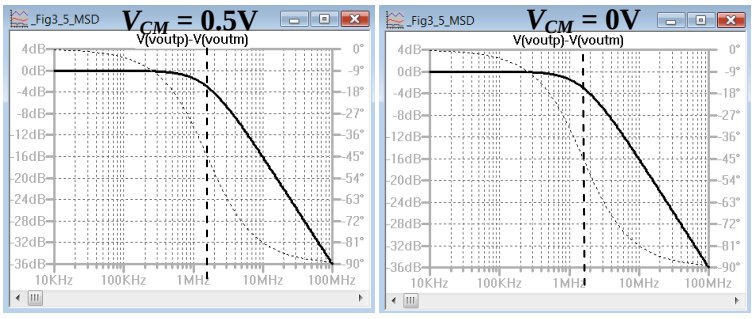
When using a fully differential topology the common mode reference will always be subtracted out of the resulting transfer function. After performing the subtractions we can see that this is the same equation as equation 3.6.

$$\frac{v_{inp} - v_{inm}}{R_I} = \frac{v_{outp} - v_{outm}}{R_F} + \frac{v_{outp} - v_{outm}}{1/sC}$$

Knowing that the differential voltage can be written as, $v_p - v_m = v$:

$$\frac{v_{in}}{R_I} = \frac{v_{out}}{R_F} + \frac{v_{out}}{1/sC}$$

The LTSPICE results (_FIG3_5_MSD) in example 3.1 use a 0.5V common mode voltage for the input and output. We can change the common mode voltage to 0V (ideal components used, we don't have to worry about input/output common mode range) and show that the results are identical:



3.3. Sketch the implementation of a first-order low pass filter using CAI with 3 dB frequency of 10 MHz and a DC gain of 6 dB. Simulate your design to verify it works as expected.

Sol: Let us consider a fully differential op amp topology to implement the first order low pass filter using continuous time analog integrator (Note: this topology has better SNR compared to single ended op amp topology).

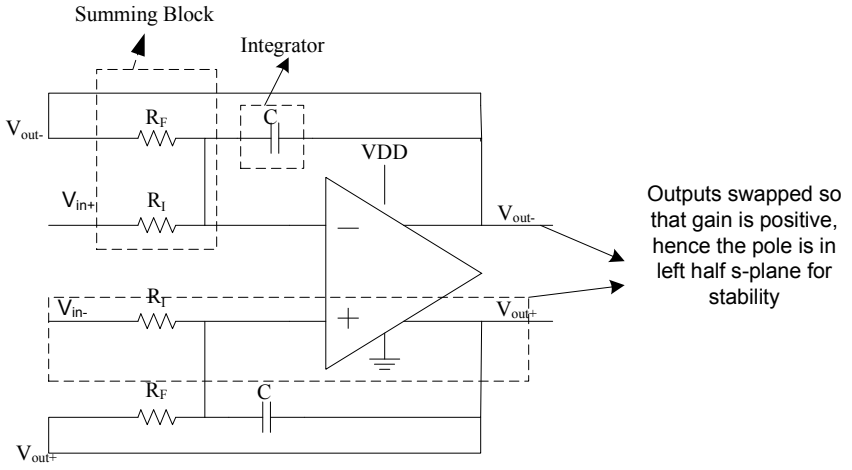


Figure 1. First order low pass filter with CAI

The differential gain of the above topology can be written as

$$\frac{V_{out+}-V_{out-}}{V_{in+}-V_{in-}}=\frac{R_F/R_I}{1+sR_FC} \tag{1}$$

The DC gain of the above topology is given by

$$\left(\frac{V_{out+}-V_{out-}}{V_{in+}-V_{in-}}\right)_{DC}=\frac{R_F}{R_I} \tag{2}$$

$$\frac{R_F}{R_I}=2 \text{ (i.e 6dB)} \tag{3}$$

$$f_{3dB}=\frac{1}{2\pi R_FC} \tag{4}$$

Let R_F=20k, R_I=10k so that gain is 2 then

$$f_{3dB}=\frac{1}{2\pi R_FC}=10\text{MHz} \tag{5}$$

Solving equation (5) gives C=0.8p

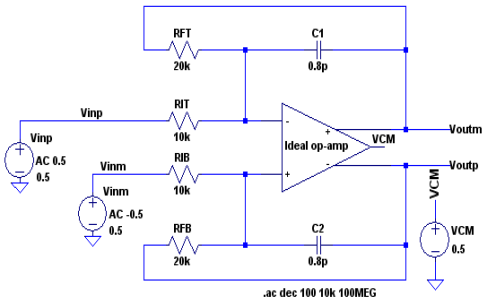


Figure 2. LTSPICE Schematic of Figure 1 (from cmosedu.com)

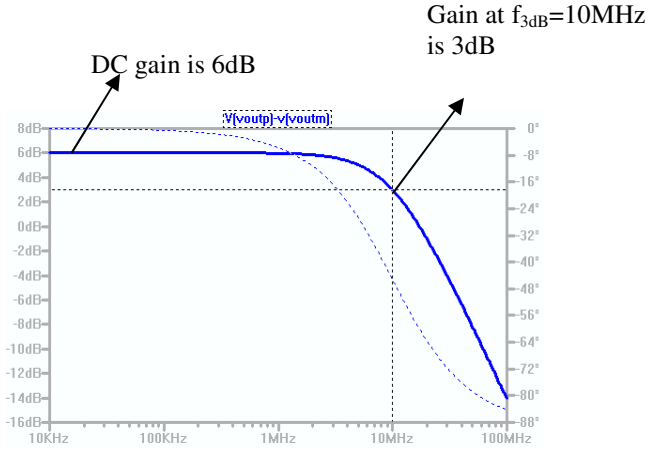


Figure 3. Frequency response of the low pass filter in Figure 1

Simulation results with selected values of R_F, R_I, C is shown in Figure 3. We can see that the dc gain is at 6dB, f_{3dB} is at 10MHz.

3.4 Plot, in the complex plane, the ideal pole location and the actual pole location due to finite op-amp unity gain frequency for the filter described in Ex. 3.4.

Solution:

The schematic of the filter is shown in Fig. 1.

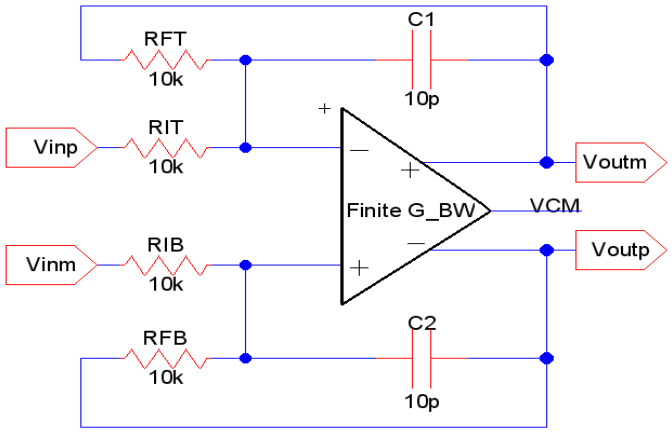


Figure 1 The schematic of the filter described in Ex. 3.4.

The output and input relationship of the filter using this topology, Eq. (3.14) in [1], is

$$\frac{v_{out}}{v_{in}}=\frac{-\frac{R_F}{R_I}}{s^2\cdot\frac{C\,R_F}{\omega_{un}}+s\cdot\left[C\,R_F+\frac{1}{\omega_{un}}\left(1+\frac{R_F}{R_I}\right)\right]+1} \tag{1}$$

For Ex. 3.4, $R_F=R_I=R$ and $RC=(10\,k\,\Omega)(10\ pF)=100\,ns$, so Eq. 1 becomes

$$\frac{v_{out}}{v_{in}}=\frac{-1}{s^2\cdot\frac{RC}{\omega_{un}}+s\cdot\left[RC+\frac{2}{\omega_{un}}\right]+1} \tag{2}$$

For ideal op-amp, $\omega_{un}\to\infty$, then rewriting Eq. 2 we get

$$\frac{v_{out}}{v_{in}}=\frac{-1}{s\cdot RC+1} \tag{3}$$

So the ideal pole location is

$$s_{p,ideal}=-1/RC=-10\,M \tag{4}$$

For the op-amp in Ex. 3.4, $\omega_{un}=2\pi\cdot f_{un}=2\pi\cdot 10\,MHz$. Substituting ω_{un} and RC into Eq. 2

we have

$$\frac{v_{out}}{v_{in}} = \frac{-1}{s^2 \cdot \frac{100\,n}{2\pi \cdot 10\,M} + s \cdot \left[100\,n + \frac{2}{2\pi \cdot 10\,M} \right] + 1} \approx \frac{-1}{s \cdot (131.8\,n) + 1} \tag{5}$$

So the actual pole location is

$$s_{p,\,actual} = -1/(131.8\,n) = -7.59\,M \tag{6}$$

The ideal and actual pole locations in the complex plane are shown in Fig. 2.

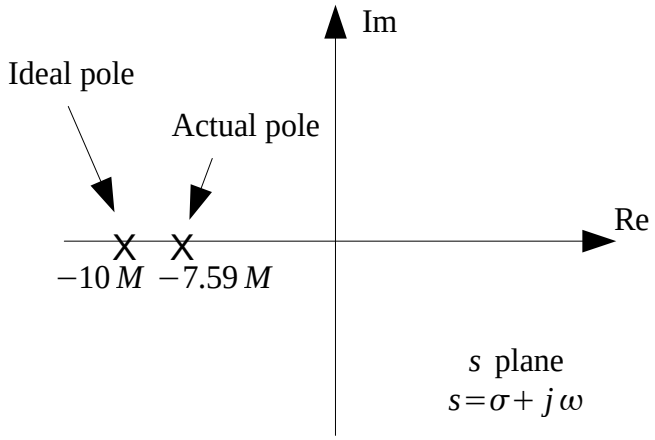


Figure 2 The ideal and actual pole locations in the complex plane.

Reference:

[1] R. J. Baker, *CMOS Mixed-signal Circuit Design, Second Edition*, Wiley-IEEE, 2009.

3.5) Plot Eq. (2.59) of the last chapter using SPICE and the op-amp model shown in Fig. 3.8.

$$A_{OL}(f) = \frac{A_{OL,DC}}{1 + j\frac{f}{f_{3dB}}} = \frac{v_{out+} - v_{out-}}{v_{in+} - v_{in-}} \qquad (2.59)$$

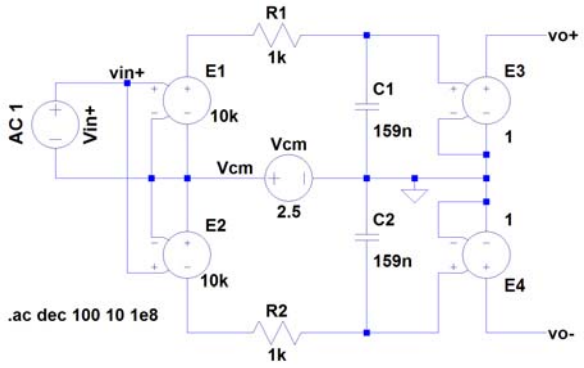


Figure 3.5.1 Duplication of Fig. 3.8 (mentioned in problem statement) from the MSD textbook, with addition of an input voltage source on vin+.

This problem requires the addition of one or two voltage sources to the input(s). For simplicity, one source is shown and used in this example. The reader will notice that vin- has been removed and that it has been shorted to V_{CM}. It is left as an alternative to add a second voltage source and connect V_{CM} to its DC offset input (like Vin+). Also of interest is to note that V_{CM} can be any arbitrary value desired. There is no limitation in this 'ideal' simulation with no supply rail constraints. A value of 2.5 was chosen assuming a V_{DD} of 5V and that ½ V_{DD} was desired for V_{CM}.

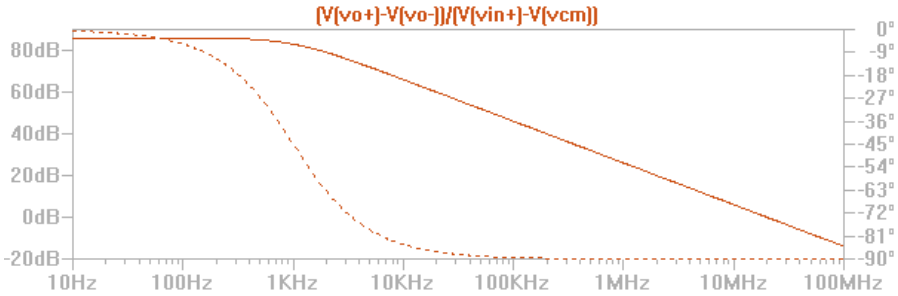


Figure 3.5.2 Plot of the finite bandwidth op-amp model shown in Fig. 3.5.1; gain vs. frequency.

From the simulation $A_{OL,DC}$ = 86.0dB, f_{3dB} = 1kHz, and f_{un} = 20MHz. As a quick check to make sure (2.59) holds, let's find A_{OL}(20MHz) , the unity gain frequency.

$$\left|A_{OL}(20MHz)\right| = \left|\frac{A_{OL,DC}}{1 + j\frac{f}{f_{3dB}}}\right| = \left|\frac{10^{86dB/20}}{1 + j\frac{20E6}{1E3}}\right| = \frac{20E3}{20E3} = 1.$$

3.6. Suppose an anti aliasing filter was required for a 12-bit data converter. Further assume the filter is to be implemented using an active-RC topology. If VDD=1.0 estimate the minimum value of the integration capacitor that should be used, assuming the filters noise performance is dominated by thermal noise. Is it wise, for 12-bit system performance, to design the filter so that its SNR is equal to the SNR of the data converter?

Sol)

Section 1: Realizing an Anti Aliasing Filter using an active RC integrator

Using an active-RC topology we can realize an anti aliasing filter (AAF) as shown in Figure 1.

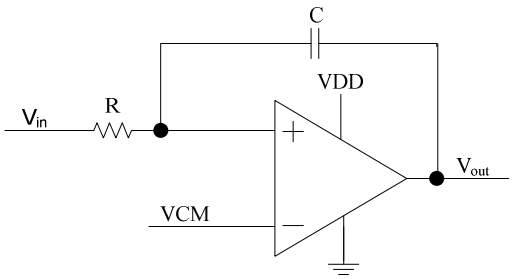


Figure 1. Anti aliasing filter(AAF)

The dominant noise in the AAF in Figure 1 is assumed to be thermal noise. The capacitor filters (decreases) the thermal noise at the output. Hence increasing the value of capacitor increases the SNR of the filter. The resulting RMS value of thermal noise is given by $\sqrt{\frac{kT}{C}}$. The SNR of the active-RC topology shown is

$$SNR = 10.\log\left(\frac{VDD^2/8}{kT/C}\right) \quad (1)$$

Where VDD=1V, k=1.38x10^{-23}J/K, T=300K

The SNR of the 12-bit data converter is given by

$$SNR_{12bitADC} = 6.02N+1.76dB \text{ where } N=12 \quad (2)$$

The SNR of the AAF (active RC circuit in this case) should at least be equal to or more than the SNR of the 12-bit data converter, so that the noise performance of the system is not degraded by the AAF. Note that this is the worst case SNR of the AAF and ideally it should be much more than that.

Equating (1) and (2) solving for C we get **C=0.83pF**.

Note: To minimize the thermal noise in AAF we need to increase the value of capacitor. But this results in decreasing the 3-dB frequency (see eq (3)) . Hence the bandwidth of the signal allowed is reduced.

$$f_{3dB} = \frac{1}{2\pi RC} \quad (3)$$

Section 2: How much SNR is good for the AAF for 12-bit performance of data converter

The Anti aliased signal goes as input to the Sample and Hold and further to the data converter (12bit ADC in Figure 2). If the SNR of the AAF is same as that of ADC, it means that the input coming to the ADC itself has a lot of noise and we have quantization noise of ADC to deal with. Hence the noise performance of the total system is degraded, and we will get say 11-bit or even less performance by the data converter.

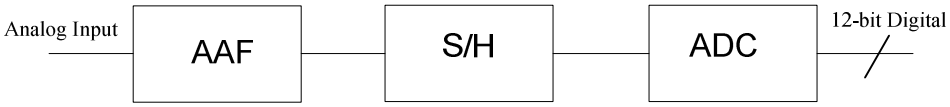


Figure 2. Anti aliasing filter followed by data converter

Hence it is better to have Anti aliasing filter that has much higher SNR compared to that of data converter.

.

Question 3.7

Repeat question 3.6 if the op-amp used in the filter has a linear output swing of 80% of the power supply voltage.

Solution

Question 3.6 states: *Suppose an anti aliasing filter was required for a 12-bit data converter. Further assume the filter is to be implemented using an active-RC topology. If VDD=1.0 estimate the minimum value of the integration capacitor that should be used, assuming the filters noise performance is dominated by thermal noise. Is it wise, for 12-bit system performance, to design the filter so that its SNR is equal to the SNR of the data converter?*

Figure 1 below shows a possible topology of the single ended op-amp used as Active-RC filter in data converter as AAF.

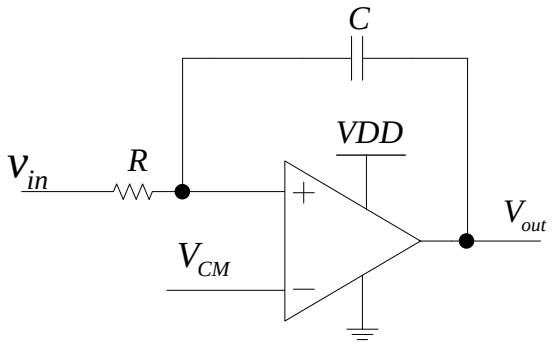


Figure1. A possible implementation of AAF with Active RC filter

The SNR equation for the filter is based on assumptions

- op-amp is not limited by linear output swing as mentioned in question (V_{out} goes all the way up to VDD)
- noise performance of filter is dominated by the thermal noise from the *R*
- V_{CM} is $VDD/2$ or half of the power supply voltage

Based on the discussion (page 82-83) the SNR of filter given by ratio of maximum RMS output voltage of $VDD/\left(2\sqrt{2}\right)$ to the RMS thermal noise of *R* limited by capacitor as $\sqrt{\frac{kT}{C}}$ and given by

$$SNR = 20 \cdot \log \frac{VDD/\left(2\sqrt{2}\right)}{\sqrt{kT/C}}$$

Now if the op-amp has a linear output swing of 80% of power supply then the total output peak to peak voltage is given as $0.8VDD$ where $V_{pp} = 0$ *to* VDD or in our case *VDD* = 1V, in other words if $V_{CM} = 0.5V$ then output is swinging from 0.9V to 0.1V. Thus the maximum RMS output voltage will be given as $0.8 \cdot VDD/\left(2\sqrt{2}\right)$. The new *SNR* of the filter is will be given as

$$SNR = 20 \cdot \log \frac{0.8 \times VDD \Big/ \left(2\sqrt{2}\right)}{\sqrt{kT/C}}$$

In order to obtain the value of C we make one more assumption of equating this value of SNR to ideal SNR of 12 bit data converter (Nyquist rate date converter and **not noise shaping or oversampling type**) given as

$$SNR_{ideal,12-bitADC} = \left(6.02N + 1.76\right) db \quad \text{where } N = 12$$

final equation can be written as ; with $VDD = 1V$; $k = 1.38\text{x}10^{-23}$ J / K or (V · Col/K); T=300K

$$20 \cdot \log \frac{0.8 \times VDD \Big/ \left(2\sqrt{2}\right)}{\sqrt{kT/C}} = \left(6.02 \times 12 + 1.76\right)$$

C is given as $\approx 1.3 pF$. It is obvious that as the signal RMS goes down SNR will go down and in order to compensate a larger capacitor have to be used to limit the thermal noise.

As for the last section of the question we can say that while designing the filter, assuming the filter's *SNR* equal to data converter's *SNR* was the worst case situation. It is always better to use filter with *SNR* performance much higher than that of data converter because the AAF filter is first stage of the data converter design. Looking at the figure 2 below, if noise is not filtered properly in AAF then it will suffer aliasing due to S/H stage and will degrade the over all *SNR* of system in addition to quantization noise.

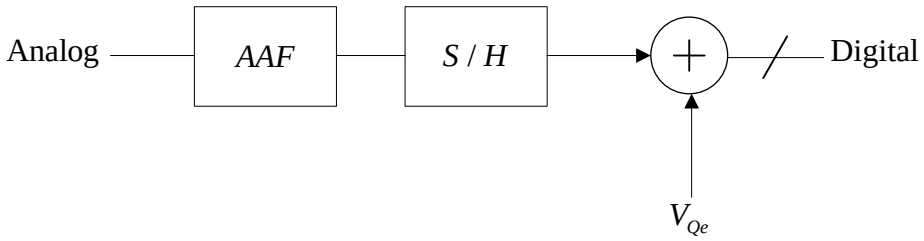


Figure2. General block diagram of A-D converter

Kaijun Li
Problem 3.8
Derive the transfer function for the filter shown in Figure 3.16 if the transconductors have different g_ms. Sketch the block diagram, similar to the one seen in Fig. 3.6, for the filter.

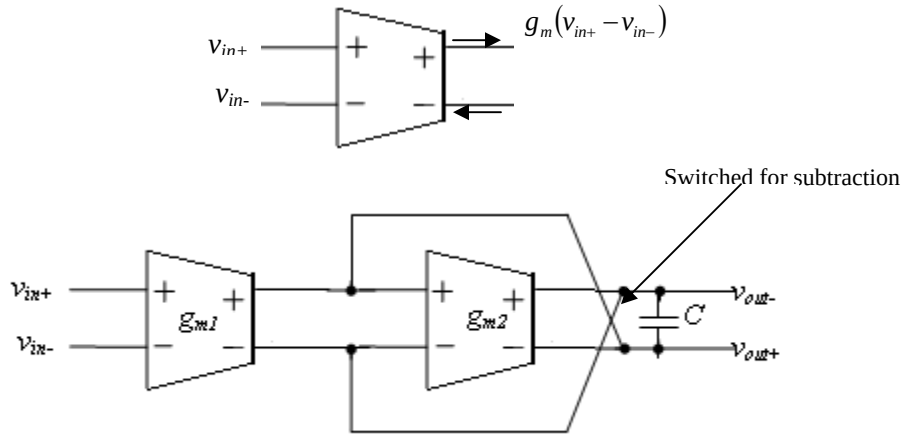


Figure 3.16 implementing a first-order filter using transconductors

Solution:
The same analysis can be applied to Fig. 3.16 with different for the two transconductors.

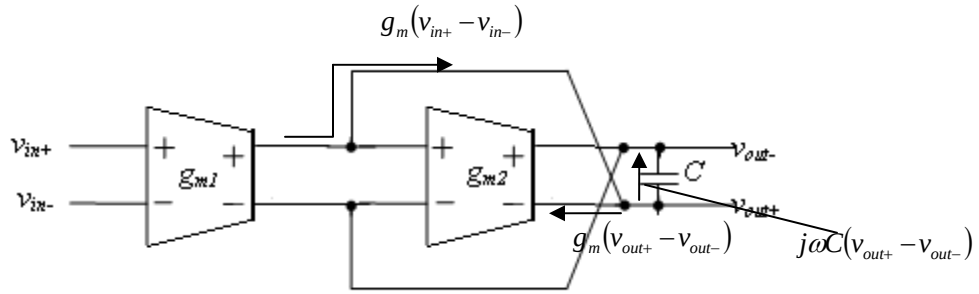


Figure 3.8-1 Applying KCL to the output node

Applying KCL to the output node, we have

$$g_{m1}(v_{in+}-v_{in-})-g_{m2}(v_{out+}-v_{out-})-j\omega C(v_{out+}-v_{out-})=0 \tag{1}$$

or

$$\frac{v_{out+}-v_{out-}}{v_{in+}-v_{in-}}=\frac{g_{m1}}{g_{m2}+j\omega C}=\frac{g_{m1}/g_{m2}}{1+j\omega C/g_{m2}} \tag{2}$$

Redrawing the block diagram in Fig. 3.6, we can write

$$\frac{v_{out}}{v_{in}}=\frac{\frac{1}{G_2}}{1+\frac{s}{G_1G_2}} \text{ and } f_{3dB}=\frac{G_1G_2}{2\pi} \tag{2}$$

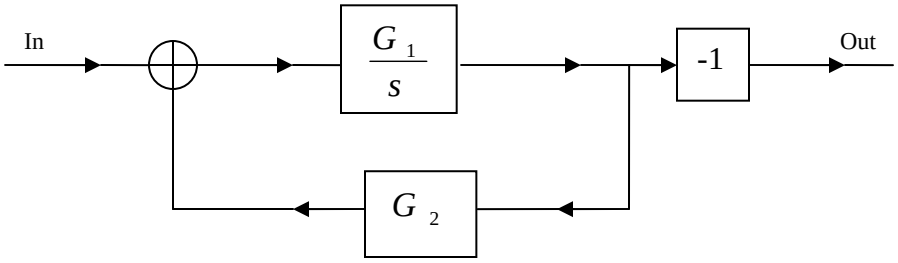


Figure 3.8-2 Block diagram seen in Fig. 3.6 (Textbook)

Comparing equations (2) and (3), we have

$$G_1 = \frac{g_{m2}}{g_{m1}}, G_2 = \frac{g_{m1}}{C}$$

The block diagram for the filter with different g_ms is drawn as below.

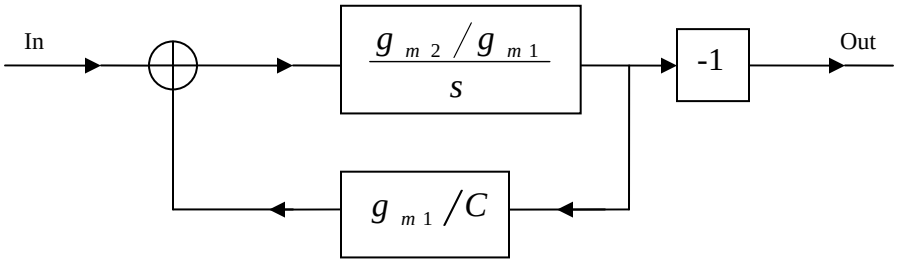


Figure 3.8-3 Block diagram for the gm-C filter

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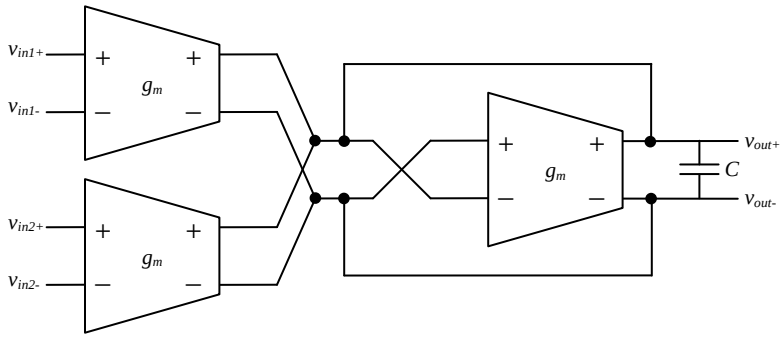
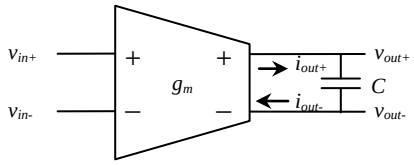
3.9 *Derive the transfer function for the following first-order transcondutor filter.*



F-1 A first-order filter with two inputs.

To begin the derivation let's start by determining the transfer characteristics of the OTA seen in F-2.



F-2 Schematic symbol of an OTA.

The properties of the OTA currents are:

$$i_{out+} = i_{out-} = g_m(v_{in+} - v_{in-})$$

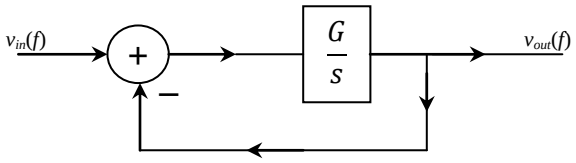
Viewing F-2 we can find the differential output voltage:

$$\frac{v_{out+} - v_{out-}}{1/j\omega C} = i_{out+} = i_{out-} = g_m(v_{in+} - v_{in-})$$

The differential OTA gain for the circuit in F-2 can be written as:

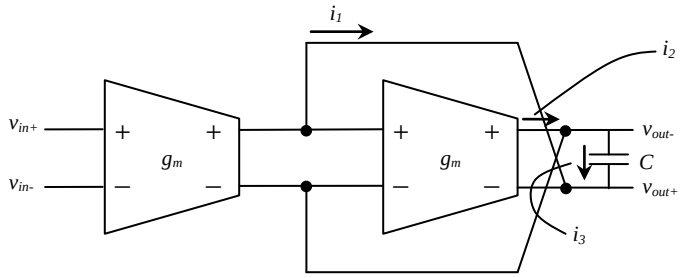
$$\frac{v_{out+} - v_{out-}}{v_{in+} - v_{in-}} = \frac{g_m}{j\omega C}$$

To create a low-pass filter using the transconductance amplifier, review F-3:



F-3 Block diagram of an integrator-based filter.

The block diagram shows that we need to subtract the output from the input; this is accomplished by reviewing F-4:



F-4 Implementing a first-order filter using transcondutors.

Summing the currents at the output gives the following equation:

$$i_3 = i_2 - i_1$$

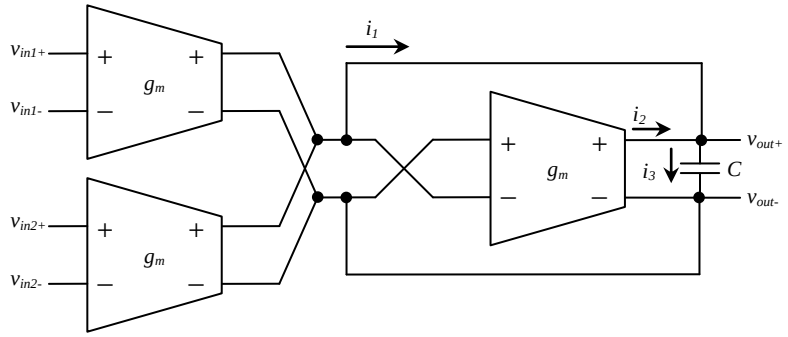
$$j\omega C(v_{out-} - v_{out+}) = g_m(v_{out+} - v_{out-}) - g_m(v_{in+} - v_{in-})$$

$$g_m(v_{in+} - v_{in-}) = g_m(v_{out+} - v_{out-}) - j\omega C(v_{out-} - v_{out+})$$

$$g_m(v_{in+} - v_{in-}) = g_m(v_{out+} - v_{out-}) + j\omega C(v_{out+} - v_{out-})$$

$$\frac{v_{out+} - v_{out-}}{v_{in+} - v_{in-}} = \frac{1}{1 + j\omega\frac{1}{g_m}C}$$

Using this technique we can refer back to F-1 and determine the transfer function by summing the currents at the output.



$$i_3 = i_1 + i_2$$

$$j\omega C(v_{out+} - v_{out-}) = g_m(v_{in1+} - v_{in1-}) + g_m(v_{in2+} - v_{in2-}) + g_m(v_{out-} - v_{out+})$$

$$j\omega C(v_{out+} - v_{out-}) = g_m(v_{in1+} - v_{in1-}) + g_m(v_{in2+} - v_{in2-}) - g_m(v_{out+} - v_{out-})$$

$$(v_{out+} - v_{out-})(j\omega C + g_m) = g_m(v_{in1+} - v_{in1-}) + g_m(v_{in2+} - v_{in2-})$$

Let v_{in1+} - v_{in1-} = v_{in1} and v_{in2+} - v_{in2-} = v_{in2}:

$$\frac{v_{out+} - v_{out-}}{v_{in1} + v_{in2}} = \frac{1}{1 + j\omega\frac{1}{g_m}C}$$

3.10 – Show the derivation details that result in Eqs. (3.44) and (3.46).

Tyler Hansen

For a perhaps more intuitive explanation, let's turn to figure 3.10.1, which is a replication of book figure 3.25 with an added graphic to help us visualize the clock relationship between phi1 and phi2.

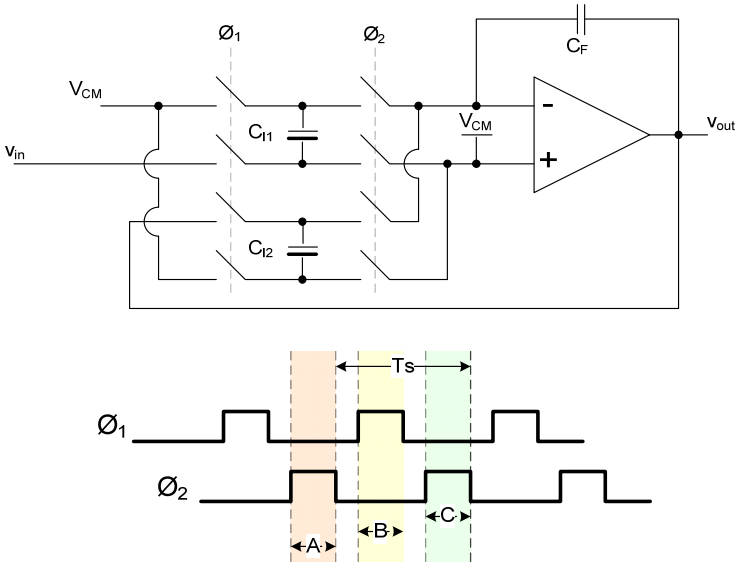


Figure 3.10.1: Implementation of a lowpass first-order filter using a switched capacitor DAI (Discrete-Analog Integrator)

Note that when phi1 is high, phi2 is low because the two clock signals must be non-overlapping. When phi1 is high, C1 and C2 are being charged by the input signal, and the ***previous output signal*** respectively. It is valuable to realize that during this time *the output is not changing*. The circuit can be re-drawn under these circumstances to look like figure 3.10.2.

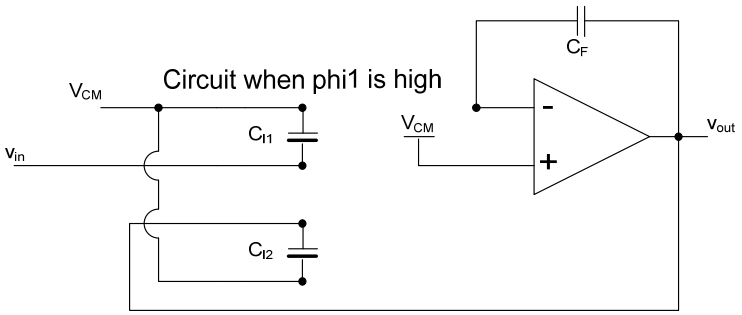


Figure 3.10.2: Schematic of figure 3.10.1 when phi1 is high, and phi2 is low.

By the end of timing period B (as defined in figure 3.10.1) the capacitors CI1 and CI2 have adequately sampled the previous output, and the current input. When phi1 goes low, and phi2 goes high, we can re-draw the schematic as shown in figure 3.10.2.

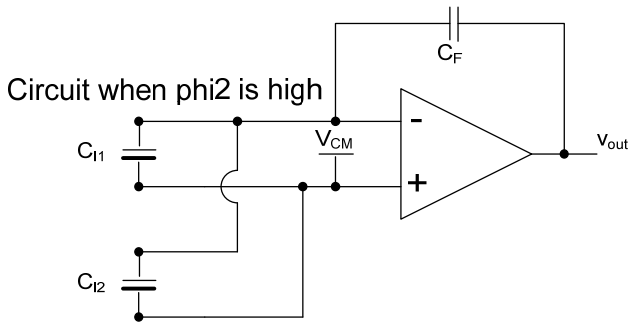


Figure 3.10.3: Schematic of figure 3.10.1 when phi2 is high, and phi1 is low.

When phi2 is high, the sampling capacitors CI1 and CI2 charge share. This performs the subtraction operation that can be seen in the block diagram of book figure 3.24 (due to the reversal of the capacitor nodes when connected in parallel through the phi2 switches). The amount of charge on the 2 sampling capacitors is then transferred to the output capacitor. This is what allows us to attribute the change in output charge from one cycle to the next is a result of the charge-sharing (subtraction in charge) of the previous output signal from the input signal. Because the input signal is sampled directly while phi1 is high (by contrast, the output is not changing at this point), the input signal only has to wait ½ of a clock cycle to be charge-shared with CI2 and transferred to the output.

Mathematically…

Book equation 3.46 defines the z-domain transfer function of a switched-capacitor implementation of a DAI (Discrete-Analog Integrator), and is copied into this solution as equation 3.10.1 below:

$$v_{out}(z) = \left(\frac{z^{-1}}{1-z^{-1}}\right) \cdot \left[\frac{C_{I1}}{C_F} v_{in}(z) \cdot z^{1/2} - \frac{C_{I2}}{C_F} \cdot v_{out}(z)\right] \qquad \text{Equation 3.10.1}$$

Note that if we manipulate equation 3.10.1 to work backwards, we get:

$$C_F \cdot v_{out}(z) \cdot (1-z^{-1}) = C_{I1} v_{in}(z) \cdot z^{-1/2} - C_{I2} \cdot v_{out}(z) \cdot z^{-1} \qquad \text{Equation 3.10.2}$$

Equation 3.10.2 is a charge conservation equation that states:

$$\Delta Q_{(C_F)} = Q_{(C_{I1})} - Q_{(C_{I2})}$$
$$C_F v_{out}(nT_s) - c_F v_{out}[(n-1)T_s] = C_{I1} v_{in}[(n-1/2)T_s] - C_{I2} v_{out}[(n-1)T_s]$$

Equation 3.10.3

It is equation 3.10.3 coupled with the explanation of how the charge is transmitted through figure 3.10.1 that derives the transfer function of 3.10.1.

Now note that figure 3.10.1 is the schematic implementation of the block diagram reproduced in figure 3.10.4 below:

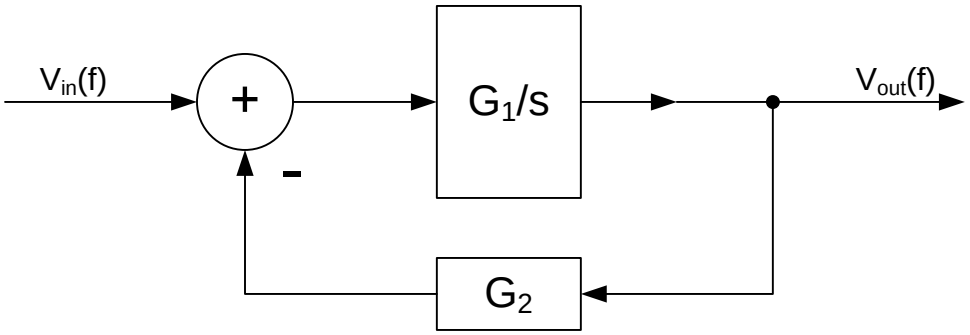


Figure 3.10.4: Block diagram of a lowpass first-order filter.

The book example claims that the schematic shown in figure 3.10.1 is the implementation of the block diagram shown in figure 3.10.4. Let's prove it. We will start by deriving the transfer function of the block diagram:

$$v_{out}(f) = \frac{G_1}{s} \cdot \left[V_{in}(f) - G_2 \cdot v_{out}(f)\right]$$

$$v_{out}(f) \cdot \left[1 + \frac{G_1 G_2}{s}\right] = v_{in}(f) \cdot \frac{G_1}{s} \qquad \text{Equation 3.10.4}$$

$$\frac{v_{out}(f)}{v_{in}(f)} = \frac{\frac{G_1}{s}}{1 + \frac{G_1 G_2}{s}}$$

On the other hand, we know that a switched capacitor configuration can be represented as a resistor with a value of $1/f_sC$ according to the discussion on page 51 of the Mixed Signal text. That being established, we can re-drawn figure 3.10.1 as figure 3.10.5below:

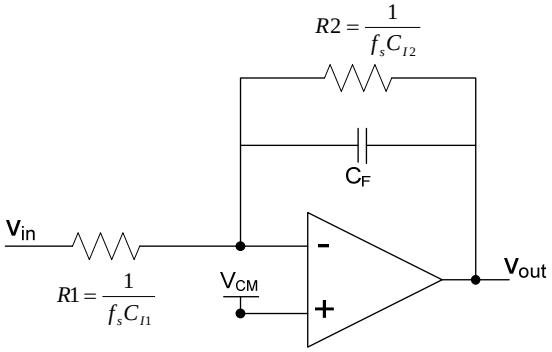


Figure 3.10.5: Equivalent resistor configuration of the switched capacitor lowpass filter seen in fig. 3.10.1.

At this point, it is trivial to write the transfer function of this circuit.

$$(v_{in} - V_{CM}) \cdot f_s C_{I1} = (V_{CM} - v_{out}) \cdot (j\omega C_F + f_s C_{I2})$$

$$v_{in} \cdot f_s C_{I1} = -v_{out} \cdot (j\omega C_F + f_s C_{I2}) \qquad \text{Equation 3.10.5}$$

$$\frac{v_{out}}{v_{in}} = \frac{f_s C_{I1}}{f_s C_{I2} + j\omega C_F} = \frac{f_s C_{I1}}{f_s C_{I2} + sC_F} = \frac{\frac{f_s}{j\omega} \cdot \frac{C_{I1}}{C_F}}{\frac{f_s}{j\omega} \cdot \frac{C_{I2}}{C_F} + 1}$$

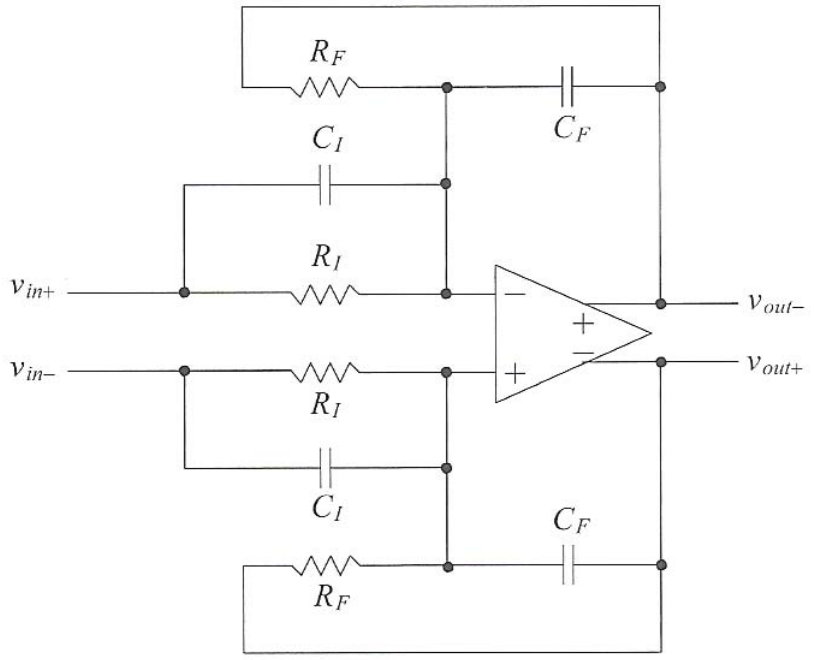
Comparing the transfer function results from equation 3.10.4, and 3.10.5, we see that they are equivalent if:

$$G1 = \frac{C_{I1}}{C_F} \cdot f_s \qquad G2 = \frac{C_{I2}}{C_F} \cdot f_s \cdot \frac{1}{G1} = \frac{C_{I2}}{C_{I1}}$$

Lincoln Bollschweiler

3.11) Show the details of how the gains (G) are derived in Fig. 3.30.

Figure 3.30 from the text was scanned and is reproduced here.



$$G_1 = \frac{1}{R_I C_F}$$

$$G_2 = \frac{R_I}{R_F}$$

$$G_3 = R_I C_I$$

Figure 3.30 Implementation of an active-RC bilinear transfer function filter.

The derivation is as follows:

We can first recognize that $R \| C = \frac{1}{\frac{1}{R} + sC} = \frac{R}{1 + sRC}$. This applies to both the forward path and the feedback path. In the forward path R_I is in parallel with C_I and in the feedback path R_F is in parallel with C_F. Second, we can recognize that the inputs to the op-amp share a common mode voltage. We can label this V_{CM} and set it to an arbitrary value. For algebraic convenience we will choose $V_{CM} = 0$. Finally, we can recognize that $v_{in}^{+} = -v_{in}^{-}$. We will use these three identities for simplifications.

$$\frac{v_{out}^{-}}{\frac{R_F}{1 + sR_F C_F}} = \frac{-v_{in}^{+}}{\frac{R_I}{1 + sR_I C_I}}$$

$$v_{out}^{-}\left(1 + sR_F C_F\right) R_I = v_{in}^{-}\left(1 + sR_I C_I\right) R_F$$

$$\frac{v_{out}}{v_{in}} = \frac{R_F}{R_I}\frac{\left(1+sR_IC_I\right)}{\left(1+sR_FC_F\right)}.$$

The transfer function is now in the form of the bilinear transfer function, as follows:

$$\frac{v_{out}(f)}{v_{in}(f)} = \frac{1}{G_2}\frac{1+\frac{s}{1/G_3}}{1+\frac{s}{G_1G_2}}.$$

We can equate the associated parts of the two equations to find the gains.

$$\frac{1}{G_2} = \frac{R_F}{R_I} \Rightarrow G_2 = \frac{R_I}{R_F}$$

$$1+\frac{s}{1/G_3} = 1+sR_IC_I \Rightarrow G_3 = R_IC_I$$

$$1+\frac{s}{G_1G_2} = 1+sR_FC_F \Rightarrow \frac{1}{G_1G_2} = R_FC_F \Rightarrow G_1 = \frac{1}{R_FC_FG_2} = \frac{1}{C_FR_I}.$$

Jason Durand

Problem 3.12 – Is it possible to tune the gain, Q, and cutoff frequency of the lowpass biquad independently? If so, how? Give examples using the simulation netlist used to generate Fig 3.38.

The circuit used to generate Fig 3.38 is the general form of the biquad filter, with the two integration stages (G_3 and G_6 in the block diagram) set to zero gain. This modifies the biquad into an active lowpass filter and is accomplished in the circuit by removing capacitors C_{I1} and C_{I2} (the integration capacitors (note – in the figure below, the capacitors have a value of 1e-18 F, which is effectively removing them).

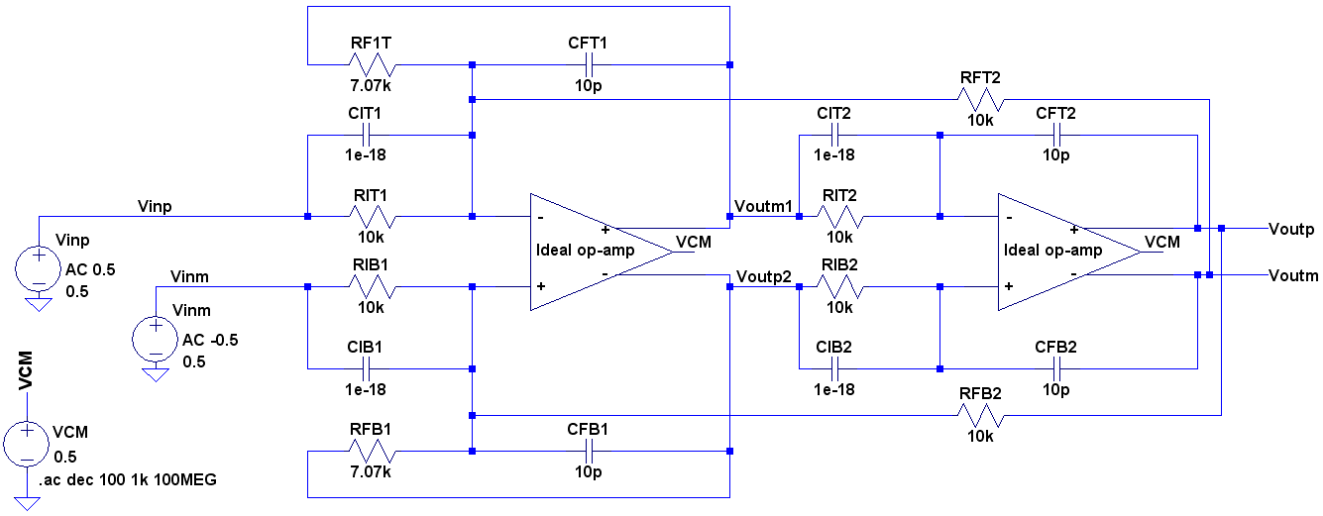


Figure 1: Circuit used to generate Fig 3.38 (Baker 104), modified for lowpass response

With the two integration capacitors removed, the general transfer function of this circuit is

$$\frac{Vout}{Vin} = \frac{\frac{1}{R_{I1} C_{F1} R_{I2} C_{F2}}}{s^2 + s\left(\frac{1}{R_{F1} C_{F1}}\right) + \frac{1}{C_{F1} R_{I2} C_{F2} R_{F2}}} \quad ,$$

where $\frac{2\pi f_0}{Q} = \frac{1}{R_{F1} C_{F1}}$ and $(2\pi f_0)^2 = \frac{1}{C_{F1} R_{I2} C_{F2} R_{F2}}$.

To independently set the gain, note that the DC gain is set by the ratio of the DC terms in the transfer function, or the s^0 terms. This translates into

$$DC\ Gain = \frac{\frac{1}{R_{I1} C_{F1} R_{I2} C_{F2}}}{\frac{1}{C_{F1} R_{I2} C_{F2} R_{F2}}} = \frac{R_{F2}}{R_{I1}} \quad .$$

Changing R_{F2} would affect the Q and the cutoff frequency of the circuit, since it is present is the other coefficients of the transfer function. However, R_{I1} is not present anywhere else in the transfer function,a

and can be changed without affecting the Q or the cutoff frequency of the filter. Therefore, we can say that the DC gain can be controlled independently of Q and f_0, and it is done by modifying the value of R_{I1}.

$$Gain = \frac{R_{F2}}{R_{I1}}$$, only adjust R_{I1} to independently adjust gain.

The next variable to attempt to individually control is the cutoff frequency, given by

$$f_0 = \frac{1}{2\pi} \cdot \sqrt{\frac{1}{C_{F1} R_{I2} C_{F2} R_{F2}}} \quad .$$

This is easy enough, choose values of the resistors and capacitors that can be implemented in the process and are reasonable, and you set the cutoff frequency. For the Q, however, you have much less freedom. The Q factor of the filter is given by

$$Q = R_{F1} C_{F1} \cdot 2\pi f_0 = R_{F1} C_{F1} \cdot (C_{F1} R_{I2} C_{F2} R_{F2})^{-\frac{1}{2}} \quad .$$

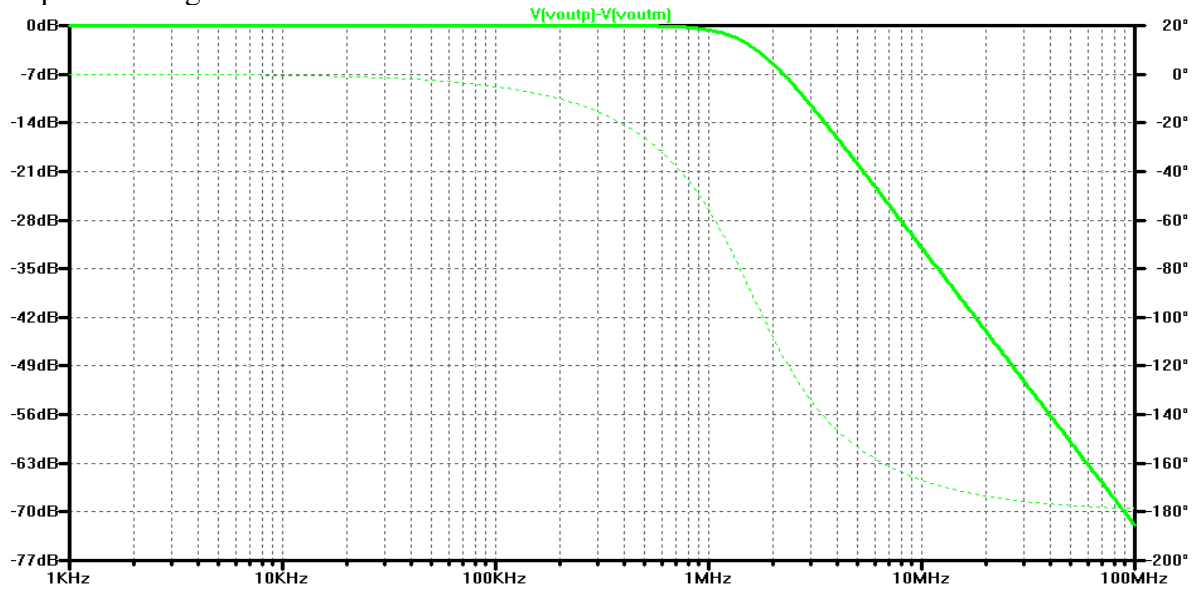
Since the value of C_{F1} is also present in the list of components that adjust cutoff frequency, you can't alter it to adjust the Q, leaving you with only R_{F1}. The equation to then set Q is given by

$$Q = R_{F1} \cdot 2\pi C_{F1} f_0$$, where Q is adjusted by changing R_{F1}.

To use these design equations, alter R_{I1} at any time to change the gain and R_{F2} at any time to change the Q factor, but a change in the cutoff frequency requires you to recalculate a value of R_{F2} for the desired Q.

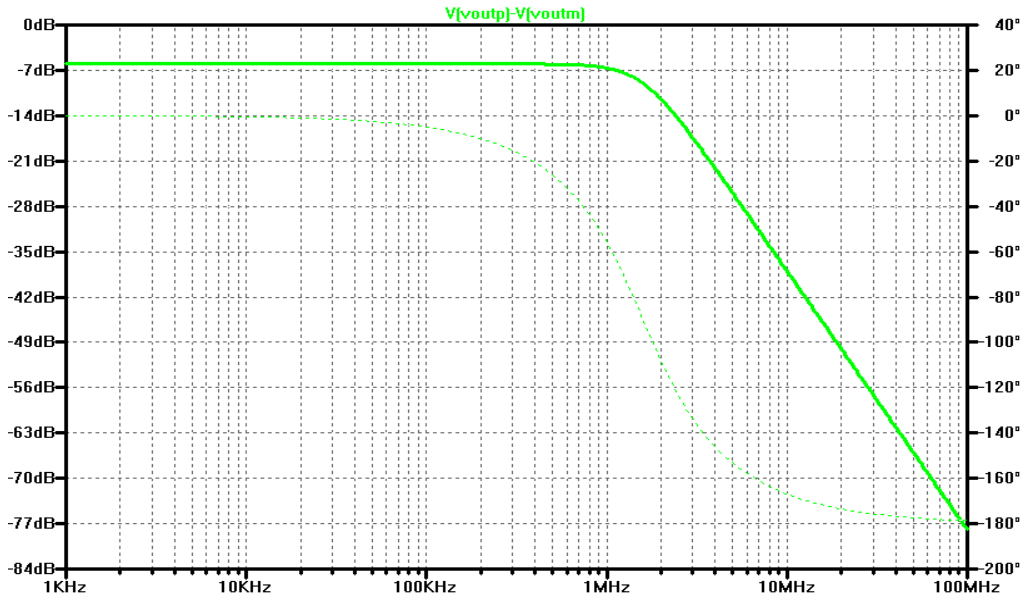
Examples:

AC response of Figure 1

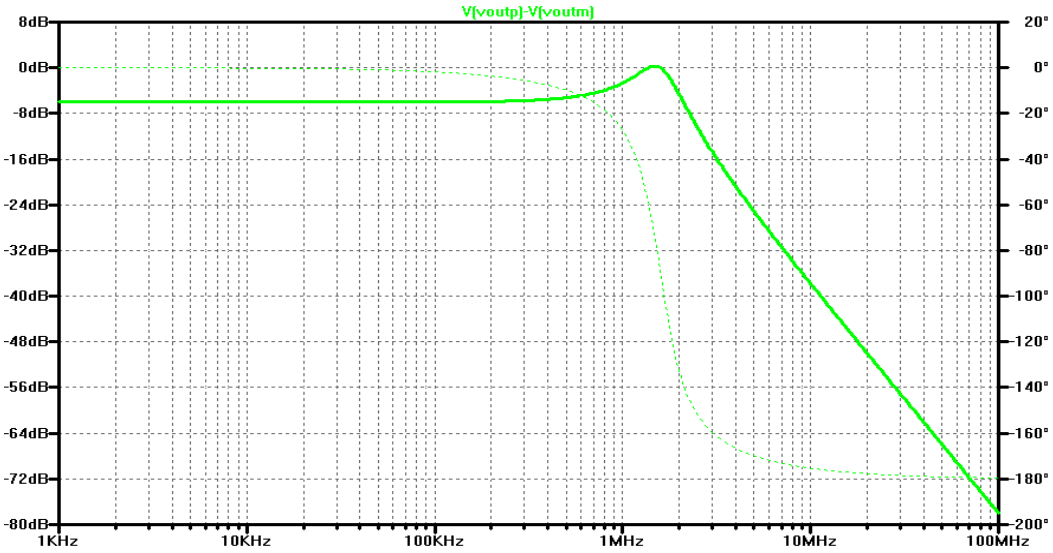


Q = .707, f_0 = 1.59 MHz, Gain = 1 (0dB).

Ex 2, Adjusted gain. R_{I1} (top and bottom) changed to 20k, for Gain = ½ (-6dB).



Ex 3, Same gain, with adjusted Q. New R_{F1} = 20k, new Q=2.



George Schwartz

Problem 3.13

What happens to the poles in the biquadratic equation, Eq. (3.62), if the Q is less than 0.5? Is the f_{max} equation in Fig. 3.35 valid?

Solution

First of all, we recognize that the poles in a biquadratic transfer function occur where the equation in the denominator is equal to zero. The equation for the denominator in the standard biquadratic transfer function is shown below.

$$P(f) = s^2 + (2\pi f_0/Q)s + (2\pi f_0)^2$$

If the Q of the filter is set equal to 0.5, the equation can be rewritten in the following way (since 1/0.5 = 2)

$$P(f) = s^2 + 2(2\pi f_0)s + (2\pi f_0)^2$$

Which is simply $(s + 2\pi f_0)^2$, which means that the filter will have a double pole at $s = -2\pi f_0$. If we remember the discriminant of a quadratic function ($b^2 - 4ac$) we see that this corresponds to the case where $b^2 - 4ac = 0$. This results in a repeated real value for the roots of our equation. Since the filter has only real poles at this point, this transfer function that can be realized by a cascade of two first-order filters.

Now let's see what will happen if we have a lower Q value. Having a lower value for Q corresponds to a larger coefficient for the linear term in the denominator of our transfer function. Having a larger linear term coefficient results in $b^2 - 4ac > 0$, which means that we will have two real poles in our transfer function. These roots will always be negative, which means that the filter will also always be stable (recalling from control system theory that when all poles are less than 0, the system will be stable). Also, this type of transfer function can be realized with the cascade of two first-order filters.

Finally, lets find when the equation in Fig. 3.35 is valid. It states in the discussion above the figure that the equation is only valid when Q is greater than 0.707. This is because the filter will only experience peaking when Q is greater than this value. This corresponds to the frequency at which the peaking will occur if Q is higher than that value. Since no peaking occurs for $Q < 0.707$, this equation is not valid and thus doesn't apply. Notice that if we make Q very high, Fmax will approach f_0.

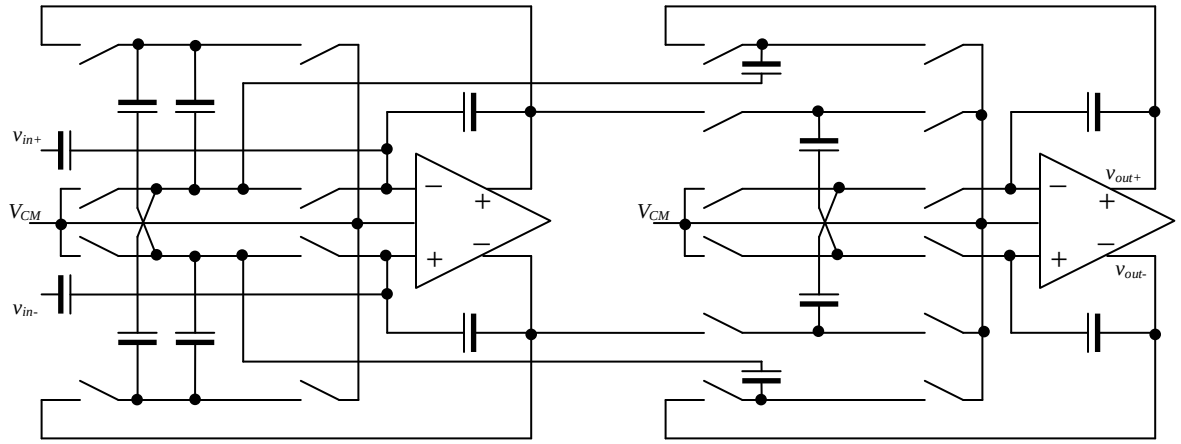
Jake Baker

3.14 Compare the size of the elements used in Exs. 3.8 and 3.9. Is there a benefit to using an active element for monolithic implementation?

The inductor in Ex. 3.8 can't be implemented on-chip hence this filter requires an off-chip inductor. The issues with adding an off-chip inductor include cost and the added parasitics associated with any signal moving on/off chip (e.g., a bonding capacitance). The active-RC filter in Ex. 3.9, however, can be implemented entirely on-chip. The largest area component in this filter, 10 pF, is still considerably smaller than the 100 pF capacitor in Ex. 3.8 and incomparably smaller than the 100 μH inductor from this same example. This makes the active-RC filter implementation the preferred solution to implement this filter in monolithic form (on a chip).

QAWI HARVARD – ECE615 (CMOS Mixed Signal Design) HW7

3.15 Show, using the simulations from Ex. 3.14, that increasing the switch resistance, and thus the spectral content present in a switched capacitor circuit, can help to stabilize high-Q switched-capacitor bandpass filters.

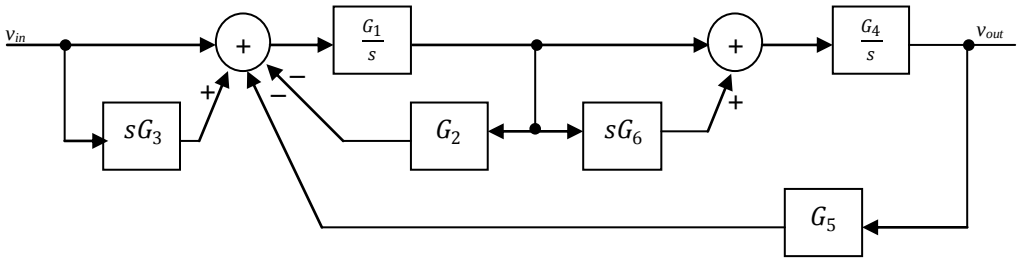


F-1 Switched-capacitor implementation of a high-Q filter

Before we add switching resistance to the schematic of Ex. 3.14 it is important to understand the transfer function of the bi-quad filter. This ensures that we understand how we select the topologies and how to determine the filters parameters.

$$\frac{v_{out}}{v_{in}} = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + \left(\frac{2\pi f_0}{Q}\right)s + (2\pi f_0)^2}$$

The implementation of this filter is accomplished when we consider the block diagram in F-2.



F-2 Block diagram of the implementation of the bi-quad transfer function

The analysis of F-2 is performed in the book and leads to the equations that allows us to select the gain terms in order to precisely set the parameters to develop the band-pass, low-pass, or all-pass filters used extensively in this section. The transfer function of F-2 is:

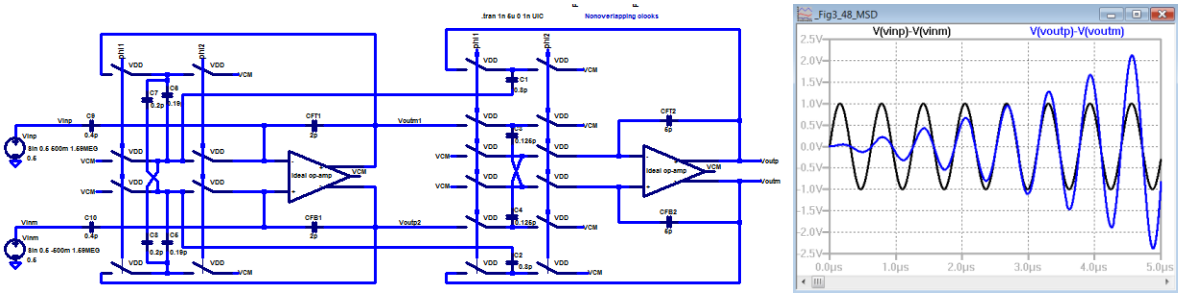
$$\frac{v_{out}}{v_{in}} = \frac{s^2 G_1 G_3 G_4 G_6 + s(G_1 G_3 G_4 + G_1 G_4 G_6) + G_1 G_4}{s^2 + s(G_1 G_2 + G_1 G_4 G_5 G_6) + G_1 G_4 G_5}$$

The transfer function of a second order low-pass filter is:

$$\frac{v_{out}}{v_{in}} = \frac{\frac{1}{LC}}{s^2 + s\frac{R}{L} + \frac{1}{LC}}$$

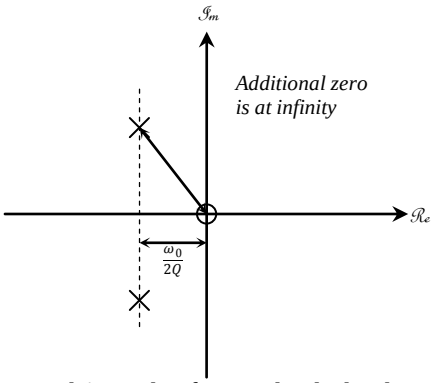
So if we want to use the bi-quad circuit to implement a second order low-pass filter we will set $a_2 = a_1 = 0$. To do this with our bi-quad block diagram implementation we can set $G_6 = G_3 = 0$, because that is the only way to remove the s and s^2 terms from the numerator without removing them from the denominator. More details are given in the book and should be understood before trying to complete this problem.

Let's now simulate the circuit in F-1 (Ex. 3.14) and show with simulations that increasing the switch resistance will improve stability. The LTSPICE schematic is seen in F-3 and is taken from the LTSPICE file provided on the book's website (*_Fig3_48_MSD.asc*).



F-3 LTSPICE schematic and simulation results showing instability for a high-Q second-order bandpass circuit

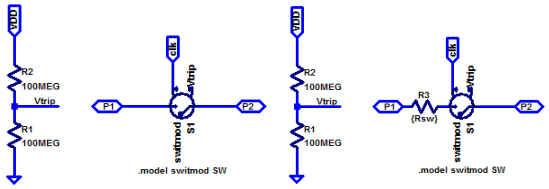
The reason for instability can be seen by examining the pole/zero plot of the second-order bandpass filter.



F-4 Pole/Zero plot of a second-order bandpass filter

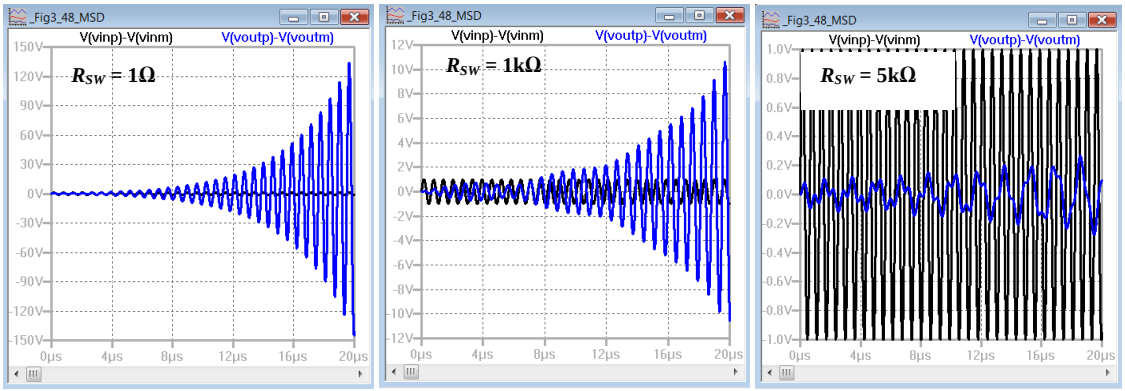
F-4 shows that for high-Q circuits the pole locations move closer to the right half plane, and poles in the right half plane will make the system unstable.

We can add switch resistance to the schematic by placing a resistor in series with the switch. We can do this for every switch in F-3, or we can modify the *switch_1.asc* schematic.



F-5 Adding switch resistance to the switch_1.asc schematic

The simulation results for varying switch resistances are seen below:



F-6 Simulation results of Ex.14 with varying simulation results

F-6 shows that the magnitude of oscillation decreases by a substantial amount. Increasing the switch resistance to a large value will eventually filter out the input signal. The analysis performed in Yantao Ma's original solution states that (paraphrasing):

1. "*Voltage drops on the resistors helps to reduce the positive feedback gain when the circuit is unstable and oscillating"*
2. *"The resistance helps to filter high frequency components associating with switching"*
3. *"The output is attenuated (filtered by switches R and the capacitive element) at f_0 and reduces the magnitude of the oscillation"*

Kaijun Li
Problem 3.16
Redesign and simulate the operation of the filter discussed in Ex 3.14, with a Q of 5, while trying to minimize the difference between C_{I1} and C_{F2}. Suggest a possible modification to the filter topology (similar to how we add G_{2Q} in Fig. 3.45) to reduce this component spread.

Solution:
In order to redesign the system to meet the specification, let us investigate how each parameter in the switch capacitor (SC) implementation affects the overall performance of the biquadratic filter.

The specification for this SC implementation is:

$$Q = 5,\ f_0 = 1.59MHz, A_v = 1$$

And these specs place requirement for relative parameters as follows:

(1) $$Q = R_{F1}\sqrt{\frac{C_{F1}}{R_{I2}C_{F2}R_{F2}}} = 5$$

As we know that $R_{F1} = \frac{1}{C_{I21} f_s}, R_{F2} = \frac{1}{C_{I22} f_s}, R_{I2} = \frac{1}{C_{I12} f_s}$, we have

$$Q = \frac{\sqrt{C_{I12}C_{I22}C_{F1}}}{\sqrt{C_{F2}} \cdot C_{I21}} = \frac{C_{F1}}{10\left(C_{I21} - C_{I21Q}\right)} \qquad (1)$$

(2) $$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{C_{F1}R_{I2}C_{F2}R_{F2}}} = 1.59MHz$$

Or $$\sqrt{\frac{f_s{}^2 C_{I12} C_{I22}}{C_{F1} C_{F2}}} = 10\ MHz \quad , \quad \sqrt{\frac{C_{I12}C_{I22}}{C_{F1}C_{F2}}} = 0.1$$

$$\frac{C_{I12}C_{I22}}{C_{F1}C_{F2}} = 0.01 \qquad (2)$$

(3) Passband gain $A_v = 1$, and it is assured by

$$a_1 = \frac{2\pi f_0}{Q} = \frac{10\times10^6}{Q} = \frac{C_{I1}}{R_{I2}C_{F1}C_{F2}} = \frac{1}{R_{F1}C_{F1}}$$

So we have the following relations:

$$\frac{10\times10^6}{Q} = \frac{f_s C_{I1} C_{I12}}{C_{F1}C_{F2}} = \frac{f_s C_{I21}}{C_{F1}}$$

$$\frac{0.1}{Q} = \frac{C_{I1}C_{I12}}{C_{F1}C_{F2}} = \frac{C_{I21}}{C_{F1}} \quad (3)$$

By combining the equations (1), (2) and (3), we have the following relations between capacitors' sizes.

$$\frac{C_{I1}}{C_{I22}} = \frac{10}{Q} \quad (4)$$

$$\frac{C_{I12}C_{I22}}{C_{F1}C_{F2}} = 0.01 \quad (5)$$

$$C_{I21} = \frac{C_{I1}C_{I12}}{C_{F2}} \quad (6)$$

It is noted that in the original design of Ex. 3.14 Q is 20, so the parameters needed to be adjusted are:

From equation (4), Q drops from 20 to 5, $\frac{C_{I1}}{C_{I22}}$ should be enlarged by 4. To meet the design goal of minimizing the difference between C_{I1} and C_{F2}, if C_{F2} is left out the same as 5pF, the size for C_{I1} can be chosen as 4.8pF (0.4 pF in Ex. 3.14) resulting C_{I22} to be 2.4pF (0.8 pF in Ex. 3.14) 83.33fF. In other words, compared to the values in Ex. 3.14, C_{I1} is 12 times larger, C_{I22} is 3 times and Q is 4 times, and equation (4) is still valid.

C_{I21} and C_{I21Q} are selected to be 0.6pF and 0.48pF with C_{F1} of 4pF to meet the equation (1) in which Q is 5.

C_{I12} is changed from 125fF to 83.33fF (two thirds smaller) since in equation (5) C_{I22} is 3 times larger than it is in Ex. 3.14 and C_{F1} is twice larger with C_{F2} staying the same.

After above analysis, simulation is performed in LTSpice, and the results are shown as follows. The simulation is 15us, and it starts saving data from 10us. So one way to check the input frequency change is by looking at the starting value for the input at 0us in the plot, which is actually the 10us for the simulation.

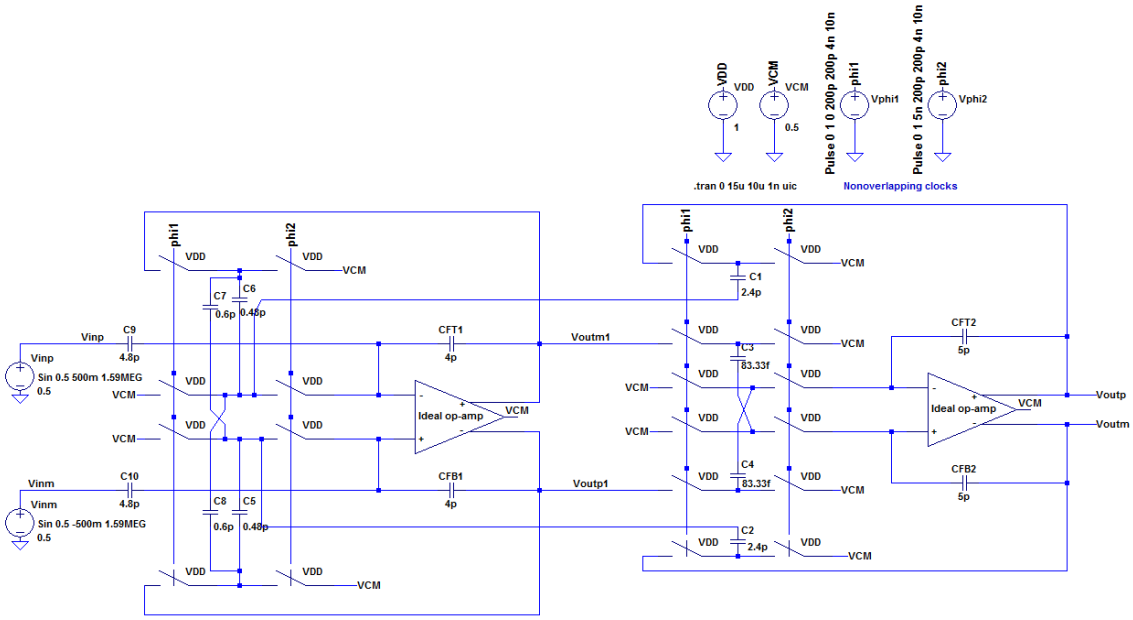


Fig. 3.16-1 Schematic for simulation

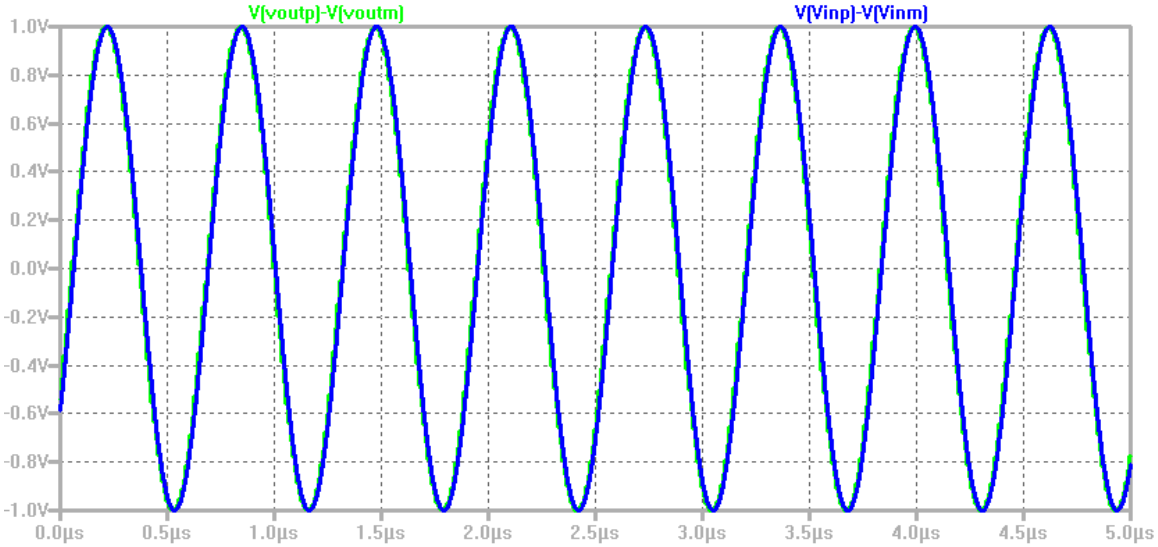


Fig.3.16-2 Input frequency is 1.59MHz

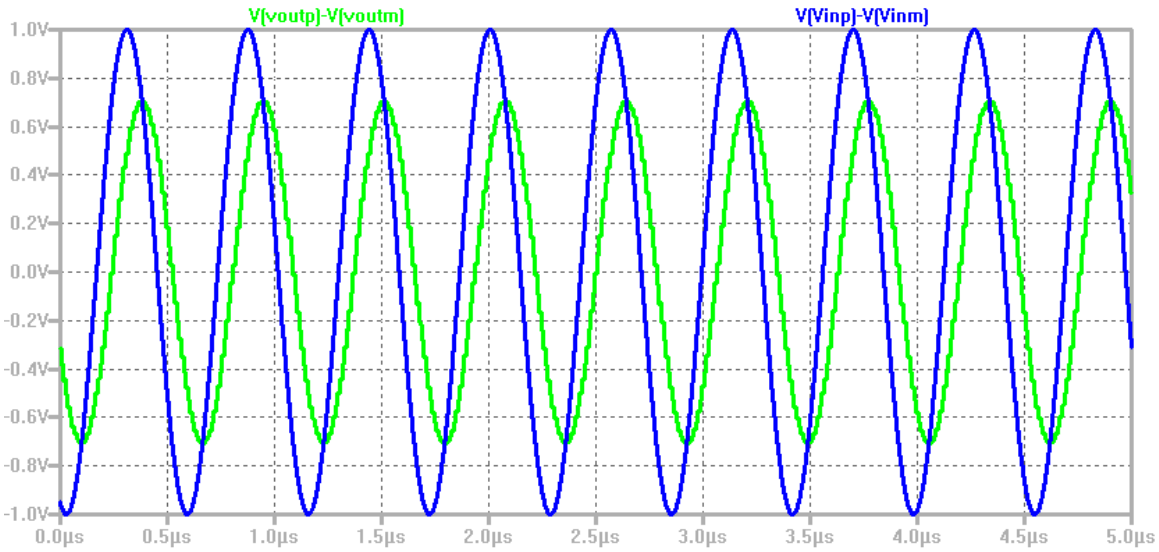


Fig.3.16-3 Input frequency is 1.45 MHz

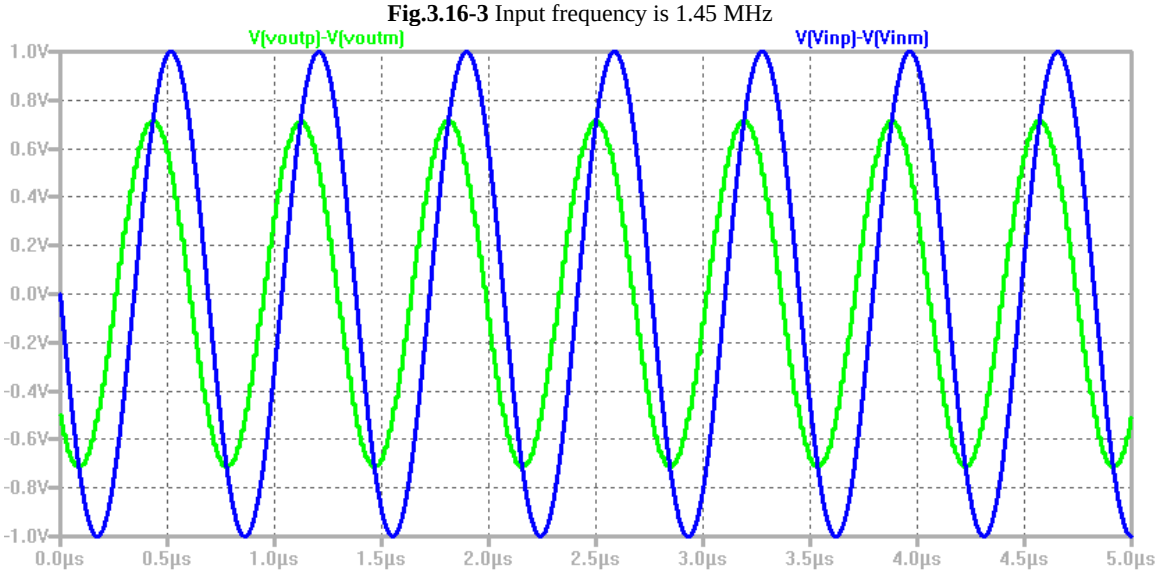


Fig.3.16-4 Input frequency is 1.77 MHz

It is noted that the 3dB frequency for this SC implementation are 1.45 MHz and 1.77 MHz respectively. And this means the actual Q is 1.59/(1.77-1.45)=4.93, which is pretty close to targeting value 5.

The two suggested topologies are shown in following two figures intending to minimize the component spread. It is noted that the negative feedbacks are introduced in order to reduce the component spread while maintaining the same transfer function.

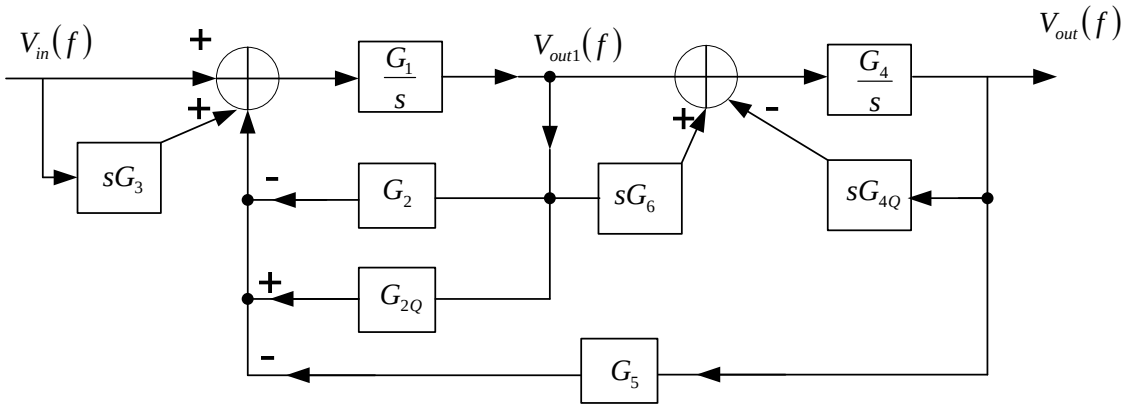


Fig.3.16-5 Topology 1 for reducing component spread

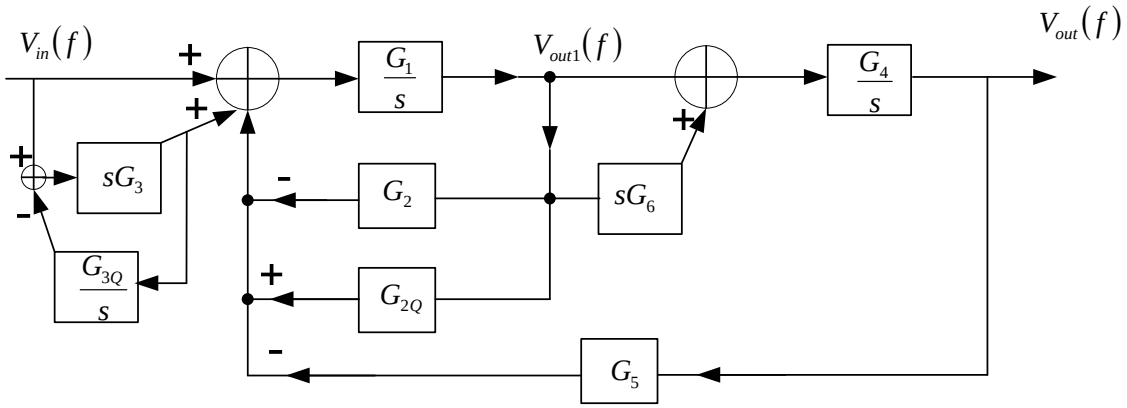


Fig.3.16-6 Topology 2 for reducing component spread

3.17) Show how to derive the transfer function of the transconductor-C biquad filter seen in Fig. 3.53. Can this filter be orthogonally tuned? If so, how?

Sol) Shown here is a transconductor-C biquad filter from Fig. 3.53 of the textbook

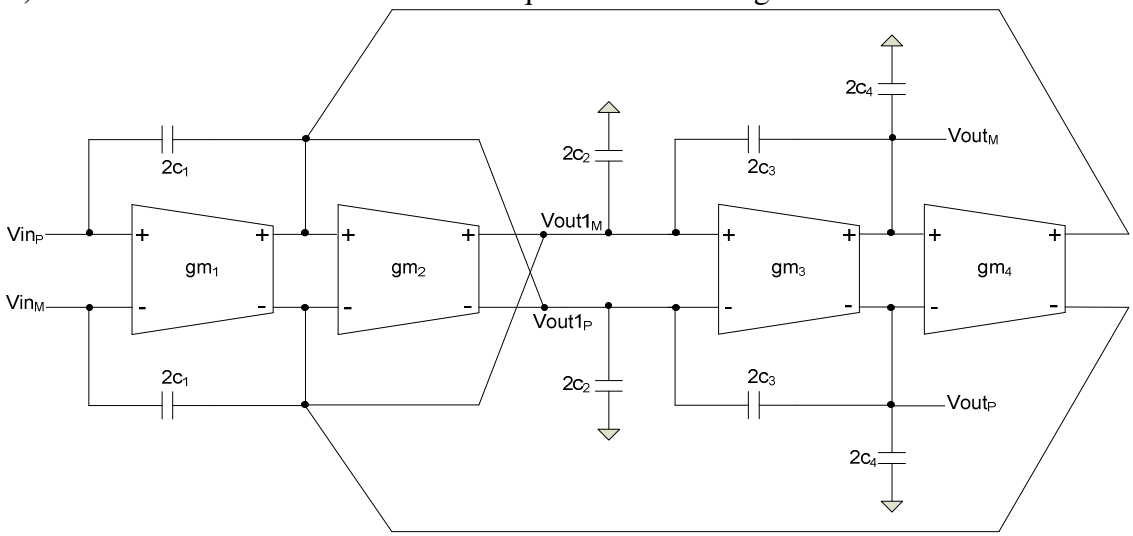


Figure 1: Transconductor-C Biquad Filter

To derive the transfer function, let's re-draw the first portion of the circuit as shown below,

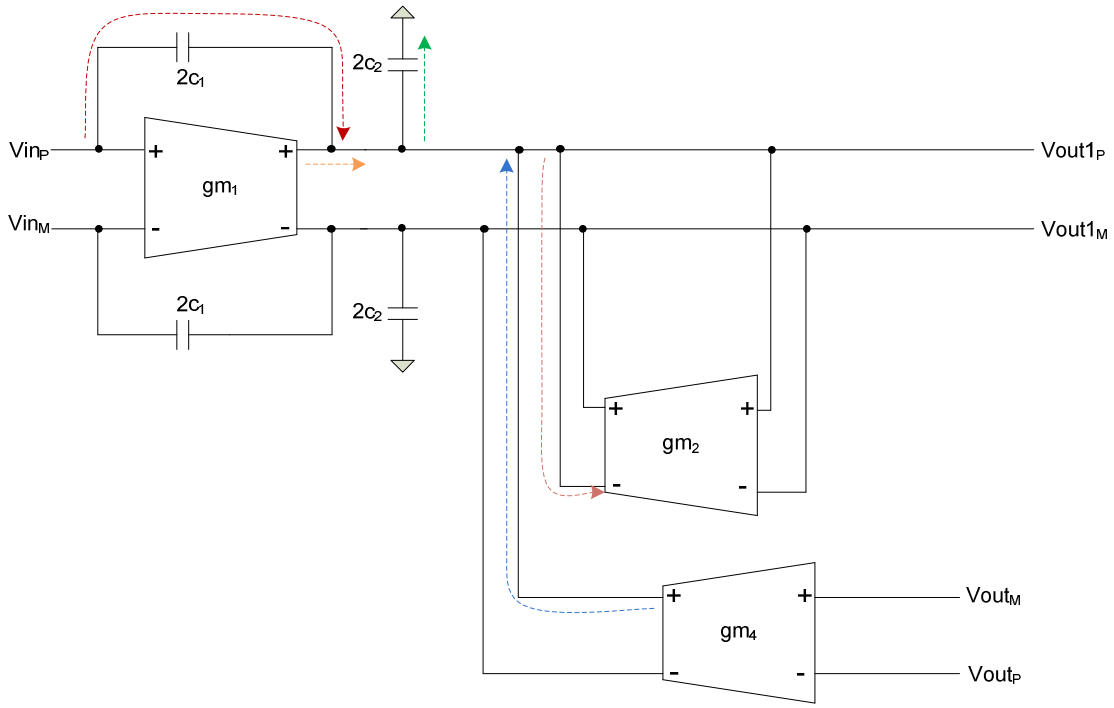


Figure 2: Only the first portion of the biquad filter is shown without the crossing wires to show how the feedback gain is implemented

Summing up the currents at the $Vout1_P$ node, we get

$$gm_1\left(Vin_P - Vin_M\right) + \left(\frac{Vin_P - Vout1_P}{1/s2C_1}\right) + \left(\frac{-Vout1_P}{1/s2C_2}\right) + \left[-gm_2\left(Vout1_P - Vout1_M\right)\right] + gm_4\left(Vout_M - Vout_P\right) = 0$$

[1]

$$gm_1\left(Vin_P - Vin_M\right) + s2C_1\left(Vin_P - Vout1_P\right) - s2C_2\left(Vout1_P\right) - gm_2\left(Vout1_P - Vout1_M\right) - gm_4\left(Vout_P - Vout_M\right) = 0$$

[2]

$$Vout_P = -Vout_M$$
$$Vout1_P = -Vout1_M$$

We also know that, $Vin_P = -Vin_M$

$$\frac{Vin_P}{1/s2C_1} = \frac{2 \cdot Vin_P}{1/sC_1} = \frac{Vin_P - Vin_M}{1/sC_1}$$

Using these equations, lets rewrite Eq. 2,

$$gm_1\left(Vin_P - Vin_M\right) + sC_1\left(2Vin_P - 2Vout1_P\right) - sC_2\left(2Vout1_P\right) - gm_2\left(Vout1_P - Vout1_M\right) - gm_4\left(Vout_P - Vout_M\right) = 0$$

[3]

$$gm_1\left(Vin_P - Vin_M\right) + sC_1\left(2Vin_P\right) - sC_1\left(2Vout1_P\right) - sC_2\left(2Vout1_P\right) - gm_2\left(Vout1_P - Vout1_M\right) - gm_4\left(Vout_P - Vout_M\right) = 0$$

[4]

$$gm_1\left(Vin_P - Vin_M\right) + sC_1\left(Vin_P - Vin_M\right) - sC_1\left(Vout1_P - Vout1_M\right) - sC_2\left(Vout1_P - Vout1_M\right) - gm_2\left(Vout1_P - Vout1_M\right) - gm_4\left(Vout_P - Vout_M\right) = 0$$

[5]

$$\left(Vin_P - Vin_M\right)\left(gm_1 + sC_1\right) - \left(gm_2 + s\left(C_1 + C_2\right)\right)\left(Vout1_P - Vout1_M\right) - gm_4\left(Vout_P - Vout_M\right) = 0 \quad \textbf{[6]}$$

$$Vout1_P - Vout1_M = \frac{\left(gm_1 + sC_1\right)\left(Vin_P - Vin_M\right) - gm_4\left(Vout_P - Vout_M\right)}{\left(gm_2 + s\left(C_1 + C_2\right)\right)} \quad \textbf{[7]}$$

Now, let's look at the second portion of the transconductor-C biquad filter and write the nodal equations for the currents getting summed up at the output $Vout_P$.

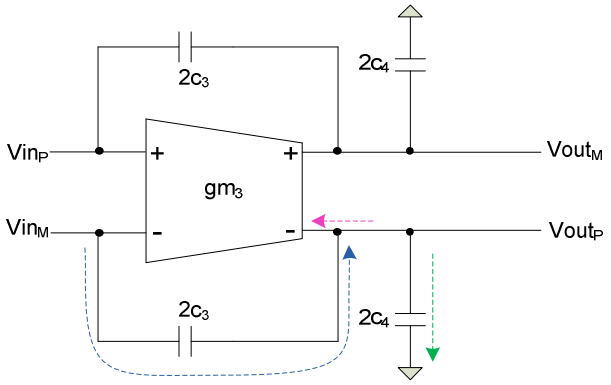


Figure 3: Only the output end of the biquad filter is shown here

$$-gm_3\left(Vout1_M - Vout1_P\right) + \left(\frac{Vout1_P - Vout_P}{1/s2C_3}\right) + \left(\frac{-Vout_P}{1/s2C_4}\right) = 0 \quad \textbf{[8]}$$

$$gm_3\left(Vout1_P - Vout1_M\right) + s2C_3\left(Vout1_P - Vout_P\right) - s2C_4\left(Vout_P\right) = 0 \quad \textbf{[9]}$$

$$gm_3\left(Vout1_P - Vout1_M\right) + sC_3\left(2Vout1_P\right) - sC_3\left(2Vout_P\right) - sC_4\left(2Vout_P\right) = 0 \textbf{ [10]}$$

$$gm_3\left(Vout1_P - Vout1_M\right) + sC_3\left(Vout1_P - Vout1_M\right) - sC_3\left(Vout_P - Vout_M\right) - sC_4\left(Vout_P - Vout_M\right) = 0 \textbf{ [11]}$$

$$\left(gm_3 + sC_3\right)\left(Vout1_P - Vout1_M\right) - s\left(C_3 + C_4\right)\left(Vout_P - Vout_M\right) = 0 \textbf{ [12]}$$

$$\left(gm_3 + sC_3\right)\left(Vout1_P - Vout1_M\right) = s\left(C_3 + C_4\right)\left(Vout_P - Vout_M\right) \textbf{ [13]}$$

Substituting Eq. 7 in Eq. 13 we get,

$$\left(gm_3 + sC_3\right)\frac{\left(gm_1 + sC_1\right)\left(Vin_P - Vin_M\right) - gm_4\left(Vout_P - Vout_M\right)}{\left(gm_2 + s\left(C_1 + C_2\right)\right)} = s\left(C_3 + C_4\right)\left(Vout_P - Vout_M\right) \textbf{ [14]}$$

$$\left(gm_3 + sC_3\right)\left[\left(gm_1 + sC_1\right)\left(Vin_P - Vin_M\right) - gm_4\left(Vout_P - Vout_M\right)\right] = \left\langle gm_2 + s\left(C_1 + C_2\right)\right\rangle \cdot \left\{s\left(C_3 + C_4\right)\right\} \cdot \left(Vout_P - Vout_M\right) \textbf{ [15]}$$

$$\left(gm_3 + sC_3\right) \cdot \left(gm_1 + sC_1\right)\left(Vin_P - Vin_M\right) = \left[gm_4\left(gm_3 + sC_3\right) + \left\langle gm_2 + s\left(C_1 + C_2\right)\right\rangle \cdot \left\{s\left(C_3 + C_4\right)\right\}\right] \cdot \left(Vout_P - Vout_M\right) \textbf{ [16]}$$

$$\left(gm_3 + sC_3\right) \cdot \left(gm_1 + sC_1\right)\left(Vin_P - Vin_M\right) = \left[gm_3 \cdot gm_4 + gm_4 \cdot sC_3 + sgm_2\left(C_3 + C_4\right) + s^2\left(C_1 + C_2\right)\left(C_3 + C_4\right)\right] \cdot \left(Vout_P - Vout_M\right) \textbf{ [17]}$$

$$\frac{Vout_P - Vout_M}{Vin_P - Vin_M} = \frac{\left(gm_3 + sC_3\right) \cdot \left(gm_1 + sC_1\right)}{s^2\left(C_1 + C_2\right)\left(C_3 + C_4\right) + s\left[gm_4C_3 + gm_2\left(C_3 + C_4\right)\right] + gm_3gm_4} \textbf{ [18]}$$

$$\frac{Vout_P - Vout_M}{Vin_P - Vin_M} = \frac{s^2C_1C_3 + s\left(gm_3C_1 + gm_1C_3\right) + gm_1gm_3}{s^2\left(C_1 + C_2\right)\left(C_3 + C_4\right) + s\left[gm_4C_3 + gm_2\left(C_3 + C_4\right)\right] + gm_3gm_4} \textbf{ [19]}$$

Dividing the numerator and denominator by $\left(C_1 + C_2\right)\left(C_3 + C_4\right)$,

$$\frac{Vout_P - Vout_M}{Vin_P - Vin_M} = \frac{s^2\frac{C_1C_3}{\left(C_1 + C_2\right)\left(C_3 + C_4\right)} + s\left(\frac{gm_3C_1 + gm_1C_3}{\left(C_1 + C_2\right)\left(C_3 + C_4\right)}\right) + \frac{gm_1gm_3}{\left(C_1 + C_2\right)\left(C_3 + C_4\right)}}{s^2 + s\left(\frac{gm_4C_3 + gm_2\left(C_3 + C_4\right)}{\left(C_1 + C_2\right)\left(C_3 + C_4\right)}\right) + \frac{gm_3gm_4}{\left(C_1 + C_2\right)\left(C_3 + C_4\right)}} \textbf{ [20]}$$

So finally, the transfer function of a transconductor-C biquad filter is given by,

$$\frac{Vout_P - Vout_M}{Vin_P - Vin_M} = \frac{s^2\frac{C_1C_3}{\left(C_1 + C_2\right)\left(C_3 + C_4\right)} + s\left(\frac{gm_3C_1 + gm_1C_3}{\left(C_1 + C_2\right)\left(C_3 + C_4\right)}\right) + \frac{gm_1gm_3}{\left(C_1 + C_2\right)\left(C_3 + C_4\right)}}{s^2 + s\left(\frac{gm_2}{\left(C_1 + C_2\right)} + \frac{gm_4C_3}{\left(C_1 + C_2\right)\left(C_3 + C_4\right)}\right) + \frac{gm_3gm_4}{\left(C_1 + C_2\right)\left(C_3 + C_4\right)}} \textbf{ [21]}$$

From Eq. 3.70 on Pg. 100 of the textbook, we have the general equation for the transfer function of the biquad filter as,

$$\frac{Vout_P - Vout_M}{Vin_P - Vin_M} = \frac{s^2 G_1 G_3 G_4 G_6 + s\left(G_1 G_3 G_4 + G_1 G_4 G_6\right) + G_1 G_4}{s^2 + s\left(G_1 G_2 + G_1 G_4 G_5 G_6\right) + G_1 G_4 G_5} \quad \textbf{[22]}$$

Comparing Eq. 22 to Eq. 21 we have

$$G_1 = \frac{gm_1}{\left(C_1 + C_2\right)} \qquad G_2 = \frac{gm_2}{gm_1} \qquad G_3 = \frac{C_1}{gm_1}$$

$$G_4 = \frac{gm_3}{\left(C_3 + C_4\right)} \qquad G_5 = \frac{gm_4}{gm_1} \qquad G_6 = \frac{C_3}{gm_3}$$

This biquad filter can be orthogonally tuned, where the locations of poles and zeros can be moved without affecting the other's location. From the equations above, C_4 and gm_4 can be tuned without effecting the other terms. Using this, we can tune the location of the poles and zeros and can create a required filter.

3.18. Repeat Ex 3.9 using the transconductor-based biquad.
Sol.

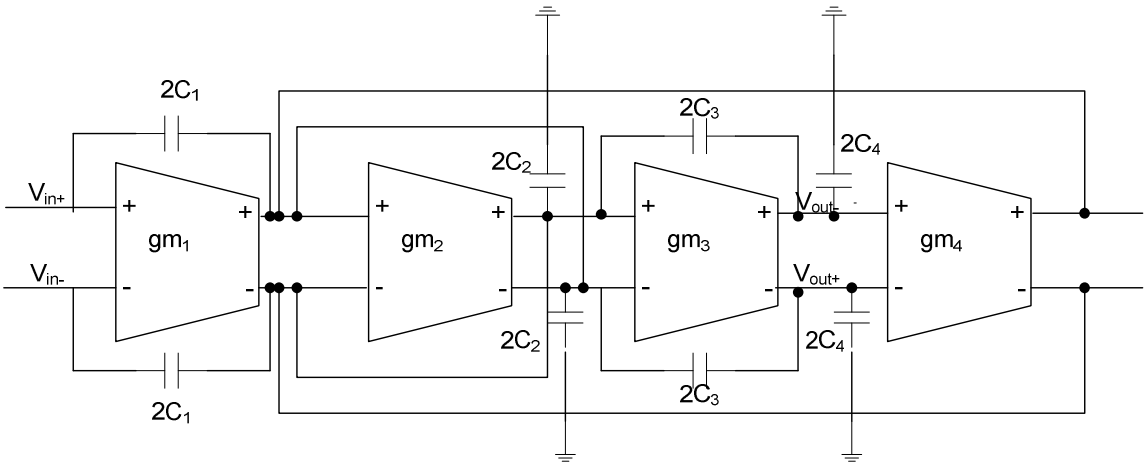


Figure 1. Implementing a biquad low pass filter using transconductors

The transfer function of the biquad shown in Figure 1 is given by

$$\left(\frac{V_{out+}-V_{out-}}{V_{in+}-V_{in-}}\right)=\frac{s^2G_1G_3G_4G_6+s(G_1G_3C_4+G_1G_4G_6)+G_1G_4}{s^2+s(G_1G_2+G_1G_4G_5G_6)+G_1G_4G_5} \quad (1)$$

For a low pass filter C1=C3=0

As stated in equation 3.62 in the book the transfer function is also given by

$$\left(\frac{V_{out+}-V_{out-}}{V_{in+}-V_{in-}}\right)=\frac{a_2s^2+a_1s+a_0}{s^2+\left(\frac{2\pi f_0}{Q}\right)s+(2\pi f_0)^2} \quad (2)$$

Comparing the denominator in (1) and (2) we have

$$G_1G_2+G_1G_4G_5G_6=\left(\frac{2\pi f_0}{Q}\right) \quad (3)$$

$$G_1G_4G_5=(2\pi f_0)^2 \quad (4)$$

But we know for low pass filter $C_1=C_3=0$ and hence the below equations follow.

$G_1 = \frac{gm_1}{C1 + C_2} = \frac{gm_1}{C}$ **as C_1=0 and assuming C_2=C_4=C**

$G_2 = \frac{gm_2}{gm_1}$

$G_3 = \frac{C_1}{gm_1} = 0$ **as C1=0**

$G_4 = \frac{gm_3}{C4} = \frac{gm_3}{C}$

$G_5 = \frac{gm_4}{gm_1}$

$G_6 = \frac{C_3}{gm_3} = 0$ **as C3=0**

From equation (3) we have

$$\left(\frac{2\pi f_0}{Q}\right) = \frac{gm_1}{C} \times \frac{gm_2}{gm_1} = \frac{gm_2}{C}$$

$$2\pi f_0 = \frac{gm_2}{C} \times Q \qquad (5)$$

From equation (4) we have

$$2\pi f_0 = \sqrt{G_1 G_4 G_5}$$

$$2\pi f_0 = \frac{\sqrt{gm_3 \times gm_4}}{C} \qquad (6)$$

From equation (5) and (6) we have

$$\frac{gm_2}{C} \times Q = \frac{\sqrt{gm_3 \times gm_4}}{C}$$

$$gm_2 = \frac{\sqrt{gm_3 \times gm_4}}{Q} \qquad (7)$$

Assuming gm_1=gm_3=gm_4=gm and substituting in (7) we get

$gm_2 = \frac{gm}{Q}$ Assuming the value of gm=gm_3=gm_4=100 uA/V and given Q=0.707 we have

gm_2=141 uA/V

Substituting the value of gm_2 in equation (5) we get **C=C_2=C_4=10 pF**

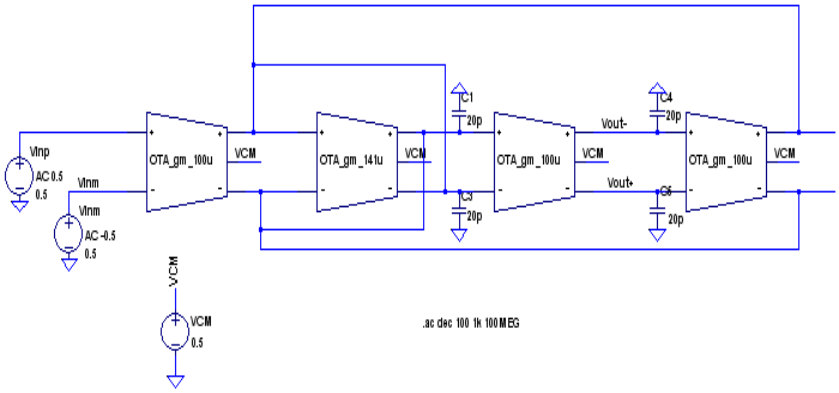


Figure 2. LTspice schematic for biquad low pass filter

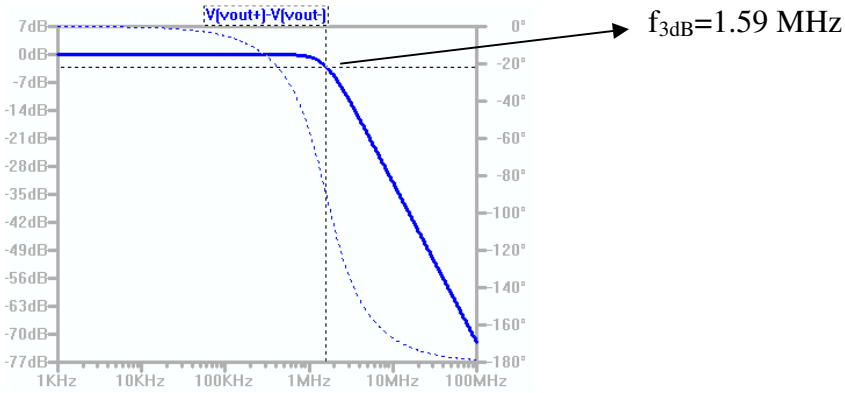


Figure 3. frequency response of biquad transconductor lowpass filter

The gain at dc is $\frac{gm_4}{gm_1}$ i.e. 0 dB as verified in simulation (see Figure 3).

3.19 How would a "high-Q" biquad be implemented using transconductors? Repeat Ex. 3.12 using the transconductor-based biquad.

Solution:

Ex. 3.12 asks for a bandpass filter with the following specifications:

$$\begin{aligned} f_o &= 1.59\ \text{MHz} \rightarrow \omega_o = 10\ \text{MHz} \\ Q &= 20 \\ A_{\text{passband}} &= 1 \rightarrow\ 0\,\text{dB} \end{aligned} \tag{1}$$

Let's get started by writing the filter's transfer function

$$\frac{v_{\text{out}}}{v_{\text{in}}} = \frac{a_1 s}{s^2 + \left(\frac{2\pi f_o}{Q}\right)s + (2\pi f_o)^2} \tag{2}$$

To minimize the component spread, we can use the topology show in the Fig. 3.44 in [1]. The biquad implementation using transconductors (gm-C) is shown in Fig. 1.

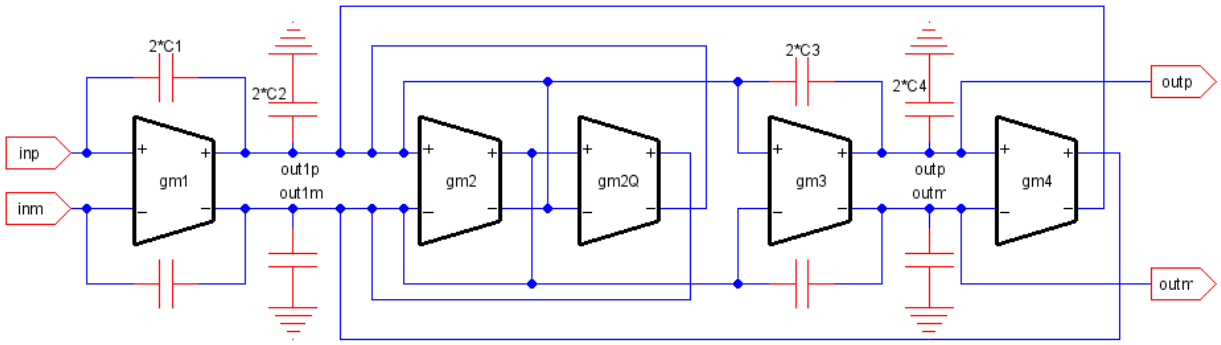


Figure 1 Implementation of "high-Q" gm-C biquad transfer function filter.

Now let's derive the transfer function for this biquad gm-C filter. First, we apply KCL to node **out1p**, or

$$\begin{aligned} &(v_{\text{in+}} - v_{\text{in-}})\cdot g_{m1} + (v_{\text{in+}} - v_{\text{out1+}})\cdot s2C_1 - v_{\text{out1+}}\cdot s2C_2 - (v_{\text{out+}} - v_{\text{out-}})\cdot g_{m4} \\ &-(v_{\text{out+}} - v_{\text{out-}})\cdot g_{m2} + (v_{\text{out1+}} - v_{\text{out1-}})\cdot g_{m2Q} = 0 \end{aligned} \tag{3}$$

Knowing

$$\begin{aligned} v_{\text{in}} &= v_{\text{in+}} - v_{\text{in-}} = 2v_{\text{in+}} \\ v_{\text{out}} &= v_{\text{out+}} - v_{\text{out-}} = 2v_{\text{out+}} \\ v_{\text{out1}} &= v_{\text{out1+}} - v_{\text{out1-}} = 2v_{\text{out1+}} \end{aligned} \tag{4}$$

we can rewrite Eq. 3 as

$$v_{\text{in}}(g_{m1} + sC_1) = v_{\text{out1}}[s(C_1 + C_2) + g_{m2} - g_{m2Q}] + v_{\text{out}}g_{m4} \tag{5}$$

Next we apply KCL to node **outp**

$$(v_{\text{out1+}}-v_{\text{out1-}})\cdot g_{m3}+(v_{\text{out1+}}-v_{\text{out+}})\cdot s\,2C_3-2\,v_{\text{out+}}\cdot sC_4=0 \tag{6}$$

Again, using Eq. 4, we can rewrite Eq. 6 as

$$v_{\text{out1}}=v_{\text{out}}\cdot\frac{s(C_3+C_4)}{sC_3+g_{m3}} \tag{7}$$

With Eqs. 5 and 7, we can relate the input, v_{in}, and the output, v_{out}

$$\frac{v_{\text{out}}}{v_{\text{in}}}=\frac{s^2(C_1C_3)+s(g_{m1}C_3+g_{m3}C_1)+g_{m1}g_{m3}}{s^2(C_1+C_2)(C_3+C_4)+s[g_{m4}C_3+(g_{m2}-g_{m2Q})(C_3+C_4)]+g_{m3}g_{m4}} \tag{8}$$

Comparing Eq. 8 with Eq. 2, we can make $a_2=a_0=0$ by setting $g_{m1}=0$ and $C_3=0$. Note that we cannot set $g_{m3}=0$ and $C_1=0$ since we will end up getting $(2\pi f_o)^2=0$ if doing so. The transfer function for setting g_{m1} and C_3 to zero and having $g_{m2Q}=g_{m2}\cdot\frac{Q-1}{Q}$ is

$$\frac{v_{\text{out}}}{v_{\text{in}}}=\frac{s\cdot\frac{g_{m3}C_1}{(C_1+C_2)C_4}}{s^2+s\cdot\frac{g_{m2}}{(C_1+C_2)Q}+\frac{g_{m3}g_{m4}}{(C_1+C_2)C_4}} \tag{9}$$

Thus

$$\begin{aligned} a_1&=\frac{g_{m3}C_1}{(C_1+C_2)C_4}\\ \frac{2\pi f_o}{Q}&=\frac{g_{m2}}{(C_1+C_2)Q}\\ (2\pi f_o)^2&=\frac{g_{m3}g_{m4}}{(C_1+C_2)C_4}\end{aligned} \tag{10}$$

For simplicity we can set $g_{m2}=g_{m3}=g_{m4}=10\,\mu A/V$, then (C_1+C_2) and C_4 must be 1 pF in order to satisfy the requirement of $f_o=1.59\,\text{MHz}$. Since we also want the passband gain to be 1, or

$$A_{\text{passband}}=\frac{a_1Q}{2\pi f_o}=\frac{g_{m3}C_1}{(C_1+C_2)C_4}\cdot\frac{Q}{2\pi f_o}=\frac{(10\,\mu A/V)\cdot C_1}{(1\,\text{pF})(1\,\text{pF})}\cdot\frac{20}{10\,\text{MHz}}=1 \tag{11}$$

we have $C_1=0.05\,\text{pF}$ and $C_2=0.95\,\text{pF}$. And $g_{m2Q}=g_{m2}\cdot Q/(Q-1)=9.5\,\mu A/V$. The "high-Q" biquad transconductor bandpass filter using these component values and the SPICE simulation are shown in Fig. 2. Note that for $g_{m1}=0$ and $C_3=0$, we simply remove these components from the circuit.

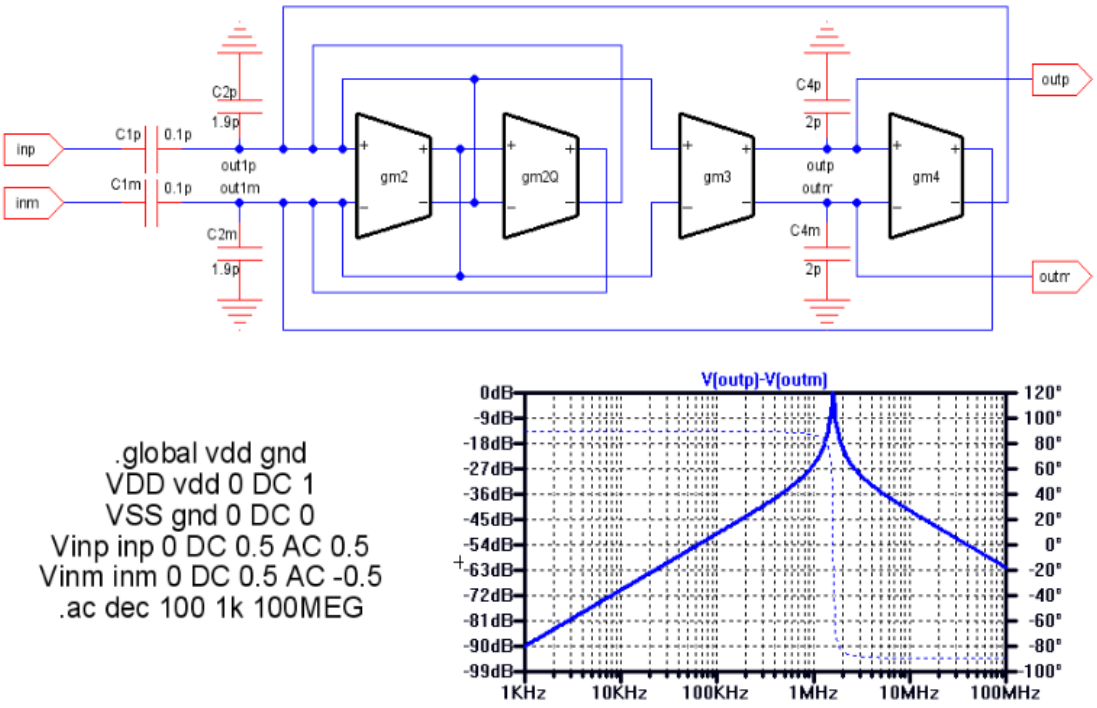


Figure 2 The "high-Q" transconductor biquad bandpass filter and the simulation.

Reference:

[1] R. J. Baker, *CMOS Mixed-signal Circuit Design, Second Edition*, Wiley-IEEE, 2009.

3.20 Show, using biquad section, how the lowpass ladder filter seen in Fig. 3.56 can be implemented.

Solution:

In order to implement Fig. 3.56 in [1] using biquad sections, we can first divide the lowpass ladder filter into three sections as shown in Fig. 1. Each section ($H_1 \sim H_3$) can be implemented using biquad filter section ($HB_1 \sim HB_3$). We the can design each of the biquad sections so they have the same frequency responses as the original circuit, or

$$H_k(s) = HB_k(s), k = 1, 2, 3 \tag{1}$$

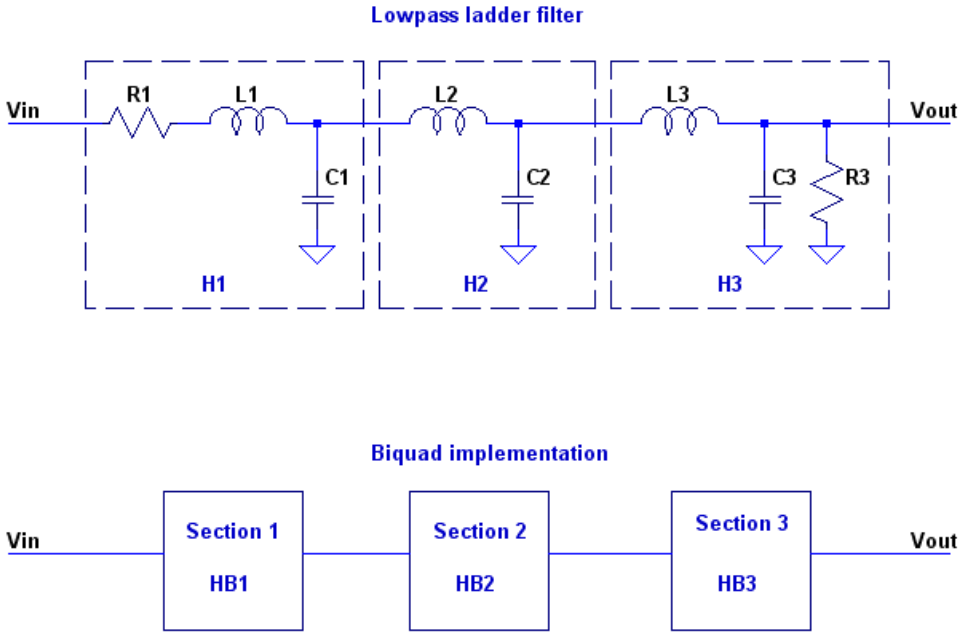


Figure 1 Implementating a lowpass ladder filter using biquad sections.

Next, we write down $H(s)$ for the each original section, or

$$\begin{aligned} H_1(s) &= \frac{1/L_1C_1}{s^2 + sR_1/L_1 + 1/L_1C_1} \\ H_2(s) &= \frac{1/L_2C_2}{s^2 + 1/L_2C_2} \\ H_3(s) &= \frac{1/L_3C_3}{s^2 + s/R_3L_3 + 1/L_3C_3} \end{aligned} \tag{2}$$

A biquad filter has a transfer function

$$HB(s)=\frac{a_2 s^2+a_1 s+a_0}{s^2+\left(2\pi\frac{f_o}{Q}\right)s+(2\pi\ f_o)^2} \tag{3}$$

In order to satisfy Eq. 1 (so each biquad section has the same transfer function as the original circuit), we need to properly design each biquad section so their transfer function have the desired coefficients ($a_{2,}a_{1,}a_{0,}f_o,$ and Q). Comparing Eq. 3 with Eq. 2, we can have

1) For Section 1,

$$\begin{aligned} &a_2=a_1=0, a_0=\frac{1}{L_1C_1} \\ &Q=\frac{1}{R_1}\sqrt{\frac{L_1}{C_1}} \\ &2\pi\ f_o=\sqrt{\frac{1}{L_1C_1}} \end{aligned} \tag{4}$$

2) For Section 2,

$$\begin{aligned} &a_2=a_1=0, a_0=\frac{1}{L_2C_2} \\ &Q=\infty \\ &2\pi\ f_o=\sqrt{\frac{1}{L_2C_2}} \end{aligned} \tag{5}$$

3) For Section 3,

$$\begin{aligned} &a_2=a_1=0, a_0=\frac{1}{L_3C_3} \\ &Q=R_3\sqrt{\frac{C_3}{L_3}} \\ &2\pi\ f_o=\sqrt{\frac{1}{L_3C_3}} \end{aligned} \tag{6}$$

The biquads with above coefficients can be implemented using either active-RC, transconductor-C, or SC filter.

Reference:

[1] R. J. Baker, *CMOS Mixed-signal Circuit Design, Second Edition*, Wiley-IEEE, 2009.