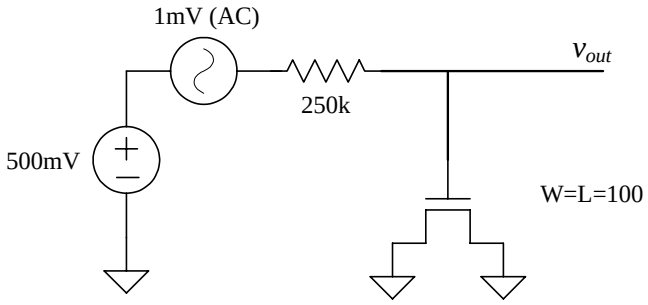
6.1) Plot the magnitude and phase of v_{out} (AC) in the following circuit, Fig. 6.20. Assume that the MOSFET was fabricated using the 50nm process (see Table 5.1) and is operating in strong inversion. Verify your answer with SPICE.

Sol: -From Fig. 6.20



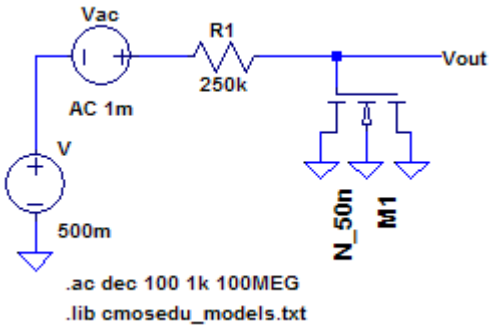
MOSFET is operating in strong inversion region and source, drain and body are connected to ground (body connection not shown). The device acts as MOSCAP, value of this capacitance can be calculated with the help of table 5.1 for 50nm process.

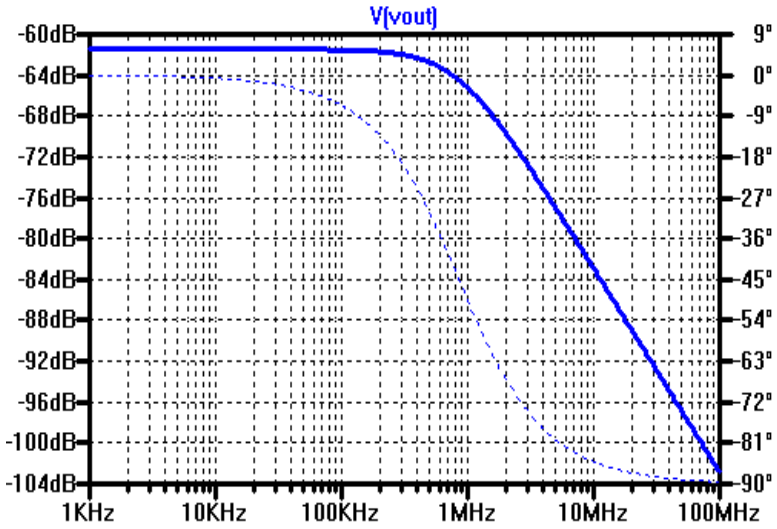
$C_{total} = C'_{ox} \times W \times L = 25fF/\mu m^2 \times (100\times 50nm) \times (100\times 50nm) = 25fF/\ \mu m^2 \times 25\ \mu m^2$; $C_{total} = 625fF$

For 1mV AC input the circuit functions as low pass RC circuit with voltage divider equation given as :-

$$Vout = Vin\left[\frac{1/j2\pi fC_{total}}{R + 1/j2\pi fC_{total}}\right] = \frac{Vin}{1 + j2\pi fRC_{total}}; \quad |Vout| = \frac{Vin}{\sqrt{1+(2\pi fRC_{total})^2}}; \quad \angle Vout = -\tan^{-1}(2\pi fRC_{total})$$

3db frequency for this case will be $f_{3db} = \frac{1}{2\pi RC_{total}} \approx 1MHz$ thus simulating the circuit from frequency of 1 kHz to 100MHz





In the above simulation plot we can see the RC response of the circuit. The magnitude plot is at approximately -60 db due to the fact that Vin taken as 1mV which will be equal to -60db. Also at the 1MHz the phase is approximately 45° and magnitude around -63db.

-Shantanu Gupta

Problem 6.2 **Rupa Balan**

If a MOSFET is used as a capacitor in the strong inversion region where the gate is one electrode and the source/drain is the other electrode, does the gate overlap of the source/drain change the capacitance? Why? What is the capacitance?

Solution:- In the strong inversion region, the channel of electrons is formed below the gate oxide in case of NMOS shorting the drain and the source.
Since source and drain of NMOS are shorted through channel of electrons, gate overlap of source/drain does not change the gate to source/drain capacitance.
Capacitance between gate and source/drain $=C_{ox}=C'_{ox}$. W. L. $(\text{scale})^2$

where $W=W_{drawn}$ and $L=L_{drawn}$.

Problem 6.3 **Krishna Duvvada**

Repeat problem 6.2 when the MOSFET is operating in the accumulation region. Keep in mind that the question is not asking for the capacitance from gate to substrate.

Solution:- When the MOSFET operates in the accumulation region, the gate overlap capacitance affects the capacitance from gate to source/drain. Here the drain and source is separated by the substrate which is the resistance. So the gate to drain/source capacitance is the overlap capacitance.

$$Cgs = C'_{ox}.\ Ldiff.\ W\ (\text{scale})^2$$

Problem 6.4 **Surendranath C Eruvuru**

If the oxide thickness of a MOSFET is 40 A^o. What is C'_{ox}?

Solution:- $C'_{ox} = \varepsilon_{ox}/T_{ox} = (8.85 \times 3.97\ aF/\mu m)/(40 \times 10^{-10}\ m) =$ $\underline{8.784\ fF/\mu m^2}$

KRISHNAMRAJU KURRA

Problem 6.5. Repeat Ex: 6.5 to get a threshold voltage of 0.8V.

Solution: Given $V_{GS} = V_{THN}$ and $V_{SB} = 1V$

Then $V_S = - V_{fp} + V_{SB}$

Where $V_{fp} = -(KT/q) \ln (N_A/n_i)$

$= -26 \text{ mV} * \ln [10^{15} (\text{atoms/cm}^3) / 1.45 * 10^{10} (\text{atoms/cm}^3)]$

$= -290\text{mV}$

We have $X_d = \sqrt{[2 \times \varepsilon_{si} \times |-2V_{fp} + V_{SB}| / qN_A}$

$=$

$$\sqrt{\left[2\times 11.7\times 8.85\times 10^{-18}\left(F/\mu m^2\right)\times\left|\left(-2\times -.29\right)+1\right|V/\left(1.6\times 10^{-19}\left(C/atom\right)\right)\times 10^{15}\left(atoms/cm^3\right)\left(cm^3/10^{12}\,\mu m^3\right)\right]}$$

$= 1.43 \ \mu m$

We have $Q'_{bo} = q \times N_A \times X_d$

$= \left(1.6\times 10^{-19}\left(C/atom\right)\right)\times 10^{15}\left(atoms/cm^3\right)\left(cm^3/10^{12}\,\mu m^3\right) \times 1.43 \ \mu m$

$= 229 \text{ aC}/\mu m^2$

PROBLEM 6.6 **Indira Priyadarshini.Vemula**

Repeat Ex. 6.3 for a p-channel device with a well doping concentration of 10^{16} atoms/cm^3?

Solution:

Given $N_D = 10^{16}$ atom/cm^3

$\gamma = (2q \in_{si} N_D)^{1/2} / C_{ox}'$

$$\gamma = \frac{(2*1.6*10^{-19}\text{ C/atom}*11.7*8.85\text{ aF/um}^2*10^{16}\text{ atom/cm}^3 * \text{cm}^3/10^{12}\text{ um}^2)^{1/2}}{1.75\text{ fF/um}^2}$$

$\gamma = 0.328 V^{1/2}$

Problem 6.7 **MESHACK P. APPIKATLA**

What is the electrostatic potential of the oxide-semiconductor interface when $V_{GS}=V_{THNO}$.

Solution: It will be equal and opposite to the electrostatic potential of the substrate.

Vs = -Vfp

Where Vs is the electrostatic potential of the interface and Vfp is the electrostatic potential of the substrate.

Problem 6.8 **Edward Kunz**

Estimate the ion implant dose required to change the threshold voltage in Ex. 6.4 without Sodium contamination, to 0.8v.

Solution: Using values from Ex. 6.4

$$V_{THNO}=-0.220v+\frac{qN_I}{C'_{OX}}=0.8\text{v}$$

$$C'_{OX}=1.75\,{}^{fF}\!/_{\mu m^2}$$

$$q=1.6*10^{-19}\,{}^{C}\!/_{atom}$$

$$0.8v=-0.220v+\frac{1.6*10^{-19}{}^{C}\!/_{atom}*N_I}{1.75\,{}^{fF}\!/_{\mu m^2}}$$

$$N_I=1.115*10^{12}\,{}^{atoms}\!/_{cm^2}$$

Problem 6.9 **Vinay Dindi**

What happens to the threshold voltage in Problem 6.8 if sodium contamination of 100e9 sodium ions/cm2 is present at the oxide-semiconductor interface?

Solution: Given Ni=100E+9 atoms/cm2=1000 atoms/um2
From E.q (6.22) and (6.23) and the results from Ex.6.4
Vthno= -220mv - qNs/C`ox + qNi/C`ox
From Prob 6.8), we know –220mv + qNi/C`ox=0.8
So, Vthno with sodium contamination= 0.8 – (1.6E-19*1000/1.75fF)= 0.7

Problem 6.10 **Satish Dulam**

How much charge (enhanced electrons) is available under the gate for conducting a drain current at the drain-channel interface when Vds = Vgs – Vthn? Why? Assume the MOSFET is operating in strong inversion, Vgs > Vthn.

Solution: In Strong inversion, the amount of charge present at any point in the channel is given by Eq 6.28. At the drain, V(y) is equal to Vds. Given that Vds is Vgs-Vthn. From Eq 6.28, the charge at the drain is zero. When the drain and source are held at ground and the gate voltage is greater than the Vthn, the MOS is already in strong inversion and the channel is uniform along the y-direction. As the drain voltage is increased, the positive voltage at the drain is removing the electrons from the inverted channel. When the drain voltage reaches (Vgs-Vthn), the net charge present at the drain is zero.

Problem 6.11 **Rahul Mhatre**

Show the details of the derivation for Eq. (6.33) for the PMOS device.

Solution:

Since the device is a PMOS MOSFET, source and drain are p+ regions and the substrate is an nwell. Therefore, all the bulk is the most positive terminal and source is more positive than drain and gate. We follow the voltage convention of **Figure 6.1** in the book. Also, the threshold for PMOS device (V_{THP}) is a negative quantity.

Consider the **Figure 6.11,** where $V_{SG} > |V_{THP}|$, so that the surface under the oxide is inverted and $V_{SD} > 0$, causing a drift current to flow from the source to the drain.

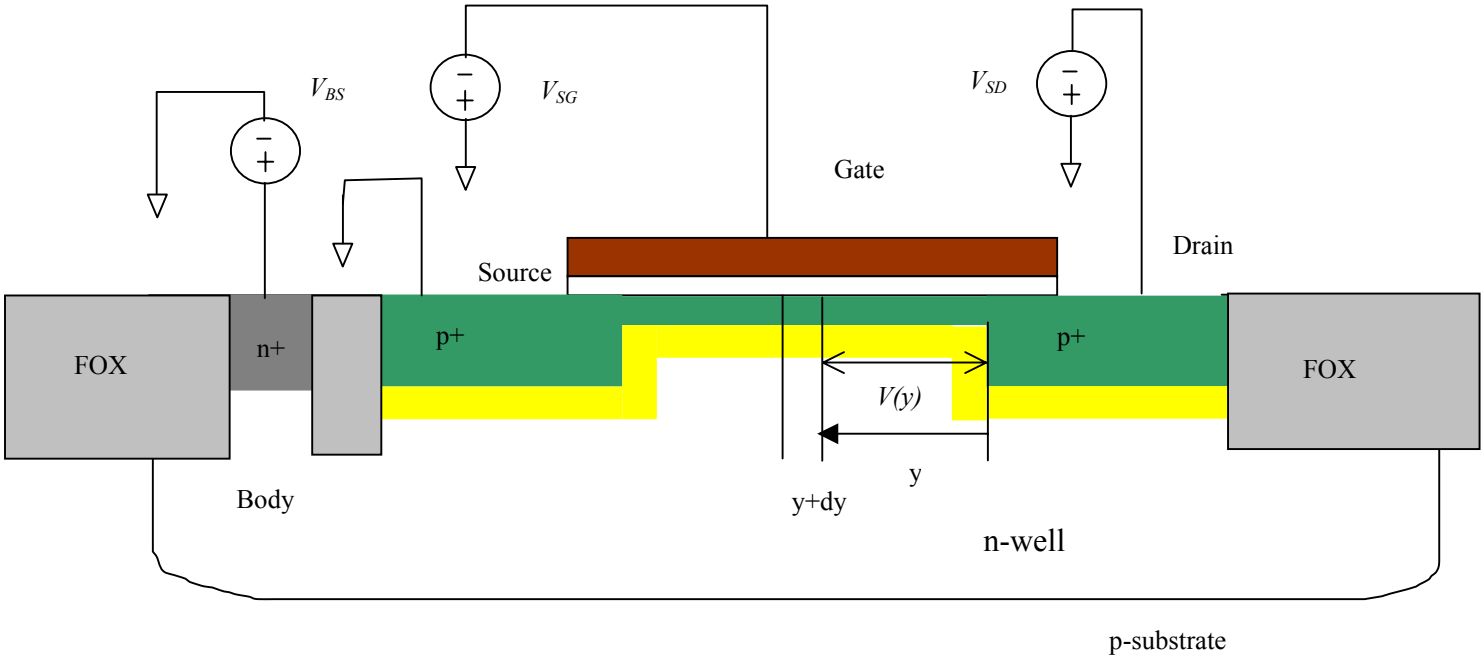


Figure 6.11 Calculation of large-signal behavior of the PMOS MOSFET in the triode region

V(y) is the channel voltage with respect to the source of the PMOS (a negative quantity) at a distance *y* away from the source. The potential difference between the Gate electrode and the channel is $V_{SG} - V(y)$. The charge/unit area in the inversion layer is given by

$$Q'_{ch} = C'_{ox}.\,[V_{SG} - V(y)\,] \qquad \text{Eq (6.1)}$$

Charge Q'_b (holes) is present in the inversion layer from the application of the threshold voltage, V_{THP}, necessary for conduction between the drain and source. This charge is given by,

$$Q'_b = C'_{ox}. |V_{THP}| \qquad \text{Eq(6.2)}$$

The total charge available in the channel, for conduction of a current between the source and the drain, is given by the difference between **Equation (6.1)** and **Equation (6.2)**, which is

$$Q'_I(y) = C'_{ox}. [V_{SG} - V(y) - |V_{THP}|] \qquad \text{Eq(6.3)}$$

where is the charge in the inverted channel.

The differential resistance of the channel region with a length dy and a width W is given by,

$$dR = (1/ \mu_p Q'_I(y)) .dy/W \qquad \text{Eq(6.4)}$$

where μ_p is the average hole mobility through the channel with units cm^2/V.sec.

The differential voltage drop across this differential resistance is given by

$$dV(y) = I_D . dR = I_D . dy / (W \mu_p Q'_I(y)) \qquad \text{Eq(6.5)}$$

Substituting Equation (6.) and rearranging

$$I_D . dy = W \mu_p C'_{ox}. [V_{SG} - V(y) - |V_{THP}|] . dV(y) \qquad \text{Eq(6.6)}$$

We define the transconductance of the PMOS MOSFET as,

$$KP_p = \mu_p C'_{ox} = \mu_p \varepsilon_{ox} / t_{ox} \qquad \text{Eq(6.7)}$$

The current can be found by integrating the left side of **Equation (6.6)** from source to drain, that is from 0 to L and the right side from 0 to V_{SD}. This current flows from source to drain. This is as shown below:

$$I_D . {}_0\int^L dy = W KP_p {}_0\int^{VSD} [V_{SG} - V(y) - |V_{THP}|] . dV(y) \qquad \text{Eq(6.8)}$$

$$I_D = KP_p (W/L) [(V_{SG} - |V_{THP}|) V_{SD} - (V_{SD}^2 / 2)]$$
$$\text{for } V_{SG} > |V_{THP}| \text{ and } V_{SD} \leq V_{SG} - |V_{THP}| \qquad \text{Eq(6.9)}$$

This current flows from Source to drain.

Problem 6.12 **John Spratt**

Using Eq. (6.35) estimate the small-signal channel resistance (the change in the drain current with changes in the drain-source voltage) of a MOSFET operating in the triode region (the resistance between the drain and source.

Solution:

Eq 6.35: $I_D=\beta*[(V_{gs}-V_{thn})V_{ds}-V_{ds}^2/2]$

$r = \Delta V_{ds} / \Delta ID$

$= (V_{ds1}- V_{ds2}) / [(\beta*[(V_{gs}-V_{thn})*(V_{ds1})-(V_{ds1})^2/2]- \beta*[(V_{gs}-V_{thn})*(V_{ds2})-(V_{ds2})^2/2]]$

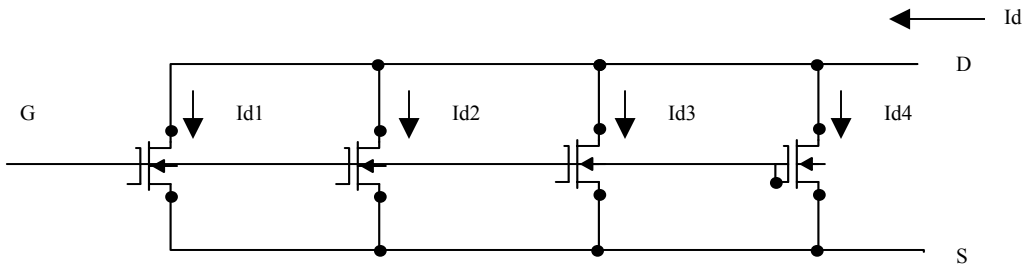
$= (V_{ds1}- V_{ds2}) / [(\beta*[(V_{gs}-V_{thn})*(V_{ds1}- V_{ds2})-(V_{ds1})^2/2+(V_{ds2})^2/2]]$

$=1 / [(\beta*[(V_{gs}-V_{thn})-(V_{ds1}+ V_{ds2})/2]]$

$r =1 / [\beta*(V_{gs}-V_{thn}- V_{ds})]$

Problem 6.13 **Steve Bard**

Question: Show, using Eqs. 6.33 and 6.37, that the parallel connection of MOSFETs shown in Fig. 5.18 behaves as a single MOSFET with a width equal to the sum of the individual MOSFET's widths.



Equivalent of Fig. 5.18

Solution: From Kirchoff's Current Law, we know that Id = Id1 + Id2 + Id3 + Id4. So if each MOSFET has the same KP, L, V_{GS}, V_{DS} and V_{THN}, equations 6.33 and 6.37 become:

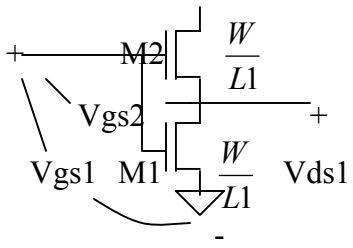
$$Id = KP_n \cdot \frac{W1+W2+W3+W4}{L} \cdot \left[(V_{GS} - V_{THN})V_{DS} - \frac{V_{DS}^{\ 2}}{2} \right] \qquad \text{for Eq. 6.33}$$

$$Id = KP_n \cdot \frac{W1+W2+W3+W4}{L} \cdot \left[(V_{GS} - V_{THN})^2 \right] \qquad \text{for Eq. 6.37}$$

This shows that the total drain current, Id, is equal to a single MOSFET with a width equal to W1 + W2 + W3 + W4.

Problem 6.14 **Shambhu Roy**

Show that the bottom MOSFET. Fig 6.21. in a series connection of two MOSFETs cannot operate in the saturation region. Neglect the body effect. Hint: Show that M1 is always in either cutoff ($V_{GS1} < V_{THN}$) or triode ($V_{DS1`} < V_{GS1} - V_{THN}$).



Solution:

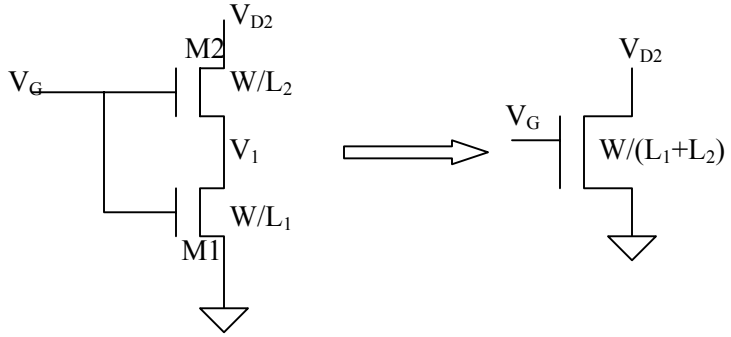
For $V_{GS1} < V_{THN}$ both MOSFETs are in the cutoff region.
When $V_{GS1} > V_{THN}$

$V_{DS1} = V_{GS1} - V_{GS2}$
Also
$V_{DS1} \geq V_{GS1} - V_{THN}$
$\Rightarrow V_{GS1} - V_{GS2} \geq V_{GS1} - V_{THN}$
$\Rightarrow V_{GS2} < V_{THN}$
Which cannot be true, therefore if top MOSFET has to operate then the bottom MOSFET cannot be in Saturation.

Problem 6.15 **Harish Reddy Singidi**

Show that the series connection of MOSFETs shown in fig. 6.21 behaves as a single MOSFET with Twice the length of the individual MOSFETs. Again neglect the body effect.

Solution:



Assuming both MOSFETs are in triode region

For M_1 $I_{D1} = I_D$

$I_{D1} = I_D = KP_n (W/L_1) [(V_G – V_{THN})V_1 - V_1^2/2]$

$(I_D L_1)/ (KP_n W) = [(V_G – V_{THN})V_1 - V_1^2/2]$

As Both MOSFETs are in series i.e., $I_{D1} = I_{D2} = I_D$

For M_2 $I_{D2} = I_D$

$I_{D2} = I_D = KP_n (W/L_2) [(V_G – V_1 - V_{THN})(V_{D2}-V_1) - (V_{D2}-V_1)^2/2]$

$(I_D L_2)/ (KP_n W) = [(V_G – V_1 - V_{THN})(V_{D2}-V_1) - (V_{D2}-V_1)^2/2]$

$[(I_D L_1)/ (KP_n W)] + [(I_D L_2)/ (KP_n W)] = [(V_G – V_{THN})V_1 - V_1^2/2] + [(V_G – V_1 - V_{THN})(V_{D2}-V_1) - (V_{D2}-V_1)^2/2]$

$[(I_D (L_1+L_2)/ (KP_n W)] = [(V_G – V_{THN}) V_{D2} - (V_{D2})^2/2]$

This is the current from drain to source for a single MOSFET with length (L_1+L_2)

If $L1 = L_2 = L$

$[(2I_D L)/ (KP_n W)] = [(V_G – V_{THN}) V_{D2} - (V_{D2})^2/2]$

$I_D = [(KP_n W)/2L] [(V_G – V_{THN}) V_{D2} - (V_{D2})^2/2]$