Cory Eskridge
EE411 Final
Problem 24.1

Common mode voltage V_{cm} is defined as the voltage applied to the inputs of a differential amplifier when the inputs are tied together. In other words, applying equal voltage to plus and minus terminals.

The minimum common-mode voltage that can be applied to a differential amplifier is the common-mode voltage that can be applied to the gates and still keep the MOSFETs operating in the saturation region. For this amplifier, V_{CMMIN} can be calculated using equation 22.11:

22.11) $$V_{CMMIN} = V_{GS1,2} + 2 \cdot V_{DS,sat}$$

To reduce V_{CMMIN} for this circuit, there are two methods we will look at. From the equation, we can see that by reducing either of the two terms, we will reduce V_{CMMIN}.

To reduce the second part of the equation, the $2V_{DS,sat}$, we can eliminate one of the transistors in the bias portion of the circuit. This will reduce V_{CMMIN} by $V_{DS,sat}$, since the voltage to keep the transistors in saturation will only have to drop across 1 transistor, instead of 2. Using the parameters from table 9.2, this results in a drop in V_{CMMIN} of 50 mV. This can be seen when comparing the simulation outputs between figure 1 and figure 2. The peak of the derivative of V_{out} corresponds to point where the transistors are switching from off or linear to saturation, and is therefore the definition of V_{CMMIN}. The simulation indicates a drop of about 40 mV.

The second method for reducing V_{CMMIN} is to reduce the first part of equation 22.11, the V_{GS}. This can be accomplished by using wider devices, as is apparent in the modified NMOS square law equation 2 (neglecting body effect):

2) $$V_{GS} = V_{thn} + \sqrt{\frac{2 \cdot I_{DS,sat} \cdot L}{KP_n \cdot W}}$$

This equation shows that to reduce V_{GS} we can increase the width of the device. Due to the biasing of the circuit, the other parameters can not be changed. Again using the parameters in table 9.2, and increasing the width of the devices from 50 to 100, we get a reduction in V_{CMMIN} of 50 mV. This reduction is can be seen in simulations when comparing figures 1 and 3 as about 60 mV, due to the body effect adjusting the threshold voltage, which was not taken into account in equation 2.

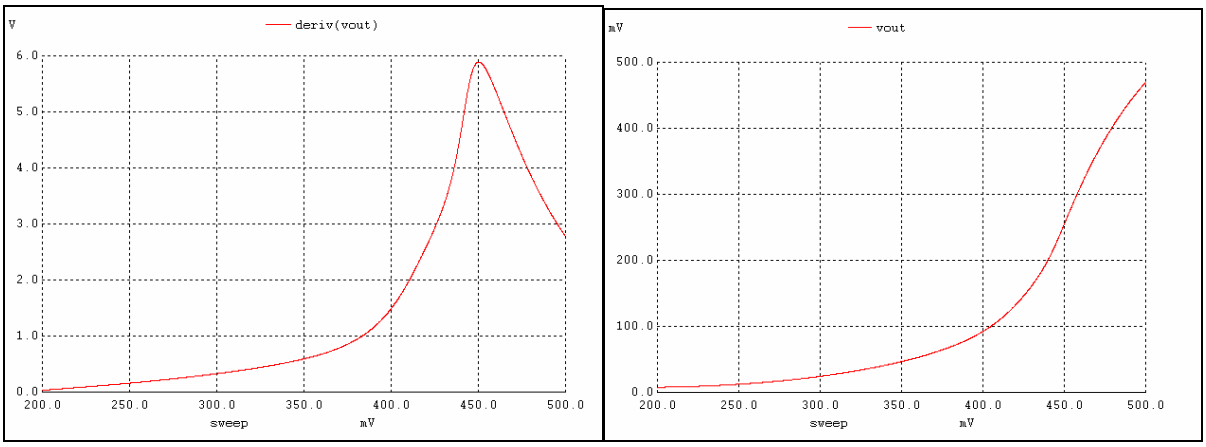


Figure 1 - Response of given circuit

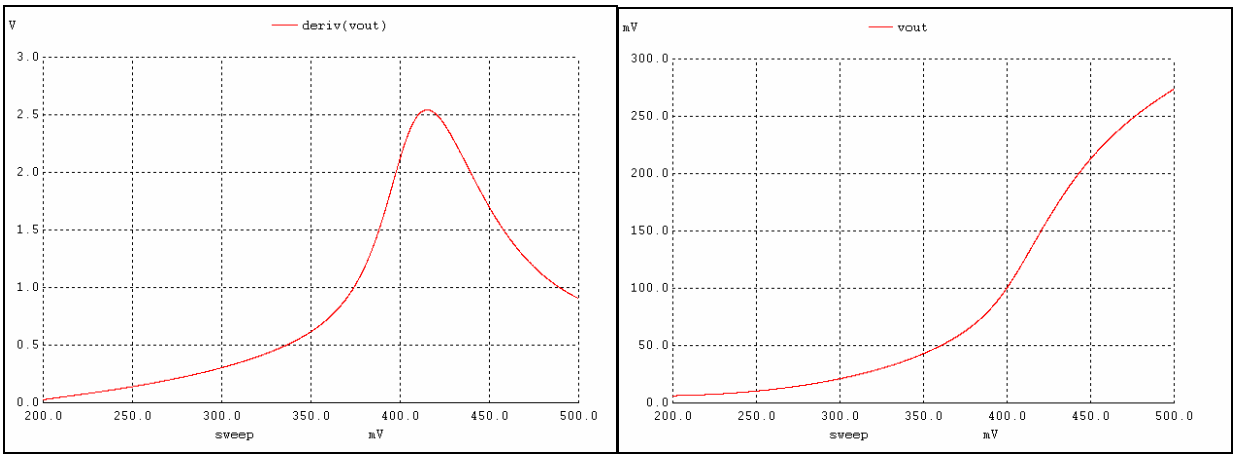


Figure 2 - Response with single bias transistor

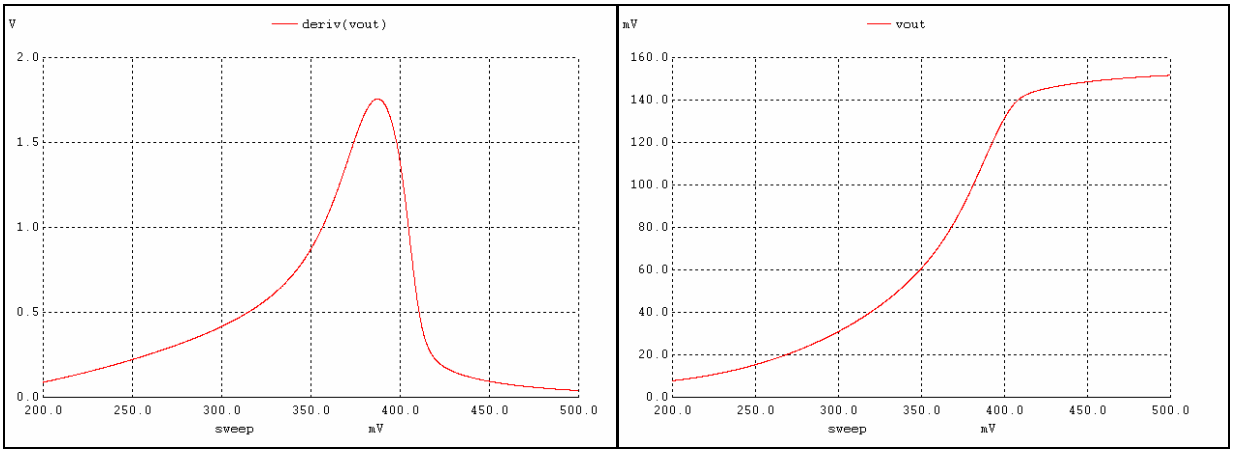


Figure 3 - response with wider devices

Other effects:
Solution 1 gives higher gain-bandwidth product because of the higher speed associated with the single transistor (figure 4, 5).

Solution 2 results in lower gain-bandwidth product, as parasitic poles are introduced (see pole splitting). This can be seen in figure 6. The open loop gain for solution 2 is lower than the given circuit, and the gain looks to fall off at 20db/dec, as opposed to 40db/dec for the given circuit. The g_m of solution 2 is higher than either solution, as can be seen by the slope of the derivative of V_{out} graphs in figures 1-3.

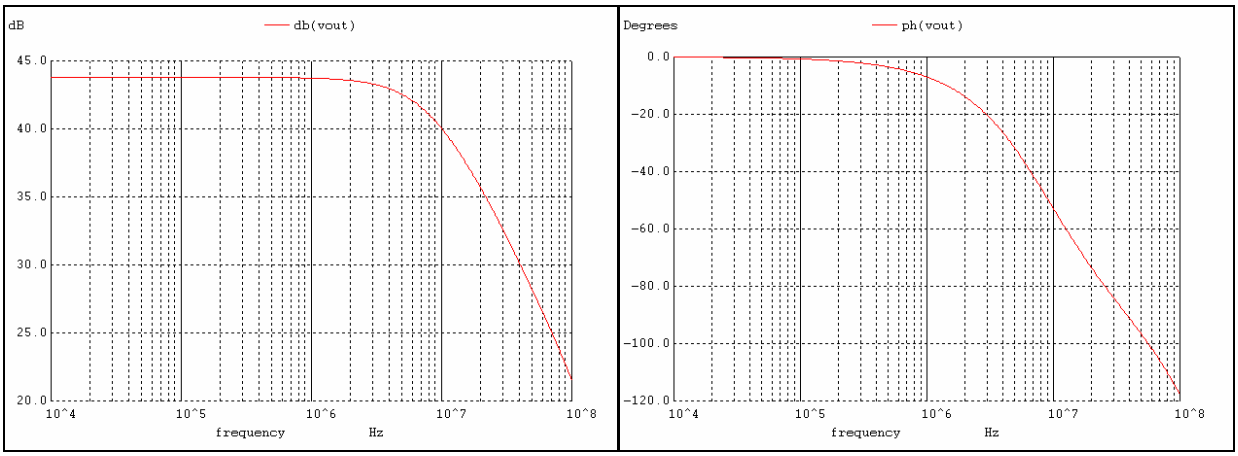


Figure 4 - frequency response for given circuit

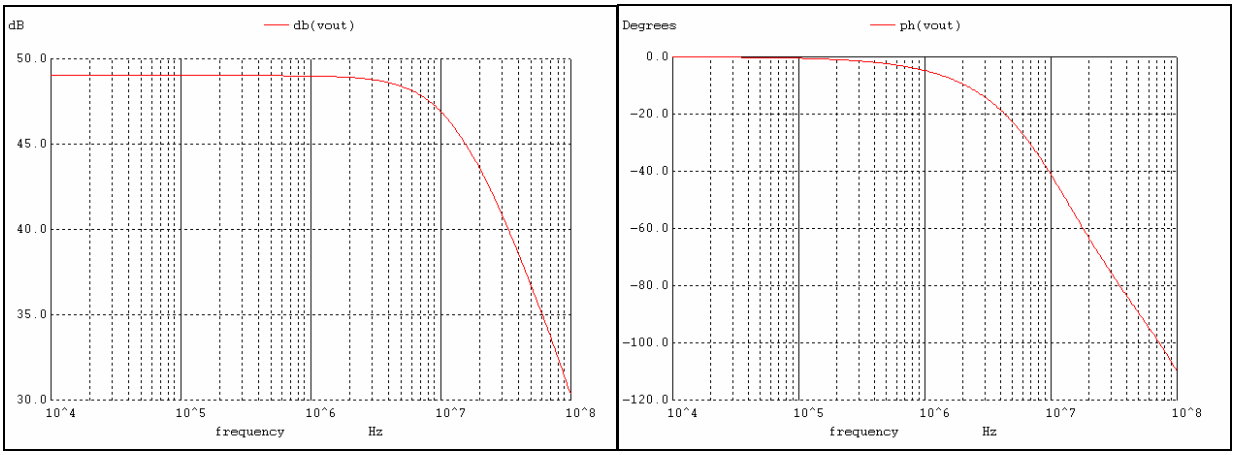


Figure 5 - frequency response for single bias transistor

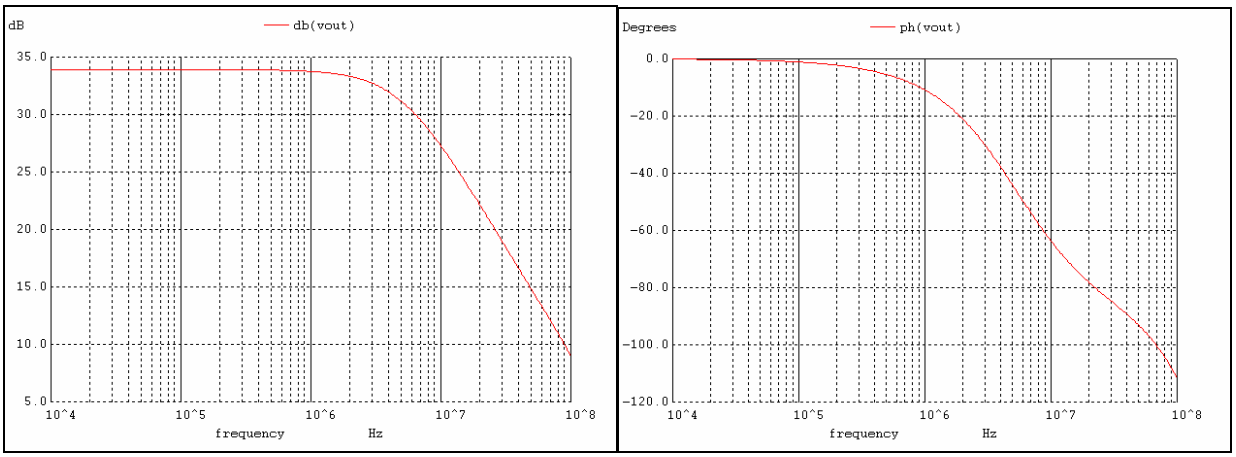


Figure 6 - frequency response with wider devices

Done By: Vaughn Johnson

24.2: Redesign the bias circuit for the op-amp in Fig.24.2 for minimum power. Compare the power dissipation of your new design to the design in Fig 24.2. Using your redesign generate the plots seen I Fig 24.3.

The two-stage op-amp in Fig 24.2 is using the biasing circuit from Fig 20.47. This biasing circuit has several outputs that are not needed for the two-stage op-amp. The op-amp only uses Vbias3 and Vbias4 for biasing the op-amp, this allows us to discard all the other biasing voltages from the circuit, which will decrease the power dissipated in the Op-amp. When the other biasing voltages are taken out we are left with the following circuit for biasing the Op-amp:

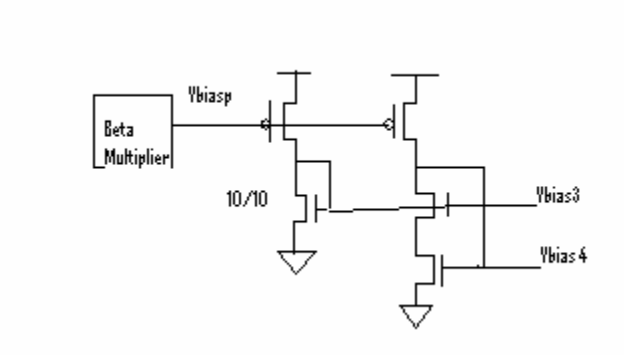
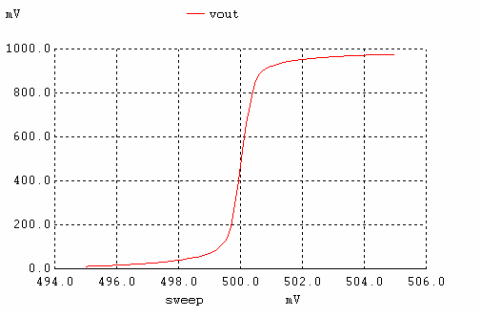


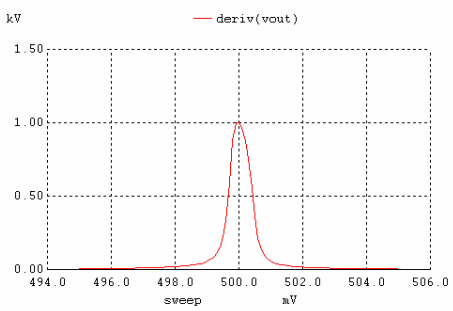
Fig1 Redesigned Biasing circuit.

With this new design we lose four branches that go from Vdd to ground, thus the current is reduced and since P=V*I the power is reduced also. Below is a table showing the differences between the new and old values:

Parameters	Original	New Design	Units
Vbias3	0.544	0.544	Volts
Vbias4	0.362	0.362	Volts
IDD	138.1	98.1	uAmps
VDD	1	1	Volts
Power	138.1	98.1	uWatts

We reduced the current by 29% thus the power was reduced by 29% of its original value. Below are the same plots as in Fig 24.3 but with the new designed bias circuit;





Netlist for simulations:

```
.control
destroy all
run

*print I(vmeas) vbias3 vbias4 vss  I(VDD) VDD*I(VDD)

plot vout
plot deriv(vout)
.endc

*.op
.option scale=50n ITL1=300
.dc vp 495m 505m .1m


VDD     VDD     0       DC      1
Vm      Vm      0       DC      0.5
Vp      Vp      0       DC      0.5
VMeas   vmeas   Vss     DC      0



M1      vd1     vm      vmeas   0       NMOS L=2 W=50
M2      vout1   vp      vmeas   0       NMOS L=2 W=50
M6B     Vdb1    Vbias4  0       0       NMOS L=2 W=100
M6T     vss     Vbias3  vdb1    0       NMOS L=2 W=100
M3      vd1     vd1     VDD     VDD     PMOS L=2 W=100
M4      vout1   vd1     VDD     VDD     PMOS L=2 W=100

M7      vout    Vout1   VDD     VDD     PMOS L=2 W=100
M8T     Vout    vbias3  vd8b    0       NMOS L=2 W=50
M8B     vd8b    vbias4  0       0       NMOS L=2 W=50


Xbias   VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias


.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1     Vbias3  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP2     Vbias4  Vbiasp  VDD     VDD     PMOS L=2 W=100


MN1     Vbias3  Vbias3  0       0       NMOS L=10 W=10
MN2     Vbias4  Vbias3  Vlow    0       NMOS L=2 W=50
MN3     Vlow    Vbias4  0       0       NMOS L=2 W=50


MBM1    Vbiasn  Vbiasn  0       0       NMOS L=2 W=50
MBM2    Vreg    Vreg    Vr      0       NMOS L=2 W=200
MBM3    Vbiasn  Vbiasp  VDD     VDD     PMOS L=2 W=100
MBM4    Vreg    Vbiasp  VDD     VDD     PMOS L=2 W=100
```

```
Rbias    Vr       0        5.5k

*amplifier
MA1      Vamp     Vreg     0        0       NMOS L=2 W=50
MA2      Vbiasp   Vbiasn   0        0       NMOS L=2 W=50
MA3      Vamp     Vamp     VDD      VDD     PMOS L=2 W=100
MA4      Vbiasp   Vamp     VDD      VDD     PMOS L=2 W=100

MCP      VDD      Vbiasp   VDD      VDD     PMOS L=100 W=100

*start-up stuff
MSU1     Vsur     Vbiasn   0        0       NMOS L=2   W=50
MSU2     Vsur     Vsur     VDD      VDD     PMOS L=20  W=10
MSU3     Vbiasp   Vsur     Vbiasn   0       NMOS L=1   W=10

.ends

* BSIM4 models
*
* 50nm models from "BPTM which is provided by the Device Group at UC Berkeley"
* Modified by RJB. These models are for educational purposes only! They are *not*
* extracted from actual silicon.
*
* Don't forget the .options scale=50nm if using an Lmin of 1
* 1<Ldrawn<200   10<Wdrawn<10000 Vdd=1V
* Change to level=54 when using HSPICE
```

By Vehid Suljic
Problem Solution for 24.3

Op-Amp in text fig. 24.2 was simulated with Vp=500 mV and sweeping Vm from 499 mV to 501 mV without MOSFETs width mismatches. Results of simulation are shown in figure 1, bellow. We can see that when Vp=Vm=500 mV, output is also at Vout=500 mV. So offset voltage is 0 volts (Vos=0V).

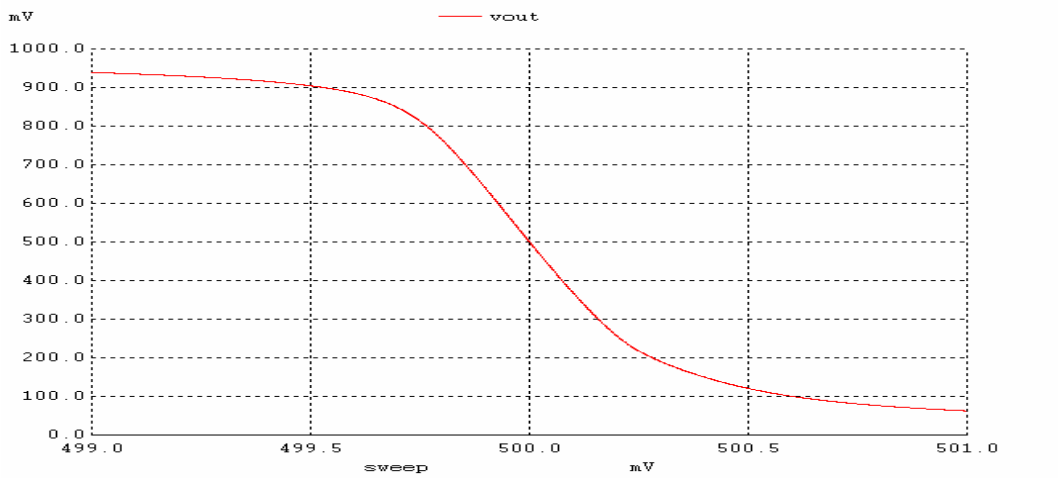


Figure 1. Simulation of Op-Amp in Fig. 24.2 without MOSFETs width mismatch

However, for only 0.2% mismatch in the widths of M1 and M2 (M1 is 50/2 and M2 is 49.9/2) we get results shown in figure 2. Now for Vp=Vm=500 mV we get output voltage of 650 mV(Vout=650 mV).

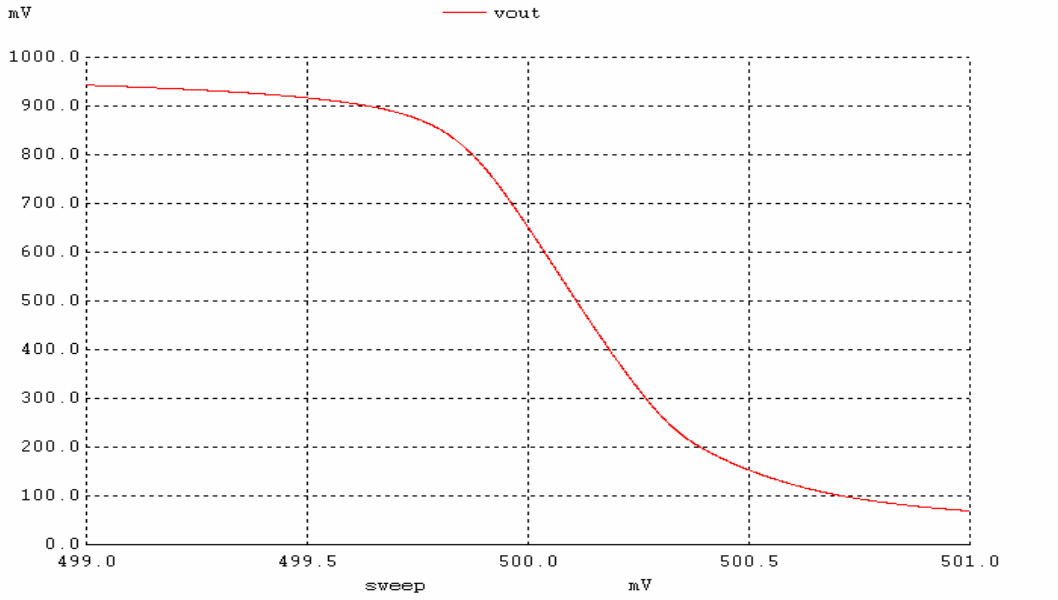


Figure 2. Simulation results for 0.2% mismatch in the widths of M1 and M2

Output offset voltage in Fig. 2 is 150 mV for only 0.2% mismatch and it can get very high for 1% mismatch in the M1 and M2 widths. This high offset is due to the gain of op-amp,

Aoldc = A1 A2= gmn(ron||rop) gmp rop ≈ 49.9 x 16.6 ≈ 828
Vos,out = Aoldc Vos

In order to find exacts offset between M1 (50/2) and M2 (49.5/2) I simulated op-amp in inverting gain of 1 configuration with R1=R2=10k. Simulation results are shown in Figure 3. From the figure bellow one can see that now for Vp=Vm=500mV offset voltage VosN=1.5 mV.

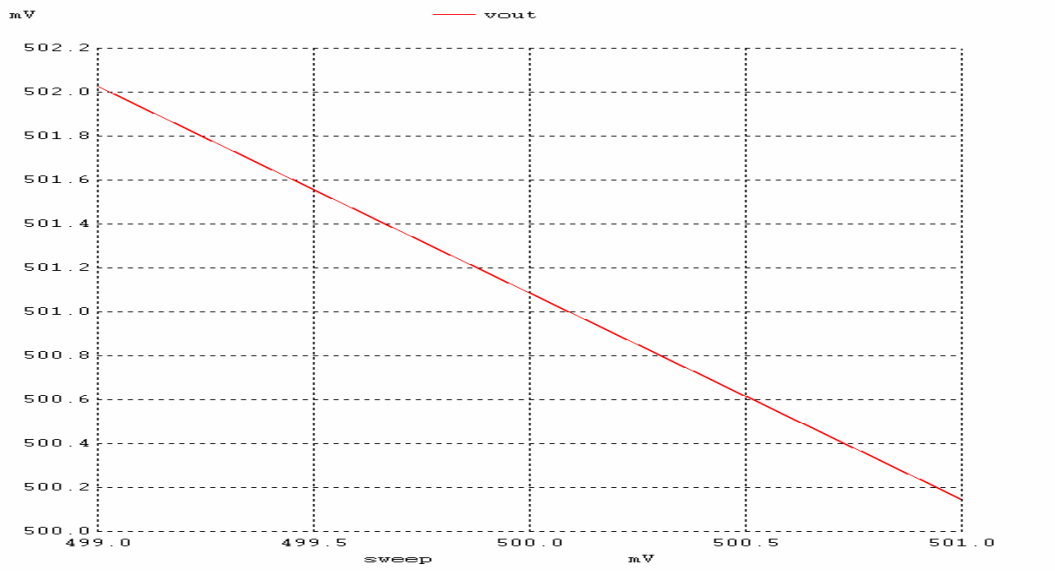


Figure 3. Simulation results for 1% mismatch in the widths of M1 and M2

Mismatch in the widths of M1-M2 and M3-M4 can be modeled as offset voltages VosN and VosP as shown in Fig. 4.

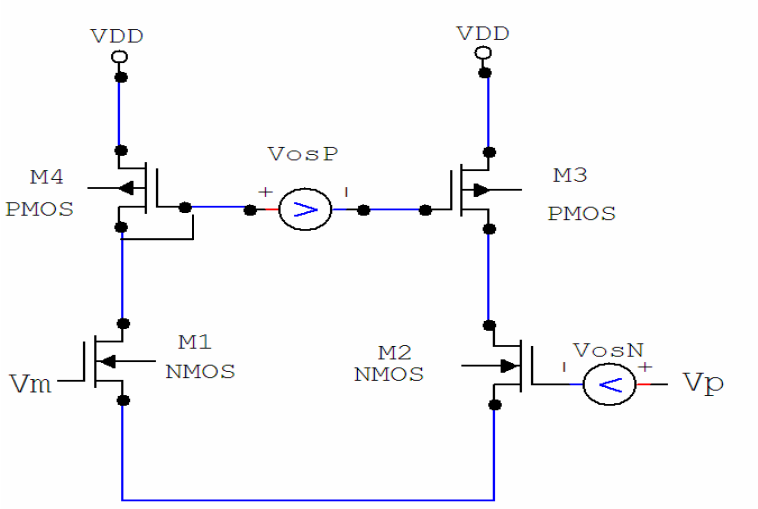


Figure 4. Model for mismatch in the widths of M1-M2 and M3-M4

From the model in fig. 4 we can relate mismatch in M3-M4 (VosP) to the M1-M2 mismatch (VosN).

id3 = gmp Vosp and id2 = gmn Vosn, since id3 = id2 we get

VosN= (gmp/gmn) VosP

Looking at this formula one can notice that if we increase gmn or decrease gmp we can reduce offset voltage due to mismatch in the widths of M3 and M4. However, we cannot reduce offset voltage due to the mismatch in the widths of M1 and M2. So mismatch in the widths of M1 and M2 is worse.

To illustrate this point I increased widths of M1 and M2 four times to 200/2. M3 and M4's widths are set to 1% mismatch (M3 is 100/2 and M4 is 99/2). Simulation results for inverting gain of 1 are shown in figure 5.

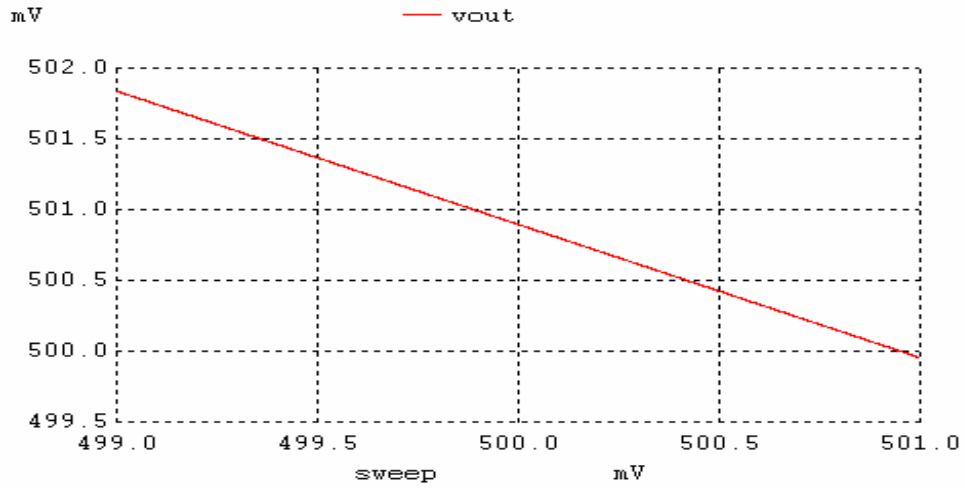


Figure 5. Simulation of offset voltage due to mismatch in the widths of M3 and M4

Now, we can see that offset voltage for Vp=Vm=500mV is only Vos=0.8 mV which is almost twice less than offset voltage due to the widths mismatch of M1 and M2 (Vos=1.5mV as shown in fig. 3).

By increasing widths of M1 and M2 we increased gmn which reduced offset voltage due to the mismatch in the widths of M3 and M4.

```
*** Problem 24.3 WinSpice Netlist***
.control
destroy all
run
plot vout
.endc

.option scale=50n ITL1=300
.dc vm 499m 501m .001m

VDD   VDD   0       DC     1
Vm    Vm    0       DC     0
Vp    Vp    0       DC     0.5

M1    vd1   vm      vss    0      NMOS L=2 W=50
M2    vout1 vp      vss    0      NMOS L=2 W=50
M6B   Vdb1  Vbias4  0      0      NMOS L=2 W=100
M6T   vss   Vbias3  vdb1   0      NMOS L=2 W=100
M3    vd1   vd1     VDD    VDD    PMOS L=2 W=100
M4    vout1 vd1     VDD    VDD    PMOS L=2 W=99

M7    vout  Vout1   VDD    VDD    PMOS L=2 W=100
M8T   Vout  vbias3  vd8b   0      NMOS L=2 W=50
M8B   vd8b  vbias4  0      0      NMOS L=2 W=50
*R2   vout  vm      10k
*R1   vm1   vm      10k



Xbias  VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias


.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1   Vbias3 Vbiasp VDD   VDD   PMOS L=2 W=100
MP2   Vbias4 Vbiasp       VDD   VDD   PMOS L=2 W=100
MP3   vp1    vp2    VDD   VDD   PMOS L=2 W=100
MP4   vp2    Vbias2 vp1   VDD   PMOS L=2 W=100
MP5   Vpcas  Vpcas  vp2   VDD   PMOS L=2 W=100
MP6   Vbias2 Vbias2 VDD   VDD   PMOS L=10 W=20
MP7   Vhigh  Vbias1 VDD   VDD   PMOS L=2 W=100
MP8   Vbias1 Vbias2 Vhigh VDD   PMOS L=2 W=100
```

```
MP9    vp3     Vbias1 VDD   VDD   PMOS L=2 W=100
MP10   Vncas   Vbias2 vp3    VDD   PMOS L=2 W=100

MN1    Vbias3 Vbias3 0      0     NMOS L=10 W=10
MN2    Vbias4 Vbias3 Vlow   0     NMOS L=2 W=50
MN3    Vlow   Vbias4 0      0     NMOS L=2 W=50
MN4    Vpcas  Vbias3 vn1    0     NMOS L=2 W=50
MN5    vn1    Vbias4 0      0     NMOS L=2 W=50
MN6    Vbias2 Vbias3 vn2    0     NMOS L=2 W=50
MN7    vn2    Vbias4 0      0     NMOS L=2 W=50
MN8    Vbias1 Vbias3 vn3    0     NMOS L=2 W=50
MN9    vn3    Vbias4 0      0     NMOS L=2 W=50
MN10   Vncas  Vncas  vn4    0     NMOS L=2 W=50
MN11   vn4    Vbias3 vn5    0     NMOS L=2 W=50
MN12   vn5    vn4    0      0     NMOS L=2 W=50

MBM1 Vbiasn Vbiasn 0      0     NMOS L=2 W=50
MBM2 Vreg   Vreg   Vr     0     NMOS L=2 W=200
MBM3 Vbiasn Vbiasp VDD    VDD   PMOS L=2 W=100
MBM4 Vreg   Vbiasp VDD    VDD   PMOS L=2 W=100

Rbias  Vr     0      5.5k

*amplifier
MA1    Vamp   Vreg   0      0     NMOS L=2 W=50
MA2    Vbiasp Vbiasn 0      0     NMOS L=2 W=50
MA3    Vamp   Vamp   VDD    VDD   PMOS L=2 W=100
MA4    Vbiasp Vamp   VDD    VDD   PMOS L=2 W=100

MCP    VDD    Vbiasp VDD    VDD   PMOS L=100 W=100

*start-up stuff
MSU1  Vsur    Vbiasn 0      0     NMOS L=2   W=50
MSU2  Vsur    Vsur   VDD    VDD   PMOS L=20  W=10
MSU3  Vbiasp  Vsur   Vbiasn 0     NMOS L=1   W=10

.ends
```

Jared Fife

Problem 24.4

This problem asks to simulate the use of the "zero-nulling" circuit in Fig. 24.15 in the op-amp of Fig. 24.8. The AC, operating-point, and transient (step) operation of the resulting op-amp are to be shown. We're also asked to verify that the gate of MP1 is at the same potential as the gate of M7 in quiescent conditions.

A drawing of the circuit is shown in here in Figure 1.

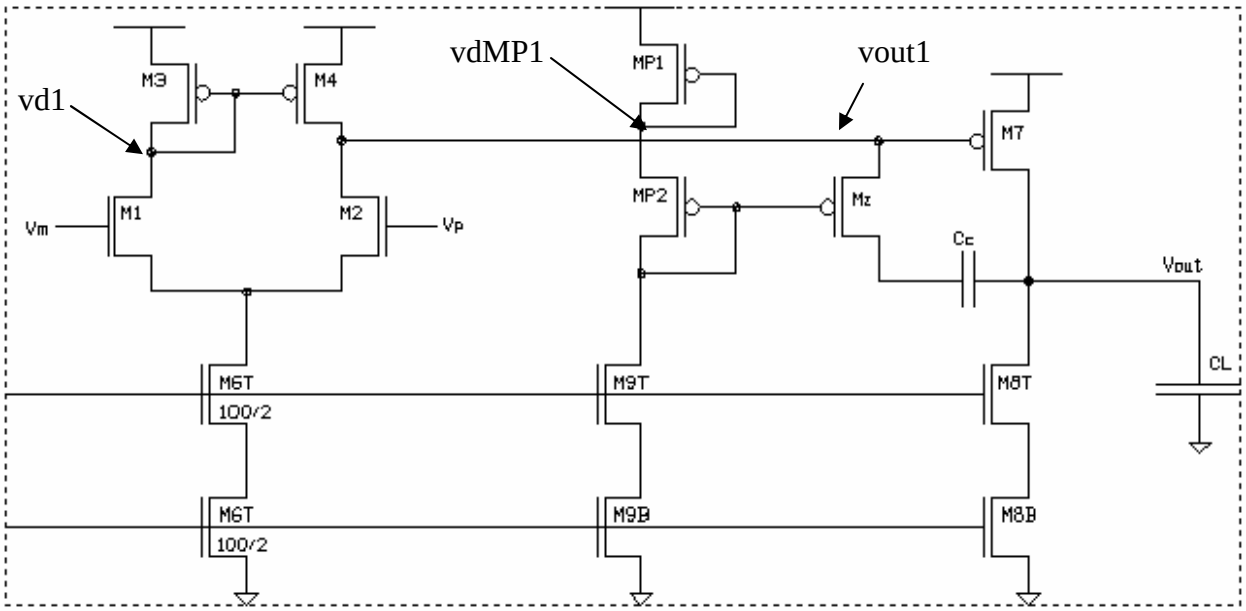


Figure 1. Op-amp circuit for problem 24.4

We'll use 100fF for C_L as was used in Fig. 24.8 in the text. For C_C, we'll use a higher value than the 100fF that was used originally in Fig. 24.8 in the text. Let's set our unity gain frequency to 10MHz as was done in eq. 24.10:

$$f_{un} = \frac{g_{m1}}{2\pi \cdot C_C} = \frac{150\mu A/V}{2\pi \cdot C_C} = 10MHz \rightarrow C_C = 2.4\,pF$$

Quiescent conditions

The gate and drain voltages of M4 and MP1 is mirrored over from M3. Also, this same voltage is mirrored to the gate of M7. To verify this in SPICE, we can perform an operating point (.op) analysis. The following voltages were recorded from SPICE:

vout1 = 6.488707e-01
vdMP1 = 6.473535e-01
vd1 = 6.500546e-01

This verifies that the circuit is biased correctly and the node voltages are mirrored over as we expected. We can also see from this analysis that we have a built in offset in the diff amp of ~2mV from the voltage difference of nodes vd1 to vout1.

AC Response

To show the AC operation of the circuit, we'll use the same configuration shown in Fig. 24.9 of the text.

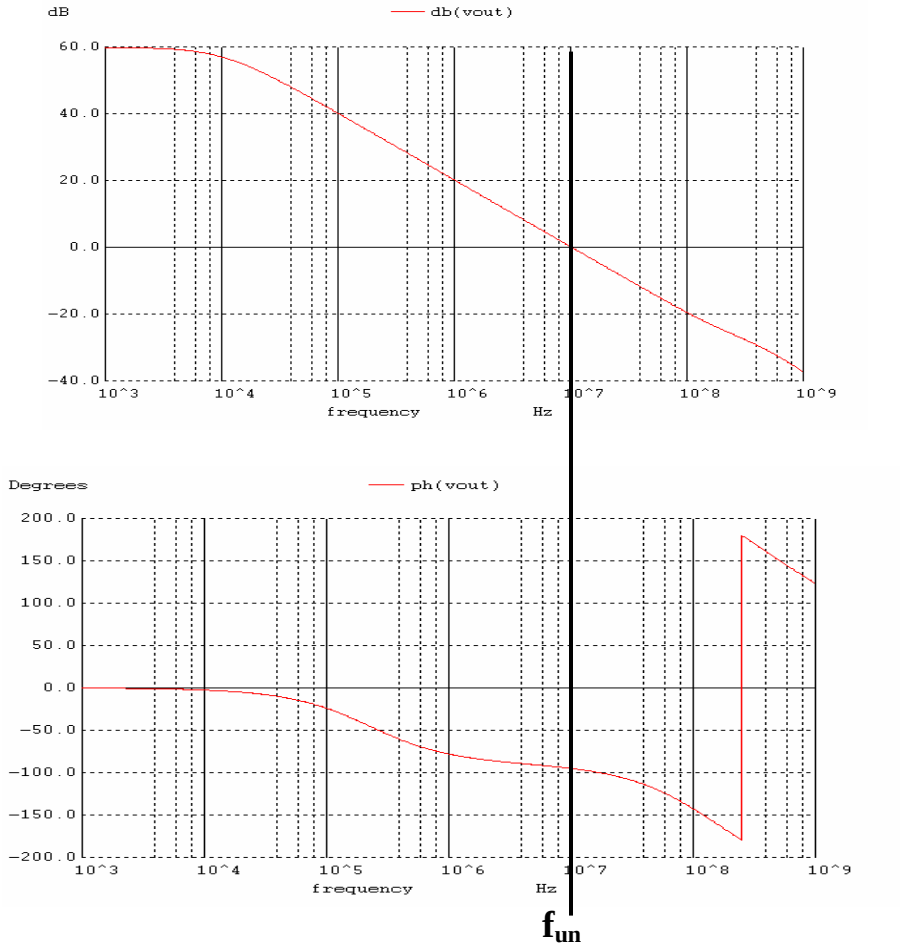


Figure 2. Open-loop frequency response of the op-amp shown in Figure 1 above.

As shown in Fig. 2, the phase margin is almost 90 degrees, so stability isn't an issue as it would be with a lower compensation capacitance. The phase margin drops to ~15 degrees if we use 100fF for C_C.

Transient Analysis

For the transient or step response of the circuit we can use the configuration shown in Fig 24.12 or 24.14 in the text. The response is well behaved and similar to Fig 24.14 in the text where C_C was also set to 2.4pF.

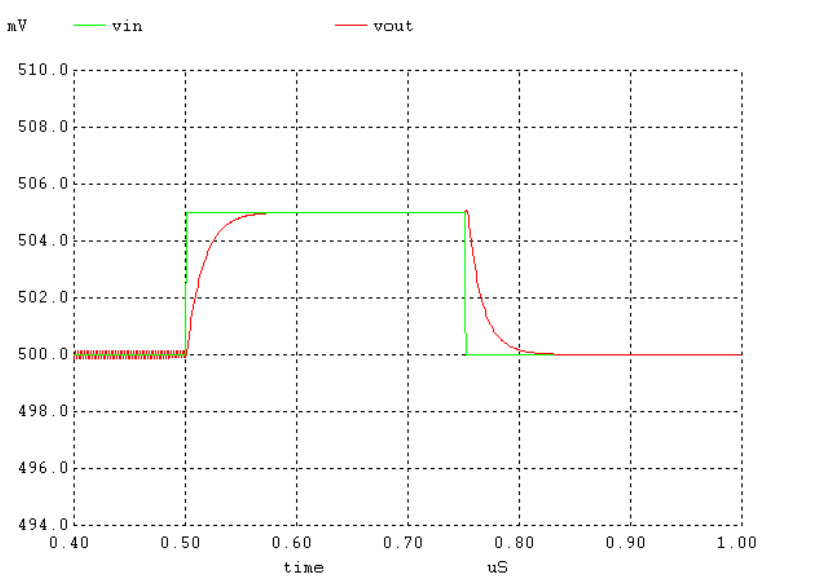


Figure 3. Transient Response of the op-amp shown in Figure 1 above.

Netlist for AC Response

*** Problem 24.4 CMOS: Circuit Design, Layout, and Simulation ***

```
.control
destroy all
run
set units=degrees
plot ph(vout)
plot db(vout)
.endc

.option scale=50n ITL1=300
.ac dec 100 1k 1G

VDD     VDD     0       DC      1
Vp      Vp      0       DC      0.5     AC      1

Rbig    Vout    Vm      100MEG
Cbig    Vm      0       10u

Cc      Vout    cc      2.4p
Cl      Vout    0       100f

M1      vd1     vm      vss     0       NMOS L=2 W=50
M2      vout1   vp      vss     0       NMOS L=2 W=50
M6B     Vdb1    Vbias4  0       0       NMOS L=2 W=100
M6T     vss     Vbias3  vdb1    0       NMOS L=2 W=100
M3      vd1     vd1     VDD     VDD     PMOS L=2 W=100
M4      vout1   vd1     VDD     VDD     PMOS L=2 W=100

MP1     vdMP1   vdMP1   VDD     VDD     PMOS L=2 W=100
MP2     vdMP2   vdMP2   vdMP1   VDD     PMOS L=2 W=100
```

```
Mz      cc      vdMP2   vout1   VDD     PMOS L=2 W=100
M9T     vdMP2   vbias3  vd9b    0       NMOS L=2 W=50
M9B     vd9b    vbias4  0       0       NMOS L=2 W=50


M7      vout    Vout1   VDD     VDD     PMOS L=2 W=100
M8T     Vout    vbias3  vd8b    0       NMOS L=2 W=50
M8B     vd8b    vbias4  0       0       NMOS L=2 W=50


Xbias   VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias


.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1     Vbias3  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP2     Vbias4  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP3     vp1     vp2     VDD     VDD     PMOS L=2 W=100
MP4     vp2     Vbias2  vp1     VDD     PMOS L=2 W=100
MP5     Vpcas   Vpcas   vp2     VDD     PMOS L=2 W=100
MP6     Vbias2  Vbias2  VDD     VDD     PMOS L=10 W=20
MP7     Vhigh   Vbias1  VDD     VDD     PMOS L=2 W=100
MP8     Vbias1  Vbias2  Vhigh   VDD     PMOS L=2 W=100
MP9     vp3     Vbias1  VDD     VDD     PMOS L=2 W=100
MP10    Vncas   Vbias2  vp3     VDD     PMOS L=2 W=100

MN1     Vbias3  Vbias3  0       0       NMOS L=10 W=10
MN2     Vbias4  Vbias3  Vlow    0       NMOS L=2 W=50
MN3     Vlow    Vbias4  0       0       NMOS L=2 W=50
MN4     Vpcas   Vbias3  vn1     0       NMOS L=2 W=50
MN5     vn1     Vbias4  0       0       NMOS L=2 W=50
MN6     Vbias2  Vbias3  vn2     0       NMOS L=2 W=50
MN7     vn2     Vbias4  0       0       NMOS L=2 W=50
MN8     Vbias1  Vbias3  vn3     0       NMOS L=2 W=50
MN9     vn3     Vbias4  0       0       NMOS L=2 W=50
MN10    Vncas   Vncas   vn4     0       NMOS L=2 W=50
MN11    vn4     Vbias3  vn5     0       NMOS L=2 W=50
MN12    vn5     vn4     0       0       NMOS L=2 W=50

MBM1    Vbiasn  Vbiasn  0       0       NMOS L=2 W=50
MBM2    Vreg    Vreg    Vr      0       NMOS L=2 W=200
MBM3    Vbiasn  Vbiasp  VDD     VDD     PMOS L=2 W=100
MBM4    Vreg    Vbiasp  VDD     VDD     PMOS L=2 W=100

Rbias   Vr      0       5.5k

*amplifier
MA1     Vamp    Vreg    0       0       NMOS L=2 W=50
MA2     Vbiasp  Vbiasn  0       0       NMOS L=2 W=50
MA3     Vamp    Vamp    VDD     VDD     PMOS L=2 W=100
MA4     Vbiasp  Vamp    VDD     VDD     PMOS L=2 W=100

MCP     VDD     Vbiasp  VDD     VDD     PMOS L=100 W=100

*start-up stuff
MSU1    Vsur    Vbiasn  0       0       NMOS L=2   W=50
MSU2    Vsur    Vsur    VDD     VDD     PMOS L=20  W=10
MSU3    Vbiasp  Vsur    Vbiasn  0       NMOS L=1   W=10

.ends
```

Netlist for Transient Response

The following lines are changed from the above netlist:

```
.control
```

```
destroy all
run
set units=degrees
plot vout vin xlimit 400n 1u ylimit 480m 520m
.endc

.option scale=50n ITL1=300
.tran 1n 1u UIC

VDD     VDD     0       DC      1
Vin     Vin     0       DC      0       PULSE 500m  505m 500n 0 0 250n 500n

M1      vd1     vout    vss     0       NMOS L=2 W=50
M2      vout1   vin     vss     0       NMOS L=2 W=50
```

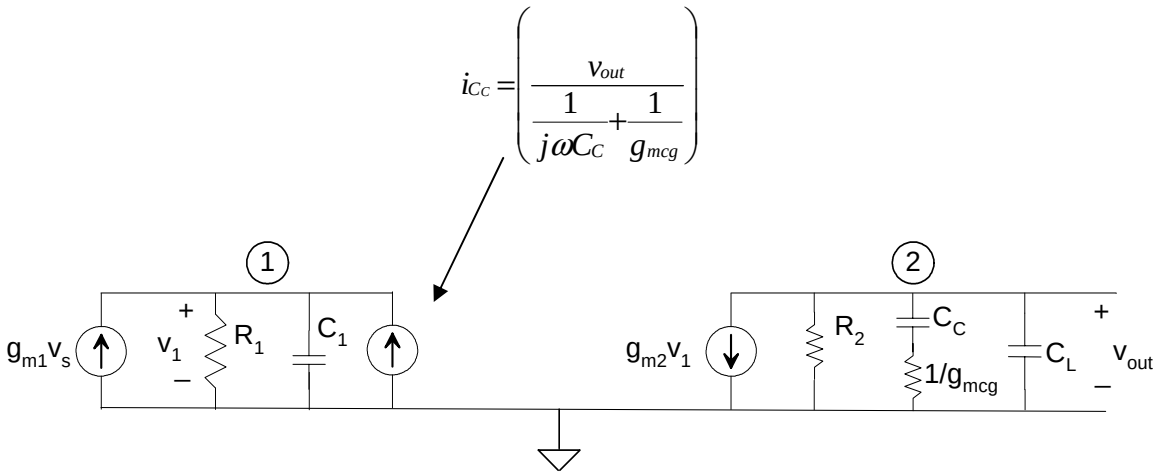
Netlist for Operating Point

For the .op analysis we comment out the .ac line in the netlist above and add the following:

```
.op
print vd1 vout1 vdMP1
```

Problem 24.5
(Mayuri Vasireddi)

The following is the model to determine the frequency response of circuit seen in Fig. 24.17



At node 1 using KCL we have

$$g_{m1} * v_s + \frac{v_{out}}{\left(\frac{1}{jwC_c} + \frac{1}{g_{mcg}}\right)} = \frac{v_1}{\left(\frac{R_1}{1 + jwC_1R_1}\right)}$$

$$\Rightarrow v_1 = \left(g_{m1} * v_s + \frac{v_{out}}{\left(\frac{1}{jwC_c} + \frac{1}{g_{mcg}}\right)} \right) * \left(\frac{R_1}{1 + jwC_1R_1}\right)$$

re - arranging the equation and substituting $jw = s$

$$\Rightarrow v_1 = \left(v_s + \frac{v_{out} * \left(\frac{sC_c}{g_{m1}}\right)}{\left(1 + \frac{sC_c}{g_{mcg}}\right)} \right) * \left(\frac{g_{m1} * R_1}{1 + sC_1R_1}\right) \qquad \text{----------(1)}$$

At node 2 the equivalent output impedence is (lets say 'α'

$$\alpha = R_2 // \left(\frac{1}{sC_C} + \frac{1}{g_{mcg}} \right) // \left(\frac{1}{\mathrm{sC_L}} \right)$$

$$\Rightarrow \alpha = \frac{\left(R_2 * \left(\frac{1}{sC_C} + \frac{1}{g_{mcg}} \right) \right)}{R_2 + \left(\frac{1}{sC_C} + \frac{1}{g_{mcg}} \right)} // \left(\frac{1}{\mathrm{sC_L}} \right)$$

$$\Rightarrow \alpha = \frac{R_2 * \left[g_{mcg} + sC_C \right]}{sC_C R_2 g_{mcg} + sC_C + g_{mcg}} // \left(\frac{1}{\mathrm{sC_L}} \right)$$

$$\Rightarrow \alpha = \frac{R_2 g_{mcg} \left[1 + \frac{sC_C}{g_{mcg}} \right]}{g_{mcg} \left[1 + \frac{sC_C}{g_{mcg}} \right] + sR_2 g_{mcg} \left(C_C + C_L \right) + s^2 R_2 C_C C_L} \quad \text{--------- (2)}$$

For output node 2,

$V_{out} = -g_{m2} * V_1 * \alpha$

substituting V_1 from (1) in the above equation, we get

$$v_{out} = -g_{m2} * \alpha * \left(v_s + \frac{v_{out} * \left(\frac{sC_C}{g_{m1}} \right)}{\left(1 + \frac{sC_C}{g_{mcg}} \right)} \right) * \left(\frac{g_{m1} * R_1}{1 + sC_1 R_1} \right)$$

$$\Rightarrow v_{out} \left(1 + \frac{sg_{m2} R_1 C_C \alpha}{\left(1 + sC_1 R_1 \right) * \left(1 + \frac{sC_C}{g_{mcg}} \right)} \right) = \left(\frac{-g_{m1} g_{m2} R_1 \alpha}{1 + sC_1 R_1} \right) v_s$$

$$\Rightarrow \frac{v_{out}}{v_s} = \frac{-g_{m1} g_{m2} R_1 \alpha \left(1 + \frac{sC_C}{g_{mcg}} \right)}{\left(1 + sC_1 R_1 \right) * \left(1 + \frac{sC_C}{g_{mcg}} \right) + sg_{m2} R_1 \alpha C_C}$$

Substituting the value of α in the above equation we get,

$$\frac{v_{out}}{v_s}=\frac{-g_{m1}g_{m2}R_1\left(1+\frac{sC_C}{g_{mcg}}\right)*\left(\frac{R_2g_{mcg}\left[1+\frac{sC_C}{g_{mcg}}\right]}{g_{mcg}\left[1+\frac{sC_C}{g_{mcg}}\right]+sR_2g_{mcg}\left(C_C+C_L\right)+s^2R_2C_CC_L}\right)}{\left(1+sC_1R_1\right)*\left(1+\frac{sC_C}{g_{mcg}}\right)+\left(sg_{m2}R_1C_C*\left(\frac{R_2g_{mcg}\left[1+\frac{sC_C}{g_{mcg}}\right]}{g_{mcg}\left[1+\frac{sC_C}{g_{mcg}}\right]+sR_2g_{mcg}\left(C_C+C_L\right)+s^2R_2C_CC_L}\right)\right)}$$

$$\Rightarrow\frac{v_{out}}{v_s}=\frac{-g_{m1}g_{m2}R_1\left(1+\frac{sC_C}{g_{mcg}}\right)*\left(\frac{R_2g_{mcg}}{g_{mcg}\left[1+\frac{sC_C}{g_{mcg}}\right]+sR_2g_{mcg}\left(C_C+C_L\right)+s^2R_2C_CC_L}\right)}{\left(1+sC_1R_1\right)+\left(sg_{m2}R_1C_C*\left(\frac{R_2g_{mcg}}{g_{mcg}\left[1+\frac{sC_C}{g_{mcg}}\right]+sR_2g_{mcg}\left(C_C+C_L\right)+s^2R_2C_CC_L}\right)\right)}$$

$$\Rightarrow\frac{v_{out}}{v_s}=\frac{-g_{m1}g_{m2}g_{mcg}R_1R_2\left(1+\frac{sC_C}{g_{mcg}}\right)}{\left(1+sC_1R_1\right)*\left(g_{mcg}\left[1+\frac{sC_C}{g_{mcg}}\right]+sR_2g_{mcg}\left(C_C+C_L\right)+s^2R_2C_CC_L\right)+\left(sg_{m2}g_{mcg}R_1R_2C_C\right)}$$

$$\Rightarrow\frac{v_{out}}{v_s}=\frac{-g_{m1}g_{m2}R_1R_2\left(1+\frac{sC_C}{g_{mcg}}\right)}{\left(1+sC_1R_1\right)*\left(\left[1+\frac{sC_C}{g_{mcg}}\right]+sR_2\left(C_C+C_L\right)+\frac{s^2R_2C_CC_L}{g_{mcg}}\right)+\left(sg_{m2}R_1R_2C_C\right)}$$

$$\Rightarrow\frac{v_{out}}{v_s}=\frac{-g_{m1}g_{m2}R_1R_2\left(1+\frac{sC_C}{g_{mcg}}\right)}{1+s\left(R_1C_1+\frac{C_C}{g_{mcg}}+R_2\left(C_C+C_L\right)+g_{m2}R_1R_2C_C\right)+s^2\left(\frac{R_1C_CC_1}{g_{mcg}}+R_1R_2C_1\left(C_C+C_L\right)+\frac{R_2C_CC_L}{g_{mcg}}\right)+s^3\left(\frac{R_1R_2C_CC_1C_L}{g_{mcg}}\right)}$$

Looking at the above equation we find a LHP zero at

$$f_z = \frac{g_{mcg}}{2\pi C_C}$$

To find the output pole, we look at the denominator of the above equation,

$$1+s\left(R_1C_1+\frac{C_C}{g_{mcg}}+R_2\left(C_C+C_L\right)+g_{m2}R_1R_2C_C\right)+s^2\left(\frac{R_1C_CC_1}{g_{mcg}}+R_1R_2C_1\left(C_C+C_L\right)+\frac{R_2C_CC_L}{g_{mcg}}\right)$$

$$+s^3\left(\frac{R_1R_2C_CC_1C_L}{g_{mcg}}\right)$$

Now,

$$\text{let K}=1+s\left(R_1C_1+\frac{C_C}{g_{mcg}}+R_2\left(C_C+C_L\right)+g_{m2}R_1R_2C_C\right)+s^2\left(\frac{R_1C_CC_1}{g_{mcg}}+R_1R_2C_1\left(C_C+C_L\right)+\frac{R_2C_CC_L}{g_{mcg}}\right)$$

The denominator then becomes

$$\text{K}+s^3\left(\frac{R_1R_2C_CC_1C_L}{g_{mcg}}\right)$$

Factorizing it, we get

$$\text{K}*\left(1+\frac{s\left(\frac{R_1R_2C_CC_1C_L}{g_{mcg}}\right)}{K/s^2}\right) \text{ in the form } \left(1+j\frac{f}{f_1}\right)*\left(1+j\frac{f}{f_2}\right)$$

$$\left(1+j\frac{f}{f_2}\right)=\left(1+\frac{s\left(\frac{R_1R_2C_CC_1C_L}{g_{mcg}}\right)}{\frac{K}{s^2}}\right)$$

$$=\left(1+\frac{s\left(\frac{R_1R_2C_CC_1C_L}{g_{mcg}}\right)}{\frac{1}{s^2}+\frac{1}{s}\left(R_1C_1+\frac{C_C}{g_{mcg}}+R_2\left(C_C+C_L\right)+g_{m2}R_1R_2C_C\right)+\left(\frac{R_1C_CC_1}{g_{mcg}}+R_1R_2C_1\left(C_C+C_L\right)+\frac{R_2C_CC_L}{g_{mcg}}\right)}\right)$$

At high frequencies, we can approximate to

$$\left(1+ j\frac{f}{f_2}\right)=\left(1+\frac{s\left(\frac{R_1R_2C_CC_1C_L}{g_{mcg}}\right)}{\left(\frac{R_1C_CC_1}{g_{mcg}}+R_1R_2C_1(C_C+C_L)+\frac{R_2C_CC_L}{g_{mcg}}\right)}\right)$$

$$\Rightarrow\left(1+ j\frac{f}{f_2}\right)=\left(1+ j\frac{2\pi f\left(\frac{R_1R_2C_CC_1C_L}{g_{mcg}}\right)}{\left(\frac{R_1C_CC_1}{g_{mcg}}+R_1R_2C_1(C_C+C_L)+\frac{R_2C_CC_L}{g_{mcg}}\right)}\right)$$

Thus

$$f_2=\frac{\left(\frac{R_1C_CC_1}{g_{mcg}}+R_1R_2C_1(C_C+C_L)+\frac{R_2C_CC_L}{g_{mcg}}\right)}{2\pi\left(\frac{R_1R_2C_CC_1C_L}{g_{mcg}}\right)}$$

Assuming $R_1R_2C_1(C_C+C_L)>>\frac{R_1C_CC_1}{g_{mcg}}$ *and* $\frac{R_2C_CC_L}{g_{mcg}}$, we get

$$f_2\approx\frac{R_1R_2C_1(C_C+C_L)}{2\pi\left(\frac{R_1R_2C_CC_1C_L}{g_{mcg}}\right)}$$

$$\Rightarrow f_2\approx\frac{g_{mcg}(C_C+C_L)}{2\pi C_CC_L}$$

Using this formula we calculate for $C_C=240\,fF$ and $C_L=100\,fF$, the output pole to be

$$f_2=\frac{150\mu*(240\,fF+100\,fF)}{2\pi*240\,fF*100\,fF}=338.2MHz$$

This matches the value from SPICE simulation (simulation results attached)

To check if the above derived equation is correct, let us find out the f_2 for different values :

1.$C_C=520\,fF$ and $C_L=100\,fF$

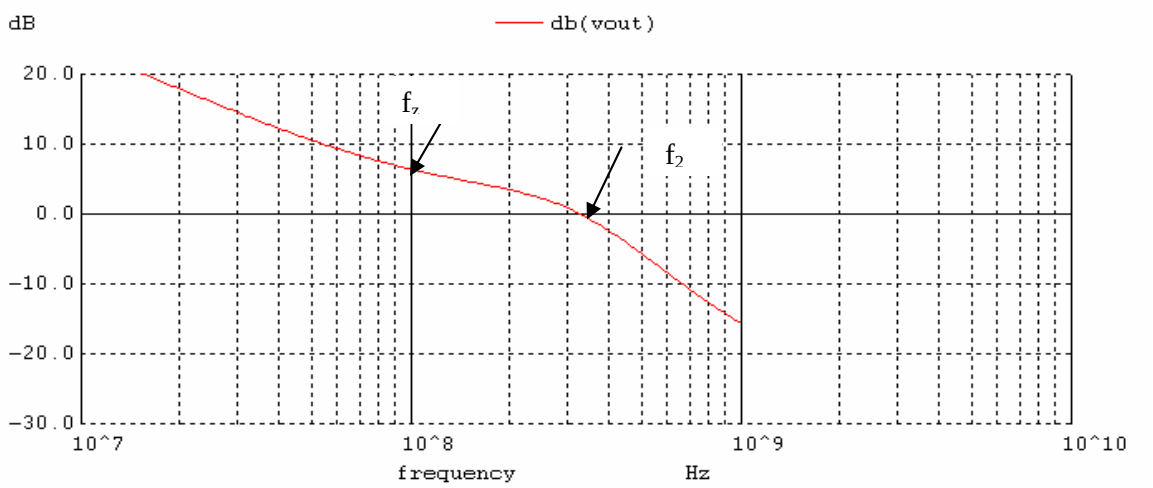
$$f_2=\frac{150\mu*(520\,fF+100\,fF)}{2\pi*520\,fF*100\,fF}=284.64MHz\qquad;\ f_z=\frac{150\mu}{2\pi*520\,fF}=45.9MHz$$

2.$C_C=2400\,fF$ and $C_L=100\,fF$

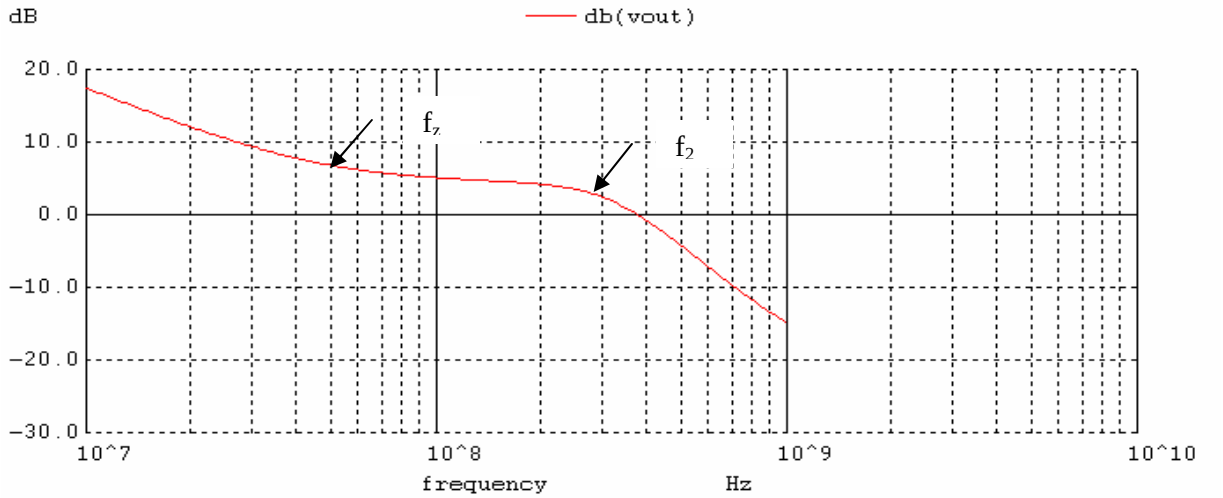
$$f_2=\frac{150\mu*(2400\,fF+100\,fF)}{2\pi*2400\,fF*100\,fF}=248.67MHz\qquad;\ f_z=\frac{150\mu}{2\pi*2400\,fF}=9.95MHz$$

SPICE simulations attached show that the above calculated values are correct

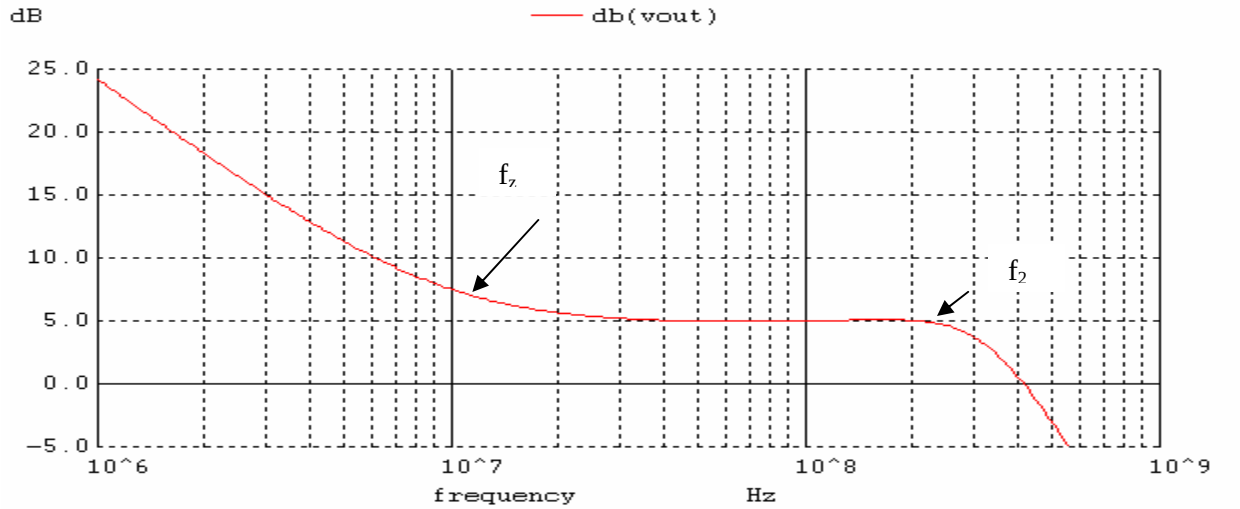
For C_C=240fF, C_L=100fF, f_2 is around 320MHz, f_z is around 100MHz



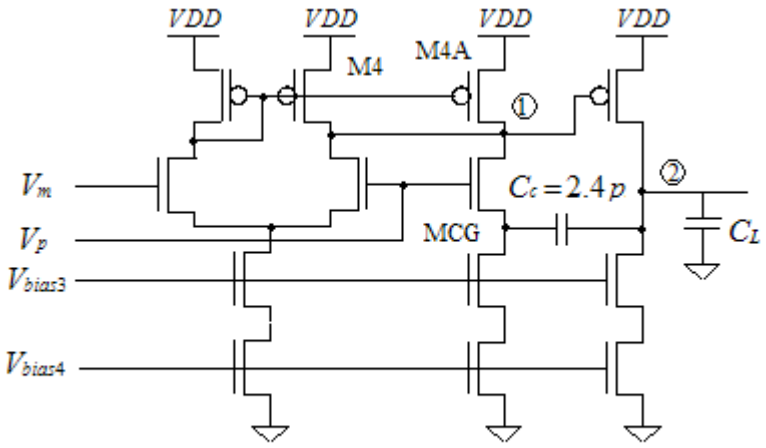
For C_C=520fF, C_L=100fF, f_2 is around 290MHz, f_z is around 50MHz



For C_C=2.4pF, C_L=100fF, f_2 is around 250MHz, f_z is around 10MHz



Problem 24.6
Bhavana Kollimarla



Hand Calculations

$C_c = 2.4pF$

$C_L = 100fF$

$C_1 = C_{gs7} + C_{dg,4A} + C_{dg,MCG} + C_{dg,4} + C_{gd,2} = 18.86fF$

$R_1 = r_{on} // r_{op} = 111.2K\Omega$

$R_2 = r_{op} // R_{ocasn} = r_{op} = 333K\Omega$

$g_{m1} = g_{mn} = 150\mu A/V$

$g_{m2} = g_{mp} = 150\mu A/V$

Location of first pole $f_1 = \dfrac{1}{2\pi \cdot g_{m2} \cdot R_1 \cdot R_2 \cdot C_c} = \dfrac{1}{2\pi \cdot 150\mu \cdot 111.2K \cdot 333K \cdot 2.4\text{p}} = 12KHz$

Location of second pole $f_2 = \dfrac{g_{m2} \cdot C_c}{2\pi \cdot C_1 \cdot C_2} \approx \dfrac{g_{m2} \cdot C_c}{2\pi \cdot C_1 \cdot (C_L + C_c)} = \dfrac{150\mu \cdot 2.4\text{p}}{2\pi \cdot 18.86\text{f} \cdot (2.4\text{p} + 100\text{f})} \approx 1.2GHz$

Unity Gain Frequency $f_{un} = \dfrac{g_{m1}}{2\pi \cdot C_c} = \dfrac{150\mu}{2\pi \cdot 2.4\text{p}} = 10MHz$

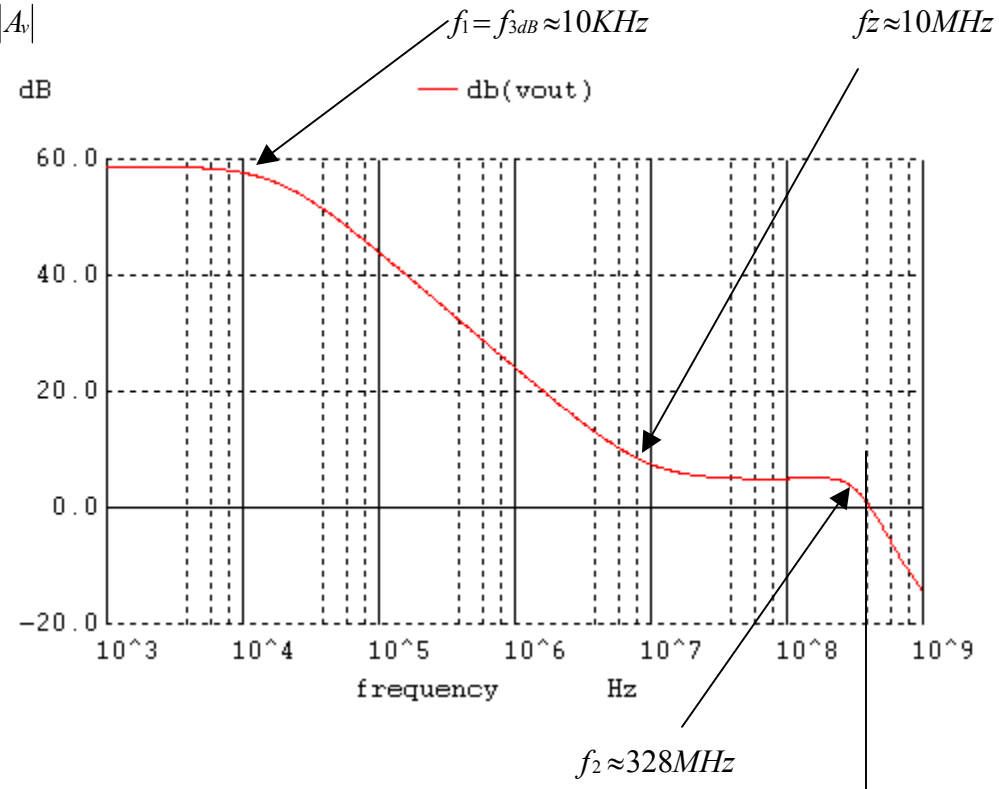
$f_z = \dfrac{g_{m1}}{2\pi \cdot C_c} = \dfrac{150\mu}{2\pi \cdot 2.4\text{p}} = 10MHz$

$A_{OL} = g_{m1} \cdot g_{m2} \cdot R_1 \cdot R_2 = 150\mu \cdot 150\mu \cdot 111.2\text{K} \cdot 333\text{K} = 831.6\text{V/V} \approx 58.3dB$

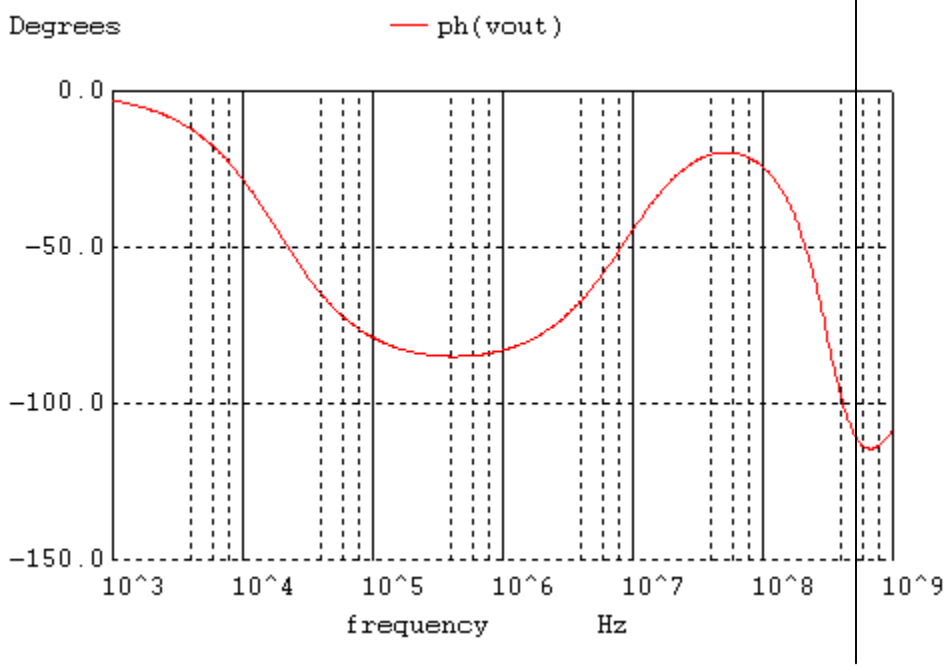
$f_{un} = A_{OL} \cdot f_{3dB} = 831.6 \cdot 12KHz = 9.9MHz$

The Simulation Results are shown below:

$|A_v|$



$\angle A_{OL}(f)$



$f_{un} \approx 410MHz$

$PM = 81^{\circ}$

	Hand Calculations	Simulations
f_1	12KHz	10KHz
f_2	1.2GHz	0.3GHz
A_{OL}	58.3dB	58.8dB
f_z	10MHz	10MHz
f_{un}	10MHz	410MHz

The hand calculations and simulation results for f_1, f_2, A_{OL}, f_z are close but the values for the unity gain frequency don't match because of the LHP zero in between the two poles which adds to the phase response and increases the speed (f_t).

Netlist

```
.control
destroy all
run
set units=degrees
plot ph(vout)
plot db(vout)
.endc
.option scale=50n ITL1=300 rshunt=1e9
.ac dec 100 1k 1G

VDD   VDD    0       DC     1
Vp    Vp     0       DC     0.5    AC     1
Rbig  Vout   Vm      10MEG
Cbig  Vm     0       10u
Cc    Vout   Vd10    2.4p
Cl    Vout   0       100f

M1    vd1    vm      vss    0      NMOS L=2 W=50
M2    vout1  vp      vss    0      NMOS L=2 W=50
M6B   Vdb1   Vbias4  0      0      NMOS L=2 W=100
M6T   vss    Vbias3  vdb1   0      NMOS L=2 W=100
M3    vd1    vd1     VDD    VDD    PMOS L=2 W=100
M4    vout1  vd1     VDD    VDD    PMOS L=2 W=100
M4a   vout1  vd1     VDD    VDD    PMOS L=2 W=100
M7    vout   Vout1   VDD    VDD    PMOS L=2 W=100
M8T   Vout   vbias3  vd8b   0      NMOS L=2 W=50
M8B   vd8b   vbias4  0      0      NMOS L=2 W=50
MCG   vout1  vp      vd10   0      NMOS L=2 W=50
M10B  vd10   vbias3  vd9    0      NMOS L=2 W=50
M9    vd9    vbias4  0      0      NMOS L=2 W=50

*include bias circuits and 50n models
```

Christopher Schance

Problem 24.7

For the op-amp in Figure 24.21 determine the CMRR using hand calculations. Verify your hand calculations using simulations. How does the CMRR change based on the DC common-mode voltage?

Solution

Using equation (24.26) shown below along with $A_{OL}(f) = A_d \cdot A_2$, where A_d is the differential-mode gain of the diff amp, A_c is the common-mode gain of the diff amp, and A_2 is the gain of the second stage of the op amp in Figure 24.21.

$$CMRR = 20 \cdot \log\left|\frac{A_{OL}(f)}{A_c \cdot A_2}\right| = 20 \cdot \log\left|\frac{A_d}{A_c}\right|$$

Calculating A_d from equation (22.22),

$$A_d = -g_{m1,2}(r_{o2} \parallel r_{o4}) = -150uA/V \cdot (167k\Omega \parallel 333k\Omega) = -16.68V/V$$

Also, calculating A_c similar to equations (22.24) and (22.26), with R_o=4.2MΩ which is the output resistance of the cascode current source created by M6T and M6B,

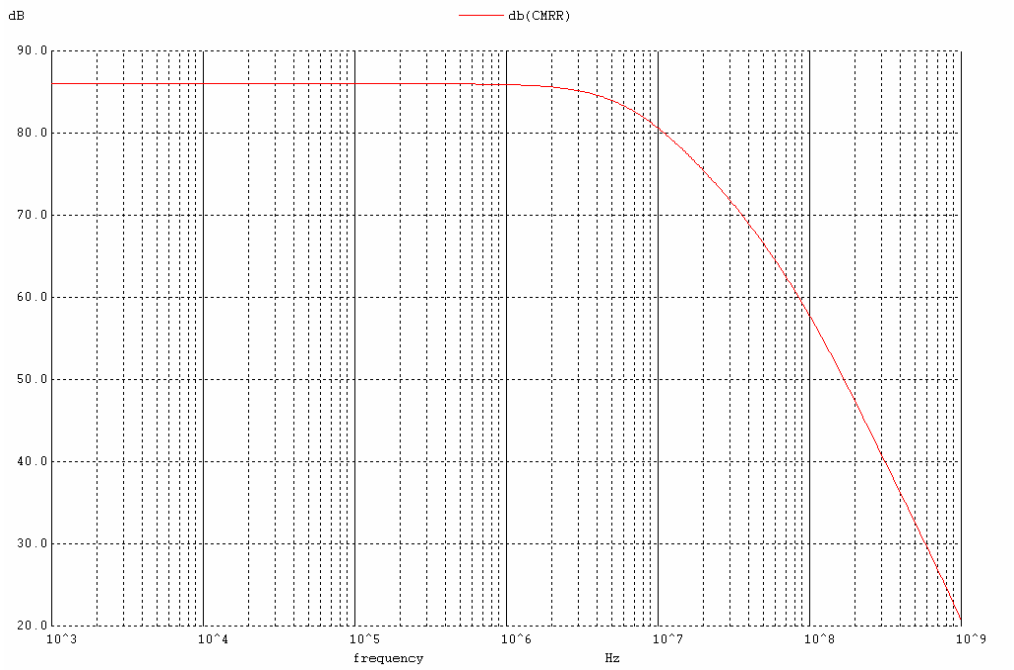
$$A_c = \frac{v_{out,diffamp}}{v_c} = \frac{\frac{1}{g_{m3,4}}}{\frac{1}{g_{m1,2}} + 2 \cdot R_o} = \frac{1}{g_{m3,4} \cdot \left(\frac{1}{g_{m1,2}} + 2 \cdot R_o\right)} = \frac{1}{150uA/V \cdot \left(\frac{1}{150uA/V} + 2 \cdot (4.2M\Omega)\right)}$$

$$A_c = 7.93 \times 10^{-4} V/V$$

Using the values of A_c and A_d in equation (24.26) yields

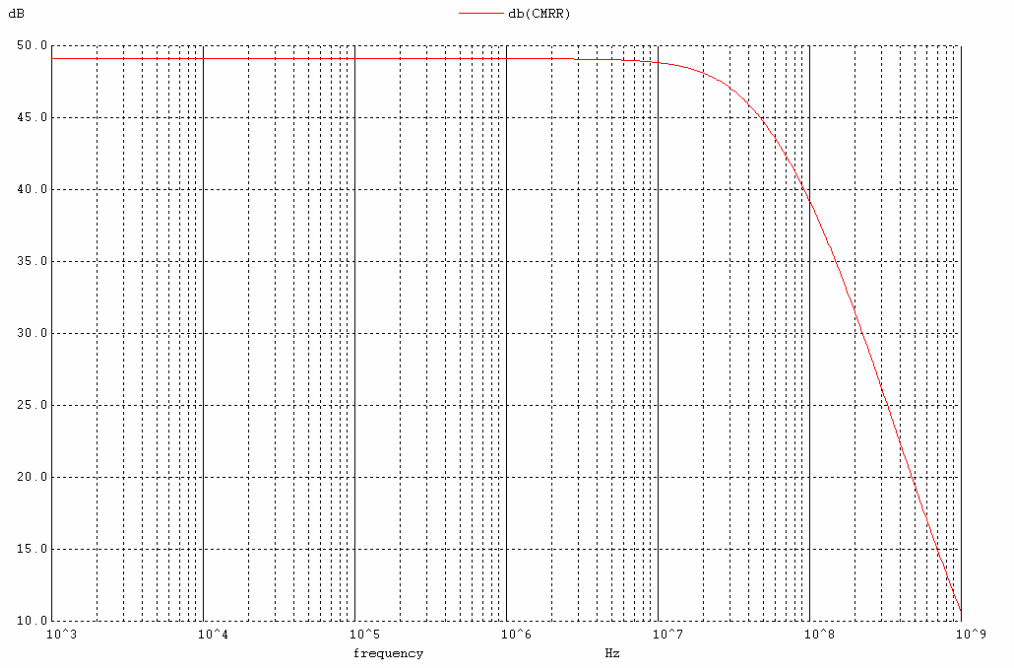
$$CMRR = 20 \cdot \log\left|\frac{A_d}{A_c}\right| = 20 \cdot \log\left|\frac{-16.68V/V}{7.93 \times 10^{-4} V/V}\right| = 86.46dB$$

In order to verify the hand calculations with SPICE, the configuration in Figure 24.25 is used. The simulation result, with a DC common-mode voltage of 700mV, is shown in the following plot. The result shows a CMRR of about 86dB, which agrees closely with the hand calculations. Also, at high frequencies, CMRR falls. This is caused by the capacitance at the sources of M1, M2 dominating at high frequencies, which results in a decrease of the impedance to ground at that node. Since this capacitance is in parallel with R_o, A_c will increase with high frequency, which causes CMRR to decrease. This drop in CMRR can be seen in the simulation results for frequencies greater than 1MHz.



CMRR of DC common-mode voltage of 700mV

Variations in the DC common-mode voltage will cause the voltage at the source of M1, M2 to vary. As a result, the voltage across the current source created by M6 will also vary. Higher DC common-mode voltages will cause the voltage across M6 to be larger, resulting in higher R_o for the current source created by M6. As a result, CMRR will go up as the DC common-mode voltage increases. This is true since R_o directly affects A_c, as outlined in the discussion above. The plot shown below is the CMRR with a DC common-mode voltage of 500mV. The CMRR drops to about 50dB for a common-mode voltage of 500mV.



CMRR for DC common-mode voltage of 500mV

```
*Problem 24.7

.control
destroy all
run
let CMRR=vaol/vaca2
plot db(CMRR)
.endc

*.option scale=50n ITL1=300 vntol=1u abstol=1u reltol=1u
.option scale=50n ITL1=300 rshunt=1e9
.ac dec 100 1k 1G

VDD     VDD     0       DC      1
Vin     Vin     0       DC      0.7     AC      1

Xopamp1 VDD     vaol    vin     vm1     opamp
Rbig1   vaol    vm1     100MEG
Cbig1   vm1     0       10u

Xopamp2 VDD     vaca2   vin     vm2     opamp
Rbig2   vaca2   vm2     100MEG
Cbig2   vin     vm2     10u


.subckt opamp VDD vout vp vm

Cc      Vout    Vd4t    240f

M1      vd1     vm      vss     0       NMOS L=2 W=50
M2      vout1   vp      vss     0       NMOS L=2 W=50
M6B     Vdb1    Vbias4  0       0       NMOS L=2 W=100
M6T     vss     Vbias3  vdb1    0       NMOS L=2 W=100
M3T     vd3t    vd1     VDD     VDD     PMOS L=1 W=100
M3B     vd1     vd1     vd3t    VDD     PMOS L=1 W=100
M4T     vd4t    vd1     VDD     VDD     PMOS L=1 W=100
M4B     vout1   vd1     vd4t    VDD     PMOS L=1 W=100

M7T     vd7t    Vout1   VDD     VDD     PMOS L=1 W=100
M7B     Vout    Vout1   vd7t    VDD     PMOS L=1 W=100

M8T     Vout    vbias3  vd8b    0       NMOS L=2 W=50
M8B     vd8b    vbias4  0       0       NMOS L=2 W=50

Xbias   VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

.ends

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1     Vbias3  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP2     Vbias4  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP3     vp1     vp2     VDD     VDD     PMOS L=2 W=100
MP4     vp2     Vbias2  vp1     VDD     PMOS L=2 W=100
MP5     Vpcas   Vpcas   vp2     VDD     PMOS L=2 W=100
MP6     Vbias2  Vbias2  VDD     VDD     PMOS L=10 W=20
MP7     Vhigh   Vbias1  VDD     VDD     PMOS L=2 W=100
MP8     Vbias1  Vbias2  Vhigh   VDD     PMOS L=2 W=100
MP9     vp3     Vbias1  VDD     VDD     PMOS L=2 W=100
MP10    Vncas   Vbias2  vp3     VDD     PMOS L=2 W=100

MN1     Vbias3  Vbias3  0       0       NMOS L=10 W=10
MN2     Vbias4  Vbias3  Vlow    0       NMOS L=2 W=50
MN3     Vlow    Vbias4  0       0       NMOS L=2 W=50
MN4     Vpcas   Vbias3  vn1     0       NMOS L=2 W=50
MN5     vn1     Vbias4  0       0       NMOS L=2 W=50
MN6     Vbias2  Vbias3  vn2     0       NMOS L=2 W=50
MN7     vn2     Vbias4  0       0       NMOS L=2 W=50
MN8     Vbias1  Vbias3  vn3     0       NMOS L=2 W=50
MN9     vn3     Vbias4  0       0       NMOS L=2 W=50
```

```
MN10    Vncas   Vncas   vn4     0       NMOS L=2 W=50
MN11    vn4     Vbias3  vn5     0       NMOS L=2 W=50
MN12    vn5     vn4     0       0       NMOS L=2 W=50

MBM1    Vbiasn  Vbiasn  0       0       NMOS L=2 W=50
MBM2    Vreg    Vreg    Vr      0       NMOS L=2 W=200
MBM3    Vbiasn  Vbiasp  VDD     VDD     PMOS L=2 W=100
MBM4    Vreg    Vbiasp  VDD     VDD     PMOS L=2 W=100

Rbias   Vr      0       5.5k

*amplifier
MA1     Vamp    Vreg    0       0       NMOS L=2 W=50
MA2     Vbiasp  Vbiasn  0       0       NMOS L=2 W=50
MA3     Vamp    Vamp    VDD     VDD     PMOS L=2 W=100
MA4     Vbiasp  Vamp    VDD     VDD     PMOS L=2 W=100

MCP     VDD     Vbiasp  VDD     VDD     PMOS L=100 W=100

*start-up stuff
MSU1    Vsur    Vbiasn  0       0       NMOS L=2   W=50
MSU2    Vsur    Vsur    VDD     VDD     PMOS L=20  W=10
MSU3    Vbiasp  Vsur    Vbiasn  0       NMOS L=1   W=10

.ends


* BSIM4 models
```

Problem 24.8 **Russell Benson, CNS**

Problem:

Simulate the Power Supply Rejection Ratios (PSRRs) for the op-amp in Figure 24.8 (with Rz of 6.5KΩ and a Cc of 2.4pF) and compare the results to the op-amp in Fig 24.21 when Cc is set to (also) 2.4pF (so each op-amp has the same gain-bandwidth).

Solution:

When designing an op-amp, a designer has many things to be concerned with including power supply rejection ratio (PSRR). The PSRR is a quantitative figure of merit for an op-amps ability to reject noise fed into the op-amp through VDD or ground. Read the discussion in Chapter 24 for a better understanding of how noise on the power supplies feeds through to the output. The equations for PSRR are as follows:

$PSRR^+$ - noise on VDD of op-amp.

$$PSRR^+ = A_{OL}(f)/(v_{out}/v^+)$$

$PSRR^-$ - noise on ground of op-amp.

$$PSRR^- = A_{OL}(f)/(v_{out}/v^-)$$

Ideally, an op-amp with infinite output resistance would show no change in v_{out} with respect to small changes on VDD or ground. Therefore, v_{out}/v^- would go to 0 and the PSRR term would be infinite. However in reality, CMOS op-amps have a finite output resistance that continues to worsen as the l of devices decreases into the nanometer range.

The schematic used to determine PSRR can be found in Figure 24.27. Note, when running simulations, only vary one of the power supplies (v^+ or v^-) at a time while holding the other constant. Generating all three graphs (A_{OL}, v^+, and v^-) can be accomplished in one netlist by setting up the op-amp as a sub-circuit and calling the sub-circuit three times (once for each of the terms above). See netlists at the end of the solution for an example. A couple of other things to mention about the netlists are that the ac signals on VDD and ground are fed to the bias circuit as well, but are not fed to CBig which is only used to bias up the op-amp properly for simulation.

Graphs for A_{OL}, v^+, and v^- for the two op-amps (Figure 24.8 and 24.21) are shown in Figures 1 and 2 on the following page.

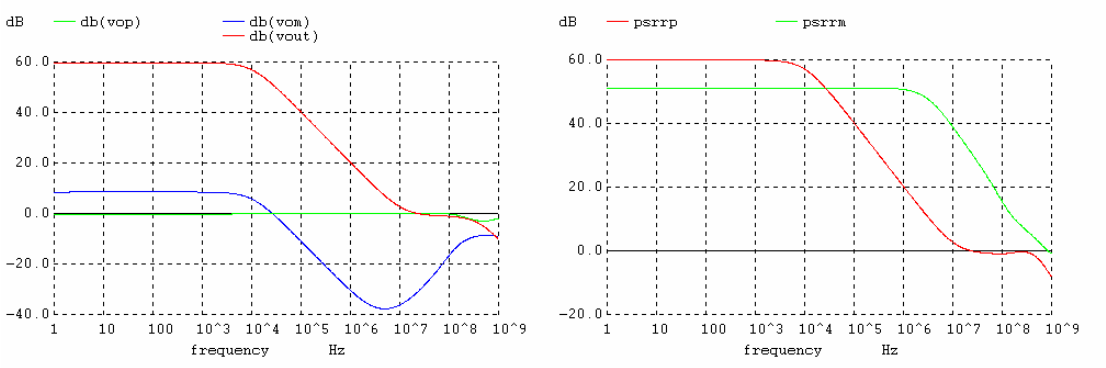


Figure1 - simulations results for op-amp in Figure 24.8.

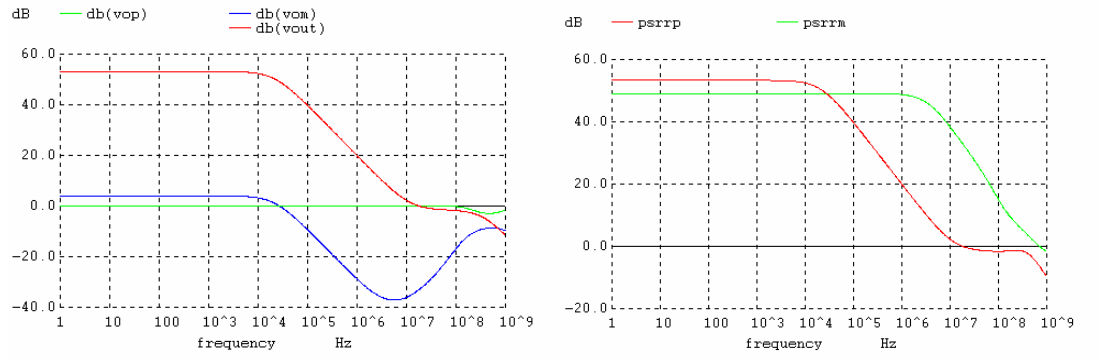


Figure1 - simulations results for op-amp in Figure 24.21.

Discussion:

To start, notice that for both op-amp topologies, the A_{OL}, v_{out}/v^+, and v_{out}/v^- graphs have the same form as those given in Figure 24b, c, and d. Note, the graphs in Figure 24 are all linear plots. Therefore for $v_{out}/v^+ = 1$, that is the same as above where $v_{out}/v^+ = 0$dB.

From the figures above it can be seen that the Figure 24.21 op-amp design does a better overall job of rejecting noise on ground in the lower frequencies. v_{out}/v^- for Figure 24.8 op-amp is ~8 while it is ~4 for Figure 24.21. This in turn increases the $PSRR^-$ for the figure 24.21 op-amp. However, one must notice that the overall open-loop gain is larger for the figure 24.8 op-amp resulting in similar $PSRR^-$ for the two topologies. v_{out}/v^+ shows no difference between the two op-amp topologies resulting in the Figure 24.21 op-amp to have a lower $PSRR^+$ overall compared to the Figure 24.8 op-amp.

Another important aspect to mention is a so-called $PSRR^+$ and $PSRR^-$ bandwidths (frequency range before $PSRR^+$ and $PSRR^-$ roll off). Note, that due to the v_{out}/v^- drop off at around 10KHz for both topologies, the $PSRR^-$ bandwidth is roughly 1MHz while the op-amp f_{3dB} frequency is back at 10KHz. This allows for a large rejection ratio within the op-amp operation range.

As mentioned above, v_{out}/v^+ remains constant at 0dB, or 1, throughout the frequency sweep. Therefore, $PSRR^+$ is basically equal to A_{OL} and the $PSRR^+$ bandwidth will be equal to the bandwidth of A_{OL}. Note, that the $PSRR^+$ bandwidth is slightly larger (few KHz) for the Figure 24.21 op-amp. However, as discussed in chapter 24, the indirect

feedback of the compensation current allows the unity gain frequency (as well as the f_{3db}) to be pushed out further increasing the speed of the op-amp while maintaining decent phase margin as compared to direct feedback compensation. This in turns translates to a better $PSRR^+$ for the indirect feedback compensation scheme. However, as shown above, the $PSRR^+$ for both topologies is within a few KHz when compensated to the same unity gain frequencies.

Netlists (note netlists do contain the bias circuit, but do not contain models):

```
*** Problem 24.8          Figure 24.8 Netlist      Russell Benson, CNS ***
.control
destroy all
run
set units=degrees
plot db(vout), db(vop), db(vom)
let psrrp=db(vout)-db(vop)
let psrrm=db(vout)-db(vom)
plot psrrp, psrrm
*print all
.endc

.option scale=50n ITL1=300 rshunt=1e9
.ac dec 100 1 1G
*.op

**********************Common Nodes*********************************
VDD     VDD     0       DC      1
VGRND   VGRND   0       DC      0
VPP     VPP     0       DC      500m
VPM     VPM     0       DC      500m

**********************Op-Amp Sim for OL Gain***********************
VP      VIN     0       DC      0.5     AC      1
RBIG    VOUT    VM      10MEG
CBIG    VM      0       100u
XAOL    VDD     VGRND   VIN     VM      VOUT    OPAMP


**********************Op-Amp Sim for AC VDD************************
VDDP    VDDP    0       DC      1       AC      1
RBP     VOP     VMP     10MEG
CBP     VMP     0       100u
XPSRR   VDDP    VGRND   VPP     VMP     VOP     OPAMP


**********************Op-Amp Sim for AC GROUND*********************
VNEGM   VNEGM   0       DC      0       AC      1
RBM     VOM     VMM     10MEG
CBM     VMM     0       100u
XMSRR   VDD     VNEGM   VPM     VMM     VOM     OPAMP


.subckt opamp  VDD     VGRND   vp      vm      vout

**********************Compensation*********************************
Cc      Vout    vout1   2400f
*RZ     VRZ     vout1   6.5k

**********************Op-Amp Circuit*******************************
M1      vd1     vm      vss     VGRND   NMOS L=2 W=50
M2      vout1   vp      vss     VGRND   NMOS L=2 W=50
M6B     Vdb1    Vbias4  VGRND   VGRND   NMOS L=2 W=100
M6T     vss     Vbias3  vdb1    VGRND   NMOS L=2 W=100
M3      vd1     vd1     VDD     VDD     PMOS L=2 W=100
M4      vout1   vd1     VDD     VDD     PMOS L=2 W=100
```

```
M7      vout    Vout1   VDD     VDD     PMOS L=2 W=100
M8T     Vout    vbias3  vd8b    VGRND   NMOS L=2 W=50
M8B     vd8b    vbias4  VGRND   VGRND   NMOS L=2 W=50

Xbias   VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas VGRND bias
.ends

**********************Bias Circuit*******************************
.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas VGRND
MP1     Vbias3  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP2     Vbias4  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP3     vp1     vp2     VDD     VDD     PMOS L=2 W=100
MP4     vp2     Vbias2  vp1     VDD     PMOS L=2 W=100
MP5     Vpcas   Vpcas   vp2     VDD     PMOS L=2 W=100
MP6     Vbias2  Vbias2  VDD     VDD     PMOS L=10 W=20
MP7     Vhigh   Vbias1  VDD     VDD     PMOS L=2 W=100
MP8     Vbias1  Vbias2  Vhigh   VDD     PMOS L=2 W=100
MP9     vp3     Vbias1  VDD     VDD     PMOS L=2 W=100
MP10    Vncas   Vbias2  vp3     VDD     PMOS L=2 W=100

MN1     Vbias3  Vbias3  VGRND   VGRND   NMOS L=10 W=10
MN2     Vbias4  Vbias3  Vlow    VGRND   NMOS L=2 W=50
MN3     Vlow    Vbias4  VGRND   VGRND   NMOS L=2 W=50
MN4     Vpcas   Vbias3  vn1     VGRND   NMOS L=2 W=50
MN5     vn1     Vbias4  VGRND   VGRND   NMOS L=2 W=50
MN6     Vbias2  Vbias3  vn2     VGRND   NMOS L=2 W=50
MN7     vn2     Vbias4  VGRND   VGRND   NMOS L=2 W=50
MN8     Vbias1  Vbias3  vn3     VGRND   NMOS L=2 W=50
MN9     vn3     Vbias4  VGRND   VGRND   NMOS L=2 W=50
MN10    Vncas   Vncas   vn4     VGRND   NMOS L=2 W=50
MN11    vn4     Vbias3  vn5     VGRND   NMOS L=2 W=50
MN12    vn5     vn4     VGRND   VGRND   NMOS L=2 W=50

MBM1    Vbiasn  Vbiasn  VGRND   VGRND   NMOS L=2 W=50
MBM2    Vreg    Vreg    Vr      VGRND   NMOS L=2 W=200
MBM3    Vbiasn  Vbiasp  VDD     VDD     PMOS L=2 W=100
MBM4    Vreg    Vbiasp  VDD     VDD     PMOS L=2 W=100

Rbias   Vr      VGRND   5.5k

*amplifier
MA1     Vamp    Vreg    VGRND   VGRND   NMOS L=2 W=50
MA2     Vbiasp  Vbiasn  VGRND   VGRND   NMOS L=2 W=50
MA3     Vamp    Vamp    VDD     VDD     PMOS L=2 W=100
MA4     Vbiasp  Vamp    VDD     VDD     PMOS L=2 W=100

MCP     VDDM    Vbiasp  VDD     VDD     PMOS L=100 W=100

*start-up stuff
MSU1    Vsur    Vbiasn  VGRND   VGRND   NMOS L=2   W=50
MSU2    Vsur    Vsur    VDD     VDD     PMOS L=20  W=10
MSU3    Vbiasp  Vsur    Vbiasn  VGRND   NMOS L=1   W=10

.ends
```

****** Problem 24.8 Figure 24.21 Netlist Russell Benson, CNS ******

```
.control
destroy all
run
set units=degrees
plot db(vout), db(vop), db(vom)
let psrrp=db(vout)-db(vop)
let psrrm=db(vout)-db(vom)
plot psrrp, psrrm
*print all
.endc

.option scale=50n ITL1=300
.ac dec 100 1 1G
*.op
```

```
**********Common Nodes**********
VDD     VDD     0       DC      1
VGRND   VGRND   0       DC      0
VPP     VPP     0       DC      500m
VPM     VPM     0       DC      500m

**********Op-Amp Sim for OL Gain**********
VP      VIN     0       DC      0.5     AC      1
RBIG    VOUT    VM      100MEG
CBIG    VM      0       100u
XAOL    VDD     VGRND   VIN     VM      VOUT    OPAMP


**********Op-Amp Sim for AC VDD**********
VDDP    VDDP    0       DC      1       AC      1
RBP     VOP     VMP     100MEG
CBP     VMP     0       100u
XPSRR   VDDP    VGRND   VPP     VMP     VOP     OPAMP


**********Op-Amp Sim for AC GROUND**********
VNEGM   VNEGM   0       DC      0       AC      1
RBM     VOM     VMM     100MEG
CBM     VMM     0       100u
XMSRR   VDD     VNEGM   VPM     VMM     VOM     OPAMP


.subckt opamp  VDD     VGRND   vp      vm      vout

**********Compensation**********
Cc      Vout    Vout1   2400f

**********Op-Amp Circuit**********
M1      vd1     vm      vss     VGRND   NMOS L=2 W=50
M2      vout1   vp      vss     VGRND   NMOS L=2 W=50
M6B     Vdb1    Vbias4  VGRND   VGRND   NMOS L=2 W=100
M6T     vss     Vbias3  vdb1    VGRND   NMOS L=2 W=100
M3T     vd3t    vd1     VDD     VDD     PMOS L=1 W=100
M3B     vd1     vd1     vd3t    VDD     PMOS L=1 W=100
M4T     vd4t    vd1     VDD     VDD     PMOS L=1 W=100
M4B     vout1   vd1     vd4t    VDD     PMOS L=1 W=100


M7T     vd7t    Vout1   VDD     VDD     PMOS L=1 W=100
M7B     Vout    Vout1   vd7t    VDD     PMOS L=1 W=100

M8T     Vout    vbias3  vd8b    VGRND   NMOS L=2 W=50
M8B     vd8b    vbias4  VGRND   VGRND   NMOS L=2 W=50

Xbias   VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas VGRND bias
.ends

**********Bias Circuit**********
.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas VGRND
MP1     Vbias3  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP2     Vbias4  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP3     vp1     vp2     VDD     VDD     PMOS L=2 W=100
MP4     vp2     Vbias2  vp1     VDD     PMOS L=2 W=100
MP5     Vpcas   Vpcas   vp2     VDD     PMOS L=2 W=100
MP6     Vbias2  Vbias2  VDD     VDD     PMOS L=10 W=20
MP7     Vhigh   Vbias1  VDD     VDD     PMOS L=2 W=100
MP8     Vbias1  Vbias2  Vhigh   VDD     PMOS L=2 W=100
MP9     vp3     Vbias1  VDD     VDD     PMOS L=2 W=100
MP10    Vncas   Vbias2  vp3     VDD     PMOS L=2 W=100

MN1     Vbias3  Vbias3  VGRND   VGRND   NMOS L=10 W=10
MN2     Vbias4  Vbias3  Vlow    VGRND   NMOS L=2 W=50
MN3     Vlow    Vbias4  VGRND   VGRND   NMOS L=2 W=50
MN4     Vpcas   Vbias3  vn1     VGRND   NMOS L=2 W=50
MN5     vn1     Vbias4  VGRND   VGRND   NMOS L=2 W=50
```

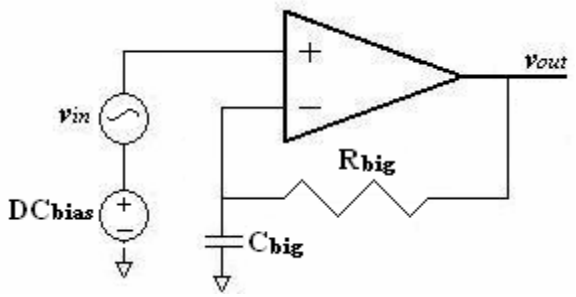
```
MN6     Vbias2  Vbias3  vn2     VGRND   NMOS L=2 W=50
MN7     vn2     Vbias4  VGRND   VGRND   NMOS L=2 W=50
MN8     Vbias1  Vbias3  vn3     VGRND   NMOS L=2 W=50
MN9     vn3     Vbias4  VGRND   VGRND   NMOS L=2 W=50
MN10    Vncas   Vncas   vn4     VGRND   NMOS L=2 W=50
MN11    vn4     Vbias3  vn5     VGRND   NMOS L=2 W=50
MN12    vn5     vn4     VGRND   VGRND   NMOS L=2 W=50

MBM1    Vbiasn  Vbiasn  VGRND   VGRND   NMOS L=2 W=50
MBM2    Vreg    Vreg    Vr      VGRND   NMOS L=2 W=200
MBM3    Vbiasn  Vbiasp  VDD     VDD     PMOS L=2 W=100
MBM4    Vreg    Vbiasp  VDD     VDD     PMOS L=2 W=100

Rbias   Vr      VGRND   5.5k

*amplifier
MA1     Vamp    Vreg    VGRND   VGRND   NMOS L=2 W=50
MA2     Vbiasp  Vbiasn  VGRND   VGRND   NMOS L=2 W=50
MA3     Vamp    Vamp    VDD     VDD     PMOS L=2 W=100
MA4     Vbiasp  Vamp    VDD     VDD     PMOS L=2 W=100

MCP     VDDM    Vbiasp  VDD     VDD     PMOS L=100 W=100

*start-up stuff
MSU1    Vsur    Vbiasn  VGRND   VGRND   NMOS L=2   W=50
MSU2    Vsur    Vsur    VDD     VDD     PMOS L=20  W=10
MSU3    Vbiasp  Vsur    Vbiasn  VGRND   NMOS L=1   W=10

.ends
```

24.9) Ben Rivera

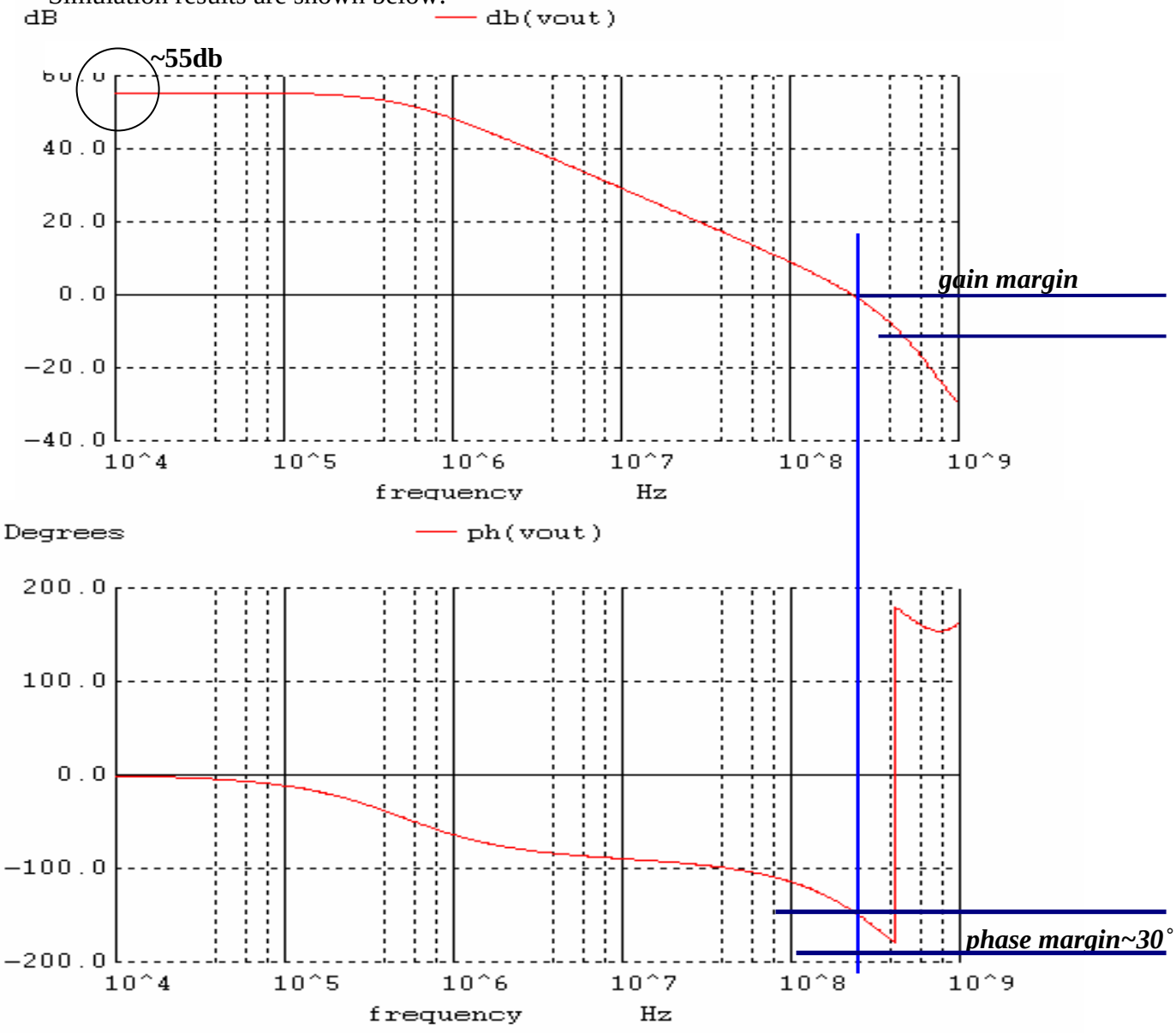
Simulate the operation of the op-amp in Fig. 24.28. Show the open-loop frequency response of the op-amp. What is the op-amp's PM? Show the op-amp's step response when it is put into a follower configuration driving a 100fF load with an input step in voltage from 100mV to 900mV.

Biasing circuit used is from Fig. 20.47.

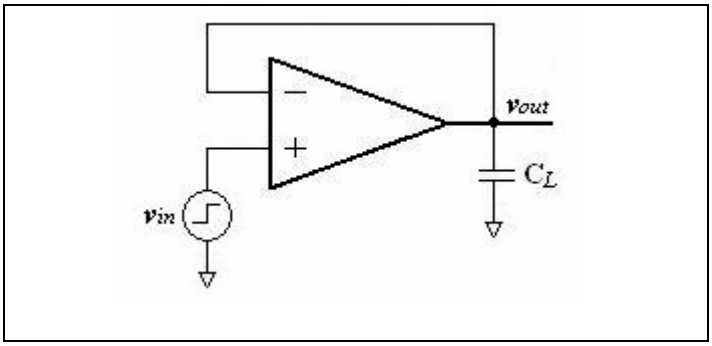
For simulating the open-loop response we know that in order to DC bias the circuit correctly we need to put the op-amp in the following configuration.

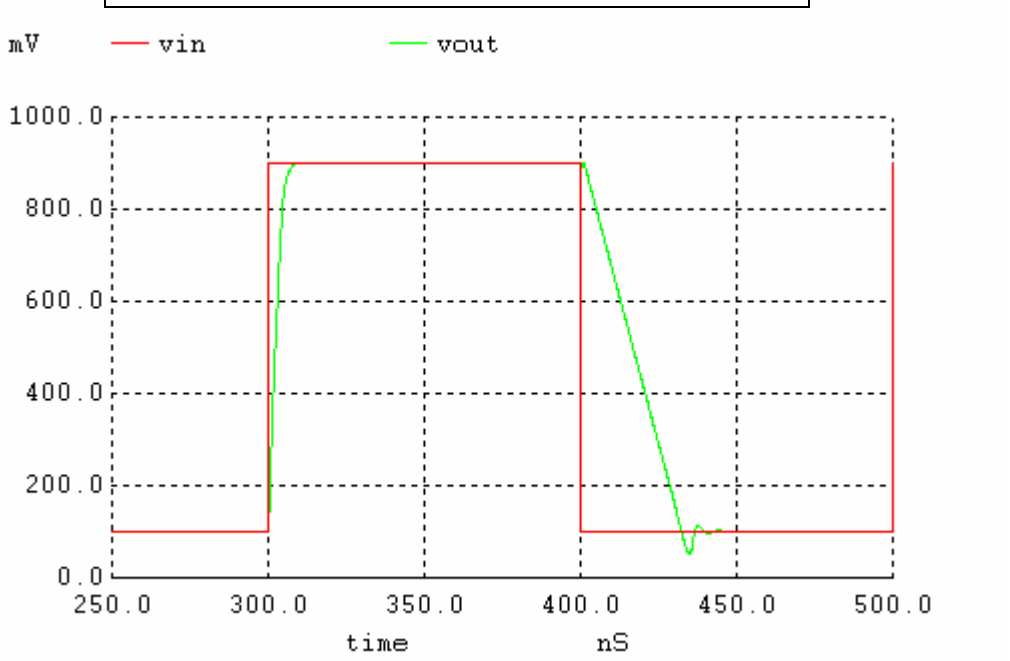


Simulation results are shown below:

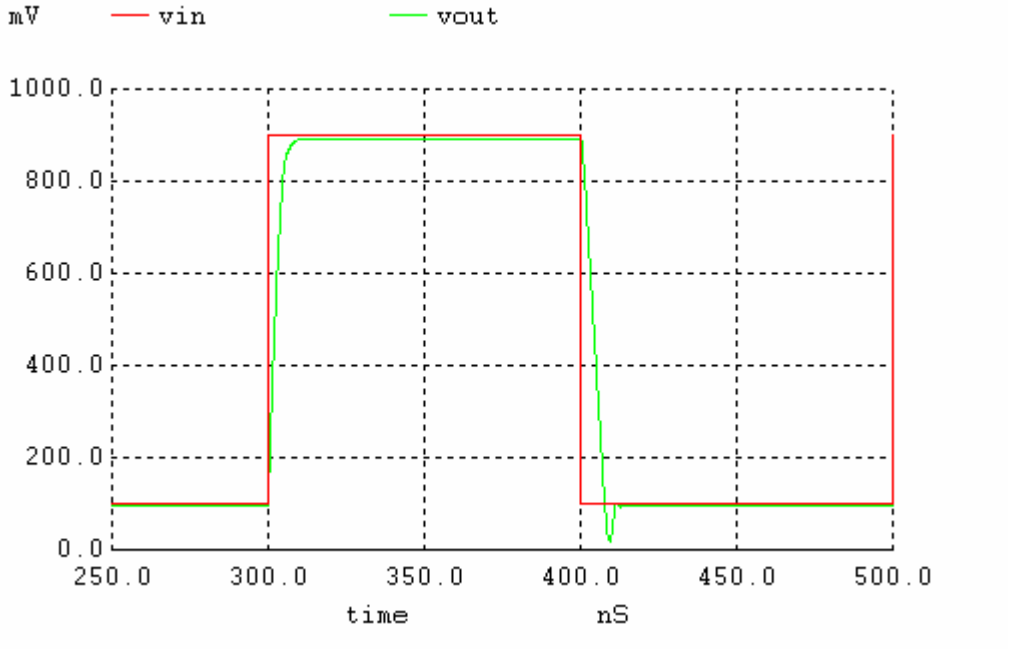


Step response of the amplifier in the follower configuration driving a 100fF load capacitance.





Step response doesn't look that good when trying to pull the voltage to ground. To improve this we can allow the NMOS transistors to sink more current by reducing the length size on the output NMOS transistors, results are shown below.



*** Figure 24.28***

```
.control
destroy all
run
set units=degrees
*plot ph(vout)
*plot db(vout)
plot vin vout ylimit 250n 500n
.endc

.option scale=50n ITL1=300 rshunt=1e9
*.ac dec 100 10k 1G
.tran .1n 600n .1n UIC

VDD    VDD    0      DC     1
*Vin   Vin    0      DC     0.5    AC     1
Vin    Vin    0      DC     0      Pulse(100m 900m 100n 0n 0n 100n 200n)

Xota   VDD    vout   vin    vm     opamp

*Rbig  vout   vm     10MEG
*Cbig  vm     0      1u
Cl     vout   0      100f

.subckt opamp VDD vout vp vm

Xbias  VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

MA1    vd3    vout   vs1    VDD    PMOS L=2 W=100
MA2    vd7    vp     vs1    VDD    PMOS L=2 W=100
MA3    vda3   vout   vsa3   0      NMOS L=2 W=50
MA4    vda4   vp     vsa3   0      NMOS L=2 W=50

M1     vs2    vbias1 VDD    VDD    PMOS L=2 W=100
M2     vs1    vbias2 vs2    VDD    PMOS L=2 W=100
M3     vd3    vbias3 vd4    0      NMOS L=2 W=50
M4     vd4    vd3    0      0      NMOS L=2 W=50
M5     vs6    vbias1 VDD    VDD    PMOS L=2 W=100
M6     vs1    vbias2 vs6    VDD    PMOS L=2 W=100
M7     vd7    vbias3 vd8    0      NMOS L=2 W=50
M8     vd8    vd7    0      0      NMOS L=2 W=50
M9     vda4   vbias3 vd9    0      NMOS L=2 W=50
M10    vd9    vd3    0      0      NMOS L=2 W=50
M11    vda3   vbias3 vd12   0      NMOS L=2 W=50
M12    vd12   vd7    0      0      NMOS L=2 W=50
M13    vs14   vda3   VDD    VDD    PMOS L=1 W=200
M14    vda3   vda3   vs14   VDD    PMOS L=1 W=200
M15    vsa3   vbias3 vd16   0      NMOS L=2 W=50
M16    vd16   vbias4 0      0      NMOS L=2 W=50
M17    vs18   vda3   VDD    VDD    PMOS L=1 W=200
M18    vda4   vda3   vs18   VDD    PMOS L=1 W=200
M19    vsa3   vbias3 vd20   0      NMOS L=2 W=50
M20    vd20   vbias4 0      0      NMOS L=2 W=50

MB1    vdmb2  vda4   VDD    VDD    PMOS L=1 W=200
MB2    vout   vda4   vdmb2  VDD    PMOS L=1 W=200
MB3    vout   vbias3 vdmb3  0      NMOS L=2 W=50
MB4    vdmb3  vbias4 0      0      NMOS L=2 W=50
```

Cc vout vs18 240f

.ends

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1	Vbias3	Vbiasp	VDD	VDD	PMOS L=2 W=100
MP2	Vbias4	Vbiasp	VDD	VDD	PMOS L=2 W=100
MP3	vp1	vp2	VDD	VDD	PMOS L=2 W=100
MP4	vp2	Vbias2	vp1	VDD	PMOS L=2 W=100
MP5	Vpcas	Vpcas	vp2	VDD	PMOS L=2 W=100
MP6	Vbias2	Vbias2	VDD	VDD	PMOS L=10 W=20
MP7	Vhigh	Vbias1	VDD	VDD	PMOS L=2 W=100
MP8	Vbias1	Vbias2	Vhigh	VDD	PMOS L=2 W=100
MP9	vp3	Vbias1	VDD	VDD	PMOS L=2 W=100
MP10	Vncas	Vbias2	vp3	VDD	PMOS L=2 W=100
MN1	Vbias3	Vbias3	0	0	NMOS L=10 W=10
MN2	Vbias4	Vbias3	Vlow	0	NMOS L=2 W=50
MN3	Vlow	Vbias4	0	0	NMOS L=2 W=50
MN4	Vpcas	Vbias3	vn1	0	NMOS L=2 W=50
MN5	vn1	Vbias4	0	0	NMOS L=2 W=50
MN6	Vbias2	Vbias3	vn2	0	NMOS L=2 W=50
MN7	vn2	Vbias4	0	0	NMOS L=2 W=50
MN8	Vbias1	Vbias3	vn3	0	NMOS L=2 W=50
MN9	vn3	Vbias4	0	0	NMOS L=2 W=50
MN10	Vncas	Vncas	vn4	0	NMOS L=2 W=50
MN11	vn4	Vbias3	vn5	0	NMOS L=2 W=50
MN12	vn5	vn4	0	0	NMOS L=2 W=50
MBM1	Vbiasn	Vbiasn	0	0	NMOS L=2 W=50
MBM2	Vreg	Vreg	Vr	0	NMOS L=2 W=200
MBM3	Vbiasn	Vbiasp	VDD	VDD	PMOS L=2 W=100
MBM4	Vreg	Vbiasp	VDD	VDD	PMOS L=2 W=100
Rbias	Vr	0	5.5k		
*amplifier					
MA1	Vamp	Vreg	0	0	NMOS L=2 W=50
MA2	Vbiasp	Vbiasn	0	0	NMOS L=2 W=50
MA3	Vamp	Vamp	VDD	VDD	PMOS L=2 W=100
MA4	Vbiasp	Vamp	VDD	VDD	PMOS L=2 W=100
MCP	VDD	Vbiasp	VDD	VDD	PMOS L=100 W=100
*start-up stuff					
MSU1	Vsur	Vbiasn	0	0	NMOS L=2 W=50
MSU2	Vsur	Vsur	VDD	VDD	PMOS L=20 W=10
MSU3	Vbiasp	Vsur	Vbiasn	0	NMOS L=1 W=10

.ends

Name:Vijayakumar Srinivasan
Problem: 24.10

Given the gain-bw(funity) product of the opamp is 100MHz. The gain of the amplifier seen in Figure 1 is -5.

Gain= -R2/R1= -5

Bandwidth=100MHZ/gain= 20MHz.

Also we have (Av*f3db)= funity, so that gives us the f3b as 20MHz. f3db is the frequency where the gain of the amplifier is down by 3db from its low frequency value.

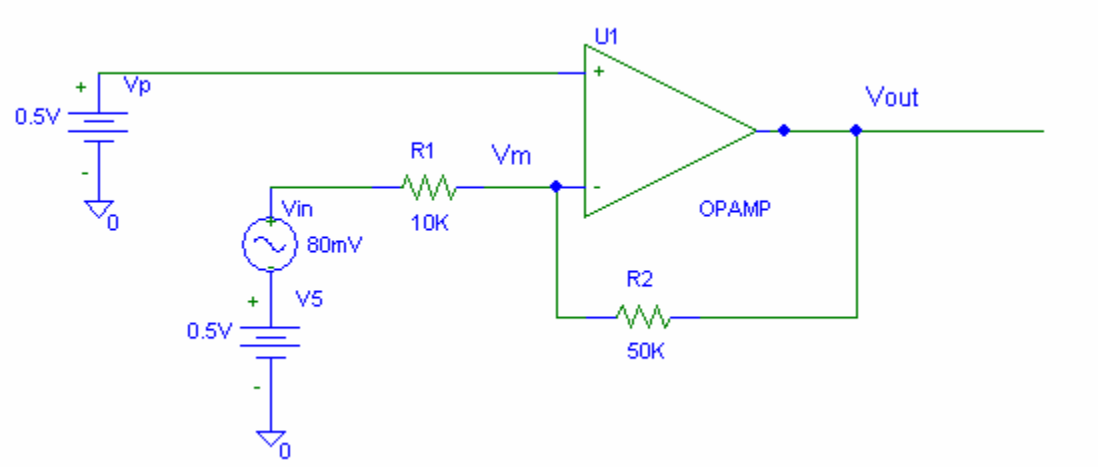


Figure1. Amplifier using Figure24.29 (refer book)

Simulating this amplifier we get, the f3b as approx. 22MHz. The difference might be due to the lot of approximation we made in our calculations. The simulation result is shown below in Figure 2.

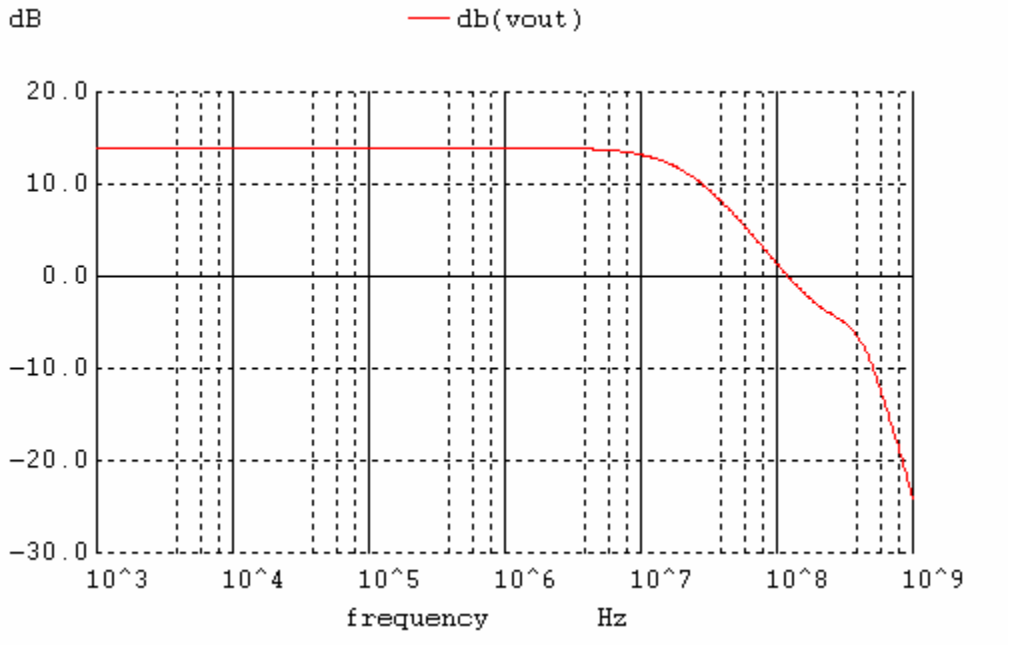


Figure 2. Gain of the amplifier shown in Figure 1

The maximum and minimum voltage on the input of the amplifier is given by taking into account that the node ‘m’ would ideally be at the same voltage as node ‘p’. The gain of the amplifier is defined as -5. If the AC input is zero, the nodes m and p would be at 500mV each. Now to get the output voltage to swing from 900-100 (mV) (which would be +400mV to -400mV with respect to the DC input), the AC input has to swing by 400mV/5=80mV. So if we give a sinusoidal AC input with an amplitude of 80mV to the DC level that we have, we should see the desired 100mV to 900mV output swing. This result is shown in Figure 3.

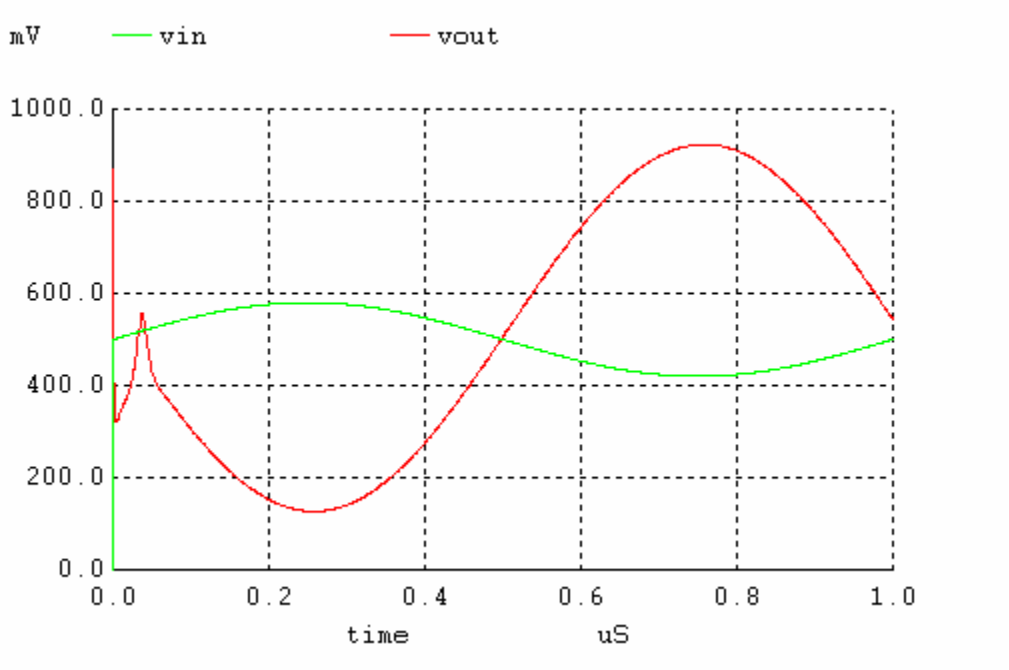


Figure 3. Output swing for the amplifier for an AC input of 80mV

The modified netlist is given below.

```
*** Figure 24.final CMOS: Circuit Design, Layout, and Simulation ***

.control
destroy all
run
set units=degrees
plot vout vin
.endc

.option scale=50n ITL1=300 reltol=1u abstol=1p
.tran 1n 1u 0n 1n UIC

VDD    VDD    0      DC     1
Vcm    Vcm    0      DC     0.5
vin    Vin    0      DC     0.5    AC     50m    sin 0.5 80m 1Meg

Xopamp       VDD    vout   vcm    vm     opamp
R2     vout   vm     50k
R1     vin    vm     10k

.subckt opamp VDD vout vp vm
```

```
Xbias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

M1B   n2    vm    n8    0     NMOS L=2 W=50
M1T   n6    n4    n2    0     NMOS L=2 W=50
M2B   n3    vp    n8    0     NMOS L=2 W=50
M2T   n1    n4    n3    0     NMOS L=2 W=50
MCM   n4    n4    n8    0     NMOS L=10 W=10
M6T   n8    Vbias3      n12   0     NMOS L=2 W=150
M6B   n12   Vbias4      0     0     NMOS L=2 W=150
M8T   n10   Vbias3      n11   0     NMOS L=2 W=50
M8B   n11   Vbias4      0     0     NMOS L=2 W=50
MFCN  n1    Vncas n10   0     NMOS L=2 W=25
MON   vout  n10   0     0     NMOS L=2 W=500

M3B   n6    Vbias2      n5    VDD   PMOS L=2 W=100
M3T   n5    n6    VDD   VDD   PMOS L=2 W=100
M5T   n13   Vbias1      VDD   VDD   PMOS L=2 W=100
M5B   n4    Vbias2      n13   VDD   PMOS L=2 W=100
M4T   n7    n6    VDD   VDD   PMOS L=2 W=100
M4B   n1    Vbias2      n7    VDD   PMOS L=2 W=100
M9T   n9    n6    VDD   VDD   PMOS L=2 W=100
M9B   n1    Vbias2      n9    VDD   PMOS L=2 W=100
MFCP  n10   Vpcas n1    VDD   PMOS L=2 W=50
MOP   vout  n1    VDD   VDD   PMOS L=2 W=1000

Cc1   vout  n7    120f
Cc2   vout  n3    120f
.ends


.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1   Vbias3      Vbiasp      VDD   VDD   PMOS L=2 W=100
MP2   Vbias4      Vbiasp      VDD   VDD   PMOS L=2 W=100
MP3   vp1   vp2   VDD   VDD   PMOS L=2 W=100
MP4   vp2   Vbias2      vp1   VDD   PMOS L=2 W=100
MP5   Vpcas Vpcas vp2   VDD   PMOS L=2 W=100
MP6   Vbias2      Vbias2      VDD   VDD   PMOS L=10 W=20
MP7   Vhigh Vbias1      VDD   VDD   PMOS L=2 W=100
MP8   Vbias1      Vbias2      Vhigh VDD   PMOS L=2 W=100
MP9   vp3   Vbias1      VDD   VDD   PMOS L=2 W=100
MP10  Vncas Vbias2      vp3   VDD   PMOS L=2 W=100

MN1   Vbias3      Vbias3      0     0     NMOS L=10 W=10
MN2   Vbias4      Vbias3      Vlow  0     NMOS L=2 W=50
MN3   Vlow  Vbias4      0     0     NMOS L=2 W=50
MN4   Vpcas Vbias3      vn1   0     NMOS L=2 W=50
MN5   vn1   Vbias4      0     0     NMOS L=2 W=50
MN6   Vbias2      Vbias3      vn2   0     NMOS L=2 W=50
MN7   vn2   Vbias4      0     0     NMOS L=2 W=50
MN8   Vbias1      Vbias3      vn3   0     NMOS L=2 W=50
MN9   vn3   Vbias4      0     0     NMOS L=2 W=50
MN10  Vncas Vncas vn4   0     NMOS L=2 W=50
MN11  vn4   Vbias3      vn5   0     NMOS L=2 W=50
MN12  vn5   vn4   0     0     NMOS L=2 W=50
```

```
MBM1  Vbiasn      Vbiasn      0     0     NMOS L=2 W=50
MBM2  Vreg  Vreg  Vr    0     NMOS L=2 W=200
MBM3  Vbiasn      Vbiasp      VDD   VDD   PMOS L=2 W=100
MBM4  Vreg  Vbiasp      VDD   VDD   PMOS L=2 W=100

Rbias Vr    0     5.5k

*amplifier
MA1   Vamp  Vreg  0     0     NMOS L=2 W=50
MA2   Vbiasp      Vbiasn      0     0     NMOS L=2 W=50
MA3   Vamp  Vamp  VDD   VDD   PMOS L=2 W=100
MA4   Vbiasp      Vamp  VDD   VDD   PMOS L=2 W=100

MCP   VDD   Vbiasp      VDD   VDD   PMOS L=100 W=100

*start-up stuff
MSU1  Vsur  Vbiasn      0     0     NMOS L=2   W=50
MSU2  Vsur  Vsur  VDD   VDD   PMOS L=20  W=10
MSU3  Vbiasp      Vsur  Vbiasn      0     NMOS L=1   W=10

.ends


* BSIM4 models here..
*
```

Problem 24.11 submitted by Usan Fung

Suppose it is decided to eliminate the 500mV common-mode voltage in the amplifier seen in Fig.24.65 and to use ground, as seen in Fig 24.66. Knowing the input voltage can only fall in between ground and VDD. What is the problem one will encounter?

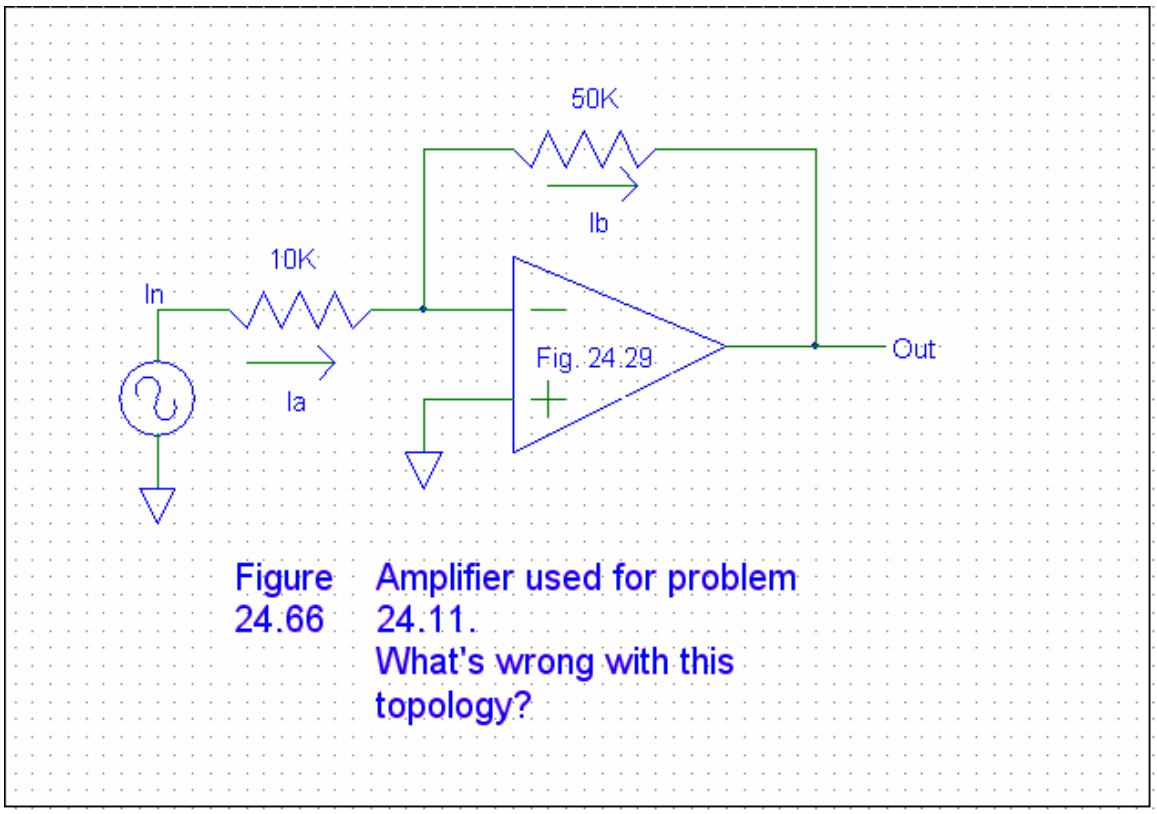


Figure 24.66 Amplifier used for problem 24.11. What's wrong with this topology?

To understand what problem one will encounter when the 500mV common mode voltage is removed and use ground instead, let's find out how the output voltage range is affected by analyzing the feedback network using the minimum and maximum input voltage allowed.

$V_+ = V_- = 0V$ Given that the common mode voltage is at ground

$I_a = (V_{in}-V_-) / 10k$ ------- (1)

$I_b = (V_--V_{out}) / 50k$ ------- (2)

1) With input voltage (V_{in}) at 0V and both V_+ and V_- at 0V, below is the calculation for the output voltage (V_{out}):

$I_a = I_b$
→ $(V_{in}-V_-) / 10k = (V_--V_{out}) / 50k$
→ $V_{out} = 0V$

2) With input voltage (V_{in}) at 1V and both V_+ and V_- at 0V, below is the calculation for the output voltage (V_{out}):

$I_a = I_b$
→ $(V_{in}-V_-) / 10k = (V_--V_{out}) / 50k$
→ $1/10k = -V_{out} / 50k$
→ $V_{out} = -5V$

From the result above, the output voltage range will be limited to within 0V and -5V which is not ideal or practical.
In order to be able to have positive output voltage, one need to have an input common mode voltage to be set, usually is the average of the two inputs in order to keep the diff amp operates in saturation region. (For example in problem 24.10, with input commode mode at 500mV)

In problem 24.10, the output voltages are at 250mV and 750mV, with an input of 0V and 1V respectively.

PROBLEM 24.12
Submitted by T.Vamshi Krishna

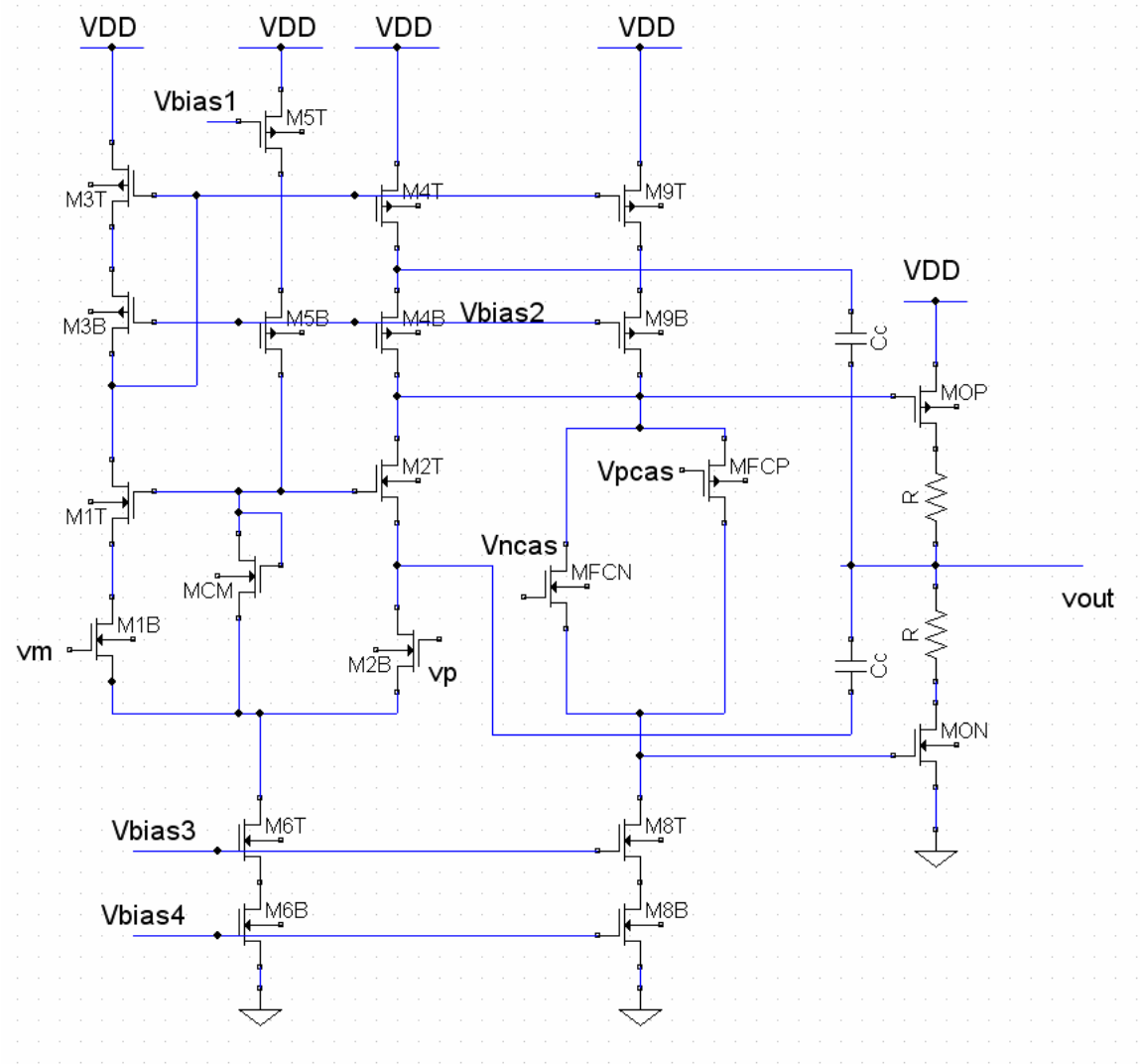


Figure 1.

The op amp in the given above configuration can source maximum amount of current when the MON transistor is off and similarly it can sink maximum amount of current when MOP is off. In the above figure since MOP and MON are sized to be 10 times than the regular sizes given in table 9.2, the amount of current that flows through each of the transistors is also increased by 10 times.

Keeping 100Ω resistors in series with the transistors will not affect the amount of current that can be sourced or sinked by the op amp. Thus the maximum amount of current the op amp can source or sink with 100Ω resistors present is still the same as the op amp without the resistors. The op amp still sources maximum current when MON transistor is off and sinks maximum amount of current when MOP is off.

But in order to demonstrate what happens if the output is shorted, consider the op amp connected in unity gain configuration as shown in figure 2 below. Now if the output is shorted then the inverting terminal of the op amp is at ground as a result the gate of the MOP will also be at ground thus turning on the MOP transistor fully. Connecting 100Ω resistors will limit the amount of current that flows through the MOP. Similar argument can be made for MON i.e. if output is connected to VDD.

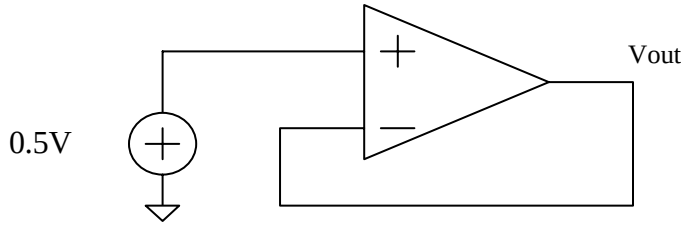


Figure 2.

To determine how the closed loop output resistance of the op amp is affected we connect a test voltage at the output and measure the test current that flows in the circuit. Thus the ratio of test voltage and test current gives the closed loop output resistance. The schematic diagram of the op amp in inverting gain of one configuration is shown below in figure 3. The load resistor and capacitor are not shown in the figure.

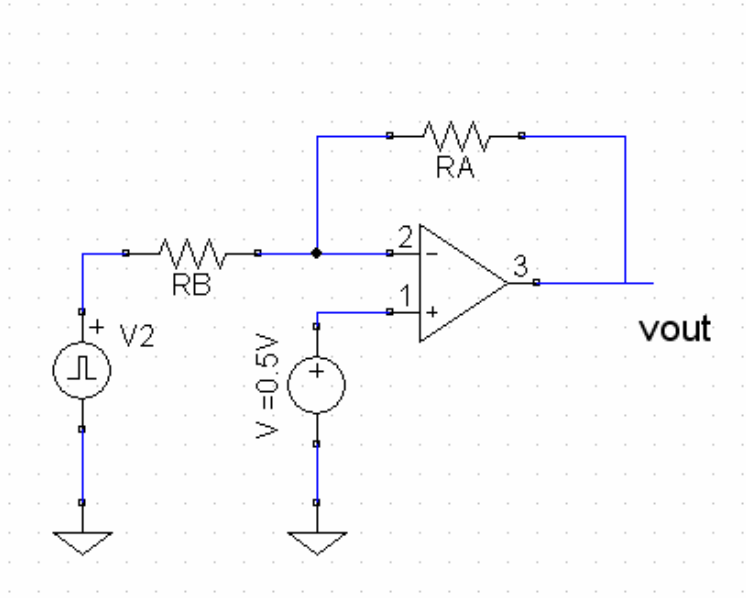


Figure 3.

The figure below shows connecting a test voltage at the output so as to measure the closed loop output resistance of the op amp shown in figure 3.

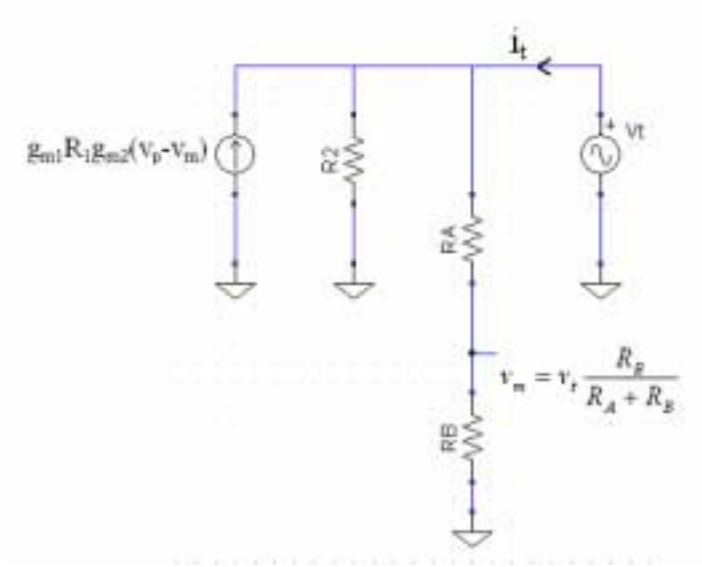


Figure 4.

$g_{m1}R_1$ is the gain of the first stage, while R_2 is the resistance of the second stage, which is given as $r_{mon}||r_{mop}$ and R_A and R_B are the feedback resistors.

First we will derive an expression for closed loop output resistance without taking the 100Ω resistors into consideration. After deriving an expression for closed loop output resistance then we will see how the 100Ω resistors affect the closed loop output resistance of the op amp.

The test current that is flowing as a result of test voltage can be written as

$$i_t = \frac{v_t}{R_2} + \frac{v_t}{R_A + R_B} + g_{m1}R_1g_{m2}(v_p - v_m) - - - - - (1)$$

From figure 4. we can write

$$v_m = v_t \frac{R_B}{R_A + R_B}$$

$$\Rightarrow \frac{v_t}{1 + \frac{R_A}{R_B}} = \frac{v_t}{1 + |A_{CL}|}$$

$v_p = 0$ (AC ground)

where $|A_{CL}|$ is the closed loop gain of the op amp.

Thus substituting the values of v_p and v_m in eq (1) we get

$$i_t = \frac{v_t}{R_2} + \frac{v_t}{R_A + R_B} + g_{m1} R_1 g_{m2} \left(\frac{v_t}{1 + |A_{CL}|}\right)$$

If we assume the current through the feedback path is small then the closed loop output resistance is given by

$$\frac{v_t}{i_t} = R_{out,CL} = \frac{1}{\frac{1}{R_2} + \frac{g_{m1} R_1 g_{m2}}{1 + |A_{CL}|}}$$

$$\frac{v_t}{i_t} = R_{out,CL} = \frac{R_2(1 + |A_{CL}|)}{1 + g_{m1} R_1 g_{m2} R_2} = \frac{R_2(1 + |A_{CL}|)}{A_{OLDC}} ----(2)$$

where A_{OLDC} is the DC open loop gain of the op amp and $R_2 = r_{mon} || r_{mop}$.

Thus the closed loop output resistance of the op amp is given by eq (2).

Now connecting 100Ω resistors at the output as shown in the figure 1, changes the output resistance of the second stage. So now the output resistance becomes

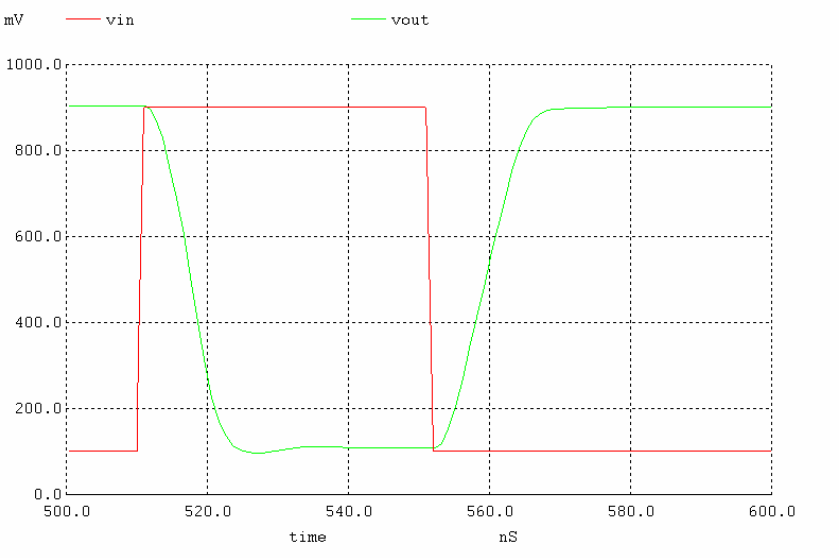
$$R_2 = (r_{mon} + 100\Omega) \text{ ll } (r_{mop} + 100\Omega)$$

Thus the second stage output resistance doesn't change much if 100Ω resistors are connected at the output, so does the closed loop output resistance of the op amp. But by adding 100Ω resistors as said earlier we get protection from output shorting to ground or VDD.

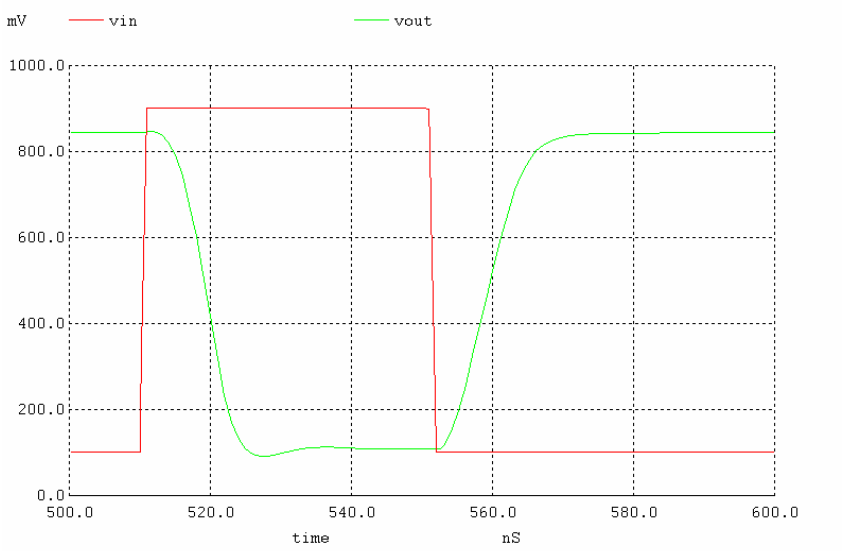
Now to see the how the step response is affected by adding 100Ω resistors we simulate the operation of the op amp in the topology as seen in figure 3 with load resistor and capacitance connected at the output.

The simulation results are shown in next page, **first without 100Ω resistors** and then we again simulate the same circuit but with 100Ω resistors connected as shown in figure 1.

Without 100Ω resistors at the output:



With 100Ω resistors at the output as shown in figure 1:



We can see that output swings only from 100mV to850mV if 100Ω resistors are connected. The drop in swing is due to the voltage drop across the 100Ω resistor.

The SPICE net list is shown below:

“ADDED RESISTORS ARE SHOWN IN BOLD LETTERS “

```
.control
destroy all
run
set units=degrees
plot vin vout
.endc
.option scale=50n
.tran 1n 600n 500n 1n UIC
VDD   VDD   0      DC    1
Vin   Vin   0      DC    0      PULSE 100m 900m   510n 1n 1n 40n
vm    vp    0      DC    0.5
Xopamp      VDD    vout  vp     vm     opamp
Rf    Vout  vm     10k
Rin   Vin   vm     10k
RL    vout  0      1k
CL    vout  0      10p
.subckt opamp VDD vout vp vm
Xbias  VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias
M1B   n2    vm     n8     0      NMOS L=2 W=50
M1T   n6    n4     n2     0      NMOS L=2 W=50
M2B   n3    vp     n8     0      NMOS L=2 W=50
M2T   n1    n4     n3     0      NMOS L=2 W=50
MCM   n4    n4     n8     0      NMOS L=10 W=10
M6T   n8    Vbias3 n12    0      NMOS L=2 W=150
M6B   n12   Vbias4 0      0      NMOS L=2 W=150
M8T   n10   Vbias3 n11    0      NMOS L=2 W=50
M8B   n11   Vbias4 0      0      NMOS L=2 W=50
MFCN  n1    Vncas  n10    0      NMOS L=2 W=25
MON   vnd   n10    0      0      NMOS L=2 W=500
R1    vnd   vout   100
M3B   n6    Vbias2 n5     VDD    PMOS L=2 W=100
M3T   n5    n6     VDD    VDD    PMOS L=2 W=100
M5T   n13   Vbias1 VDD    VDD    PMOS L=2 W=100
M5B   n4    Vbias2 n13    VDD    PMOS L=2 W=100
M4T   n7    n6     VDD    VDD    PMOS L=2 W=100
M4B   n1    Vbias2 n7     VDD    PMOS L=2 W=100
M9T   n9    n6     VDD    VDD    PMOS L=2 W=100
M9B   n1    Vbias2 n9     VDD    PMOS L=2 W=100
MFCP  n10   Vpcas  n1     VDD    PMOS L=2 W=50
MOP   vpd   n1     VDD    VDD    PMOS L=2 W=1000
R2    vpd   vout   100
Cc1   vout  n7     120f
Cc2   vout  n3     120f
.ends
```

Work presented by: Sandeep Pemmaraju

PROBLEM 24.13

Resimulate the OTA in figure24.33 driving a 1pF load capacitance (to determine f_{un}) if K=10.How do the simulation results compare to the hand calculations using Eq. (24.41)? Estimate the parasitic poles associated with the gates of M4 and M5. Are these comparable to f_{un}?

SOLUTION:

The figure for which the followed discussion is related is as shown below:

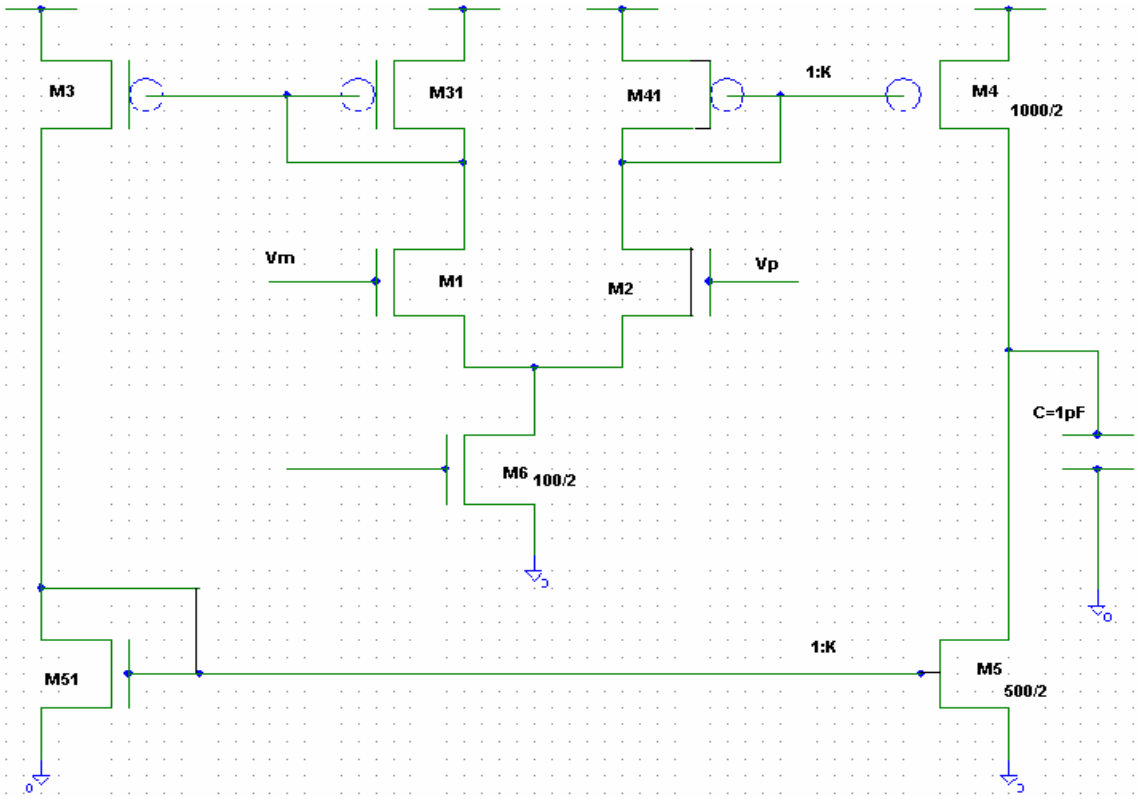


Figure1: Schematic of the OTA with K=10

The transconductance and unity gain frequency expressions for the OTA for the schematic shown above are:

The terminology 1:K in figure determines that M4 and M5 can be sized 'K' times larger than the other MOSFETs in the circuit.

Transconductance of the OTA is given by

$$g_{mOTA} = K.g_m \quad \text{..... (1)}$$

And

$$f_{un} = \frac{K.g_m}{2\pi C_L} \quad \text{.....(2)}$$

Where g_m=transconductance of the normal sized MOSFETS.

To better understand the problem, lets see how the unity gain frequency changes when the factor K is changed form 1 to 10.

Hand calculations and simulations for K=1:

Lets see if our hand calculations match with the above simulated result:

(1) Unity gain frequency- f_{un}:

Taking the values from table 9.2:

$$f_{un} = \frac{K.g_m}{2\pi C_L} = \frac{150uA/V}{2\pi.1pF} = 24MHz$$ Which is pretty close to the simulated value.

(2) 3dB Frequency:

$$f_{3db} = \frac{1}{2\pi(r_{o4} // r_{o5})C_L} = 1.4MHz$$ Which is also the result in the simulation.

(3) Low frequency gain:

$$A = g_m.(r_{o4} // r_{o5}) = 16.65V/V = 24.4dB$$

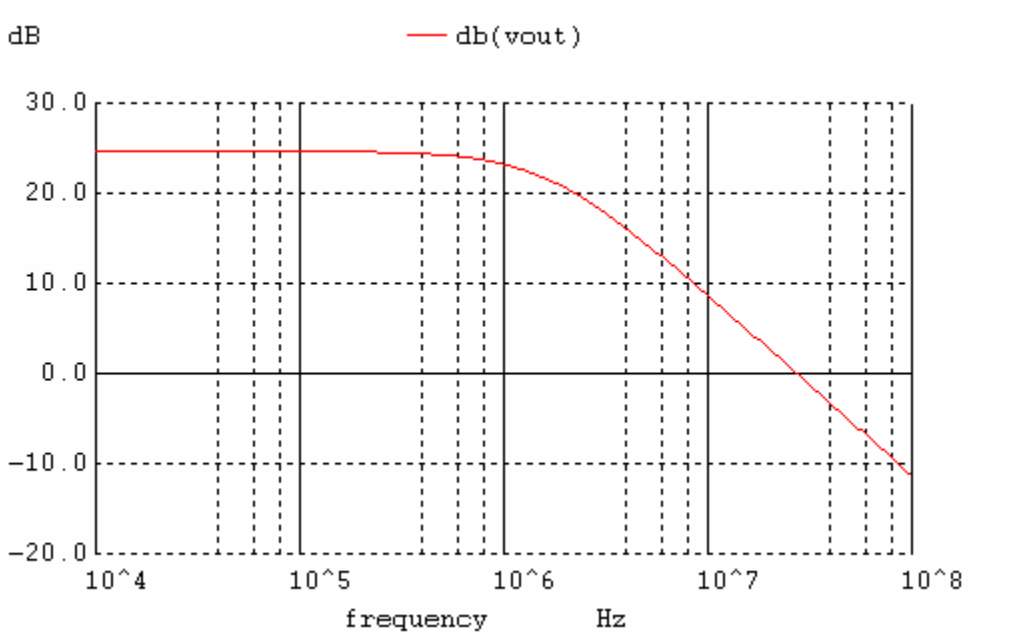


Figure2: Showing the gain response for K=1

Simulations and hand calculations for K=10:

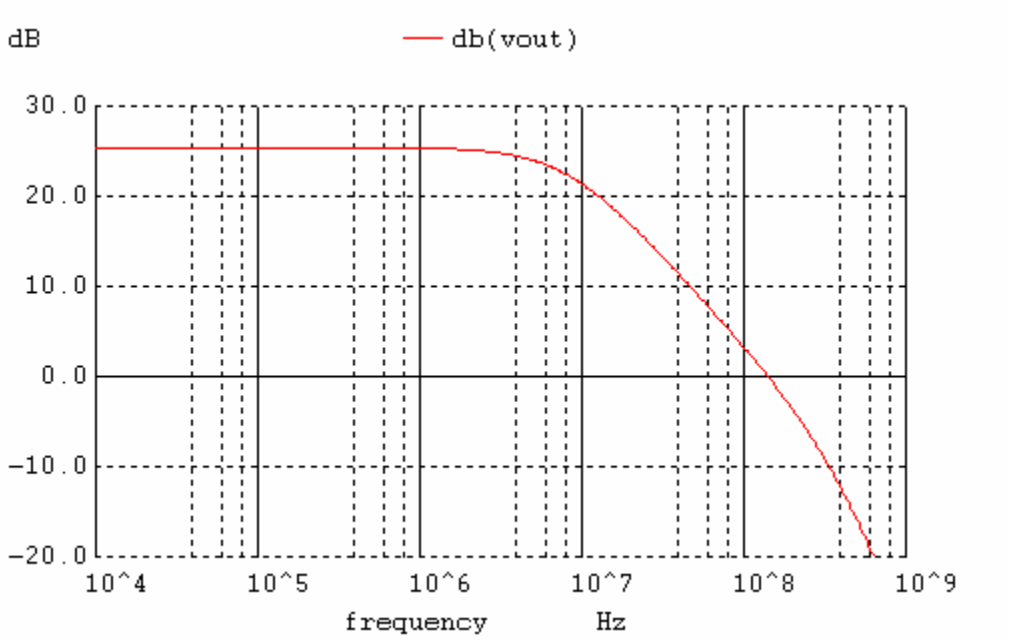


Figure3: Showing the gain response for output MOSFETs sized by a factor of K=10.

Since the output resistance and trans conductance cannot be determined exactly with equations for short channel MOSFETs, we will do some simulations to extract the values of the same for a device with increased width (K=10).

OUTPUT RESISTANCE:

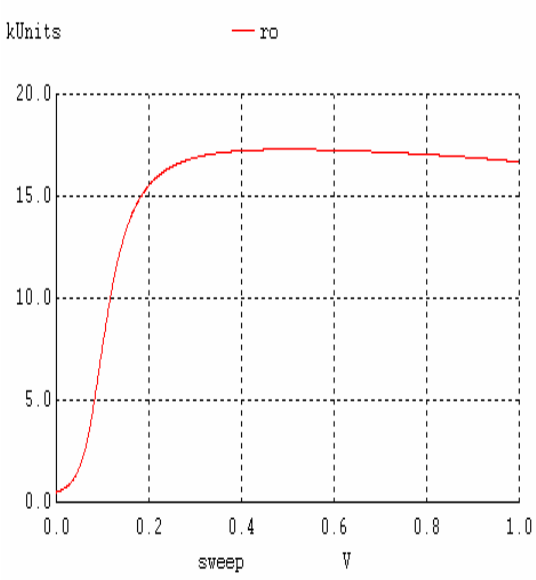


Figure4:Ro for NMOS device 500/2

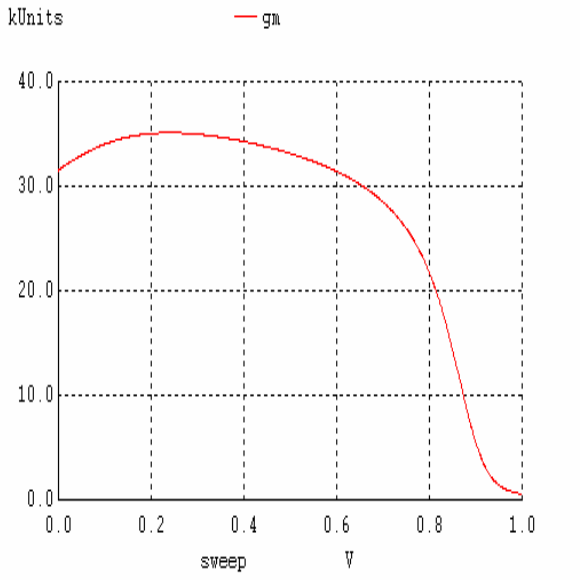


Figure5: Ro for a PMOS device 1000/2

HAND CALCULATIONS:

(1) From equation 24.41 the Trans conductance of the OTA is given by:

$$g_{mOTA} = K.g_m = 10.\ 150uA/V = 1.5mA/V.$$

(2) Unity gain frequency:

$$f_{un} = \frac{K.g_m}{2\pi C_L} = \frac{1500uA/V}{2\pi.1pF} = 240MHz\,.$$

Which is comparable to the simulation results in figure3.To get a more exact match with the simulated value it is advisable to extract g_m of the increased size devices from simulations.

(3) 3-dB Frequency:

$$f_{3db} = \frac{1}{2\pi(r_{o4} // r_{o5})C_L} = \frac{1}{2\pi(17k // 35k).1pF} = 13.9MHz.$$

output resistance values are taken from simulations in figure 4 and 5.

(3) Low frequency gain:

$$A = g_m.(r_{o4} // r_{o5}) = 1500(17k // 35k)V/V = 16.5V/V = 24.34dB$$

This is same as what was obtained for K=1.

So the hand calculations match well with the simulated value.

PART 2:

PARASITIC POLES:

So far we did not pay much attention to the parasitic poles in the circuit. Lets see if they are really important to be considered or not.

Here lets consider the poles associated with the gates o M4 and M5.

The gate of M4 is connected to a gate drain connected MOSFET which is M41.So the resistance of this MOSFET is $1/g_m$. This resistance is in parallel with the gate to source capacitance of M4 (C_{sg}).

So the the pole associated with the gate of M4 is given by:

$$f_{parasiticM4} = \frac{1}{2\pi(1/g_{m41})C_{sg4}}. = \frac{1}{2\pi(1/150uA/V).(8.34*10\,fF)} = 286.2\text{MHz}$$

Here the source to gate capacitance is calculated by multiplying the value in table 9.2 with K=10.

Figure6 clearly shows that at approximately the above specified frequency, the slope of the plot starts to fall at 40dB/dec indicating the presence of the pole.

This pole is very much comparable with the Unity gain frequency (240MHz) and will affect the frequency response of interest.

Lets see if the pole associated with gate of M5 can affect the frequency response:

$$f_{parasiticM4} = \frac{1}{2\pi(1/g_{m51}).C_{gs5}}. = \frac{1}{2\pi(1/150uA/V).(4.17*10\,fF)} = 572.4MHz$$

So the parasitic pole is shown in figure below. At about this frequency, the plot starts to roll off at 60dB/dec which indicates the presence of the second parasitic pole created by M5.
If K is around a 100 then these poles will fall below the unity gain frequency.

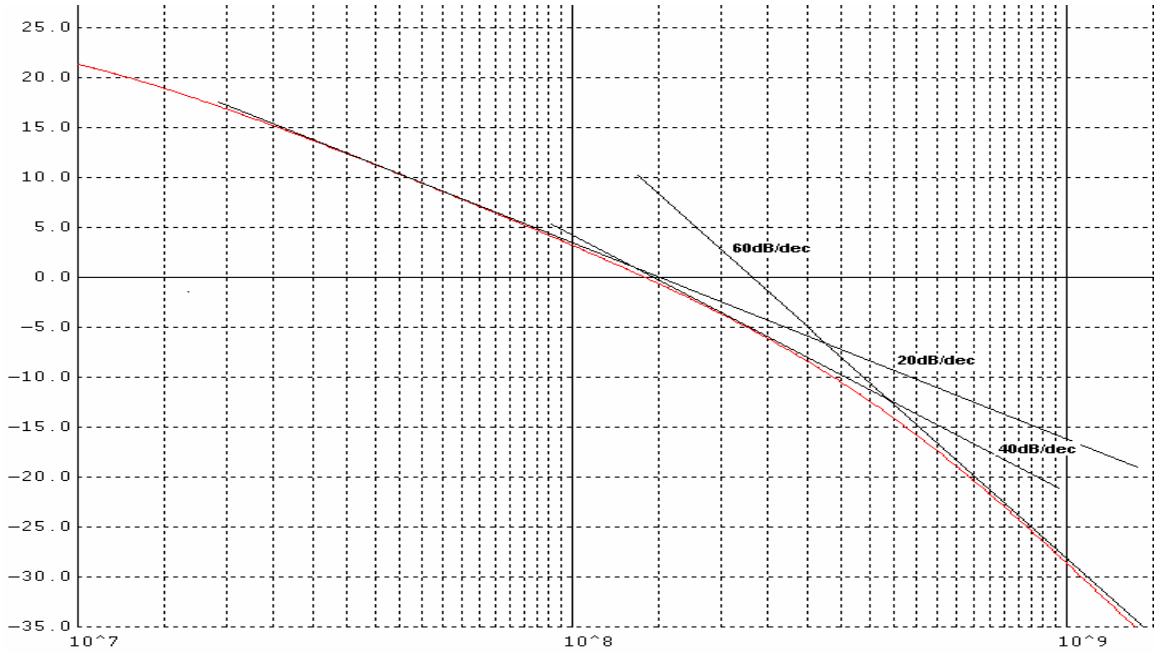


Figure6: Zoomed in view of figure3.
Hand-calculations match with the simulations.

So the bottom line is that as we increase the factor K,the poles associated with the gates of M4 and M5 become comparable to unity gain frequency and can affect the gain response in the frequency of interest region.

NETLIST:

```
.control
destroy all
run
set units=degrees
plot ph(vout)
plot db(vout) xlimit 10k 1g ylimit -20 30
.endc

.option scale=50n ITL1=300 rshunt=1e9
.ac dec 100 1k 10g
*.op

VDD        VDD        0          DC         1
```

```
Vin     Vin     0       DC      0.5     AC      1
Xota    VDD     vout    vin     vm      ota
Rbig    vout    vm      1MEG
Cbig    vm      0       100u
CL      vout    0       1p
.subckt ota VDD vout vp vm

Xbias   VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias
M1      vd1     vm      vss     0       NMOS L=2 W=50
M2      vd2     vp      vss     0       NMOS L=2 W=50
M31     vd1     vd1     VDD     VDD     PMOS L=2 W=100
M3      vd3     vd1     VDD     VDD     PMOS L=2 W=100
M41     vd2     vd2     VDD     VDD     PMOS L=2 W=100
M4      vout    vd2     VDD     VDD     PMOS L=2 W=1000
M51     vd3     vd3     0       0       NMOS L=2 W=50
M5      vout    vd3     0       0       NMOS L=2 W=500
M6      vss     vbias4  0       0       NMOS L=2 W=100
.ends

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1     Vbias3  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP2     Vbias4  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP3     vp1     vp2     VDD     VDD     PMOS L=2 W=100
MP4     vp2     Vbias2  vp1     VDD     PMOS L=2 W=100
MP5     Vpcas   Vpcas   vp2     VDD     PMOS L=2 W=100
MP6     Vbias2  Vbias2  VDD     VDD     PMOS L=10 W=20
MP7     Vhigh   Vbias1  VDD     VDD     PMOS L=2 W=100
MP8     Vbias1  Vbias2  Vhigh   VDD     PMOS L=2 W=100
MP9     vp3     Vbias1  VDD     VDD     PMOS L=2 W=100
MP10    Vncas   Vbias2  vp3     VDD     PMOS L=2 W=100

MN1     Vbias3  Vbias3  0       0       NMOS L=10 W=10
MN2     Vbias4  Vbias3  Vlow    0       NMOS L=2 W=50
MN3     Vlow    Vbias4  0       0       NMOS L=2 W=50
MN4     Vpcas   Vbias3  vn1     0       NMOS L=2 W=50
MN5     vn1     Vbias4  0       0       NMOS L=2 W=50
MN6     Vbias2  Vbias3  vn2     0       NMOS L=2 W=50
MN7     vn2     Vbias4  0       0       NMOS L=2 W=50
MN8     Vbias1  Vbias3  vn3     0       NMOS L=2 W=50
MN9     vn3     Vbias4  0       0       NMOS L=2 W=50
MN10    Vncas   Vncas   vn4     0       NMOS L=2 W=50
MN11    vn4     Vbias3  vn5     0       NMOS L=2 W=50
MN12    vn5     vn4     0       0       NMOS L=2 W=50

MBM1    Vbiasn  Vbiasn  0       0       NMOS L=2 W=50
MBM2    Vreg    Vreg    Vr      0       NMOS L=2 W=200
MBM3    Vbiasn  Vbiasp  VDD     VDD     PMOS L=2 W=100
MBM4    Vreg    Vbiasp  VDD     VDD     PMOS L=2 W=100

Rbias   Vr      0       5.5k

*amplifier
MA1     Vamp    Vreg    0       0       NMOS L=2 W=50
MA2     Vbiasp  Vbiasn  0       0       NMOS L=2 W=50
MA3     Vamp    Vamp    VDD     VDD     PMOS L=2 W=100
MA4     Vbiasp  Vamp    VDD     VDD     PMOS L=2 W=100

MCP     VDD     Vbiasp  VDD     VDD     PMOS L=100 W=100

*start-up stuff
MSU1    Vsur    Vbiasn  0       0       NMOS L=2   W=50
MSU2    Vsur    Vsur    VDD     VDD     PMOS L=20  W=10
MSU3    Vbiasp  Vsur    Vbiasn  0       NMOS L=1   W=10

.ends
```

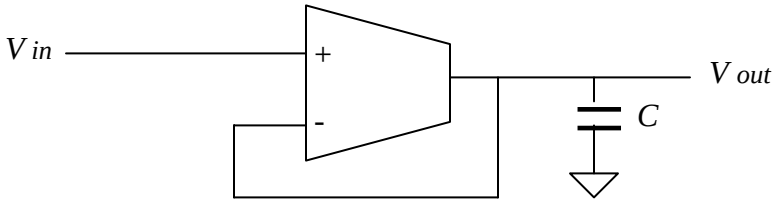
Problem 24.14 Miles Wiscombe

Question:

Using the OTA in fig. 24.35 design a lowpass filter with a 3 dB frequency of 1MHz.

Solution:

Since we are using the OTA as a lowpass filter instead of an amplifier I will connect the circuit in the unity follower configuration shown below.



The first step in the design is to determine the output transfer function of this configuration. We know that the output voltage is equal to the output current times the impedance of the load capacitance.

$$V_{out} = i_{out} * \frac{1}{j\omega C} \quad \text{(Equation 1)}$$

In this configuration i_{out} is mirrored from the dif-amp structure. This causes i_{out} to equal g_m * (Vplus – Vminus). In the unity follower configuration this corresponds to the following equation.

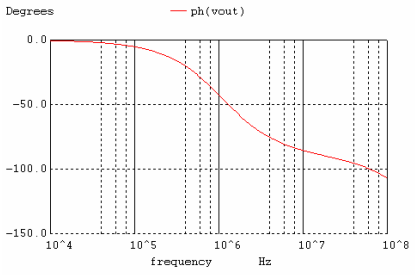
$$g_m * (V_{in} - V_{out}) \text{ (Equation 2)}$$

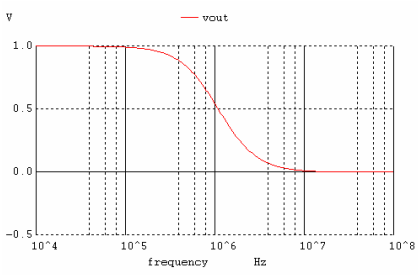
Plugging in equation 2 for i_{out} the transfer function can be simplified to the following equation.

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + j\omega(C * \frac{1}{g_m})} \quad \text{(Equation 3)}$$

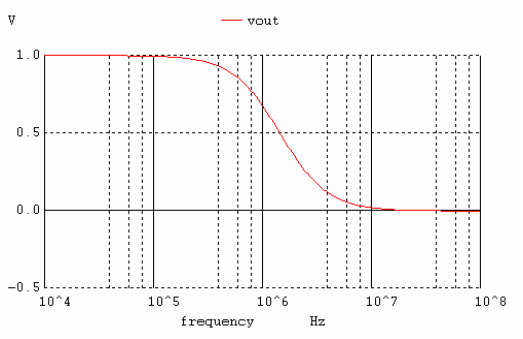
From equation 3, the 3 dB frequency is equal to $\frac{1}{2\pi(C * \frac{1}{g_m})}$.

When this is set to 1MHz and the g_m value in table 9.2 (since we are designing using these sizes) of 150 uA/V is used we can solve for C. Doing so, we receive a value of 23.87pF. The following plots are the simulation results for figure 24.35 in the unity follower configuration (diagram1) with a load capacitance of 23.87 pF.





The above plot of Vout shows that the output is at about 550 mV at 1MHz. The equation got us very close but in order to fine tune our design, simulations must be ran to more closely reach a value of 707 mV (3 dB down) at 1MHz. By adjusting the capacitance value to 18 pF we closely match the 3dB frequency of 1MHz specification. The following plot shows this situation.



Netlist:

```
*** Problem 24.14 ***
.control
destroy all
run
set units=degrees
plot ph(vout)
plot db(vout)
.endc

.option scale=50n ITL1=300
.ac dec 100 10k 100MEG

VDD     VDD     0       DC      1
Vin     Vin     0       DC      0.5     AC      1

Xo      VDD     vout    vin     vout    ota

CL      vout    0       18p

.subckt ota VDD vout vp vm

Xbias   VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias
M1      vd1     vm      vss     0       NMOS L=2 W=50
M2      vd2     vp      vss     0       NMOS L=2 W=50
M31t    vd31t   vd1     VDD     VDD     PMOS L=2 W=100
M31b    vd1     Vbias2  vd31t   VDD     PMOS L=2 W=100
M3t     vd3t    vd1     VDD     VDD     PMOS L=2 W=100
M3b     vd3b    Vbias2  vd3t    VDD     PMOS L=2 W=100
M51t    vd3b    vbias3  vd51b   0       NMOS L=2 W=50
M51b    vd51b   vd3b    0       0       NMOS L=2 W=50
M41t    vd41t   vd2     VDD     VDD     PMOS L=2 W=100
M41b    vd2     vbias2  vd41t   VDD     PMOS L=2 W=100
M4t     vd4t    vd2     VDD     VDD     PMOS L=2 W=100
M4b     vout    vbias2  vd4t    VDD     PMOS L=2 W=100
M5t     vout    vbias3  vd5b    0       NMOS L=2 W=50
M5b     vd5b    vd3b    0       0       NMOS L=2 W=50
M6tr    vss     vbias3  vd6br   0       NMOS L=2 W=50
M6br    vd6br   vbias4  0       0       NMOS L=2 W=50
M6tl    vss     vbias3  vd6bl   0       NMOS L=2 W=50
M6bl    vd6bl   vbias4  0       0       NMOS L=2 W=50
.ends

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1     Vbias3  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP2     Vbias4  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP3     vp1     vp2     VDD     VDD     PMOS L=2 W=100
MP4     vp2     Vbias2  vp1     VDD     PMOS L=2 W=100
MP5     Vpcas   Vpcas   vp2     VDD     PMOS L=2 W=100
MP6     Vbias2  Vbias2  VDD     VDD     PMOS L=10 W=20
MP7     Vhigh   Vbias1  VDD     VDD     PMOS L=2 W=100
MP8     Vbias1  Vbias2  Vhigh   VDD     PMOS L=2 W=100
MP9     vp3     Vbias1  VDD     VDD     PMOS L=2 W=100
MP10    Vncas   Vbias2  vp3     VDD     PMOS L=2 W=100

MN1     Vbias3  Vbias3  0       0       NMOS L=10 W=10
MN2     Vbias4  Vbias3  Vlow    0       NMOS L=2 W=50
MN3     Vlow    Vbias4  0       0       NMOS L=2 W=50
MN4     Vpcas   Vbias3  vn1     0       NMOS L=2 W=50
MN5     vn1     Vbias4  0       0       NMOS L=2 W=50
MN6     Vbias2  Vbias3  vn2     0       NMOS L=2 W=50
MN7     vn2     Vbias4  0       0       NMOS L=2 W=50
MN8     Vbias1  Vbias3  vn3     0       NMOS L=2 W=50
```

```
MN9         vn3         Vbias4      0           0           NMOS L=2 W=50
MN10        Vncas       Vncas       vn4         0           NMOS L=2 W=50
MN11        vn4         Vbias3      vn5         0           NMOS L=2 W=50
MN12        vn5         vn4         0           0           NMOS L=2 W=50

MBM1        Vbiasn      Vbiasn      0           0           NMOS L=2 W=50
MBM2        Vreg        Vreg        Vr          0           NMOS L=2 W=200
MBM3        Vbiasn      Vbiasp      VDD         VDD         PMOS L=2 W=100
MBM4        Vreg        Vbiasp      VDD         VDD         PMOS L=2 W=100

Rbias       Vr          0           5.5k

*amplifier
MA1         Vamp        Vreg        0           0           NMOS L=2 W=50
MA2         Vbiasp      Vbiasn      0           0           NMOS L=2 W=50
MA3         Vamp        Vamp        VDD         VDD         PMOS L=2 W=100
MA4         Vbiasp      Vamp        VDD         VDD         PMOS L=2 W=100

MCP         VDD         Vbiasp      VDD         VDD         PMOS L=100 W=100

*start-up stuff
MSU1        Vsur        Vbiasn      0           0           NMOS L=2   W=50
MSU2        Vsur        Vsur        VDD         VDD         PMOS L=20  W=10
MSU3        Vbiasp      Vsur        Vbiasn      0           NMOS L=1   W=10

.ends
```

Problem 24.15 Solution by Robert J. Hanson, CNS

Let's begin the solution by calculating (by hand) the gain of each stage in the Cascode OTA circuit with common-source output buffer given in Figure 24.37. Then we will simulate the circuit in Figure 24.37 with M8T in the circuit and compare the results with that of the hand calculations, and with the results when M8T is removed from the circuit:

(The mathematical formulas and results below are copied from MATHCAD)

1.) Calculating the gain of the first stage A1, using the values listed in Table 9.2:

$gmn1 := 150.0 \cdot 10^{-6}$

$gmp1 := 150.0 \cdot 10^{-6}$

$ron1 := 167 \cdot 10^{3}$

$rop1 := 333 \cdot 10^{3}$

$Rocasn1 := gmn1 \cdot ron1^{2}$

$Rocasp1 := gmp1 \cdot rop1^{2}$

$Rocasn1 = 4.183 \cdot 10^{6}$

$Rocasp1 = 1.663 \cdot 10^{7}$

$$Ro1 := \frac{1}{\frac{1}{Rocasn1} + \frac{1}{Rocasp1}}$$

$Ro1 = 3.343 \cdot 10^{6}$

$A1 := gmn1 \cdot Ro1$

$A1 = 501.399$

2.) Calculating the gain (V/V) of the second stage A2OLD, with **M8T IN the circuit**. Note that gmn and gmp are 10x larger here and ron and rop are 10x smaller due to the 10x increase in W compared to the values listed in Table 9.2, also calculating the total low frequency gain AtotOLD:

$gmn2 := 1500 \cdot 10^{-6}$

$gmp2 := 1500 \cdot 10^{-6}$

$ron2 := 16.7 \cdot 10^{3}$

$rop2 := 33.3 \cdot 10^{3}$

$Rocasn2 := gmn2 \cdot ron2^{2}$

$Rocasn2 = 4.183 \cdot 10^{5}$

$$RoutOLD := \frac{1}{\frac{1}{rop2} + \frac{1}{Rocasn2}}$$

$RoutOLD = 3.084 \cdot 10^{4}$

$A2OLD := gmn2 \cdot RoutOLD$

$A2OLD = 46.267$

$AtotOLD := A1 \cdot A2OLD$

$AtotOLD = 2.32 \cdot 10^{4}$

3.) Calculating the gain (V/V) of the second stage A2NEW and the total low frequency gain AtotNEW, with **M8T REMOVED from the circuit**:

$$RoutNEW := \frac{1}{\frac{1}{rop2} + \frac{1}{ron2}}$$

$RoutNEW = 1.112 \cdot 10^4$

$A2NEW := gmn2 \cdot RoutNEW$

$A2NEW = 16.683$

$AtotNEW := A1 \cdot A2NEW$

$AtotNEW = 8.365 \cdot 10^3$

4.) Calculating the total low frequency gains in dB with **M8T in and out of the circuit**:

$GainOLD := 20 \cdot \log(AtotOLD)$ (OLD = with M8T in the circuit)

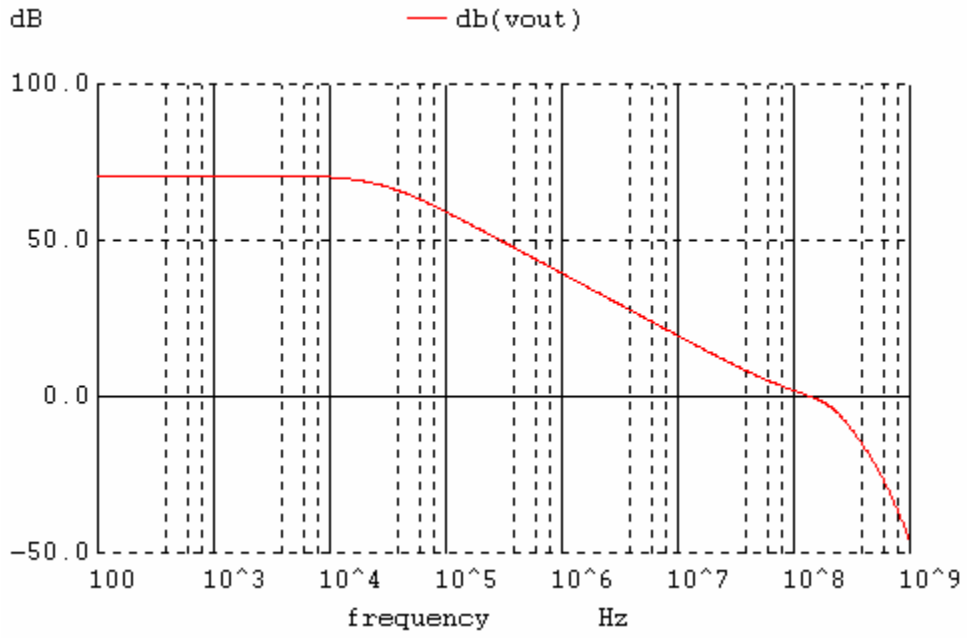
$GainNEW := 20 \cdot \log(AtotNEW)$ (NEW = with M8T removed from the circuit)

$GainOLD = 87.309$

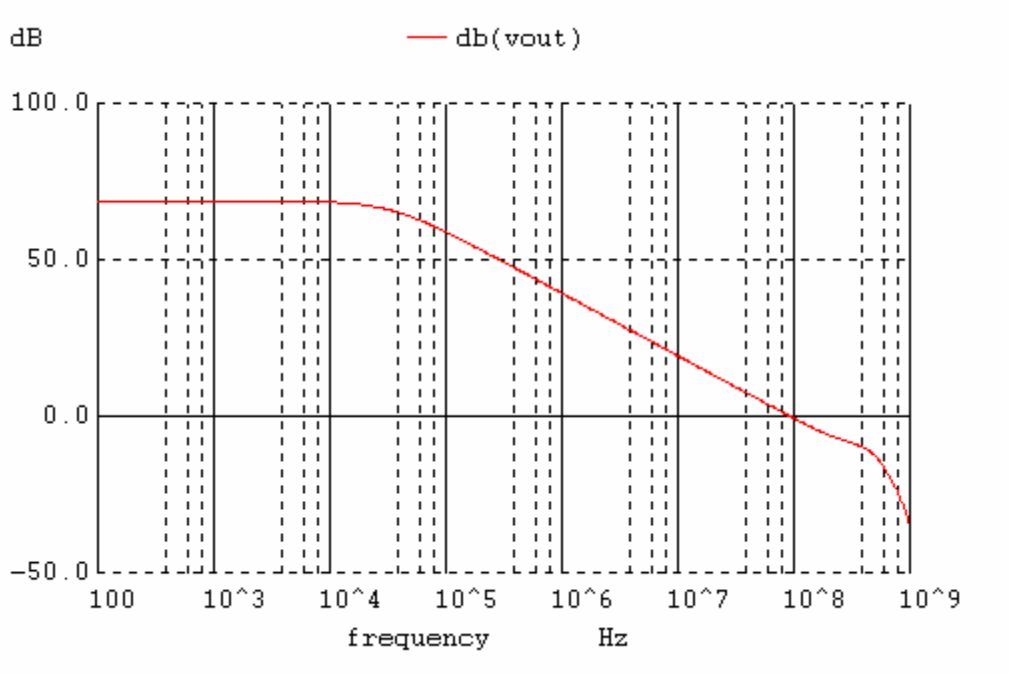
$GainNEW = 78.449$

4.) **Important point:** Notice that with M8T removed from the circuit the output resistance of the second stage changes from approximately rop2 (33.3k) to about 11.1k. This is because the output resistance when M8T is removed is just ron2 and rop2 in parallel. And, since ron2 is half of rop2, it follows that the resistance becomes 1/3* rop2

5.) Now let's compare the hand calculations with SPICE simulations using BSIM4 50nm design rules. First, the graph below shows the open loop gain of the circuit in Figure 24.37 with M8T in the circuit, the low frequency gain is about 70.7dB:



6.) Removing MOSFET M8T from the circuit and the output shorted to the drain of M8B results in the following simulation results where the low frequency gain is about 68.8 dB.



7.) The table below shows a direct comparison between the calculated and simulated results:

	M8T in Circuit	M8T Removed
Hand Calculation (dB)	87.3	78.4
Simulation (dB)	70.7	68.8
Hand Calculation (V/V)	23200	8365
Simulation (V/V)	3427	2754

As a rough estimate based on the note in #4, we can estimate the change in the gain using the following:

GainNEW = GainOLD/3 (V/V)

In dB form becomes: 20*log(GainNew) = 20*log(GainOLD) - 20log(3)
Therefore, the gain difference is merely approximated as 20*log(GainNew) = 20*log(GainOLD) - 9.5dB**. In other words, the gain should decrease by about 9.5dB when M8T is removed.**

The discrepancy between the simulation and hand-calculation results is because the values used in the hand calculations are only approximations, due to differences in device sizing and biasing. This solution does, however, illustrate how the gain of the circuit in figure 24.37 is degraded, due to the decrease in the stage-2 output resistance when MOSFET M8T is removed from the circuit.

The SPICE NetList used for generating the simulations with M8T removed is provided below for reference (the BSIM4 Level 14 parameters and biasing circuitry can be downloaded from CMOSEDU.COM and are omitted to save space):

```
*** Figure 24.37 with MOSFET M8T removed from the circuit ***
.control
destroy all
run
set units=degrees
plot ph(vout)
plot db(vout)
.endc
.option scale=50n ITL1=300 rshunt=1e9
.ac dec 100 100 1G

VDD     VDD     0       DC      1
Vin     Vin     0       DC      0.5     AC      1
Xo      VDD     vout    vin     vm      opamp
Rbig    vout    vm      10MEG
Cbig    vm      0       10u
*CL     vout    0       1p

.subckt opamp VDD vout vp vm

Xbias   VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias
M1      vd1     vp      vss     0       NMOS L=2 W=50
M2      vd2     vm      vss     0       NMOS L=2 W=50
M31t    vd31t   vd1     VDD     VDD     PMOS L=2 W=100
M31b    vd1     Vbias2  vd31t   VDD     PMOS L=2 W=100
M3t     vd3t    vd1     VDD     VDD     PMOS L=2 W=100
M3b     vd3b    Vbias2  vd3t    VDD     PMOS L=2 W=100
M51t    vd3b    vbias3  vd51b   0       NMOS L=2 W=50
M51b    vd51b   vd3b    0       0       NMOS L=2 W=50
M41t    vd41t   vd2     VDD     VDD     PMOS L=2 W=100
M41b    vd2     vbias2  vd41t   VDD     PMOS L=2 W=100
M4t     vd4t    vd2     VDD     VDD     PMOS L=2 W=100
M4b     vout1   vbias2  vd4t    VDD     PMOS L=2 W=100
M5t     vout1   vbias3  vd5b    0       NMOS L=2 W=50
M5b     vd5b    vd3b    0       0       NMOS L=2 W=50
M6tr    vss     vbias3  vd6br   0       NMOS L=2 W=50
M6br    vd6br   vbias4  0       0       NMOS L=2 W=50
M6tl    vss     vbias3  vd6bl   0       NMOS L=2 W=50
M6bl    vd6bl   vbias4  0       0       NMOS L=2 W=50
M7      Vout    Vout1   VDD     VDD     PMOS L=2 W=1000
*M8t    Vout    vbias3  vd8b    0       NMOS L=2 W=500
M8b     Vout    vbias4  0       0       NMOS L=2 W=500
Cc      Vout    vd5b    240f
.ends
```

Aaron Johnson
EE511

Problem 24.16

Problem Statement

Suppose, to simulate the open-loop gain of an OTA, the big resistor and capacitor used in Fig. 24.43 are removed and the inverting input is connected to 500mV. Will this work? Why or why not? What happens if the OTA doesn't have an offset voltage? Will it work then?

Simulations

The configuration change is shown in Figure 1 below.

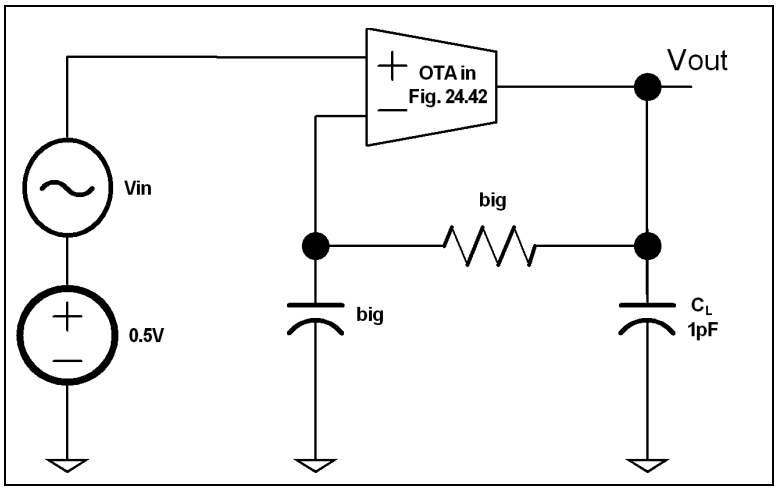


Figure 1: OTA configuration as seen in Figure 24.43 in the book.

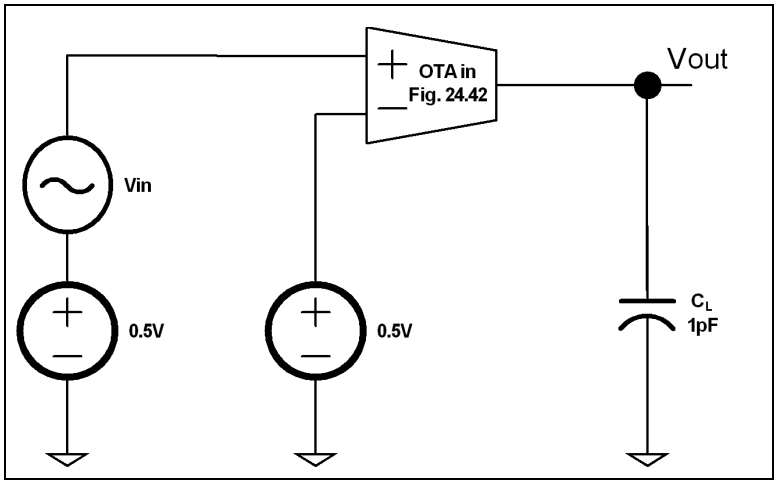


Figure 2: New OTA configuration for problem 24.16.

The first step to determine if the configuration works is to simulate the new circuit and compare it to the old circuit. The netlist can be seen at the end of the problem. The first simulation will look at

the case where there is NO offset. Upon simulation of the circuits shown in figures 1 and 2, the plots in figures 3 and 4, respectively, were obtained.

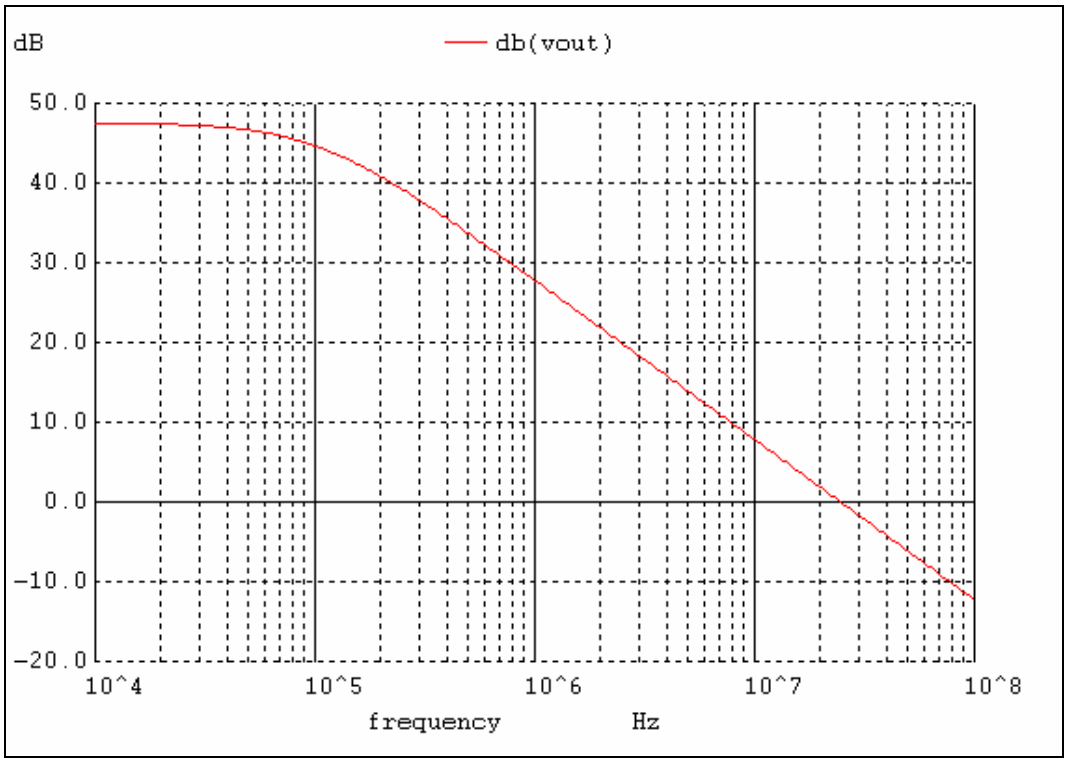


Figure 3: Plot of the output of the circuit in figure 24.43 showing the open loop gain of 47.5dB.

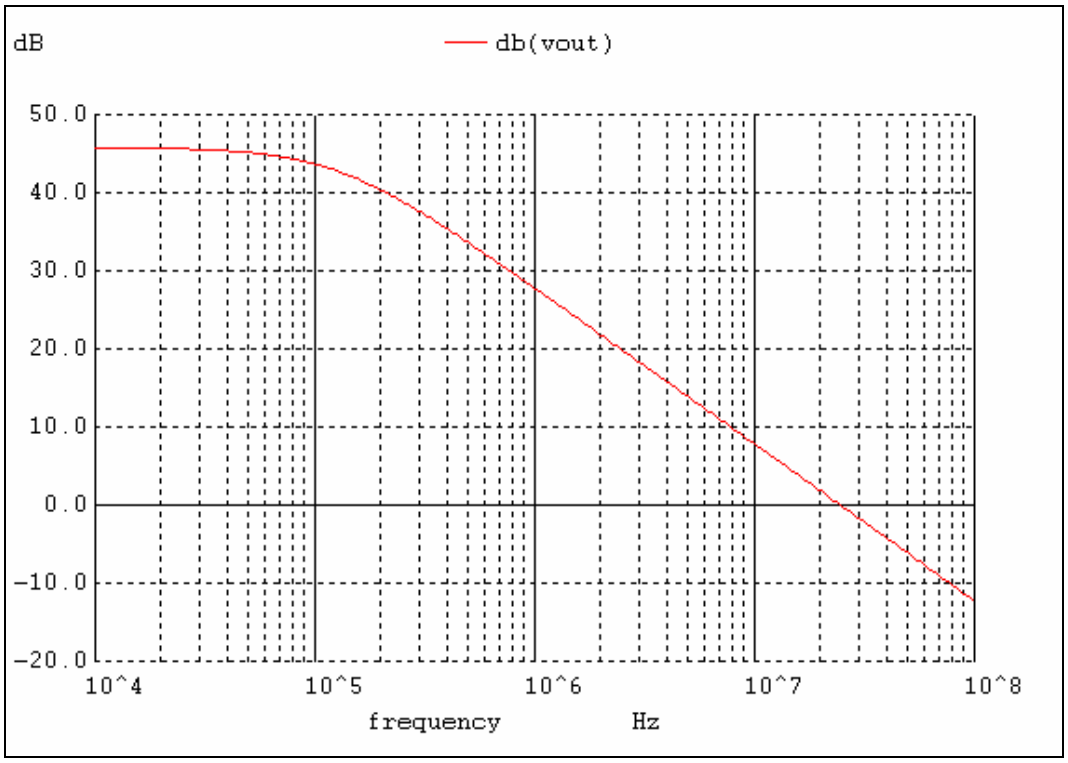


Figure 4: Plot of the output of the circuit for problem 24.16 showing the open loop gain of 46dB.

After looking at the plots in figures 3 and 4, it can be seen that the response is basically the same and therefore **the circuit can be used to simulate the open loop gain for the case when there is not an offset**.

The next step is to see if the circuit will work with an offset. As discussed in the book, there are various ways an offset may be introduced. The first way of introducing an offset will be to add a voltage source, V_{OS} = 10mV, in series with the sources in the noninverting input in figure 2. When this was done, the plot in figure 5 was produced. The figure shows that by adding 10mV of offset, the gain was decreased by 29dB. When V_{OS} was increased even further, the gain decreased even more.

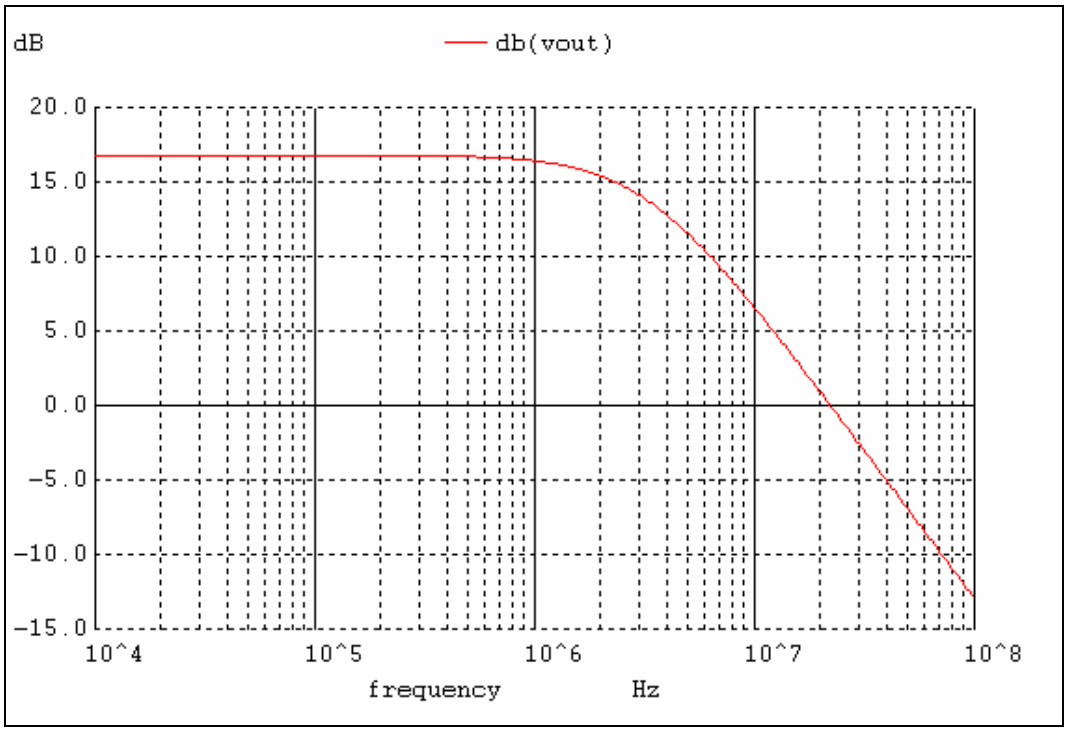


Figure 5: Plot showing how an offset voltage affects the open loop gain (17dB instead of 46dB) for the circuit shown in figure 2.

In the next example, we will introduce a systematic offset. The widths of the transistors in the current source on the output branch, namely M10, and M12 will be increased by 5% or 52.5um drawn. By increasing these widths, the transistors will want to sink 105% the normal current or 10.5 uA. When this was done, the plot in figure 6 was produced. The figure shows that this modification decreases the gain by 19dB. Similarly as before, when the widths were increased even more the gain dropped more. (In fact, when doubling the width, the gain went to –4dB, thus attenuating the signal.)

An offset was introduced to the original circuit (figure 1) by doubling the widths of M10 and M12, making those transistors wanting to sink 20 uA. Upon doing this, the gain dropped just slightly to 44 dB.

So, this circuit configuration can not be used to simulate the open loop gain for the case when there is an offset.

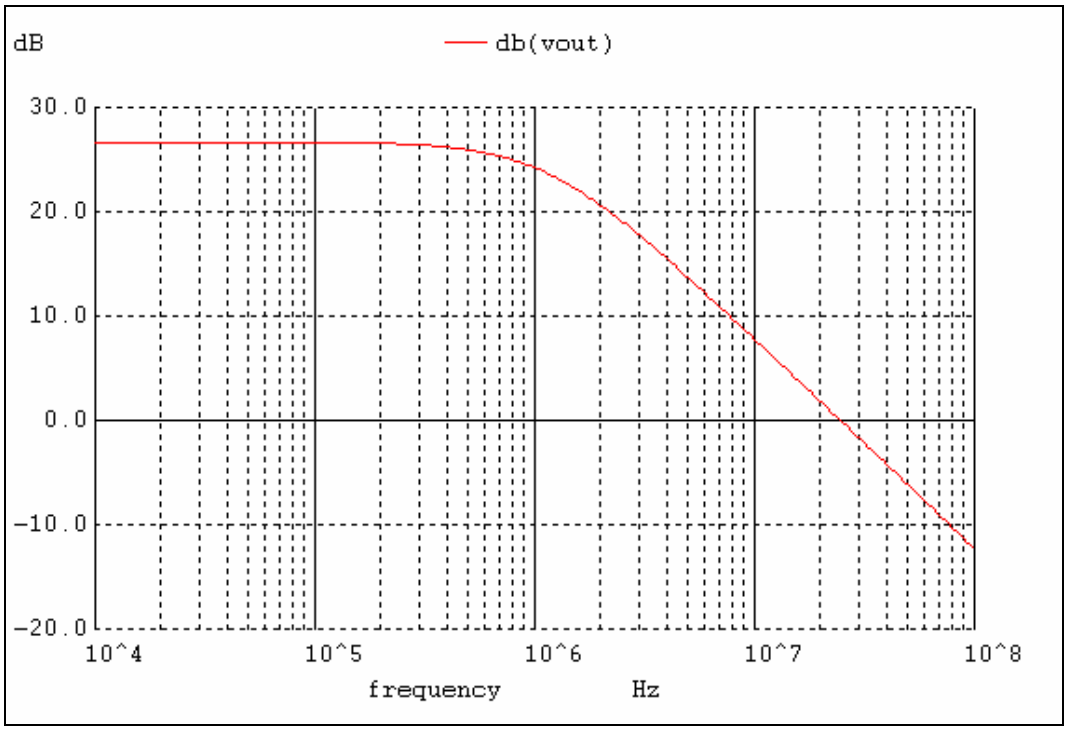


Figure 6: Plot showing how a 5% transistor width increase affects the open loop gain (27dB instead of 46dB) for the circuit shown in figure 2.

Discussion

The circuit configuration seen in figure 2, is not a good circuit to use to find the open loop gain. The circuit's simulated gain changes dramatically with a small offset. As discussed in the book, there are unavoidable offsets such as process shifts and matching that cannot be avoided, so this configuration would never give an accurate gain.

The circuit in figure 2 does not have any feedback, however, the circuit in figure 1 does have feedback at DC (The resistor is basically a short at DC because there is no current flowing). This allows the Vm node to be regulated, which is why this configuration is a better choice.

Netlist with some comments for Problem 24.16

```
*** Problem 24.16 CMOS: Circuit Design, Layout, and Simulation ***

.control
destroy all
run
set units=degrees
plot db(vout)
.endc

.option scale=50n ITL1=300 rshunt=1e9
.ac dec 100 10k 100MEG

VDD      VDD      0        DC       1
Vin      Vp       0        DC       0.5      AC       1
* To add VOS just increase Vin's DC value by 10mV.
Vin2     Vm       0        DC       0.5

Xota     VDD      vout     vp       vm       fota
CL       vout     0        1p

.subckt fota VDD vout vp vm

Xbias    VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias
M1       vd1      vp       vss      0        NMOS L=2 W=50
M2       Vd2      vm       vss      0        NMOS L=2 W=50
M3LT     vss      vbias3   vd3lb    0        NMOS L=2 W=50
M3LB     vd3lb    vbias4   0        0        NMOS L=2 W=50
M3RT     vss      vbias3   vd3rb    0        NMOS L=2 W=50
M3RB     vd3rb    vbias4   0        0        NMOS L=2 W=50

M5L      vd1      vd7      VDD      VDD      PMOS L=2 W=100
M5R      vd1      vd7      VDD      VDD      PMOS L=2 W=100
M7       vd7      vbias2   vd1      VDD      PMOS L=2 W=100
M9       vd7      vbias3   vd11     0        NMOS L=2 W=50
M11      vd11     vbias4   0        0        NMOS L=2 W=50

M6L      vd2      vd7      VDD      VDD      PMOS L=2 W=100
M6R      vd2      vd7      VDD      VDD      PMOS L=2 W=100
M8       vout     vbias2   vd2      VDD      PMOS L=2 W=100
M10      vout     vbias3   vd12     0        NMOS L=2 W=50
M12      vd12     vbias4   0        0        NMOS L=2 W=50
* To see the systematic offset, just change the widths of M10 and M12 to 52.5.
.ends

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1      Vbias3   Vbiasp   VDD      VDD      PMOS L=2 W=100
MP2      Vbias4   Vbiasp   VDD      VDD      PMOS L=2 W=100
MP3      vp1      vp2      VDD      VDD      PMOS L=2 W=100
MP4      vp2      Vbias2   vp1      VDD      PMOS L=2 W=100
MP5      Vpcas    Vpcas    vp2      VDD      PMOS L=2 W=100
MP6      Vbias2   Vbias2   VDD      VDD      PMOS L=10 W=20
MP7      Vhigh    Vbias1   VDD      VDD      PMOS L=2 W=100
MP8      Vbias1   Vbias2   Vhigh    VDD      PMOS L=2 W=100
MP9      vp3      Vbias1   VDD      VDD      PMOS L=2 W=100
MP10     Vncas    Vbias2   vp3      VDD      PMOS L=2 W=100
MN1      Vbias3   Vbias3   0        0        NMOS L=10 W=10
MN2      Vbias4   Vbias3   Vlow     0        NMOS L=2 W=50
MN3      Vlow     Vbias4   0        0        NMOS L=2 W=50
MN4      Vpcas    Vbias3   vn1      0        NMOS L=2 W=50
MN5      vn1      Vbias4   0        0        NMOS L=2 W=50
MN6      Vbias2   Vbias3   vn2      0        NMOS L=2 W=50
MN7      vn2      Vbias4   0        0        NMOS L=2 W=50
MN8      Vbias1   Vbias3   vn3      0        NMOS L=2 W=50
MN9      vn3      Vbias4   0        0        NMOS L=2 W=50
MN10     Vncas    Vncas    vn4      0        NMOS L=2 W=50
MN11     vn4      Vbias3   vn5      0        NMOS L=2 W=50
MN12     vn5      vn4      0        0        NMOS L=2 W=50
MBM1     Vbiasn   Vbiasn   0        0        NMOS L=2 W=50
MBM2     Vreg     Vreg     Vr       0        NMOS L=2 W=200
MBM3     Vbiasn   Vbiasp   VDD      VDD      PMOS L=2 W=100
MBM4     Vreg     Vbiasp   VDD      VDD      PMOS L=2 W=100
Rbias    Vr       0        5.5k
*amplifier
MA1      Vamp     Vreg     0        0        NMOS L=2 W=50
MA2      Vbiasp   Vbiasn   0        0        NMOS L=2 W=50
MA3      Vamp     Vamp     VDD      VDD      PMOS L=2 W=100
MA4      Vbiasp   Vamp     VDD      VDD      PMOS L=2 W=100
MCP      VDD      Vbiasp   VDD      VDD      PMOS L=100 W=100
*start-up stuff
MSU1     Vsur     Vbiasn   0        0        NMOS L=2   W=50
MSU2     Vsur     Vsur     VDD      VDD      PMOS L=20  W=10
MSU3     Vbiasp   Vsur     Vbiasn   0        NMOS L=1   W=10

.ends
```

Problem 21.17
Qawi Harvard
Boise State University

Why is the non-inverting topology (Fig. 24.49) inherently faster than the inverting topology (Fig. 29.39)? What are the feedback factors, β, for each topology? Use the op-amp in Fig. 24.48 to compare the settling times for a +1 and a -1 amplifier driving 10pF.

A hint to the solution is given in the problem statement. Begin this problem by analyzing the non-inverting and inverting topologies given below in figure 1.

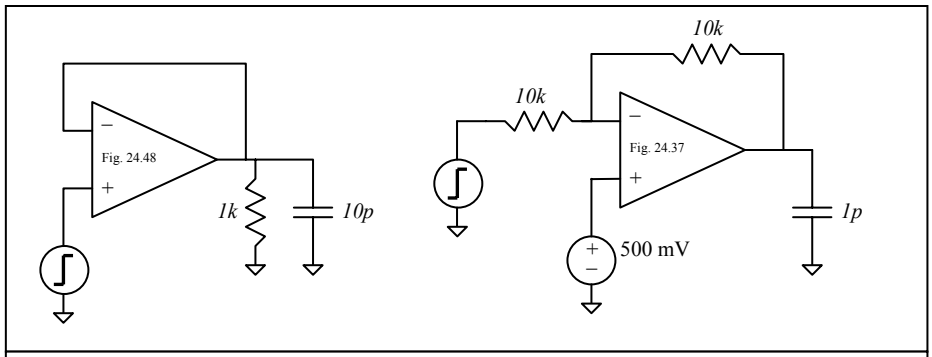


Figure 1 Non-inverting (left) and inverting (right) topologies

The feedback factor represents the amount of output that is feedback to the input of the op-amp. The non-inverting topology seen at the left of figure 1 shows that the output is directly feedback to the input of the op-amp and therefore has a $\beta = 1$. To determine the feedback factor of the inverting topology, it is easiest to note the voltage divider that is obtained when the input voltage is zero. When the input is low the output is high and the voltage on the inverting terminal of the op-amp is $0.5v_{out}$. After realizing this voltage divider, it is clear to see that $\beta = 0.5$ for the inverting configuration seen in figure 1. The topologies that are analyzed for this problem are in the closed loop form therefore the closed loop gain must be calculated.

$$A_{CL}(f) = \frac{A_{OL}(f)}{1 + \beta A_{OL}(f)}$$

Assuming that the op-amp is compensated correctly the open loop frequency response of the amplifier can be approximated to be:

$$A_{OL}(j\omega) = \frac{A_{OLDC}}{1 + \dfrac{j\omega}{\omega_{3dB}}}$$

where the frequency response of the op-amp behaves as if there is a single low frequency pole at ω_{3dB}. Using the two equations above determine the frequency response of the closed loop gain.

$$A_{CL}(j\omega) = \frac{A_{OLDC}}{1 + \frac{j\omega}{\omega_{3dB}} + \beta A_{OLDC}} = \frac{\omega_{3dB} A_{OLDC}}{s + \omega_{3dB}(1 + \beta A_{OLDC})} = \frac{A_{OLDC}}{1 + \beta A_{OLDC}} \cdot \frac{1}{1 + \frac{j\omega}{\omega_{3dB}(1 + \beta A_{OLDC})}}$$

Analyze this equation to be sure that it is understood. The closed loop frequency response is determined by the feedback factor, bandwidth, and open loop gain of the op-amp. For the non-inverting topology with β =1 the DC (closed loop) gain is approximately 1 and the bandwidth increases (the op-amp reacts faster). The inverting topology has a larger DC gain and a smaller bandwidth (slower). This is why the inverting configuration behaves slower than the non-inverting configuration. Another intuitive analysis is to realize that the non-inverting configuration has both inputs of the op-amp being driven, while the inverting configuration has only one input node driven, this will result in slower operation of the op-amp.

When placing op-amps into closed loop configurations this effect (known as Bandwidth Extension/Reduction) must be taken into consideration. When an op-amp is placed into a closed loop topology the following analogy can be made: As β increases the gain goes down and the bandwidth ($\omega_{3dB} = 2\pi f_{3dB}$) goes up, as β decreases the gain goes up and the bandwidth goes down.

To analyze the performance of the op-amp in figure 24.48 in a plus 1 and minus 1 configuration use the two topologies in figure one. Figure 2 shows the simulation results of step responses of the op-amp.

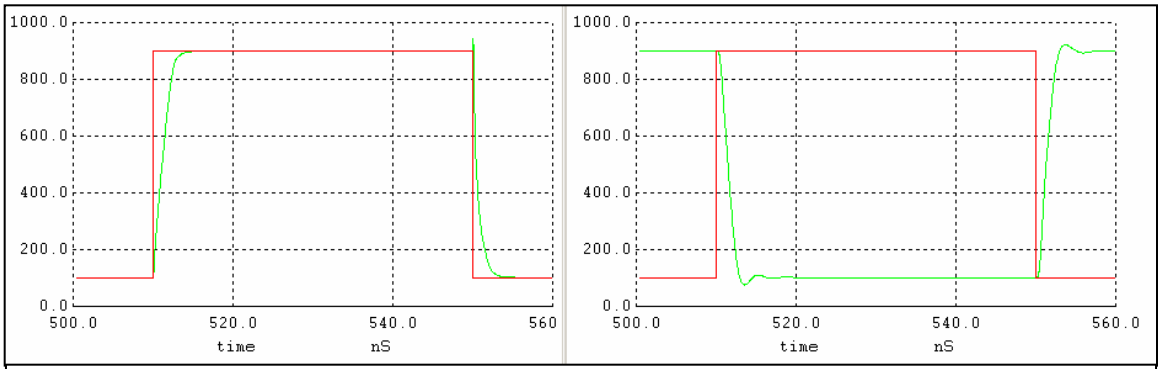
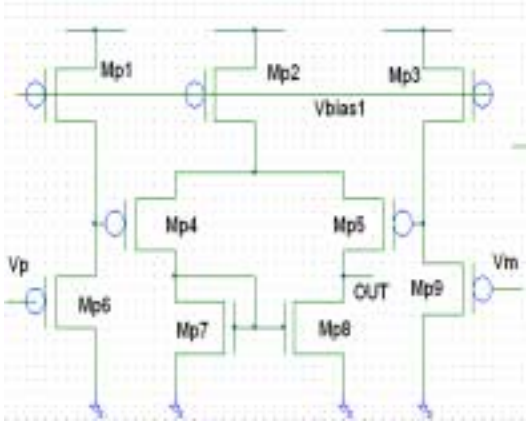
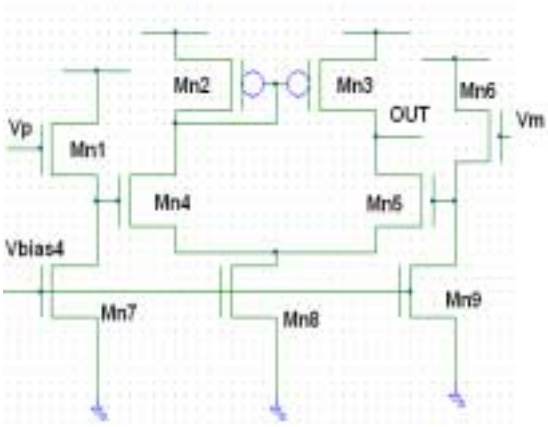


Figure 2 Simulation results of the op-amp in Fig. 24.28 in a +1 and -1 gain configuration

Figure 2 shows that the settling times of both configurations. The load capacitance was 10pF, and $R_1 = R_2 = 10k$. The settling time of the non-inverting configuration is less than that of the inverting configuration.

Problem 24.18 Submitted by: S. Sandhya Reddy





P Diff Amp **N Diff Amp**

Fig 24.50 Diff Amps with source-follower level shifters for use in GE

DC ANALYSIS:

With the lengths of current source/sink MOSFETs Mp1-3 and Mn7-9 increased from 2u to 10u, the V_{SG}/V_{GS} of the amplifying device will change (infact decrease). The current that flows with L=2 devices is 10uA.

Now when the lengths of the above mentioned devices are increased the current that flows through Mp1, Mp3 in PMOS DIFF AMP and Mn7, Mn9 in NMOS DIFF AMP are both equal to 7.8u (this was found with a '. OP' statement). The figure below shows the I_D-V_{GS} plots of a L=2 device. The V_{GS} value corresponding to 7.8uA current can be extracted from the graphs shown below and they turn up to be 320mV both for NMOS and PMOS (from the Sims fig 2).

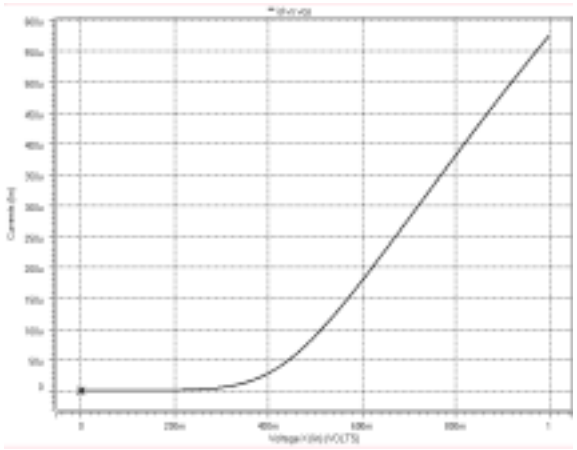
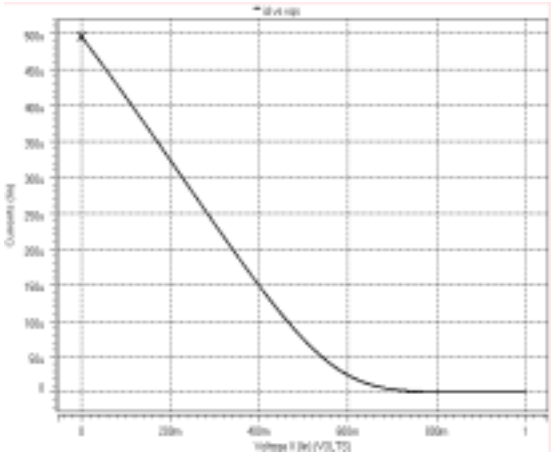


Fig2.I_D vs. V_{GS} plot for a 50/2 NMOS device.



I_D vs. V_{SG} plot for a 100/2 PMOS device

AC ANALYSIS OF DIFFERENTIAL AMPLIFIERS (GE):

P Diff Amp:

With devices of length=2 (biasing Mosfets), gain ($g_m r_{on} || g_m r_{op}$) =3.39dB and f_{3dB} is 80.7 KHz as shown in the figures below (fig 3a).

Now as gate to source voltage of the amplifying device is decreased 320mV we would expect f_{3dB} to decrease, gain $g_m r_{on} || g_m r_{op}$ to increase.

From Sims $g_m r_{on} || g_m r_{op}$ with the L=10 devices is 4.43dB and f_{3dB} is 79 KHz which agrees with the above statement. *This can be observed from sim (fig 3b).*

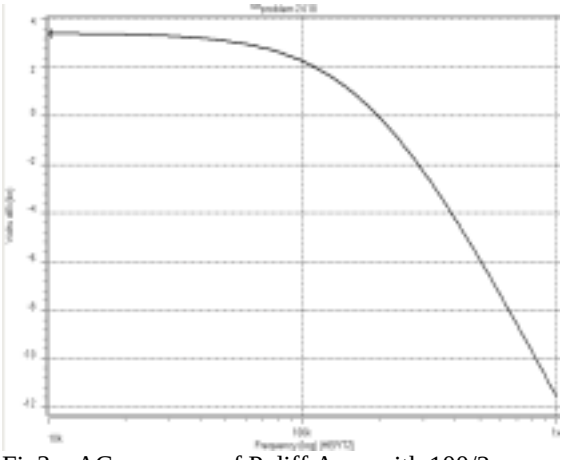


Fig3a. AC response of P diff Amp with 100/2 biasing devices.

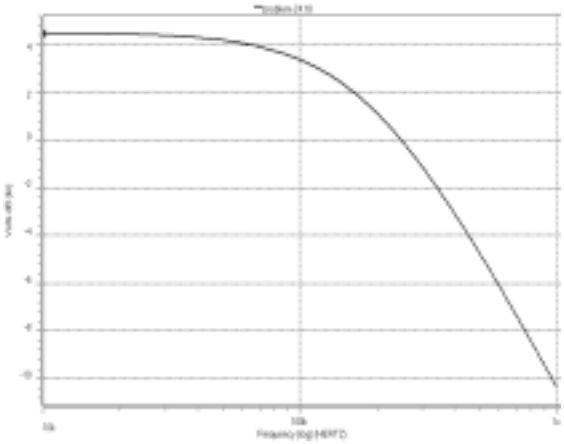


Fig3b. AC response of P diff Amp with 100/10 biasing devices.

N Diff Amp:

With L=2 biasing devices— gain is 1.97dB and f_{3dB} is 79 KHz.

With L=10 biasing devices—gain is 3.70dB and 75.8 KHz.

This can be observed from sim (fig4a, 4b).

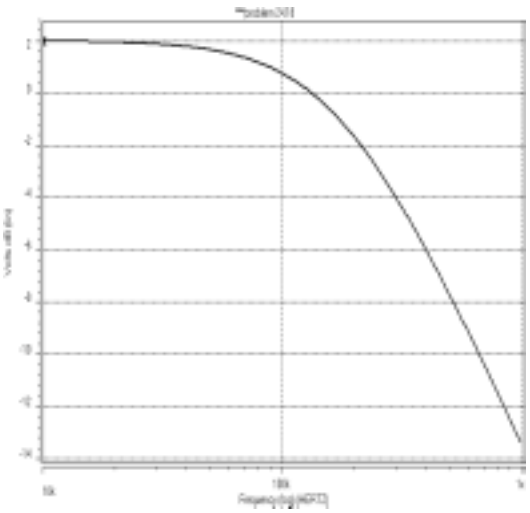


Fig4a. AC response of N diff Amp with 50/2 Biasing devices.

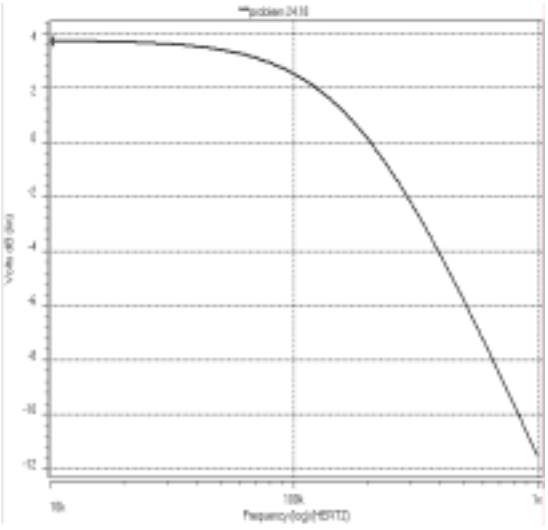


Fig4b. AC response of N diff Amp with 50/10 Biasing devices.

From the results obtained above we see that there is only a small decrease in f_{3dB} and a small increase in the gain.

AC ANALYSIS OF OPERATIONAL AMPLIFIER:

Frequency response of op-amp in fig 24.51(in text book with L=2 in GE biasing devices) is shown in fig (5).

From fig (5) Gain=75.3dB, f_{3dB} = 47.2 KHz and f_{un}=373 MHz.

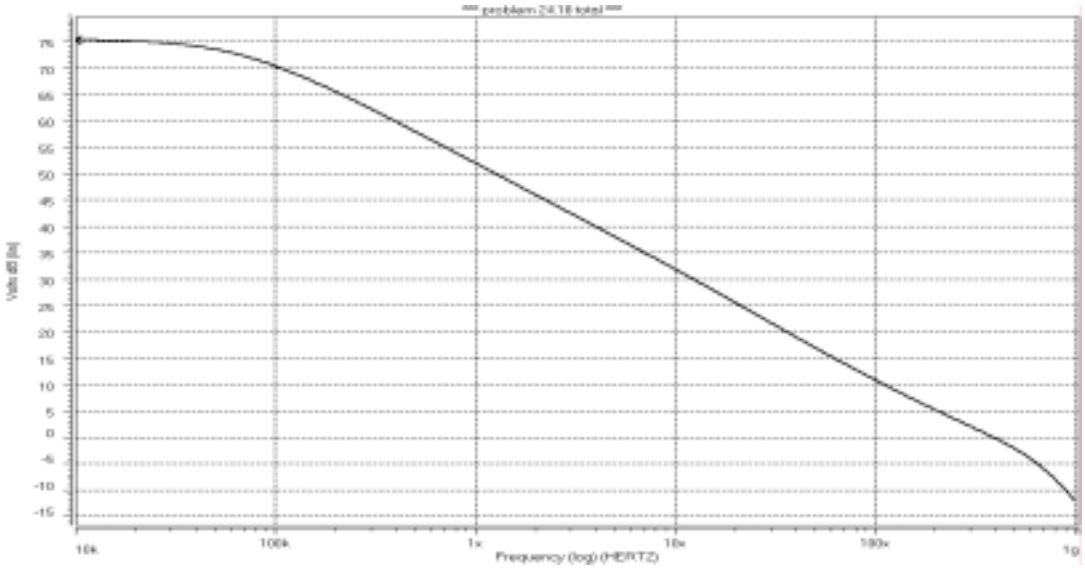


Fig5. Frequency response of op-amp shown in fig 24.51

Frequency response of op-amp with modified GE is as shown in fig (6). From fig (6) Gain=75.1dB, f_{3dB}=48dB and f_{un}=380 MHz.

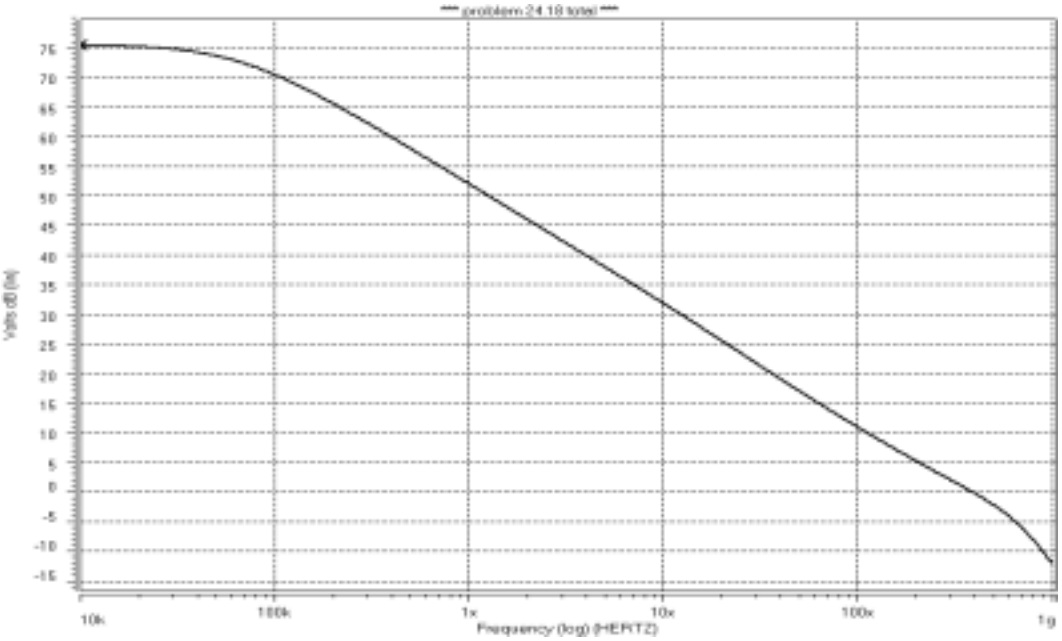


Fig6. Frequency response of op-amp with modified GE

As seen from the above graphs, using the modified GE Diff amps in the op-amp *didn't change the frequency characteristics much* of the op-amp. This can be explained as below:

The frequency response of the op-amp with GE circuitry is

$$A_{OLD,GE}(f) = A_{OLDC}(f) \bullet A_{GE}(f) \text{---------- (1)}$$

$$\Rightarrow A_{OLGE}(f) = \frac{A_{OLDC}}{1 + j\frac{f}{f_{3dB}}} \bullet \frac{A_{GEDC}}{1 + j\frac{f}{f_{3dBGE}}} \text{ ---------- (2)}$$

$$\text{If } f >>> f_{3dB} \text{ then } A_{OLGE}(f) = \frac{A_{OLDC}}{\frac{f}{f_{3dB}}} \bullet A_{GE}(f) \text{------ (3)}$$

$$f_{3dB} = \frac{1}{2.\pi.(R_{0casn} \amalg R_{0casp}).A_{GE}(f).C_C} \text{ -- (4) (From eq. 24.61 of textbook)}$$

Substituting eq.4 in eq.3 that is considering frequencies above f_{3dB}

$$A_{OLGE}(f) = \frac{A_{OLDC}}{2.\pi.f.(R_{0casn} \amalg R_{0casp}).C_C} \text{ ----- (4)}$$

From the above equations it is clear that the bandwidth (f_{3dB}) of the added amplifier may not be wide. As long as their (added amplifiers) bandwidth is larger than the OP-AMP the GE works as desired. As from fig (3a, 3b) and fig (4a, 4b) we can see that the f_{3dB} of GE is larger than that of OP-AMP though the lengths of the biasing mosfets increased. So it is because of this reason we couldn't observe any change in the frequency response of the OP-AMP.

The current drawn from power supply (VDD) in the modified op-amp (using the lower power GE diff amps) was 6uA less than that seen in fig 24.53. The results of the simulations are as below:

. OP Results:

With L=10 Biasing devices

Element 0:vdd
Volts 1.0000
Current -425.6308u
Power 425.6308u
Total voltage source power dissipation=
425.4667u watts

With L=2 Biasing devices

Element 0:vdd
Volts 1.0000
Current -430.9439u
Power 430.9439u
Total voltage source power dissipation=
430.7762u watts

Transient response:

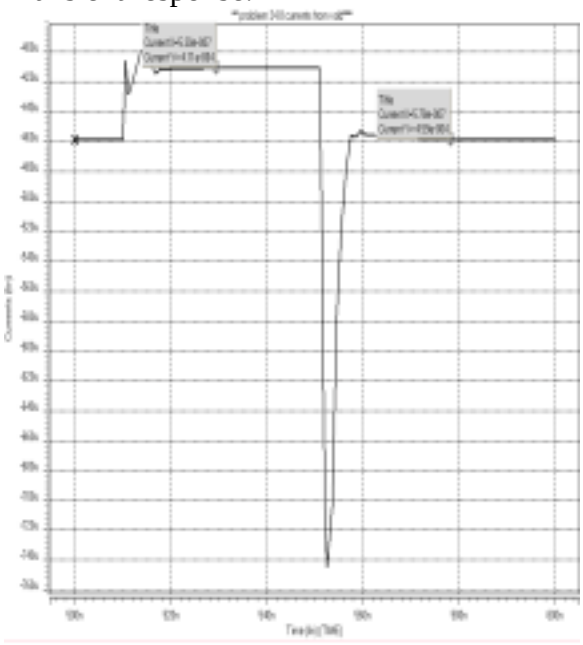


Fig 7. Current from VDD in op-amp with L=2 biasing devices in the GE amplifier.

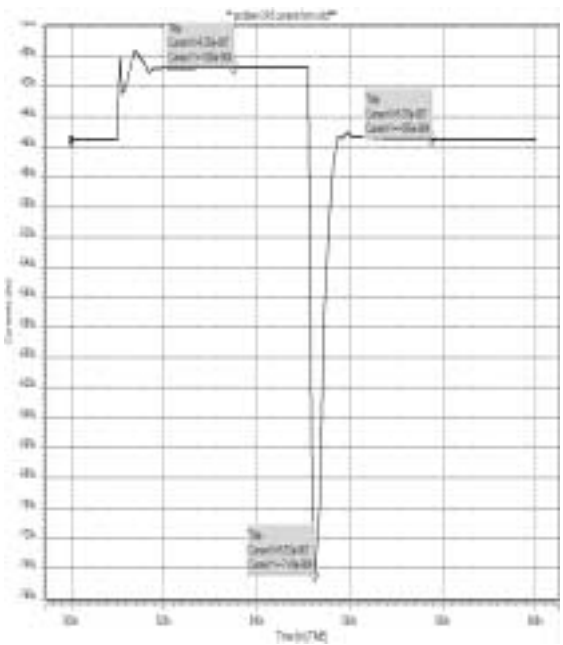


fig8. Current from VDD in op-amp with L=10 biasing devices in the GE amplifier.

CONCLUSION:

The power consumption of the OP-Amp can be decreased by increasing the lengths of the biasing devices in the GE amplifier (decreasing the biasing current and hence the power). Doing this will no way affect the AC response of the Op-Amp as far as the f_{3dB} (bandwidth) of the GE amplifier is more than the bandwidth of the Op-Amp.

NOTE:

Simulations were done in HSPICE using the same netlist used for figure 24.53 except that the biasing devices were changed to L=10.

Problem 24-19
Eric Becker
enebecker@cableone.net

Discussion:

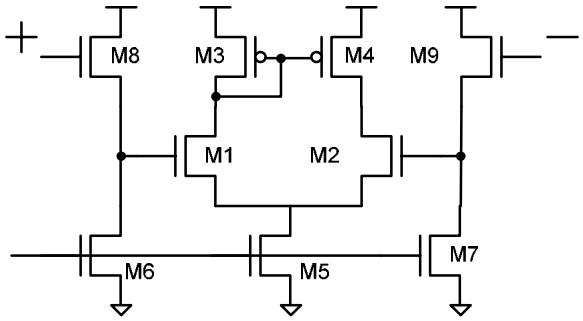


Figure 1. N-type Gain Enhancement Diff-amp

Figure 1 shows an N-type diff-amp that can be utilized for gain enhancement in op-amp design. The purpose of the source follower level shifters is to allow amplification of signals near ground (for P-type amps) or V_{DD} (for N-type amps). For the N-type case M1 and M2 remain in the saturation region because $V_{G1,2}$ is held at $V_{DD} - V_{GS}$. Looking at the saturation equation for M1 gives: $V_{DD} - V_{SG} \geq V_{DD} - V_{GS} - V_{THN}$ ➔ $V_{GS}-V_{SG} \geq -V_{THN}$ which is always true based on values from table 9.2. This justifies the need for source followers in this topology of amplifier.

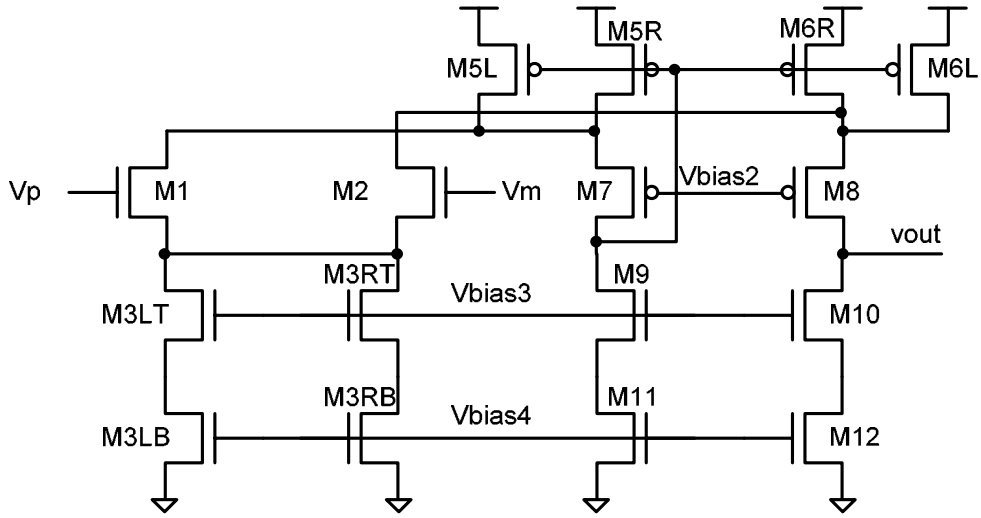


Figure 2. NMOS folded Cascode OTA

Figure 2 shows an NMOS folded cascode OTA. Performing a similar analysis on transistor M1 will show that source follower level shifters are not required for this topology. Assuming $Vp = V_{DD}$ then the following saturation equation can be written for M1: $V_{DD} - V_{SDsat} \geq V_{DD} - V_{THN}$ ➔ $-V_{SDsat} \geq -V_{THN}$ which is also always true based upon table 9.2. The source followers aren't needed because the input diff pair can swing well above V_{DD} (see derivation of equation 22.10). Conversely, for the PMOS folded cascode OTA the input diff-pair can swing well below ground making the need for source follower level shifters unnecessary.

Simulation Results:

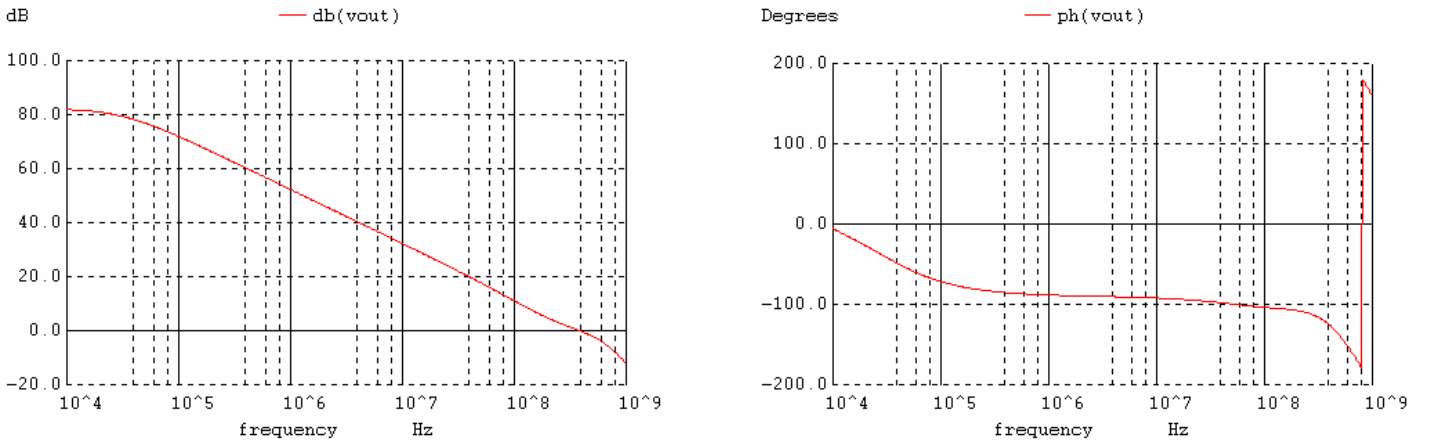


Figure3. AC response of the op-amp in Fig 24.51 with Folded Cascode OTAs as Gain Enhancement Amps

Figure 3 shows the simulation results of the circuit in Fig 24.51 when GE Folded Cascode OTAs are used instead of GE diff-amps. Compared to Fig 24.53 the unity gain frequency and the phase margin at this frequency remain approximately the same. The open loop gain, however has increased substantially by about 10dB.

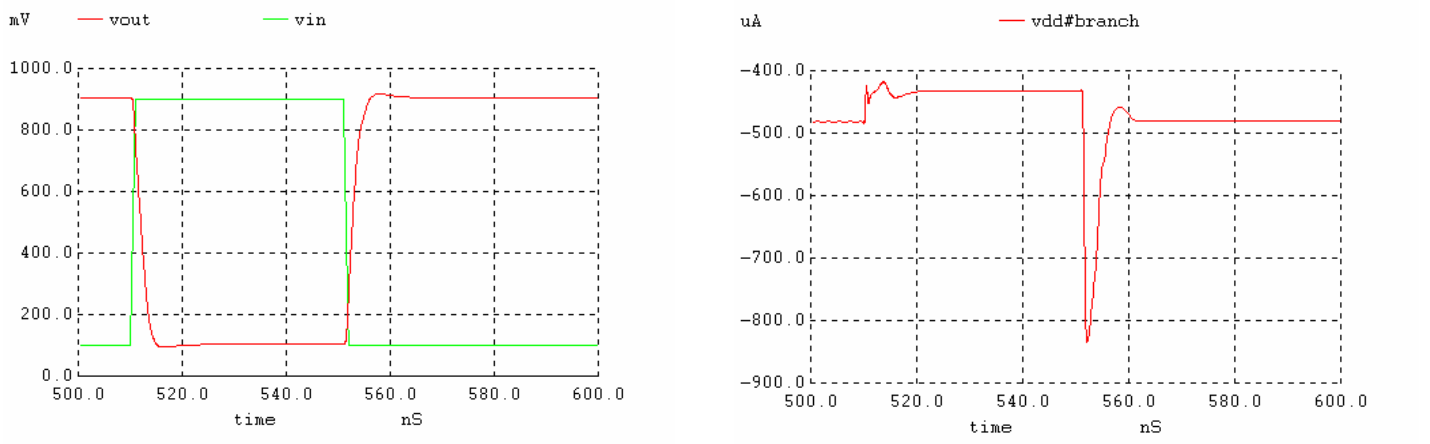


Figure 4. Step Response and Current draw of the op-amp in Fig 24.51 with GE Folded Cascode OTAs

Figure 4 shows the transient step response and current draw of this op-amp. Note that the step response is nearly identical to that of Fig 24.53. This is because the GE amps do not effect the overall speed of the op-amp. The tHL=1.5ns (time high-to-low) and tLH=1.25ns (time low-to-high). Also to negate overshoot the gain enhancement compensation capacitors were doubled to 480fF. The static current draw of this circuit with folded cascode OTAs is approximately 30uA more than the regular draw GE diff-amps. This makes sense because there are four 10uA branches in the GE diff amp, but six 10uA branches in the GE folded cascode OTA. Since are two GE amps (N and P type) the net current difference is 40uA (very close to the observed 30uA or so).

In conclusion, the folded cascode OTA offers a viable gain enhancement substitute over the common GE diff-amp. The main benefit is increased gain with a constant unity gain frequency (which means constant speed). The drawbacks are increased power dissipation and increased susceptibility to instability (which just requires more attention while compensating).

Edits to Netlist from Fig 24.53:

```
xnamp    VDD     Vbias2   Vbias3   Vbias4   outn     vd1      vd2      namp
xpamp    VDD     Vbias1   Vbias2   Vbias3   outp     vd11     vd12     pamp

.ends

.subckt pamp     VDD      Vbias1   Vbias2   Vbias3   vout     vp       vm
M1       Vd1     vp       vss      VDD      PMOS L=2 W=100
M2       Vd2     vm       vss      VDD      PMOS L=2 W=100
M3LB     vss     Vbias2   vd3lt    VDD      PMOS L=2 W=100
M3LT     vd3lt   Vbias1   VDD      VDD      PMOS L=2 W=100
M3RB     vss     Vbias2   vd3rt    VDD      PMOS L=2 W=100
M3RT     vd3rt   Vbias1   VDD      VDD      PMOS L=2 W=100
M5L      vd1     vd7      0        0        NMOS L=2 W=50
M5R      vd1     vd7      0        0        NMOS L=2 W=50
M7       vd7     Vbias3   vd1      0        NMOS L=2 W=50
M6L      vd2     vd7      0        0        NMOS L=2 W=50
M6R      vd2     vd7      0        0        NMOS L=2 W=50
M8       vout    Vbias3   vd2      0        NMOS L=2 W=50
M9       vd7     Vbias2   vd11     VDD      PMOS L=2 W=100
M11      vd11    Vbias1   VDD      VDD      PMOS L=2 W=100
M10      vout    Vbias2   vd12     VDD      PMOS L=2 W=100
M12      vd12    Vbias1   VDD      VDD      PMOS L=2 W=100
cc       vout    0        480f
.ends

.subckt namp     VDD      Vbias3   Vbias4   Vbias2   vout     vp       vm
M1       vd1     vp       vss      0        NMOS L=2 W=50
M2       Vd2     vm       vss      0        NMOS L=2 W=50
M3LT     vss     Vbias3   vd3lb    0        NMOS L=2 W=50
M3LB     vd3lb   Vbias4   0        0        NMOS L=2 W=50
M3RT     vss     Vbias3   vd3rb    0        NMOS L=2 W=50
M3RB     vd3rb   Vbias4   0        0        NMOS L=2 W=50
M5L      vd1     vd7      VDD      VDD      PMOS L=2 W=100
M5R      vd1     vd7      VDD      VDD      PMOS L=2 W=100
M7       vd7     Vbias2   vd1      VDD      PMOS L=2 W=100
M6L      vd2     vd7      VDD      VDD      PMOS L=2 W=100
M6R      vd2     vd7      VDD      VDD      PMOS L=2 W=100
M8       vout    Vbias2   vd2      VDD      PMOS L=2 W=100
M9       vd7     Vbias3   vd11     0        NMOS L=2 W=50
M11      vd11    Vbias4   0        0        NMOS L=2 W=50
M10      vout    Vbias3   vd12     0        NMOS L=2 W=50
M12      vd12    vbias4   0        0        NMOS L=2 W=50
cc       vout    0        480f
.ends
```

Kloy Debban

P24.20

Referring to figure 24.6, (which is repeated below in figure 1 of this solution,) and according to equation 24.5:

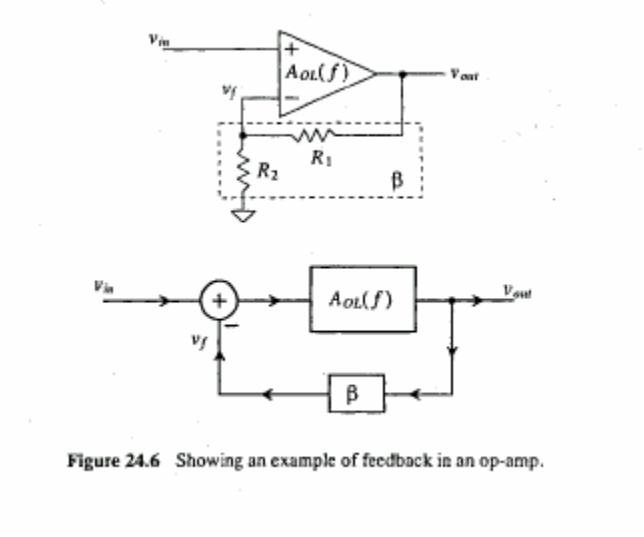


Figure 24.6 Showing an example of feedback in an op-amp.

Figure 1.

$$A_{CL}(f) = \frac{V_{out}}{V_{in}} = \frac{A_{OL}(f)}{1+\beta * A_{OL}(f)} \quad (24.5)$$

If $A_{OL}(f) \to \infty$, then the closed loop gain $A_{CL}(f) \to \frac{1}{\beta}$, and:

$$V_{out} = A_{CL}(f) * V_{in} = \frac{1}{\beta} * V_{in} \Rightarrow \beta = \frac{V_{in}}{V_{out}} = \frac{250mV}{500mV} = \frac{1}{2}$$

Now, if $A_{OL(f)}$ does not go to ∞, then using equation 24.5, and solving for V_{out},

$$V_{out} = V_{in} * \frac{A_{OL}(f)}{1+\beta * A_{OL}(f)} \Rightarrow 500mV \pm 1mV = 250mV * \frac{A_{OL}(f)}{1+\frac{1}{2} * A_{OL}(f)}$$

Solving for the absolute value of $A_{OL(f)}$:

$$\Rightarrow \left|A_{OL}(f)\right| = \frac{500mV \pm 1mV}{250mV - \frac{500mV \pm 1mV}{2}} \approx 1000$$

Problem 24.21. (Ken Waller)

Design a voltage regulator that can supply at least 50 mA of current at 500mV with VDD as low as 600mV using the minimum amount of Cload.

The voltage regulator circuit that I chose, shown in Figure 1, can pull the gate of the large PMOS output device, P5, very close to VSS to meet the 600 mV VDD specification. The device size for P5 was determined by calculating the width needed to source 90 mA with VDD at 600 mV. I picked 90 mA to guarantee that the design will have margin to process parameters and operating conditions such as temperature. I calculated the width using both the short and long L equations and simulations verified that the long L equation gave a better answer. I rounded the width of P5 up to 50,000u.

Long L Equation:

W = (2 * L * ID) / [KPp * (VGS – VTHp)**2]

Where VGSmin = 600 mV – 70 mV = 530 mV

W = 2 * 0.09A / [60 uA/V * (0.53V – 0.28V)**2]

W = 48,000u

Short L Equation:

W = ID / [Vsat * Cox' * (VGS – VTHp – VDSsat)]

W = 0.09A / [(90 * 10**9 um/s) * (25 fF/um**2) * (0.53V – 0.28V – 0.05V)]

W = 200u or 4,000 drawn

I shifted the 500 mV VREF signal down by 5% so that I did not have to directly connect VREG to the gate of N2. This allows the VREG voltage to be adjusted either up or down by changing the value of resistor R3 and or R6. I only shifted the REF voltage at the gate of N0 down 5% to keep current source transistor N1 in the saturation region.

The switching current driving the gate of P5 was increased by sizing up P4 and N3. This extra current reduced the magnitude of the VREG voltage dip

whenever the output current load was either increased. Transistor P5 is biased on by the current source device N5 and resistors R5 and R6. Capacitor C0 is used to improve the large signal performance of the regulator by coupling the gate of P5, GPU or Gate of Pull-up, to VREG. For example, when VREG moves to a lower voltage, GPU will be pulled lower by capacitor C0, which will increase the VGS voltage of P5 thereby increasing the amount of current it supplies to the load. All of the other transistors were sized with the biasing from Table 9.2.

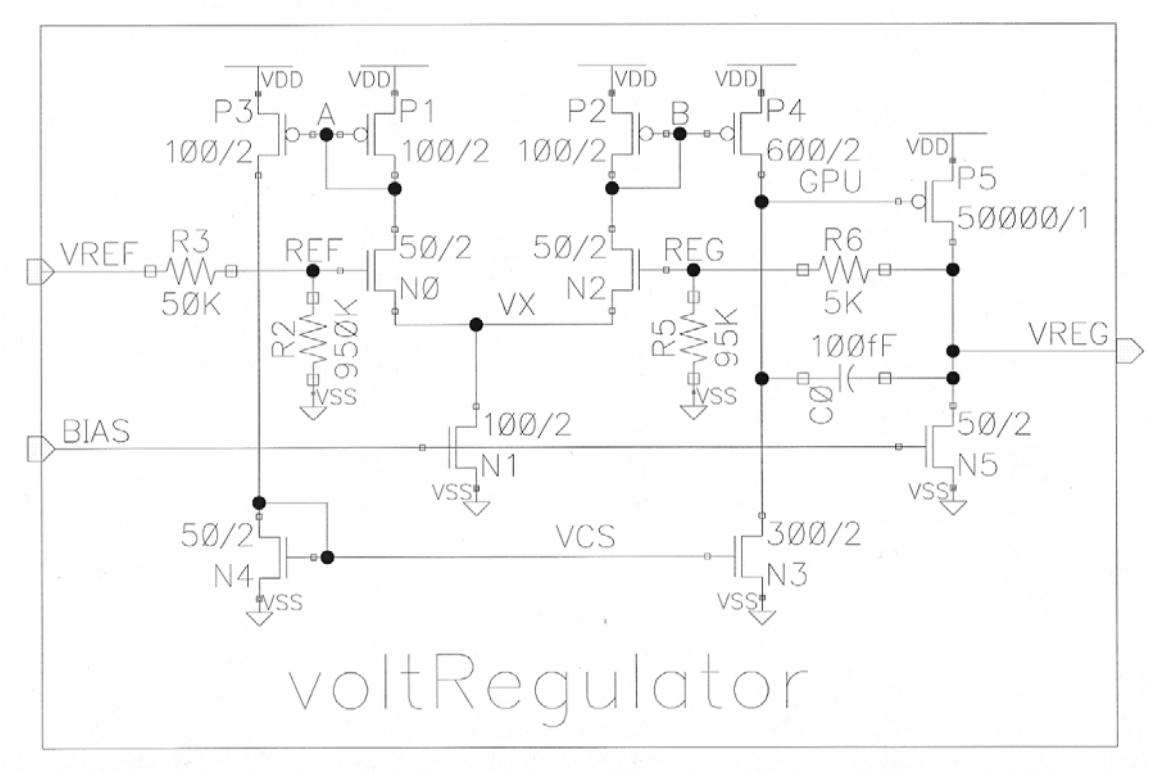


Figure 1 – Voltage Regulator Schematic

The transient response of the voltage regulator circuitry with three types of current spikes was investigated. They were a fast ramp up to a large DC current, 50 mA, followed by a fast ramp back to no current, a slow ramp up to a 75 mA current followed by a slow ramp down, and two short duration 50 mA current spikes. Figures 2, 4 and 8 show how the voltage regulator circuitry reacted to these three type of current spikes with three different values of capacitive loads. Figure 2 had a 1 nF load, Figure 4 had a 10 nF load, and Figure 8 had a 100 nF load.

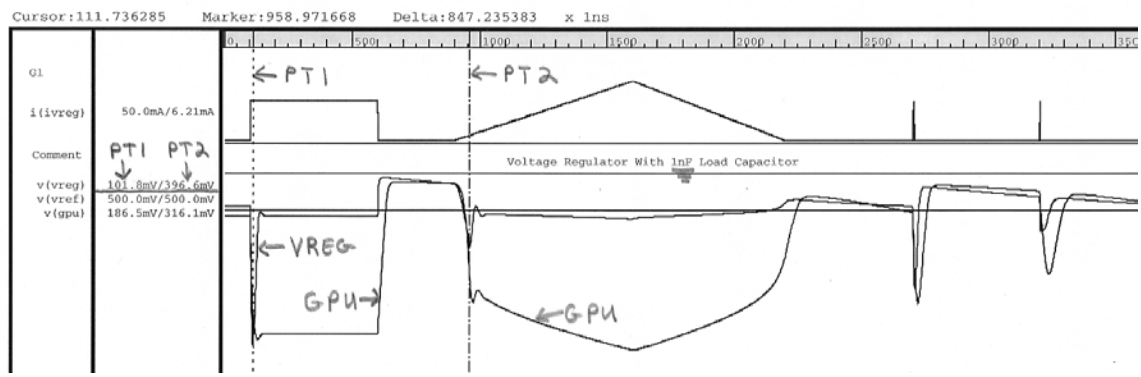


Figure 2 – Transient Response With A 1 nF Load Capacitance

In Figure 2, the top waveform, I(ivreg), is the transient current stimulus that is applied to the VREG output node. PT1 is at the start of the 1ns ramp up to pulling a 50 mA current out of the voltage regulator. Notice that the V(vreg) voltage falls from 500mV to 101 mV before recovering. The signal GPU is the gate of the 50,000 drawn micron device (final size is 2,500u), P5. When the fast current ramp occurs, most of the current will be supplied by the capacitive load until GPU reaches a low enough value to set P5's VGS to supply 50 mA. It takes the voltage regulator 12 ns to get GPU biased and stop VREG from falling and 38 ns before VREG recovers to the correct voltage. At 600 ns the 50 mA current is turned of in 1 ns and notice that VREG overshoots the 500 mV target by 90 mV before GPU gets to a high enough voltage so P5 only supplies the bias current. Due to the small amount of biasing current on the VREG node, it will take a long time, thousands of nano-seconds, to reach the 500 mV target.

PT2 is at the start of the 700 ns ramp up to 75 mA. VREG dips to 396 mV before recovering in 47 ns to the correct voltage. The two current spikes at the end of the simulation output show the circuit's response to a 10 ns wide (332 mV) and a 4 ns wide (451 mV) 50 mA current spike. Notice that VREG is poorly regulated for both of these current spike cases. The 1 nF capacitor is not large enough to hold the VREG voltage while the voltage regulator turns on.

Figure 2A shows a blowup of the response to a 50 mA fast ramp on and off. Notice how large the VREG voltage glitch is when the current is quickly ramped to 50 mA. Capacitor C0 can be increased in size to more closely couple GPU to VREG but this will significantly slow down the response for the slow ramp condition. Since the gate to drain capacitance of P5 is 1 pF,

C0 needs to be several pico farads to have an effect. When the current is quickly ramped off, VREG overshoots the 500 mV target by 95 mV and notice how slowly the bias current is pulling VREG down to the correct voltage. Figure 2B shows a blowup of the response to the fast ramp with the bias current of N5 increased from 10 uA to 2 mA. This 2 mA current will bias the GPU node to a lower voltage and the voltage regulator can respond quicker to the current spike since GPU does not have to move as many milli-volts. The glitch stills has a low voltage of 221 mV and is not any narrower. This extra current improved the recovery response of the circuit to the overshoot when the current is quickly ramped off.

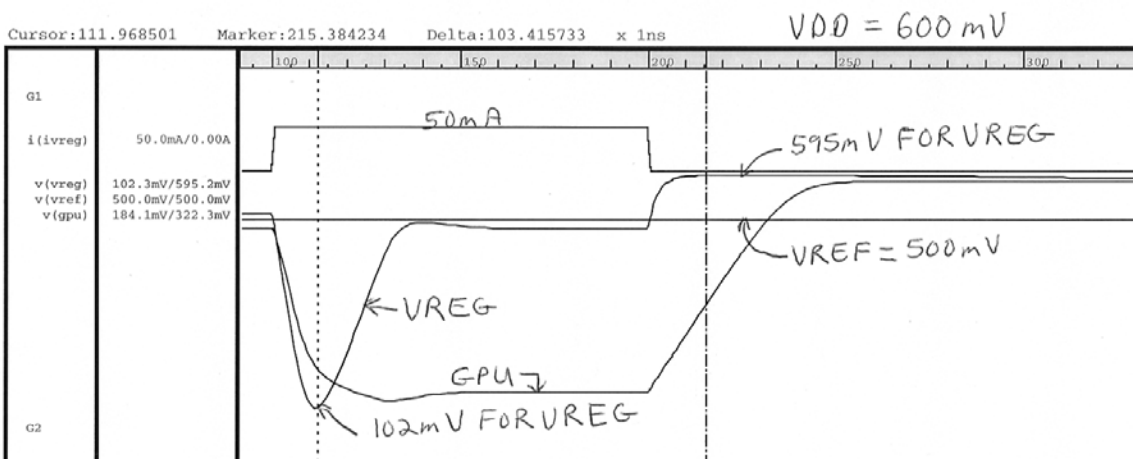


Figure 2A – Transient Response For a Fast Ramp With a 1 nF Load Capacitance

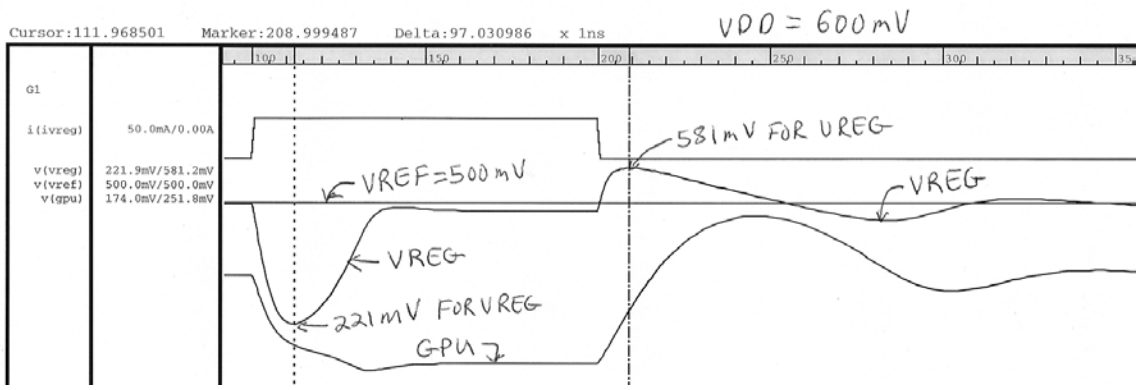


Figure 2B – Transient Response For a Fast Ramp With a 1 nF Load Capacitance and a 2 mA Load Current

Figure 3A and 3B show the frequency response of the Figure 1 circuitry with a 1 nF load capacitance.

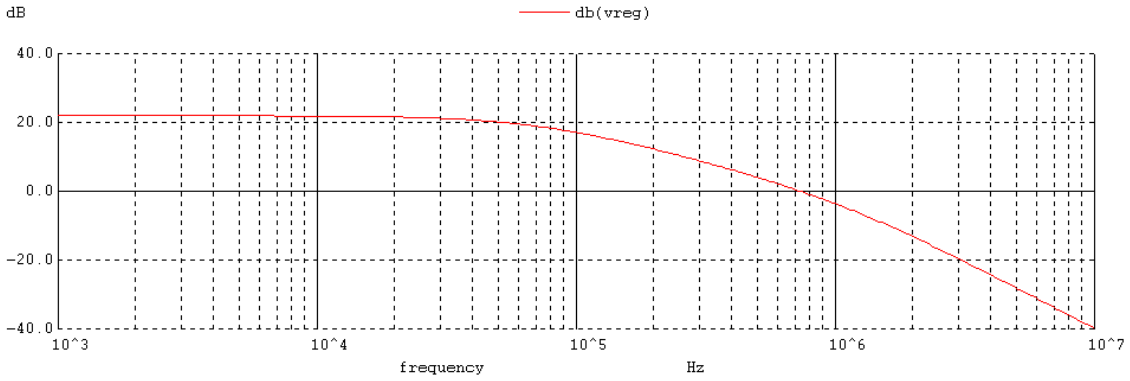


Figure 3A - Gain Response With CLoad = 1 nF
FUN = 740 KHz, AOLDC = 21.9 dB

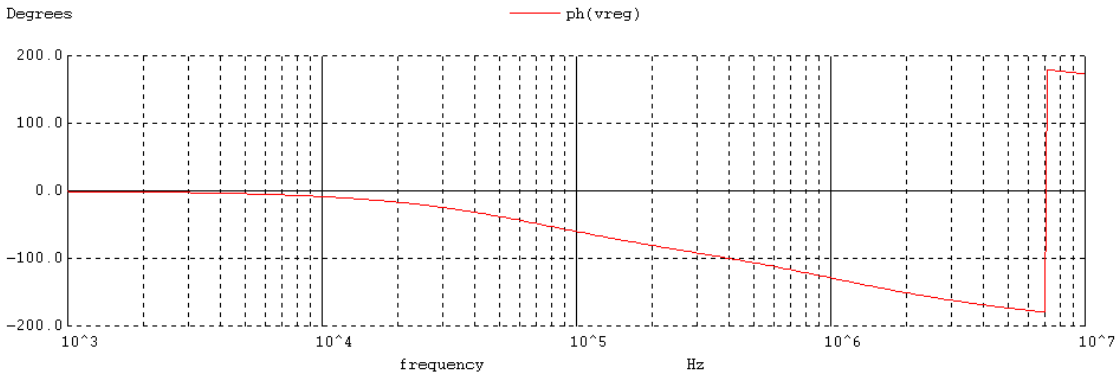


Figure 3B - Phase Response With CLoad = 1 nF
PHASE MARGIN = 62 Degrees

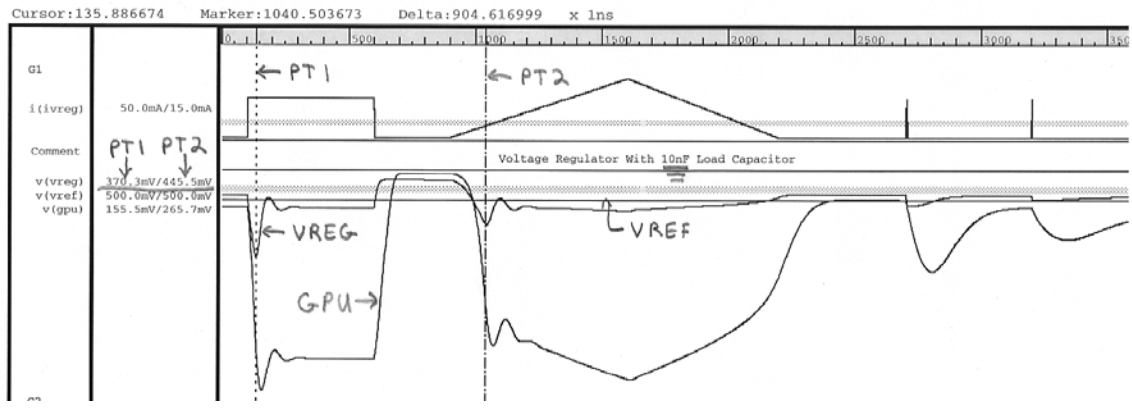


Figure 4 – Transient Response With A 10 nF Load Capacitance

In Figure 4, the top waveform, I(ivreg), is the transient current stimulus that is applied to the VREG output node. PT1 is at the start of the 1ns ramp up to pulling a 50 mA current out of the voltage regulator. Notice that the V(vreg) voltage falls from 500 mV to 370 mV before recovering. The signal GPU is the gate of the 50,000 drawn micron device (final size is 2,500), P5. When the fast current ramp occurs, most of the current will be supplied by the capacitive load until GPU reaches a low enough value to bias P5's VGS to supply 50 mA. It takes the voltage regulator 33 ns to get GPU biased and stop VREG from falling and 71 ns before VREG recovers to the correct voltage. At 600 ns the 50 mA current is turned of in 1 ns and notice that VREG overshoots the 500 mV target by 47 mV before GPU gets to a high enough voltage so P5 only supplies the bias current. Due to the small amount of biasing current on the VREG node and the 10 nF load capacitance, it will take an even longer time to reach the 500 mV target than the 1 nF load capacitance version.

PT2 is at the start of the 700 ns ramp up to 75 mA. VREG dips to 445 mV before recovering in 90 ns to the correct voltage. The two current spikes at the end of the simulation output show the circuits response to a 10 ns wide and a 4 ns wide 50 mA current spike. VREG is able to stay within 10 mV of the 500 mV target during these two current spikes. With a 10 nF load capacitance, the voltage regulator can handle large short duration current spikes but stills has trouble with the fast current ramp to a large DC current. Its response to the slow ramp case is not very good but with extra bias current this can be corrected.

Figure 4A shows a blowup of the response to a 50 mA fast ramp on and off. Notice how much shallower the VREG voltage glitch is versus Figure 2A and noticed that the glitch is fifty percent wider when the current is quickly ramped to 50 mV. The longer duration is caused by the added time it takes P5 to charge the ten times larger output capacitance. When the current is quickly ramped off, VREG overshoots the 500 mV target by 47 mV and will take thousand of nano-seconds to pull VREG down to the correct voltage. Figure 4B shows a blowup of the response to the fast ramp with the bias current of N5 increased from 10 uA to 2 mA. The glitch stills has a low voltage of 403 mV and is not any narrower. However, this extra current improved the recovery response of the circuit to the overshoot when the current is quickly ramped off and VREG was never more than 30 mV away from VREF during the slow ramp current condition. The bias current must be larger than 10 uA when the load capacitance is so large to quickly correct any overshoot potential.

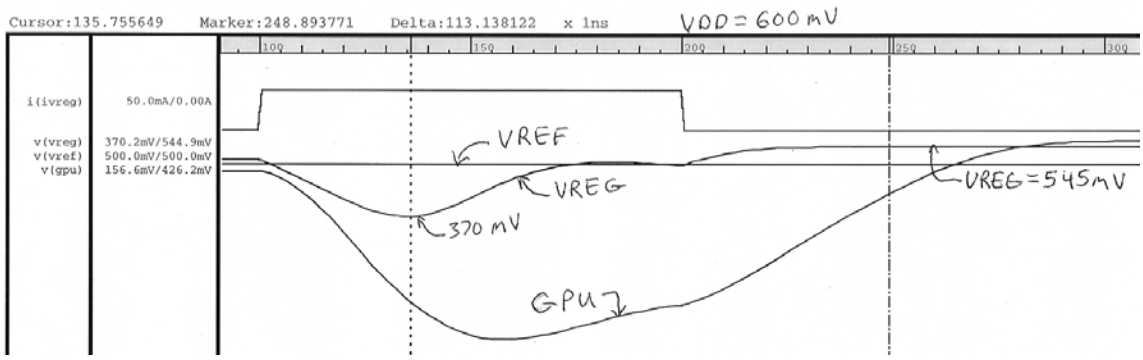


Figure 4A – Transient Response For a Fast Ramp With a 10 nF Load Capacitance

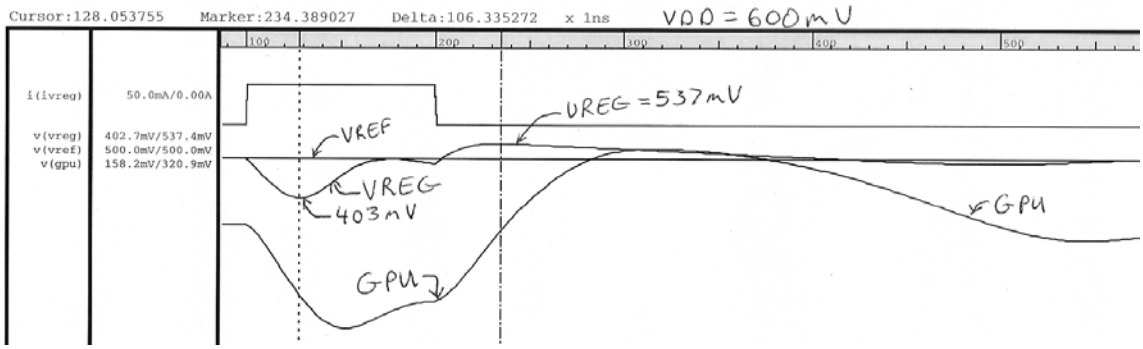


Figure 4B – Transient Response For a Fast Ramp With a 10 nF Load Capacitance and a 2 mA Load Current

The frequency response was hand calculated for the 10 nF load capacitance case. Figure 5 shows the schematic I used to calculate the input and output poles. Node V1 corresponds to node GPU and node V2 corresponds to node VREG in Figure 1.

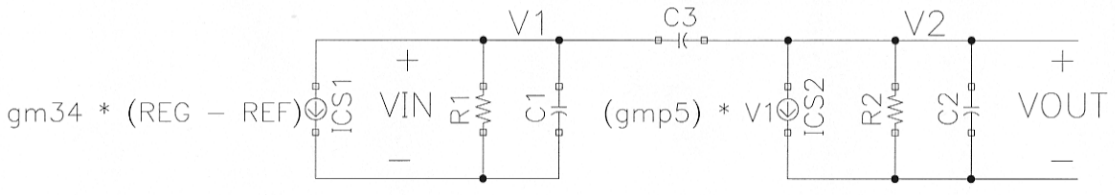


Figure 5 – Frequency Response With 10 nF Load Capacitance

R1 = RONp4 || RONn3 = 333K * 100 / 600 || 167K * 50 / 300
R1 = 55.5K || 27.8K = 18.5K

C1 = Cgsp5 + Cgdp4 + Cgdn3
C1 = 50,000 * 8.34f / 200 + 600 * 3.7f / 100 + 300 * 1.56f / 50
C1 = 2.1 pF

C3 = Cgdp5 + C0 = 50,000 * 3.7f / 200 + 100 f = 1.03 pF

R2 = RONp5 || RONn5 = 333K * 50 / 50000 || 167K = 333

C2 = Cload + Cgdn5 = 10 nF

gmp5 = sqroot(50,000 / 50) * 150 uA/V = 4.7 mA /V
gmp5 simulated at 195 mA/V and RONp5 simulated at 28 with the device exhibiting very strange behavior even with the L=2. The PMOS model did not work correctly for a DC sweep with a W = 50,000.

gm34 = 150 uA/V * 300 / 50 = 900 uA/V simulated at 1 mA/V

A1st = gm34 * R1 = 900 uA/V * 18.5K = 16.7 V/V

A2nd = gmp5 * R2 = 4.7 mA/V * 333 = 1.57 V/V

AOLDC = A1st * A2nd = 16.7 * 1.57 = 26.2 = 28.4 dB

f1 = 1 / [2 * pi * R1 * (C1 + C3 * (A2nd + 1))]
f1 = 1 / [6.28 * 18.5K * (2.1p + 1.6p)
f1 = 2.3 MHz

f2 = (gmp5 * C3) / [2 * pi * (C1 * C2 + C1 * C3 + C2 * C3)]
f2 = 4.7m * 1.03p / [6.28 * (2.1p * (10n + 1p) + 10n * 1p)]
f2 = 24 KHz

fz = gm2 / (2 * pi * C3) = 4.7m / (6.28 * 1.03p) = 726 MHz

Figure 6 shows the schematic used to AC simulate the voltage regulator. From simulation results shown in Figure 7A and Figure 7B; f1 = 1.5 MHz, f2 = 17 KHz, fun = 98 KHz, and AOLDC = 21.9 dB. All of these value were reasonably close to the hand calculated values.

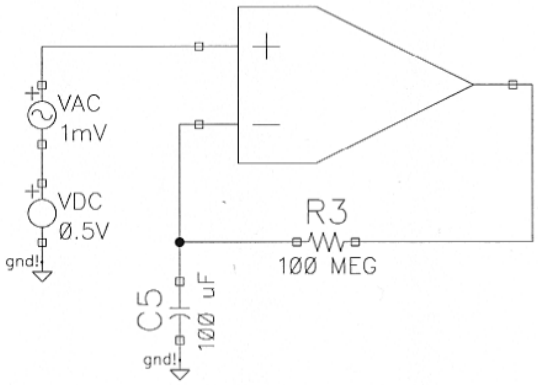


Figure 6 – Schematic To Measure Frequency Response

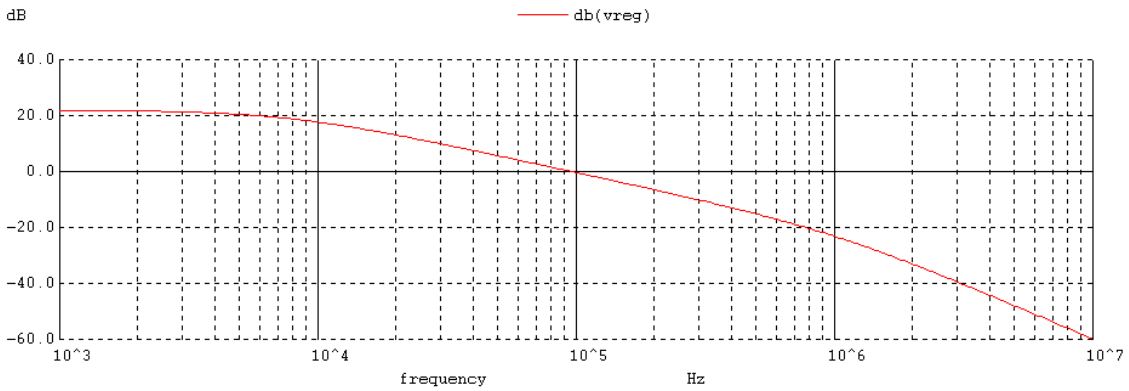


Figure 7A - Gain Response With CLoad = 10 nF
FUN = 98 KHz, AOLDC = 21.8 dB

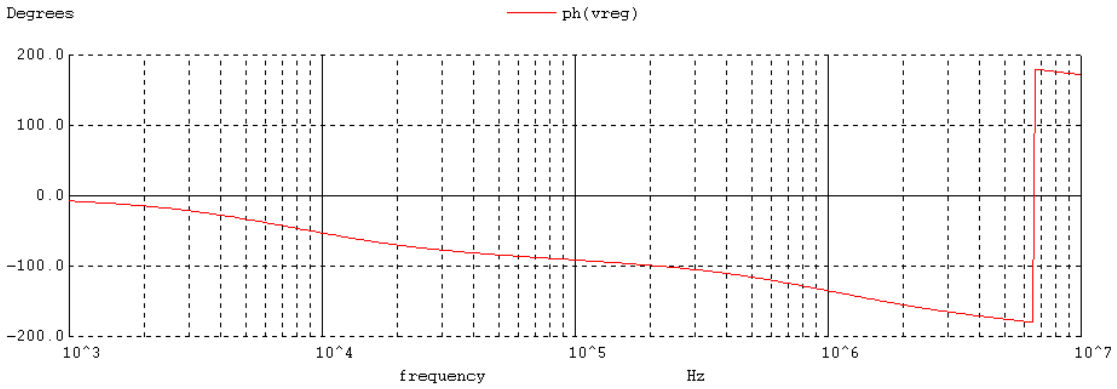


Figure 7B - Phase Response CLoad = 10 nF
Phase Margin = 88 Degrees

In Figure 8, the top waveform, I(ivreg), is the transient current stimulus that is applied to the VREG output node. PT1 is at the start of the 1ns ramp up to

pulling a 50 mA current out of the voltage regulator. Notice that the V(vreg) voltage falls from 500mV to 459 mV before recovering. It takes the voltage regulator 106 ns to get GPU biased and stop VREG from falling and 250 ns before VREG recovers to the correct voltage. At 600 ns the 50 mA current is turned of in 1 ns and notice that VREG overshoots the 500 mV target by 10 mV before GPU gets to a high enough voltage to shutoff. The simulation results with the 100 nF capacitor look acceptable for all the current transient cases. The problem with using a 100 nF is that it is too large to fit on a computer chip. Simulations show that the larger Cload is, the better the voltage regulator circuit works.

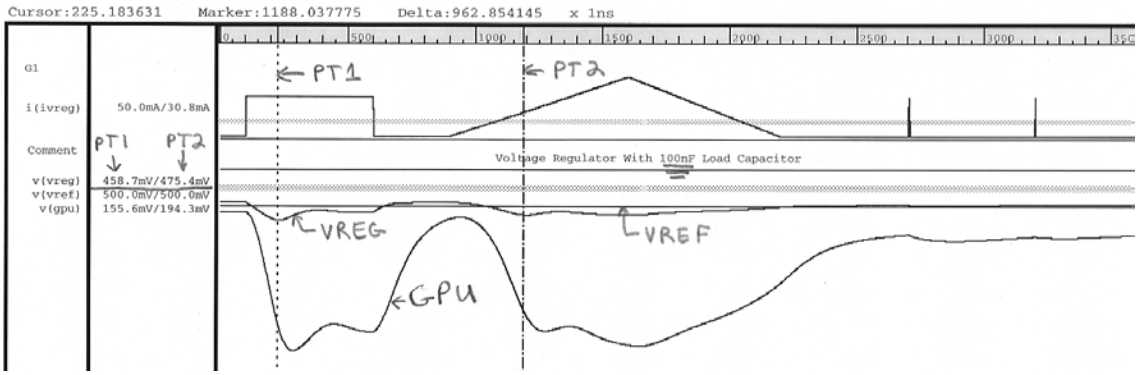


Figure 8 – Transient Response With A 100 nF Load Capacitance

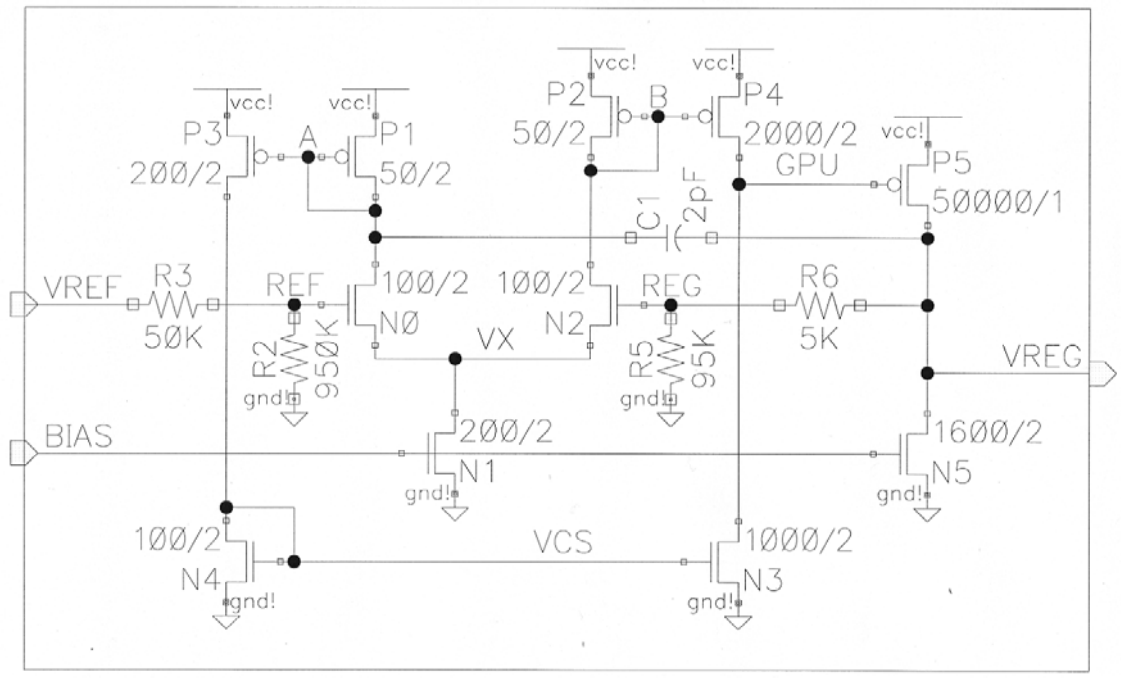


Figure 9 – Final Voltage Regulator Schematic

I redesign the voltage regulator circuit to improve the response with a 10 nF load and the new circuit is shown in Figure 9. To improve the transient response of the voltage regulator for a fast current ramp, node GPU must switch faster so P5 will supply most of the current instead of relying on the capacitor. The switching current driving GPU was increased by sizing N3 from 300u to a 1000u and P4 from 600u to 2000u. The differential amp current was doubled to 32 uA and both of these changes reduced the dip voltage from 370 mV to 412 mV when VDD is 600 mV. The slow ramp dip is now acceptable at 476 mV.

I wanted to increase the biasing current to 2 mA to improve the fast ramp off condition and reduce the fast ramp on dip voltage but this lowered the phase margin to 25 degrees. The extra current moved the unity gain frequency up to 3 MHz and the AOLDC to 36.7 dB. Pole f2 moved out to 100 KHz and pole f1 occurred at 1.1 MHz. Changing transistor N5 size or the VREG bias current dramatically moved the location of the unity gain frequency, the output pole location and the open loop gain. I picked a size of 1600/2 or a bias current of 350 uA to keep the phase margin around 80 degrees. This change reduced the dip voltage to 425 mV.

Further Increases to the widths of P4 and N3 as well as P5 had very little effect on the performance for this fast ramp case. Making the Ls of P4 and N3 equal to one improved the performance significantly but caused a very large offset in the VREG voltage with no load current that I was unable to remove. To improve the performance I need to increase the current driving node GPU without adding any more parasitic load. I decided to increase the current by raising the VGS bias voltages of P4 and N3 by sizing down P1 and P2. This size change caused a three times increase in the current driving GPU and reduced the dip voltage to 445 mV and all of these changes reduced the overshoot voltage from 545 mV to 509 mV. I also hooked the compensation capacitor C0 to node A instead of GPU which will increase the current in N3 when VREG falls and decrease the current in N3 when VREG rises. This capacitor increased the current in N3 by 12 percent during the fast current transient with less voltage change on VREG. These circuit changes improved the dip voltage to 452 mV and the overshoot voltage to 505 mV. The durations of these perturbations or dips were reduced unlike the increase in duration when adding extra load capacitance. Figure 10 shows the transient response for this new circuit for the fast ramp case. I did not show the other cases since VREG is fairly stable for the new circuit with only 27 mV of total change. Figure 11 shows the transient response for VDD equal to 1V. Notice that VREG has a 22 mV offset when driving only the

bias current. At VDD equal to 600 mV, VREG had a negative offset of 22 mV at the 50 mA load current. In Figure 10 and 11, the gate voltages, REF and REG, of the diff pairs are shown and notice how the voltage regulator does not try to correct the offset for these two cases.

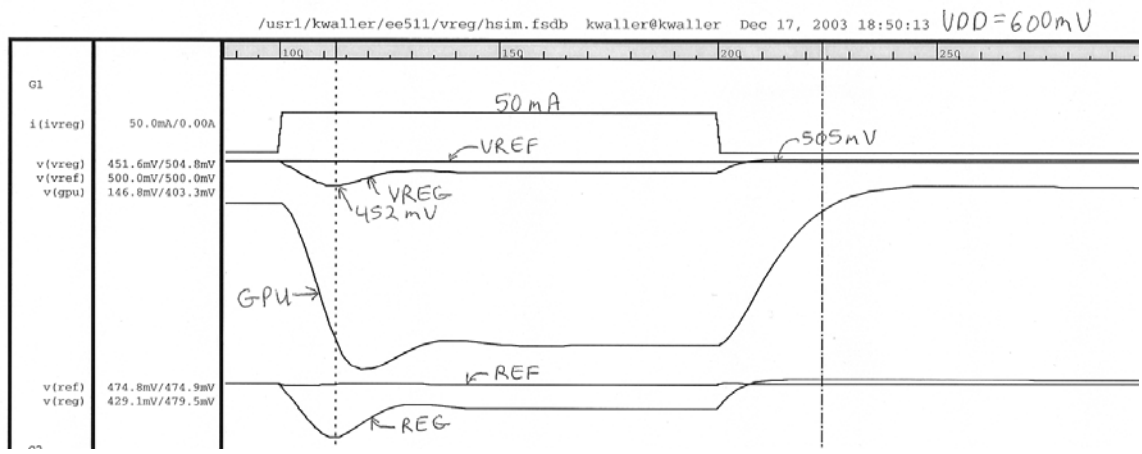


Figure 10 – Transient Response To A 50 mA Fast Ramp

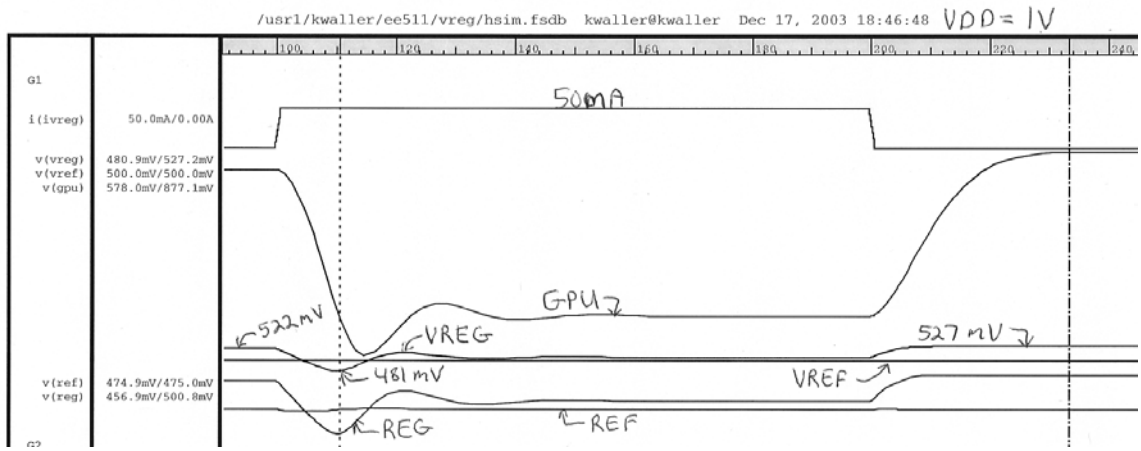


Figure 11 – Transient Response To A 50 mA Fast Ramp
VDD = 1V

Figure 12A and 12B show the frequency response for the circuit shown in Figure 9 with a 10 nF load capacitance. The unity gain frequency was 550 KHz with a phase margin of 72 degrees. The phase margin and unity gain frequency can be moved by changing the VREG bias current or the size of N5.

The voltage regulator current was 1 mA including the 350 uA VREG bias current. If you could add more load capacitance or tolerate a dip voltage of

425 mV the current could be lowered by 430 uA by sizing up P1 and P2. I used a beta multiplier circuit's VBIASN to drive BIAS.

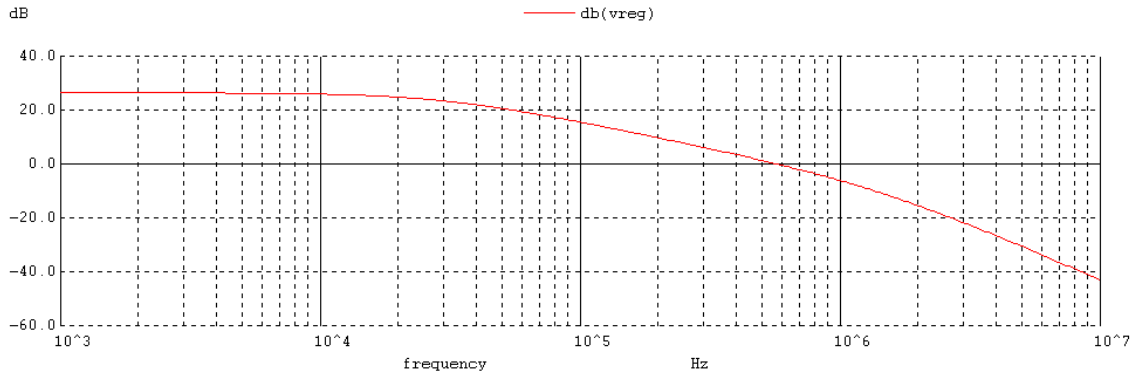


Figure 12A - Gain Response With CLoad = 10 nF
FUN = 550 KHz, AOLDC = 26.4 dB

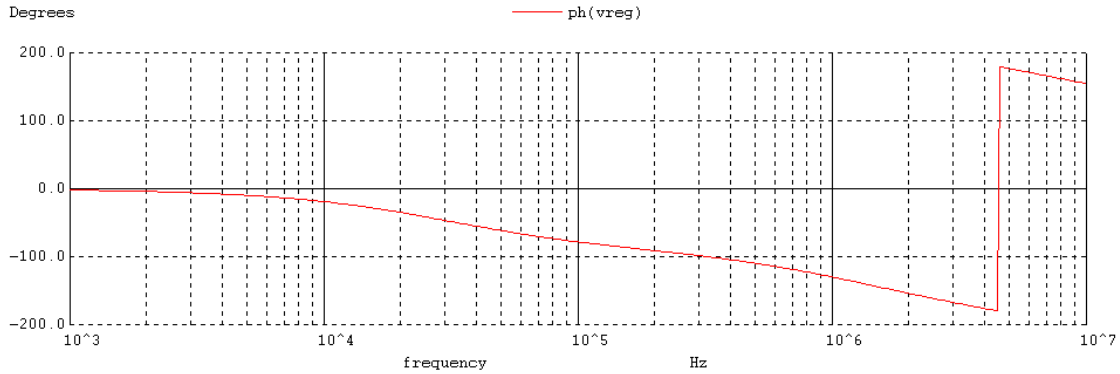
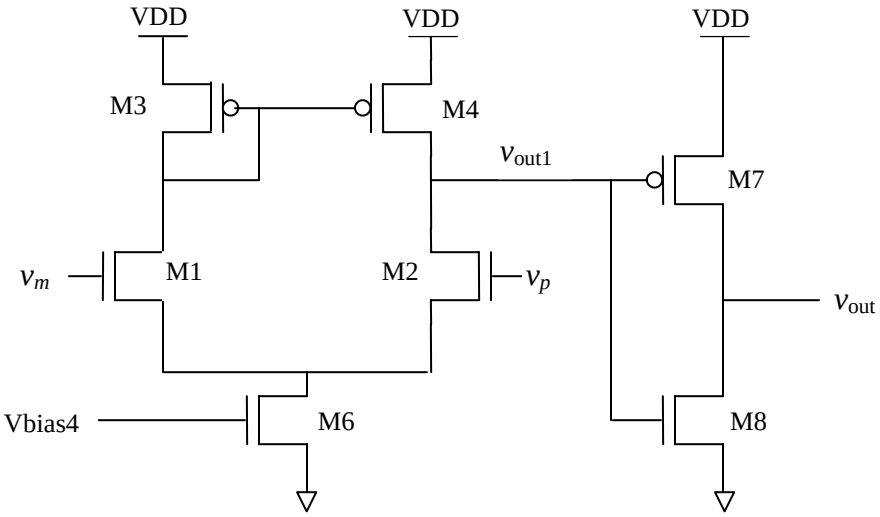


Figure 12B - Phase Response CLoad = 10 nF
Phase Margin = 72 Degrees

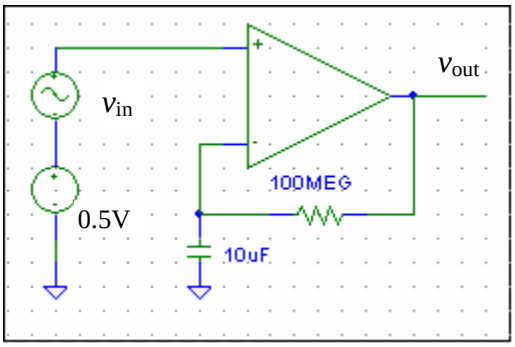
Prob. 24.22 [Ravindra P]
Using the nominal sizes from Table 9.2 and the bias circuit in Fig. 20.47, simulate using a .op analysis, the operation of the op-amp in Fig. 24.58 in the configuration seen in Fig. 24.9. What is the current flowing in M7 and M8 when VDD is 1V? Is 1.2V?

Soln.

The op-amp in Fig. 24.58 is a NMOS diff amp driving an inverter.



The op-amp is operated in the following configuration. The feedback resistor [10MEG] and the capacitor [100uF] form a large time constant such that none of the AC output voltage is fed back to the inverting input. The DC bias level is fed back so that the op-amp biases correctly [i.e. all MOSFET's are operating in saturation].



Operating Point Analysis

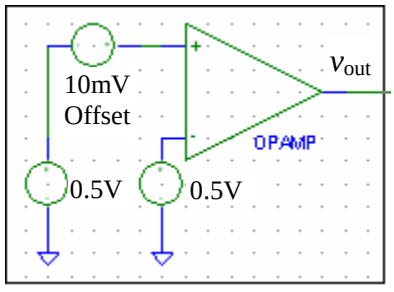
vd1	= 0.65
vout	= 0.512
vout1	= 0.49
vm	= 0.49
vp	= 0.5
vss	= 0.12
v7#branch	= 71 µA
v8#branch	= 71 µA
v3#branch	= 9.5µA
vdd	= 1
vdd#branch	= -200 µA
vhigh	= 0.78
vlow	= 0.15
vbias1	= 0.64
vbias2	= 0.36
vbias3	= 0.54
vbias4	= 0.36
vncas	= 0.8
vpcas	= 0.2
vp#branch	= -0.23e-10

Operation

Using an .op analysis we can analyze the issues with the operation of this op-amp. When both the inverting and non-inverting inputs are at 0.5V,

Current through diff-amp = 10 µA
Current through M7/M8 = 12 µA

When we have an input-referred offset of 10mv [simulated by adding a 10mv DC source to V_p]

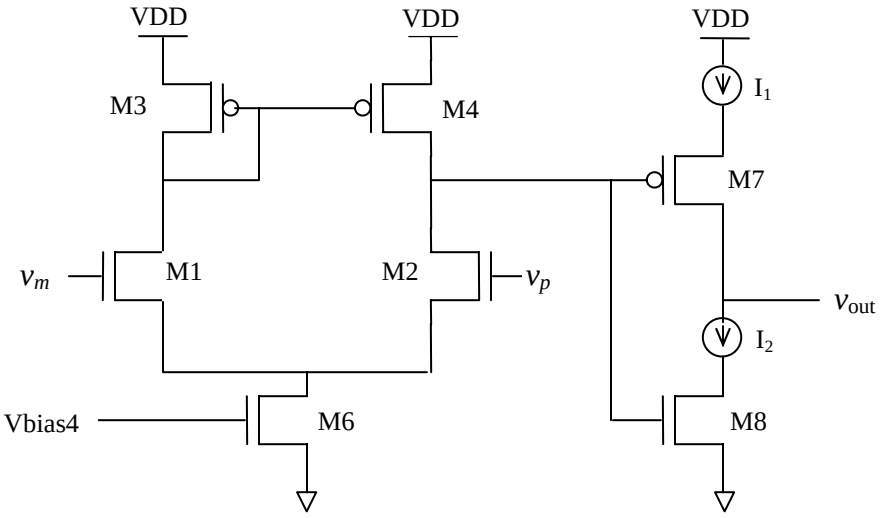


Current through diff-amp = 10 µA
Current through M7/M8 = 54 µA

We see that the current in M7/M8 has increased around 5 times the current in diff-amp. So we clearly see that the op-amp has a *poor systematic input-referred offset voltage.*

To find the current in M7 and M8, zero volt voltage sources [which act as current ammeters] are inserted in spice. By doing an .op analysis, we can find the currents in M7 and M8 [op-amp in configuration seen in Fig. 24.9 of the material].

When VDD = 1V,
i1 = 71.5 µA
i2 = 71.5 µA
When VDD=1.2V,
i1 = 148.5 µA
i2 = 148.5 µA



We see significant change in the current in M7 and M8 with change in VDD. The current flowing in the push-pull output stage is not set by a bias circuit. So it *varies significantly with process, temperature and power supply variations*. Here we see a significant variation of 77 µA in the currents with a 200mV change in power supply.

NETLIST

```
.control
destroy all
run
let i1= - V7#BRANCH
let i2= - V8#BRANCH
PRINT i1 i2
PRINT V3#BRANCH
.endc

.option scale=50n ITL1=300

.op

VDD     VDD     0       DC      1
Vp      Vp      0       DC      0.5     AC      1
Rbig    vout    vm      10MEG
Cbig    vm      0       100u

M1      vd1     vm      vss     0       NMOS L=2 W=50
M2      vout1   vp      vss     0       NMOS L=2 W=50
M3      vd1     vd1     VD3     VDD     PMOS L=2 W=100
V3      VDD     VD3     0
M4      vout1   vd1     VDD     VDD     PMOS L=2 W=100
M6      Vss     Vbias4  0       0       NMOS L=2 W=100

v7      vdd     vd7     0
M7      vout    Vout1   vd7     VDD     PMOS L=2 W=100
v8      vout    vd8     0
M8      vD8     vout1   0       0       NMOS L=2 W=50
Xbias   VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1     Vbias3  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP2     Vbias4  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP3     vp1     vp2     VDD     VDD     PMOS L=2 W=100
MP4     vp2     Vbias2  vp1     VDD     PMOS L=2 W=100
MP5     Vpcas   Vpcas   vp2     VDD     PMOS L=2 W=100
MP6     Vbias2  Vbias2  VDD     VDD     PMOS L=10 W=20
MP7     Vhigh   Vbias1  VDD     VDD     PMOS L=2 W=100
MP8     Vbias1  Vbias2  Vhigh   VDD     PMOS L=2 W=100
MP9     vp3     Vbias1  VDD     VDD     PMOS L=2 W=100
MP10    Vncas   Vbias2  vp3     VDD     PMOS L=2 W=100

MN1     Vbias3  Vbias3  0       0       NMOS L=10 W=10
MN2     Vbias4  Vbias3  Vlow    0       NMOS L=2 W=50
MN3     Vlow    Vbias4  0       0       NMOS L=2 W=50
MN4     Vpcas   Vbias3  vn1     0       NMOS L=2 W=50
MN5     vn1     Vbias4  0       0       NMOS L=2 W=50
MN6     Vbias2  Vbias3  vn2     0       NMOS L=2 W=50
MN7     vn2     Vbias4  0       0       NMOS L=2 W=50
MN8     Vbias1  Vbias3  vn3     0       NMOS L=2 W=50
MN9     vn3     Vbias4  0       0       NMOS L=2 W=50
MN10    Vncas   Vncas   vn4     0       NMOS L=2 W=50
```

```
MN11    vn4     Vbias3  vn5     0       NMOS L=2 W=50
MN12    vn5     vn4     0       0       NMOS L=2 W=50
MBM1    Vbiasn  Vbiasn  0       0       NMOS L=2 W=50
MBM2    Vreg    Vreg    Vr      0       NMOS L=2 W=200
MBM3    Vbiasn  Vbiasp  VDD     VDD     PMOS L=2 W=100
MBM4    Vreg    Vbiasp  VDD     VDD     PMOS L=2 W=100

Rbias   Vr      0       5.5k

*amplifier
MA1     Vamp    Vreg    0       0       NMOS L=2 W=50
MA2     Vbiasp  Vbiasn  0       0       NMOS L=2 W=50
MA3     Vamp    Vamp    VDD     VDD     PMOS L=2 W=100
MA4     Vbiasp  Vamp    VDD     VDD     PMOS L=2 W=100

MCP     VDD     Vbiasp  VDD     VDD     PMOS L=100 W=100

*start-up stuff
MSU1    Vsur    Vbiasn  0       0       NMOS L=2   W=50
MSU2    Vsur    Vsur    VDD     VDD     PMOS L=20  W=10
MSU3    Vbiasp  Vsur    Vbiasn  0       NMOS L=1   W=10

.ends


* BSIM4 models
----------------------

.end
```

Problem 24.23 Roger Porter

When the circuit in *Figure 24.59* is simulated with unity feedback and the .op analysis, M7 and M8 have the following currents.

VDD = 1
Current in M7 = 3.19uA
Current in M8 = 3.19uA

VDD = 1.2
Current in M7 = 16.6uA
Current in M8 = 16.6uA

As can be seen, the current changes considerably with variations in VDD. This is because the current in the output stage isn't being controlled.

When VDD = 1, the gate of M8 is at a value that is being set by the source follower and the level-shifter mosfets. The source follower wants that node to be at a value of a V_{GS} drop below the value of the drain of M2. The drain of M2 is ideally at the same value as the drain(and gate) of M1. The value of the drain of M1 is a V_{SG} drop below VDD. For the biasing conditions of Table 9.2 this is VDD-350mV = 650mV. If the gate of the source-follower is at 650mV then the gate of M8 should be a V_{GS} drop below this value, 650 mV –350mV = 300mV. This is above the threshold voltage of M8 but is below the desired V_{GS} for M8 (350mV). If the source follower is not in its own well then we can expect the body effect to cause its V_{GS} to be more than 350mV. Another issue with this node voltage is that it is considerably higher than the V_{DSsat} for the level shifter and since its output resistance is finite, it is going to sink slightly more current than 10uA. The current that goes through the level-shifter must also go through the source-follower, leading to a slight increase in the V_{GS} of the source follower. This means that the drain of M2 will be slightly higher than the drain of M1. For M1 and M2 to have the same current, the gate and/or drain of M1 will need to increase slightly. When we simulate this circuit, both increase a little. This causes there to be an input referred offset.

Lets look at the simulated values.

WinSpice 203 -> print vp vm d1 d2 g8 vout
vp = 5.000000e-01
vm = 5.014316e-01
d1 = 6.840346e-01
d2 = 7.114012e-01
g8 = 2.892833e-01

The actual voltage on the gate of M8 (g8) is 0.289 V which is very near the threshold voltage, M8 is barely on. The drain of M2 (d2) is 0.711V which is indeed above VDD-V_{SG} = 0.65 V as we expected. The drain of M1(d1) is 0.684 is also above 0.65 V as we

expected. The gate of M1 is .5014 V, about 1.4 mV above the gate of M2 that is tied to 0.5 V. This is the input-referred offset mentioned above.

To see this offset visually, lets run a DC sweep of the gate of M2 while we tie the gate of M1 to 0.5 V and plot the output voltage.

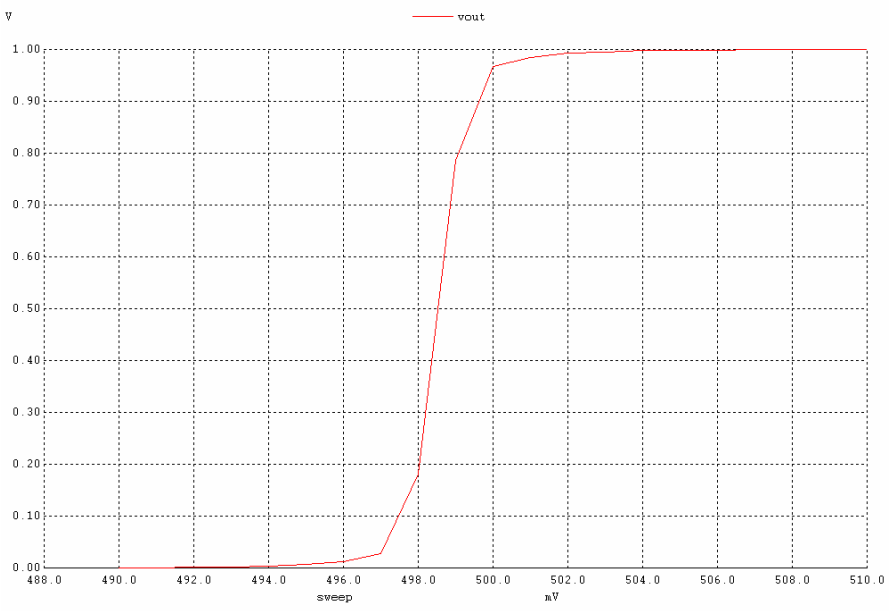


Figure 1 input-referred offset

Since we tied the gate of M1 to 0.5 V, which is opposite of what we did in the .OP analysis the offset is in the other direction. Vout is at 0.5 mV at about 1.4mV before it should be.

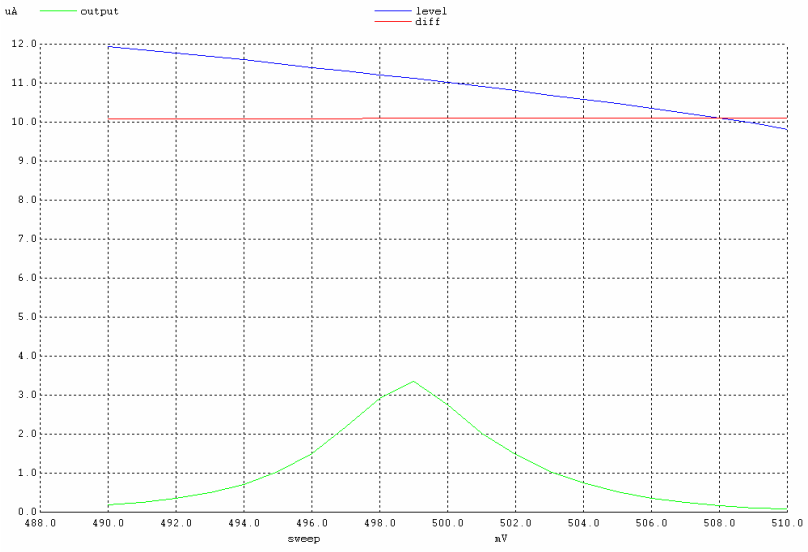


Figure 2 The currents in the op-amp (VDD=1)

When VDD = 1.2, the drains of M1 and M2 will now be near (VDD – V_{SG}) 1.2 – 0.35 = .85 V. The gate of M8 will be near 0.85 – 0.35 = 0.5 V. As in the discussion above for VDD=1, these values will be slightly different than the ideal because of the finite output resistance (and body effect) of the mosfets. Lets look at the simulated values.

WinSpice 223 -> print vp vm d1 d2 g8 vout
vp = 5.000000e-01
vm = 4.970092e-01
d1 = 8.844932e-01
d2 = 8.221796e-01
ds5 = 3.784160e-01
vout = 4.970092e-01

As can be seen the gate of M8 is above the desired V_{GS} of M8 (350 mV) causing more current to flow through the output branch. As stated above, the current through M8 is 16.6uA when VDD=1.2.

Note.
If the source follower is placed in it's own well, the circuit will improve and the offset will be reduced. The simulation results for this case are shown below (VDD=1)

print vp vm d1 d2 g8 I(vm6) I(vm5b) I(vm8)
vp = 5.000000e-01
vm = 4.995408e-01
d1 = 6.844616e-01
d2 = 6.752027e-01
g8 = 3.243805e-01
vm6#branch = 1.009505e-05
vm5b#branch = 1.141040e-05 (current through the level-shifter and source-follower)
vm8#branch = 6.381320e-06

Now the offset is only about 5 µV. But, the output stage current will still vary greatly with VDD variations.

Problem 24.24: Solution submitted by Jagadeesh Gownipalli

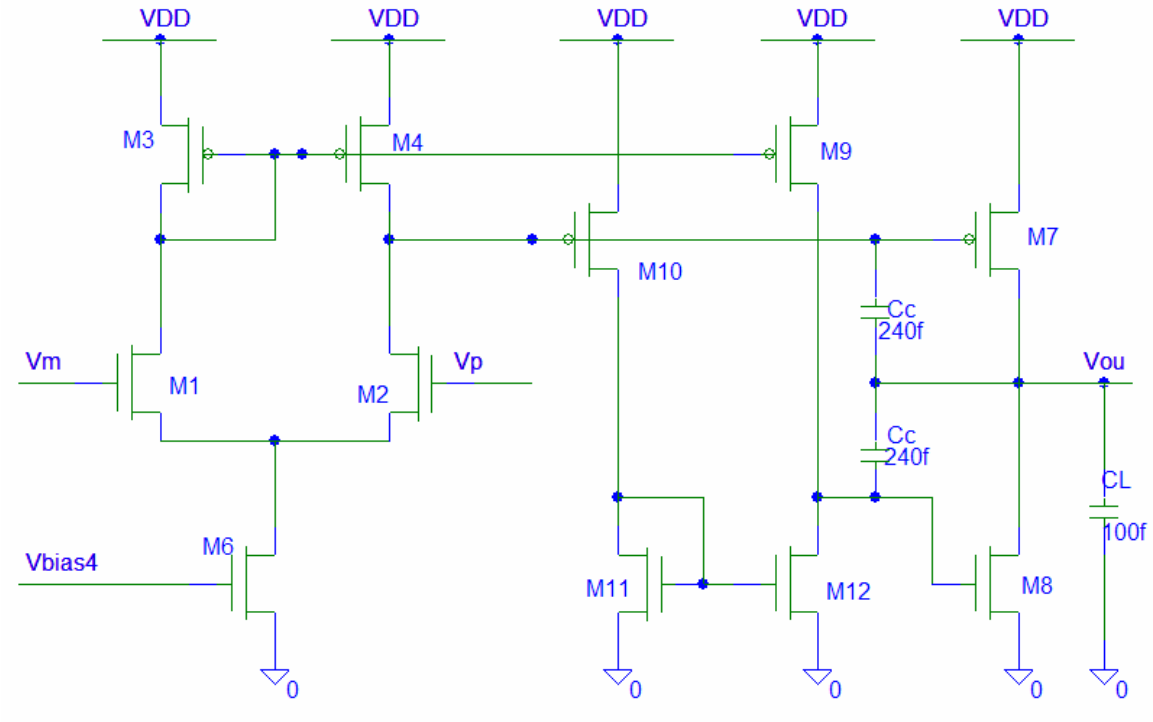


Fig 1 OP-AMP

Fig 1 shown above is Op-Amp shown in Fig 24.60 of the text book with compensated capacitors Cc , compensated capacitors are added from vout to two high impedance nodes vd12 and vd4.

Open Loop Frequency Response:

Resistance seen across first stage I.e. drain of M4 is $R_1 = r_{op4} \parallel r_{on2}$

Resistance seen across second stage I.e. drain of M12 is $R_2 = r_{on9} \parallel r_{op12}$

Resistance seen across second stage I.e. drain of M7 is $R_3 = r_{on8} \parallel r_{op7}$

Since M7 and M8 have 3 times the width of normal NMOS and PMOS

$$R_3 = \frac{r_{on}}{3} \parallel \frac{r_{op}}{3}$$ and $g_{m7}=g_{m8}=3.g_m$

$A_{OLDC} = A1 .A2 . A3$

Where A_1 = Gain of first stage(Diff amp) = $g_{m1} . R_1$

A_2 = Gain of second stage = $g_m . R_2$

A_3 = Gain of (Class AB) push pull amp) = $(g_{m7} + g_{m8}) . R_3$

Therefore open loop Dc gain A_{OLDC} of Op-Amp is

$$A_{OLDC} = g_{m1} . R_1 . g_m . R_2 .(g_{m7} + g_{m8}) . R_3$$

Since M7 and M8 are 300/2 and 150/2 devices(3 times the width)

R_1=111K ohms , R_2=111K, R_3=37K ohms, $g_{m7}=g_{m8}=3.g_m$=450uA/V and g_{m1}=150uA/V

Therefore

A_{OLDC} = 9231 V/V (79.3 dB)

And unit unity-gain frequency f_{un} is

$f_{un} = g_m/2.\pi.Cc$ =100Meg Hz.

From simulations both gain and f_{un} are verified with hand caluculations and phase margin is about 50 degrees.

Simulations:
Spice file

```
*** Problem 24.24 CMOS: Circuit Design, Layout, and Simulation ***

.control
destroy all
run
plot i(vdd)
plot vout vin
.endc

.option scale=50n ITL1=300 reltol=1u abstol=1p
.tran 1n 600n 500n 1n UIC

VDD    VDD    0      DC     1.2
Vin    Vin    0      DC     0      PULSE 100m 900m     510n 1n 1n 40n
Vcm    Vcm    0      DC     0.5

Xo     VDD    vout   vcm    vm     opamp
Rf     Vout   vm     10k
Rin    Vin    vm     10k
CL     vout   0      100f

.subckt opamp VDD vout vp vm
Xbias  VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias
M3     vd3    vd3    VDD    VDD    PMOS L=2 W=100
M4     vd4    vd3    VDD    VDD    PMOS L=2 W=100
M1     vd3    vm     vs12   0      NMOS L=2 W=50
M2     vd4    vp     vs12   0      NMOS L=2 W=50
M6     vs12   vbias4 0      0      NMOS L=2 W=100

M10    vd10   vd4    VDD    VDD    PMOS L=2 W=100
M11    vd10   vd10   0      0      NMOS L=2 W=50
M9     vd12   vd3    VDD    VDD    PMOS L=2 W=100
M12    vd12   vd10   0      0      NMOS L=2 W=50

M7     Vout   Vd4    VDD    VDD    PMOS L=2 W=300
M8     Vout   vd12   0      0      NMOS L=2 W=150

Cc1    Vout   vd4    240f
```

```
Cc2    Vout   vd12   240f
.ends


.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1    Vbias3 Vbiasp VDD    VDD    PMOS L=2 W=100
MP2    Vbias4 Vbiasp        VDD    VDD    PMOS L=2 W=100
MP3    vp1    vp2    VDD    VDD    PMOS L=2 W=100
MP4    vp2    Vbias2 vp1    VDD    PMOS L=2 W=100
MP5    Vpcas  Vpcas  vp2    VDD    PMOS L=2 W=100
MP6    Vbias2 Vbias2 VDD    VDD    PMOS L=10 W=20
MP7    Vhigh  Vbias1 VDD    VDD    PMOS L=2 W=100
MP8    Vbias1 Vbias2 Vhigh  VDD    PMOS L=2 W=100
MP9    vp3    Vbias1 VDD    VDD    PMOS L=2 W=100
MP10   Vncas  Vbias2 vp3    VDD    PMOS L=2 W=100

MN1    Vbias3 Vbias3 0      0      NMOS L=10 W=10
MN2    Vbias4 Vbias3 Vlow   0      NMOS L=2 W=50
MN3    Vlow   Vbias4 0      0      NMOS L=2 W=50
MN4    Vpcas  Vbias3 vn1    0      NMOS L=2 W=50
MN5    vn1    Vbias4 0      0      NMOS L=2 W=50
MN6    Vbias2 Vbias3 vn2    0      NMOS L=2 W=50
MN7    vn2    Vbias4 0      0      NMOS L=2 W=50
MN8    Vbias1 Vbias3 vn3    0      NMOS L=2 W=50
MN9    vn3    Vbias4 0      0      NMOS L=2 W=50
MN10   Vncas  Vncas  vn4    0      NMOS L=2 W=50
MN11   vn4    Vbias3 vn5    0      NMOS L=2 W=50
MN12   vn5    vn4    0      0      NMOS L=2 W=50

MBM1   Vbiasn Vbiasn 0      0      NMOS L=2 W=50
MBM2   Vreg   Vreg   Vr     0      NMOS L=2 W=200
MBM3   Vbiasn Vbiasp VDD    VDD    PMOS L=2 W=100
MBM4   Vreg   Vbiasp VDD    VDD    PMOS L=2 W=100

Rbias  Vr     0      5.5k

*amplifier
MA1    Vamp   Vreg   0      0      NMOS L=2 W=50
MA2    Vbiasp Vbiasn 0      0      NMOS L=2 W=50
MA3    Vamp   Vamp   VDD    VDD    PMOS L=2 W=100
MA4    Vbiasp Vamp   VDD    VDD    PMOS L=2 W=100

MCP    VDD    Vbiasp VDD    VDD    PMOS L=100 W=100

*start-up stuff
MSU1   Vsur   Vbiasn 0      0      NMOS L=2   W=50
MSU2   Vsur   Vsur   VDD    VDD    PMOS L=20  W=10
MSU3   Vbiasp Vsur   Vbiasn 0      NMOS L=1   W=10

.ends
```

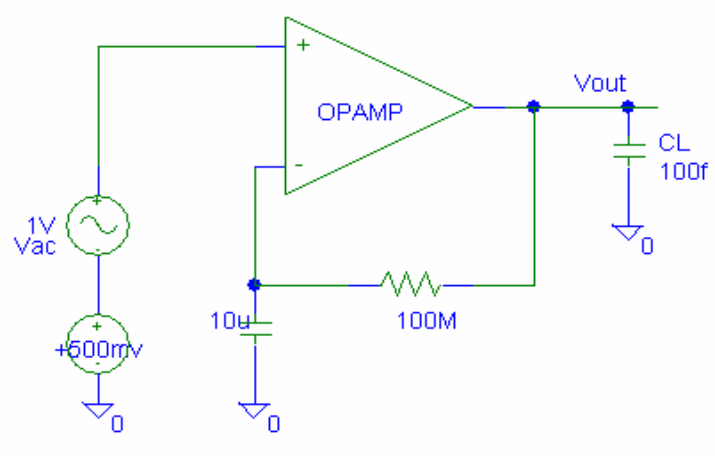


Fig 2 Open Loop Response

Fig 2 shows the open loop response of OP-Amp configuration used to calculate A_{OLDC}. Hand caluculated values for A_{OLDC} and f_{un} are verified from Fig 3.

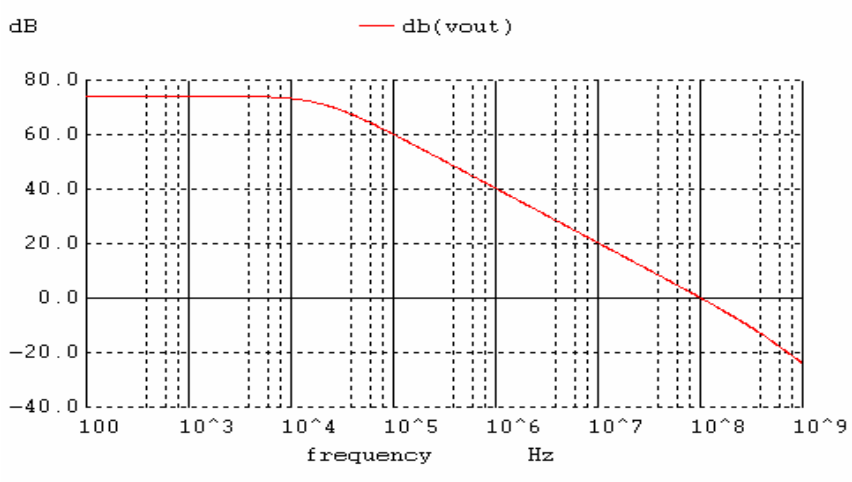


Fig 3 Open Loop Response of Fig2

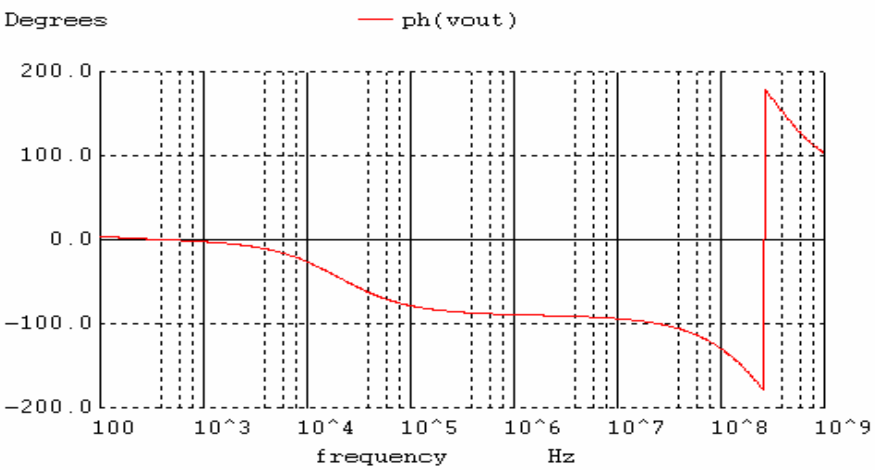


Fig 4 Phase Response of Fig 2

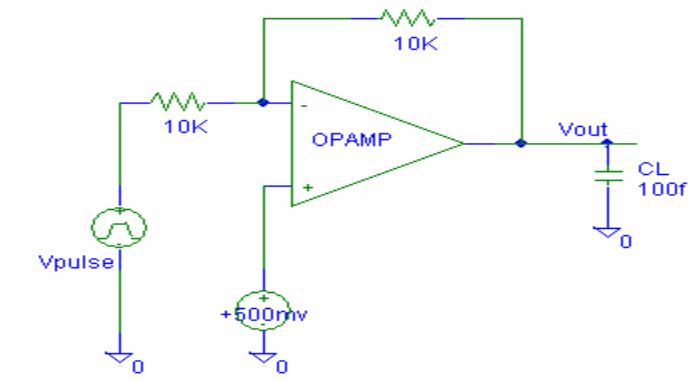


Fig 5 Step Response of OP-AMP driving 100fF

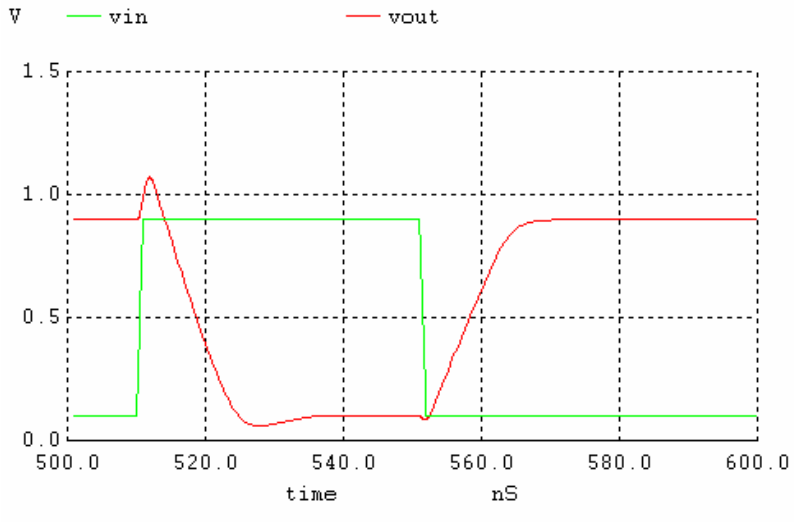


Fig 6 Step Reponse of OP-AMP

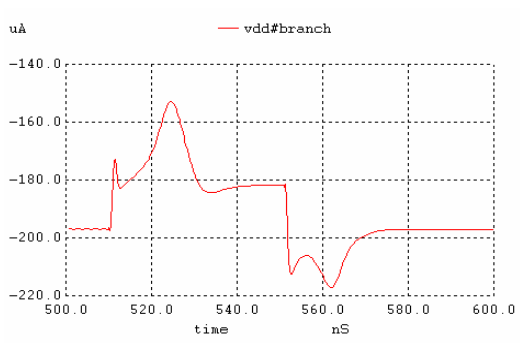


Fig 7 Current pulled from VDD for VDD=1V

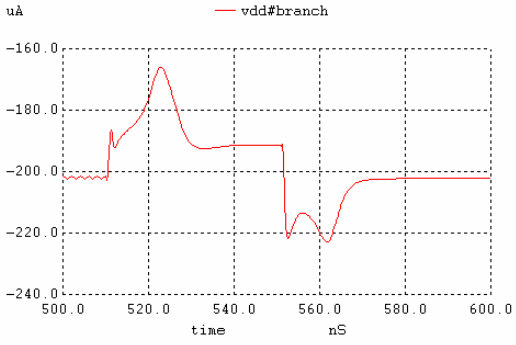


Fig 8 Current pulled from VDD for VDD=1.2V

From Fig 7 and Fig 8 it shows that current pulled from VDD for 1V and for 1.2V are relatively constant(about 4uA difference)

Problem 24.25 Submitted by: Motheeswara Salla (Morty)

Replace the common source output stage in the op-amp of fig 24.61 with a class AB output stage like the one seen in fig24.60. Simulate the operation of the amplifier (Ac and Transient)

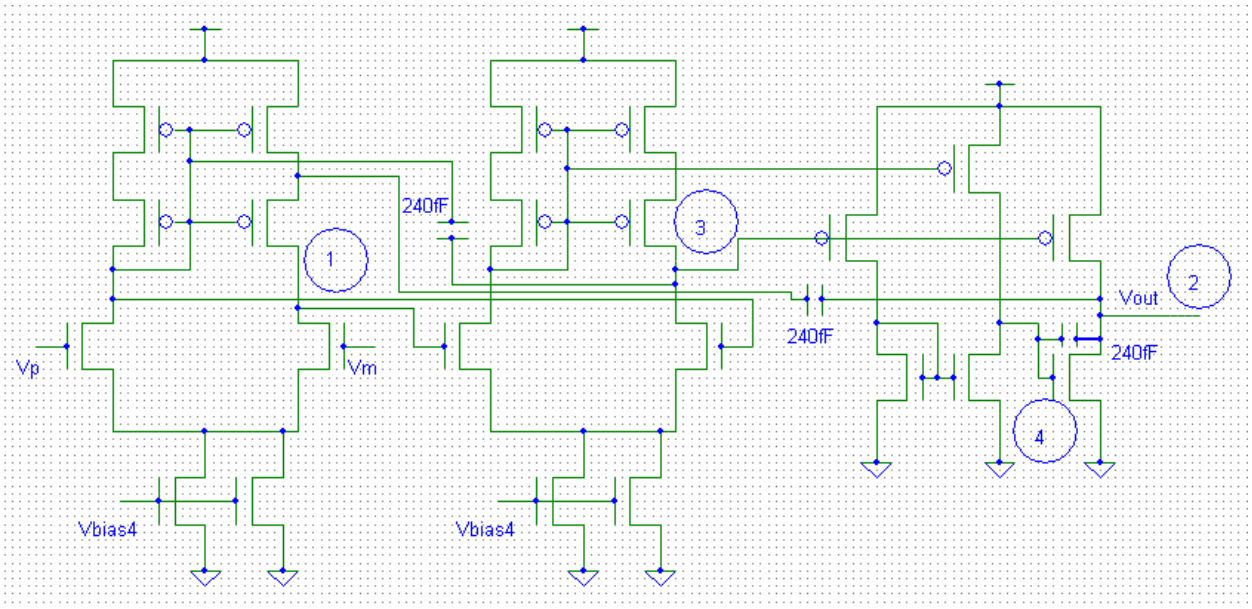


Figure 1

Figure 24.61 is modified and a class AB stage is added as shown in figure 1. The simulation results are given below

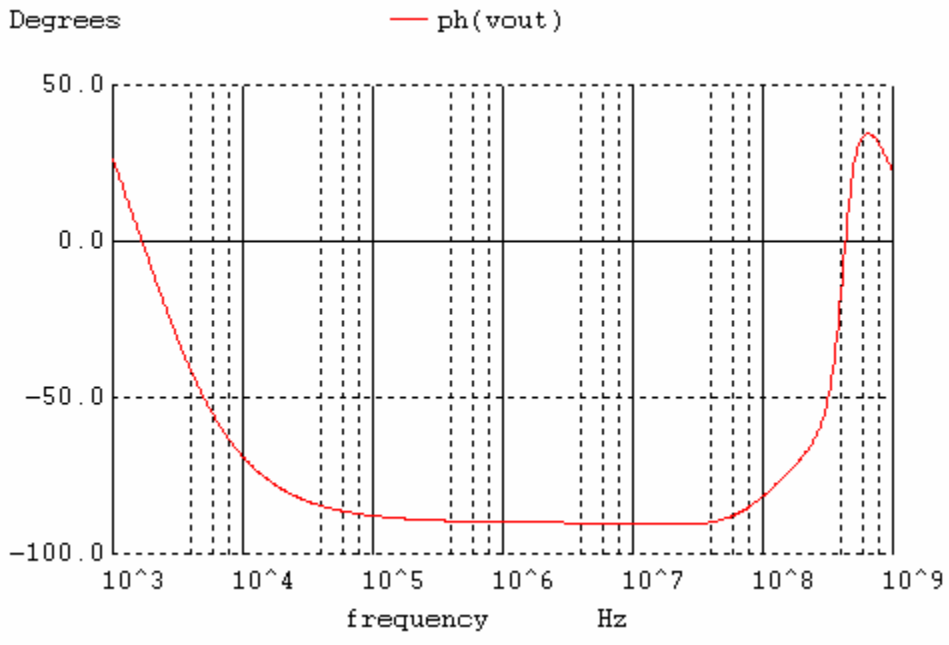


Figure 2

The phase response of Figure 1 is apparently not good. The above response is a program issue. We have a small R_{big} resistance which is connected to V_m. The resistance is very small

which interfered with output resistance and caused a parasitic zero. When R_{big} and C_{big} are modified to 100Meg and 100uF, the response looked like the one shown in figure 3. Please note that at this time there is no compensation capacitance added to node 4.

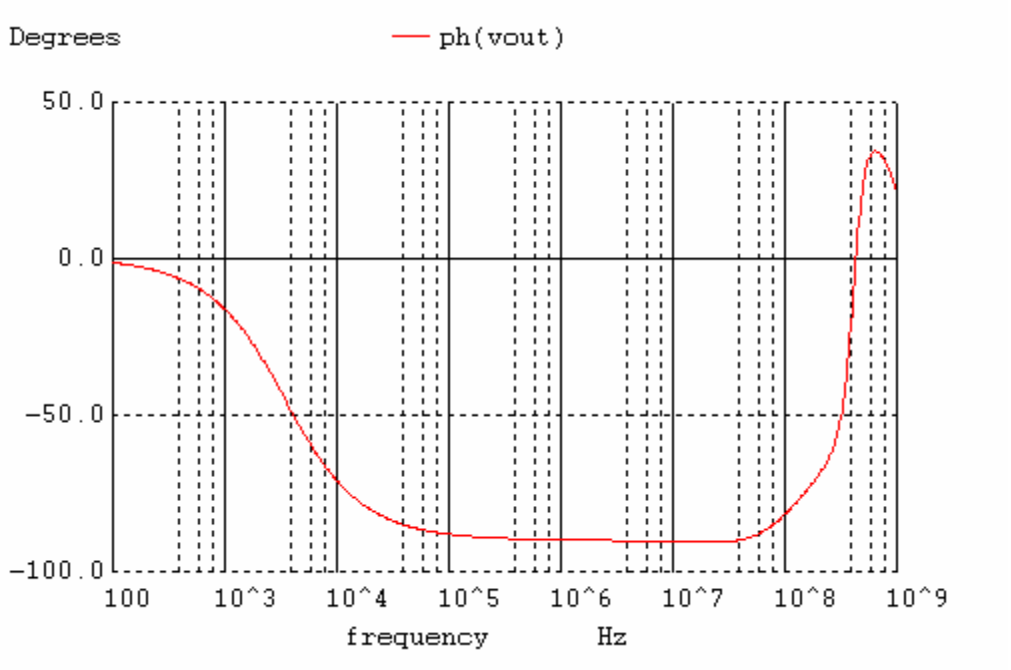


Figure 3: Phase response with no compensation capacitance at node 4

There is an unwanted pole added by high impedance node 4. So it needs to be compensated. A 240fF cap is added at node 4 as shown in figure 1 to compensate the pole. The phase and frequency response are shown in figure 4 and 5 respectively.

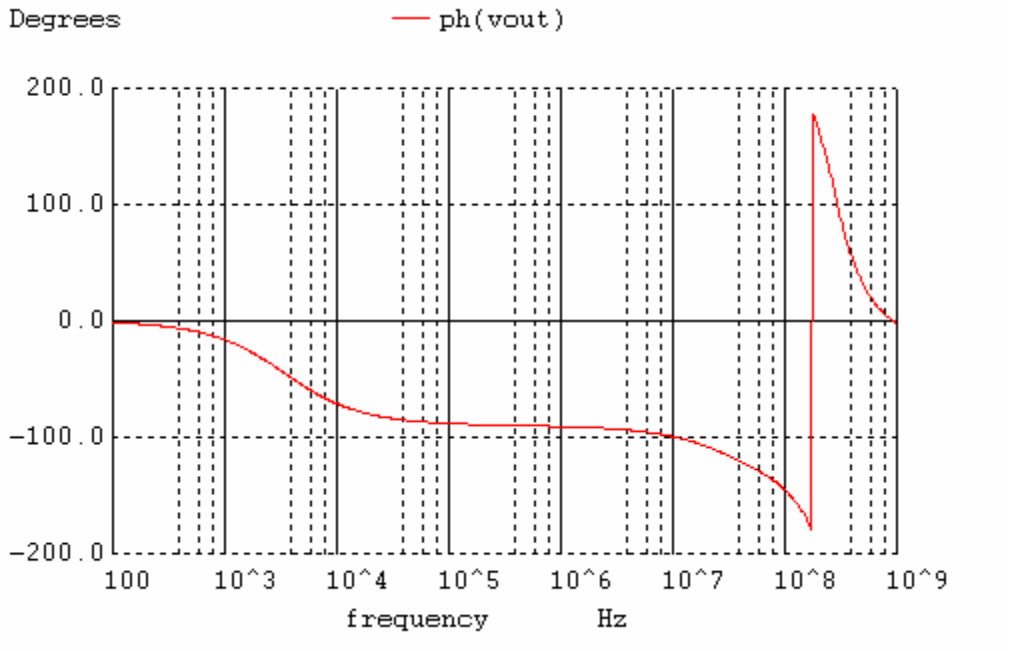


Figure 4

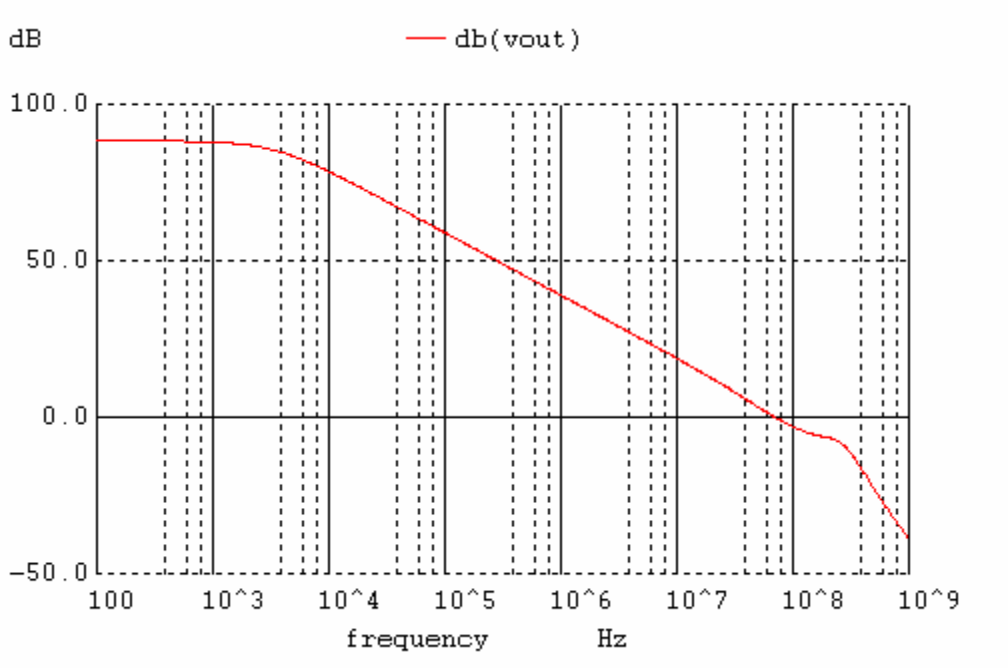


Figure 5

The phase and frequency response looks good. The phase margin and gain margin is not great. The step response may not look so great.

Netlist:

```
*** Figure 1 ***

.control
destroy all
run
set units=degrees
plot ph(vout)
plot db(vout)
.endc

.option scale=50n ITL1=300
.AC dec 100 100 1G


VDD   VDD   0      DC    1

vin   vin   0      DC    0.5   AC    0.5
Rbig  vout  vm     100MEG
Cbig  vm    0      100u

Cc1   n3    n1i    240f
Cc2   vout  vd41   240f
Cc3   vout  dvd09  240f

Xbias  VDD Vbiasn Vbiasp bbias
```

```
M3T1  vd31  n1i    VDD   VDD   PMOS L=1 W=100
M3B1  n1i   n1i    vd31  VDD   PMOS L=1 W=100
M4T1  vd41  n1i    VDD   VDD   PMOS L=1 W=100
M4B1  n1    n1i    vd41  VDD   PMOS L=1 W=100

M3T2  vd32  n3i    VDD   VDD   PMOS L=1 W=100
M3B2  n3i   n3i    vd32  VDD   PMOS L=1 W=100
M4T2  vd42  n3i    VDD   VDD   PMOS L=1 W=100
M4B2  n3    n3i    vd42  VDD   PMOS L=1 W=100



M11   n1i   vm     vs1   0     NMOS L=2 W=50
M21   n1    vin    vs1   0     NMOS L=2 W=50
M6L1  vs1   vbiasn 0     0     NMOS L=2 W=50
M6R1  vs1   vbiasn 0     0     NMOS L=2 W=50

M12   n3i   n1     vs2   0     NMOS L=2 W=50
M22   n3    n1i    vs2   0     NMOS L=2 W=50
M6L2  vs2   vbiasn 0     0     NMOS L=2 W=50
M6R2  vs2   vbiasn 0     0     NMOS L=2 W=50

MAB10I      dvd10i n3    VDD   VDD   PMOS L=1 W=100
MAB09I      dvd09i n3i   VDD   VDD   PMOS L=1 W=100
MAB07I      vouti  n3    VDD   VDD   PMOS L=1 W=100
MAB10       dvd10  n3    dvd10i VDD  PMOS L=1 W=100
MAB09       dvd09  n3i   dvd09i VDD  PMOS L=1 W=100
MAB07       vout   n3    vouti VDD   PMOS L=1 W=100
MAB11       dvd10  dvd10 0     0     NMOS L=2 W=50
MAB12       dvd09  dvd10 0     0     NMOS L=2 W=50
MAB08       vout   dvd09 0     0     NMOS L=2 W=50
```