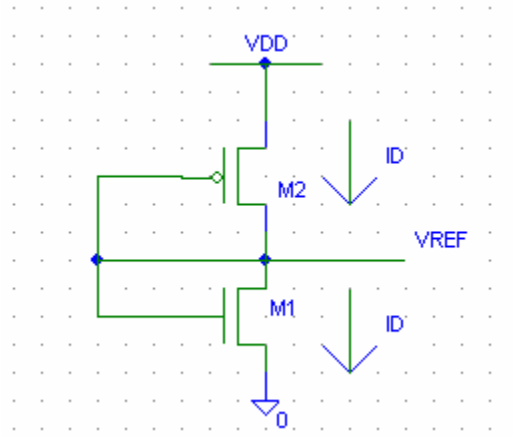P23.1

Figure 1

Above in Figure 1 is the MOSFET only reference from Figure 23.2 in the text.

Since the current through the two MOSFETS is equal, and $v_{GS}=v_{SG}=V_{REF}$ and using equation 9.56.

$$ID = v_{sat} * C_{ox}'*W * (v_{GS} - V_{THN} - v_{DS,Sat}) \quad (9.56)$$

Setting the two currents equal and solving for Wn/Wp gives:

$$\frac{Wn}{Wp} = \frac{v_{satp} * Cox'*(VDD - Vref - Vthp - v_{SD,Sat})}{v_{satn} * Cox'*(Vref - Vthn - v_{DS,Sat})}$$

$$\frac{Wn}{Wp} = \frac{90 * 10^3 * (1 - .5 - .28 - 50 * 10^{-3})}{110 * 10^3 * (.5 - .28 - 50 * 10^{-3})} \approx \frac{80}{100}$$

Using the value of the width of the NMOS calculated above (80) the reference voltage is off by 50uV. Therefore some tweaking of the width of the NMOS was in order. Changing this width to 50 gives the desired reference voltage. The netlist and the plot of the behavior of the MOSFET only reference with variations in VDD and Temperature can be seen below in figure 2.

The behavior with variations in temperature is very good, but the reference voltage varies around 700mV with variations in VDD, when VDD is swept from 0 to 1.5 Volts.
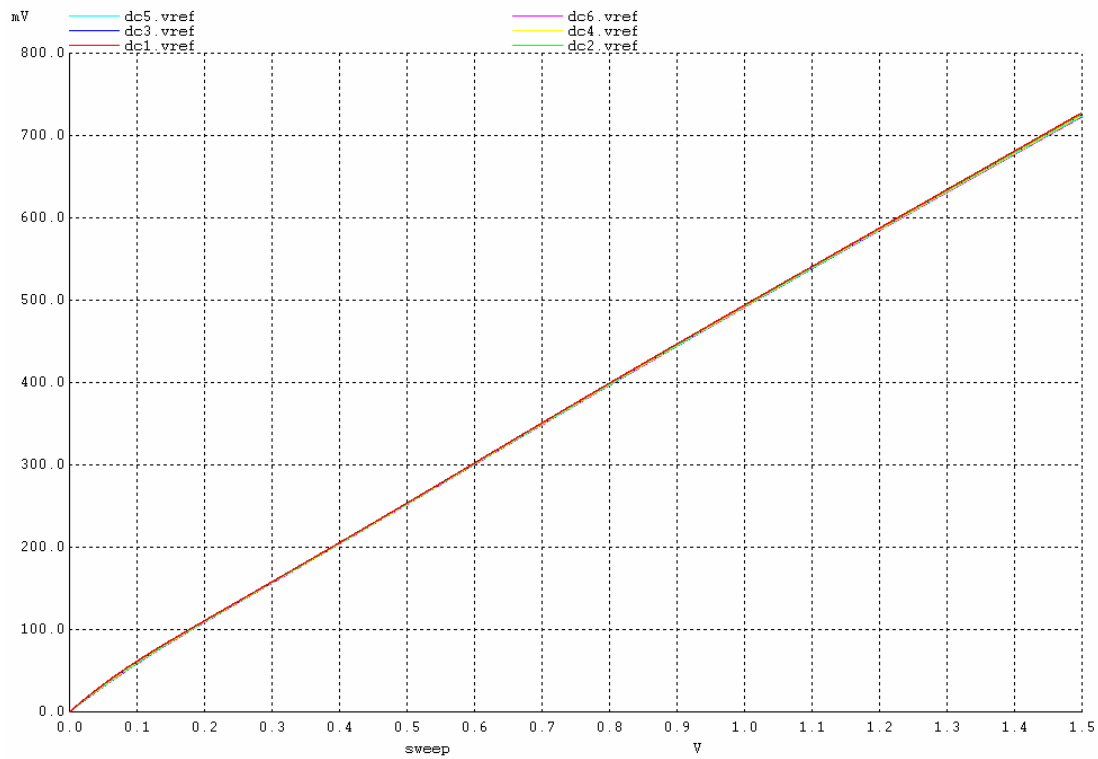
Figure 2.

```
.control
destroy all
set temp=0
run
set temp=25
run
set temp=27
run
set temp=50
run
set temp=75
run
set temp=100
run
plot dc1.vref dc2.vref dc3.vref dc4.vref dc5.vref dc6.vref
.endc

.option scale=50n
.dc VDD 0 1.5 1m

VDD      VDD      0        DC       1
M2       VREF     VREF     VDD      VDD       PMOS L=2 W=100
M1       VREF     VREF     0        0         NMOS L=2 W=50
BSIM4 models
*
* 50nm models from "BPTM
```

Problem 23.2

Using long channel MOSFET parameters, design a 500mV (nominal) voltage reference using the $3V_{THN}$ topology.

A simple derivation proves equation (23.7):

$$V_{REF} = V_{GS}\left(\frac{R_1}{R_2} + 1\right)$$

Knowing that V_{REF} should be half a volt, and that $V_{GS} \approx V_{THN}$ if the width of the NMOS gate is very wide, we have:

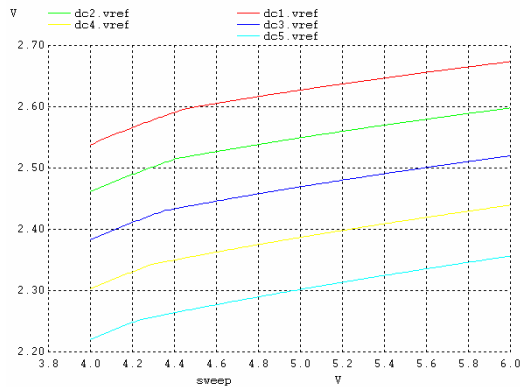$$2.5 = 0.8\left(\frac{R_1}{R_2} + 1\right) \Rightarrow \frac{R_1}{R_2} \approx 2.125$$

The following choices suit the answer given above:

$R_1 = 85k\Omega$
$R_2 = 40k\Omega$
$R = 30k\Omega$

Figure 1: Sensitivity of Reference to Variations in V_{DD} and T

Note that the TC's of R_1 and R_2 do not affect the behavior of the reference because they simply cancel in equation (23.7). Examining Figure 1, we see that:

$$\frac{\partial V_{REF}}{\partial V_{DD}} = \frac{137mV}{2V} = 0.07 \ \ volts \ \ per \ \ volt$$

$$\frac{\partial V_{REF}}{\partial T} = \frac{84mV}{25°C} = 3.36 \times 10^{-3} \ V\!\!\Big/\!_{°C} \Rightarrow TCV_{REF} = 672 \ ppm\!\!\Big/\!_{°C}$$

The netlist is seen below:

```
        *** matt's 23.2 ***

.control
destroy all
*run
*plot vref a
*plot -vdd#branch
set temp=0
run
set temp=25
run
set temp=50
run
set temp=75
run
set temp=100
run
plot dc1.vref dc2.vref dc3.vref dc4.vref dc5.vref
.endc

.option scale=1u

m1      vref  a     0      0     nmos  w=200 l=1
r1      vref  a     85k
r2      a     0     40k
r       vdd   vref  30k

vdd     vdd   0     5

.dc     vdd   4     6      .01

.MODEL NMOS NMOS LEVEL  = 3
+ TOX    = 200E-10         NSUB   = 1E17       GAMMA  = 0.5
+ PHI    = 0.7            VTO    = 0.8        DELTA  = 3.0
+ UO     = 650            ETA    = 3.0E-6     THETA  = 0.1
+ KP     = 120E-6         VMAX   = 1E5        KAPPA  = 0.3
+ RSH    = 0              NFS    = 1E12       TPG    = 1
+ XJ     = 500E-9         LD     = 100E-9
+ CGDO   = 200E-12        CGSO   = 200E-12    CGBO   = 1E-10
+ CJ     = 400E-6         PB     = 1          MJ     = 0.5
+ CJSW   = 300E-12        MJSW   = 0.5
*
.MODEL PMOS PMOS LEVEL  = 3
+ TOX    = 200E-10         NSUB   = 1E17       GAMMA  = 0.6
+ PHI    = 0.7            VTO    = -0.9       DELTA  = 0.1
+ UO     = 250            ETA    = 0          THETA  = 0.1
+ KP     = 40E-6          VMAX   = 5E4        KAPPA  = 1
+ RSH    = 0              NFS    = 1E12       TPG    = -1
+ XJ     = 500E-9         LD     = 100E-9
+ CGDO   = 200E-12        CGSO   = 200E-12    CGBO   = 1E-10
+ CJ     = 400E-6         PB     = 1          MJ     = 0.5
+ CJSW   = 300E-12        MJSW   = 0.5

.end
```

Problem 23.3:

Suppose it was desired in Fig. 23.7 to make M1 and M2 the same size. However, to increase the gate-source voltage of M1, relative to M2, the width of M3 is increased by K. How do the equations governing the operation of the BMR change? How does the current flowing in the BMR change?

Solution:

W/L,4 = KW/L,3.

Let the current flowing in the M2/M4 side be I_D so the current flowing in M3/M1 is KI_D. By KVL we have

$$V_{GS,1} = V_{GS,2} + RI_D \qquad (1)$$

Also, by the square law equation for saturation we have

$$V_{GS,1} = \sqrt{\frac{2I_D K}{\beta}} + V_{THN} \qquad (2)$$

and

$$V_{GS,2} = \sqrt{\frac{2I_D}{\beta}} + V_{THN} \qquad (3)$$
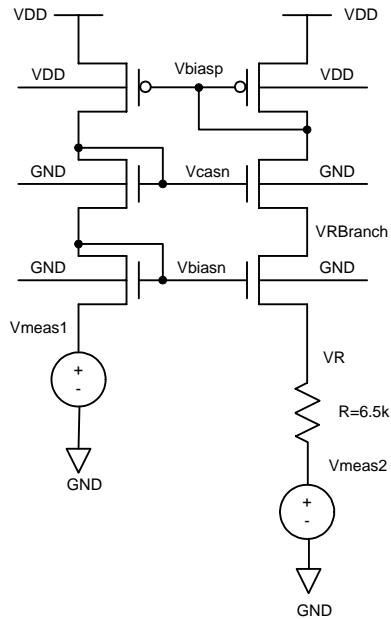
Plugging (2) and (3) into (1) we find

$$\sqrt{\frac{2I_D K}{\beta}} + V_{THN} = \sqrt{\frac{2I_D}{\beta}} + V_{THN} + RI_D$$

$$\sqrt{\frac{2I_D K}{\beta}} - \sqrt{\frac{2I_D}{\beta}} = RI_D$$

$$\frac{1}{R}\sqrt{\frac{2I_D}{\beta}}\left(\sqrt{K} - 1\right) = I_D$$

$$I_D^2 = \frac{2I_D}{R^2\beta}\left(\sqrt{K} - 1\right)^2$$

Dividing out I_D we find that the current flowing through M2 is

$$I_D = \frac{2}{R^2\beta}\left(\sqrt{K} - 1\right)^2$$

This can be then used to find V_{REF}.

23.4) The modified current Beta Multiplier is shown below. The netlist for it follows.


```
.control
destroy all
run
let Iref1=Vmeas1#branch
let Iref2=Vmeas2#branch
plot Iref1 Iref2
plot Vbiasp Vcasn
.endc

.option scale=50n
.dc VDD 0 1.5 1m

VDD VDD 0 DC=1

R0      Vmeas2 Vr    R=6.5k
Vmeas2 Vmeas2 0      dc=0.0
Vmeas1 Vmeas1 0      dc=0.0

MP1 vdd    Vbiasp Vcasn vdd PMOS L=2.0 w=100.0
MP0 Vbiasp Vbiasp vdd   vdd PMOS L=2.0 w=100.0

*Cascode NMOS transistors
MN0 VRBranch Vcasn Vbiasp 0 NMOS L=2.0 W=50.0
MN2 Vbiasn    Vcasn Vcasn  0 NMOS L=2.0 W=50.0

*NMOS Bias Voltage Generator
MN1 Vr      Vbiasn VRBranch 0 NMOS l=2.0 w=200.0
MN3 Vmeas1 Vbiasn Vbiasn    0 NMOS l=2.0 w=50.0

*Start Up Circuit
MSU1 Vsur    Vbiasn  0       0    NMOS L=2    W=50
MSU2 Vsur    Vsur    VDD     VDD PMOS L=20   W=10
MSU3 Vbiasp Vsur    Vbiasn 0    NMOS L=1    W=10
```
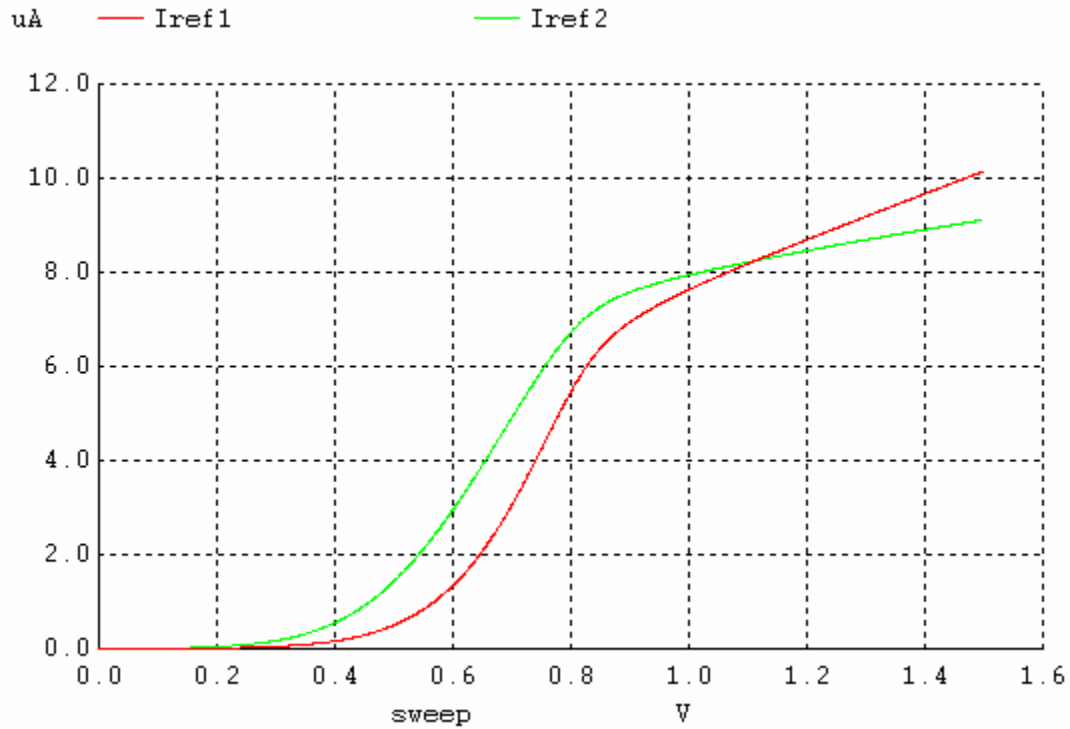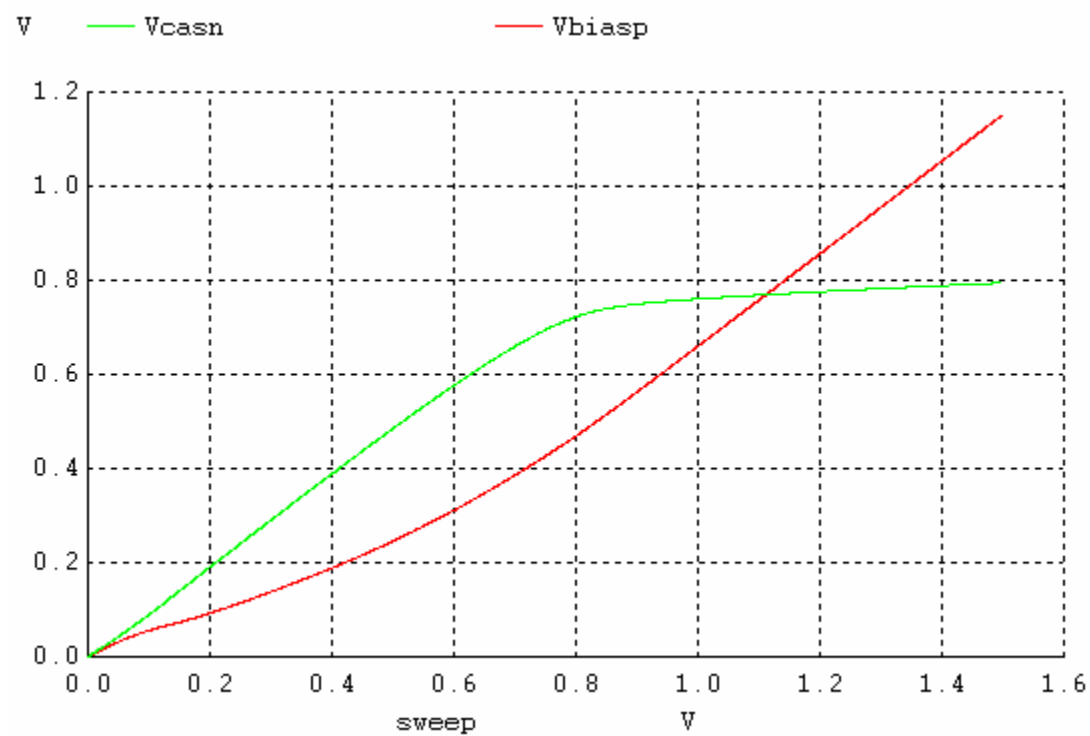
```
.end
```

Note that the transistor models were not included since they are same for every other circuit. Simulating the above circuits yields the following figure.

As expected the currents are not equal since the drain source voltages of the PMOSs are not the same. This is shown in the next figure.

Solution for Problem 23.5

For Short channel process for figure 23.13 Beta-Multiplier circuit

$$I_D = I_{REF} = v_{sat}.c_{ox}'.w(V_{GS} - V_{THN} - V_{DSSAT})$$

V_{REF} of BMR of shot channel process is

$$V_{REF} = V_{GS2} + I_{REF}.R \text{ ---------------------(1)}$$

where $V_{GS2} = \dfrac{I_{REF}}{v_{sat}.c_{ox}'.k.w} + V_{THN} + V_{DSSAT}$ and $V_{REF} = \dfrac{I_{REF}}{v_{sat}.c_{ox}'.w} + V_{THN} + V_{DSSAT}$

Solving above equation we get

$$R = \frac{1}{g_m}(1 - \frac{1}{k})$$

using Table 9.2 and k=4 we get R=5K ohms.

Since $V_{REF}=V_{GS1}$ therefore

$$V_{REF} = \frac{I_{REF}}{v_{sat}.c_{ox}'.w} + V_{THN} + V_{DSSAT}$$

and I_{REF} is independent of Resistor.

Therefore V_{REF} is independent of TCR since I_{REF} independent of Resistor. TCV_{REF} is only dependent on threshold voltage $V_{THN.}$

Therefore TCR of BMR is zero.

Net list
*** Problem 23.5 CMOS: Circuit Design, Layout, and Simulation ***

```
.control
destroy all
set temp=0
run
set temp=25
run
set temp=50
run
set temp=75
run
set temp=100
run
plot dc1.i(vdd) dc2.i(vdd) dc3.i(vdd) dc4.i(vdd) dc5.i(vdd)
plot dc1.vref dc2.vref dc3.vref dc4.vref dc5.vref
.endc

.option scale=50n
.dc VDD 0 1.2 1m

VDD      VDD     0       DC      1

M1       Vbiasn  Vbiasn  0       0         NMOS L=2 W=10
M2       Vref    Vref    Vr      0         NMOS L=2 W=40
M3       Vbiasn  Vbiasp  VDD     VDD       PMOS L=2 W=100
M4       Vref    Vbiasp  VDD     VDD       PMOS L=2 W=100

Rbias    Vr      0       5.0k    Rmod
```
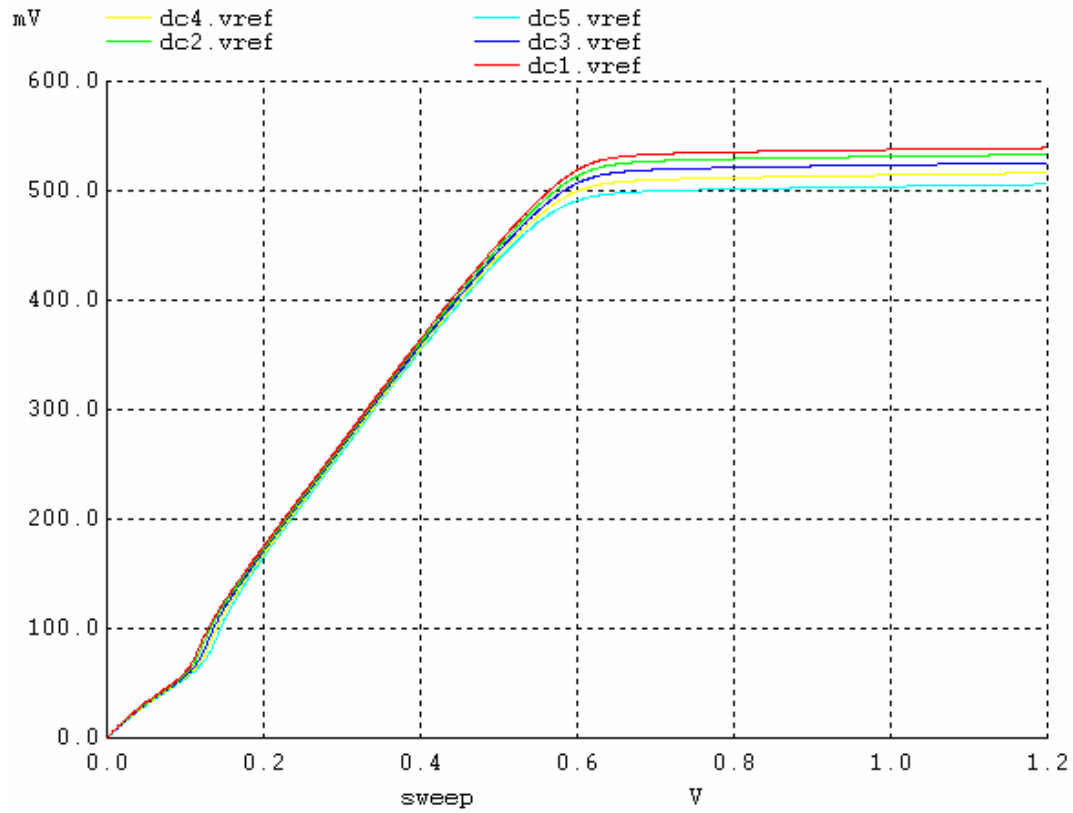
```
.model RMOD R TC1=0.002

*amplifier
MA1      Vamp     Vref     0        0        NMOS L=2 W=10
MA2      Vbiasp   Vbiasn   0        0        NMOS L=2 W=10
MA3      Vamp     Vamp     VDD      VDD      PMOS L=2 W=100
MA4      Vbiasp   Vamp     VDD      VDD      PMOS L=2 W=100

*start-up stuff
MSU1     Vsur     Vbiasn   0        0        NMOS L=2   W=10
MSU2     Vsur     Vsur     VDD      VDD      PMOS L=20  W=10
MSU3     Vbiasp   Vsur     Vbiasn   0        NMOS L=1   W=10
```


Above figure shows the simulation results of Beta multiplier refrence circuit at T=0,25,50,75 and 100°C.

Problem 23.6   **Dennis Montierth**

$R = 5.5K$
$W_1 = W$
$W_2 = K*W_1$ $K = 4$

You can see from the left side of the circuit in Fig. 23.16b that VREF is equal to the gate to source drop of M1. This results because the amplifier feedback holds its inputs at the same voltage. The other important voltage on the right hand side of the circuit is the gate to source drop of M2. The drop across the resistor is therefore equal to $VGS_1 - VGS_2$.

Knowing this I next solve for the current which is equal through both branches.

$ID = (VGS_1 - VGS_2) / R = (2*ID*L/(KP*W*R^2))^{.5} + VTHN / R - (2*ID*L/(KP*K*W*R^2))^{.5} - VTHN / R$

$ID = (2*ID*L/(KP*W*R^2))^{.5} * (1 - 1/K^{.5})$

$ID^2 = (2*ID*L/(KP*W*R^2)) * (1 - 1/K^{.5})^2$

$ID = (2*L/(KP*W*R^2)) * (1 - 1/K^{.5})^2$

Once I have the value of the current and knowing that VGS_1 is equal to V_{REF} I can just write an equation for VGS_1.

$V_{REF} = VGS_1 = (2*ID*L/(KP*W))^{.5} + VTHN$

Next, Plugging ID into this equation:

$V_{REF} = 2L / (W * KP * R) * (1 - 1/K^{.5}) + VTHN$ $K = 4$ and $R = 5.5K$

Next, I will derive the functions that govern how the circuit performs with temperature variation.

$TCV_{REF} = 1 / V_{REF} * dV_{REF}/dT$

$dV_{REF}/dT = dVTHN / dt + 2 * L / W (1-1/K^{.5}) * d / dT (R^{-1} * KP(T)^{-1})$

$dV_{REF}/dT = dVTHN / dt + 2 * L / W (1-1/K^{.5}) * ((-1)R^{-1} * KP(T)^{-2} dKP / dT + (-1)KP(T)^{-1} * R^{-2} dR / dT)$

$dV_{REF}/dT = dVTHN / dt - 2 * L / W (1-1/K^{.5}) * R^{-1} * KP(T)^{-1} (1/KP(T) dKP/dT + 1 / R dR/dT)$

Problem 23.7:

In all CMOS applications, generally the p-substrate is connected to ground. If an n^+ implant in a p-substrate is used as a diode, then to forward bias the diode, it will be required to apply a negative voltage . A charge pump is required to develop the negative voltage , which leads to an increase in the layout area and hence is a practical problem.

Negative
Voltage

n^+

K

A

p-substrate

GND
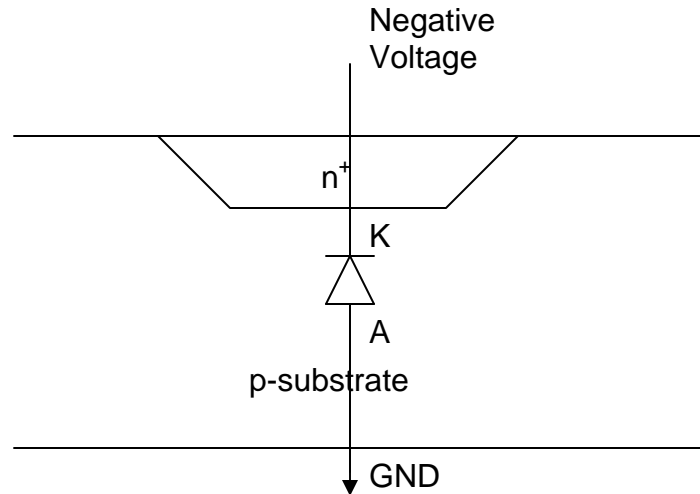
23.8)

The current through a forward biased diode is given by

$$I_D = I_S . e^{V_D / n.V_T} \qquad \text{------------------------} \quad \textbf{(1)}$$

We are given that for $I_D = 1uA$, $V_D = 700mV$.
At room temperature, $V_T = 26mV$

So, we get

$$I_S = \frac{1uA}{e^{26.92 / n}}$$

Given $\dfrac{dV_D}{dT} = -2mV / C$

From Eq. (1), $\dfrac{dV_D}{dT} = n.\dfrac{dV_T}{dT}.\ln\dfrac{I_D}{I_S}$

$$\frac{dV_D}{dT} = n.85\frac{uV}{C}.\ln\frac{1uA}{I_S}$$

This equation is ambiguous because, in reality V_D decreases with increasing temperature. In reality I_S is a function of temperature too. So we do not use this equation. We need to solve Eq. (2) from simulations to get the best value for I_S and n so that we get the desired value for $\dfrac{dV_D}{dT}$
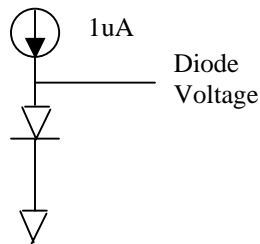
From simulations we see that with n=0.7 and $I_S = 1.5 \times 10^{-23}$, we get $\dfrac{dV_D}{dT} = -1.9mV / C$
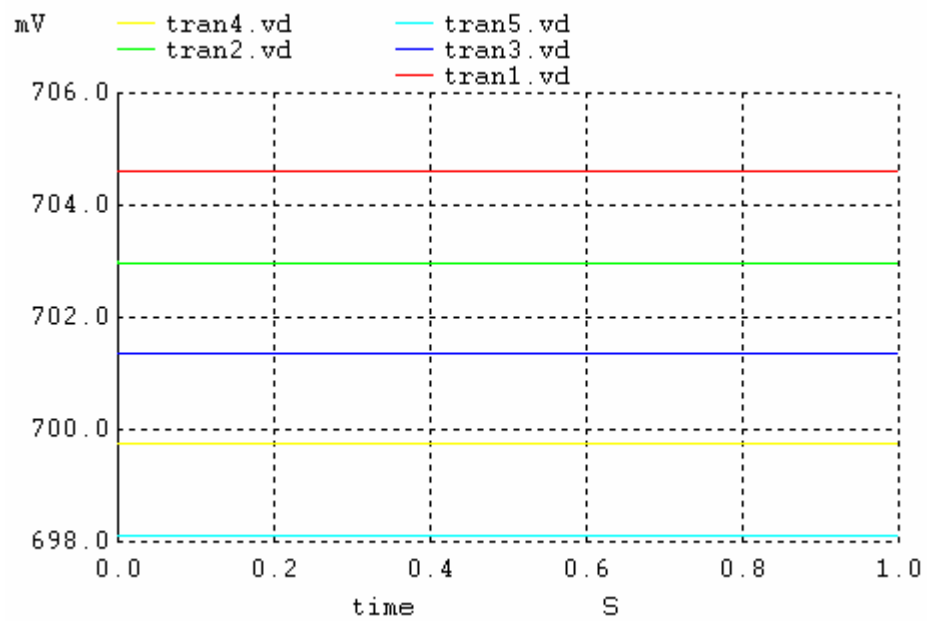
NETLIST

```
.control
destroy all
set temp=25
run
set temp=26
run
set temp=27
run
set temp=28
run
set temp=29
run
plot tran1.vd tran2.vd tran3.vd tran4.vd tran5.vd
.endc

.tran 1m 1

ID       0          VD        DC        1u

D1       VD        0          PNPDIODE

.MODEL        PNPDIODE        D        Is=1.5e-23        n=.7
.end
```

Problem (9).

To generate a SPICE model for Schottky diode as seen in Fig 23.21.

In SPICE the junction diode model can also be used for both junction diodes as well as the Schottky diodes.

The general form of a Schottky diode in WINSPICE is given below:

DXXXXXXX N+ N- MNAME <AREA> <OFF> <IC=VD> <TEMP=T>

where N+, N- are the positive and negative nodes, AREA is the area factor, IC=VD specifies the optional initial condition and T is the operating temperature of the device.
The current and voltage characteristics of Schottky diode generated from a WINSPICE net list is shown below:
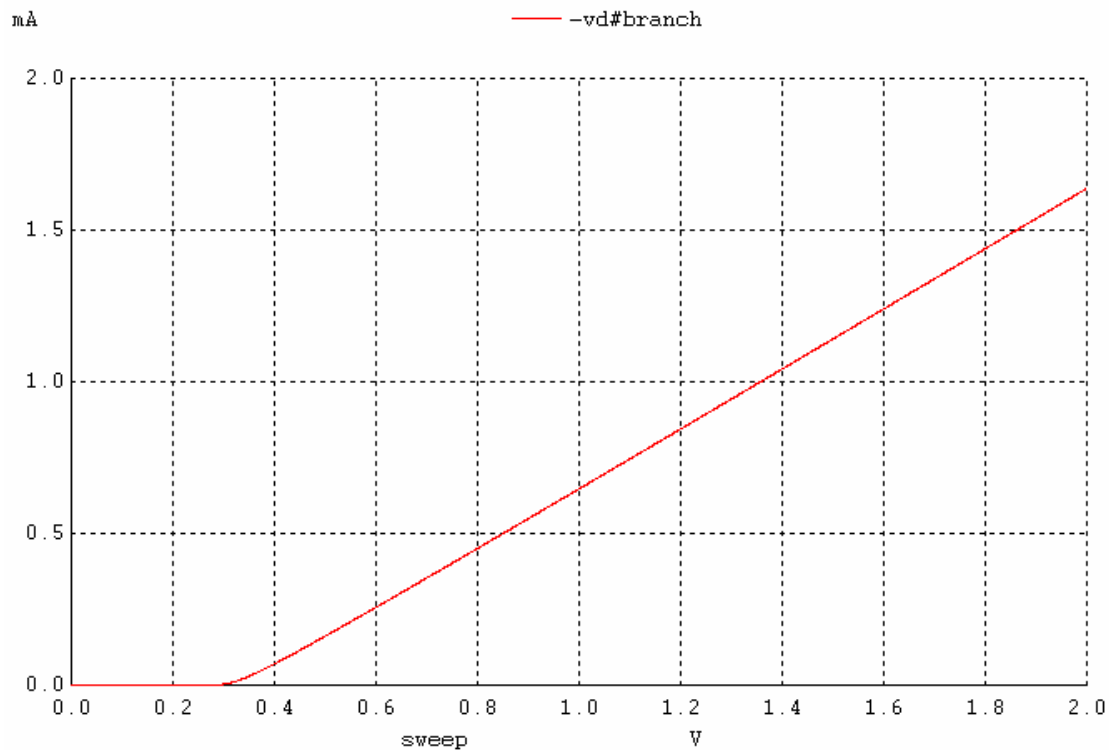
The corresponding net list is shown below:
.control
destroy all
RUN
PLOT (-VD#BRANCH)
.endc
.DC VD 0 2 1m
VD VD 0 DC 0
D1 VD 0 SCHOTTKY
.MODEL SCHOTTKY D IS=1e-18 n=0.4 XTI=2 RS=1K
.end

NOTE: We don't require XTI in generating the DC characteristics of a diode but if we want to model the temperature dependence of the diode's saturation current we require the value of XTI. For a diode the DC characteristics are determined by Is (saturation current) and n, for Schottky the saturation current temperature exponent is generally 2..

Problem 23.10

Start-up circuit not shown.
NMOS are 10/2.
PMOS are 30/2.
Scale factor is 1 micron.
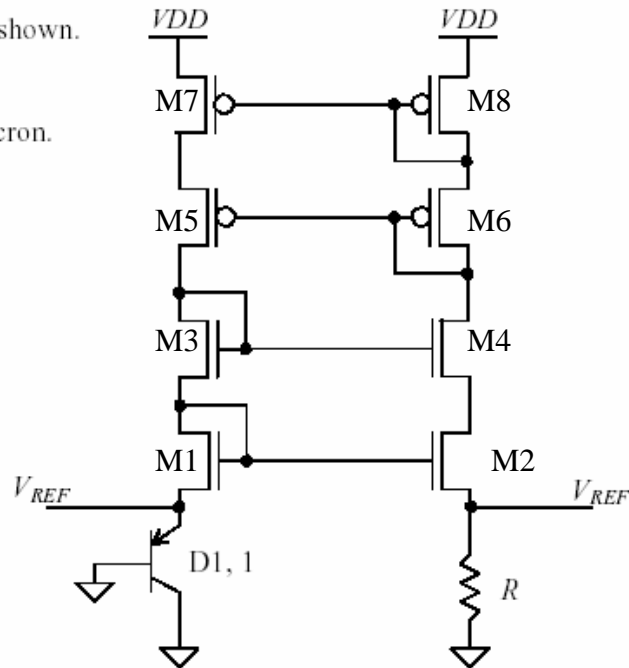
Figure 23.22 Diode-referenced self-biasing circuit.

Assuming the following:

$V_{thn} = .8V$

$V_{thp} = .9V$

$KP_N = 120uA/V^2$

$KP_P = 40uA/V^2$

$V_{fb} = .7V$

Minimun VDD will ensure that all of p-channel and n-channel devices will turn on enough to conduct 1uA current.

Looking at the right side of the circuit:

$$VDD_{min} = Vsg_8 + Vsg_6 + Vds, sat_4 + Vds, sat_2 + Vref$$

$$I_{D6} = \frac{KP_P}{2}\frac{W}{L}\left(Vsg_6 - V_{thp}\right)^2$$

$$1uA = \frac{40uA/V^2}{2}\frac{30}{2}\left(Vsg_6 - .9\right)^2$$

$$Vgs_6 = .9577V = Vgs_8$$

$$I_{D2} = \frac{KP_N}{2}\frac{W}{L}\left(Vgs_2 - V_{thn}\right)$$
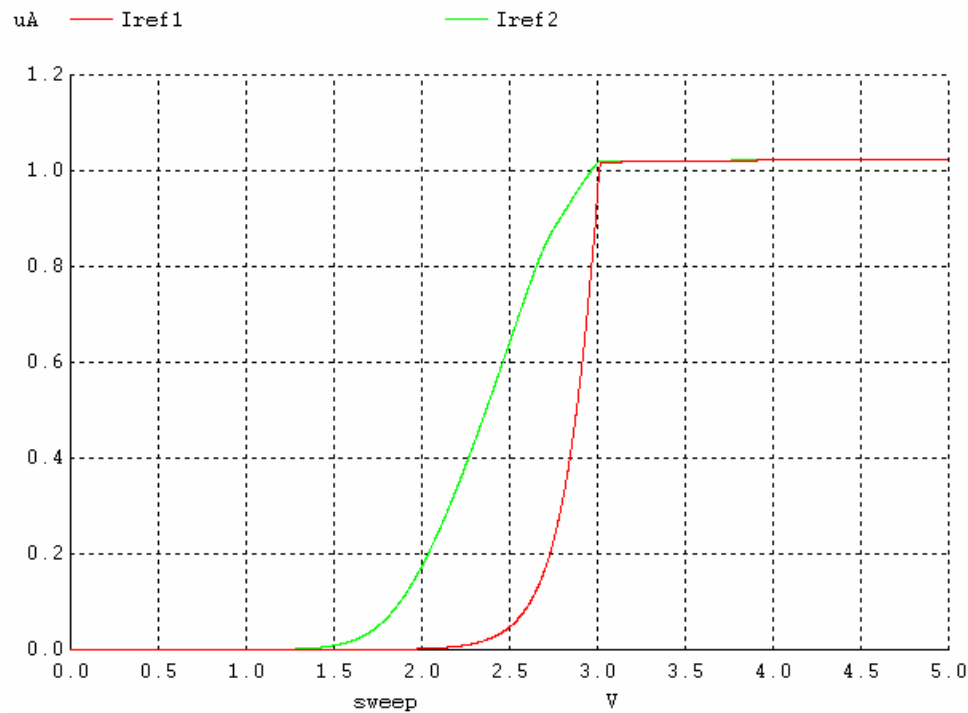
$$1uA = \frac{120u^2/V^2}{2}\frac{10}{2}\left(Vds, sat_2\right)$$

$$Vds, sat_4 = Vds, sat_2 = .0577V$$

$$VDD_{min} = 2.(.9577) + 2.(.0577) + .7 = 2.7V$$

$$Vgs_1 = Vgs_2 = Vgs_3 = Vgs_4 Vds, sat_2 + V_{thn} = .0577 + .8 = .8577V$$

$$Vgs_5 = Vgs_6 = Vgs_7 = Vgs_8 = .9577V$$

Based on simulation the minimum VDD allowable is around 2.9V which is pretty close with hand calculation.
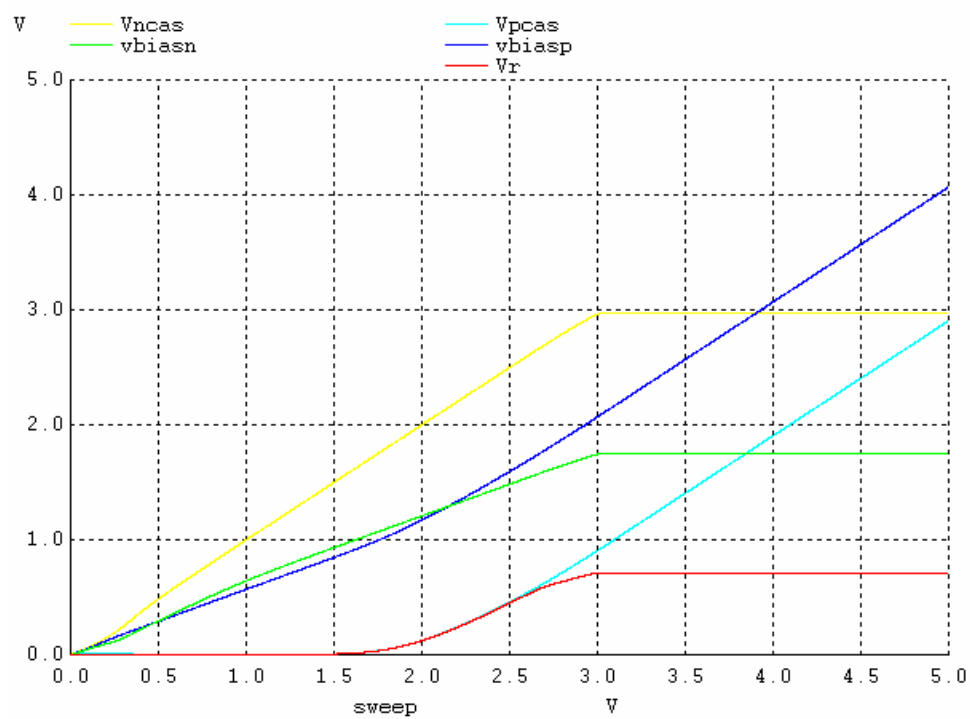
Problem 23.11.

Single Diode:
If the voltage across the diode is V_D and the reverse saturation current is given by I_S , then the current flowing through the diode is given by:
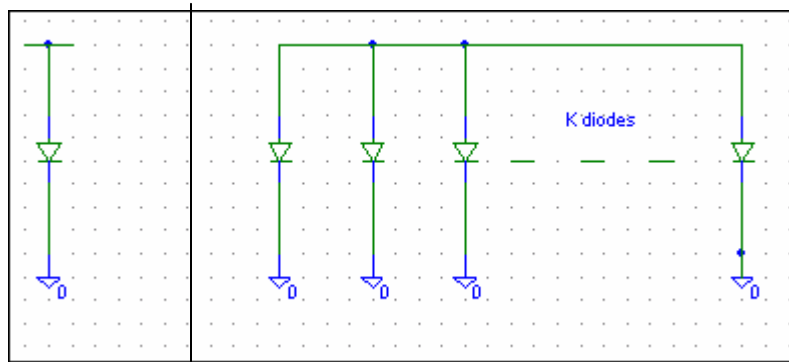
$$I_D = I_S . e^{(\frac{V_D}{n.V_T})}$$

figure : left: single diode ; Right: 'K' similar diodes in parallel.

K diodes in parallel:
Now consider the K similar diodes in parallel with the voltage across each of the diode remaining the same. Then the total current flowing through all the diodes is the sum of the currents flowing through each diode.

$$I_{TOTAL} = I_S . e^{(\frac{V_D}{n.V_T})} + I_S . e^{(\frac{V_D}{n.V_T})} + I_S . e^{(\frac{V_D}{n.V_T})} + ...k.times... + I_S . e^{(\frac{V_D}{n.V_T})}$$

$$\Rightarrow I_{TOTAL} = K.(I_S . e^{(\frac{V_D}{n.V_T})})$$

So the current flowing through all the diodes is 'K' times the current flowing through a single forward biased diode.

So K diodes in parallel behave like a single diode with a scale current of $K.I_S$.

23.12) Reference design that would output a voltage of $n.V_T$

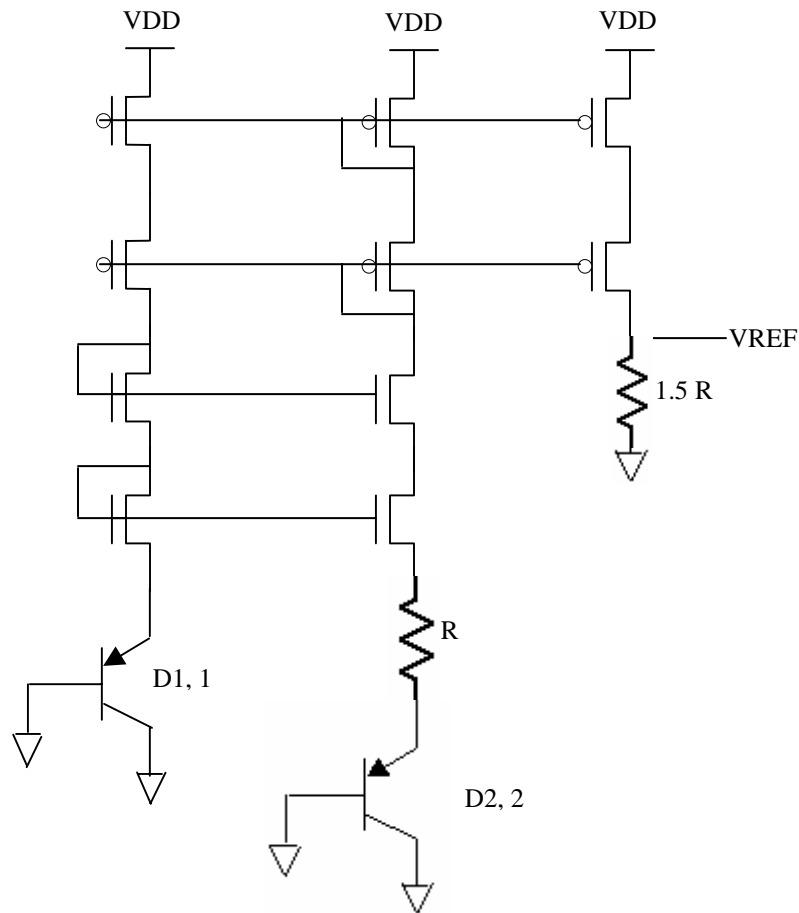Consider a PTAT voltage reference based on the thermal voltage-referenced self-biased circuit [fig. 23.25]

From Eq. (23.32), we have

$$V_{REF} = \frac{nk.L.\ln K}{q} \cdot T = n \cdot V_T \cdot L \cdot \ln K$$

So if we can make the product $L \cdot \ln K = 1$, then we can get the desired output.

If we take K=2, [number of diodes in parallel], then we get L =1.5
Its better to have minimum number of diodes [2,here] in parallel to reduce the power consumption.

All PMOS are 30/2 and all NMOS are 10/2,
scale = 1um, Start-up circuit not shown.

Problem 23.13

Determine if the performance of the BGR of Fig 23.32 can be enhanced by using the topology of Fig 23.33. Use simulations to verify your answer.
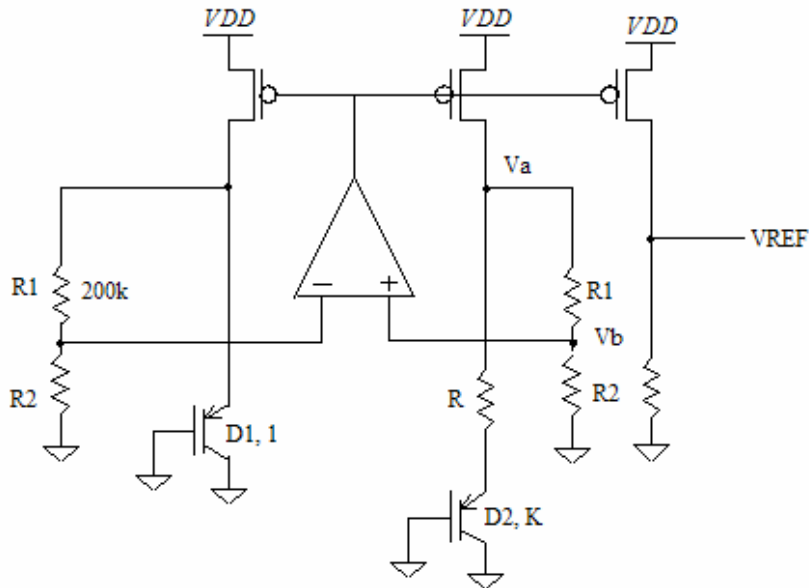
From the figure it can be seen that there is a resistive divider and the voltage V_b is given by

$$V_b = V_a \cdot \frac{R_2}{R_1 + R_2}$$

$$V_a = V_b \cdot (1 + \frac{R_1}{R_2})$$

Hence if V_b moves by 1mV then V_a moves by 2mV when the resistors have the same value. So there will be a variation in the PMOS drain to source voltages with variations in VDD So the performance of the BGR of Fig 23.33 will not be that good when compared to Fig 23.32.

Net list
*** Figure 23.13 CMOS: Circuit Design, Layout, and Simulation ***
.control
destroy all
set temp=0
run
set temp=25
run
set temp=50

```
run
set temp=75
run
set temp=100
run
plot dc1.vref dc2.vref dc3.vref dc4.vref dc5.vref
plot dc1.vref dc2.vref dc3.vref dc4.vref dc5.vref xlimit 950m 1.05 ylimit 500m 600m
*plot vref
.endc
.option scale=50n
.dc VDD 0 1.1 1m
VDD   VDD   0        DC     1

M1      vd1     vbiasp  VDD   VDD   PMOS L=2 W=20
M2      vr      vbiasp  VDD   VDD   PMOS L=2 W=20
M3      vref    vbiasp  VDD   VDD   PMOS L=2 W=20
D1      Vd1     0       PNPDIODE
D2      vd2     0       PNPDIODE 8
.model PNPDIODE    D       IS=1e-18 n=1

R1      Vd1     vk1     244.5k rmod
Rr      Vr      vd2     52k     rmod
R2      vr      vk2     244.5k rmod
R3      vk1     0       244.5k rmod
R4      vk2     0       244.5k rmod
RL      vref    0       208k   rmod
.model rmod    r       TC1=0.002

Xamp  VDD   vbiasp vk2     vk1      ndiff

.subckt ndiff    VDD   vout    vp      vm
M1      vob     vp      vss     0       NMOS L=2 W=10
M2      vout    vm      vss     0       NMOS L=2 W=10
M3      vss     vob     0       0       NMOS L=2 W=10
M4      vob     vob     VDD     VDD     PMOS L=2 W=20
M5      vout    vob     VDD     VDD     PMOS L=2 W=20
.ends

**start-up circuit
Mpu     vsu     vbiasp VDD   VDD   PMOS L=2 W=20
Mpd     vsu     vbiasp 0       0       NMOS L=100 W=10
Ms      vd1     vsu     VDD     VDD     PMOS L=1 W=10
```
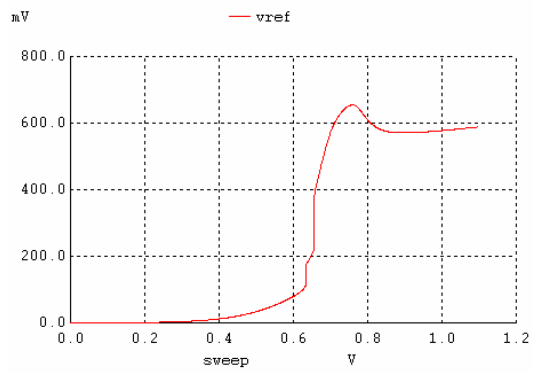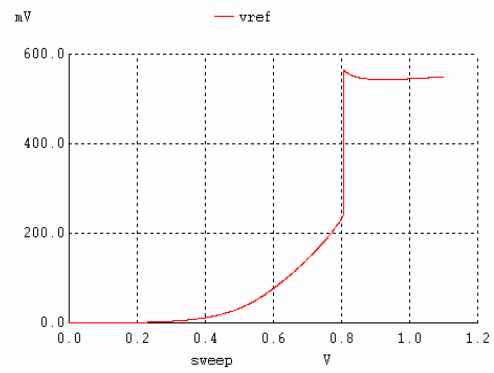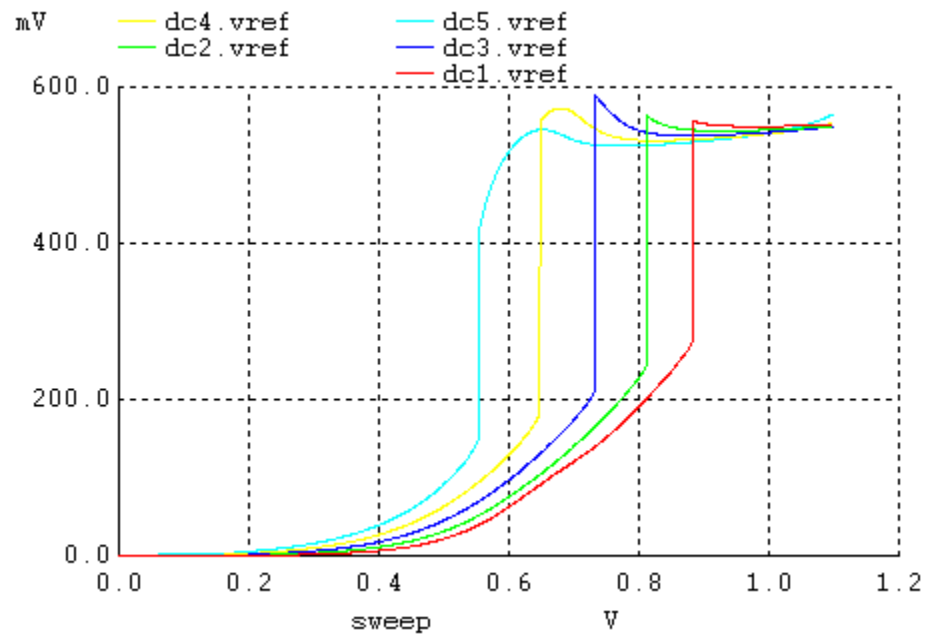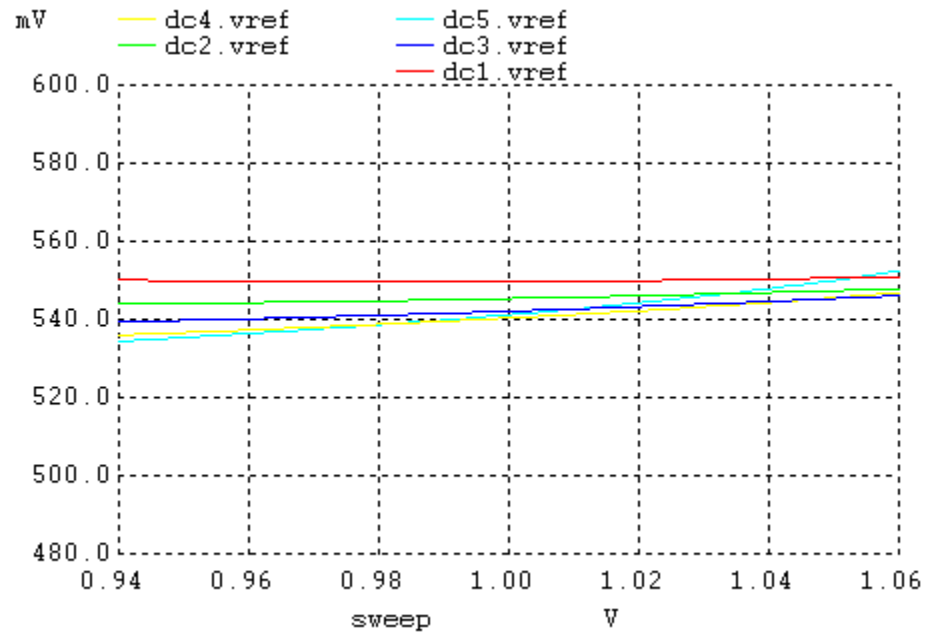
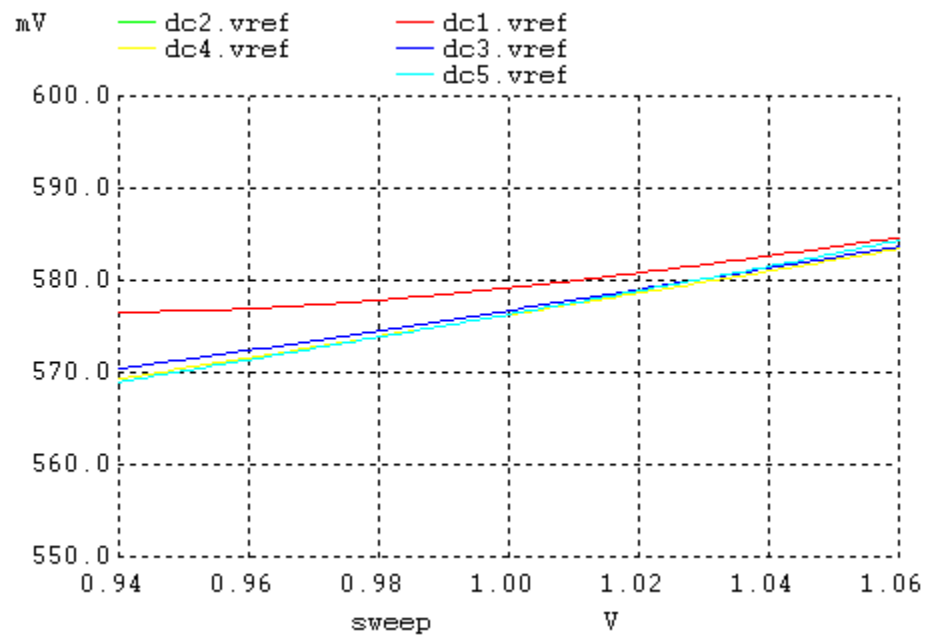Vref's sensitivity with VDD for Fig 23.32   Vref's sensitivity with VDD for Fig 23.33

Vref's sensitivity with VDD and Temperature for Fig 23.33

Vref's sensitivity with VDD and Temperature for Fig 23.33 Zoomed in view

Vref's sensitivity with VDD and Temperature for Fig 23.32 Zoomed in view

It can be seen from the Simulations above that the temperature behavior of the BGR without the resistive divider is better than the one with the divider.