7.1) ***Show how to derive Eqs. (7.1) and (7.2) from the block diagram seen in Fig. 7.1.***

Sol) Equations 7.1 and 7.2 are given below,

$$v_{out}(z) = z^{-1} \cdot v_{in}(z) + \left(1 - z^{-1}\right) \cdot V_{Qe}(z) \quad \textbf{[7.1]}$$

$$v_{out}(z) = v_{in}(z) \cdot \overbrace{\frac{A(z)}{1 + A(z)}}^{STF(z)} + V_{Qe}(z) \cdot \overbrace{\frac{1}{1 + A(z)}}^{NTF(z)} \quad \textbf{[7.2]}$$

The block diagram seen in Fig. 7.1 is shown below. It is the basic 1st order Delta-Sigma Noise shaping modulator.

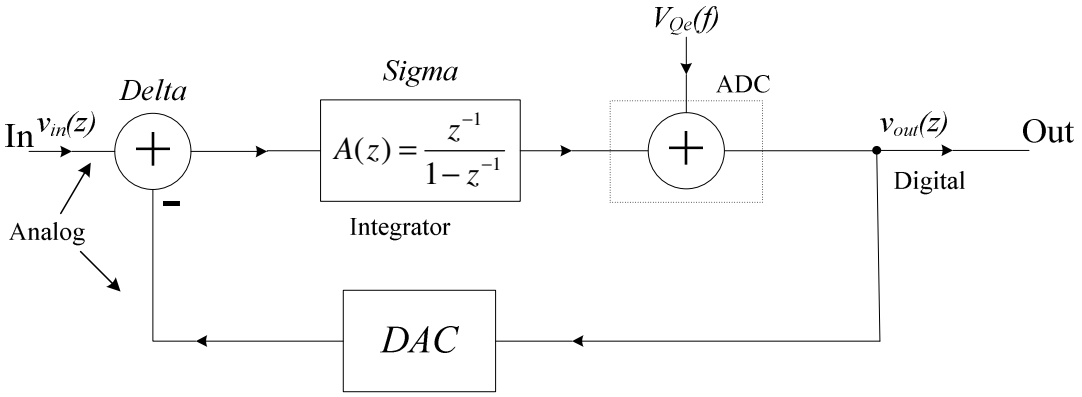


Figure 1: Block Diagram of a Noise-Shaping (NS) Modulator

The noise shaping property of the modulator can be shown using the transfer function of the system. Since the DAC does not add any quantization noise to the system, we can assume the transfer function for it to be equal to unity or we can just think of it as a wire connecting the output to the input.

$$\left[v_{in}(z) - v_{out}(z)\right] \cdot A(z) + V_{Qe}(z) = v_{out}(z) \quad \textbf{[1]}$$

$$v_{in}(z) \cdot A(z) - v_{out}(z) \cdot A(z) + V_{Qe}(z) = v_{out}(z) \quad \textbf{[2]}$$

$$v_{in}(z) \cdot A(z) + V_{Qe}(z) = v_{out}(z) + v_{out}(z) \cdot A(z) \quad \textbf{[3]}$$

$$v_{in}(z) \cdot A(z) + V_{Qe}(z) = v_{out}(z) \cdot \left[1 + A(z)\right] \quad \textbf{[4]}$$

$$v_{out}(z) = v_{in}(z) \cdot \overbrace{\frac{A(z)}{1 + A(z)}}^{STF(z)} + V_{Qe}(z) \cdot \overbrace{\frac{1}{1 + A(z)}}^{NTF(z)} \quad \textbf{[5]}$$

Substituting $A(z) = \dfrac{z^{-1}}{1 - z^{-1}}$, we get

$$v_{out}(z) = v_{in}(z) \cdot \frac{\left(\dfrac{z^{-1}}{1 - z^{-1}}\right)}{1 + \left(\dfrac{z^{-1}}{1 - z^{-1}}\right)} + V_{Qe}(z) \cdot \frac{1}{1 + \left(\dfrac{z^{-1}}{1 - z^{-1}}\right)} \quad \textbf{[6]}$$

$$v_{out}(z) = v_{in}(z) \cdot \frac{\left(\frac{z^{-1}}{1-z^{-1}}\right)}{\frac{1-z^{-1}+z^{-1}}{1-z^{-1}}} + V_{Qe}(z) \cdot \frac{1}{\frac{1-z^{-1}+z^{-1}}{1-z^{-1}}} \quad \textbf{[7]}$$

$$v_{out}(z) = \underbrace{z^{-1}}_{STF} \cdot v_{in}(z) + \underbrace{\left(1-z^{-1}\right)}_{NTF} \cdot V_{Qe}(z) \quad \textbf{[8]}$$

This shows that using the 1st order noise shaping modulator with switched capacitors we get a signal transfer function that is just a delay through the modulator. The input just passes the modulator with a delay. But the quantization noise has a transfer function of $\left(1-z^{-1}\right)$, which is the transfer function of a differentiator (See Section 1.2.2) the magnitude response of the differentiator shows that the quantization noise is eliminated at DC and low frequencies and it is pushed or shaped into the high frequency region away from our signal bandwidth of interest.

Kaijun Li
Problem 7.2
After reviewing Sec. 2.2.3, would it be possible to replace the delaying integrator seen in Fig. 7.2 with a non-delaying integrator? If so, what is the NTF and STF of the modulator? Is the modulator stable?

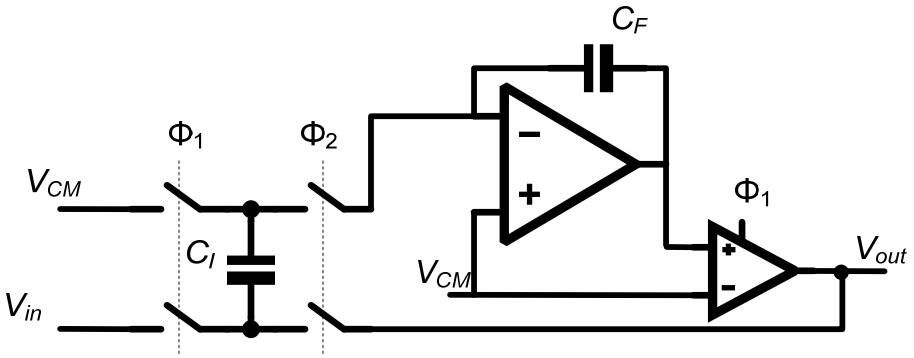


Fig. 7.2 Circuit implementation of a first-order NS modulator

Solution:
As shown in Fig. 7.2, the unit delay for the delaying integrator is caused by clocking the clocked-comparator using Φ_1 clock. To implement a non-delaying integrator, the clock can be replaced by Φ_2 clock as shown in the following figure.

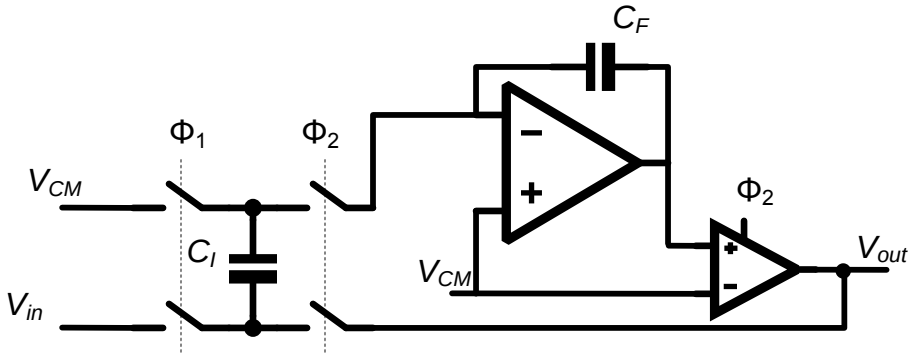


Fig. 7.2-1 Circuit implementation of a first-order NS modulator with non-delaying integrator

The block diagram for Fig. 7.2-1 is drawn in Fig. 7.2-2.

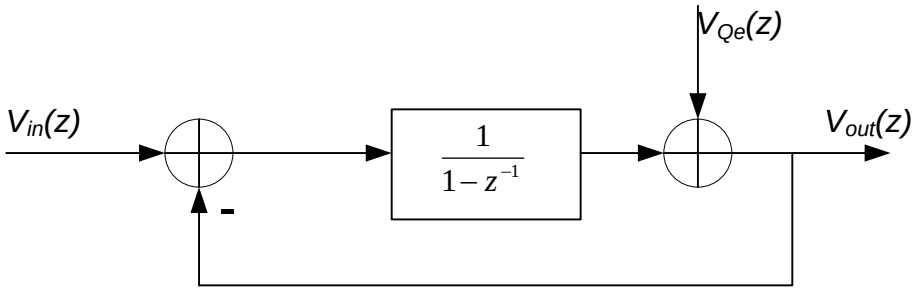


Fig. 7.2-2 Block diagram of a first-order NS modulator with non-delaying integrator

The signal transfer function (*STF*) and the noise transfer function (*NTF*) are found as:

$$STF = \frac{\frac{1}{1 - z^{-1}}}{1 + \frac{1}{1 - z^{-1}}} = \frac{1}{2 - z^{-1}} \tag{7.2-1}$$

$$NTF = \frac{1}{1 + \frac{1}{1 - z^{-1}}} = \frac{1 - z^{-1}}{2 - z^{-1}} \tag{7.2-1}$$

It is noted that the pole of the *STF* and *NTF* is $z = \frac{1}{2}$ which is located inside the unit circle and the system is stable. We can prove the stability through impulse response as well.

The impulse responses of *STF* and *NTF* are:

$$Z^{-1}(STF\ (z)) = Z^{-1}\left(\frac{1}{2 - z^{-1}}\right) = Z^{-1}\left(\frac{1/2}{1 - z^{-1}/2}\right) = \frac{1}{2}\left(1 + \frac{1}{2}z^{-1} + \frac{1}{4}z^{-2} + \frac{1}{8}z^{-3} + \cdots\right)$$

$$h_1[n] = \frac{1}{2}\left(1, \frac{1}{2}, \frac{1}{4}, \frac{1}{8}, \cdots, \left(\frac{1}{2}\right)^k, \cdots,\right), k \geq 0$$

$$Z^{-1}(NTF\ (z)) = Z^{-1}\left(\frac{1 - z^{-1}}{2 - z^{-1}}\right) = Z^{-1}\left(\frac{1}{2} \cdot \frac{1 - z^{-1}}{1 - z^{-1}/2}\right) = \frac{1}{2}\left(1 - \frac{1}{2}z^{-1} - \frac{1}{4}z^{-2} - \frac{1}{8}z^{-3} - \cdots\right)$$

$$h_2[n] = \frac{1}{2}\left(1, -\frac{1}{2}, -\frac{1}{4}, -\frac{1}{8}, \cdots, -\left(\frac{1}{2}\right)^k, \cdots,\right), k \geq 1$$

which leads to

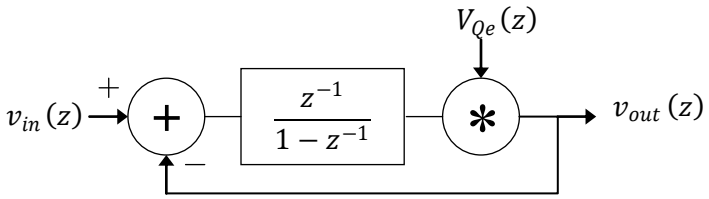
$$\sum_{n=0}^{\infty} |h_1[n]| = \sum_{n=0}^{\infty} \frac{1}{2}\left|\left(\frac{1}{2}\right)^n\right| = \frac{1}{2}\sum_{n=0}^{\infty}\left(\frac{1}{2}\right)^n = \frac{1}{2} \cdot \frac{1}{1 - \frac{1}{2}} = 1 < \infty\ ,$$

$$\sum_{n=0}^{\infty} |h_2[n]| = \frac{1}{2} + \sum_{n=1}^{\infty} \frac{1}{2}\left|-\left(\frac{1}{2}\right)^n\right| = \frac{1}{2} + \frac{1}{2}\sum_{n=1}^{\infty}\left(\frac{1}{2}\right)^n = \frac{1}{2} + \frac{1}{2} \cdot \frac{\frac{1}{2}}{1 - \frac{1}{2}} = 1 < \infty$$

Therefore, the system is still stable using the non-delaying integrator.

7.3 Using SPICE simulations, show how passing the digital signal seen in Fig. 7.3 through an RC lowpass filter will reduce the modulation noise in the signal and help to recover the original analog input signal. What happens to the original signal's amplitude if it's filtered, by the added RC filter, too much?

Before performing the SPICE simulations, let's take a quick walk through the building blocks of the discrete first order noise shaping (NS) modulator.

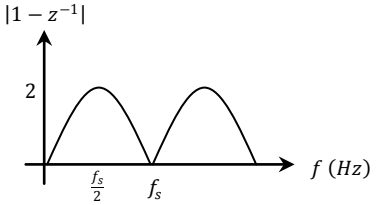


F-1 Block of a discrete NS modulator

The transfer function of the NS modulator seen in F-1 is:

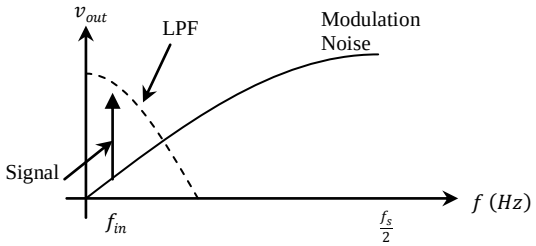
$$v_{out}(z) = z^{-1}v_{in}(z) + (1 - z^{-1})V_{Qe}(z)$$

The transfer function shows that the output signal is the delayed input signal plus the differentiated quantization noise. Differentiation in the z-plane has the magnitude response seen in F-2.



F-2 Magnitude response of the digital differentiator

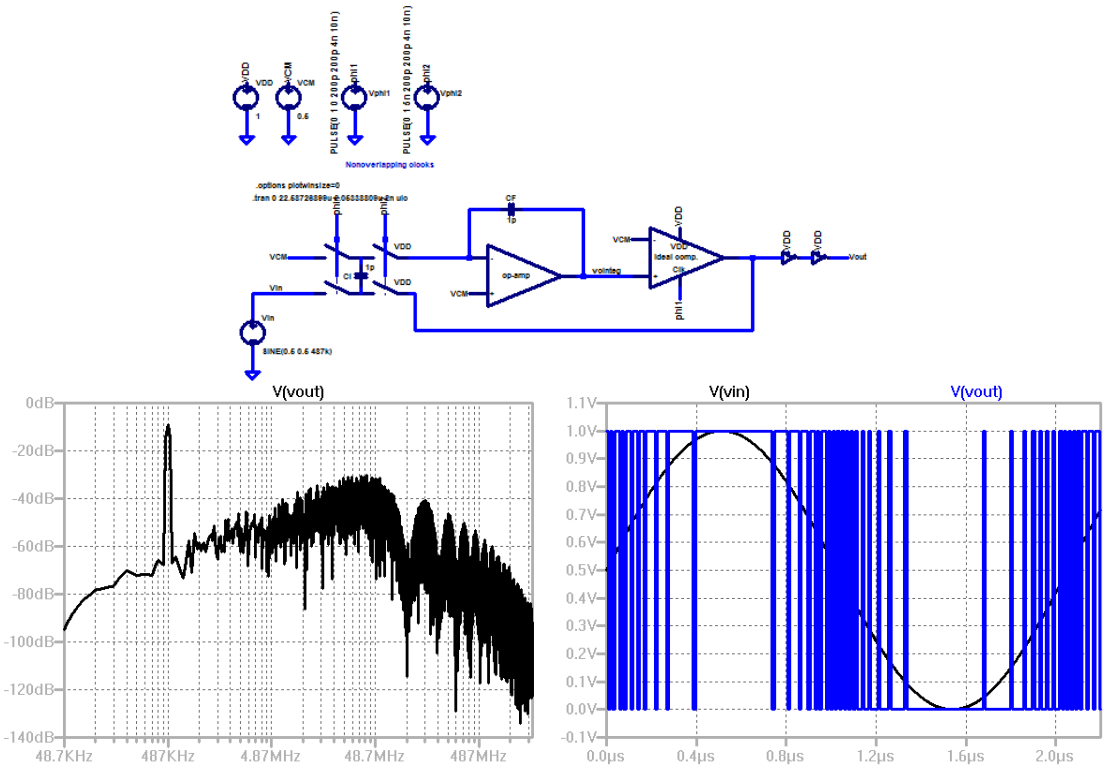
The linear plot in F-2 shows that the quantization noise will be modulated to higher frequencies (f_s/2). If we have a high sampling frequency or low input signal spectrum we can remove a large amount of the quantization noise with filtering. The output will be the convolution of the input signal along with the differentiated quantization noise. As long as the input frequency remains much less than the sampling frequency we can plot the output spectrum (before filtering).



F-3 Output signal with modulation noise and LPF

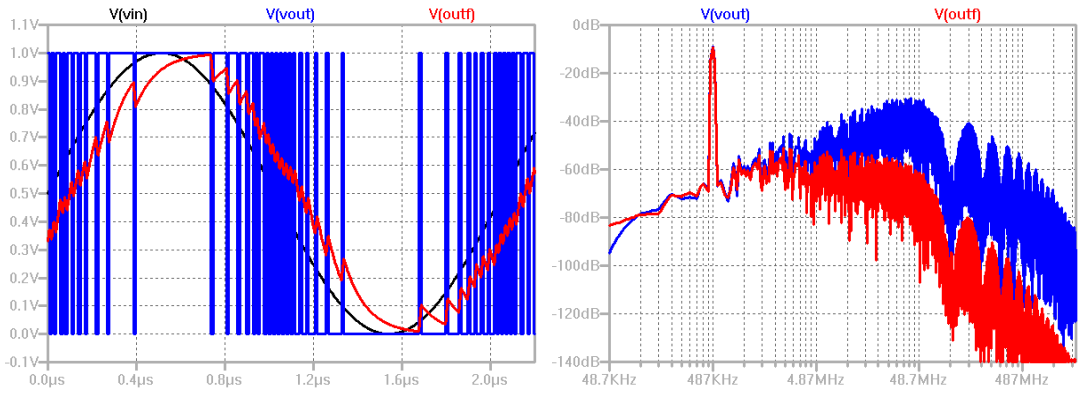
F-3 shows that as long as $f_{in} << f_s$ the modulation noise can be removed by sending the output signal through a simple lowpass filter (LFP). F-3 also shows that if the RC values that we choose are too large ($f_{3dB} < f_{in}$) we will attenuate the desired signal. We can use simulations to validate our understanding.

Using _Fig7_3_MSD from the website we can set up the simulation by setting f_{in} = 500 *kHz*, f_{clk} = 100 *MHz*, t_{start} = 2 *µs*, t_{stop} = 12 *µs*, and later *RC* = 100 *ns* (f_{3dB} = 1.59 *MHz*). We can use both the transient response and the fast Fourier transform (FFT) to view the output signal before and after filtering.



F-4 _Fig7_3_MSD schematic and simulation results

I used a 487 *MHz* input signal to prevent coherent sampling from the clock. F-3 shows the FFT and transient response of the first order NS modulator. The log-log FFT plot shows that the noise is modulated out to higher frequencies and repeats as expected from F-2. When we filter the signal we will attenuate the high frequency noise.



F-5 Transient and FFT of the filtered output

F-5 shows the output signal after being passed through an *RC* filter in both the time and frequency domain. Note that the transient output is not attenuated, also the FFT shows the filters affect on the high frequency noise.

7.4 Show the spectrums (modulator input, digital output, and analog output after filtering) of the signals in question 7.3. Discuss what the spectrums indicate.

Q. 7.3 asks to pass the output of the circuit that produces Fig. 7.3 through a low-pass RC filter and to show how this reduces the modulation noise.

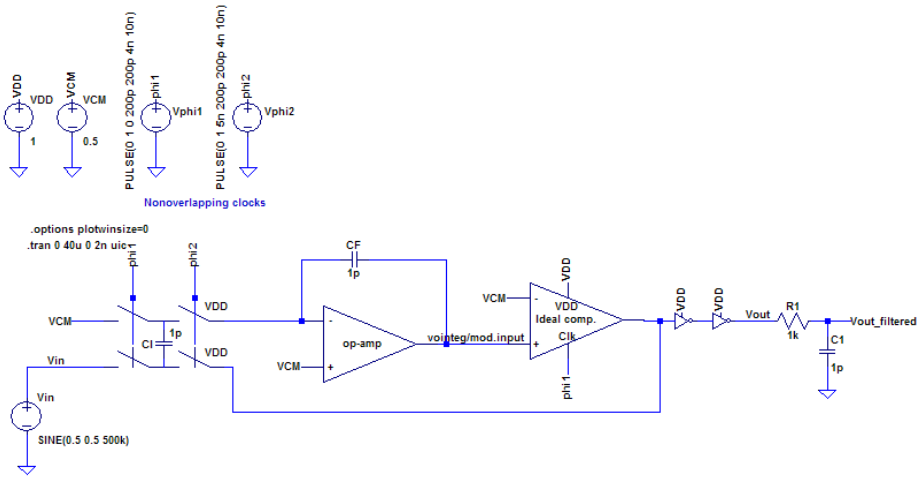


Figure 1. First-order NS modulator using switched capacitors and an active integrator.

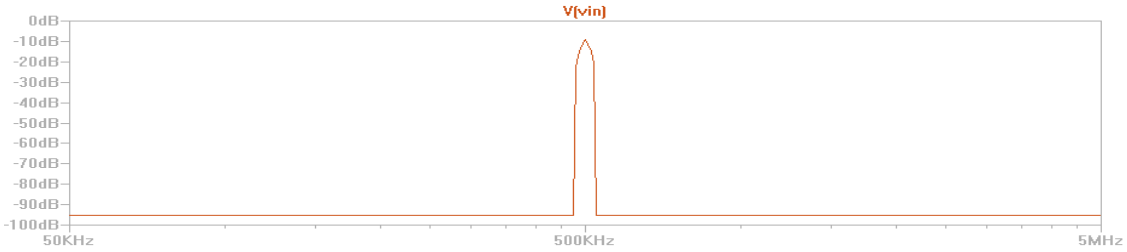


Figure 2. Modulators input signal.

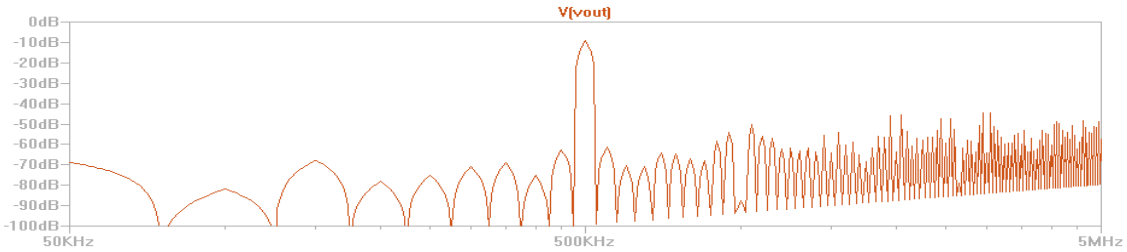


Figure 3. Unfiltered digital output.

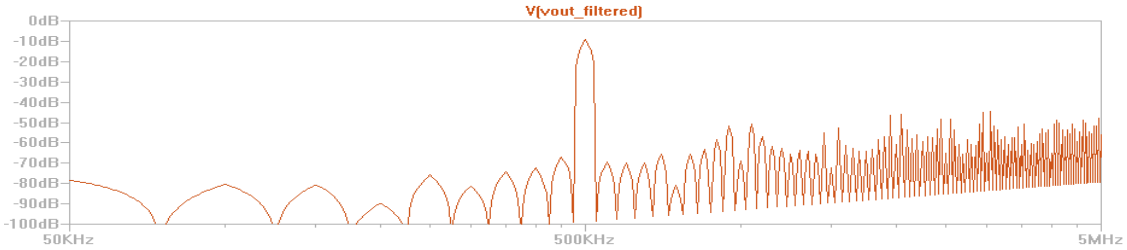


Figure 4. Filtered digital output with RC = 1e-9. $1/(2\pi RC)$ = 159MHz = filter f_{3dB}.

Figure 2 shows the input signal to the modulator. As expected, a perfect sine wave has no noise and shows a spectrum with only one frequency mode visible, at the input frequency of 500kHz.

Figure 3 is the unfiltered digital output, just before the RC filter. This FFT shows both the wanted signal at 500kHz as well as all of the modulation noise.

Figure 4 shows the output after going through an RC filter with RC = 1E-9, giving an f_{3dB} of 159MHz. Comparing Figs. 3 and 4 we see that the noise has been attenuated after going through the lowpass RC filter. The wanted signal at 500kHz, however, has been unchanged.

If we were to decrease RC by enough so the f_{3dB} is comparable to, or below, f_{in}, then we should see an attenuation of the input signal, in addition to seeing the noise roll off at -20dB/dec following the f_{3dB} frequency. Figure 5 shows this situation with RC = 1E-6, f_{3dB}=159kHz. Here the wanted signal has been attenuated by approximately 10dB

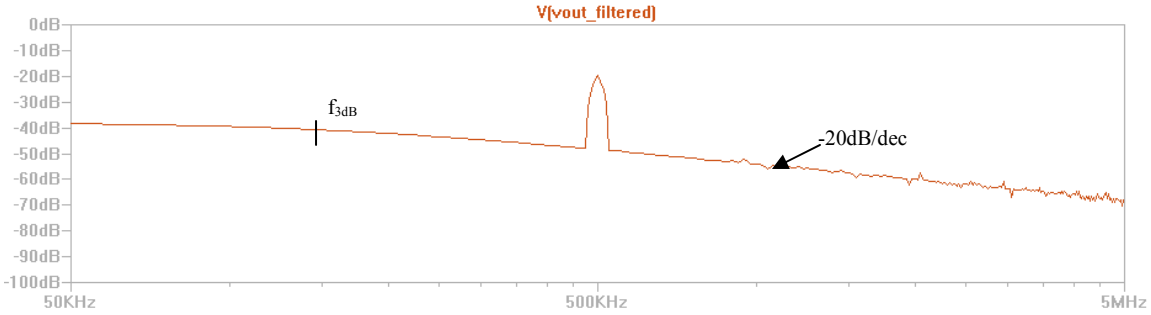
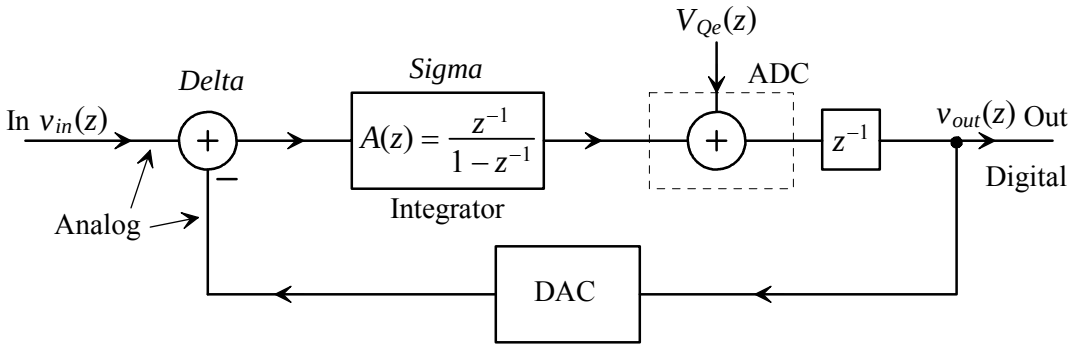


Figure 5. Filtered digital output with RC = 1e-6. $1/(2\pi RC)$ = 159kHz = filter f_{3dB}.

Jake Baker

7.5 If an extra delay, z^{-1}, was added to the forward path of the modulator in Fig. 7.2 would the resulting topology be stable? Why or why not?

The block diagram for Fig. 7.2 was shown in Fig. 7.1. Below shows this diagram with the added delay (a D-Flip-Flop).



The transfer function, see Eq. (7.2), can now be written as

$$v_{out}(z) = \frac{z^{-2}v_{in}(z)}{1-z^{-1}+z^{-2}} + \frac{(1-z^{-1})z^{-1}}{1-z^{-1}+z^{-2}} \cdot V_{Qe}(z)$$

or

$$v_{out}(z) = \frac{v_{in}(z)}{z^2-z+1} + \frac{(z-1)}{z^2-z+1} \cdot V_{Qe}(z)$$

We know that for the system to be stable the poles must be inside the unit circle. The poles are located at

$$z_{p1,p2} = \frac{1}{2} \pm j\frac{\sqrt{3}}{2}$$

which is right on the edge of the unit circle. While we placed poles right on the unit circle when we designed comb filters, which used integer numbers, we can't do this in a switched-capacitor circuit. The noise will cause the poles to move outside the unit circle and the system will become unstable (**so adding the extra delay is very bad**).

Jason Durand

Problem 7.6 – Show, using timing diagrams, how Equation 7.3 is correct.

Equation 7.3 describes the input/output relationship fed back around the single bit ADC (comparator) in a first order noise shaping modulator. The relationship is

$$Desired\ ADC\ input/output\ =\ \frac{z^{-1}}{1-z^{-1}}(v_{in}-v_{out})$$

when implemented with a discrete analog integrator, as in figure 1.

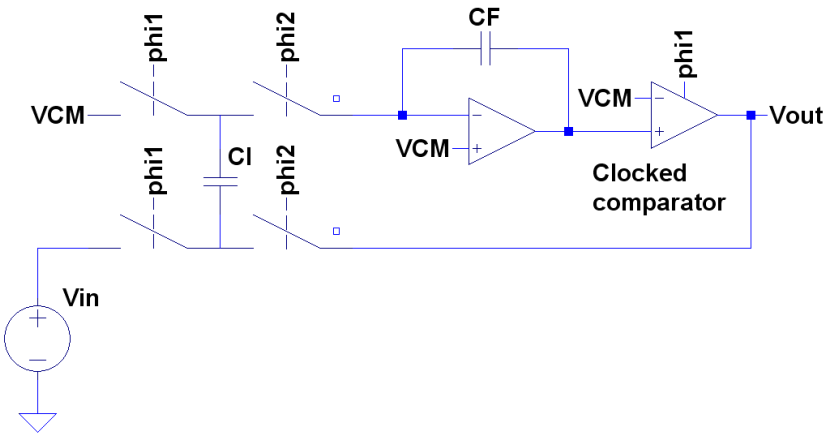


Figure 1 First-order NS Modulator.

In figure 1, the phi1 and phi2 signals are non-overlapping clock signals, which are shown in figure 2.

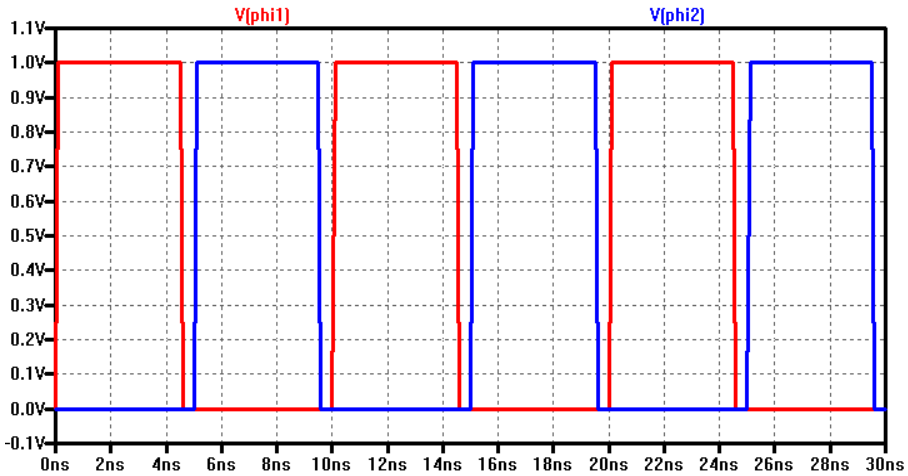


Figure 2 Non-overlapping Clocks

Equation 7.3 is valid, and it becomes clear when looking at the clock signals in figure 2. When phi1 is high, C_I tracks Vin and stores a charge, $Q_I=C_I V_{in}$. The clocks then switch after a brief time where both are turned off (the non-overlapping part) and the fed-back part (V_{out}) is subtracted from the stored charge Q_I (from capacitor C_I) and integrated through the feedback from the opamp through C_F, appearing at the opamp output, which is the ADC input for this problem. This charge movement is

described by the formula

$$V_{ADCin} = \frac{V_{in}(z)z^{-1/2} - V_{out}(z)}{1 - z^{-1}} \cdot \frac{C_I}{C_F} \quad .$$

Note the similarity of this equation to the two input entry on table 2.2, for the discrete analog integrator. Since the ADC (comparator) is then clocked at phi1, one half clock cycle after the signal is available at the comparator input, the equation becomes

$$V_{ADCin} = \frac{V_{in}(z)z^{-1} - V_{out}(z)z^{-1/2}}{1 - z^{-1}} \cdot \frac{C_I}{C_F}$$

when the comparator is clocked. The output changes and feeds back to the discrete analog integrator, but is not actually integrated until the phi2 signal goes high, connecting the path to the integrator. This is written as

$$V_{ADCin} = \frac{V_{in}(z)z^{-1} - V_{out}(z)z^{-1}}{1 - z^{-1}} \cdot \frac{C_I}{C_F} \quad ,$$

which can be algebraically rearranged to form equation 7.3, verifying equation 7.3. The gain of the integrator, or C_I / C_F drops out of the equation because it cancels with the non-linear gain of the comparator, which (ideally) acts to normalize the gain of the entire system to one.

Lincoln Bollschweiler

7.7 For the NS modulator shown in Fig. 7.5 used for digital to analog conversion, what component serves as the ADC? What component serves as the DAC?

The accumulator (digital delaying integrator) serves as the DAC and the quantizer circuit serves as the ADC. This can be seen more easily by examining the (b) part of Fig. 7.5. We see that the digital word formed by the quantizer is fed back to the input and subtracted from the input word where the accumulator can integrate the two and send a pseudo (quantized) analog signal to the output.

Lincoln Bollschweiler

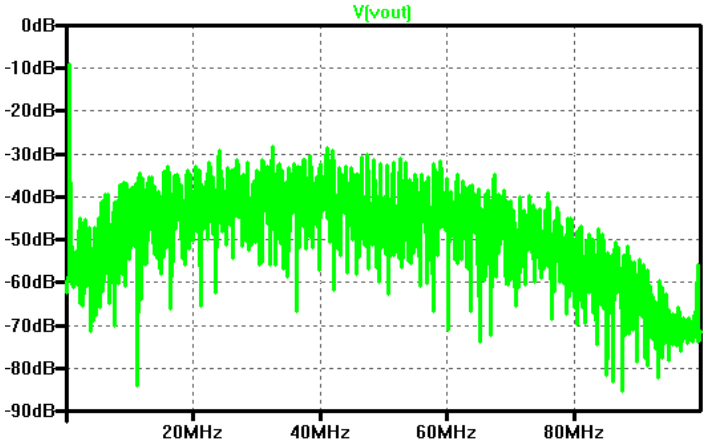
7.8 Explain how the quantizer in Fig. 7.5 functions.

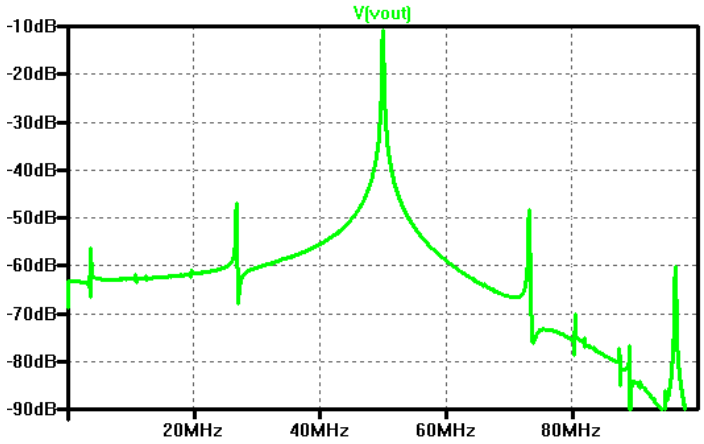
The quantizer is (can be) a simple MUX with two hardwired inputs. The length of the word for these inputs is set to match the length of the digital input word arriving at v_{in}. The MUX inputs are 011111… (two's complement of binary offset 111111… [V_{DD} or V^+]) or 100000… (two's complement of binary offset 000000… [ground or V^-]). The MUX selector is the MSB of the output of the accumulator. If the MSB is a 1, the case for V_{DD} is sent. If it is a 0, the case for ground is sent. The word sent back to the summer / accumulator is in two's complement to accomplish the subtraction at the summer.

Jake Baker

7.9 What are we assuming about an input signal if the modulation noise follows Eq. (7.5)?

We assume the input signal is changing, that is, not DC. Below shows the simulation output spectrum (signal and noise) for the modulator in Fig. 7.2 when the input is 500 kHz. The simulation time was increased to 20 us. Below this is the spectrum we get when we apply a DC input voltage of 500 mV. Note that the spectrum isn't "rounded" as it is in the top plot but rather has basically a single tone at $f_s/2$. While the shape of the spectrums will change with input DC voltages the point is that we won't get noise spectrums with the shape seen in Fig. 7.6 when the input is slow or DC. Modulators using a second-order topology are much more robust to tones in the output spectrums. The two feedback loops randomize the noise even for a DC input signal.





Jake Baker

7.10 What is the magnitude of Eq. (7.5) (plot it against frequency)?

Equation (7.5) is

$$NTF(f)V_{Qe}(f) = \left(1 - e^{-j2\pi\frac{f}{f_s}}\right) \cdot \frac{V_{LSB}}{\sqrt{12 f_s}}$$

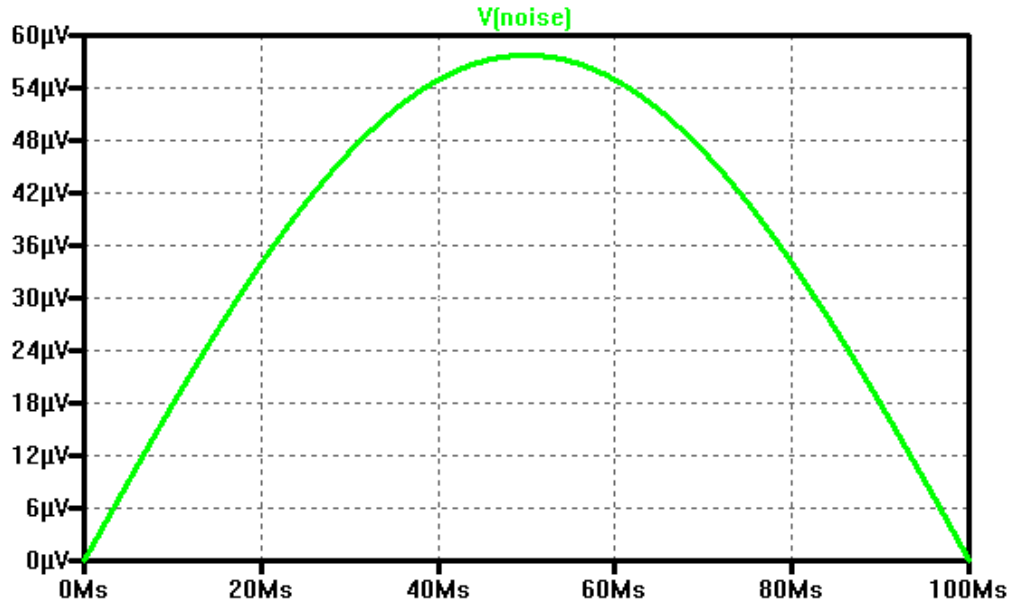
The term in parantheses represents differentiation and its magnitude can be written, with the help of Eq. (1.46), as

$$\left|1 - e^{-j2\pi\frac{f}{f_s}}\right| = 2\left|\sin\pi\frac{f}{f_s}\right|$$

so

$$\left|NTF(f)V_{Qe}(f)\right| = 2\left|\sin\pi\frac{f}{f_s}\right| \cdot \frac{V_{LSB}}{\sqrt{12 f_s}}\ ,\ \text{units } V/\sqrt{Hz}$$

Using $V_{LSB} = 1V$ and an $f_s = 100\ MHz$ this equation is plotted below using LTspice (see, also, Fig. 7.6).



Jason Durand

Problem 7.11 – What is the difference between quantization noise and modulation noise?

Quantization noise is the noise that is added to a signal when it is converted to a digital signal. A digital signal can only represent fractional values of VDD, with the number of steps equal to 2^N, where N is number of bits. By contrast, an analog signal can hold all voltage values up to the VDD of the system, a continuous range. The noise that is added during analog to digital conversion to move the input analog value to one of the digital steps is the quantization noise. Mathematically, the quantization noise can be treated as a random variable, with RMS voltage equal to

$$V_{Qe,RMS}(f) = \frac{V_{LSB}}{\sqrt{12 f_s}} \quad ,$$

which is spread equally over all frequencies. For ease of calculations and as a worst case assumption, all the noise is modeled to occur between 0 and $f_s/2$. This is the quantization noise, present in all ADC's.

Modulation noise has the same total power as the quantization noise in a system, but it is shaped differently (multiplied by the noise transfer function). The goal of most noise shaping data converters is to move the bulk of the quantization noise to a higher frequency, and then passing the output through a low-pass filter which (ideally) removes all the noise.

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7.12 Show the steps and assumptions leading to Eq. (7.12).

Equation 7.12 is below:

$$V_{Qe,RMS} \approx \frac{V_{LSB}}{\sqrt{12}} \cdot \frac{\pi}{\sqrt{3}} \cdot \frac{1}{K^{3/2}}$$

The steps and assumptions leading up to Eq. 7.12 are discussed in sections 7.1.1 and 7.1.2, but let's repeat them here and add additional information.

The first assumption used when characterizing the spectral characteristics of the quantization noise is that Bennett's criterion holds, that is:

- The input's signals amplitude falls within V_{REF+} and V_{REF-} of the ADC.
- The ADC's LSB is much smaller than the amplitude of the input signal.
- The input signal is busy.

When using a 1-bit quantizer (clocked comparator), the second of Bennett's criteria is not valid. The noise shaping modulators feedback (subtracts) a signal that represents the quantization noise to the input signal. This fed-back signal relaxes the second criteria.

The RMS quantization noise voltage is:

$$V_{Qe,RMS} = \frac{V_{LSB}}{\sqrt{12}} \ (V)$$

The second assumption is that all of the quantization noise falls within the Nyquist frequency ($f_s/2$). This allows us to determine the quantization power spectral density and voltage spectral density as:

$$V_{Qe}^2(f) = \frac{V_{LSB}^2}{12 f_s} \left({}^{V^2}/_{Hz} \right)$$

$$V_{Qe}(f) = \frac{V_{LSB}}{\sqrt{12 f_s}} \left({}^{V}/_{\sqrt{Hz}} \right)$$

Equation 7.12 is the quantization noise after being filtered by a digital filter with and $OSR = K$, and therefore a bandwidth $B = f_s/2K$. So to determine how much of the quantization noise is left after being filtered we must determine what the quantization noise voltage/power spectral density is after being shaped.

The *NTF* used to shape the noise is:

$$NTF = (1 - z^{-1}) = 1 - e^{-j 2\pi \frac{f}{f_s}}$$

$$|NTF| = \left| 1 - e^{-j 2\pi \frac{f}{f_s}} \right| = \left| 1 - \cos\left(-2\pi \frac{f}{f_s}\right) - j \sin\left(-2\pi \frac{f}{f_s}\right) \right|$$

From section 1.2.2 the magnitude of the *NTF* is:

$$|NTF| = 2\left|\sin \pi \frac{f}{f_s}\right|$$

The quantization noise present in a particular bandwidth (*B*) is then:

$$V_{Qe,RMS}^2(f) = 2\int_0^B |NTF|^2 \left|V_{Qe}(f)\right|^2 df = 8\int_0^B \left|\sin \pi \frac{f}{f_s}\right|^2 \left|\frac{V_{LSB}}{\sqrt{12 f_s}}\right|^2 df = 8\frac{V_{LSB}^2}{12 f_s}\int_0^B \sin^2\left(\pi \frac{f}{f_s}\right) df$$

Remembering, for an *OSR* = *K* the filters bandwidth will be:

$$B = \frac{f_s}{2K}$$

Also recall the Taylor series expansion of trigonometric functions:

$$\sin x = \sum_{n=0}^{\infty} \frac{(-1)^n}{(2n+1)!} x^{2n+1} = x - \frac{x^3}{3!} + \frac{x^5}{5!} \cdots$$

So that for small *x*, *sinx* ≈ *x*, which is a good approximation because f_s is much greater than *f* for large *OSR*.

$$8\frac{V_{LSB}^2}{12 f_s}\int_0^B \sin^2\left(\pi \frac{f}{f_s}\right) df \approx 8\frac{V_{LSB}^2}{12 f_s}\int_0^{\frac{f_s}{2K}} \left(\pi \frac{f}{f_s}\right)^2 df = 8\frac{\pi^2 V_{LSB}^2}{12 f_s^3}\int_0^{\frac{f_s}{2K}} f^2 df = 8\frac{\pi^2 V_{LSB}^2}{12 f_s^3}\left[\frac{1}{3}\frac{f_s^3}{8K^3}\right] = \frac{V_{LSB}^2}{12}\frac{\pi^2}{3}\frac{1}{K^3}$$

$$V_{Qe,RMS}^2(f) \approx \frac{V_{LSB}^2}{12}\frac{\pi^2}{3}\frac{1}{K^3}\left(V^2/_{Hz}\right)$$

So that the *RMS* modulation noise is:

$$V_{Qe,RMS}(f) \approx \frac{V_{LSB}}{\sqrt{12}}\frac{\pi}{\sqrt{3}}\frac{1}{K^{3/2}}\left(V/_{\sqrt{Hz}}\right)$$

To summarize the assumptions:

- Bennett's criteria holds (the noise spectral content is flat for a quantizer)
- All of the quantization noise falls within the Nyquist band

Kaijun Li
Problem 7.13
Is the statement on page 238 that “every doubling in the oversampling ratio results in 1.5 bits increase in resolution” really true if *K* is small? Explain.

Solution:
Ideal SNR for a first order noise shaping data converter is:

$$SNR = 6.02N + 1.76 - 5.17 + 30 \cdot \log_{10}(K)$$

This leads to the effective number of bits (ENOB) as

$$ENOB = \frac{SNR - 1.76}{6.02} = N + 1.5 \cdot \log_2(K) - 5.17/6$$

Which indicates that there is 1.5 bits increase for every doubling in oversampling ratio *K*. However, we also notice that for above equations to be valid, *K* needs to be greater than 2. So, if *K* is small but greater than 2, the statement on page 238 that “every doubling in the oversampling ratio results in 1.5 bits increase in resolution” is still valid.

7.14) ***Does noise-shaping work for DC input signals? If so, how?***

Sol)

Yes noise-shaping works for DC input signals too. The noise-shaping modulator has a feedback loop to get a running average of the analog input signal. The modulator's digital output is averaged to get a representation of the analog input signal.

The noise transfer function of the NS modulator is a magnitude response of a digital differentiator, whose magnitude is zero at DC and peaks at a high frequency of fs/2. In other words, the noise is shaped or modulated towards high frequencies, as this is an unwanted signal being added to the input signal, the output needs to be low-pass filtered and the high frequency noise can be eliminated.

7.15. Show the steps leading up to Eq. (7.22).

Sol. **Analysis of how the SNR of the first order modulator (data converter) is affected because of filtering by Sinc filter**

In order to achieve better SNR for a first order modulator L averaging (sinc) filters are cascaded for modulator of order M. L is given by L=M+1 (eq 7.17 in book). We know M=1 for a first order modulator, hence L=2.

$$H(z)=\left[\frac{1}{K}\cdot\frac{1-z^{-K}}{1-z^{-1}}\right]^{L}=\left[\frac{1}{K}\cdot\frac{1-z^{-K}}{1-z^{-1}}\right]^{2}$$

Hence

$$|H(f)|=\left|\left[\frac{1}{K}\cdot\frac{1-e^{-\frac{j2K\pi f}{fs}}}{1-e^{-\frac{j2\pi f}{fs}}}\right]^{2}\right|$$

$$|H(f)|=\left|\left[\frac{1}{K}\cdot\frac{1-\cos\left(\frac{2K\pi f}{fs}\right)-j\sin\left(\frac{2K\pi f}{fs}\right)}{1-\cos\left(\frac{2\pi f}{fs}\right)-j\sin\left(\frac{2\pi f}{fs}\right)}\right]^{2}\right|$$

$$|H(f)|=\left|\frac{1}{K}\cdot\frac{\sin\left(\frac{K\pi f}{f_s}\right)}{\sin\left(\frac{\pi f}{f_s}\right)}\right|^{2}$$

$$|H(f)|^{2}=\left|\frac{1}{K}\cdot\frac{\sin\left(\frac{K\pi f}{f_s}\right)}{\sin\left(\frac{\pi f}{f_s}\right)}\right|^{4} \qquad (1)$$

RMS-Quantization noise on the output of a cascaded first order modulator with sinc filter can be calculated from the below equation.

$$V^{2}_{Qe,\,RMS}=2\int_{0}^{fs/2}|NTF(f)|^{2}\cdot|V_{Qe}(f)|^{2}\cdot|H(f)|^{2} \qquad (2)$$

We know that for first order noise shaping modulator

$$V_{Qe}(f)=\frac{V_{LSB}}{\sqrt{12f_s}} \qquad (3)$$

Substituting equation (2) in (1) we get

$$NTF(z)=1-z^{-1}$$

$$NTF(f)=1-e^{-\frac{j2\pi f}{fs}}$$

Further the magnitude of NTF(f) is given by

$$\mathrm{NTF(f)} = 2\sin\left(\frac{\pi f}{f_s}\right) \tag{4}$$

$$V^2_{Qe,\,RMS} = 2\int_0^{fs/2} \frac{V^2_{LSB}}{12f_s} \cdot 4\sin^2\left(\frac{\pi f}{f_s}\right) \cdot \left| \frac{1}{K} \frac{\sin\left(\frac{K\pi f}{f_s}\right)}{\sin\left(\frac{\pi f}{f_s}\right)} \right|^4 df \tag{5}$$

$$V^2_{Qe,\,RMS} = 8\int_0^{fs/2} \frac{V^2_{LSB}}{12f_s} \cdot \frac{1}{K^4} \left| \frac{\sin^4\left(\frac{K\pi f}{f_s}\right)}{\sin^2\left(\frac{\pi f}{f_s}\right)} \right| df \tag{6}$$

If we let $\theta = \frac{\pi f}{f_s}$

$$V^2_{Qe,\,RMS} = \frac{V^2_{LSB}}{12f_s} \cdot \frac{8}{K^4} \cdot \frac{f_s}{\pi} \int_0^{\pi/2} \left| \frac{\sin^4 K\theta}{\sin^2\theta} \right| d\theta \tag{7}$$

$$V^2_{Qe,\,RMS} = \frac{V^2_{LSB}}{12} \cdot \frac{8}{K^4} \cdot \frac{1}{\pi} \int_0^{\pi/2} \left| \frac{\sin^4 K\theta}{\sin^2\theta} \right| d\theta \tag{8}$$

In order to determine the quantization noise we have to solve the integration term below.

$$\int_0^{\pi/2} \left| \frac{\sin^4 K\theta}{\sin^2\theta} \right| d\theta$$

Let us prove the value of this integral is going to be $\frac{K\pi}{4}$. Let us take different values of K=1, 2

Case 1: K=1

$$\int_0^{\pi/2} \left| \frac{\sin^4\theta}{\sin^2\theta} \right| d\theta = \int_0^{\pi/2} \left| \sin^2\theta \right| d\theta = \int_0^{\pi/2} \left| \frac{1-\cos 2\theta}{2} \right| d\theta = \left[\frac{\theta}{2} - \frac{\sin 2\theta}{4} \right]_0^{\pi/2} = 1\cdot(\pi/4) \tag{9}$$

Case 2: K=2

$$\int_0^{\pi/2} \left| \frac{\sin^4 2\theta}{\sin^2\theta} \right| d\theta = \int_0^{\pi/2} \left| \frac{\sin^2 2\theta \cdot \sin^2 2\theta}{\sin^2\theta} \right| d\theta$$

$$= \int_0^{\pi/2} \left| \frac{4\sin^2\theta \cdot \cos^2\theta \cdot \sin^2 2\theta}{\sin^2\theta} \right| d\theta$$

$$= \int_0^{\pi/2} \left| 4\cos^2\theta \cdot 4\sin^2\theta \cdot \cos^2\theta \right| d\theta$$

$$= \int_0^{\pi/2} \left| 4\cos^4\theta \cdot 4(1-\cos^2\theta) \right| d\theta$$

$$= \int_0^{\pi/2} \left| 4\cos^4\theta \cdot 4\sin^2\theta \right| d\theta$$

$$= \int_0^{\pi/2} 16\left| \cos^4\theta - \cos^6\theta \right| d\theta \quad (10)$$

We can solve the above integrals using the following method.

$$\int \cos^4\theta d\theta = \int \cos^2\theta(1-\sin^2\theta)d\theta$$

$$= \int (\cos^2\theta - \cos^2\theta\sin^2\theta)d\theta$$

$$= \int \left(\frac{1+\cos 2\theta}{2} - \frac{\sin^2 2\theta}{4}\right)d\theta$$

$$= \frac{\theta}{2} + \frac{1}{4}\sin 2\theta - \frac{\theta}{8} + \frac{1}{32}\sin 4\theta$$

$$= \frac{3\theta}{8} + \frac{1}{4}\sin 2\theta + \frac{1}{32}\sin 4\theta$$

$$= \frac{12\theta}{32} + \frac{8}{32}\sin 2\theta + \frac{1}{32}\sin 4\theta$$

$$\int \cos^4\theta d\theta = \frac{1}{32}\left(12\theta + 8\sin 2\theta + \sin 4\theta\right) \quad (11)$$

Similarly the integral $\int \cos^6\theta d\theta$ can be reduced to as shown below.

$$\int \cos^6\theta d\theta = \frac{5\theta}{16} + \frac{15}{64}\sin 2\theta + \frac{3}{64}\sin 4\theta + \frac{1}{192}\sin 6\theta \quad (12)$$

Substituting eq (11) and eq (12) in eq (10) we get

$$\int_0^{\pi/2} \left| \frac{\sin^4 2\theta}{\sin^2\theta} \right| d\theta = 16\left(\frac{12}{32}\cdot\frac{\pi}{2} - \frac{5}{16}\cdot\frac{\pi}{2}\right) = 2\cdot\frac{\pi}{4} \quad (13)$$

From eq (9) and eq (13) we can conclude

$$\int_0^{\pi/2} \left| \frac{\sin^4 K\theta}{\sin^2\theta} \right| d\theta = K\cdot\frac{\pi}{4} \quad (14)$$

Substituting eq (14) in eq (8) we get

$$V^2_{Qe,\,RMS} = \frac{V^2_{LSB}}{12}\cdot\frac{8}{K^4}\cdot\frac{1}{\pi}\cdot K\cdot\frac{\pi}{4} \quad (15)$$

$$V^2_{Qe,\,RMS} = \frac{V^2_{LSB}}{12}\cdot\frac{2}{K^3} \quad (16)$$

$$V_{Qe,\,RMS} = \frac{V_{LSB}}{\sqrt{12}}\cdot\frac{\sqrt{2}}{K^{3/2}} \quad (17)$$

We can see that for values of K are greater than or equal to 2 the RMS quantization noise is reduced from the original value of $\frac{V_{LSB}}{\sqrt{12}}$.

7.16 What is the difference between a NS ADC and a Nyquist ADC?

Solution:

Fig. 1 shows the typical block diagrams for Nyquist ADCs and NS ADCs.

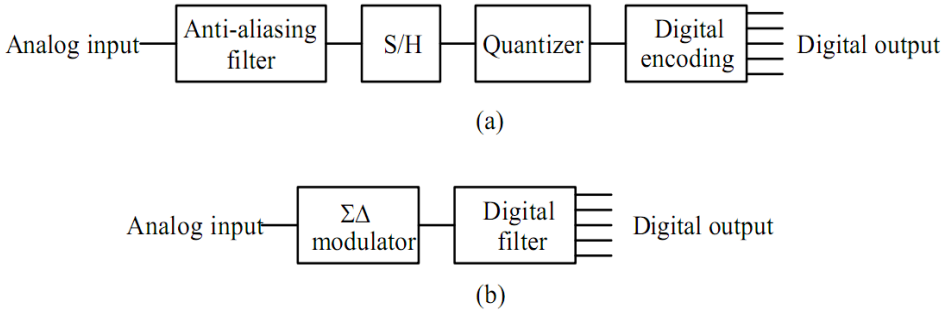


Figure 1 Typical block diagram for (a) Nyquist ADCs and (b) NS ADCs

The major differences between a NS ADC and a Nyquist ADC are:

1) Anti-aliasing filter

In a Nyquist ADC, an anti-aliasing filter is required to filter the analog input in order to minimize the aliasing effect. For a NS ADC, however, aliasing is usually not an issue since the analog input is oversampled (the sampling frequency is much higher than the Nyquist frequency). Thus anti-aliasing filter is usually not needed in NS ADCs.

2) Sample-and-hold (S/H) circuit

For Nyquist ADCs, S/H circuits are needed. Dedicated S/H is not required in a NS ADC. Discrete-time NS ADCs typically employ switched-capacitor circuits which perform the S/H function. Continuous-time NS ADCs do not require S/H.

3) Digital Encoding

The output of the quantizer in a Nyquist ADC needs to be converted to desired digital format. For example, the quantizer outputs of a Flash ADC are thermometer codes. Hence a circuit for converting the thermometer codes to binary format is usually needed. In a NS ADC, the encoding process is done by a digital filter.

4) Limit cycle oscillation

In Nyquist ADC, the output code doesn't vary for a DC input. In a NS ADC, however, a DC input results in a varying output codes due to the feedback topology in the NS modulator (limit cycle oscillation). Limit cycle oscillations are commonly observed in nonlinear systems. It is a self-exited periodic behavior which can cause undesired harmonic tones in the output spectrum of NS ADCs. Limit cycle oscillations also cause dead zone for a varying input (a small change in the input doesn't result in a change in the output code).

Solution by Geng Zheng

7.17 In your own words, describe ripple in the output of a digital filter connected to a NS modulator.

Solution:

The ripple is caused by the nature of the NS modulator. The feedback topology of a NS modulator makes its output always “busy” (alternating between one and zero) even when the modulator input is a DC value. For a DC input, the output of the NS modulator is a single repetitive code. For example, if the DC input is the common-mode voltage, the modulator output might be 0101010101, 001100110011, 000111000111, etc. This fact causes the digital filter output to have ripple. The closer the DC input to the common-mode voltage, the larger the magnitude of the ripple.

We know that a periodic signal will rise the energy in some certain frequencies. The repetitive modulator output results in harmonic tones in the frequency domain. Consider a DC common-mode input, the modulator output is a square wave with 50 % duty cycle. Using Fourier series we can write a square wave with frequency f_o as

$$X(t)=\frac{4}{\pi}\left(\sin(2\pi f_o t)+\frac{1}{3}\sin(2\pi\cdot 3\cdot f_o t)+\frac{1}{5}\sin(2\pi\cdot 5\cdot f_o t)+...\right) \quad (1)$$

which shows the harmonic terms. Different DC inputs will result in output square wave with different duty cycle and thus different ripple magnitudes and frequencies at the filter output.

Solution by Geng Zheng

7.18 Does adding a dither signal to the input of a NS modulator help reduce the peak-to-peak ripple in the digital filter output? Does it help to break up tones in the filter's output?

Solution:

Adding a dither signal to the input of a NS modulator doesn't help reduce the peak-to-peak ripple in the digital filter output. In fact, it may cause the filter output to have larger peak-to-peak ripple if the filter doesn't average enough. However, adding a dither signal does help to break up tones in the filter's output in the spectrum. The dither signal, random noise, help to spread the energy of the NS modulator output to wider spectrum. That is, the total energy of the modulator is still the same but break up into more frequency components.

7.19 Derive Eq. (7.26).

Solution:

Let's get started with drawing the block diagram of a NS modulator with forward gain G_F, the product of the integrator gain G_I and comparator gain G_C, as shown in Fig. 1.

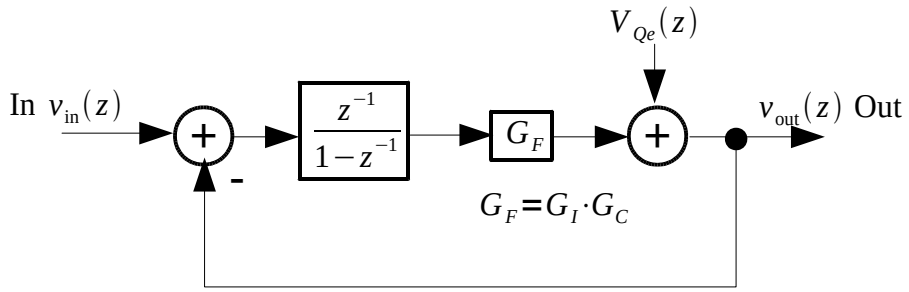


Figure 1 Block diagram of a NS modulator.

With Fig. 1, we can write

$$v_{out}(z) = \left(v_{in}(z) - v_{out}(z)\right) \cdot \frac{z^{-1}}{1-z^{-1}} \cdot G_F + V_{Qe}(z) \tag{1}$$

Multiplying both sides of Eq. 1 by $1-z^{-1}$ we have

$$v_{out}(z) \cdot (1-z^{-1}) = \left(v_{in}(z) - v_{out}(z)\right) \cdot z^{-1} \cdot G_F + V_{Qe}(z) \cdot (1-z^{-1}) \tag{2}$$

or

$$v_{out}(z) \cdot (1 - z^{-1} + G_F \cdot z^{-1}) = v_{in}(z) \cdot z^{-1} \cdot G_F + V_{Qe}(z) \cdot (1-z^{-1}) \tag{3}$$

Knowing $1 - z^{-1} + G_F \cdot z^{-1} = 1 + z^{-1}(G_F - 1)$, Eq. 3 becomes

$$v_{out}(z) = v_{in}(z) \cdot \frac{z^{-1} \cdot G_F}{1 + z^{-1}(G_F - 1)} + V_{Qe}(z) \cdot \frac{(1-z^{-1})}{1 + z^{-1}(G_F - 1)} \tag{4}$$

or Eq. (7.26).

7.20. Repeat Ex 7.3. if the integrator's gain is set to 0.5.

Ex 7.3. Show, using SPICE simulations and the modulator of Fig 7.2, that an integrator gain of 0.4 will result in an op-amp output range well with in the power supply range.

Sol)

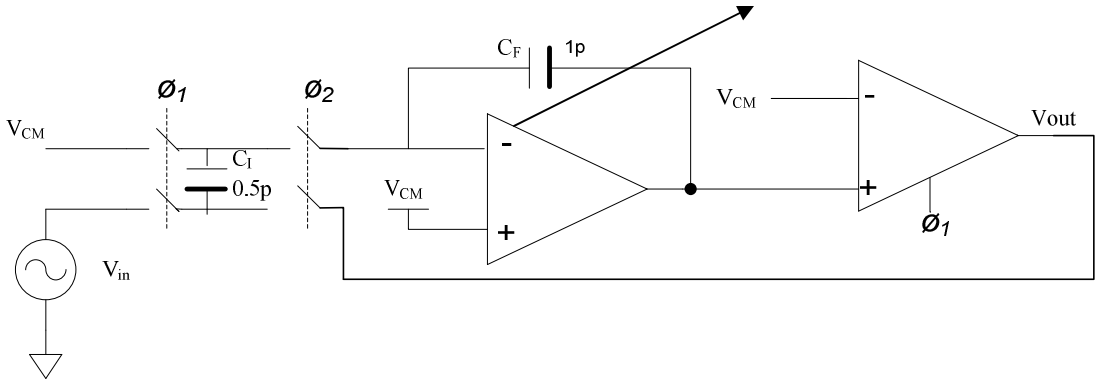


Figure 1. First order NS modulator with an integrator gain of 0.5 at f_s=100 MHz

The integrator gain is set by the capacitor C_I in the first order NS modulator shown in Figure 1. The integrator gain G_I is given by

$$G_I = \frac{C_I}{C_F} \qquad (1)$$

Given G_I=0.5, C_F=1p then C_I=0.5p.

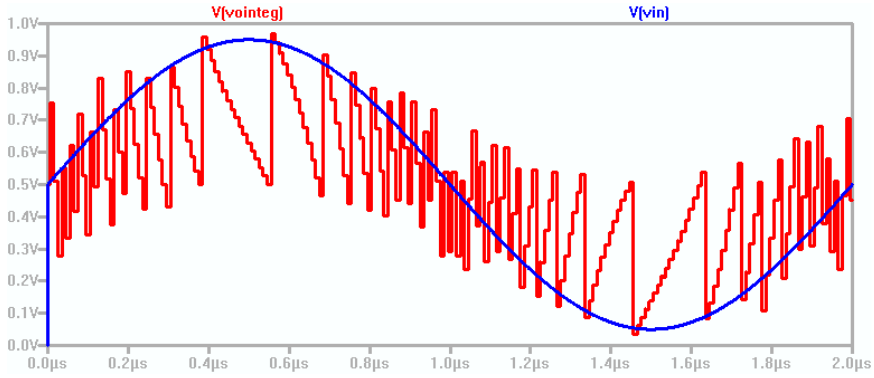


Figure 2. The output of the op-amp shown in Figure 1.

The output at the op amp (integrator output) is shown in Figure 2. The output swing is limited to 90% of the supply range. We can see (in Figure 3) that the integrator output saturates (goes beyond the range of power supply) when the value of C_I is 0.6p or greater (i.e. G_I is 0.6 or greater).

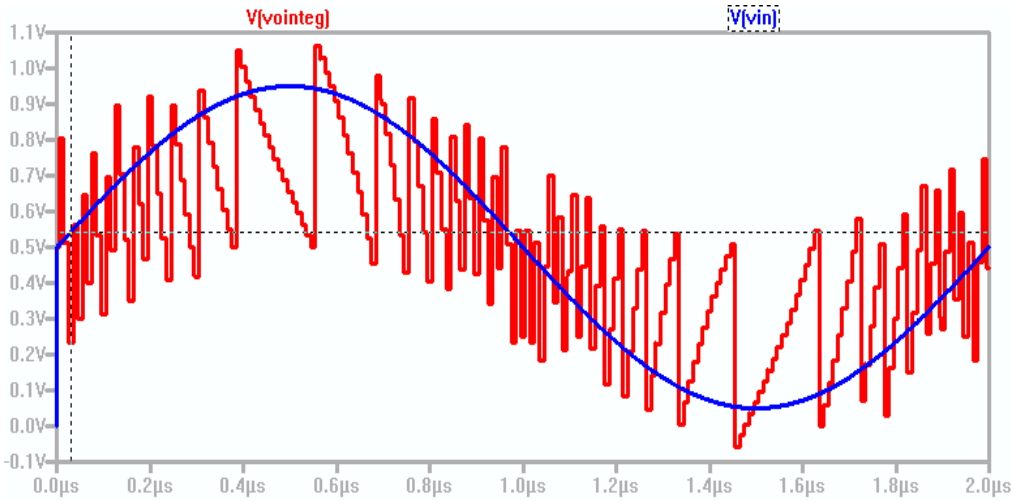


Figure 3. The output of the op-amp shown in Figure 1 with C_I=0.6p.

7.21. Estimate the range of G_c for the quantizer seen in Fig. 7.16. How does this compare to the range of G_c for the 1-bit quantizer seen in Fig. 7.15? Name two benefits of the 1-bit quantizer over multi-bit quantizer.

Sol. The transfer characteristic of a 3 bit quantizer is shown in Figure 1.

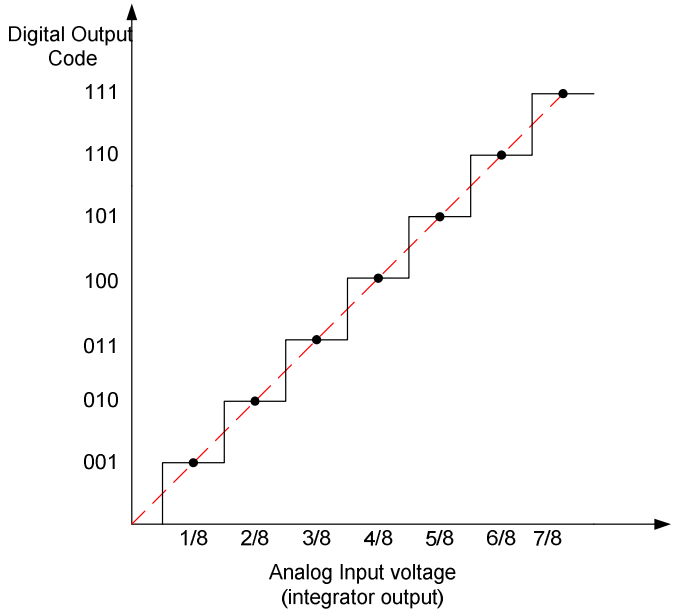


Figure 1. Transfer characteristic of a 3-bit ADC (quantizer)

The maximum gain of the 3-bit quantizer is given by $G_c = \frac{\triangle y}{\triangle x} = \frac{001-000}{(1/8)-0} = 8$. The minimum gain is 0 (i.e. for analog input voltages less than 1/8 the output digital code is zero).

Hence the range of G_c for the 3-bit ADC (quantizer) is given by

$$0 \le G_c \le 8 \qquad (1)$$

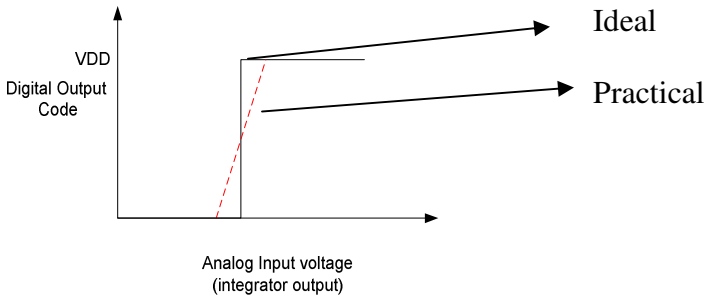


Figure 2. Transfer characteristic of a 1-bit ADC (quantizer)

In a 1-bit quantizer as seen in Figure 2 the output transition is abrupt hence gain is very high (in the order of thousand).

Harikrishna Rapole

Benefits of the 1-bit quantizer over multi-bit quantizer

1. The input to the multi bit quantizer has limited swing to represent all values of analog voltages. As the multi bit quantizer has less gain, the quantizer can only have limited output codes. Unless the output codes are scaled, the inputs allowed to the modulator are limited. But with a 1-bit quantizer which has high gain it is easy to represent all the output codes.
2. The limited gain of the multi-bit quantizer (G_c) might result in forward gain (G_F) that is not exactly unity. The gain of the active integrator can be increased to avoid this problem. Hence the requirements on the gain of the op amp are increased. In a 1-bit quantizer this is not a problem as the comparator has very high gain. Op amp need not have high gain to have forward loop gain (G_F) equal to unity.

7.22. Verify that Eq 7.30 is correct. Use pictures if needed.
Sol) This problem is an analysis of the effect of finite op-amp gain; hence the comparator in the first order NS modulator is removed to simplify the analysis. The discrete analog integrator (DAI) in the NS modulator is shown in the Figure 1.

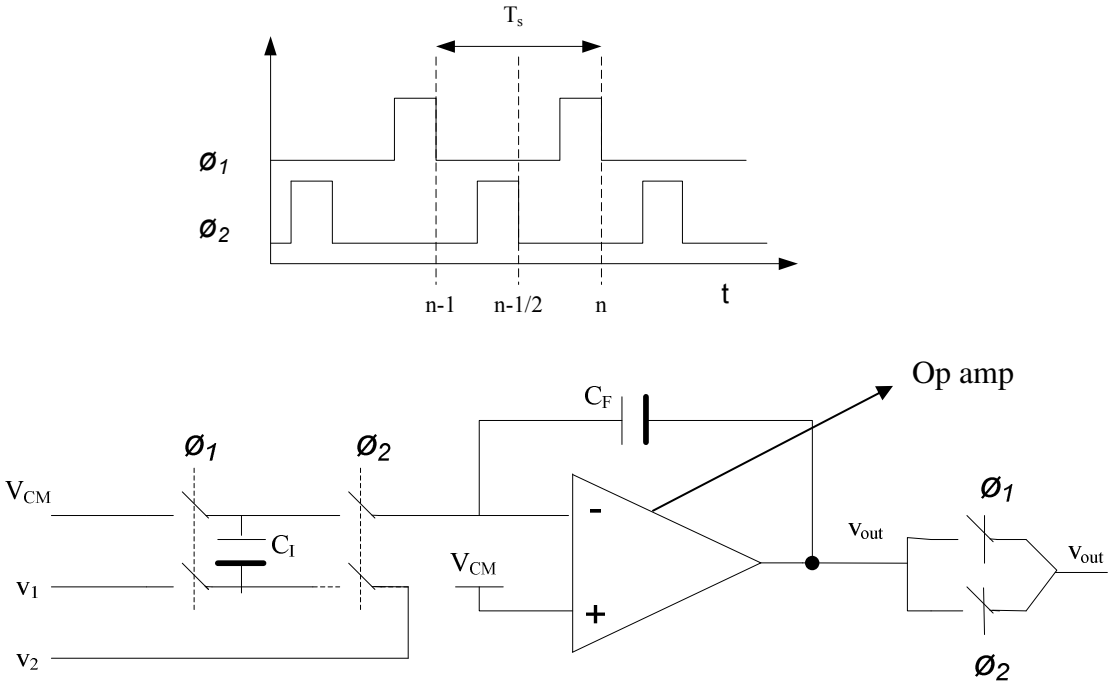


Figure 1. DAI in the First order NS modulator

The op amp has a finite open loop gain $A_{OL}(f)$.

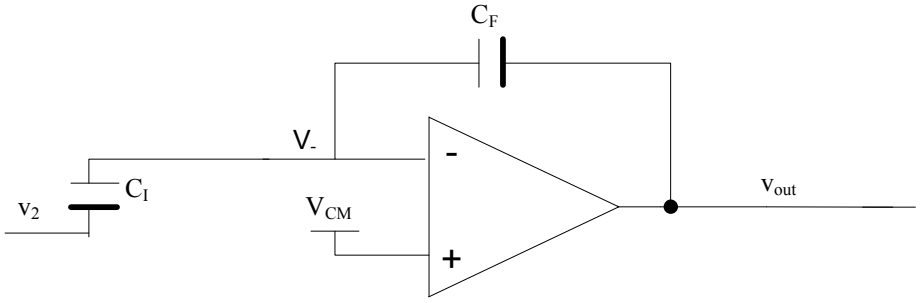


Figure 2. DAI when $Ø_2$ turns on

Figure2 shows the DAI when $Ø_2$ turns on. The open loop gain of the op amp is given by

$$A_{OL}(f)=\frac{v_{out}[nTs]}{(V_{CM}-V_{-})} \qquad (1)$$

$$V_{-}=V_{CM} - \frac{v_{out}[nT_s]}{A_{OL}(f)} \quad (2)$$

Let us consider the charge stored on the C_I capacitor when $Ø_2$ switch turns on. Since one end of the capacitor is at v_2 and the other end is at V_{-}, the charge stored on the capacitor C_I at **$t=nT_s$** becomes

$$Q_2 = C_I(V_{-} - v_2[nT_s]) \quad (3)$$

$$Q_2 = C_I(V_{CM} - \frac{v_{out}[nT_s]}{A_{OL}(f)} - v_2[nT_s]) \quad (4)$$

Eq (4) verifies Eq 7.30.

7.23) ***In your own words, and without equations, describe integrator leakage. How would you relate integrator leakage, found in integrators that use an active element as seen in the NS modulators found in this chapter, to the passive integrators used in the NS modulators discussed in the last chapter?***

Sol)

In an active integrator, when the op-amp is not ideal i.e., it has finite gain then the op-amp does not hold its negative terminal at exactly virtual ground. Due to this, not all the charge stored on the input capacitor is transferred to feedback capacitor C_F. This charge that did not make it to the feedback capacitor is known as integrator leakage.

As mentioned above, the integrators that use an active element, have integrator leakage due to the op-amp not being ideal and not being able to transfer all the charge from the input capacitor to the feedback capacitor.

For first order passive NS modulator, were we use a passive integrator using RC circuit, the integrator leakage can arrive due to presence of a comparator offset. Because if the comparator has an offset(V_{os}), and if the negative terminal is held at Vcm, the positive terminal will be held at Vcm – V_{os} due to this the comparator will switch its output states a bit too early and not all the charge from the input capacitor C will be leaked off, this can lead to integrator leakage in passive integrators.

7.24) ***Would large parasitic op-amp input capacitance affect the settling time of a DAI? Verify your answer using simulations with ideal op-amps (infinite open-loop gain) and non-ideal op-amps (open-loop gains around the oversampling ratio, K).***

Sol)

If an op-amp has a large parasitic input capacitance, it will affect the settling time of a DAI. Let us consider figure 7.18, which shows the feedback factor in the DAI.

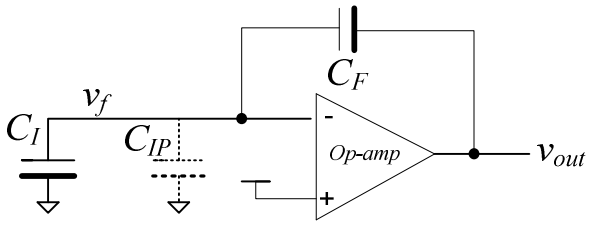


Figure 1: Input parasitic Capacitor of the op-amp

Assuming the settling time of the op-amp is linear, we can write the change in the op-amp's output assuming a dominate pole compensated op-amp as

$$v_{out} = V_{outfinal}(1 - e^{-t/\tau}) \quad \textbf{[1]}$$

Since the op-amp is assumed to be a dominant pole compensated, the magnitude response of a RC circuit looks like

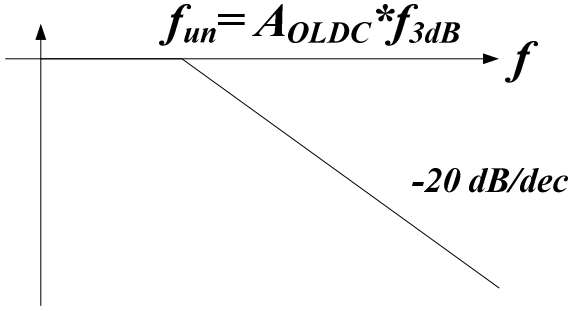


Figure 2: Frequency response

Where the gain band-width product is given by,

$$A_{OLDC} \cdot f_{3dB} = f_{un} \quad \textbf{[2]}$$

$$A_{OLDC} \cdot \frac{1}{2\pi RC} = f_{un} \quad \textbf{[3]}$$

$$\frac{V_{Out}}{V_{in}} \cdot \frac{1}{2\pi f_{un}} = RC \quad \textbf{[4]}$$

$$\frac{V_{Out}}{V_f} \cdot \frac{1}{2\pi f_{un}} = RC \quad \textbf{[5]}$$

$$\frac{1}{\left(\frac{V_f}{V_{Out}}\right)} \cdot \frac{1}{2\pi f_{un}} = RC \quad \textbf{[6]}$$

$$\frac{1}{\beta}\cdot\frac{1}{2\pi f_{un}} = RC = \tau \quad \textbf{[7]}$$

For a DAI without any input parasitic capacitance, the feedback factor β is given by,

$$\beta = \frac{C_F}{C_F + C_I} \quad \textbf{[8]}$$

But for a DAI with input parasitic capacitance of C_{IP}, as shown in the Fig. 1, we have the input parasitic capacitance parallel to the input capacitance of the DAI, so the total capacitance on the input of the op-amp is now, $C_I + C_{IP}$.

Therefore the feedback factor now becomes,

$$\beta = \frac{C_F}{C_F + C_I + C_{IP}} \quad \textbf{[9]}$$

And Eq. 1 becomes,

$$v_{out} = V_{outfinal}\left(1 - e^{-t/\left(\frac{1}{\beta}\cdot\frac{1}{2\pi f_{un}}\right)}\right) \quad \textbf{[10]}$$

$$v_{out} = V_{outfinal}\left(1 - e^{-2\pi\beta\cdot f_{un}\cdot t}\right) \quad \textbf{[11]}$$

$$v_{out} = V_{outfinal}\left(1 - e^{-2\pi\frac{C_F}{C_F+C_I+C_{IP}}\cdot f_{un}\cdot t}\right) \quad \textbf{[12]}$$

Therefore, we see that the op-amp will take longer to settle to its final value due to the presence of the input parasitic capacitor.

Settling time of an op-amp is defined as the time it takes for the output to settle to less than 1% of its final value. In the figures below, the point at which the output has reached 99% of its final value is highlighted to measure the settling time.

An ideal op-amp can hold both the positive and negative inputs at a constant voltage due to its high-gain. This will basically hold the charge on the input parasitic capacitor at a constant and the presence of the input parasitic capacitor would not affect the settling time of the output of the integrator.

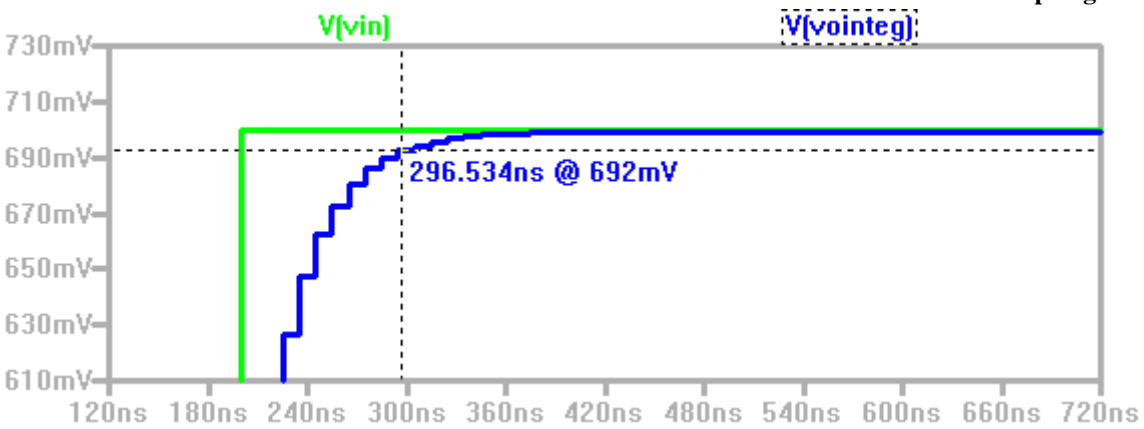


Figure 3: Ideal op-amp setting time without any input parasitic capacitor

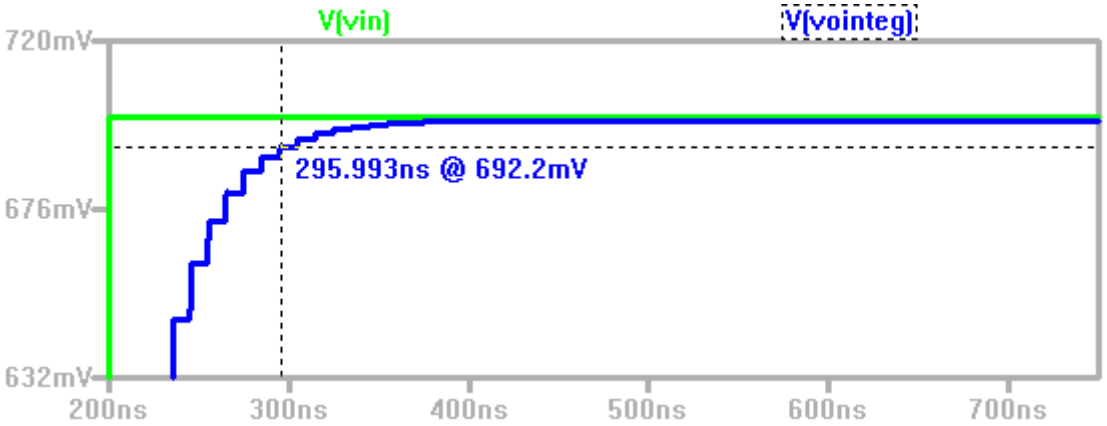


Figure 4: Ideal op-amp setting time with input parasitic capacitor

We see from Figs. 3 and 4 that the settling time of the ideal op-amp is not affected by the parasitic capacitor added at its input.

Shown below are simulations for non-ideal op-amp with and without parasitic capacitor.

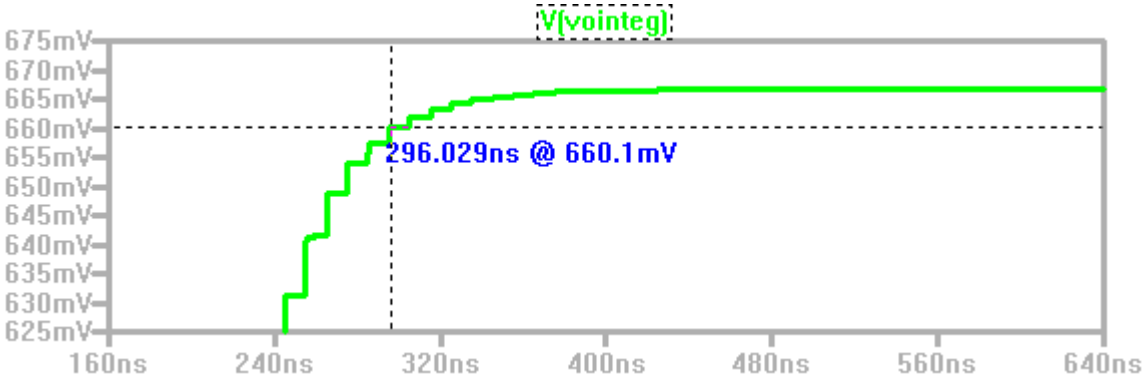


Figure 5: Non-ideal op-amp without input parasitic capacitor

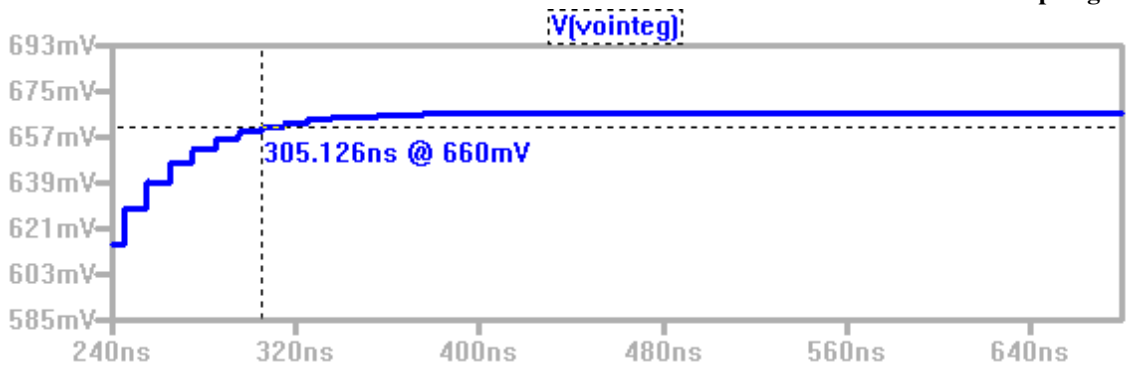


Figure 6: Non-ideal op-amp with input parasitic capacitor

From Figs 5 and 6 we see that when the input parasitic capacitor is added to the non-ideal op-amp's negative input, the output of the integrator takes longer to settle to its final value.

Kaijun Li
Problem 7.25
In your own words, how does over-sampling affect input-referred offset/noise and the effects of a jittery clock on an NS data converter?

Solution:
As shown in equations (7.44) and (7.45) in the textbook, the modulator's input-referred offset/noise passing through an ideal low-pass filter with a bandwidth of $B(=f_s/2K)$ results in

$$V_{n,ckt}(f) = \frac{V_n}{\sqrt{f_s}} \quad \text{for } f<f_s/2 \tag{7.44}$$

$$V_{ckt,RMS} = \sqrt{2 \cdot \int_0^B \frac{V_n^2}{f_s} \cdot df} = \frac{V_n}{\sqrt{K}} \tag{7.45}$$

The RMS value for clock jitter is found by

$$V_{jitter,RMS} = \sqrt{P_{AVG,jitter}} = \frac{1}{K} \cdot \left[\sigma \cdot \frac{V_p}{\sqrt{2}} \cdot 2\pi f_{in} \right]^2 \tag{5.51}$$

The noise contribution can be calculated as

$$V_{n,RMS} = \sqrt{V_{Qe,RMS}^2 + V_{jitter,RMS}^2 + V_{ckt,RMS}^2} \tag{7.46}$$

It is noted that the averaging filter (low-pass filter) reduces both the input-referred offset/noise and the clock jitter noise by K.
The signal-to-noise ratio (SNR) of the NS data converter is:

$$SNR = 20 \log \frac{V_p / \sqrt{2}}{V_{n,RMS}}$$

Therefore, the over-sampling or averaging helps the overall performance of the NS data converter in terms of SNR.

Kaijun Li
Problem 7.26
Determine the transfer function of the DAI shown in Fig. 7.20.

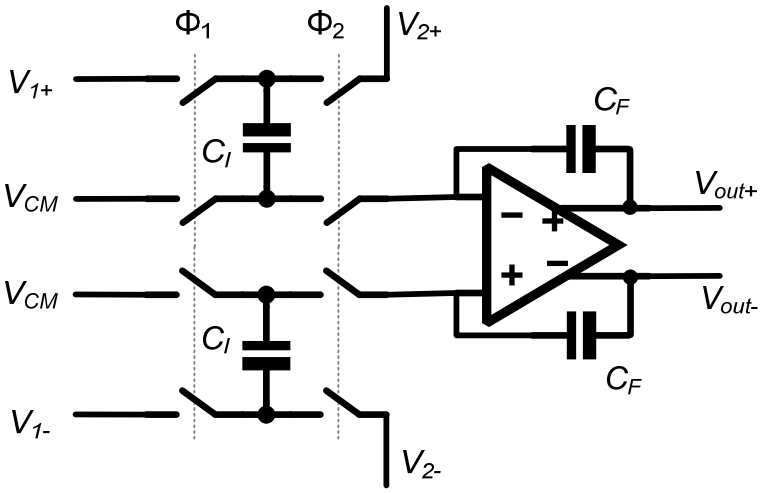
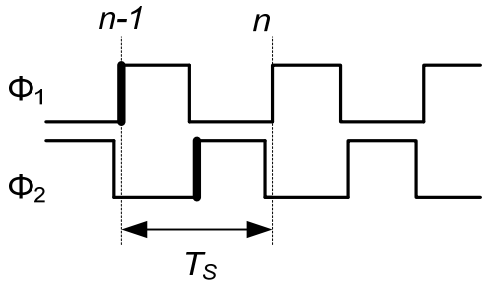


Fig. 7.20 Fully-differential discrete-analog integrator (DAI) implementation

Solution:
The transfer function of the fully-differential DAI can be derived similarly as the single-ended DAI. To determine the transfer function of the DAI, it is important to understand the timing which is drawn in following figure.



When Φ_1 switches open at (n-1/2)T_s or n-1/2, the charge stored on the capacitor C_I are:

$$Q_{1(top)} = C_I\left(V_{CM} - v_{1+}\left[(n-1/2)T_s\right]\right) \quad (1)$$

$$Q_{1(bottom)} = C_I\left(V_{CM} - v_{1-}\left[(n-1/2)T_s\right]\right) \quad (2)$$

When Φ_2 switches close, the charge on the capacitor C_I are:

$$Q_{2(top)} = C_I\left(V_{CM} - v_{2+}\left[nT_s\right]\right) \quad (3)$$

$$Q_{2(bottom)} = C_I\left(V_{CM} - v_{2-}\left[nT_s\right]\right) \quad (4)$$

The difference $Q_1 - Q_2$ is

$$Q_{1(top)} - Q_{2(top)} = C_I\left(v_{2+}\left[nT_s\right] - v_{1+}\left[(n-1/2)T_s\right]\right) \quad (5)$$

$$Q_{1(bottom)} - Q_{2(bottom)} = C_I\left(v_{2-}\left[nT_s\right] - v_{1-}\left[(n-1/2)T_s\right]\right) \quad (6)$$

$Q_1 - Q_2$ is transferred to the capacitors C_F which can be written as

$$Q_{1(top)} - Q_{2(top)} = -C_F\left(v_{out+}\left[nT_s\right] - v_{out+}\left[(n-1)T_s\right]\right) \quad (7)$$

$$Q_{1(bottom)} - Q_{2(bottom)} = -C_F\left(v_{out-}[nT_s] - v_{out-}[(n-1)T_s]\right) \tag{8}$$

Therefore, by equalizing equations (5)-(8), and knowing that $V_{out} = v_{out+} - v_{out-}$, $V_1 = v_{1+} - v_{1-}$, and $V_2 = v_{2+} - v_{2-}$, we have

$$C_I\left(V_2[nT_s] - V_1[(n-1/2)T_s]\right) = -C_F\left(V_{out}[nT_s] - V_{out}[(n-1)T_s]\right) \tag{9}$$

Taking the z-transform of equation (9), we get

$$V_{out}(z) = \frac{C_I}{C_F} \cdot \frac{V_1(z)\cdot z^{-1/2} - V_2(z)}{1 - z^{-1}} \tag{10}$$

So the transfer function of the fully-differential DAI is the same as that of the single-ended DAI.

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7.27 Derive Eq. (7.51).

Equation 7.51 is the *RMS* quantization noise for a second order discrete noise shaping (NS) modulator.

$$V_{Qe,RMS} \approx \frac{V_{LSB}}{\sqrt{12}} \cdot \frac{\pi^2}{\sqrt{5}} \cdot \frac{1}{K^{5/2}}$$

To begin the derivation we must understand why the following assumptions are made:

- Bennett's criterion holds
- All of the quantization noise falls within the Nyquist frequency

When Bennett's criterion is met the quantization noise of a 1-bit quantizer (with feedback that relaxes the second criteria) will have a flat response with *RMS*, voltage spectral density, and power spectral density of:

$$V_{Qe,RMS} = \frac{V_{LSB}}{\sqrt{12}} \ (V)$$

$$V_{Qe}(f) = \frac{V_{LSB}}{\sqrt{12 f_s}} \ (V/\sqrt{Hz})$$

$$V_{Qe}^2(f) = \frac{V_{LSB}^2}{12 f_s} \ (V^2/Hz)$$

Using the second-order NS modulator with an over sampling ratio of *K* we can determine the filter bandwidth to be:

$$B = \frac{f_s}{2K}$$

To determine the quantization noise that remains after being passed through a filter with bandwidth of *B* we need to find the magnitude of the noise transfer function (*NTF*). We know that the second order NS modulator modulates the quantization noise with a second-order differentiator, so:

$$NTF = (1 - z^{-1})^2 = \left(1 - e^{-j 2\pi \frac{f}{f_s}}\right)^2$$

The magnitude of this transfer function is (review section 1.2.2):

$$|NTF| = 4 \left| \sin^2 \pi \frac{f}{f_s} \right|$$

We can integrate the power spectral density of the modulated quantization noise over the bandwidth of interest to determine the remaining noise after filtering.

$$V_{Qe,RMS}^2(f) = 2\int_0^B |NTF|^2 \left|V_{Qe}(f)\right|^2 df = 32\int_0^B \left|\sin^2 \pi\tfrac{f}{f_s}\right|^2 \left|\frac{V_{LSB}}{\sqrt{12 f_s}}\right|^2 df = 32\frac{V_{LSB}^2}{12 f_s}\int_0^B \sin^4\left(\pi\tfrac{f}{f_s}\right) df$$

When $f_s >> f$ we can use Taylor series expansion of the trigonometric function and approximate:

$$\sin x = \sum_{n=0}^{\infty} \frac{(-1)^n}{(2n+1)!} x^{2n+1} = x - \frac{x^3}{3!} + \frac{x^5}{5!} \cdots$$

$$\sin x = x$$

For small x, which is the case as long as $f_s >> f$.

$$32\frac{V_{LSB}^2}{12 f_s}\int_0^B \sin^4\left(\pi\tfrac{f}{f_s}\right) df = 32\frac{V_{LSB}^2}{12 f_s}\int_0^{\frac{f_s}{2K}} \left(\pi\frac{f}{f_s}\right)^4 df = 32\frac{V_{LSB}^2}{12 f_s}\frac{\pi^4}{{f_s}^4}\int_0^{\frac{f_s}{2K}} f^4 df = 32\frac{V_{LSB}^2}{12 f_s}\frac{\pi^4}{{f_s}^4}\frac{1}{5}\frac{f_s^5}{32K^5}$$

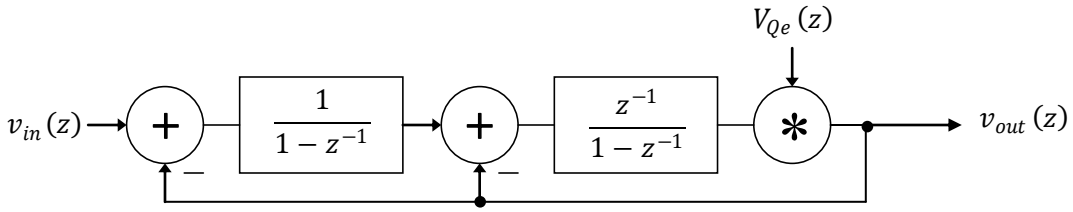
$$V_{Qe,RMS}^2(f) = \frac{V_{LSB}^2}{12}\frac{\pi^4}{5}\frac{1}{K^5}$$

Taking the square root:

$$V_{Qe,RMS}(f) \approx \frac{V_{LSB}}{\sqrt{12}}\frac{\pi^2}{\sqrt{5}}\frac{1}{K^{5/2}} \left(V/\sqrt{Hz}\right)$$

7.28 Sketch the implementation of the full-differential second-order NS modulator.

The block diagram of the second-order modulator is seen below.



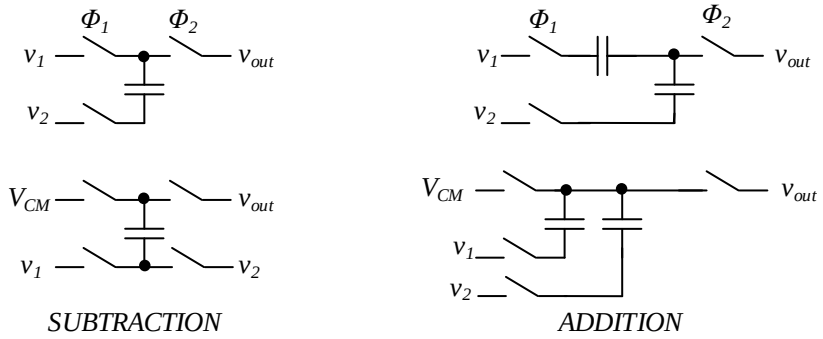
F-1 Block diagram of a second-order NS modulator

The block diagram leads to the following transfer function:

$$v_{out}(z) = z^{-1}v_{in}(z) + (1-z^{-1})^2 V_{Qe}(z)$$

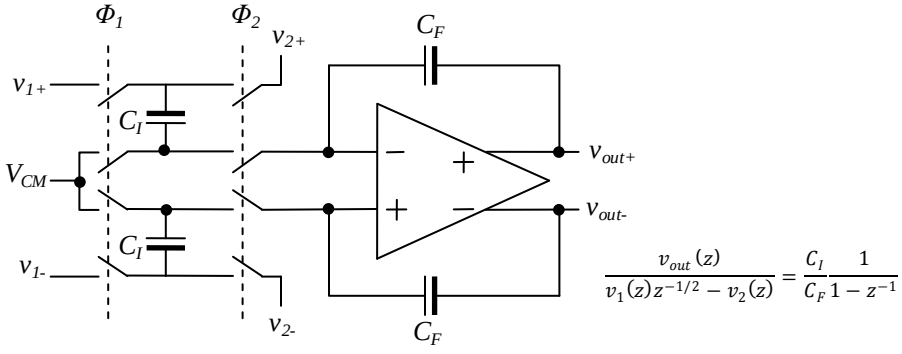
This equation shows that the noise is modulated with a second order response while the input signal is delayed. Filtering the output signal will remove the quantization noise in a particular bandwidth for $f_s >> f$.

Before implementing F-1 with fully differential discrete analog integrators (DAI) let's review addition and subtraction using switched capacitors by viewing F-2.



F-2 Reviewing subtraction and addition using switched capacitors

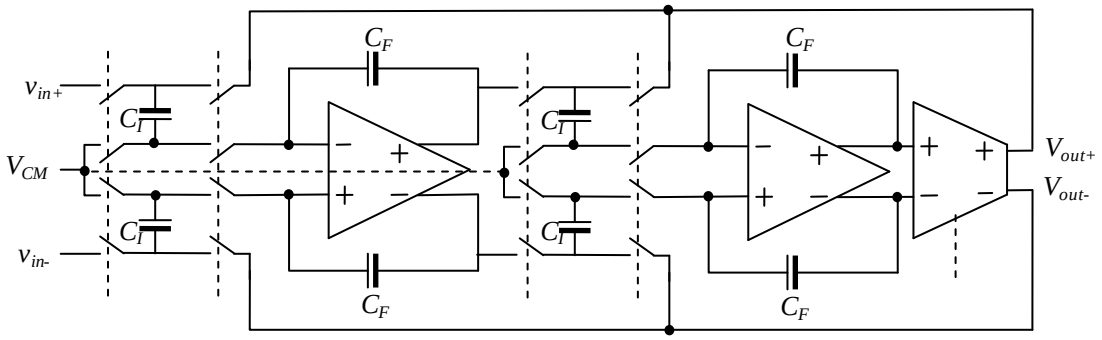
The block diagram of F-1 allows us to use known configurations to implement a second-order NS modulator. Let's look at the non-delaying integrator developed in chapter 2:



F-3 Fully-differential discrete analog integrator (DAI)

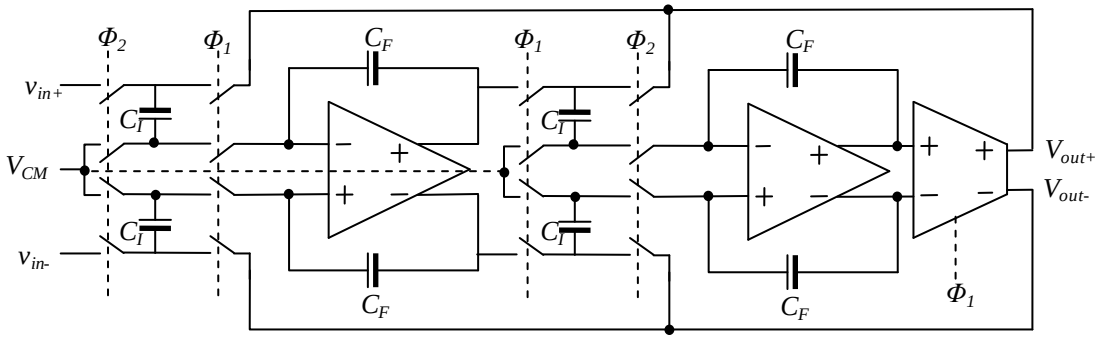
F-3 shows the fully-differential implementation of the non-delaying integrator. Notice that the v_2 signal is subtracted from the input signal. This will allow us to feedback the output signal to the v_2 node and perform the subtraction seen in F-1. To create a delaying integrator we simply connect to the output through a Φ_1 switch to introduce a clock cycle delay (z^{-1}) from the input to the output.

To implement F-1 with fully differential DAIs let's place two in parallel and add a comparator. We will leave the clock signals off and just connect it up so that we can analyze how to clock the modulator.



F-4 Fully-differential second-order NS modulator without clock signals

We know we want the second integrator to be delaying so if we clock the input with Φ_1 then we need to clock the comparator with Φ_1. Since the output of the first integrator will be connected with Φ_1 then we need to clock its input with Φ_2 to have it become a non-delaying integrator.

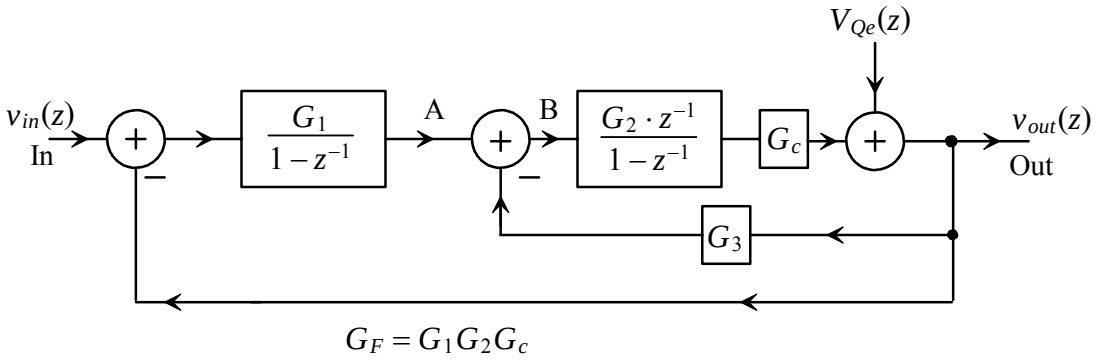


F-4 Fully-differential second-order NS modulator with clock signals

Jake Baker

7.29 Derive Eq. (7.61).

The block diagram, Fig. 7.32, used in this derivation is seen below.



The signal at point A is

$$\frac{(v_{in} - v_{out}) \cdot G_1}{1 - z^{-1}}$$

while the signal at point B is

$$\frac{(v_{in} - v_{out}) \cdot G_1}{1 - z^{-1}} - G_3 \cdot v_{out}$$

We can then write

$$\frac{(v_{in} - v_{out}) \cdot z^{-1} G_1 G_2 G_c}{(1 - z^{-1})^2} - \frac{G_2 G_3 G_c \cdot z^{-1} v_{out}}{(1 - z^{-1})} + V_{Qe} = v_{out}$$

and

$$\frac{z^{-1} G_1 G_2 G_c}{(1 - z^{-1})^2} \cdot v_{in} + V_{Qe} = v_{out}\left(1 + \frac{z^{-1} G_1 G_2 G_c}{(1 - z^{-1})^2} + \frac{G_2 G_3 G_c \cdot z^{-1}}{(1 - z^{-1})}\right)$$

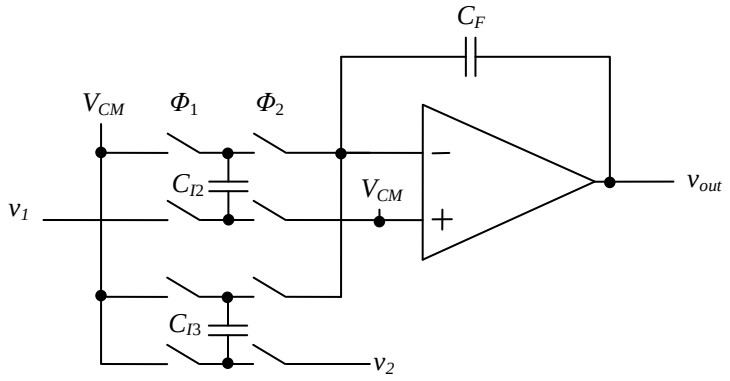
Multiplying both sides by $(1 - z^{-1})^2$ gives

$$z^{-1} G_1 G_2 G_c \cdot v_{in} + V_{Qe}(1 - z^{-1})^2 = v_{out}\left[(1 - z^{-1})^2 + z^{-1} G_1 G_2 G_c + G_2 G_3 G_c \cdot z^{-1} \cdot (1 - z^{-1})\right]$$

and finally

$$v_{out}(z) = \frac{G_1 G_2 G_c \cdot z^{-1} v_{in}(z) + (1 - z^{-1})^2 \cdot V_{Qe}(z)}{1 + z^{-1} \cdot (G_1 G_2 G_c + G_2 G_3 G_c - 2) + z^{-2} \cdot (1 - G_2 G_3 G_c)}$$

7.30 Sketch the fully-differential equivalent of Fig. 7.33.



F-1 Sketch of Figure 7.33

Let's derive the transfer function of this schematic assuming Φ_2 goes low at time nT_s and that the charge flows to the output over an entire clock cycle. At nT_s the charge from v_2 is transferred without a delay.

$$Q_2 = (V_{CM} - v_2)C_{I3}$$

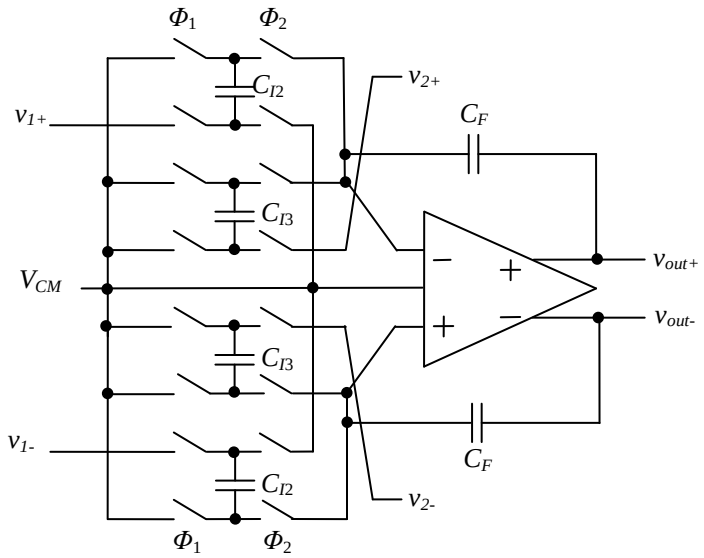
$$Q_1 = \left(V_{CM} - v_1 z^{-1/2}\right)C_{I2}$$

$$v_{out}\,C_F - v_{out}\,z^{-1}C_F = (V_{CM} - v_2)C_{I3} - \left(V_{CM} - v_1 z^{-1/2}\right)C_{I2}$$

$$v_{out}\,C_F - v_{out}\,z^{-1}C_F = v_1 z^{-1/2}C_{I2} - v_2 C_{I3}$$

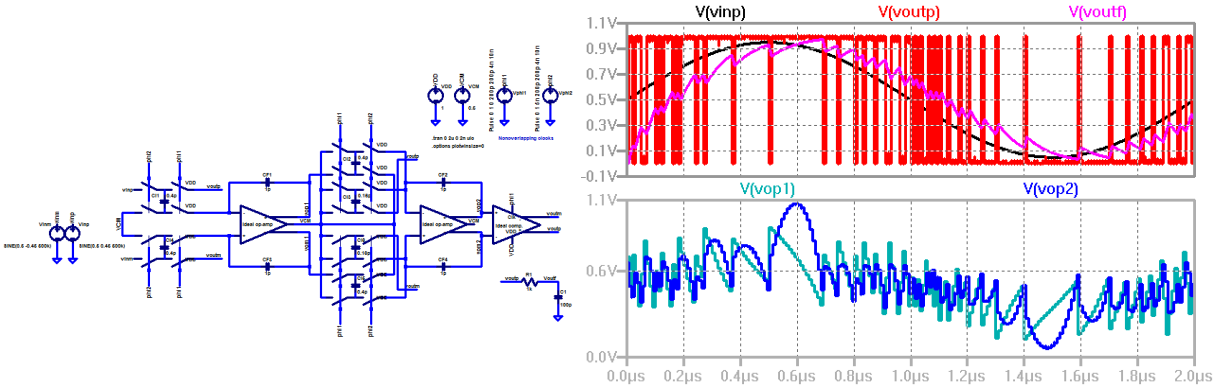
$$v_{out} = v_1 \frac{z^{-1/2}}{1 - z^{-1}}\frac{C_{I2}}{C_F} - v_2 \frac{1}{1 - z^{-1}}\frac{C_{I3}}{C_F}$$

To implement this schematic with fully differential op-amps we just use the switched-capacitor network on both the inverting and non-inverting inputs.



F-2 Sketch of fully-differential implementation of the circuit seen in F-1

To verify this fully-differential topology we can use _Fig7_36_MSD from the website with our fully-differential implementation. The schematic and simulation results are seen below.



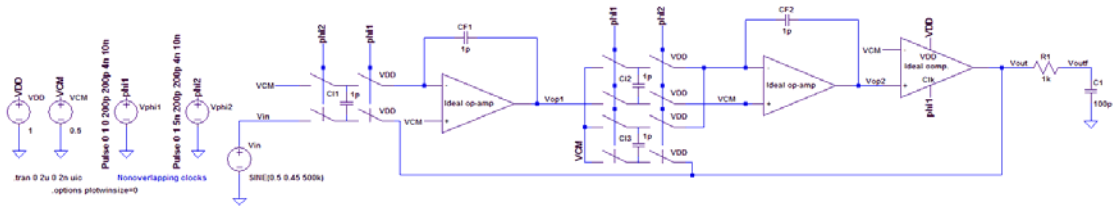
F-3 Schematic and simulation results of the fully-differential implementation

The simulation results in F-3 match that of Figure 7.36 proving that the topology was implemented correctly.

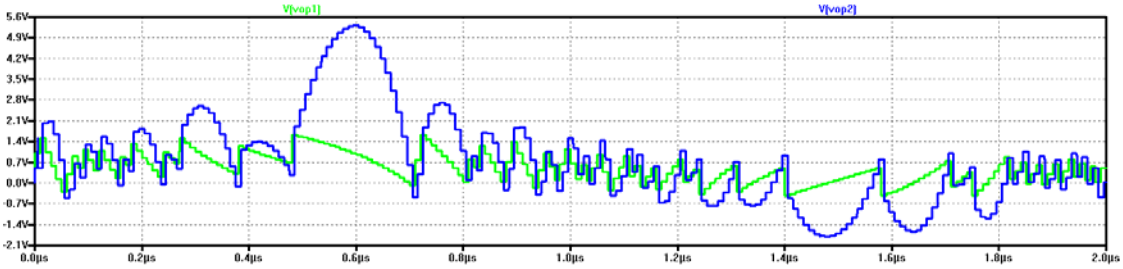
Jake Baker

7.31 Resimulate the modulator in Ex. 7.4 if the gains are set to one. Comment on the stability of the resulting circuit.

The simulation schematic of the modulator with the gains set to one is seen below.



The simulated outputs of the integrators is seen below.

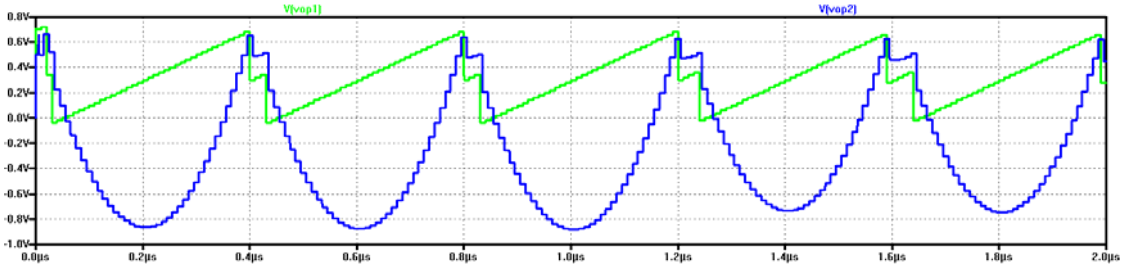


Knowing the power supply voltage is 1 V we see that the outputs of the integrators are swinging beyond the power supply rails. This simulation used ideal components and so the feedback loop remains stable. In a transistor implementation the outputs of the integrators are limited to the power supply rails so the integrators will saturate. In other words, the forward gain will drop towards zero and the loop will move towards instability. It should be pointed out that even if the loop doesn't become unstable the outputs of the integrators saturating will drastically reduce the modulator's SNR and so it should be avoided.

Jake Baker

7.32 Resimulate the modulator in Ex. 7.4 if the input is only 50 mV. Comment on the stability of the resulting circuit.

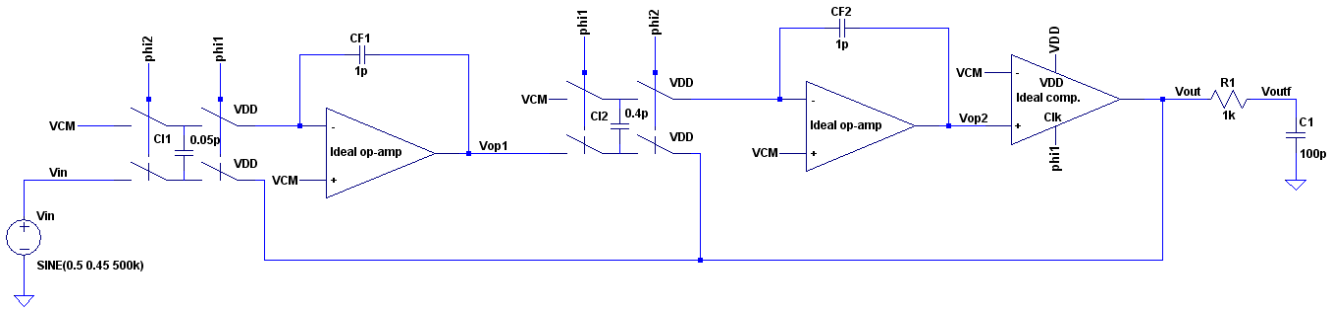
The simulation results showing the integrators' outputs are seen below. Knowing the power supply rails are ground and 1 V we see that the integrator outputs are not staying in this range (so the integrators will saturate in a real circuit). This indicates stability is a concern (see Question 7.31). The simplest solution to this problem is to limit the input signal swing. Another solution is to further reduce the integrators' gains. The point is that **integrator saturation is bad** and should be avoided. Saturating integrators push the modulators towards instability and result in a reduction in SNR.



Jason Durand

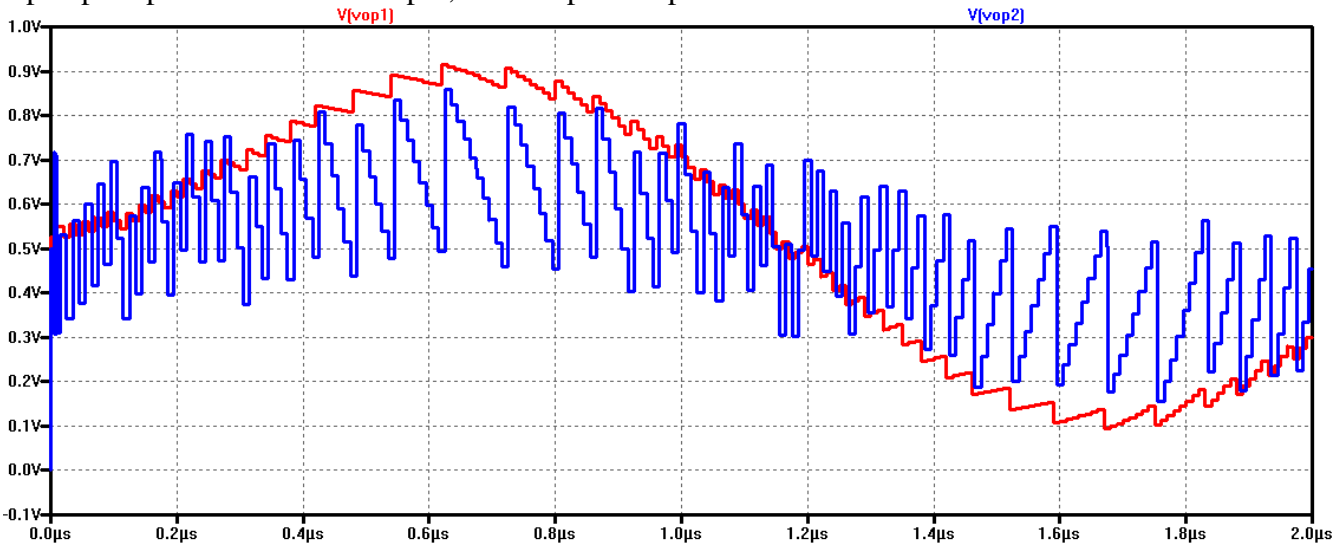
Problem 7.33 – Regenerate Fig 7.40 by selecting integrator gains so that the maximum output swing of any opamp is 800mV peak to peak.

Figure 7.40 is generated by the following spice simulation:



Nodes vop1 and vop2 are the opamp outputs, and in a real circuit, are limited in swing to the power rails, usually gnd and vdd. The gain of the overall system is one (due to the non-linearity if the comparator gain) but the gain of each integrator stage is important so that the output does not saturate, which can impact the SNR of the data converter. The gain of each integrator is the ratio of the input comparator to the feedback comparator, or C_I/C_F. To keep the outputs within the power supply rails, the gain of the first integrator is set extremely low (0.05) and the second is higher, (0.4).

Opamp outputs with 500kHz input, 900mV peak to peak.



The main possible problem with this is the size of the input capacitor of the first integrator, since a smaller capacitor moves more with a given amount of noise on the interconnects, and noise from the switches.

Jake Baker

7.34 Comment, in your own words, on why the actual *SNR* of a NS-based data converter can be worse than the ideal values calculated in the chapter.

1. The op-amp used in the integrator may have finite gain leading to integrator leakage, the charge stored on the switched-capacitors isn't fully transfered to the feedback capacitor in the integrator. This slopping of charge will reduce the *SNR*.

2. The op-amp's noise will add to the input signal and reduce the *SNR*. This may not be an issue in topologies using a large oversampling ratio since the bandwidth of the op-amp's noise is then relatively small.

3. The comparator, while one of the least critical components in the modulator, can also effect the *SNR*. The comparator's noise can have an effect too, though it's considerably less important than the op-amp's noise. The bigger issue is the comparator making a full output transition. If the output doesn't fully "decide" the effects on the *SNR* can be dramatic.

4. The thermal noise, kT/C, associated with the MOSFET switches will also reduce the modulator's *SNR*.

5. Using imperfect clock signals can have an effect on the *SNR* as discussed in Ch. 5. In continuous-time modulators these effects can be signifcant where the jittering clock signal adds to the varying delay of the clocked comparator. The effects of the comparator decision varying is considerably less of an issue in discrete-time modulators as long as the comparator makes a decision in $< T_S/2$. However, a varying clock signal, as discussed in Sec. 5.2, can still have an effect on the *SNR* in switched-capacitor circuits.

7.35 Derive Eq. (7.75). Make sure each step of the derivation includes comments. The equation in question is

$$N_{inc} = \frac{1}{6.02}\left[\left(20M + 10\right)\cdot \log K - 20\log\left(\frac{\pi^M}{\sqrt{2M+1}}\right)\right]. \qquad (7.75)$$

1. Definitions

A first order noise shaping modulator (NSM) has a noise transfer function (NTF) of

$$NTF\left(z\right) = 1 - z^{-1}, \qquad (1)$$

which is the representation of a digital differentiator. Higher order modulators differentiate the noise with the same transfer function, raised to the power of the modulator's order. Therefore, an Mth order NSM has

$$NTF\left(z\right) = \left(1 - z^{-1}\right)^M, \qquad (2)$$

which can be represented as

$$NTF\left(f\right) = \left(1 - e^{-j2\pi\frac{f}{f_s}}\right)^M \qquad (3)$$

in the frequency domain. Using Euler's identity, we can convert this to

$$NTF\left(f\right) = \sqrt{2\left(1 - \cos 2\pi\frac{f}{f_s}\right)}^M \qquad (4)$$

which, if we use the trigonometric identity

$$1 - \cos x = 2\sin^2\frac{x}{2}, \qquad (5)$$

we arrive at the useful version

$$NTF\left(z\right) = 2^M \sin^M\left(\pi\frac{f}{f_s}\right). \qquad (6)$$

The quantization noise of the NSM, $V_{Qe}(z)$, is represented in the frequency domain by

$$V_{Qe}(f) = \frac{V_{LSB}}{\sqrt{12 f_s}}. \qquad (7)$$

2. Modulation Noise

The magnitude of the modulation noise is the product of the magnitude of the quantization noise (7) with the magnitude of the NTF (6). This describes how the noise is shaped into the higher frequency range.

$$\left|NTF(f)\right|\cdot\left|V_{Qe}(f)\right| = \left|2^{M}\sin^{M}\frac{\pi f}{f_s}\right|\cdot\left|\frac{V_{LSB}}{\sqrt{12 f_s}}\right| \tag{8}$$

3. RMS Quantization Noise

In moving towards the goal of finding an equation for the increased number of bits (N_{inc}), we first need to find the signal to noise ratio (SNR), and to do that we first need to determine the amount of noise present in the bandwidth of interest. This derivation assumes the quantization noise of interest occupies the bandwidth 0 → B, where

$$B = {f_s}\big/{2K}. \tag{9}$$

K is the oversampling ratio and f_s is the clocking frequency. This derivation also assumes that the bandwidth is passed through an ideal low pass filter. With these assumptions stated, we can proceed to calculate the RMS quantization noise for the NSM from 0 to B. Using (8), and remembering to integrate on both sides of the frequency spectrum,

$$\begin{aligned} V_{Qe,RMS}^2 &= 2\int_0^B \left|NTF(f)\right|^2\cdot\left|V_{Qe}(f)\right|^2 df \\ &= 2\int_0^B\left[2^{M}\sin^{M}\frac{\pi f}{f_s}\right]^2\cdot\left[\frac{V_{LSB}}{\sqrt{12 f_s}}\right]^2 df \\ &= 2\cdot\frac{V_{LSB}^2}{12 f_s}\cdot 2^{2M}\cdot\int_0^B \sin^{2M}\frac{\pi f}{f_s}df. \end{aligned} \tag{10}$$

Here, if we assume that our input frequency is much, much less than our clocking frequency ($f << f_s$), then we can use the small angle approximation

$$\sin x \approx x. \tag{11}$$

Plugging (11) into (10) we find

$$\begin{aligned} V_{Qe,RMS}^2 &\approx 2\cdot\frac{V_{LSB}^2}{12 f_s}\cdot 2^{2M}\cdot\int_0^B\left(\frac{\pi f}{f_s}\right)^{2M} df \\ &\approx 2\cdot\frac{V_{LSB}^2}{12 f_s}\cdot 2^{2M}\cdot\frac{\pi^{2M}}{f_s^{2M}}\int_0^B f^{2M}df \\ &\approx 2\cdot\frac{V_{LSB}^2}{12 f_s}\cdot 2^{2M}\cdot\frac{\pi^{2M}}{f_s^{2M}}\left[\frac{f^{2M+1}}{2M+1}\right]_0^B. \end{aligned} \tag{12}$$

Plugging (9) into (12) we find

$$V_{Qe,RMS}^2 \approx 2 \cdot \frac{V_{LSB}^2}{12 f_s} \cdot 2^{2M} \cdot \frac{\pi^{2M}}{f_s^{2M}} \cdot \frac{f_s^{2M+1}}{2^{2M+1} \cdot K^{2M+1}}. \tag{13}$$

which reduces to

$$V_{Qe,RMS}^2 \approx \frac{V_{LSB}^2}{12} \cdot \frac{1}{2M+1} \cdot \frac{\pi^{2M}}{K^{2M+1}}. \tag{14}$$

Finally, the RMS quantization noise is

$$V_{Qe,RMS} \approx \frac{V_{LSB}}{\sqrt{12}} \cdot \frac{1}{\sqrt{2M+1}} \cdot \frac{\pi^{M}}{K^{M+1/2}}. \tag{15}$$

4. SNR_{ideal}

$$SNR_{ideal} = 20 \log \frac{V_P / \sqrt{2}}{V_{Qe,RMS}} \tag{16}$$

$$V_{LSB} = 1LSB = \frac{V_{REF^+} - V_{REF^-}}{2^N}, \text{ for N } \geq 2. \tag{17}$$

$$V_P = \frac{V_{REF^+} - V_{REF^-}}{2} \tag{18}$$

Plugging (17) into (15) and then that result along with (18) into (16) we find

$$SNR_{ideal} = 20 \log \frac{\frac{V_{REF^+} - V_{REF^-}}{2\sqrt{2}}}{\frac{V_{REF^+} - V_{REF^-}}{2^N \cdot \sqrt{12}} \cdot \frac{1}{\sqrt{2M+1}} \cdot \frac{\pi^M}{K^{M+1/2}}}$$

$$= 20 \log \left(2^N \cdot \frac{\sqrt{3}}{\sqrt{2}} \cdot \frac{\sqrt{2M+1} \cdot K^{M+1/2}}{\pi^M} \right) \tag{19}$$

$$= 6.02N + 1.76 - 20 \log \left(\frac{\pi^M}{\sqrt{2M+1}} \right) + (20M + 10) \cdot \log K.$$

We also know that

$$SNR_{ideal} = 6.02\left(N + N_{inc}\right) + 1.76. \qquad (20)$$

5. N_{inc}

The last step we need to take to find N_{inc} is to equate (19) and (20) and solve. Doing this we find

$$6.02N + 1.76 - 20\log\left(\frac{\pi^M}{\sqrt{2M+1}}\right) + \left(20M + 10\right)\cdot\log K = 6.02\left(N + N_{inc}\right) + 1.76$$

$$-20\log\left(\frac{\pi^M}{\sqrt{2M+1}}\right) + \left(20M + 10\right)\cdot\log K = 6.02N_{inc} \qquad (21)$$

$$N_{inc} = \frac{1}{6.02}\left[\left(20M + 10\right)\cdot\log K - 20\log\left(\frac{\pi^M}{\sqrt{2M+1}}\right)\right]$$

■

7.36 Resimulate Fig. 7.44 using a two-bit ADC and DAC.

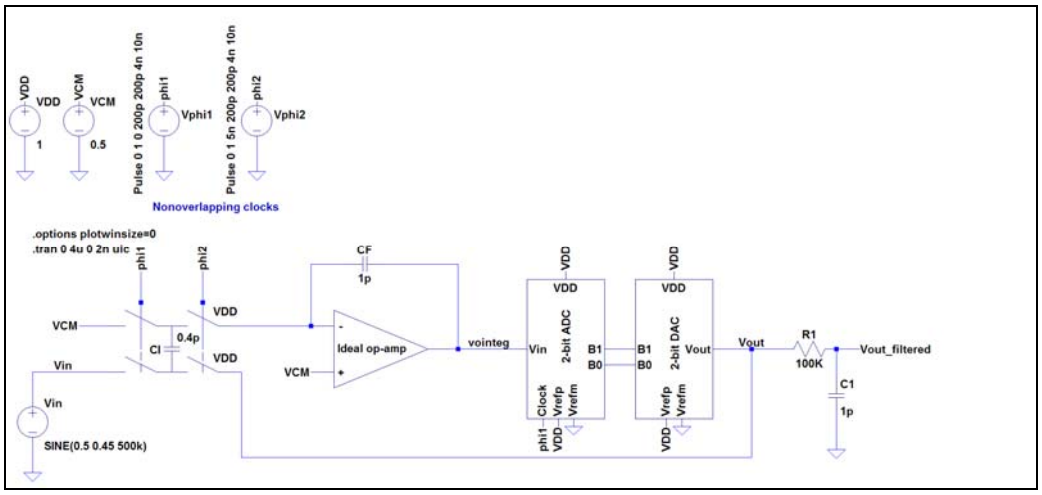


Figure 1. First-order 2-bit NS modulator.

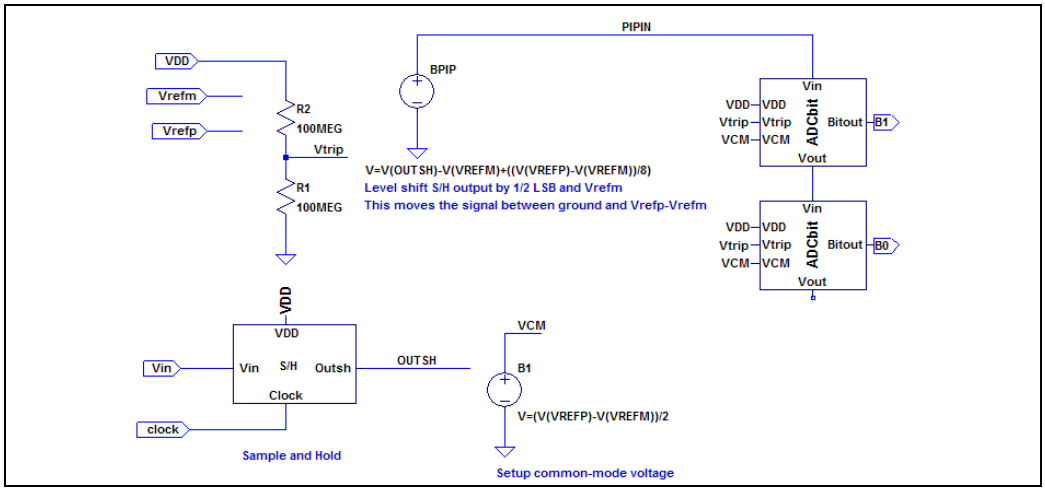


Figure 2. Ideal 2-bit ADC.

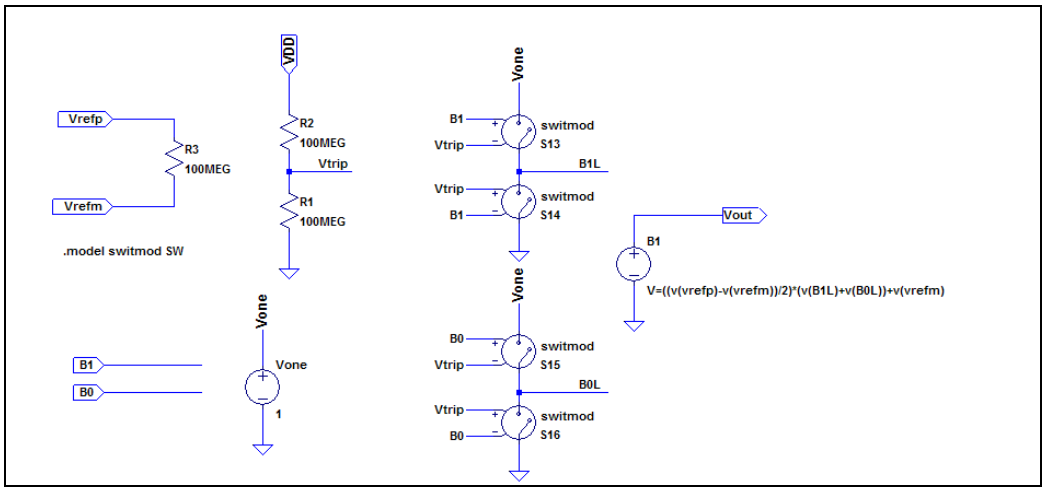


Figure 3. Ideal 2-bit DAC.

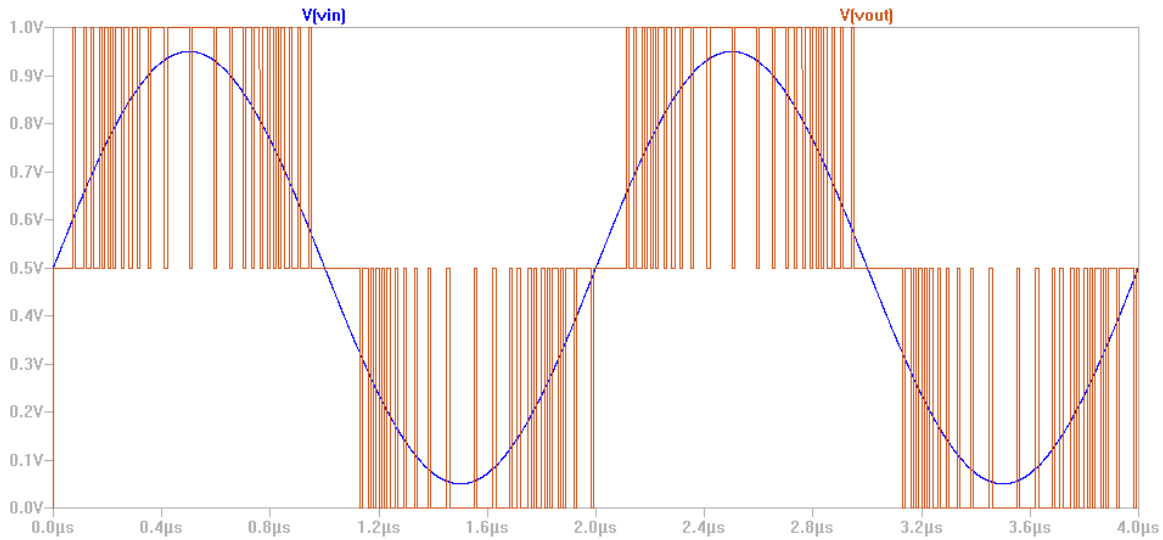


Figure 4. Simulation of the 2-bit first order NS modulator.

7.37 Sketch a possible implementation of a quantizer for the error feedback modulator shown in Fig. 7.48.

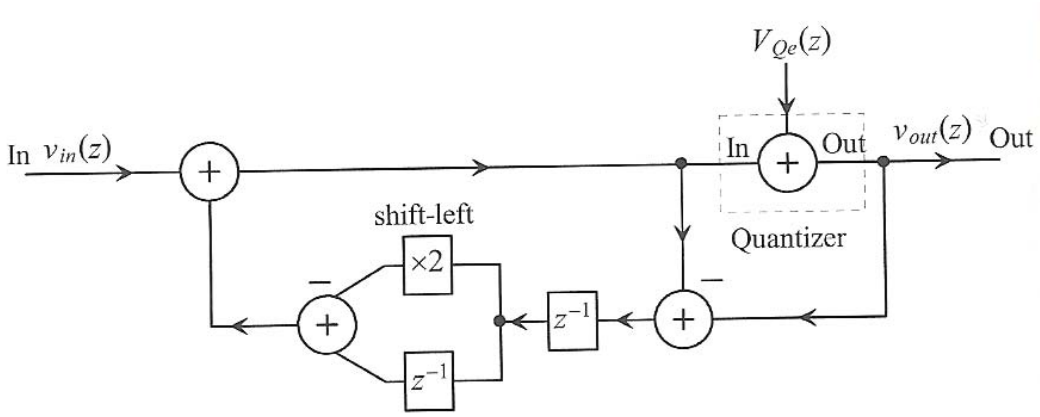


Figure 7.48 Block diagram of a second-order error feedback modulator.

The answer to this question is given in Fig. 7.49. For completeness it will be re-sketched here. The sketch in Fig. 7.49 implies the ability to send more than 1 bit to V_{out}. This implementation will assume that only the MSB gets sent out. Additionally, it will be assumed that the input to the quantizer is 4 bits and, to aid understanding, each bitline will be shown individually as opposed to being bussed.

Jake Baker

7.38 What transfer function does the following block diagram implement?

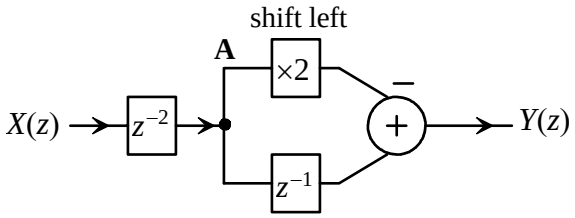


Figure 7.60 Circuit for question 7.38.

The signal at point A is

$$X(z) \cdot z^{-2}$$

so the output is

$$Y(z) = X(z) \cdot z^{-2} \cdot (z^{-1} - 2)$$

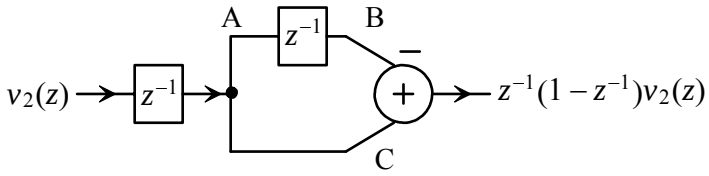
or

$$Y(z) = X(z) \cdot z^{-3} - 2 \cdot X(z) \cdot z^{-2}$$

Jake Baker

7.39 In Fig. 7.54 sketch the block diagram implementation of the circuit in series with the $v_2(z)$ output.

The circuit in series with this output has a transfer function of $z^{-1}(1-z^{-1})$ and a block diagram given by



The modulator output, $v_2(z)$, is 1-bit. The block z^{-1} is implemented with a single D-Flip-Flop so node A is also 1-bit in size. Nodes B and C are 1-bit as well. However, consider what happens if node B is a 1 and node C is a 0. The final output is −1. How do we represent this number? What we need to do, prior to applying the data to the adder, is change the 1-bit code into a two's complement number. This means

$$1 \rightarrow 001\ (+1)$$

and

$$0 \rightarrow 111\ (-1)$$

or, in other words, we increase the word size to 3-bits by tying the lower bit high and extending the sign bit.

If node C is a 1 (+1) and node B is a 0 (−1) the final output is 001 − 111 = 010 (+2). If nodes B and C are both 1s then the output is 0 (000). This can only happen if the word size is > 1.

In other words, a modulator output of 1 is change to +1 = V_{REFP} (= *VDD* in the book) and a modulator output of 0 is changed to −1 = V_{REFM} (= 0 *V* in the book). If nodes B and C are always high, or always low, then the output of the circuit is 000, or V_{CM} (= *VDD*/2 in the book).

7.40) ***Derive the transfer function of the topology seen in Fig. 7.61 (show details of your derivation). What is the input common-mode voltage of the op-amp? Is this a concern when not using a negative supply voltage? If the input signals have a common-mode of VDD/2, does this affect the common-mode voltage of the circuit's output (remember that the op-amp is part of an integrator). Would it be a good idea, now that the inputs of the op-amp and the top plates of the capacitors are tied to ground or the virtual ground of the op-amp, to swap the bottom and top plates of the capacitors? Why or why not? Use SPICE to support your answers.***

Sol)

The Fig. 7.61 is shown below; it is a switched capacitor implementation of the dual summing block for a cascaded modulator.

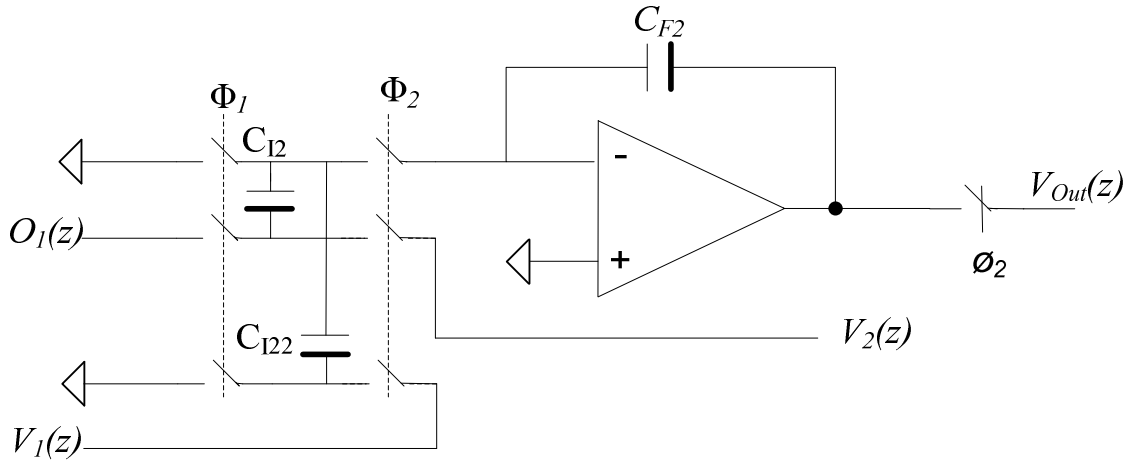


Figure 1:Dual Summing Block for a cascaded modulator

The transfer function of this topology will be derived using super-position techniques. Firstly, we will derive the transfer function for the top input branch with the C_{I2} capacitor, then we will derive the transfer function for the bottom branch and add the two results. Here, the output of the DAI, $V_{out1}(z)$ will be derived for inputs $O_1(z)$ and $V_2(z)$.

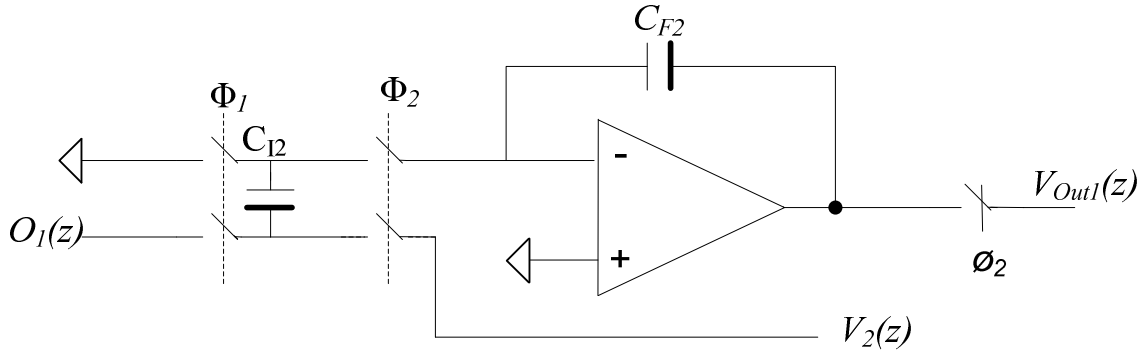


Figure 2: Using superposition, V1 input is eliminated

The timing diagram for the non-overlapping clocks is shown below.

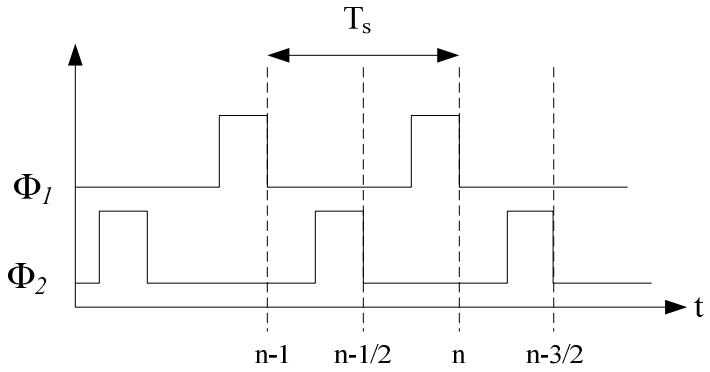


Figure 3: Timing diagram for the non-overalpping clocks

Note that the output of the DAI is clocked at Φ_2 clock phase. Right before the Φ_1 switch opens (Φ_1 goes low) at n-1, the charge stored on C_{I2} is

$$Q_1 = O_1 \cdot (N-1) T_S \cdot C_{I2} \quad \textbf{[1]}$$

When the Φ_2 switch opens (Φ_2 goes low) at n-1/2, the charge stored on C_{I2} is

$$Q_2 = \left[V_2 \cdot \left(N - \frac{1}{2} \right) T_S \right] C_{I2} \quad \textbf{[2]}$$

Since the op-amp holds its inverting terminal at virtual ground, the difference between the two charges is transferred to the op-amps feedback capacitor, which results in an output voltage change. This change is

$$\left[V_{Out1}\left(N - \frac{3}{2} \right) T_S - V_{Out1}\left(N - \frac{1}{2} \right) T_S \right] C_{F2} = Q_2 - Q_1 \quad \textbf{[3]}$$

$$\left[V_{Out1}\left(N - \frac{3}{2} \right) T_S - V_{Out1}\left(N - \frac{1}{2} \right) T_S \right] C_{F2} = \left[V_2 \cdot \left(N - \frac{1}{2} \right) T_S \right] C_{I2} - \left[O_1 \cdot (N-1) T_S \right] C_{I2} \quad \textbf{[4]}$$

$$\left[V_{Out1}(z) \cdot z^{-\frac{3}{2}} - V_{Out1}(z) \cdot z^{-\frac{1}{2}} \right] C_{F2} = \left[V_2(z) \cdot z^{-\frac{1}{2}} - O_1(z) \cdot z^{-1} \right] C_{I2} \quad \textbf{[5]}$$

$$V_{Out1}(z) \cdot \cancel{z^{-\frac{1}{2}}} \left[z^{-1} - 1 \right] C_{F2} = \cancel{z^{-\frac{1}{2}}} \cdot \left[V_2(z) - O_1(z) \cdot z^{-\frac{1}{2}} \right] C_{I2} \quad \textbf{[6]}$$

$$V_{Out1}(z) = \frac{C_{I2}}{C_{F2}} \left[\frac{V_2(z) - O_1(z) \cdot z^{-\frac{1}{2}}}{z^{-1} - 1} \right] \quad \textbf{[7]}$$

$$V_{Out1}(z) = \frac{C_{I2}}{C_{F2}} \left[\frac{O_1(z) \cdot z^{-\frac{1}{2}} - V_2(z)}{1 - z^{-1}} \right] \quad \textbf{[8]}$$

Now, let us find the transfer function for input $V_1(z)$

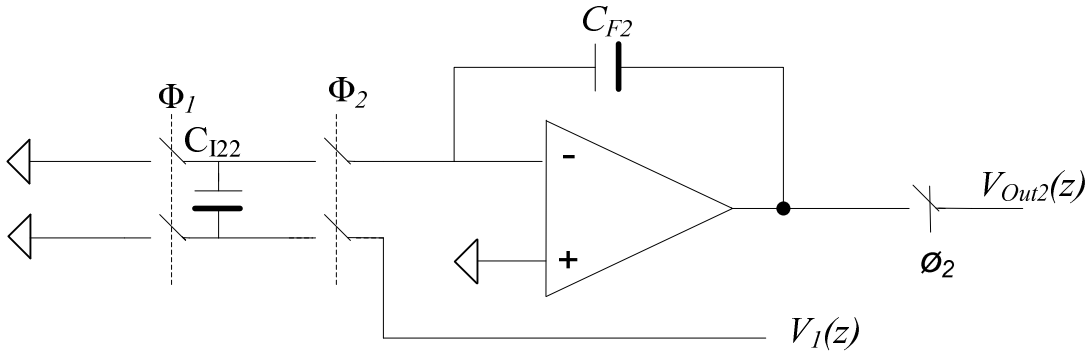


Figure 4: Using superposition, inputs O1 and V2 are eliminated

When Φ_1 opens the charge stored on the input capacitor C_{I22} is zero, as it is connected between two ground nodes.

$$Q_1 = 0 \quad \textbf{[9]}$$

Charge stored on the input capacitor when Φ_2 switches open is

$$Q_2 = V_1 \cdot \left(N - \frac{1}{2} \right) T_S \cdot C_{I22} \quad \textbf{[10]}$$

The change in output again is calculated using the charge transferred to the feedback capacitor, we can write

$$\left[V_{Out2}\left(N - \frac{3}{2} \right) T_S - V_{Out2}\left(N - \frac{1}{2} \right) T_S \right] C_{F2} = Q_2 - Q_1 \quad \textbf{[11]}$$

$$\left[V_{Out2}\left(N - \frac{3}{2} \right) T_S - V_{Out2}\left(N - \frac{1}{2} \right) T_S \right] C_{F2} = V_1 \cdot \left(N - \frac{1}{2} \right) T_S \cdot C_{I22} - 0 \quad \textbf{[12]}$$

$$\left[V_{Out2}(z) \cdot z^{-\frac{3}{2}} - V_{Out2}(z) \cdot z^{-\frac{1}{2}} \right] C_{F2} = V_1(z) \cdot z^{-\frac{1}{2}} \cdot C_{I22} \quad \textbf{[13]}$$

$$V_{Out2}(z) \cdot \cancel{z^{-\frac{1}{2}}} \left[z^{-1} - 1 \right] C_{F2} = V_1(z) \cdot \cancel{z^{-\frac{1}{2}}} \cdot C_{I22} \quad \textbf{[14]}$$

$$V_{Out2}(z) = \frac{C_{I22}}{C_{F2}} \left(\frac{-V_1(z)}{1 - z^{-1}} \right) \quad \textbf{[15]}$$

Adding the two output voltages using superposition, we get the final output Vout(z) as,

$$V_{Out}(z) = V_{Out1}(z) + V_{Out2}(z) = \frac{C_{I2}}{C_{F2}} \left[\frac{O_1(z) \cdot z^{-\frac{1}{2}} - V_2(z)}{1 - z^{-1}} \right] + \frac{C_{I22}}{C_{F2}} \left(\frac{-V_1(z)}{1 - z^{-1}} \right) \quad \textbf{[16]}$$

Therefore the transfer function of the topology seen in Fig. 7.61 is given by,

$$V_{Out}(z) = O_1(z) \cdot \frac{C_{I2}}{C_{F2}} \left(\frac{z^{-\frac{1}{2}}}{1 - z^{-1}} \right) - V_2(z) \frac{C_{I2}}{C_F} \left(\frac{1}{1 - z^{-1}} \right) - V_1(z) \frac{C_{I22}}{C_{F2}} \left(\frac{1}{1 - z^{-1}} \right) \quad \textbf{[17]}$$

The input common mode voltage for this topology is zero volts or referenced to ground. This is a concern if we do not use negative supply voltage, because in a real circuit implementation, if the input mosfet gate is held at ground and its source is also held at ground, the gate-to-source voltage of that input mosfet is zero and the mosfet will be off and the op-amp would not work. Another comment about the negative supply voltage is that the output should be able to swing between positive and negative voltages, and for that we need negative rail voltage.

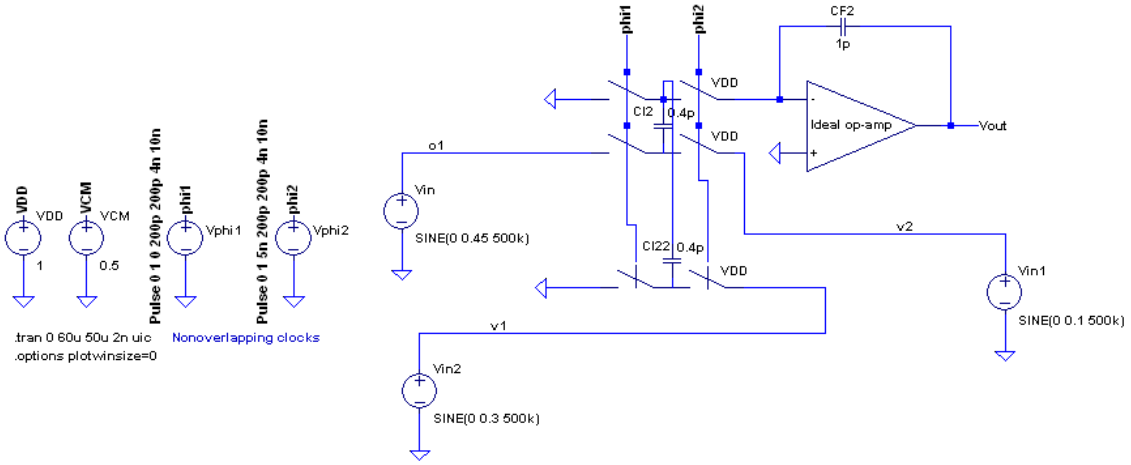


Figure 5: Spice schematic of the summing block (Vcm=0)

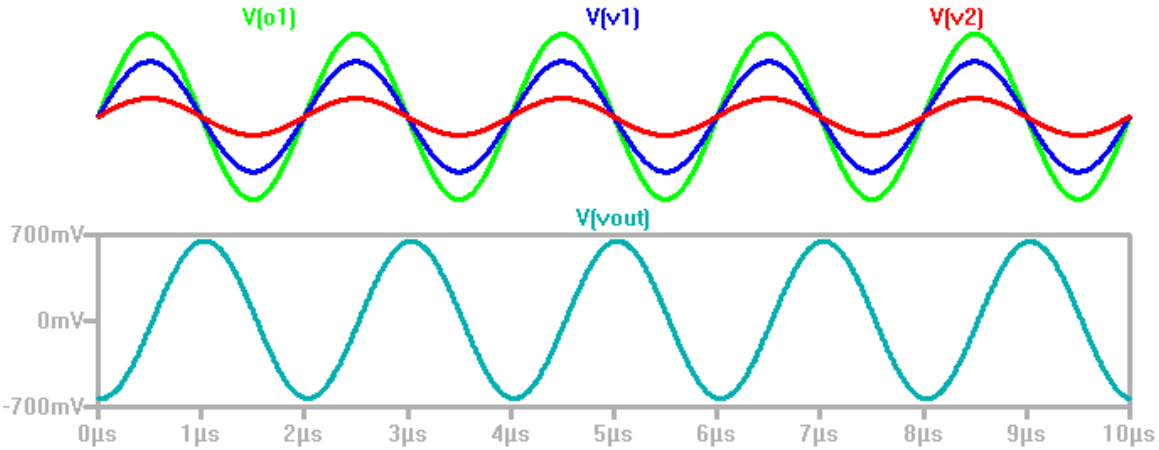
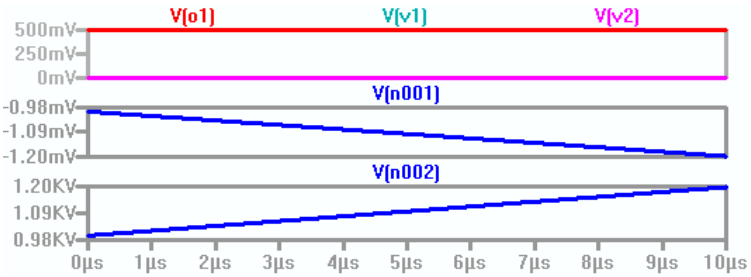


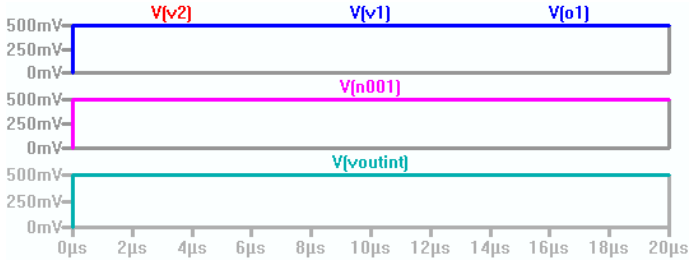
Figure 6: Input and output waveforms shown (Vcm=0)

We can see that the integral of sine wave is a cosine which is the output shown above. When the input voltages have a common mode voltage of zero same as that of the op-amp, the output is just an integrated version of the input voltages (o1-v1-v2) that swings around the common mode voltage of zero volts.

If the input signals now have a common-mode voltage of VDD/2, and the positive terminal of the op-amp is still held at ground, it will cause the output of the op-amp to grow without bounds. This is because the op-amp will hold the negative terminal at ground, and when the input is swinging around a common mode voltage of VDD/2, the charge from the input capacitor is constantly being transferred to the feedback capacitor.



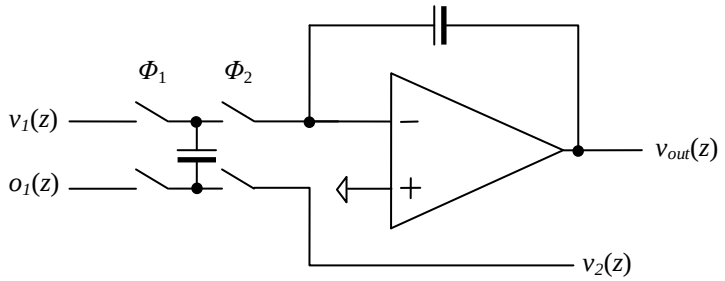
But if the negative terminal of the op-amp is changed from ground to common mode voltage VDD/2, this will move the common mode voltage of the op-amp to VDD/2.



For this topology swapping the bottom and top plates of the capacitors does not affect the operation, as the unwanted parasitic capacitor for capacitors C_{I2} and C_{I22} are held at ground during times when Φ_1 or Φ_2 are closed, even in this new modified configuration the topology should be parasitic insensitive as the amount of charge being transferred to the feedback capacitor is not affected by the charge on the parasitic capacitor. But in a real circuit implementation, it is not a good idea to switch the top and bottom plates as the negative terminal of the op-amp is not constantly being held at ground as the op-amp will have finite gain; this would affect the charge being transferred to the feedback capacitor and the topology becomes sensitive to the parasitic capacitor. Also, by reversing the top and bottom plates, we are placing the parasitic capacitor on the input of the op-amp and this can directly inject the substrate noise into the op-amp which is unwanted.

7.41 Repeat question 7.40 for the op-amp circuit seen in Fig. 7.62.

7.40 Derive the transfer function of the topology seen in Fig. 7.61 (show details of your derivation). What is the input common-mode voltage of the op-amp? Is this a concern when not using a negative supply voltage? If the input signals have a common-mode of VDD/2, does this affect the common-mode voltage of the circuit's output (remember that the op-amp is part of an integrator). Would it be a good idea, now that the inputs of the op-amp and the top plates of the capacitors are tied to ground or the virtual ground of the op-amp, to swap the bottom and top plates of the capacitors? Why or why not? Use SPICE to support your answers.



F-1 Sketch of Figure 7.62

Let's derive the transfer function of the circuit in F-1 quickly using what we have learned.

$$v_{out}\,C_F - v_{out}\,z^{-1}C_F = (0 - v_2)C_I - \left(v_1 z^{-1/2} - o_1 z^{-1/2}\right)C_I$$

$$v_{out} = o_1 \frac{z^{-1/2}}{1 - z^{-1}} \frac{C_I}{C_F} - v_1 \frac{z^{-1/2}}{1 - z^{-1}} \frac{C_I}{C_F} - v_2 \frac{1}{1 - z^{-1}} \frac{C_I}{C_F}$$

This was done by using a quick approach which skips the transformation from the time domain and performs the analysis in the z-domain only. Below is a detailed explanation of how this transfer function was derived.

We determined which clock signal "updates" the output. In F-1 the clock signal that updates the output is Φ_2. We set the time when Φ_2 goes low as nT_s, and recalled that the displacement current through the feedback capacitor must be equal on the v_{out} node and the inverting terminal to the op-amp. Another way of looking at this is to realize that the delta charge on both sides of the capacitor must be equal.

We characterize switched-capacitor networks over a time period which allows all of the input signals to be sampled, and the output signal to be updated with the sampled signals. The majority of the time this sample and update process occurs over T_s (in the discrete domain – over $(n-1)T_s$ to nT_s).

F-1 shows that when Φ_2 is high the v_2 signal is updating the output. Since we defined the time when Φ_2 goes low as nT_s, we can say that the v_2 signal does not experience a delay. We know that Φ_1 clock is delayed (w.r.t. Φ_2) by ½ a clock cycle, which means that the charge supplied from o_1 and v_1 will be delayed by ½ a clock cycle.

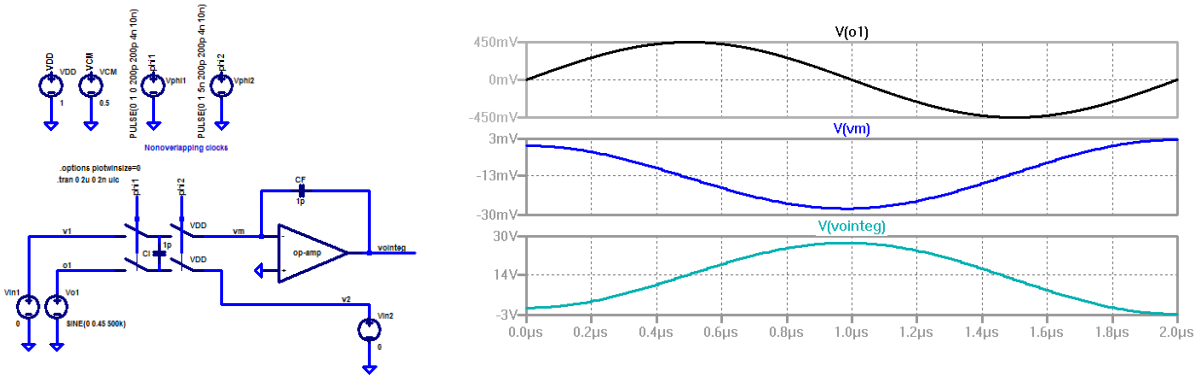
To keep the sign of the displacement current correct we take the charge when the output is updated minus the delayed charged. This leads to the equations below.

$$v_{out}\,C_F - v_{out}\,z^{-1}C_F = (0 - v_2)C_I - \left(v_1 z^{-1/2} - o_1 z^{-1/2}\right)C_I$$

$$v_{out} = o_1 \frac{z^{-1/2}}{1 - z^{-1}} \frac{C_I}{C_F} - v_1 \frac{z^{-1/2}}{1 - z^{-1}} \frac{C_I}{C_F} - v_2 \frac{1}{1 - z^{-1}} \frac{C_I}{C_F}$$

The input common-mode voltage of the op-amp is $0V$ (ground). This is a concern; because if a negative power supply is not used the op-amp will not go high. If your input signal does not go negative you will never be able to pull off the integrated charge on the feedback capacitor, which will keep pushing the non-inverting terminal further above your inverting terminal.

Using LTSPICE we can prove these statements, consider the schematic in F-2.

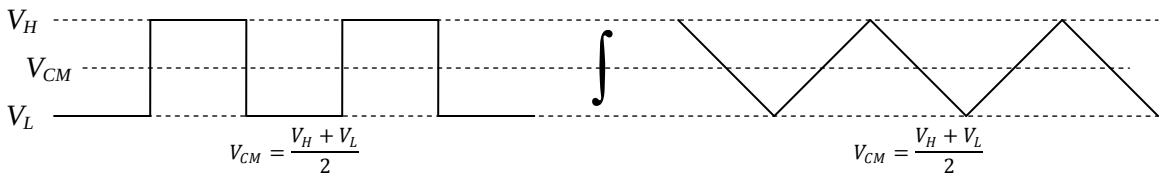


F-2 LTSPICE schematic and simulation results of F-1 (V_{CMIN} = $0V$)

To simulate F-2 we set v_1 and v_2 to the input common mode voltage (did not subtract anything from o_1) so that we can view the integration. F-2 also shows the simulation results for an input common mode voltage of $0V$. Note for an input common mode voltage you will need a negative supply so that the input signals can go below ground. The simulation results show that the integration is being performed correctly and that inverting terminal and the output go below $0V$ (the input common-mode voltage is $0V$).

If we set the input common-mode voltage to *VDD*/2 the common-mode voltage of the output is not changed because the op-amp has its non-inverting terminal set to ground. If we changed the non-inverting terminal to *VDD/2* along with all of the input signals then the output of the integrator would have the same common-mode voltage as the input.

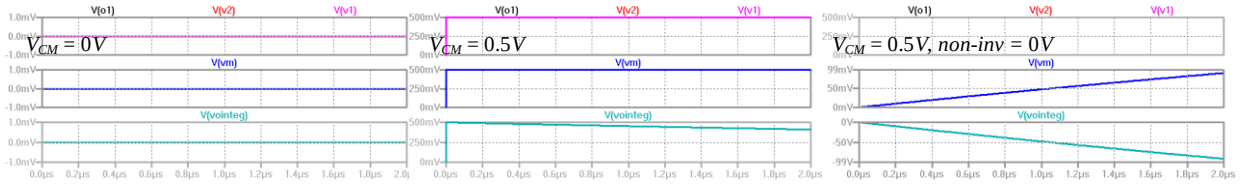
Another way to look at why the output common-mode range equals the input common-mode range is to look at the integration of a square wave. Consider the diagram in F-3.



F-3 Showing how the common-mode voltage is determined for an integration of a square wave

If the non-inverting terminal of the op-amp remains at $0V$ and we increase the common-mode voltage of the input signals to *VDD*/2, the v_m node would increase. When the v_m node increases the output of the op-amp will remain at ground (grow negative without bound when using ideal components). To prove this

we can run several simulations with different common-mode input voltages. F-4 shows the simulation results when using *DC* voltages for our input signals.



F-4 Changing the input common-mode voltage and viewing the output common-mode voltage

F-3 verifies our observations and shows the output growing negative without bound when V_{CM} is increased while keeping the non-inverting terminal at ground.

Now that the top plate of the capacitor is tied to ground (or virtual ground) it is not a good idea to swap the bottom plate of the capacitors. The parasitic capacitance of the top plate is less than the parasitic capacitance of the bottom plate. For a given delta voltage supplied to the parasitic capacitor, the charge associated with that voltage difference will be greater for a larger capacitance. In the case of the bottom plate versus the top plate, more erroneous charge will be supplied to the output. An additional consideration to this question is the substrate noise.

If we were to reverse the top and bottom plates of the capacitor we would place substrate noise at the input of the op-amp. This noise would be magnified by the op-amp and fed directly to the output. Due to these concerns we should not reverse the top and bottom plates of the capacitor.