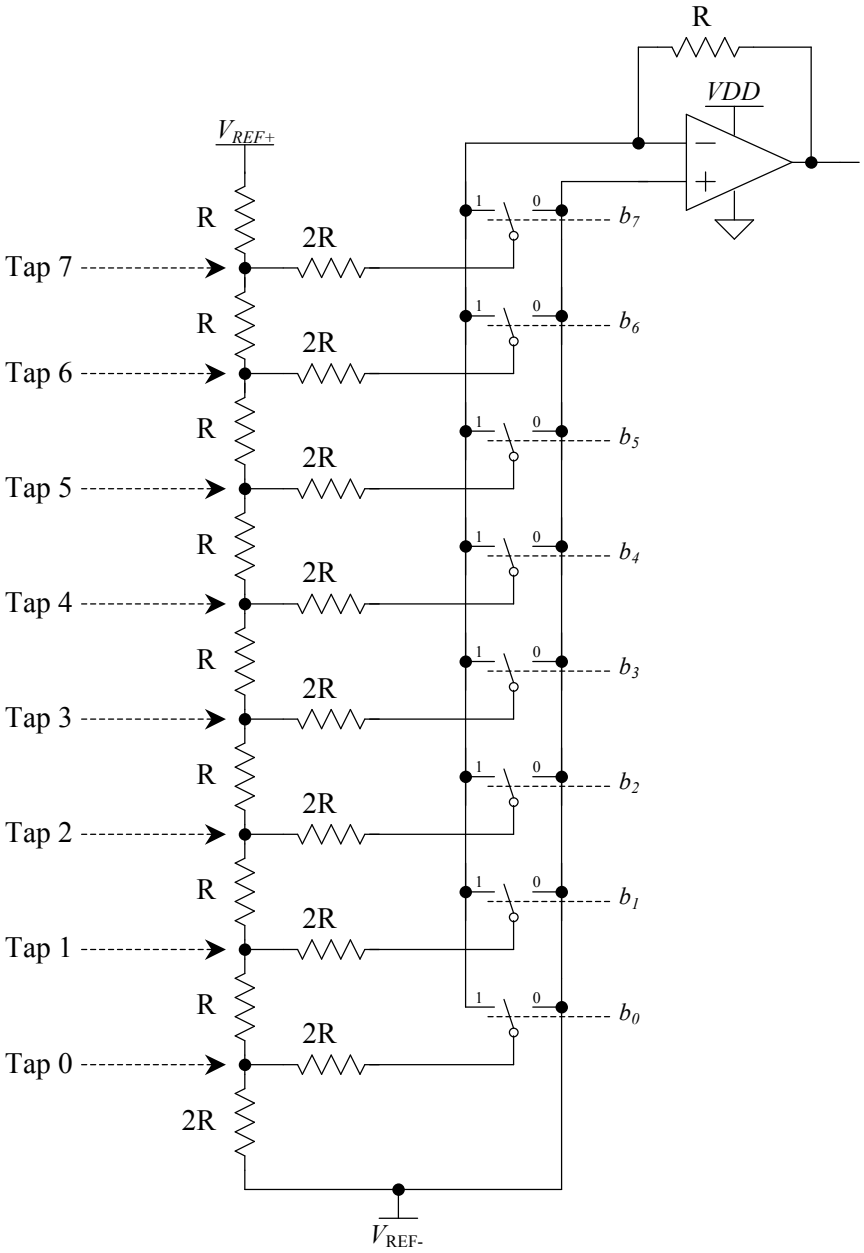
30.1 Assuming the DAC shown in Fig. 30.1 is 8 bits and V_{REF+} = 1 V and V_{REF-} = 0 V, what are the voltages on each of the R-2R taps?



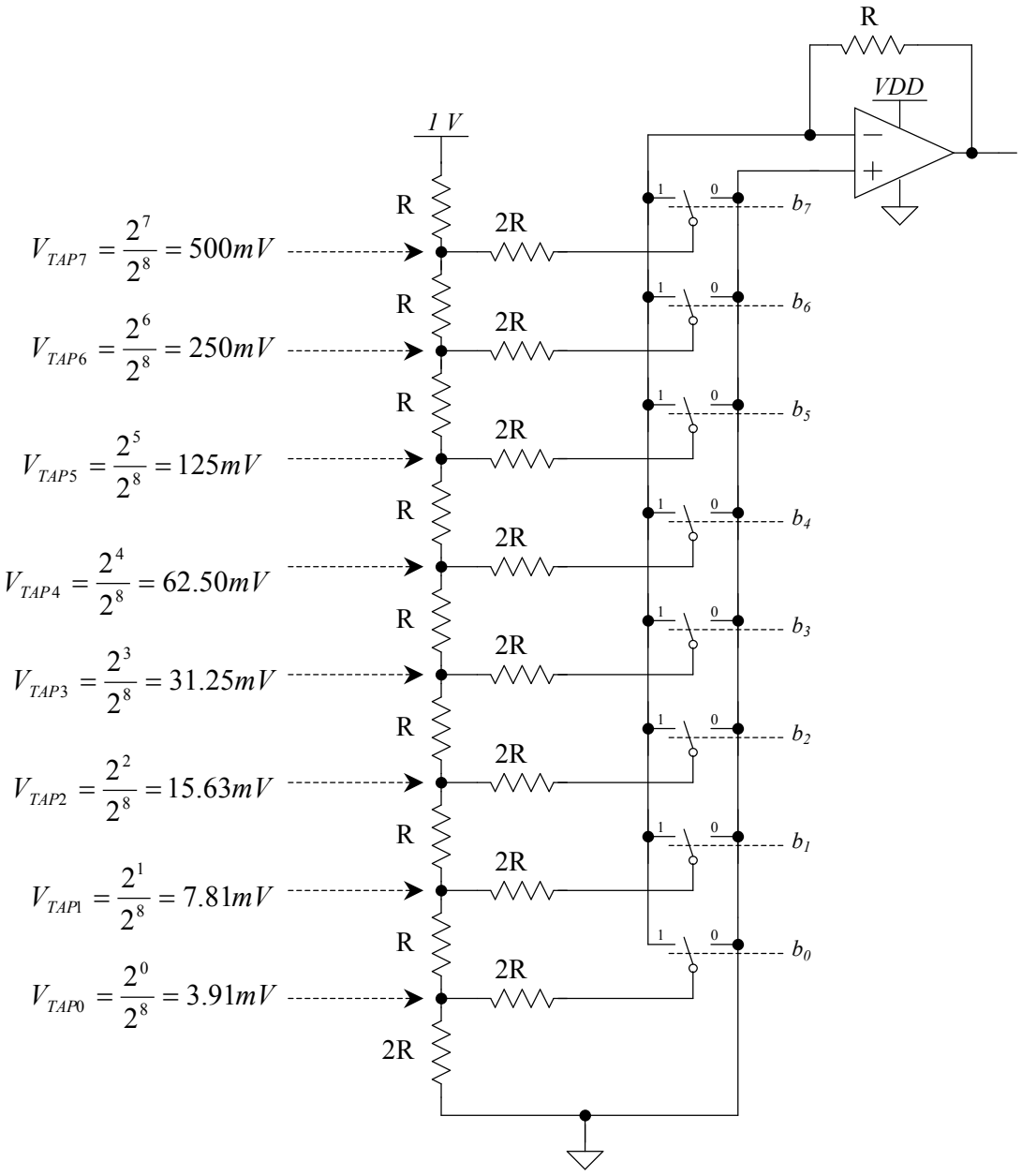
8-bit current-mode R-2R DAC

From Eq. (30.1): $V_{TAPX} = \frac{2^X}{2^N} \cdot (V_{REF+} - V_{REF-}) + V_{REF-}$ where X is the X^{th} tap.

Since V_{REF+} = 1 V and V_{REF-} = 0 V, we can rewrite the equation as:

$$V_{TAPX} = \frac{2^X}{2^N} \text{ V}$$

The tap voltages are shown on the schematic below.



(P.30.2)Give an example of how the traditional current-mode DAC will have limited output swing.

Consider traditional current mode R-2R DAC shown in the figure 30.2-1. The amount of current flowing through each 2R resistor depends on the node voltage TAPX and V_{REF-}. The current through 2R resistor is either diverted to inverting or non-inverting input of the operational amplifier depends on the digital inputs (b_0 to b_{n-1}). The main problem with this topology is limited output swing. In order to explain limited output swing of the DAC, assume the operational amplifier have an infinite gain and no offset.

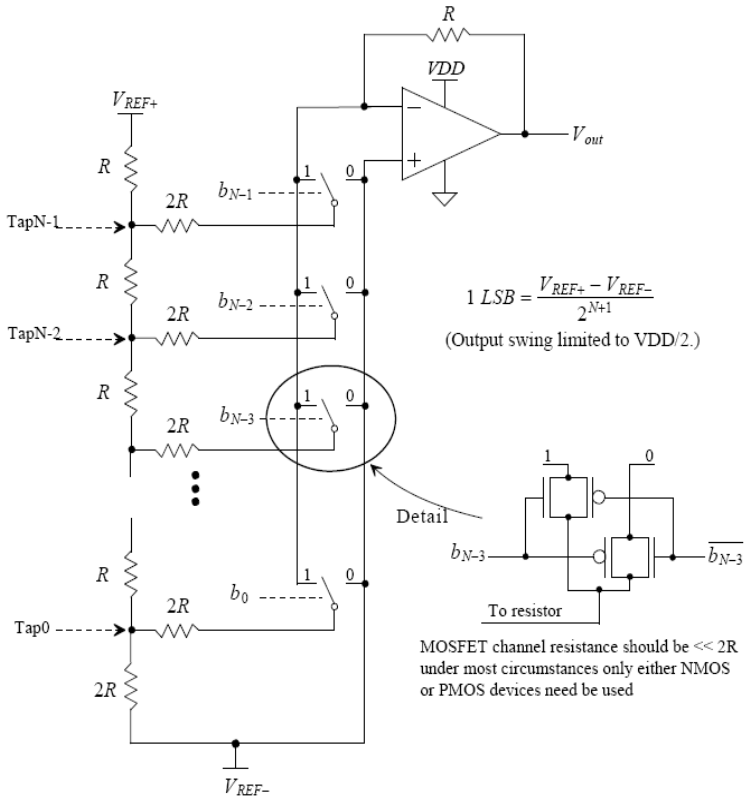


Figure 30.2-1 Traditional R-2R DAC.

Case (i) $V_{REF+} > 0V$ or V_{DD}; $V_{REF-}=0V$

For the given case, inverting and non-inverting nodes of the operational amplifier are always at 0V. For any digital input bits, the current flows from V_{REF+} to inverting node (0V) and flow through feedback resistor. From equation 30.2-1, it is clear that the output voltage is always being negative. But this can't happen when power supply voltage is V_{DD} or positive. Figure 30.2-2 shows the simulation results of the 3-bit DAC. It clearly shows that the output voltage swings from -5V to 0.

$$V_{Out} = -I_{Total}.R \tag{30.2.1}$$

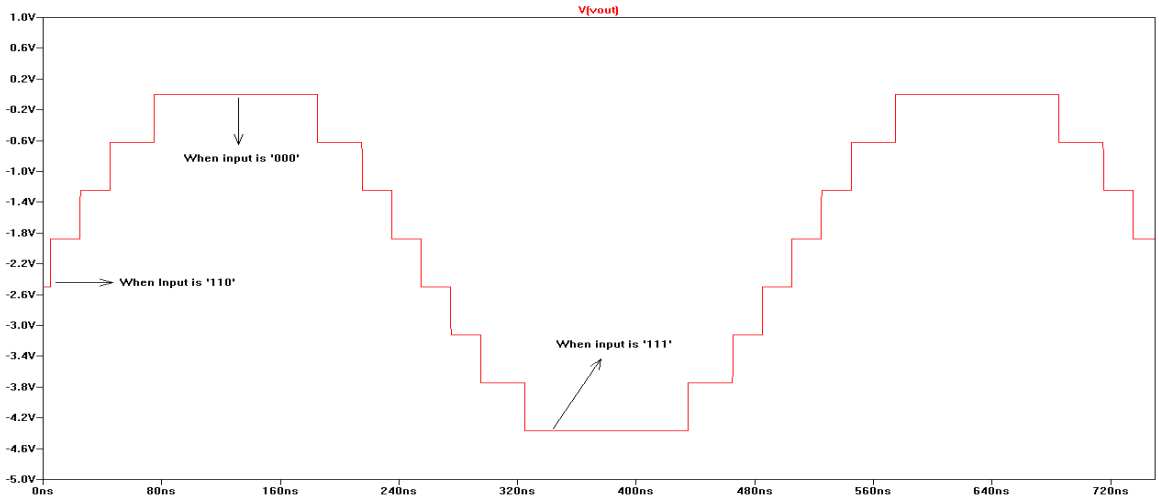


Figure 30.2-2 Output of 3-bit DAC when V_{REF+} = 5V and V_{REF-} = 0V.

Case (ii) $V_{REF-} > V_{REF+}$ (or) $V_{REF-} = V_{DD}$; V_{REF+} = 0V

For the given case, inverting and non-inverting nodes of the operational amplifier are always at V_{DD}. For any digital inputs, the current flows from output node to inverting node (V_{DD}) of the operational amplifier through feedback resistor R and reaches V_{REF+} through 2R resistor depends on input digital bits. From equation 30.2-3, output voltage is always being positive and more than $V_{DD.}$ But this can't happen when power supply voltage is V_{DD}. Figure 30.2-3 shows the simulation results of the 3-bit DAC. It clearly shows that the output voltage swings from 5V to 10V.

$$V_{Out} = V_{DD} + I_{Total}.R \tag{30.2.3}$$

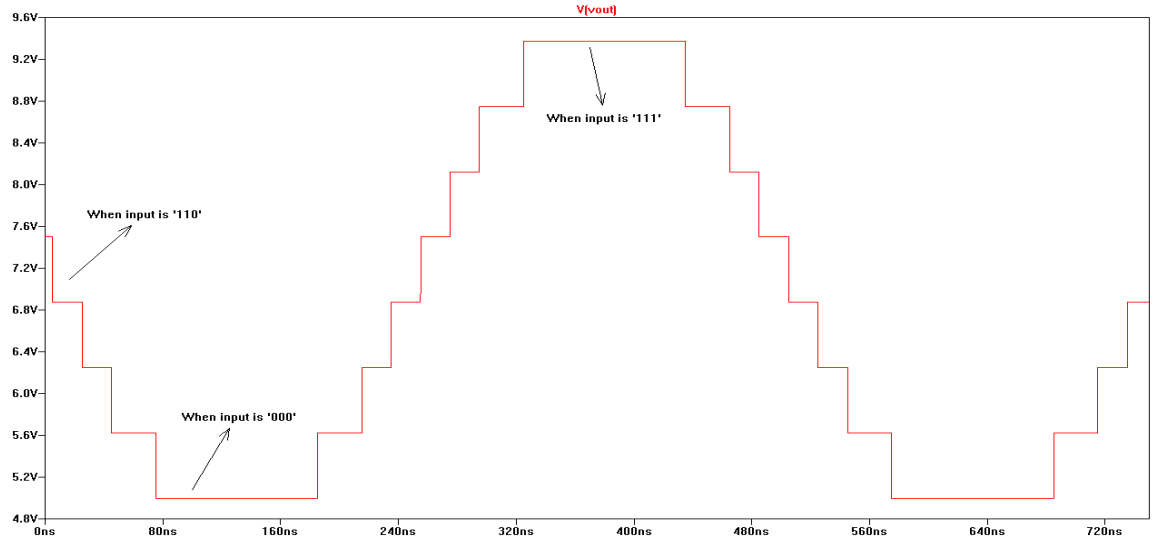


Figure 30.2-3 Output of 3-bit DAC when V_{REF+} = 0V and V_{REF-} = 5V.

Case (iii) $V_{REF+} = V_{DD}$; $V_{REF-}=V_{DD}/2$

For the given case, inverting and non-inverting nodes of the operational amplifier are always at $V_{DD}/2$. For any digital inputs, the current flows from V_{REF+} to output node through 2R and feedback resistor R. From equation 30.2-4, output voltage swings between V_{REF-} and V_{REF-} - (V_{REF+}-V_{REF-}). Figure 30.2-4 shows the simulation results of the 3-bit DAC. It clearly shows that the output voltage swings from 0V to 2.5V.

$$V_{Out} = \frac{V_{DD}}{2} - I_{Total}.R \tag{30.2.4}$$

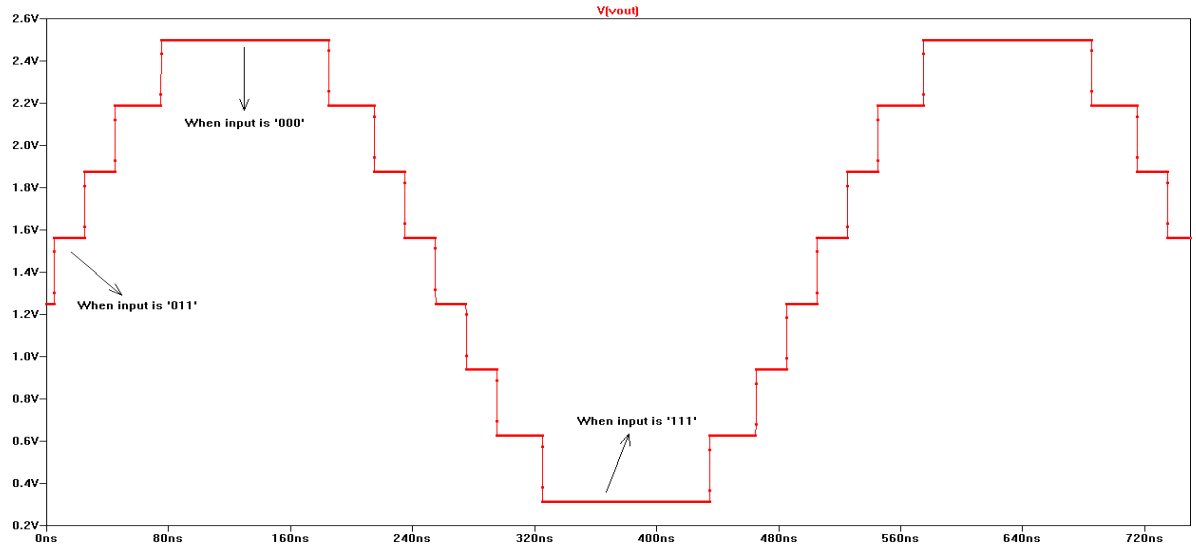


Figure 30.2-4 Output of 3-bit DAC when V_{REF+} = 5V and V_{REF-} = 2.5V.

In all the three cases, either output swings above or below the power supply voltage or only half of the power supply voltage. This also reduces the dynamic range of the DAC, which is usually not desirable. This concludes that the traditional R-2R DAC have limited output swing.

Justin Wood

30.3 Repeat Problem 30.1 for the DAC shown in Fig. 30.2.

Problem 30.1: Assuming the DAC shown in Fig. 30.1 is 8 bits and V_{REF+} = 1V and V_{REF-} = 0, what are the voltages on each of the R-2R taps?

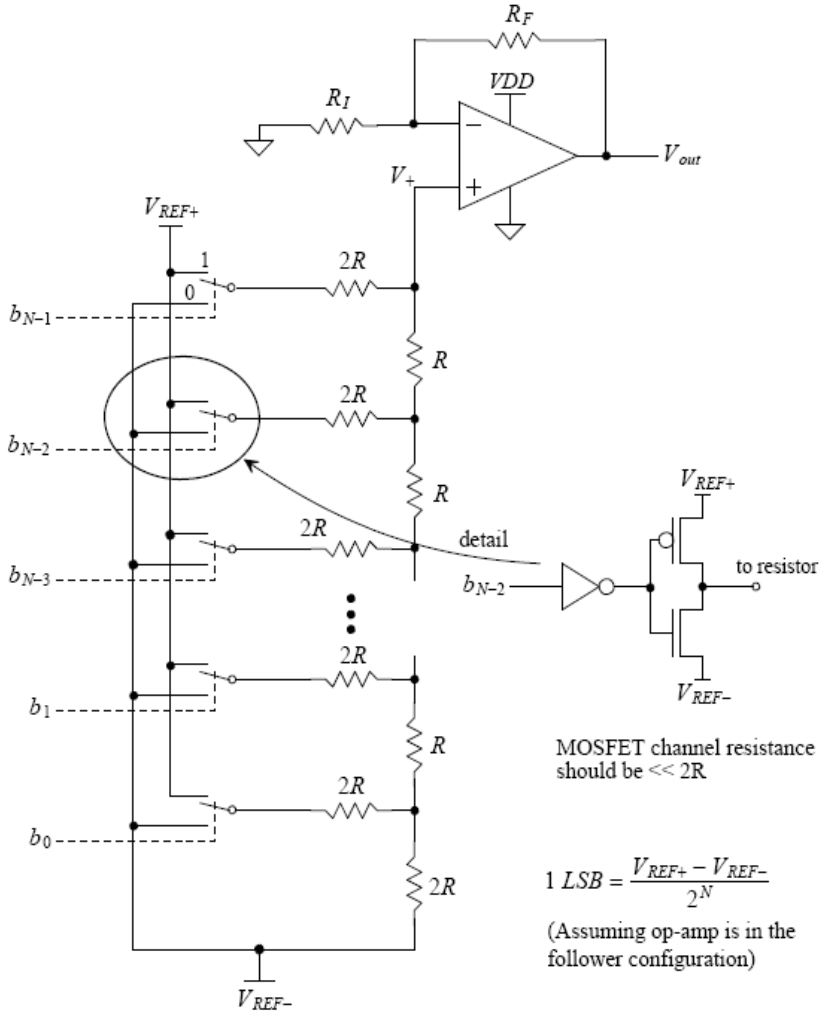


Figure 30.2 Traditional voltage-mode R-2R DAC.

Applying KCL at each node (T7 -> T0), we can derive the following equations for the node voltages:

$$\frac{V_{T7}-\left[V_{REF+}(b_7)+V_{REF-}(\bar{b}_7)\right]}{2R}+\frac{V_{T7}-V_{T6}}{R}=0\Rightarrow\frac{3V_{T7}}{2}-V_{T6}=\frac{V_{REF+}(b_7)+V_{REF-}(\bar{b}_7)}{2}$$

$$\frac{V_{T6}-\left[V_{REF+}(b_6)+V_{REF-}(\bar{b}_6)\right]}{2R}+\frac{V_{T6}-V_{T7}}{R}+\frac{V_{T6}-V_{T5}}{R}=0\Rightarrow-V_{T7}+\frac{5V_{T6}}{2}-V_{T5}=\frac{V_{REF+}(b_6)+V_{REF-}(\bar{b}_6)}{2}$$

$$\frac{V_{T5}-\left[V_{REF+}(b_5)+V_{REF-}(\bar{b}_5)\right]}{2R}+\frac{V_{T5}-V_{T6}}{R}+\frac{V_{T5}-V_{T4}}{R}=0\Rightarrow-V_{T6}+\frac{5V_{T5}}{2}-V_{T4}=\frac{V_{REF+}(b_5)+V_{REF-}(\bar{b}_5)}{2}$$

$$\frac{V_{T4}-\left[V_{REF+}(b_4)+V_{REF-}(\bar{b}_4)\right]}{2R}+\frac{V_{T4}-V_{T5}}{R}+\frac{V_{T4}-V_{T3}}{R}=0\Rightarrow-V_{T5}+\frac{5V_{T4}}{2}-V_{T3}=\frac{V_{REF+}(b_4)+V_{REF-}(\bar{b}_4)}{2}$$

$$\frac{V_{T3}-\left[V_{REF+}(b_3)+V_{REF-}(\bar{b}_3)\right]}{2R}+\frac{V_{T3}-V_{T4}}{R}+\frac{V_{T3}-V_{T2}}{R}=0\Rightarrow-V_{T4}+\frac{5V_{T3}}{2}-V_{T2}=\frac{V_{REF+}(b_3)+V_{REF-}(\bar{b}_3)}{2}$$

$$\frac{V_{T2}-\left[V_{REF+}(b_2)+V_{REF-}(\bar{b}_2)\right]}{2R}+\frac{V_{T2}-V_{T3}}{R}+\frac{V_{T2}-V_{T1}}{R}=0\Rightarrow-V_{T3}+\frac{5V_{T2}}{2}-V_{T1}=\frac{V_{REF+}(b_2)+V_{REF-}(\bar{b}_2)}{2}$$

$$\frac{V_{T1}-\left[V_{REF+}(b_1)+V_{REF-}(\bar{b}_1)\right]}{2R}+\frac{V_{T1}-V_{T2}}{R}+\frac{V_{T1}-V_{T0}}{R}=0\Rightarrow-V_{T2}+\frac{5V_{T1}}{2}-V_{T0}=\frac{V_{REF+}(b_1)+V_{REF-}(\bar{b}_1)}{2}$$

$$\frac{V_{T0}-\left[V_{REF+}(b_0)+V_{REF-}(\bar{b}_0)\right]}{2R}+\frac{V_{T0}-V_{T1}}{R}+\frac{V_{T0}-V_{REF-}}{2R}=0\Rightarrow-V_{T1}+2V_{T0}=\frac{V_{REF+}(b_0)+V_{REF-}(\bar{b}_0)}{2}+\frac{V_{REF-}}{2}$$

Knowing the digital input, we can solve for the tap voltages.

$$\begin{bmatrix}\frac{3}{2}&-1&0&0&0&0&0&0\\-1&\frac{5}{2}&-1&0&0&0&0&0\\0&-1&\frac{5}{2}&-1&0&0&0&0\\0&0&-1&\frac{5}{2}&-1&0&0&0\\0&0&0&-1&\frac{5}{2}&-1&0&0\\0&0&0&0&-1&\frac{5}{2}&-1&0\\0&0&0&0&0&-1&\frac{5}{2}&-1\\0&0&0&0&0&0&-1&2\end{bmatrix}\cdot\begin{bmatrix}V_{T7}\\V_{T6}\\V_{T5}\\V_{T4}\\V_{T3}\\V_{T2}\\V_{T1}\\V_{T0}\end{bmatrix}=\begin{bmatrix}\frac{V_{REF+}(b_7)+V_{REF-}(\bar{b}_7)}{2}\\\frac{V_{REF+}(b_6)+V_{REF-}(\bar{b}_6)}{2}\\\frac{V_{REF+}(b_5)+V_{REF-}(\bar{b}_5)}{2}\\\frac{V_{REF+}(b_4)+V_{REF-}(\bar{b}_4)}{2}\\\frac{V_{REF+}(b_3)+V_{REF-}(\bar{b}_3)}{2}\\\frac{V_{REF+}(b_2)+V_{REF-}(\bar{b}_2)}{2}\\\frac{V_{REF+}(b_1)+V_{REF-}(\bar{b}_0)}{2}\\\frac{V_{REF+}(b_0)+V_{REF-}(\bar{b}_0)}{2}-\frac{V_{REF-}}{2}\end{bmatrix}$$

For V_{REF+} = 1V and V_{REF-} = 0V and digital input of 0000 0001, we solve the matrix above and get the following node voltages:

V_{T7}=0.0039
V_{T6}=0.0059
V_{T5}=0.1074
V_{T4}=0.0210
V_{T3}=0.0417
V_{T2}=0.0834
V_{T1}=0.1667
V_{T0}=0.3333

V_{T7} is V_+ which for 0000 0001 should be 1 LSB ($V_{REF+}/2^8$) or 0.0039V. The tap voltages can similarly be calculated for all 2^8 input combinations.

An alternative method for calculating the node voltage would be to use superposition and determine the contribution from each bit at a given node. For example, the contribution from b_7 to V_{T7} or V_+ would be $\frac{b_7 \cdot V_{REF+} + \overline{b}_7 \cdot V_{REF+}}{2}$. Equation 30.5 was derived in this manner.

30.4 For the wide-swing current mode DAC shown in Fig. 30.3, what are the voltages at the taps along the R-2R string assuming 8 bits, V_{REF+} = 1 V, V_{REF-} = 0, and a digital input code of 0000 0000?

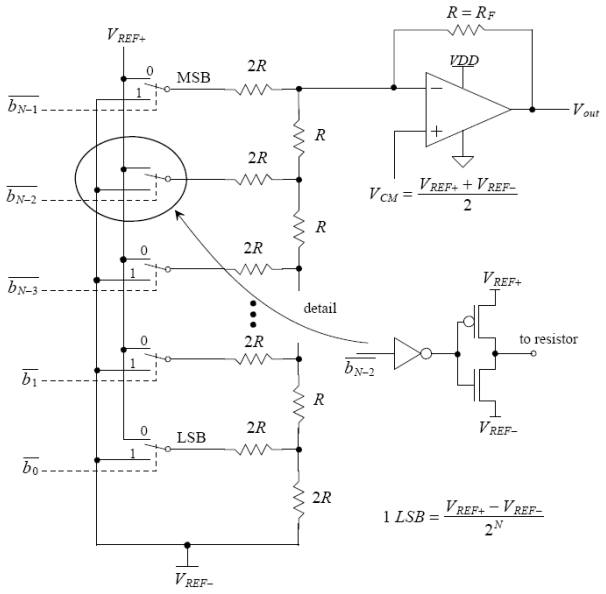
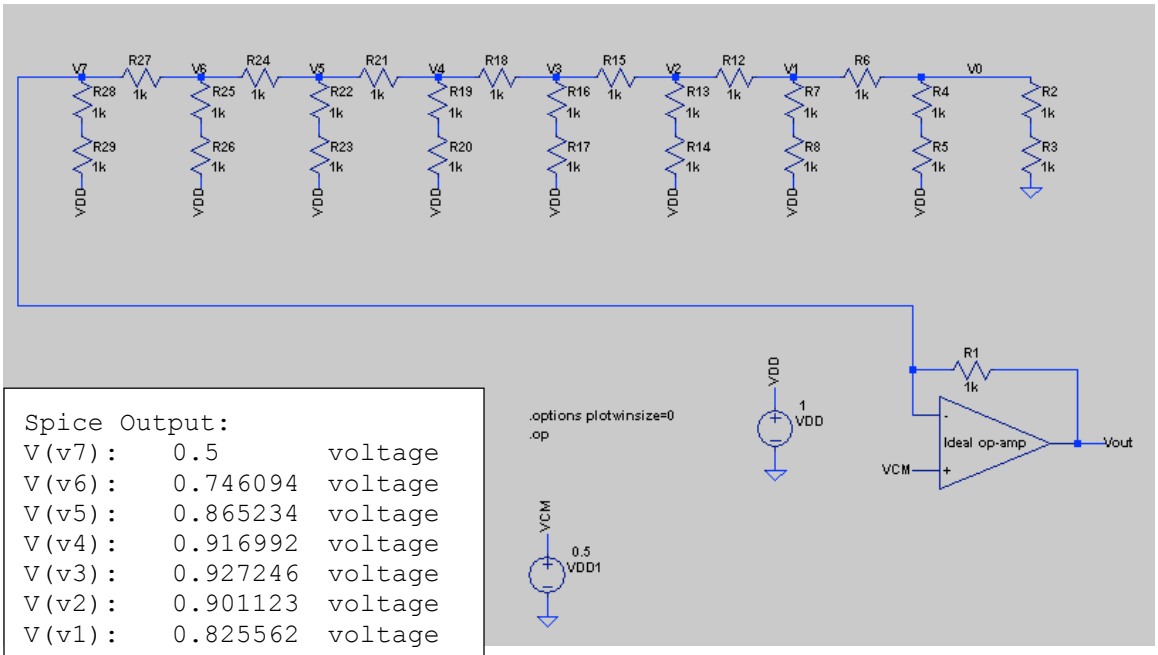


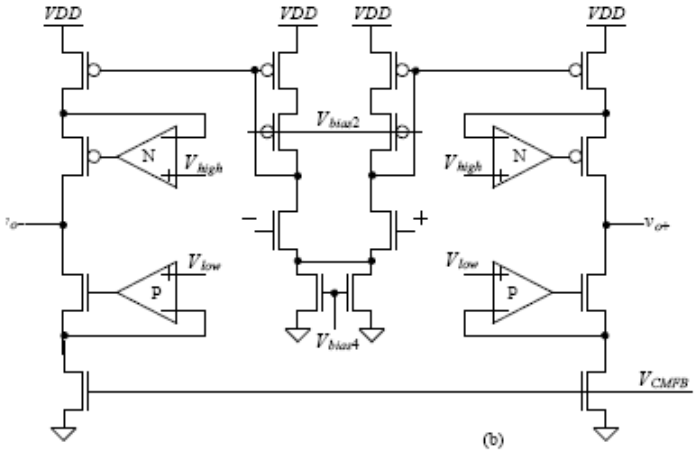
Figure 30.3 Wide-swing current-mode R-2R DAC.

Using LTSpice with the schematic below, we can find the voltages of each node.




```
Spice Output:
V(v7):    0.5       voltage
V(v6):    0.746094  voltage
V(v5):    0.865234  voltage
V(v4):    0.916992  voltage
V(v3):    0.927246  voltage
V(v2):    0.901123  voltage
V(v1):    0.825562  voltage
V(v0):    0.662781  voltage
```

30.5 Can the op-amp shown in Fig. 30.37 be used in fully-differential implementations of the DACs shown in Figs. 30.1 – 30.3? Why or why not?



Showing just the op-amp schematic from Fig. 30.37

The op-amp in Fig. 30.37 is an OTA without an output buffer. It is fine to use in a S/H circuit when driving a purely capacitive load. However, the DACs in Figs. 30.1 – 30.3 have a feedback resistor connected to the output. This resistive load will kill the gain of the OTA and will be detrimental to the correct operation of the DAC. Additionally, the stability of an OTA without an output buffer is directly related to the load capacitance. From Eq. 24.44, $f_{un} = \frac{g_m}{2\pi \cdot C_L}$. As the load capacitance is decreased, the unity gain frequency of the OTA will push out, resulting in less phase margin. This is demonstrated below in the simulation of Fig. 24.36 with a 1 pF load capacitance versus a 50 fF load capacitance. The DACs in Figs. 30.1 – 30.3 may drive a small load capacitance and so the stability of the op-amp would be a concern.

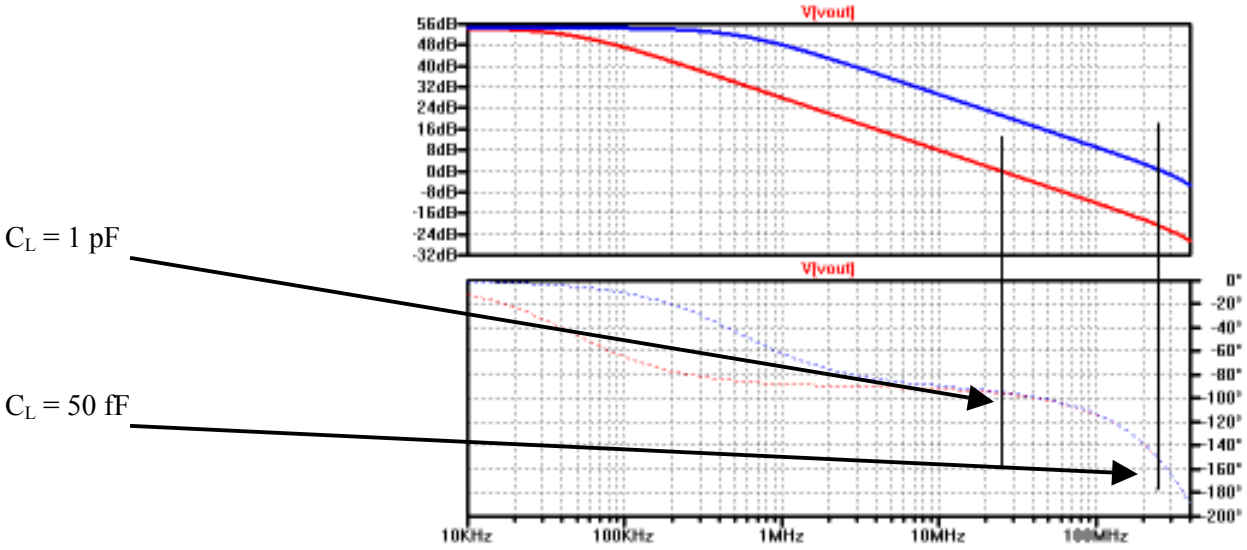


Fig. 24.36 Simulation with C_L = 1 pF and C_L = 50 fF

(P.30.6) Show the detailed derivation of Eqs. (30.12)-(30.14).

The step error of the current flowing through the feedback resistor R_F, due to the resistor mismatch at the midscale transition, is given in equation 30.6.1.

$$\Delta I = \frac{V_{REF+} - V_{REF-}}{2(R - \Delta R)}\left(1 - \frac{1}{2^{N-1}}\right) - \frac{V_{REF+} - V_{REF-}}{2(R + \Delta R)} \tag{30.6.1}$$

The final output step error (DNL) is given, under the assumption of R_F=R, in equation 30.6.2.

$$DNL = \Delta I.R \tag{30.6.2}$$

$$\Delta I.R = \left(\frac{V_{REF+} - V_{REF-}}{2(R - \Delta R)}\left(1 - \frac{1}{2^{N-1}}\right) - \frac{V_{REF+} - V_{REF-}}{2(R + \Delta R)}\right).R$$

$$\Delta I.R = (V_{REF+} - V_{REF-})\left(\frac{R}{2(R - \Delta R)} - \frac{R}{2^{N-1}.2.(R - \Delta R)} - \frac{R}{2(R + \Delta R)}\right) \tag{30.6.3}$$

Multiply both sides of equation 30.6.3 by $(R - \Delta R).(R + \Delta R)$,

$$\Delta I.R.(R - \Delta R).(R + \Delta R) = (V_{REF+} - V_{REF-})\left(\frac{R}{2}.(R + \Delta R) - \frac{R}{2^N}.(R + \Delta R) - \frac{R}{2}.(R - \Delta R)\right)$$

$$\Delta I.R.(R - \Delta R).(R + \Delta R) = (V_{REF+} - V_{REF-})\left(\frac{R^2}{2} + \frac{\Delta R.R}{2} - \frac{R^2}{2^N} - \frac{\Delta R.R}{2^N} - \frac{R^2}{2} + \frac{\Delta R.R}{2}\right)$$

$$\Delta I.R.(R - \Delta R).(R + \Delta R) = (V_{REF+} - V_{REF-})\left(\Delta R.R - \frac{R^2}{2^N} - \frac{\Delta R.R}{2^N}\right)$$

$$\Delta I.R = \frac{(V_{REF+} - V_{REF-})}{(R - \Delta R).(R + \Delta R)}\left(\Delta R.R - \frac{R^2}{2^N} - \frac{\Delta R.R}{2^N}\right)$$

$$\Delta I.R = \frac{(V_{REF+} - V_{REF-})}{(R^2 - \Delta R^2)}\left(\Delta R.R - \frac{R^2}{2^N} - \frac{\Delta R.R}{2^N}\right) \tag{30.6.4}$$

Take $\Delta R.R$ out of equation 30.6.4 results,

$$\Delta I.R = \frac{(V_{REF+} - V_{REF-}).\Delta R.R}{\Delta R.R.\left(\frac{R}{\Delta R} - \frac{\Delta R}{R}\right)}\left(1 - \frac{R}{2^N.\Delta R} - \frac{1}{2^N}\right) \tag{30.6.5}$$

Since $\frac{\Delta R}{R} << \frac{R}{\Delta R}$; $\frac{\Delta R}{R}$ is neglected in equation 30.6.5 and simplified as follow,

$$\Delta I.R = \frac{\left(V_{REF+} - V_{REF-}\right).\Delta R}{R}\left(1 - \frac{R}{2^N.\Delta R} - \frac{1}{2^N}\right)$$

$$\Delta I.R = \left(V_{REF+} - V_{REF-}\right).\left(\frac{\Delta R}{R} - \frac{1}{2^N}\left(1 + \frac{\Delta R}{R}\right)\right) \tag{30.6.6}$$

Since $\frac{\Delta R}{R} << 1$; $\frac{\Delta R}{R}$ is neglected in equation 30.6.6 and simplified as follow,

$$\boxed{DNL = \Delta I.R = \left(V_{REF+} - V_{REF-}\right).\left(\frac{\Delta R}{R} - \frac{1}{2^N.}\right)}$$

For the DNL to be within 1LSB, the required matching of the resistor is given as

$$\frac{\left(V_{REF+} - V_{REF-}\right)}{2^N} \geq \left(V_{REF+} - V_{REF-}\right).\left(\frac{\Delta R}{R} - \frac{1}{2^N.}\right)$$

$$\frac{1}{2^N} \geq \frac{\Delta R}{R} - \frac{1}{2^N}$$

$$\boxed{\left|\frac{\Delta R}{R}\right| \leq \frac{1}{2^{N-1}}} \tag{30.6.7}$$

30.7 Why would we want to use both current segments and binary-weighted currents to implement a current-mode DAC? (Why use segmentation?)

Using binary-weighted currents for the LSBs and current segments for the MSBs, or segmenting, is typically used to help improve DNL. It also allows for the use of less accurate components while still achieving good DNL. It is important to note that segmentation does not improve INL.

The advantage of segmentation can easily be seen by looking at the worst-case DNL (when the input code transistions from 0111... to 1000...). Using the DAC in figure 30.5, transitioning from 0111... to 1000... would increase the current I_F from 2047µA to 2048µA. If we can only allow 1/2 LSB error, the MSB current accuracy would have to be less than +/-0.024% (0.5/2048). This would be very challenging.

Now let's consider the case where we use 8 segments for 3 MSBs (See Figure 30.6). Each time the 4 MSBs increment, 256µA is added to I_F. Now, when we transition from 0111... to 1000... we are adding in a segment of 256µA rather than 2048µA. For 1/2 LSB error in this case, the current accuracy would only have to be +/-0.195% to maintain 1/2 LSB error.

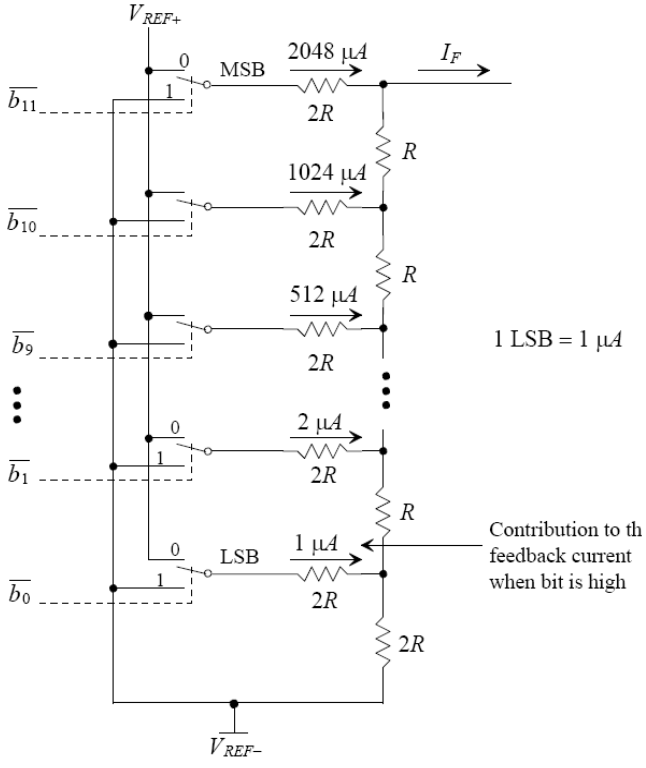


Figure 30.5 Showing how currents sum into the feedback current.

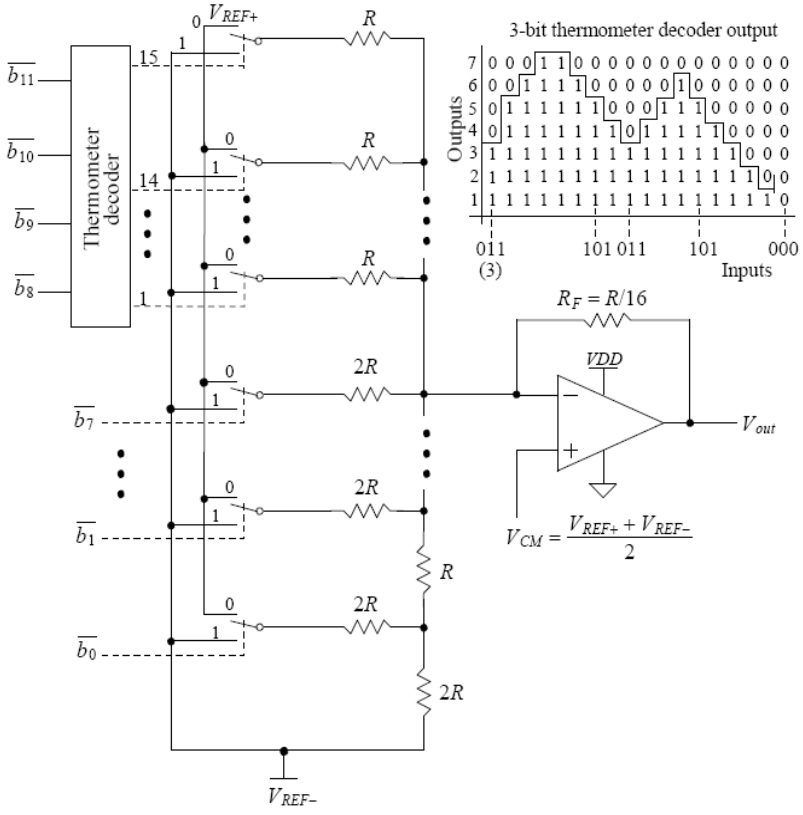


Figure 30.6 Segmentation in a wide-swing R-2R DAC.

Adam Johnson

30.8 Why do we subtract ΔA in Eq. (30.36)? Why not add the gain variation?

We want to derive the AOLDC that is necessary to have ½ LSB accuracy in our data converter. The assumption is that the feedback components are ideal, and so the gain variation is caused by $A_{OLDC} < \infty$. The maximum value that A_{CL} can be is $1/\beta$ in the ideal case when A_{OLDC} is ∞, so the gain variation must be less than the ideal case, caused by $A_{OLDC} < \infty$. Therefore, we must subtract the gain variation from the ideal A_{CL}.

Adam Johnson

30.9 Does the matching of the capacitors matter in the S/H of Fig. 30.31? Why or why not?

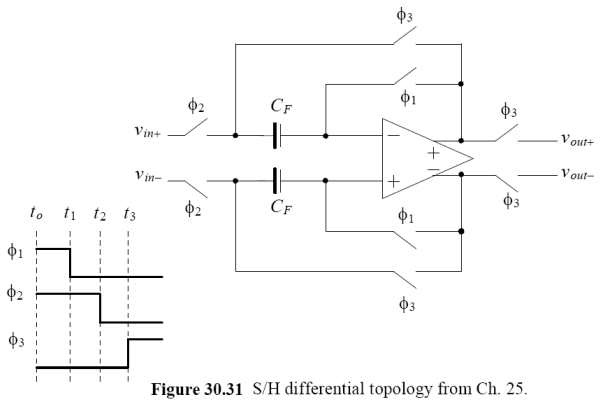
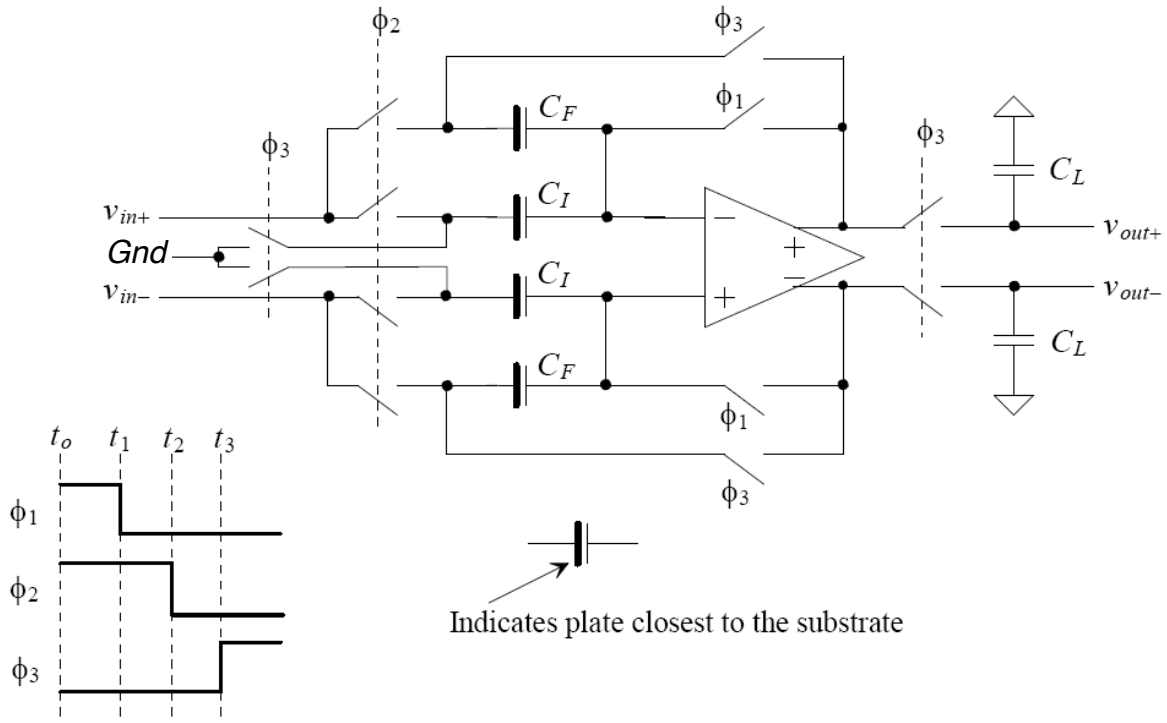


Figure 30.31 S/H differential topology from Ch. 25.

No. Since the two sides of the diff amp never interact, and there is no charge sharing between the capacitors, the matching between the two is not of consequence. The important thing is that the timing of the switching is sufficient to full charge both capacitors, and that the capacitors are big enough that any leakage component during the hold phase won't significantly change the voltage across the capacitor.

Justin Wood

30.10 Derive the transfer function of the S/H in Fig. 30.30 if V_{CM} on the left side of the schematic is replaced with ground so that the bottom plates of the C_1 capacitors are grounded when Φ_3 goes high.



To calculate the transfer function of the S/H we start by writing equations for the charge stored on C_I and C_F during the sample (Φ_1, Φ_2 high) and also during the hold (Φ_3 high). For the positive input, the charge stored on C_I and C_F during the sample is:

$$Q_I^{\phi_1} = C_I \cdot \left(v_{in+} - V_{cm} \pm V_{OS}\right)$$
$$Q_F^{\phi_1} = C_F \cdot \left(v_{in+} - V_{cm} \pm V_{OS}\right)$$

When Φ_3 goes high (Φ_2 and Φ_1 are low), the change on C_I is:

$$Q_I^{\phi_3} = C_I \cdot \left(0 - V_{X+} \pm V_{OS}\right)$$

Note that when Φ_3 closes the input to the opamp can't stay at V_{CM} if charge is to be conserved, it is labeled as V_{X+} in the previous equation.
The charge on C_F ($Q_F^{\Phi_3}$) can be written as:

$$Q_F^{\Phi_3} = Q_F^{\Phi_1} + Q_I^{\Phi_1} - Q_I^{\Phi_3}$$

(the charge on C_F from the sample + difference in charge on C_I between the sample and hold). $Q_F^{\Phi_3}$ can also be written with respect to the output as:

$$Q_F^{\phi_3} = C_F \cdot \left(v_{out+} - V_{X+} \pm V_{OS}\right)$$

Combining the above equations yields:

$$C_F \cdot \left(v_{out+} - V_{x+} \pm V_{OS}\right) = Q_F^{\Phi_1} + Q_I^{\Phi_1} - Q_I^{\Phi_3}$$

$$C_F \cdot \left(v_{out+} - V_{x+} \pm V_{OS}\right) = C_F \cdot \left(v_{in+} - V_{cm} \pm V_{OS}\right) + C_I \cdot \left(v_{in+} - V_{cm} \pm V_{OS}\right) - C_I \cdot \left(0 - V_{x+} \pm V_{OS}\right)$$

$$C_F \cdot \left(v_{out+} - V_{x+} \pm V_{OS}\right) = C_F \cdot \left(v_{in+} - V_{cm} \pm V_{OS}\right) + C_I \cdot \left(v_{in+} - V_{cm}\right) + C_I \cdot \left(V_{x+}\right)$$

$$v_{out+} = v_{in+} - V_{cm} + V_x + \frac{C_I}{C_F} \cdot \left(v_{in} - V_{cm} + V_{x+}\right)$$

$$v_{out+} = \left(1 + \frac{C_I}{C_F}\right) v_{in+} - \left(1 + \frac{C_I}{C_F}\right)\left(V_{cm} - V_{x+}\right)$$

Similarly for the negative side:

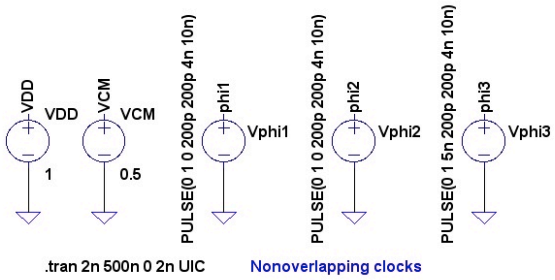
$$v_{out-} = \left(1 + \frac{C_I}{C_F}\right) v_{in-} - \left(1 + \frac{C_I}{C_F}\right)\left(V_{cm} - V_{x-}\right)$$

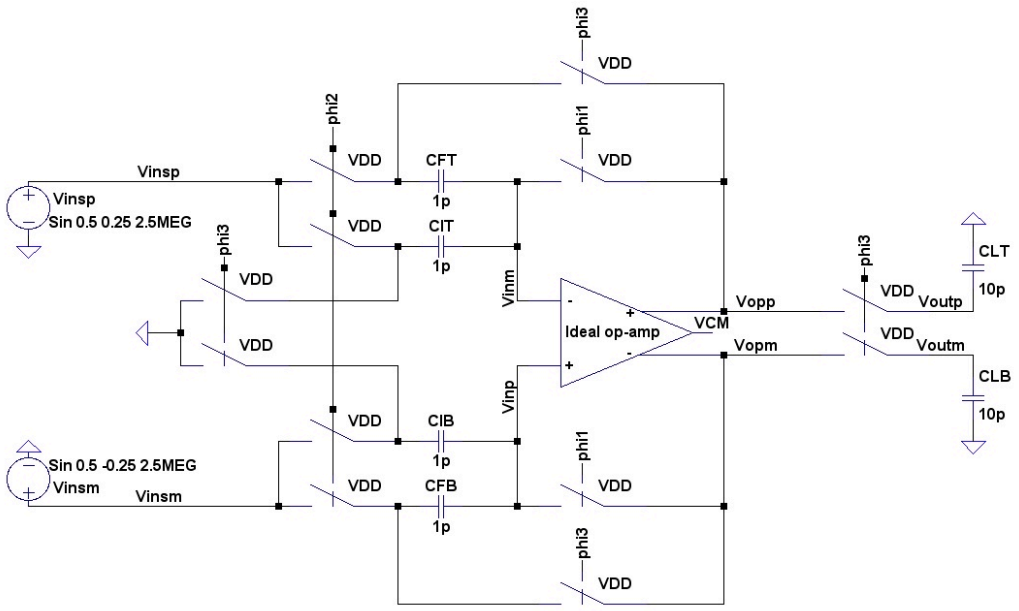
For fully differential signals the equation becomes:

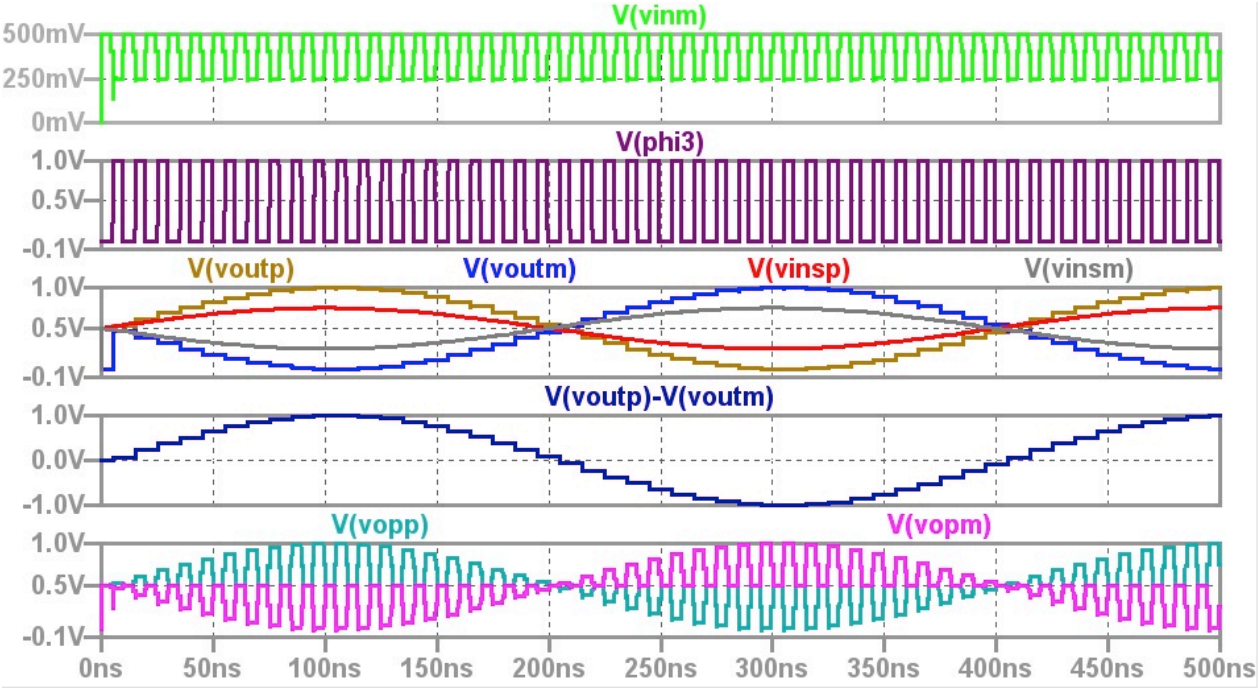
$$\left(v_{out+} - v_{out-}\right) = \left(1 + \frac{C_I}{C_F}\right) \cdot \left(v_{in+} - v_{in-}\right)$$

$$\frac{v_{out}}{v_{in}} = \left(1 + \frac{C_I}{C_F}\right)$$

A simulation of the circuit is shown below - notice that the opamp input terminal pulses down to 250mV when Φ_3 goes high.







(P.30.11)Determine the transfer function of S/H in Fig. 30.34 if the top left ϕ_2-controlled switch is connected to the input instead of V_{CM}. Include the offset and simulate the operation of the circuit to verify your calculation.

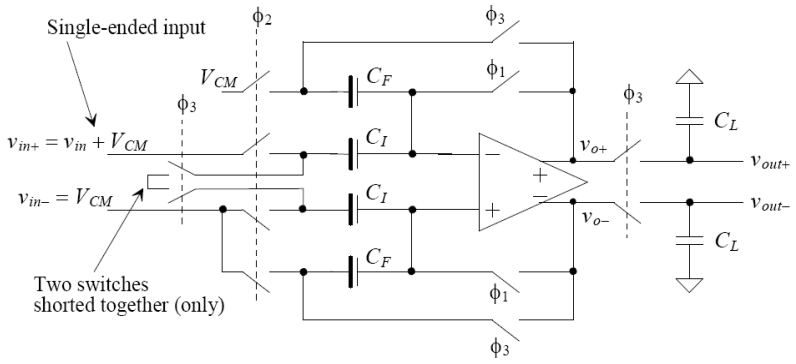


Figure 30.11-1 Single ended to differential S/H.

The relationship between the output and input of the S/H shown in the figure 30.11-1 if the top left ϕ_2-controlled switch is connected to the input instead of V_{CM} can be determined as follow.

Calculation of *vout+*

The charge stored on C_I and C_F from v_{in+} input when $\phi_{1,2}$ switches are closed is given as

$$Q_I^{\phi 1,2} = C_I\left(v_{in+} - V_{CM} \pm V_{OS}\right) = C_I\left(v_{in} + V_{CM} - V_{CM} \pm V_{OS}\right) = C_I\left(v_{in} \pm V_{OS}\right) \quad (30.11\text{-}1)$$

$$Q_F^{\phi 1,2} = C_F\left(v_{in+} - V_{CM} \pm V_{OS}\right) = C_F\left(v_{in} + V_{CM} - V_{CM} \pm V_{OS}\right) = C_F\left(v_{in} \pm V_{OS}\right) \quad (30.11\text{-}2)$$

where V_{OS} is the offset voltage of the operational amplifier, v_{in} and V_{CM} are input signal and the common mode voltage. When ϕ_3 goes high, the charge on C_I and C_F is given as

$$Q_I^{\phi 3} = C_I\left(V_x - V_{CM} \pm V_{OS}\right) \quad (30.11\text{-}3)$$

$$Q_F^{\phi 3} = C_F\left(v_{Out+} - V_{CM} \pm V_{OS}\right) \quad (30.11\text{-}4)$$

where V_x is the voltage on the bottom plate of the capacitor C_I when ϕ_3 switch is closed.

The difference between the summation of $Q_I^{\phi 1,2}$, $Q_F^{\phi 1,2}$ and $Q_I^{\phi 3}$ is the charge transferred to C_F when ϕ_3 goes high. The voltage is then determined knowing charge must be conserved.

$$Q_F^{\phi 3} = Q_I^{\phi 1,2} + Q_F^{\phi 1,2} - Q_I^{\phi 3} \quad (30.11\text{-}5)$$

$$C_F\left(v_{Out+} - V_{CM} \pm V_{OS}\right) = C_I\left(v_{in} \pm V_{OS}\right) + C_F\left(v_{in} \pm V_{OS}\right) - C_I\left(V_x - V_{CM} \pm V_{OS}\right) \quad (30.11\text{-}6)$$

By simplifying 30.14-6, v_{out+} can be determined as

$$\boxed{v_{Out+} = v_{in}\left(\frac{C_I}{C_F}+1\right)-\frac{C_I}{C_F}\left(V_x\right)+V_{CM}\left(\frac{C_I}{C_F}+1\right)} \tag{30.11-7}$$

Calculation of *vout-*

The charge stored on C_I and C_F from v_{in-} input when $\phi_{1,2}$ switches are closed is given as

$$Q_I^{\phi 1,2} = C_I\left(v_{in-} - V_{CM} \pm V_{OS}\right) = C_I\left(\pm V_{OS}\right) \tag{30.11-8}$$

$$Q_F^{\phi 1,2} = C_F\left(v_{in-} - V_{CM} \pm V_{OS}\right) = C_F\left(\pm V_{OS}\right) \tag{30.11-9}$$

When ϕ_3 goes high, the charge on C_I and C_F is given as

$$Q_I^{\phi 3} = C_I\left(V_x - V_{CM} \pm V_{OS}\right) \tag{30.11-10}$$

$$Q_F^{\phi 3} = C_F\left(v_{Out-} - V_{CM} \pm V_{OS}\right) \tag{30.11-11}$$

The difference between the summation of $Q_I^{\phi 1,2}$, $Q_F^{\phi 1,2}$ and $Q_I^{\phi 3}$ is the charge transferred to C_F when ϕ_3 goes high. The voltage is then determined knowing charge must be conserved.

$$Q_F^{\phi 3} = Q_I^{\phi 1,2} + Q_F^{\phi 1,2} - Q_I^{\phi 3} \tag{30.11-12}$$

$$C_F\left(v_{Out+} - V_{CM} \pm V_{OS}\right) = C_I\left(\pm V_{OS}\right) + C_F\left(\pm V_{OS}\right) - C_I\left(V_x - V_{CM} \pm V_{OS}\right) \tag{30.11-13}$$

By simplifying 30.14-13, v_{out-} can be determined as

$$\boxed{v_{Out-} = -\frac{C_I}{C_F}\left(V_x\right)+V_{CM}\left(\frac{C_I}{C_F}+1\right)} \tag{30.11-14}$$

From equation 30.14-7, 14, transfer function or relationship between output and input can be written as

$$v_{OUT} = v_{OUT+} - v_{OUT-} = v_{in}\left(\frac{C_I}{C_F}+1\right)-\frac{C_I}{C_F}\left(V_x\right)+V_{CM}\left(\frac{C_I}{C_F}+1\right)+\frac{C_I}{C_F}\left(V_x\right)-V_{CM}\left(\frac{C_I}{C_F}+1\right) \tag{30.11-15}$$

$$\boxed{\frac{v_{OUT}}{v_{in}} = \left(\frac{C_I}{C_F}+1\right)} \tag{30.11-16}$$

Notice in equation 30.14-16, operational amplifier offset is auto zeroed out and the signal is centered at 0 rather than V_{CM}.

Figure 30.11-2 shows the simulation set-up with V_{OS} of 50mV on inverting terminal of fully differential operational amplifier with C_F=C_I=1pF. As derived in equation 30.11-16, the output results with a gain of 2 and centered at 0V are shown in the figure 30.11-3.

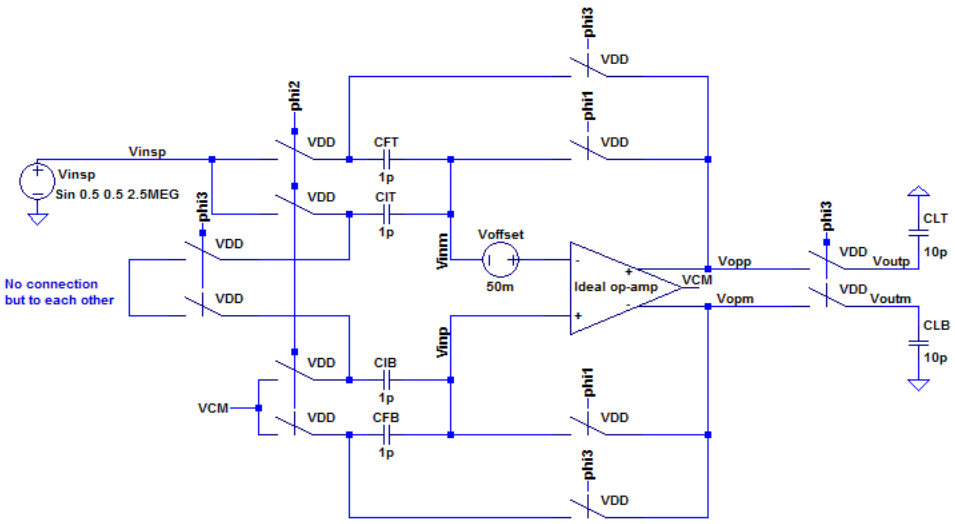


Figure 30.11-2 Simulation Set-up.

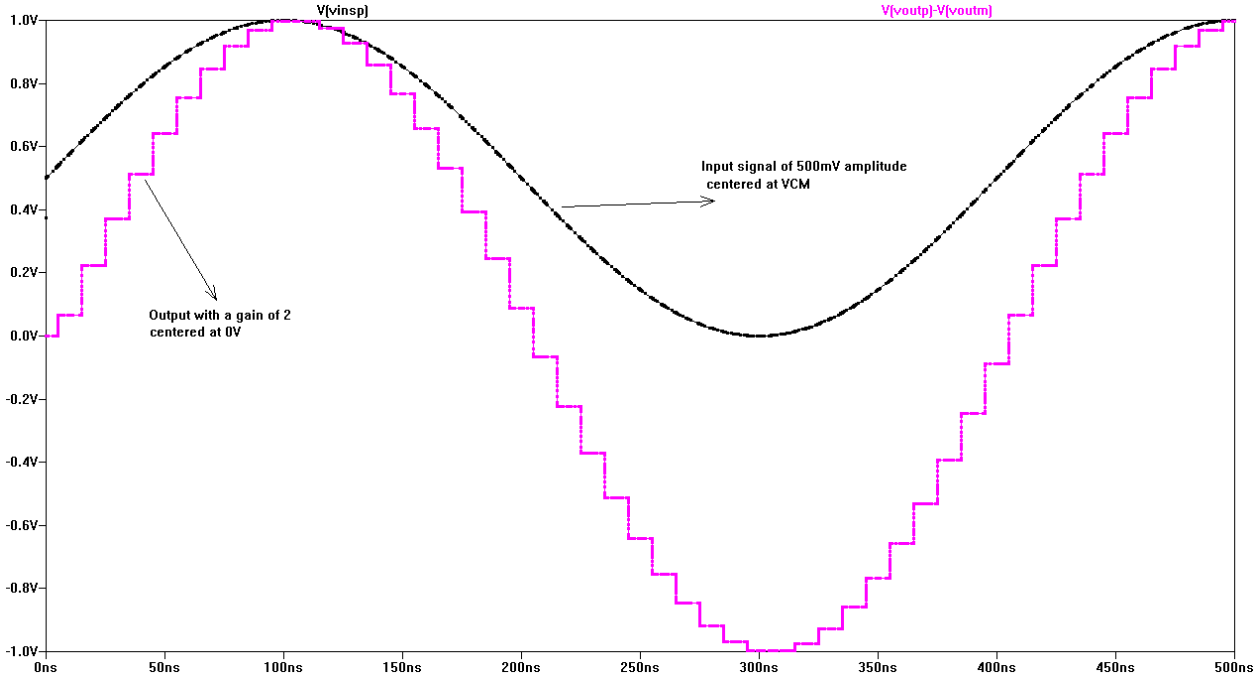


Figure 30.11-3 Simulation Result.

30.12 Repeat Ex. 30.10 if the cyclic ADC's input is 0.41 V.

The block diagram of a cyclic ADC is shown in Figure 30.38.

For this problem we have:

$N = 8$

$V_{REF} = 1$ V

$V_{CM} = 0.5$ V

$V_{IN} = 0.41$ V

The operation of the 8-bit cycle ADC with an input voltage of 0.41 V is shown in the table below.

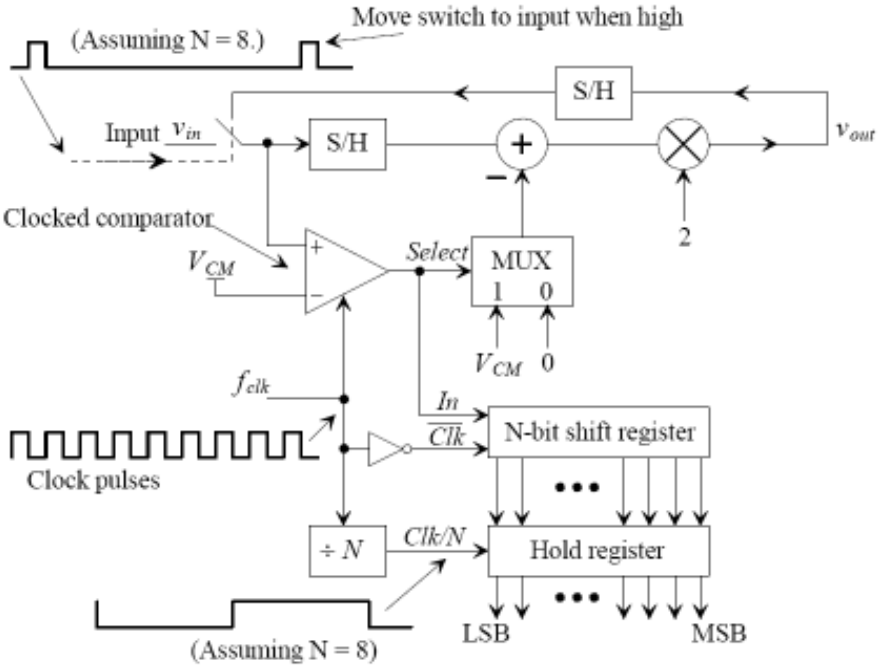


Figure 30.38 Block diagram of a cyclic ADC.

Clock Cycle	Bit	Sample Voltage (V)	Comparator Output	Subtract (V)	After Subtract (V)	After Multiply x2 (V)
1	b7	0.4100	0	0	0.4100	0.8200
2	b6	0.8200	1	0.5	0.3200	0.6400
3	b5	0.6400	1	0.5	0.1400	0.2800
4	b4	0.2800	0	0	0.2800	0.5600
5	b3	0.5600	1	0.5	0.0600	0.1200
6	b2	0.1200	0	0	0.1200	0.2400
7	b1	0.2400	0	0	0.2400	0.4800
8	b0	0.4800	0	0	0.4800	0.9600

The final output of the ADC hold register is 01101000.

To verify, we can calculate the corresponding voltage:

$$V_{IN,converted} = \frac{1}{4} + \frac{1}{8} + \frac{1}{32} = 0.40625\text{ V} \approx 0.41\text{ V}$$

30.13 Is kick-back noise from the comparator a concern for the circuit of Fig. 30.39?

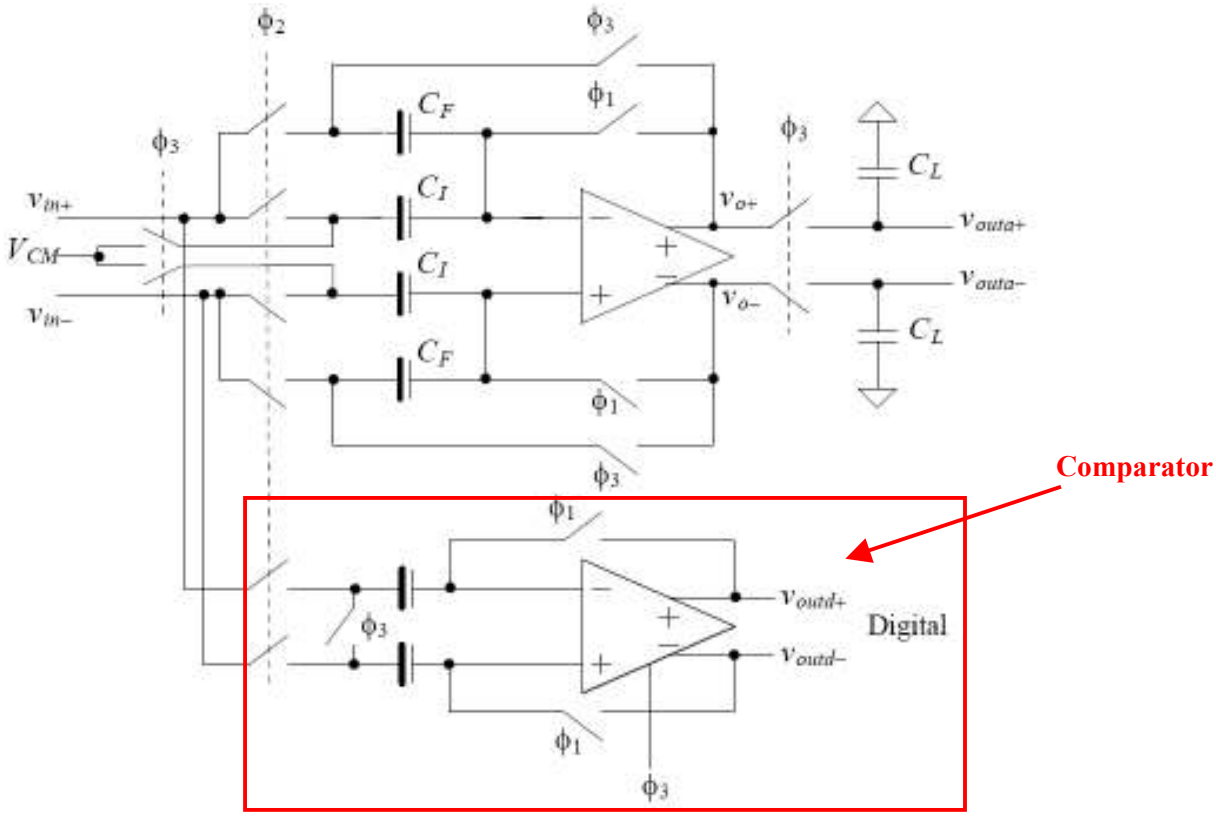
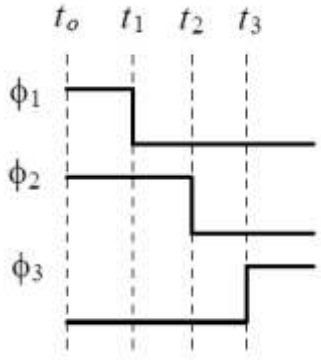


Figure 30.39 Implementation of the comparator with an S/H for use in a cyclic ADC.

Kick-back noise from the comparator is not a concern. ϕ_2 and ϕ_3 are nonoverlapping clocks. When the comparator is clocked with ϕ_3, the v_{in+} and v_{in-} inputs are already disconnected from the comparator circuit since the ϕ_2 switches are open. Therefore, the S/H input voltage is not corrupted by kick-back noise from the comparator.



Clocks used in Fig. 30.39

(P.30.14)Derive the transfer function for the circuit shown in the Fig.30.80.

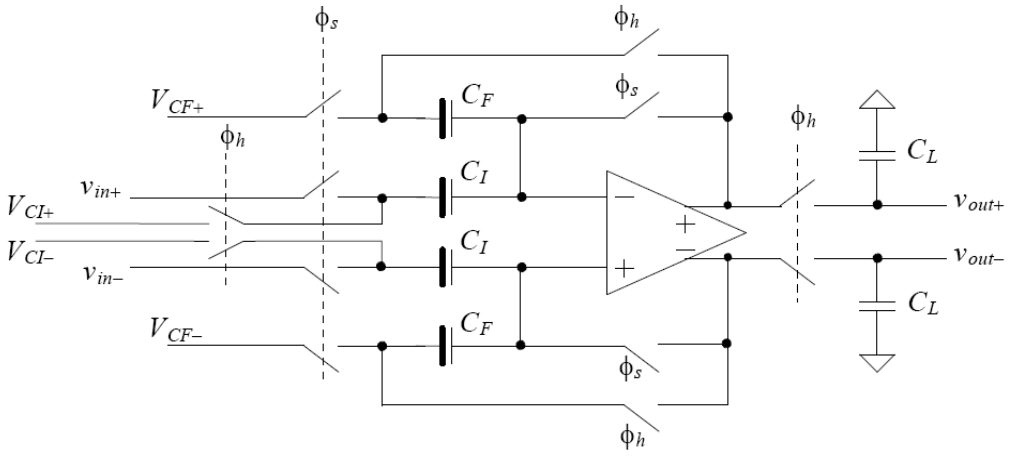


Figure 30.14-1 Circuit used in problem 30.14.

The relationship between the output and intput of the sample and hold circuit shown in the figure 30.14-1 can be determined as follow. The charge stored on C_I and C_F when ϕ_S switches are closed is given as

$$Q_I^{\phi s} = C_I\left(v_{in+} - V_{CM} \pm V_{OS}\right) \tag{30.14-1}$$

$$Q_F^{\phi s} = C_F\left(V_{CF+} - V_{CM} \pm V_{OS}\right) \tag{30.14-2}$$

where V_{OS} is the offset voltage of the operational amplifier, v_{in+} and V_{CM} are the differential input signal and common mode voltage. When ϕ_H goes high, the charge on C_I is

$$Q_I^{\phi h} = C_I\left(V_{CI+} - V_{CM} \pm V_{OS}\right) \tag{30.14-3}$$

The difference between $Q_I^{\phi s}$ and $Q_I^{\phi h}$ is transferred to C_F when ϕ_h goes high. The voltage is then determined knowing charge must be conserved.

$$Q_I^{\phi h} + Q_F^{\phi h} = Q_I^{\phi s} + Q_F^{\phi s} \tag{30.14-4}$$

$$C_F\left(v_{OUT+} - V_{CM} \pm V_{OS}\right) = C_I\left(v_{in+} - V_{CM} \pm V_{OS}\right) + C_F\left(V_{CF+} - V_{CM} \pm V_{OS}\right) - C_I\left(V_{CI+} - V_{CM} \pm V_{OS}\right)$$

By simplifying above equation, the output voltage is determined as

$$C_F v_{OUT+} = C_I v_{in+} + C_F V_{CF+} - C_I V_{CI+} \tag{30.14-5}$$

The positive output voltage can be written as

$$\boxed{v_{OUT+} = \frac{C_I}{C_F} v_{in+} + V_{CF+} - \frac{C_I}{C_F} V_{CI+}} \tag{30.14-6}$$

From equation 30.14-6, the negative output voltage can be written as

$$\boxed{v_{OUT-} = \frac{C_I}{C_F} v_{in-} + V_{CF-} - \frac{C_I}{C_F} V_{CI-}} \tag{30.14-7}$$

From equation 30.14-6 and 30.14-7, the fully differential output signal or transfer function of the circuit in figure 30.14-1 can be written as follow,

$$\boxed{v_{OUT} = v_{OUT+} - v_{OUT-} = \frac{C_I}{C_F}(v_{in+} - v_{in-}) + (V_{CF+} - V_{CF-}) - \frac{C_I}{C_F}(V_{CI+} - V_{CI-})} \tag{30.14-8}$$

The block diagram of the equation 30.14-7 is shown in the figure 30.14-2.

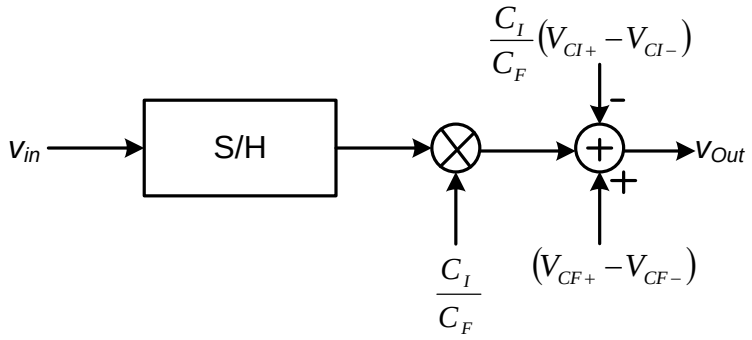


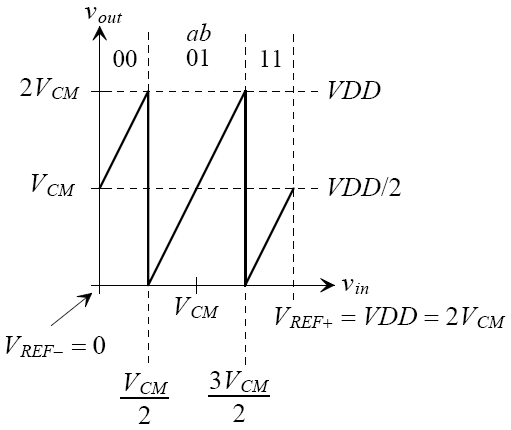
Figure 30.14-2 Block diagram of equation 30.14-7.

Justin Wood

30.15 Repeat Ex. 30.16 if the input voltage is 0.41V.

Repeat Ex. 30.10 if 1.5 bits/stage are used. Assume the converter is ideal and the comparators switch precisely at $V_{CM}/2$ (=250mV here) and $3V_{CM}/2$ (= 750mV here). Assume all latches initially contain zeros.

The transfer curve for the 1.5 bits/stage ADC is shown below.



Single-ended input and output

For the first stage, V_{IN} = 410mV. With V_{IN} between $V_{CM}/2$ and $3V_{CM}/2$, $a_{1.5(7)}b_{1.5(7)}$ would be 01. Therefore, we subtract $V_{CM}/2$ (250mV) from the V_{IN}, multiply by 2, and feed it to the next stage (V_{OUT} would be 320mV). The digital output bits are then determined based on the $a_{1.5(n)}b_{1.5(n)}$ and carry value c_n. To determine the digital outputs, we use equations 30.67, 30.68, 30.71, and 30.72 as shown below.

$$b_0 = \overline{a_{1.5(0)}} b_{1.5(0)}$$
$$c_0 = a_{1.5(0)}$$
$$b_1 = \overline{a_{1.5(1)}} b_{1.5(1)} \oplus c_0$$
$$c_1 = \overline{a_{1.5(1)}} b_{1.5(1)} c_0$$
$$b_{n-1} = \overline{a_{1.5(n-1)}} b_{1.5(n-1)} \oplus a_{1.5(n-2)} \oplus c_{n-2}$$
$$c_{n-1} = \overline{a_{1.5(n-1)}} b_{1.5(n-1)} a_{1.5(n-2)} + c_{n-2}\left(\overline{a_{1.5(n-1)}} b_{1.5(n-1)} + a_{1.5(n-2)}\right)$$
$$b_n = a_{1.5(n-1)} \oplus c_{n-1}$$

V_{IN}, $a_{1.5n}b_{1.5n}$, V_{OUT}, and Digital output for each stage are shown in the table below.

Stage	V_{IN}	$a_{1.5(n)}b_{1.5(n)}$	V_{OUT}	Digital Output
1 (n=7)	410mV	01	320mV	$b_7 = \overline{a_{1.5(7)}}b_{1.5(7)} \oplus a_{1.5(6)} \oplus c_6 = 1$ $c_7 = \overline{a_{1.5(7)}}b_{1.5(7)}a_{1.5(6)} + c_6\left(\overline{a_{1.5(7)}}b_{1.5(7)} + a_{1.5(6)}\right) = 0$
2 (n=6)	320mV	01	140mV	$b_6 = \overline{a_{1.5(6)}}b_{1.5(6)} \oplus a_{1.5(5)} \oplus c_5 = 1$ $c_6 = \overline{a_{1.5(6)}}b_{1.5(6)}a_{1.5(5)} + c_5\left(\overline{a_{1.5(6)}}b_{1.5(6)} + a_{1.5(5)}\right) = 0$
3 (n=5)	140mV	00	780mV	$b_5 = \overline{a_{1.5(5)}}b_{1.5(5)} \oplus a_{1.5(4)} \oplus c_4 = 1$ $c_5 = \overline{a_{1.5(5)}}b_{1.5(5)}a_{1.5(4)} + c_4\left(\overline{a_{1.5(5)}}b_{1.5(5)} + a_{1.5(4)}\right) = 0$
4 (n=4)	780mV	11	60mV	$b_4 = \overline{a_{1.5(4)}}b_{1.5(4)} \oplus a_{1.5(3)} \oplus c_3 = 0$ $c_4 = \overline{a_{1.5(4)}}b_{1.5(4)}a_{1.5(3)} + c_3\left(\overline{a_{1.5(4)}}b_{1.5(4)} + a_{1.5(3)}\right) = 0$
5 (n=3)	60mV	00	620mV	$b_3 = \overline{a_{1.5(3)}}b_{1.5(3)} \oplus a_{1.5(2)} \oplus c_2 = 1$ $c_3 = \overline{a_{1.5(3)}}b_{1.5(3)}a_{1.5(2)} + c_2\left(\overline{a_{1.5(3)}}b_{1.5(3)} + a_{1.5(2)}\right) = 0$
6 (n=2)	620mV	01	740mV	$b_2 = \overline{a_{1.5(2)}}b_{1.5(2)} \oplus a_{1.5(1)} \oplus c_1 = 0$ $c_2 = \overline{a_{1.5(2)}}b_{1.5(2)}a_{1.5(1)} + c_1\left(\overline{a_{1.5(2)}}b_{1.5(2)} + a_{1.5(1)}\right) = 1$
7 (n=1)	740mV	01	980mV	$b_1 = \overline{a_{1.5(1)}}b_{1.5(1)} \oplus c_0 = 0$ $c_1 = \overline{a_{1.5(1)}}b_{1.5(1)}c_0 = 1$
8 (n=0)	980mV	11	460mV	$b_0 = \overline{a_{1.5(0)}}b_{1.5(0)} = 0$ $c_0 = a_{1.5(0)} = 1$
-	-	-	-	$b_8 = a_{1.5(7)} \oplus c_7 = 0$

The bits b_8 -> b_0 are 0 1110 1000 (232). Subtracting 0 0111 1111 (127) from $b_{8->0}$ gives us our final output, which is 0 0110 1001 (105).

Adam Johnson

30.16 Repeat Ex. 30.17 if the input voltage is 0.41 V.

Equivalent problem: Determine the output of the ADC in Fig. 30.38 if the input voltage is 0.41 V, and 1.5 bits/stage are used, and comparators switch at 305 mV and 675 mV. Assume all latches initially are zero.

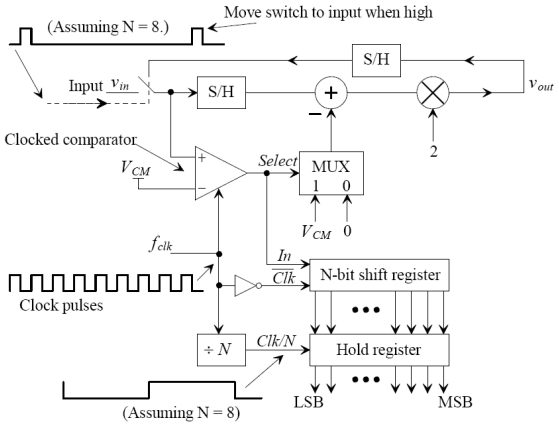


Figure 30.38 Block diagram of a cyclic ADC.

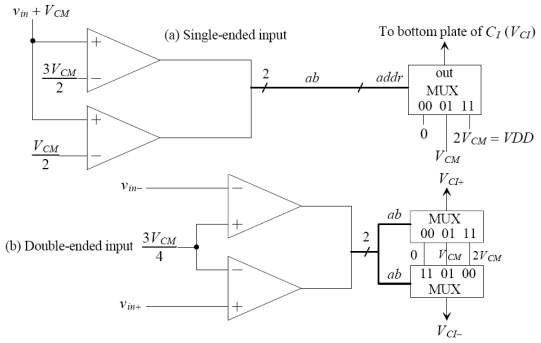


Figure 30.51 Implementing comparators and MUX for 1.5 bits.

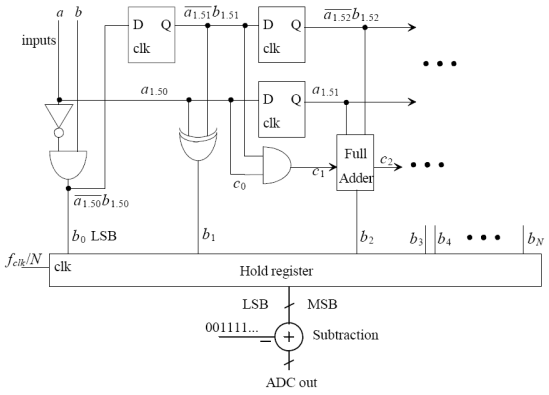


Figure 30.53 Combining the outputs of the cyclic ADC when 1.5 bits/stage is used.

Using Eq. (30.60), we can find v_{out}, where $v_{in,k-1} = v_{out,k}$, calculating v_{in}, $a_{1.5x}b_{1.5x}$ and v_{out} from k=N-1 to k=0. We calculate the digital output b_k and c_k from k=0 to k=N-1.

v_{in}	$a_{1.5x}b_{1.5x}$	v_{out}	Digital out
410 mV (N-1 = 7)	01	320 mV	$b_7 = \overline{a_{1.57}}b_{1.57} \oplus a_{1.56} \oplus \overline{c_6} = 1$ $c_7 = \overline{a_{1.57}}b_{1.57}a_{1.56} + c_6(\overline{a_{1.57}}b_{1.57} + a_{1.56}) = 0$
320 mV (N-2 = 6)	01	140 mV	$b_6 = \overline{a_{1.56}}b_{1.56} \oplus a_{1.55} \oplus \overline{c_5} = 1$ $c_6 = \overline{a_{1.56}}b_{1.56}a_{1.55} + c_5(\overline{a_{1.56}}b_{1.56} + a_{1.55}) = 0$
140 mV (N-3 = 5)	00	780 mV	$b_5 = \overline{a_{1.55}}b_{1.55} \oplus a_{1.54} \oplus \overline{c_4} = 1$ $c_5 = \overline{a_{1.55}}b_{1.55}a_{1.54} + c_4(\overline{a_{1.55}}b_{1.55} + a_{1.54}) = 0$

780 mV (N-4 = 4)	11	60 mV	$b_4 = \overline{a_{1.54}} b_{1.54} \oplus a_{1.53} \oplus c_3 = 0$ $c_4 = \overline{a_{1.54}} b_{1.54} a_{1.53} + c_3(\overline{a_{1.54}} b_{1.54} + a_{1.53}) = 0$
60 mV (N-5 = 3)	00	620 mV	$b_3 = \overline{a_{1.53}} b_{1.53} \oplus a_{1.52} \oplus c_2 = 1$ $c_3 = a_{1.53} b_{1.53} a_{1.52} + c_2(\overline{a_{1.53}} b_{1.53} + a_{1.52}) = 0$
620 mV (N-6 = 2)	01	740 mV	$b_2 = \overline{a_{1.52}} b_{1.52} \oplus a_{1.51} \oplus c_1 = 0$ $c_2 = a_{1.52} b_{1.52} a_{1.51} + c_1(\overline{a_{1.52}} b_{1.52} + a_{1.51}) = 1$
740 mV (N-7 = 1)	11	-20 mV	$b_1 = \overline{a_{1.51}} b_{1.51} \oplus c_0 = 0$ $c_1 = a_{1.51} b_{1.51} a_{1.50} + c_0(\overline{a_{1.51}} b_{1.51} + a_{1.50}) = 0$
-20 mV (N-8 = 0)	00	460 mV	$b_0 = \overline{a_{1.50}} b_{1.50} = 0$ $c_0 = a_{1.50} = 0$

and $b_8 = a_{1.57} \oplus c_7 = 0$. Therefore, subtracting 001111111… to remove the (V_{CM} - 0.5 LSB) component,

$$\begin{array}{rl} & 0\ 1110\ 1000\ (232) \\ -\ & \underline{0\ 0111\ 1111\ (127)} \\ & 0\ 0110\ 1001\ (105) \end{array}$$

We can evaluate the analog equivalent of the digital output as follows.

$$V_{OUT} = \frac{105}{255} \cdot 1V = 412mV$$

30.17 Resketch the clock waveforms for Fig. 30.54 if bottom plate sampling were used.

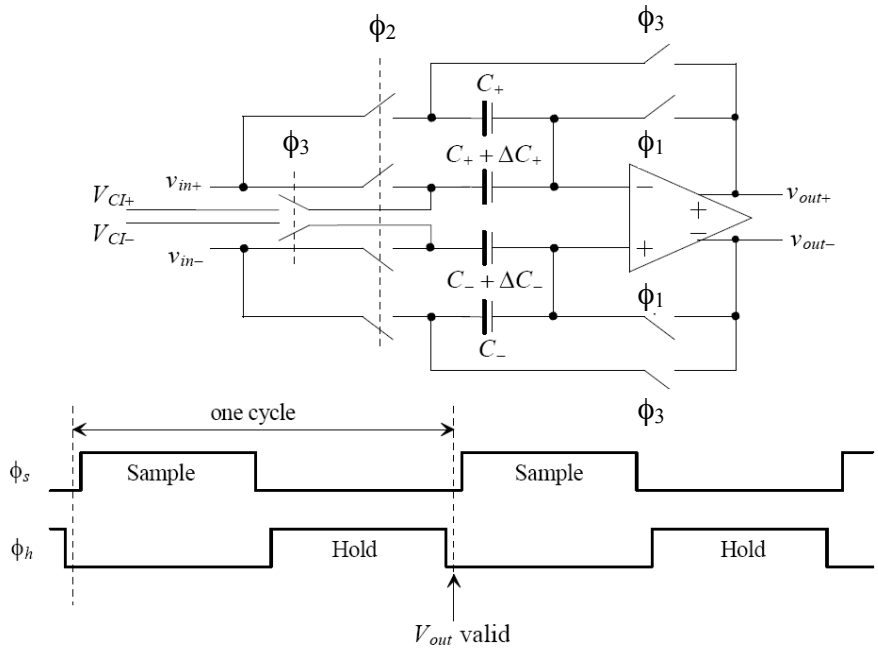
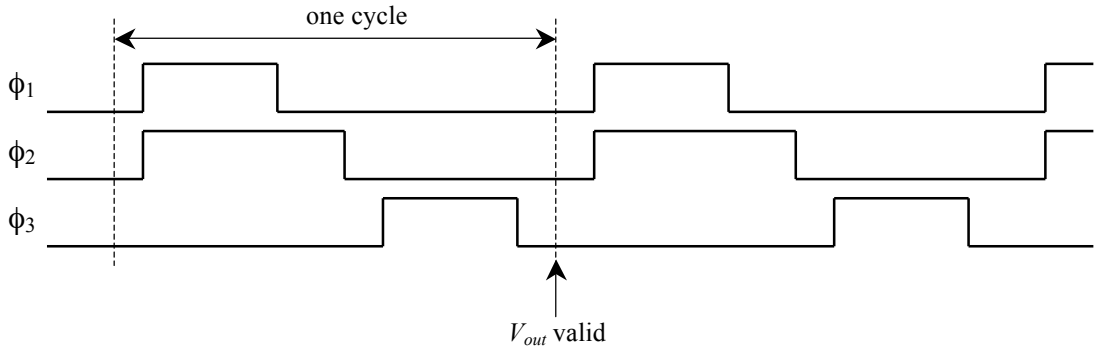


Figure 30.54 S/H of Fig. 30.42 with mismatched capacitors.

Figure 30.54 waveform with bottom plate sampling.



30.18 Show the derivation leading up to Eq. (30.83). Show, using practical values for mismatch, how the squared mismatch terms are negligible.

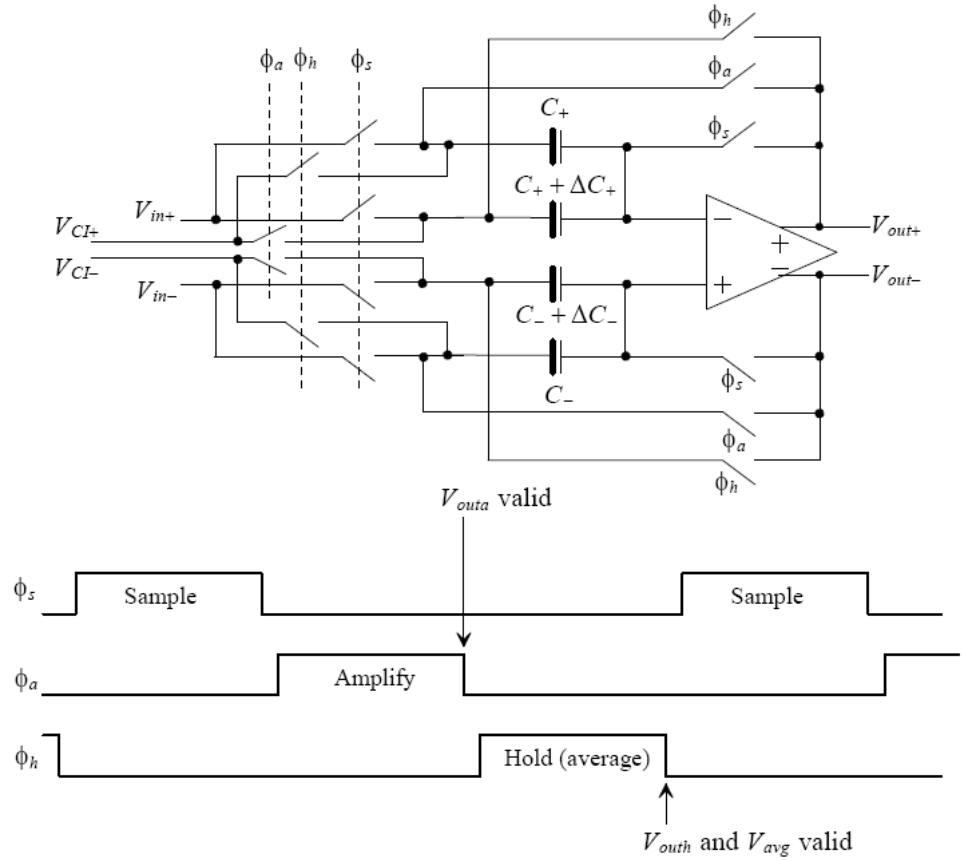


Figure 30.55 S/H using capacitor error averaging.

Starting with equation 30.82 the derivation is as follows:

$$v_{outh+} = \left(1 - \frac{\Delta C_+}{C_+}\right) \cdot v_{outa+} + \left(\frac{\Delta C_+}{C_+}\right) \cdot V_{CI+} \qquad (30.82)$$

Substituting 30.76 to replace v_{outa+}

$$v_{outh+} = \left(1 - \frac{\Delta C_+}{C_+}\right) \cdot \left(2 \cdot v_{in+} - V_{CI+} + \frac{\Delta C_+}{C_+} \cdot \left(v_{in+} - V_{CI+}\right)\right) + \left(\frac{\Delta C_+}{C_+}\right) \cdot V_{CI+}$$

multiplying terms thru yields:

$$v_{outh+} = 2 \cdot v_{in+} - V_{CI+} + \frac{\Delta C_+}{C_+} \cdot \left(v_{in+} - V_{CI+}\right) - \left[2 \cdot v_{in+} \frac{\Delta C_+}{C_+} - V_{CI+} \frac{\Delta C_+}{C_+} + \left(\frac{\Delta C_+}{C_+}\right)^2 \cdot \left(v_{in+} - V_{CI+}\right)\right] + \left(\frac{\Delta C_+}{C_+}\right) \cdot V_{CI+}$$

collecting like terms and reordering yields:

$$v_{outh+} = 2 \cdot v_{in+} - V_{CI+} + \frac{\Delta C_+}{C_+} \cdot \left(v_{in+} - V_{CI+}\right) - 2 \cdot v_{in+} \frac{\Delta C_+}{C_+} + V_{CI+} \frac{\Delta C_+}{C_+} - \left(\frac{\Delta C_+}{C_+}\right)^2 \cdot \left(v_{in+} - V_{CI+}\right) + \left(\frac{\Delta C_+}{C_+}\right) \cdot V_{CI+}$$

$$v_{outh+} = 2 \cdot v_{in+} - V_{CI+} + \frac{\Delta C_+}{C_+} \cdot \left(v_{in+} - V_{CI+}\right) - 2 \cdot v_{in+} \frac{\Delta C_+}{C_+} + 2 \cdot V_{CI+} \frac{\Delta C_+}{C_+} - \left(\frac{\Delta C_+}{C_+}\right)^2 \cdot \left(v_{in+} - V_{CI+}\right)$$

$$v_{outh+} = 2 \cdot v_{in+} - V_{CI+} + \frac{\Delta C_+}{C_+} \cdot \left(v_{in+} - V_{CI+}\right) - \frac{2 \cdot \Delta C_+}{C_+} \cdot \left(v_{in+} - V_{CI+}\right) - \left(\frac{\Delta C_+}{C_+}\right)^2 \cdot \left(v_{in+} - V_{CI+}\right)$$

$$v_{outh+} = 2 \cdot v_{in+} - V_{CI+} - \frac{\Delta C_+}{C_+} \cdot \left(v_{in+} - V_{CI+}\right) - \left(\frac{\Delta C_+}{C_+}\right)^2 \cdot \left(v_{in+} - V_{CI+}\right)$$

The assumption made for equation 30.83 was that the $(\Delta C_+/C_+)^2$ term was negligible, which allows us to simplify to equation 30.83

$$v_{outh+} = 2 \cdot v_{in+} - V_{CI+} - \frac{\Delta C_+}{C_+} \cdot \left(v_{in+} - V_{CI+}\right) \qquad (30.83)$$

Let's assume v_{in} = 0.5V (v_{in+}=0.75V, v_{in-}=0.25V). Ideally, v_{out+} would equal 1V. Our process typically has a 1% capacitor mismatch (1.00pF vs. 1.01pF). Ignoring the $(\Delta C_+/C_+)^2$ term the output would be:

$$v_{outh+} = 2 \cdot 0.75 - 0.5 - \frac{0.01}{1} \cdot \left(0.75 - 0.5\right) = 0.9975 mV$$

If we include the $(\Delta C_+/C_+)^2$ term the output would be:

$$v_{outh+} = 2 \cdot 0.75 - 0.5 - \frac{0.01}{1} \cdot \left(0.75 - 0.5\right) - \left(\frac{0.01}{1}\right)^2 \cdot \left(0.75 - 0.5\right) = 0.997475 mV$$

The resulting error from the squared term is two order of magnitudes smaller and is negligible.

(P.30.19)What happens to the error adjustment term in Eq. (30.92) if the capacitors in the S/H are perfectly matched?

The equation 30.92 is

$$v_{avg+} - v_{avg-} = \left(v_{outa+} - v_{outa-}\right) - \frac{\left(v_{outa+} - v_{outh+}\right) - \left(v_{outa+} - v_{outh-}\right)}{2} \tag{30.19-1}$$

If the capacitors are perfectly matched in the S/H, the error adjustment term $\frac{\left(v_{outa+} - v_{outh+}\right) - \left(v_{outa+} - v_{outh-}\right)}{2}$ becomes zero. In order to prove that, consider the figure shown in figure 30.19-1.

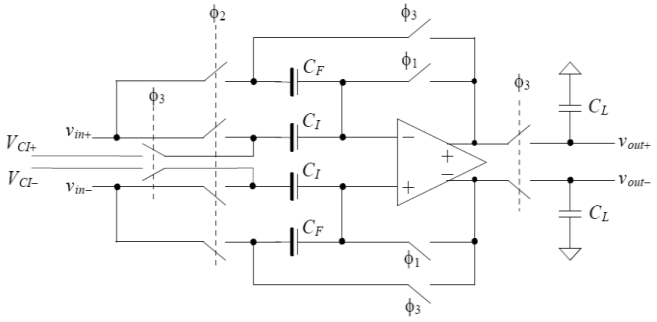


Figure 30.19-1 S/H circuit without mismatch.

From the figure 30.19-1, v_{out+} and v_{out-} can be written as follow,

$$v_{Out+} = 2v_{in+} - V_{CI+} = v_{Outa+} \tag{30.19-2}$$

$$v_{Out-} = 2v_{in-} - V_{CI-} = v_{Outa-} \tag{30.19-3}$$

In order to overcome the capacitor mismatch in S/H, S/H circuit is implemented with capacitor error averaging as shown in the figure 30.19-2.

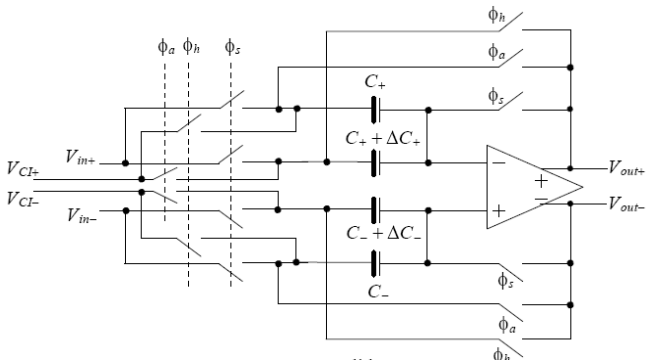


Figure 30.19-2 S/H circuit using capacitor error averaging.

From figure 30.19-2, the output is given as

$$v_{Out+} = 2v_{in+} - V_{CI+} - \frac{\Delta C}{C}\left(v_{in+} - V_{CI+}\right) \tag{30.19-4}$$

$$v_{Out-} = 2v_{in-} - V_{CI-} - \frac{\Delta C}{C}\left(v_{in-} - V_{CI-}\right) \tag{30.19-5}$$

As the problem states, if ΔC=0, then 30.19-4, 5 becomes

$$v_{Outh+} = v_{Out+} = 2v_{in+} - V_{CI+} \tag{30.19-6}$$

$$v_{Outh-} = v_{Out-} = 2v_{in-} - V_{CI-} \tag{30.19-7}$$

From equation 30.19-6, 7 and 30.19-2, 3, it is clear that $v_{Outa+} = v_{Outh+}$ and $v_{Outa-} = v_{Outh-}$. So, the error adjustment term in the 30.19-1 becomes zero. Basically if there is no capacitor mismatch, the S/H circuit with error averaging works same as figure 30.19-1 expect taking more time.

30.20 Repeat Ex. 30.18 if all capacitors are 1 pF (the ideal situation) and verify that the error out of the stage is zero.

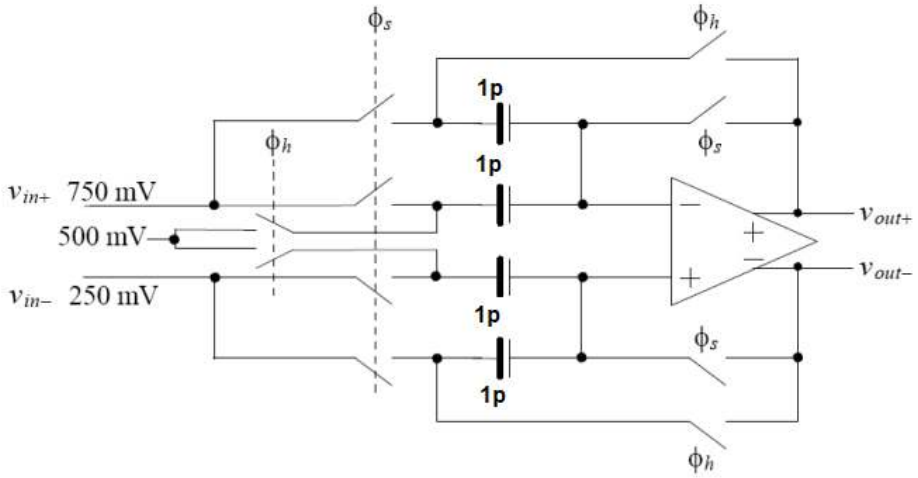


Figure 30.57 with all capacitors = 1 pF

The input voltage is:

$$v_{in} = v_{in+} - v_{in-} = 750mV - 250mV = 500mV$$

The output voltage (with the help of Eq (30.76) and Eq (30.77) is:

$$v_{out} = v_{out+} - v_{out-} = \left[2 \cdot v_{in+} - V_{CI+} + \frac{\Delta C_+}{C_+} \cdot \left(v_{in+} - V_{CI+}\right)\right] - \left[2 \cdot v_{in-} - V_{CI-} + \frac{\Delta C_-}{C_-} \cdot \left(v_{in-} - V_{CI-}\right)\right]$$

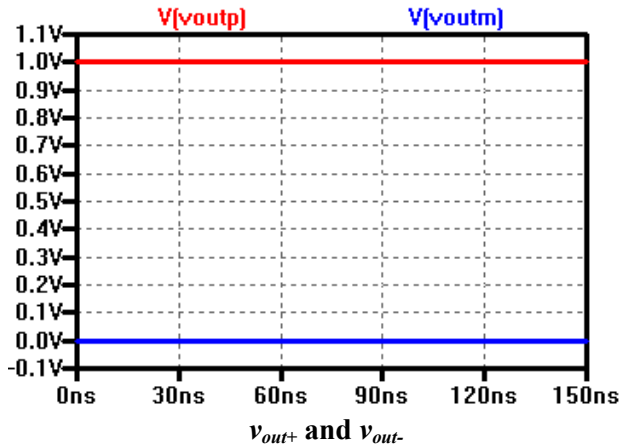
Since all of the capacitors are 1 pF, we have the ideal situation where $\frac{\Delta C}{C} = 0$.

We can then re-write the output equation as:

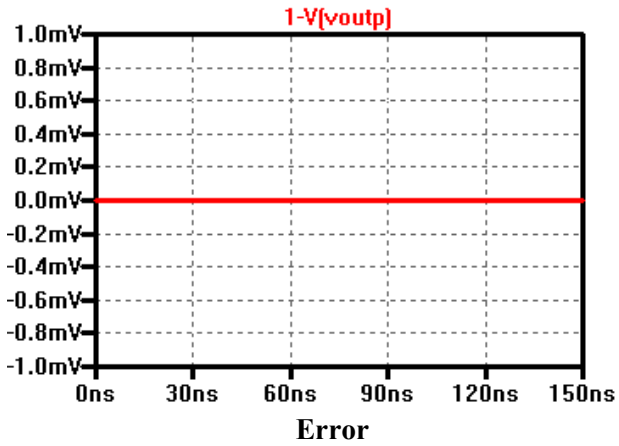
$$v_{out} = v_{out+} - v_{out-} = \left[2 \cdot v_{in+} - V_{CI+}\right] - \left[2 \cdot v_{in-} - V_{CI-}\right]$$

$$v_{out} = v_{out+} - v_{out-} = \left[2 \cdot 750mV - 500mV\right] - \left[2 \cdot 250mV - 500mV\right] = 1V - 0V = 1V$$

The simulation results are shown below. We have the ideal output voltages of $v_{out+} = 1V$ and $v_{out-} = 0V$, and thus the error out of the stage is 0.



v_{out+} and v_{out-}



Error

30.21 Sketch a circuit to provide the inputs for the four-phase, nonoverlapping clock generator shown in Fig. 30.81.

We can refer to Figures 30.64 and 30.65 for one possible solution. The figures show an implementation for a three-phase nonoverlapping clock. It is a fairly trivial task to extend it to work for a four-phase nonoverlapping clock.

Looking at Fig. 30.65, we can see that two flip-flops are used but we are only generating three output signals. We should be able to slightly modify the circuit to give us our four-phase solution. First, looking at Fig. 30.65, we can determine the values of D_1, D_2, Q_1, Q_2, In1, In2, and In3 as shown below.

Clock Cycle	D1	D2	Q1	Q2	In1	In2	In3
0	-	-	0	0	1	1	0
1	0	1	0	1	1	0	1
2	1	1	1	1	0	1	1
3	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.

Notice that there is one unused state (D_1=1, D_2=0). We can use this state to generate the low pulse for the fourth output (In4 input to Fig. 30.81). The added state is shown in red in the figure below.

Clock Cycle	D1	D2	Q1	Q2	In1	In2	In3	In4
0	-	-	0	0	1	1	0	1
1	0	1	0	1	1	0	1	1
2	1	1	1	1	0	1	1	1
3	1	0	1	0	1	1	1	0
4	0	0	0	0	1	1	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

Utilizing some simple Karnaugh maps (or just eyeball it), we can simplify the combinations logic for the flip-flop inputs and the output signals (In1-4) as follows:

$$D_{1,n} = Q_{2,n-1}$$

$$D_{2,n} = \overline{Q_{1,n-1}}$$

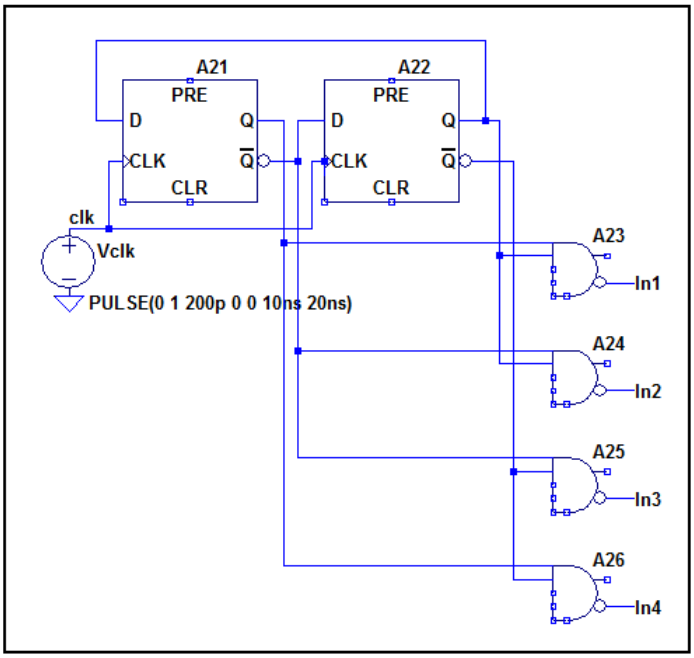
$$In1 = \overline{Q_1 \cdot Q_2}$$

$$In2 = \overline{\overline{Q_1} \cdot Q_2}$$

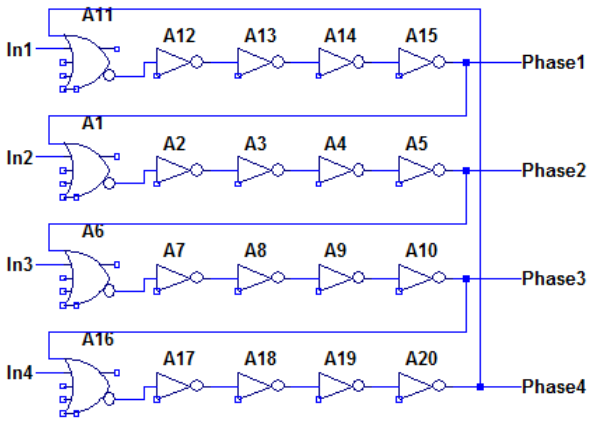
$$In3 = \overline{\overline{Q_1} \cdot \overline{Q_2}}$$

$$In4 = \overline{Q_1 \cdot \overline{Q_2}}$$

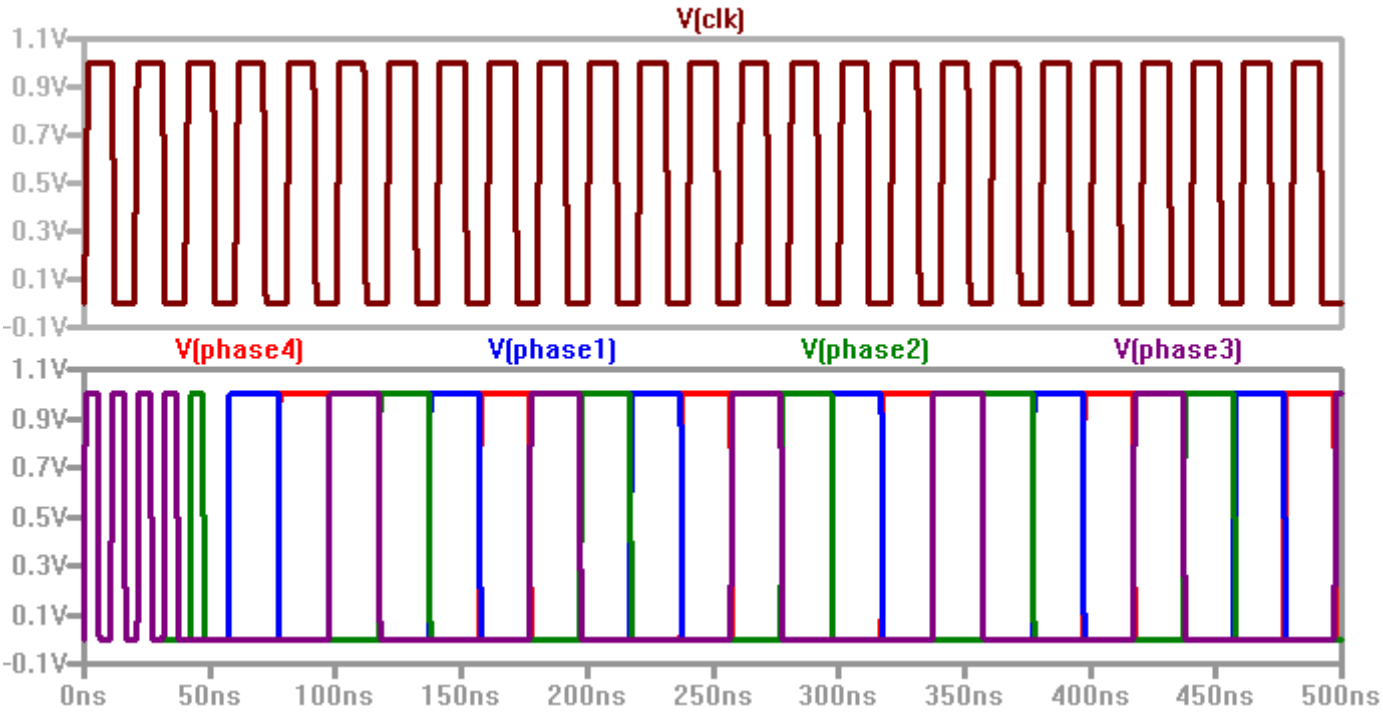
The schematics and simulation results are shown below.



Solution to Problem 30.21



Circuit from Fig. 30.81



Simulation Results (T_{clk}=20ns)

(P.30.22)What is the main advantage of using dynamic CMFB over other CMFB circuits? What is the main disadvantage?

Main advantages of using dynamic CMFB over other CMFB circuits are

(i) Dynamic CMFB loop set no restriction on maximum allowable differential input signal unlike other CMFB circuits.
(ii) Dynamic CMFB have no additional parasitic poles in common mode loop.
(iii) No slew rate limitation and unity gain of frequency in common mode loop like other CMFB circuits.
(iv) Loading of common load loop is relaxed with dynamic CMFB.
(v) Switched capacitor resistors used in dynamic CMFB performs both averaging and the differencing needed for CMFB amplifier.
(vi) During sampling phase, the operational amplifier inputs are forced to V_{CM} rather than forcing it to $V_{CM}+V_{OS}$ like other topologies.
(vii) Dynamic CMFB is very linear.

Main disadvantages of using dynamic CMFB over other CMFB circuits are

(i) Other CMFB circuits don't have charge injection and leakage current errors for faster settling and lower clock feed through noise.
(ii) Additional switches in dynamic CMFB circuitry to avoid operational amplifier output to sink/source a current into V_{CM} causes the operational amplifier output to approach the power supply rails during sample phase. But this is not a big issue on OTA based design.

Justin Wood

30.23 Can MOSFETs be used to implement the on-chip decoupling capacitors in Fig. 30.77?

Yes. Typically the decoupling capacitors are very large, but it is common to split it up into many smaller capacitors connected in parallel, which would allow an array of MOSFETs to serve as the decouping capacitor. However, depending on the MOSFET characteristics problems would arise. One potential problem with using MOSFETs would be an increased leakage over other types of capacitors. Leakage thru the MOSFETs results in the DC current flowing in our reference voltages, which typically is not desired. The DC current can cause a drop in supply voltage to the analog or digital circuit and consequently cause problems when the output signal approaches your supply voltage.

Using thick gateox MOSFETs may result in less leakage, but results in a tradeoff for layout area as the MOSFET capacitance would also drop. They may also be advantages to using PMOS vs. NMOS depending on the process as they may be better isolated from substrate noise that could couple onto the supplies.

There would obviously be tradeoffs, but in general, MOSFETs could serve as viable option for on-chip decoupling capacitors.

30.24 Sketch the cross-sectional view of the layout in Fig. 30.78.

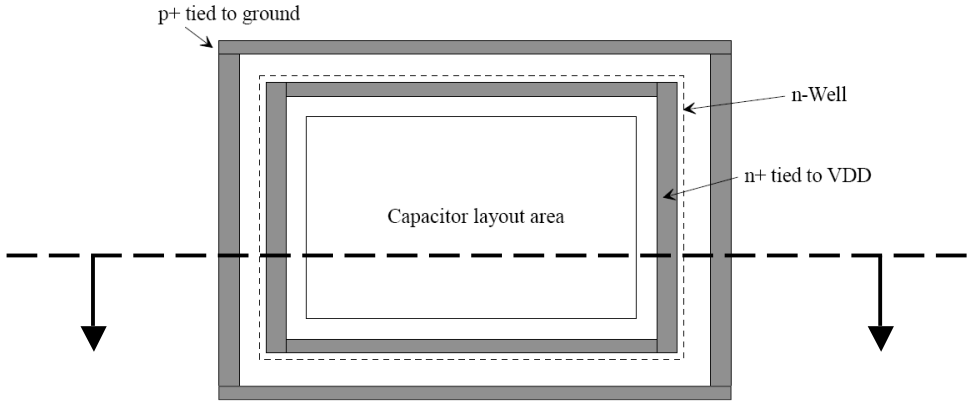
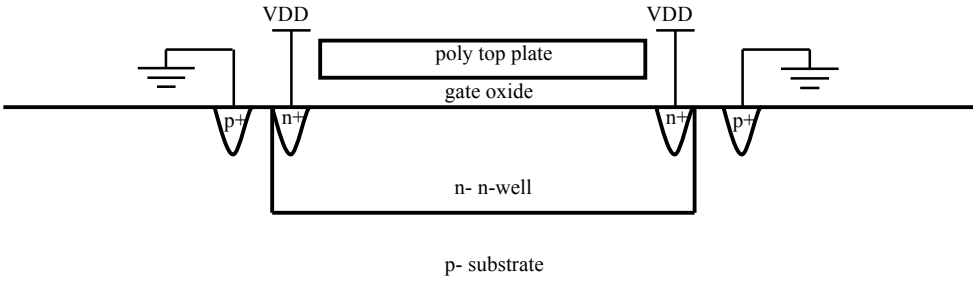


Figure 30.78 Using guard rings for protection in sensitive analog blocks.



30.25 Figure 30.82 shows the implementation of a pipeline DAC. How would we implement this DAC using a topology similar to Fig. 30.42? Sketch the DAC's implementation and the timing signals (clock phases) used.

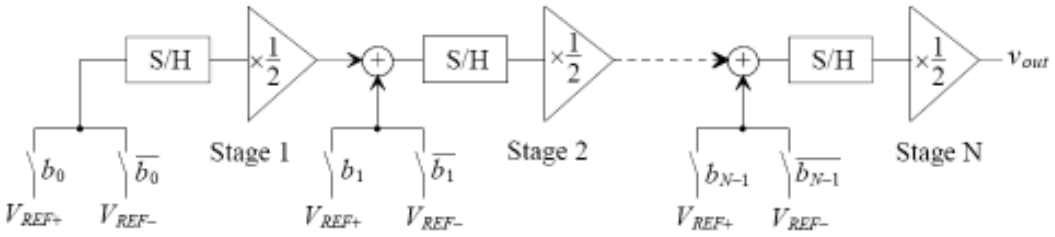


Figure 30.82 A pipeline digital-to-analog converter.

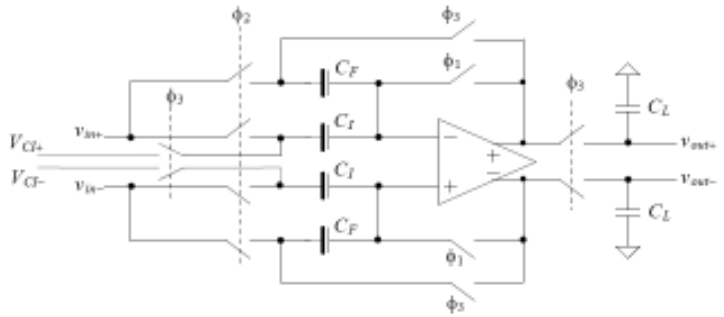


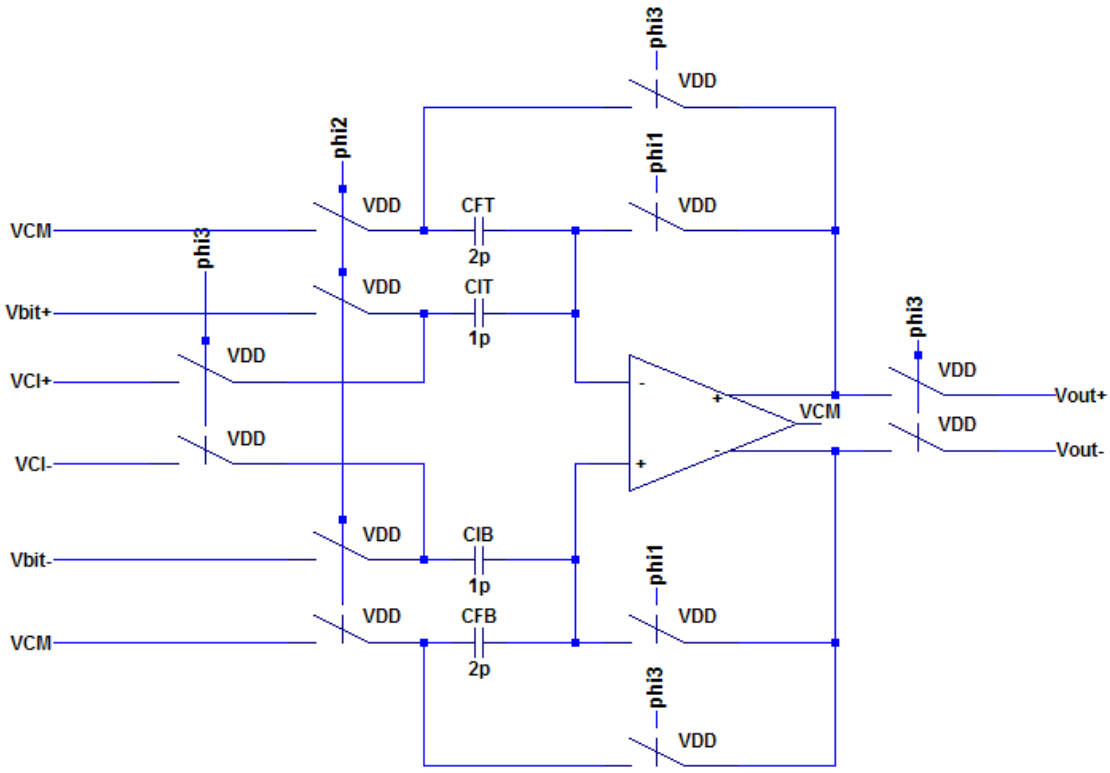
Figure 30.42 S/H used in Ex. 30.12

For this implementation, we use Fig. 30.42 as a starting point but make some simple modifications. Consider the circuit shown on the next page. It is one stage of a pipeline DAC implementation based on the S/H circuit of Fig. 30.42. First of all, since we need a x$\frac{1}{2}$ multiplication, we must get rid of the "+1" in the gain equation (see Eq. 30.53). We accomplish this by connecting the left side of the C_F capacitors to V_{CM} instead of v_{in}. With this modification, the gain will be reduced to just $\frac{C_I}{C_F}$. The output equation is then:

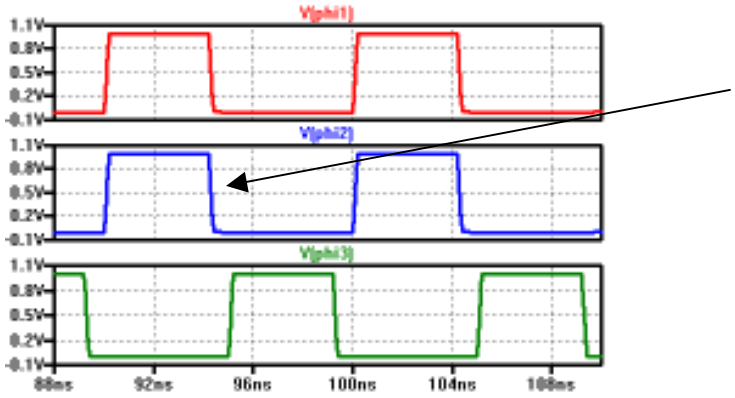
$$v_{out} = v_{out+} - v_{out-} = \frac{C_I}{C_F} \cdot \left[\left(v_{in+} - v_{in-} \right) - \left(V_{CI+} - V_{CI-} \right) \right]$$

To get a gain of 0.5, we simply set C_I = 1 pF and C_F = 2 pF. Next, we will add the output voltage of the previous stage to the current stage's input by simply connecting the outputs of the previous stage to the V_{CI} inputs of the current stage. Since we do not want to subtract but rather want to add, we will connect the positive output of the previous stage to the current stage's V_{CI-} input, and we will connect the negative output of the previous stage to the current stage's V_{CI+} input.

With these simple modifications, we basically have all we need to implement the pipeline DAC. The clock signals will be the same nonoverlapping clock signals used in Fig. 30.42. A schematic of one stage is shown below along with the clock signals.



One Stage of Pipeline DAC

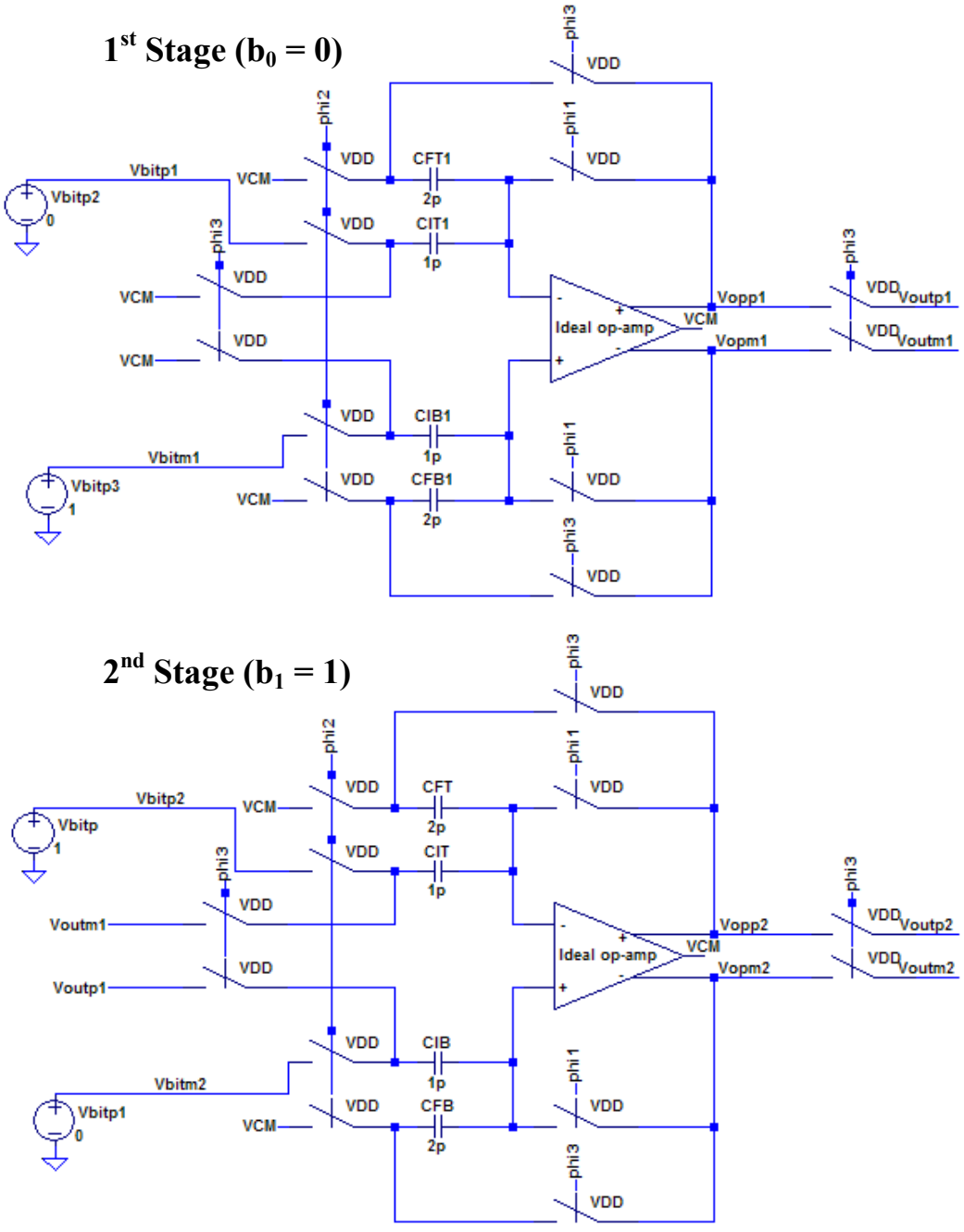


Phi2 clock falling edge should be slightly delayed from Phi1. It is not delayed in the sim since we are using an ideal op-amp in the sim. The response of the ideal op-amp is so fast it will cause issues if Phi1 and Phi2 are not the same.

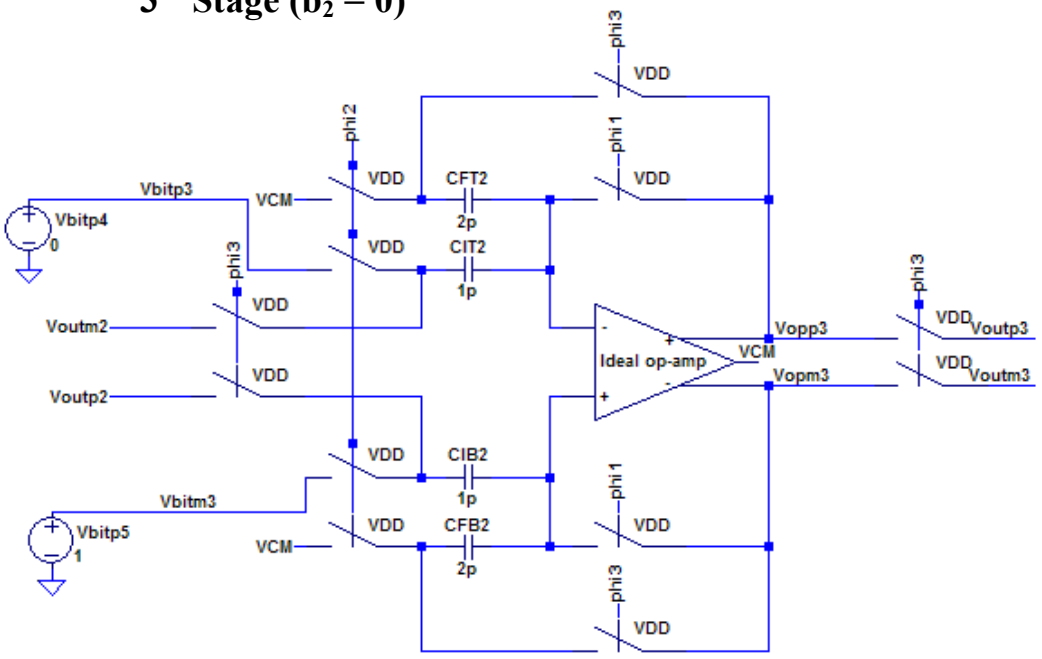
Clock Signals Used in Pipeline DAC

To demonstrate the correct operation of this design, a 4-bit pipeline DAC was implemented using this topology. The schematics of each stage and the final simulation results are shown below.

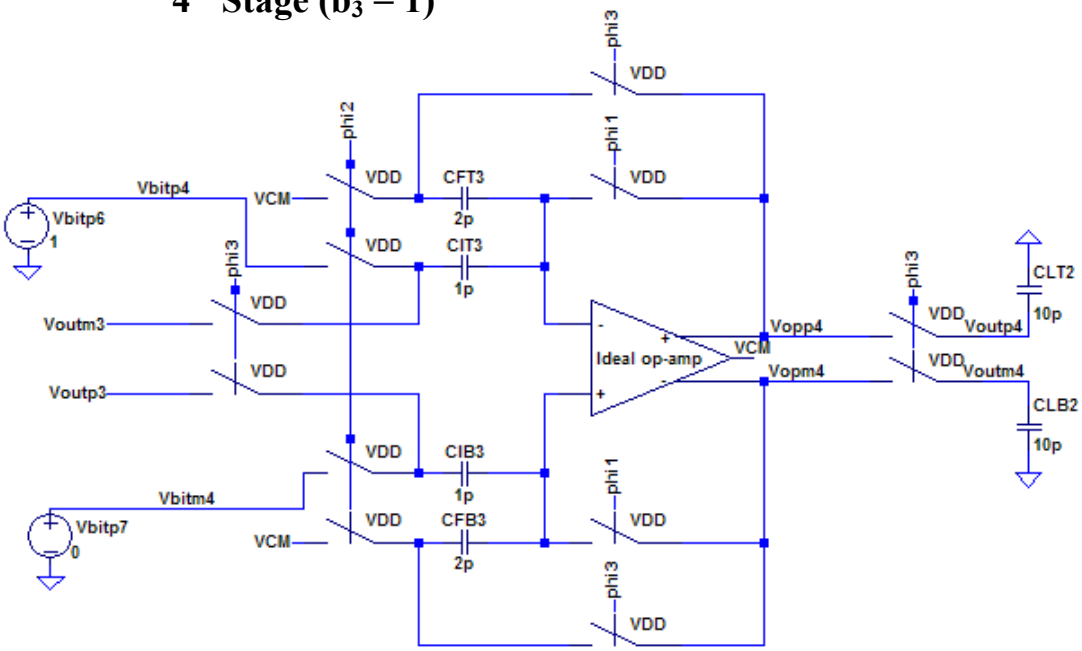
The input to the DAC is 0101 (MSB->LSB) and we expect the output to be 0.3125 V (see Example 29.9). Also note that V_{REF} = 1 V.

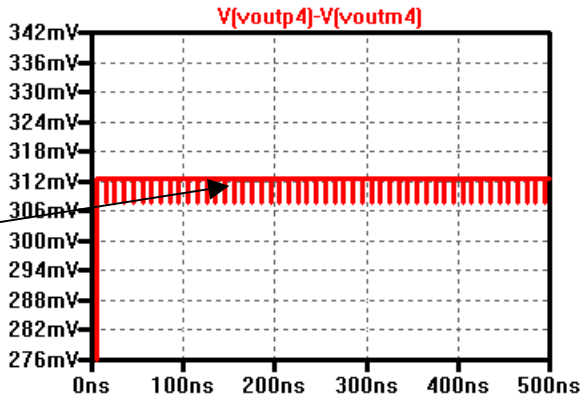


3rd Stage ($b_2 = 0$)



4th Stage ($b_3 = 1$)





The output is 0.3125 V as expected

Simulation Results of the 4-bit pipeline DAC