Problem 17.1

Regenerate Table 17.1. If the water level where a cup of water is removed is 4.7 instead of 5. How are the results affected? If the sensing time is increased how are the final results affected (compare a water level of 5 against 4.7).

In table 17.1, if the water level to remove a cup of water is 4.7 instead of 5, the results are not affected. This is shown in the table below.

Time (sec)	Water level in sigma buckets(cup)	Remove cup?	Running average
0	4.7	no	0
10	4.95	**yes**	1
20	4.2	no	0.5
30	4.45	no	0.33
40	4.7	no	0.25
50	4.95	**yes**	0.4
60	4.2	no	0.33
70	4.45	no	0.29
80	4.7	no	0.25
90	4.95	**yes**	0.33
100	4.2	no	0.3
110	4.45	no	0.27
120	4.7	no	0.25
130	4.95	**yes**	0.3
140	4.2	no	0.29
150	4.45	no	0.26
160	4.7	no	0.25
170	4.95	**yes**	0.29

In the following table, the sensing time increases to 370 sec. The final results compare both water level 5 and 4.7. From the table we can see, the longer we sense the closer our output moves to 0.25 cup/10 seconds. And, if there is any error, it will average out over time.

Water level =4.7 cup: Water level =5 cup:

Time (sec)	Water level in sigma buckets(cup)	Remove cup?	Running average	Water level in sigma buckets(cup)	remove cup?	Running average
0	4.7	no	0	5	no	0
10	4.95	**yes**	1	5.25	**yes**	1
20	4.2	no	0.5	4.5	no	0.5
30	4.45	no	0.33	4.75	no	0.33
40	4.7	no	0.25	5	no	0.25
50	4.95	**yes**	0.4	5.25	**yes**	0.4
60	4.2	no	0.33	4.5	no	0.33
70	4.45	no	0.29	4.75	no	0.29
80	4.7	no	0.25	5	no	0.25
90	4.95	**yes**	0.33	5.25	**yes**	0.33
100	4.2	no	0.3	4.5	no	0.3
110	4.45	no	0.27	4.75	no	0.27
120	4.7	no	0.25	5	no	0.25
130	4.95	**yes**	0.3	5.25	**yes**	0.3
140	4.2	no	0.29	4.5	no	0.29
150	4.45	no	0.26	4.75	no	0.26
160	4.7	no	0.25	5	no	0.25
170	4.95	yes	0.29	5.25	yes	0.29
180	4.2	no	0.28	4.5	no	0.28
190	4.45	no	0.26	4.75	no	0.26
200	4.7	no	0.25	5	no	0.25
210	4.95	yes	0.29	5.25	yes	0.29
220	4.2	no	0.27	4.5	no	0.27
230	4.45	no	0.26	4.75	no	0.26
240	4.7	no	0.25	5	no	0.25
250	4.95	**yes**	0.28	5.25	**yes**	0.28
260	4.2	no	0.27	4.5	no	0.27
270	4.45	no	0.26	4.75	no	0.26
280	4.7	no	0.25	5	no	0.25
290	4.95	**yes**	0.28	5.25	**yes**	0.28
300	4.2	no	0.27	4.5	no	0.27
310	4.45	no	0.26	4.75	no	0.26
320	4.7	no	0.25	5	no	0.25
330	4.95	**yes**	0.27	5.25	**yes**	0.27
340	4.2	no	0.26	4.5	no	0.26
350	4.45	no	0.26	4.75	no	0.26
360	4.7	no	0.25	5	no	0.25
370	4.95	**yes**	0.27	5.25	**yes**	0.27

Problem 17.2

time, seconds	water level in the sigma bucket (cups)	add cup? (water level > 5?)	Running average
0	5	no	0
10	4.7	yes	0.5
20	5.4	no	0.33
30	5.1	no	0.25
40	4.8	yes	0.4
50	5.5	no	0.33
60	5.2	no	0.29
70	4.9	yes	0.38
80	5.6	no	0.33
90	5.3	no	0.3
100	5	no	0.27
110	4.7	yes	0.33
120	5.4	no	0.31
130	5.1	no	0.29
140	4.8	yes	0.33
150	5.5	no	0.31
160	5.2	no	0.29
170	4.9	yes	0.33

note: assume 5 cups initially; 0.3 cups leaves every 10 seconds

P17.3

Referring to figure 17.6, with I_{cup} replaced with a resistor R_{cup}, and assuming that the clock frequency is large, (this is required so that ΔV_{bit} is small, which simplifies the equations.) Equations 17.3 through 17.8 are derived below,

$$\text{With, } I_{cup} = I_R = \frac{VDD - V_{bit}}{R_{cup}}$$

$$\frac{I_{bit}}{C_{bit}} = \frac{\Delta V_{bit}}{T} \quad (17.3)$$

$$Q_{bit} = I_{bit} * T = C_{bit} * \Delta V_{bit} \quad (17.4)$$

$$Q_{cup} = \frac{VDD - V_{bit}}{R_{cup}} * \frac{M}{N} * T \quad (17.5)$$

$$Q_{bit} = I_{bit} * T = Q_{cup} = \frac{VDD - V_{bit}}{R_{cup}} * \frac{M}{N} * T \quad (17.6)$$

$$I_{bit} * \frac{R_{cup}}{VDD - V_{bit}} = \frac{M}{N} \quad (17.7)$$

$$\Delta V_{bit,max} = \frac{VDD - V_{bit}}{R_{cup}} * \frac{T}{C_{bit}} \quad (17.8)$$

The current through the resistor must be larger than the I_{bit}. If it is not, the current through the resistor will not be able to keep I_{bit} fed, and V_{bit} will go to zero.

EE 5/497 Memory Circuit Design

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Prob 17-4: Demonstrate, using SPICE simulations, that the error because of parasitics, as seen in fig 17.7, is reduced by connecting the switch to a 1v source instead of ground.

[Ans]:

Based on Fig 17-4-1 and Fig 17-4-2, we can analyze the current source parasitic capacitance effects on DSM sensing precision. SPICE simulation results are shown as Fig 17-4-4, Fig17-4-5, and Fig17-4-6; summarized as Table 17-4-3.

By interpolating the simulation results, we can make the following conclusions:
(1). Sensing Error because of parasitics, as seen in fig 17.7, is reduced by connecting the switch to a VDD source instead of ground.

(2). Sensing Error due to $C_{parasitics}$ can be eliminated by choosing the proper voltage source connected to C_{par} during transition in order to compensate the charge sharing between C_{par} and $C_{bit.}$. As indicated in Fig 17-4-6, I would recommend $0.75V_{DD}$ instead of V_{DD}.

(3). Current noise through $C_{parasitics}$ is also a good indication of charge sharing or injection; we will mainly care about at NO-to-YES transitions.

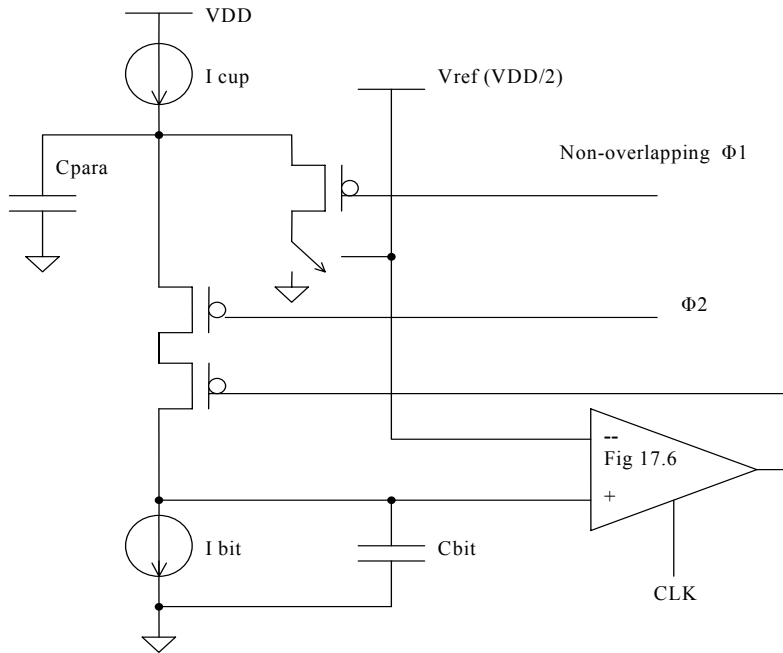Fig 17-4-1 Analysis of Current source parasitic Capacitance Effect
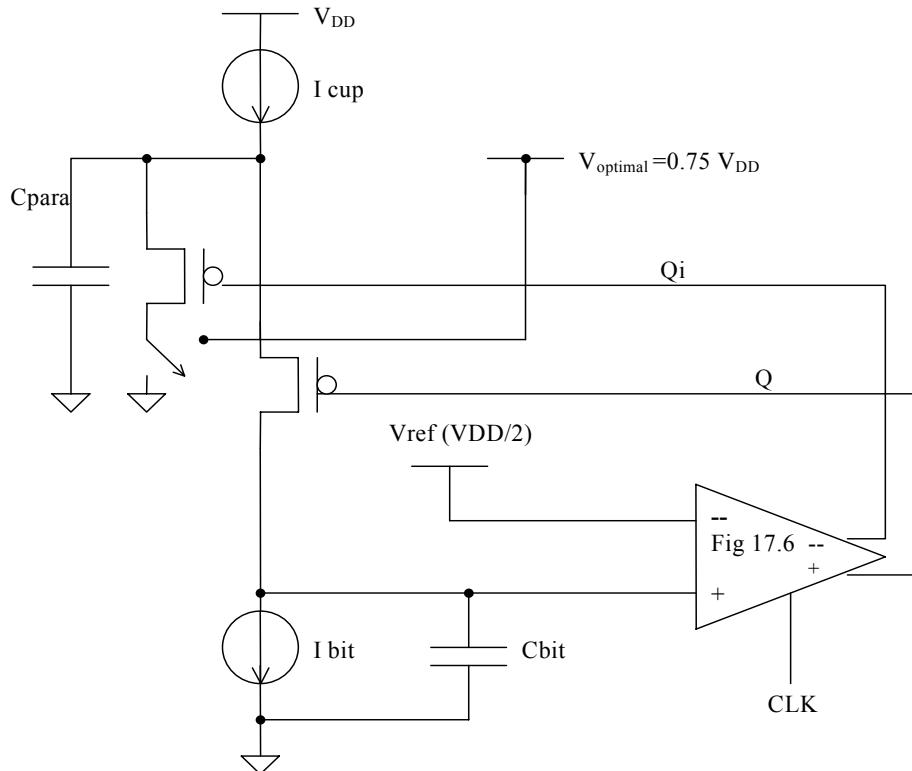
Fig 17-4-2 Alternative design of Current source parasitic Capacitance Effect

Table 17-4-3 SPICE Simulation results of parasitic Capacitance effects

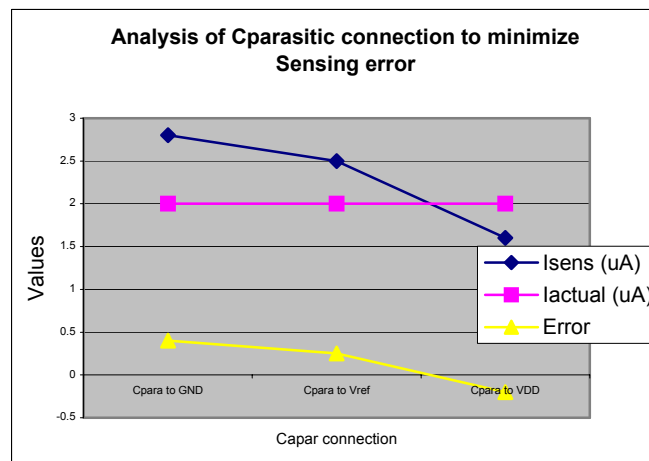|	C_{par} to GND	C_{par} to Vref	C_{par} to VDD
I_{sense} (uA)	2.8	2.5	1.6
I_{actual} (uA)	2	2	2
Error (%)	40%	25%	-20%

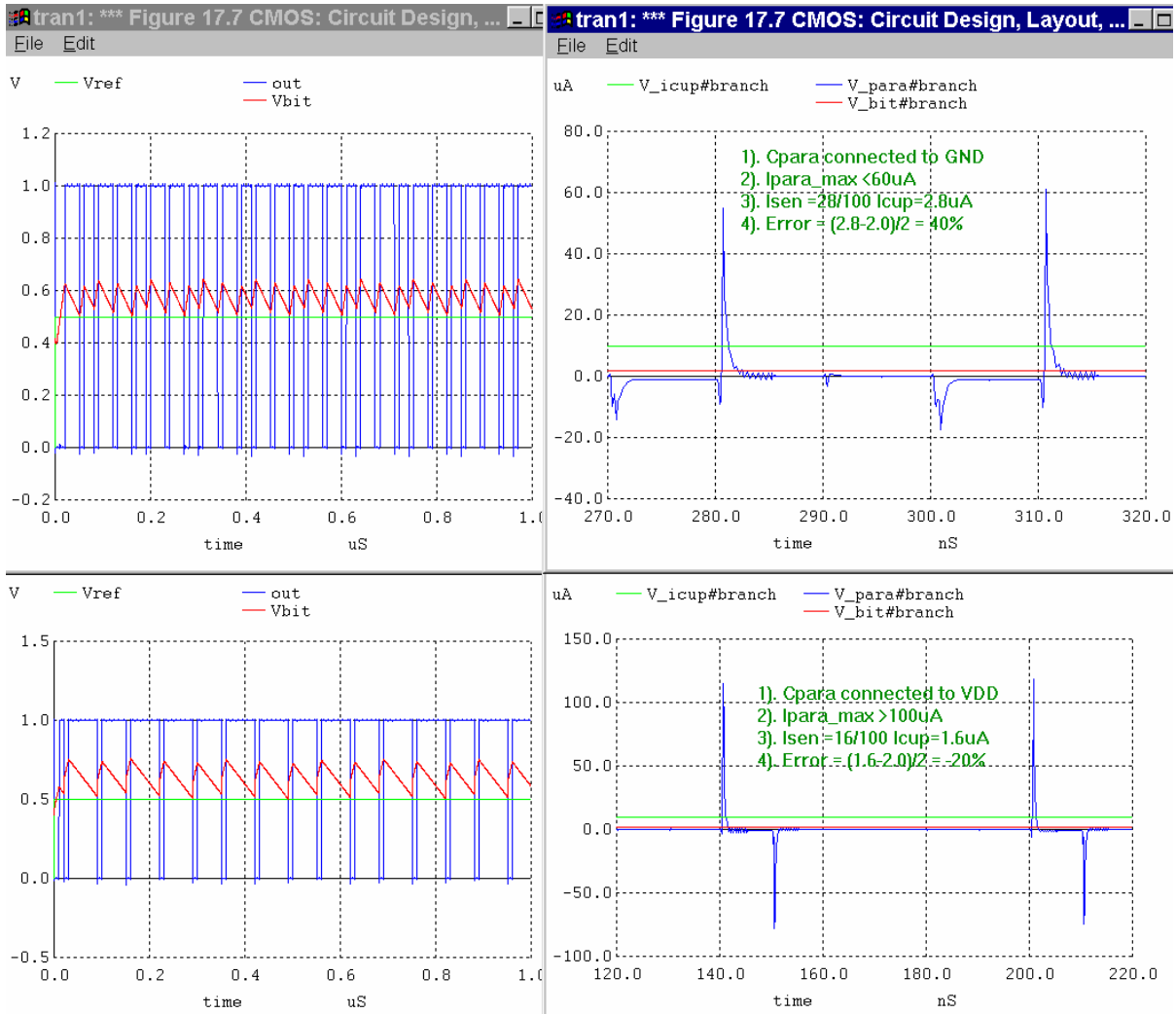Fig 17-4-4 SPICE Simulation parasitic Capacitance (connect GND-Top /VDD-Bottom)
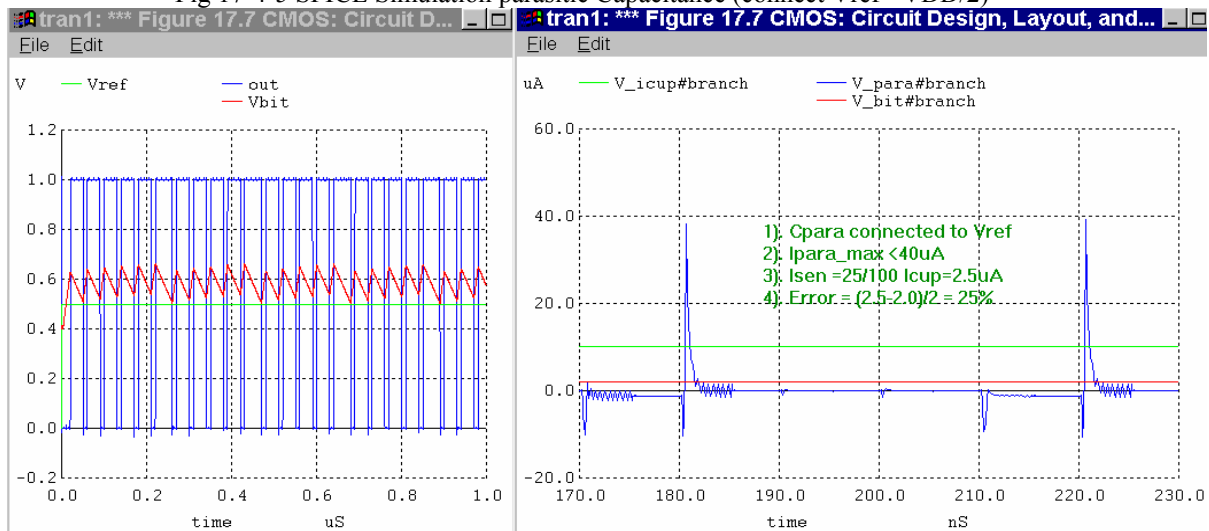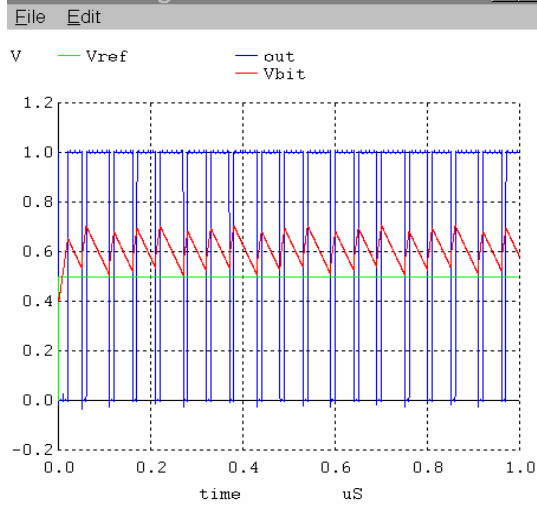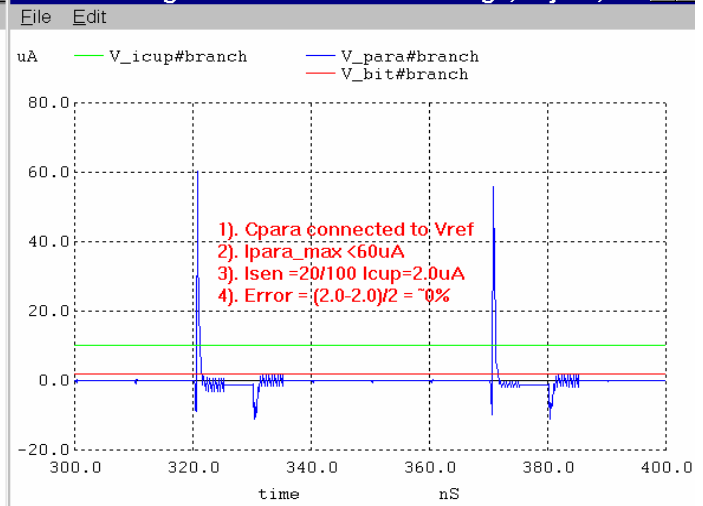
Fig 17-4-5 SPICE Simulation parasitic Capacitance (connect Vref =VDD/2)

Fig 17-4-6 SPICE Simulation parasitic Capacitance (connect {Vref +VDD}/2= 0.75VDD) to eliminate sensing error caused by Cpara from current source

Left window:

tran1: *** Figure 17.7 CMOS: Circuit Des... _ □

File   Edit

V   — Vref   — out
                    — Vbit

Right window:

tran1: *** Figure 17.7 CMOS: Circuit Design, Layout, a... _ □

File   Edit

uA   — V_icup#branch   — V_para#branch
                          — V_bit#branch

1). Cpara connected to Vref
2). Ipara_max <60uA
3). Isen =20/100 Icup=2.0uA
4). Error = (2.0-2.0)/2 = ~0%

Problem 17.5   **Tris Tanadi (ttanadi@hotmail.com)**
Showing, using simulations, that if the output of the comparator swings from VDD to VDD/2 we can
eliminate M4 in Fig. 17.9 and still have $Q_{cup} = C_{cup}*(VDD - V_{REF} - V_{THP})$. Why? Does the amount of
current supply by VDD/2 increase? Could this be a problem?

Answer:
We will compare the operation of circuit from Fig. 17.18 with similar circuit but without M4 plus with the
following extra circuit.
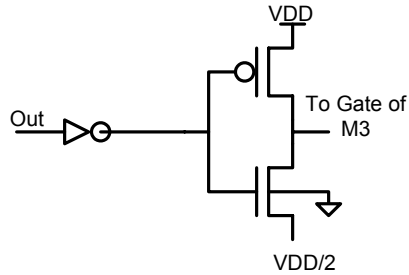
Yes, we will still have $Q_{cup} = C_{cup}*(VDD - V_{REF} - V_{THP})$ because when output of the comparator is
low we will dump the charge from C_{cup} to the bit line. Since the logic low of the comparator is VDD/2
which is equal to VREF then the equation still valid. The next two plots are comparing the result using Fig.
17.18 and the new circuit. The Vbit using both circuits are similar. This means that Qcup between two
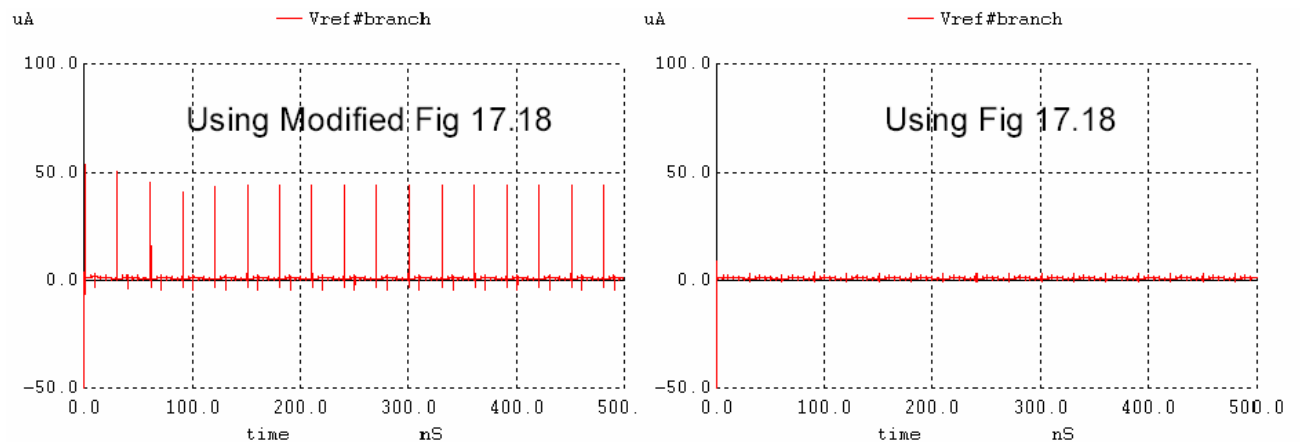circuits are the same too.

Using Fig 17.18
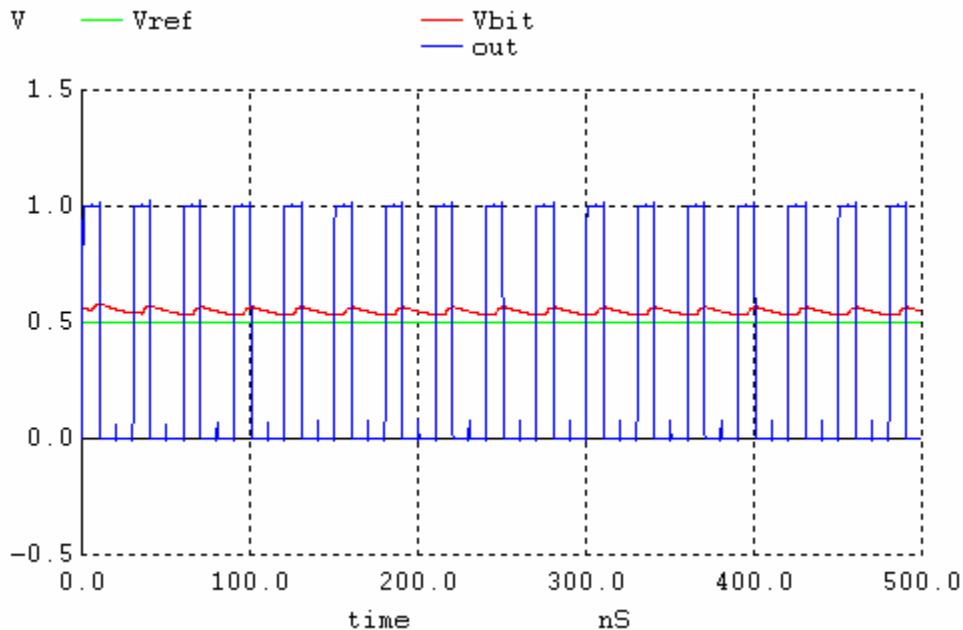
Using new circuit.
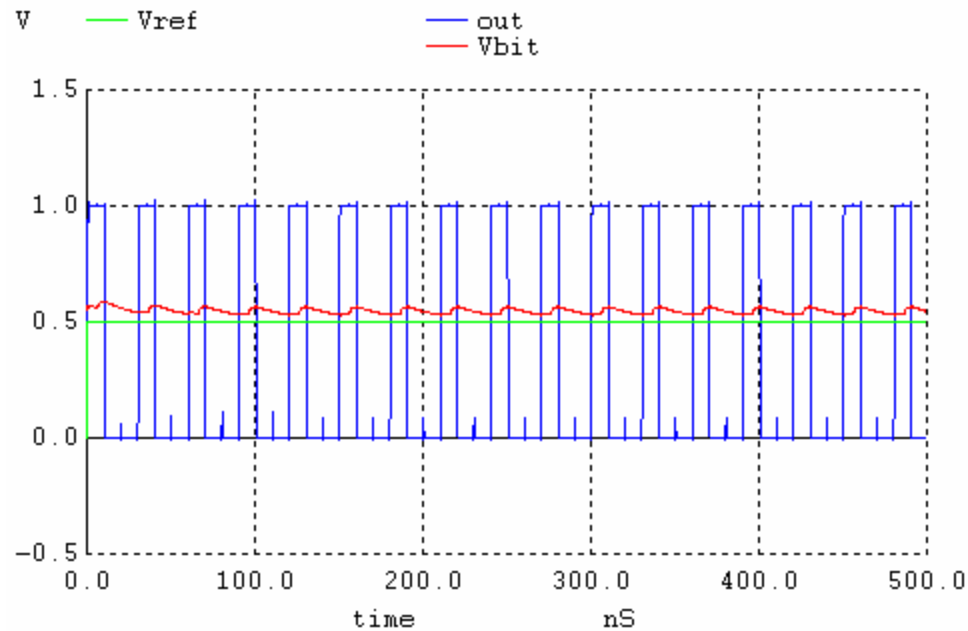
Using the modified Fig 17.19, we will burn more current through VREF because of the extra inverter to change the swing of the comparator output will draw current whenever the output is switched LOW.

The problems of using this circuit are the current increase from VREF and also the extra are required for the extra inverters.

The SPICE source code for the modified circuit:

```
*** Problem 17.5 ***

.control
destroy all
run
let out=Qi
plot Vbit Vref out
```

```
       plot Vref#branch ylimit -10u 100u
       .endc

       .option scale=50n
       .ic V(vbit)=550m
       .tran .25n 500n 0 .25n UIC

       VDD      VDD      0          DC        1
       Vphi1    phi1     0          DC        0         PULSE 1 0 1n 0 0 4n 10n
       Vphi2    phi2     0          DC        0         PULSE 1 0 6n 0 0 4n 10n
       Vclock   clock    0          DC        0         PULSE 0  1 0 0 0 5n 10n
       Vref     Vref     0          DC        0.5

       M1       Vd1      phi1       VDD       VDD       PMOS L=1 W=20
       M2       Vd2      phi2       Vd1       VDD       PMOS L=1 W=20
       M3       Vbit     vx         Vd2       VDD       PMOS L=1 W=20
       Ccup     Vd1      0          100f

       Cbit     Vbit     0          500f
       Rmbit    Vbit     Vref       50k

       * The extra circuit from Fig. 17.18
       X2 Q     Qbar     VDD Inv
       M4       vx       Qbar       Vref      0         NMOS L=1 W=10
       M5       vx       Qbar       VDD       VDD       PMOS L=1 W=20


       X1       VDD      Vbit       Vref      clock     Qi        Q         Comp

       .subckt Comp        VDD      Inp       Inm       clock     Qi        Q
       M1       d1       Outp       db1       0         NMOS L=1 W=10
       M2       d2       Outm       db2       0         NMOS L=1 W=10
       M3       Outm     Outp       VDD       VDD       PMOS L=1 W=20
       M4       Outp     Outm       VDD       VDD       PMOS L=1 W=20

       MS1      Outm     clock      d1        0         NMOS L=1 W=10
       MS2      Outp     clock      d2        0         NMOS L=1 W=10
       MS3      Outm     clock      VDD       VDD       PMOS L=1 W=20
       MS4      OUtp     clock      VDD       VDD       PMOS L=1 W=20

       MB1      db1      Inp        0         0         NMOS L=1 W=10
       MB2      db2      Inm        0         0         NMOS L=1 W=13

       X1       Outp     Q          Qi        VDD       Nand
       X2       Qi       Outm       Q         VDD       Nand

       .ends

       .subckt Nand A B ANANDB VDD
       M1       ANANDB A            d2        0         NMOS L=1 W=10
       M2       d2       B          0         0         NMOS L=1 W=10
       M3       ANANDB A            VDD       VDD       PMOS L=1 W=20
       M4       ANANDB B            VDD       VDD       PMOS L=1 W=20
       .ends

       .subckt Inv In Out VDD
       M1       out      In         0         0         NMOS L=1 W=10
       M2       out      In         VDD       VDD       PMOS L=1 W=20
       .ends
```
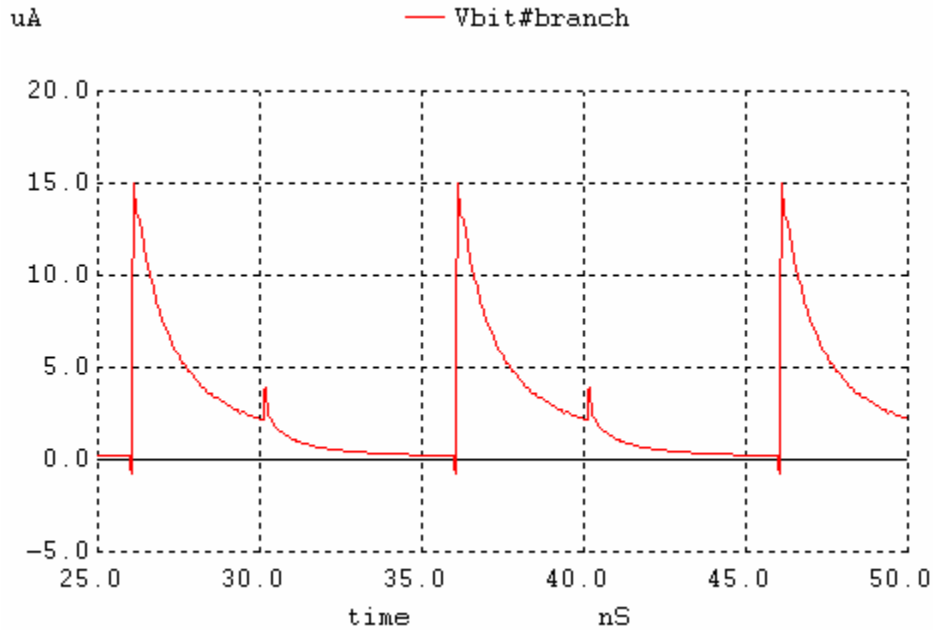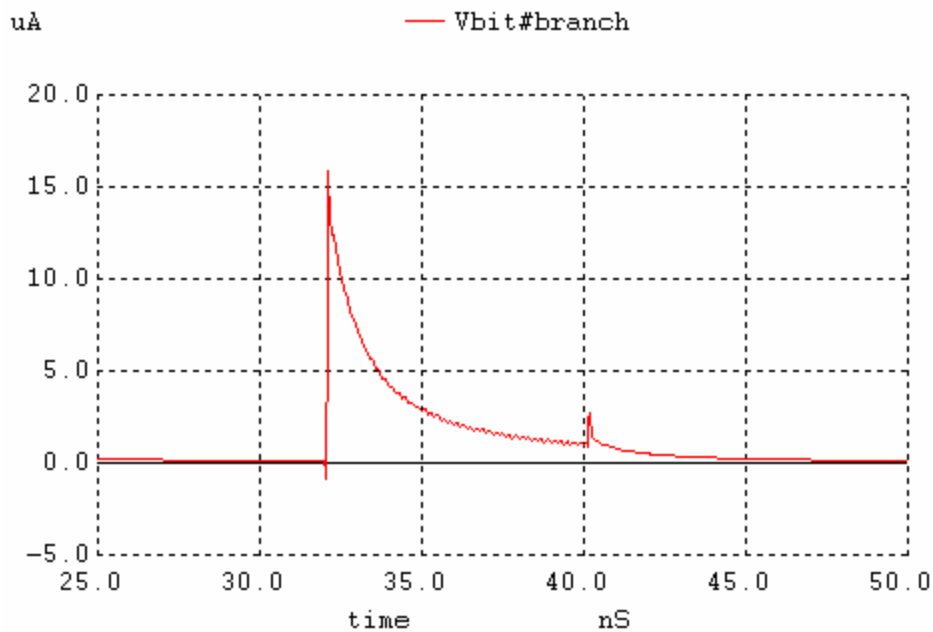
17.6 By reducing the clock frequency, Ccup will be discharged more so the incomplete settling will be more complete. From the simulation results below, when phi2 shut off, Ccup has dumped more charge onto the bit line at lower clock frequency and a wider M4.
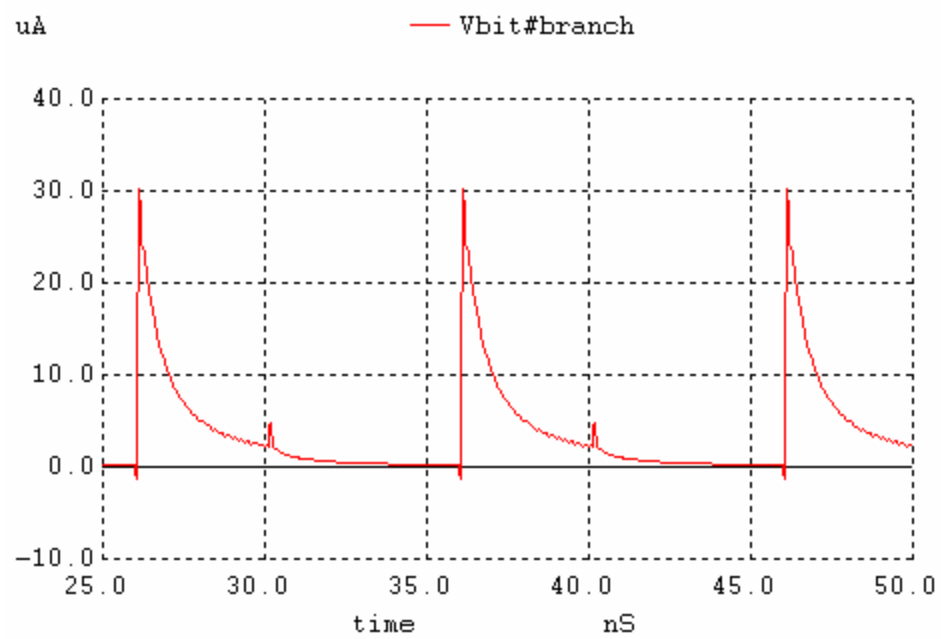
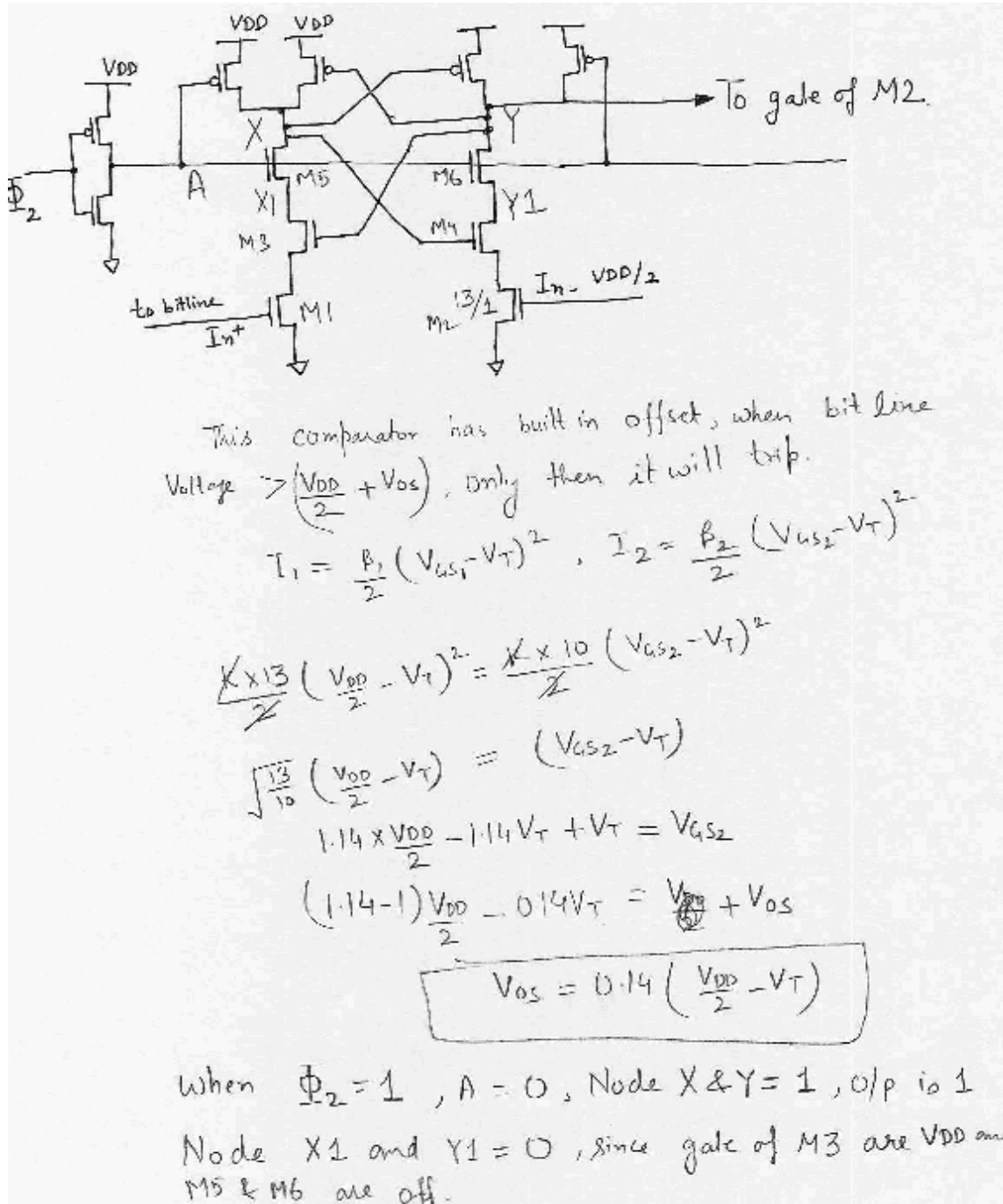Clock is at 10ns, phi2 low time is at 4 ns and M4 is 40 wide:

Clock is at 10ns, phi2 low time is at 4 ns:

M4 with width 100.

Problem 17.7

This comparator has built in offset, when bit line Voltage $> \left(\frac{V_{DD}}{2} + V_{os}\right)$, only then it will trip.

$$I_1 = \frac{\beta_1}{2}\left(V_{GS_1} - V_T\right)^2, \quad I_2 = \frac{\beta_2}{2}\left(V_{GS_2} - V_T\right)^2$$

$$\frac{\cancel{K} \times 13}{\cancel{2}}\left(\frac{V_{DD}}{2} - V_T\right)^2 = \frac{\cancel{K} \times 10}{\cancel{2}}\left(V_{GS_2} - V_T\right)^2$$

$$\sqrt{\frac{13}{10}}\left(\frac{V_{DD}}{2} - V_T\right) = \left(V_{GS_2} - V_T\right)$$

$$1.14 \times \frac{V_{DD}}{2} - 1.14 V_T + V_T = V_{GS_2}$$

$$(1.14 - 1)\frac{V_{DD}}{2} - 0.14 V_T = \frac{V_{DD}}{2} + V_{os}$$

$$\boxed{V_{os} = 0.14\left(\frac{V_{DD}}{2} - V_T\right)}$$

When $\phi_2 = 1$, $A = 0$, Node X & Y = 1, o/p is 1
Node X1 and Y1 = 0, since gate of M3 are VDD and
M5 & M6 are off.

Operation :
        When phi2= 1 , Two upper PMOS transistor will be ON and M5 and M6 will be off , NMOS M3 and M4 has gate at VDD and M1 and M2 has gate at Bit line and VDD/2. Since There is no current in this case because M5 and M6 are off so X1 and Y1 are pulled to gnd.. Both the outputs will be high in this case.
When phi2 = 0 , Sensing operation starts , both outputs are pulled towards low (initially) , but at different rates , If bitline < VDD/2 +Vos then Output Y will go to gnd finally and X will be at VDD and if bitline >

VDD/2 +Vos then output Y will be at VDD but it will glitch (because initially both the outputs are pulled towards gnd).

This glitch may cause Error in Averaging , because when we expect there is no charge transfer from Ccup to Cbit , It can transfer the charge because of the glitch. The simulation below shows the glitch vs. time.
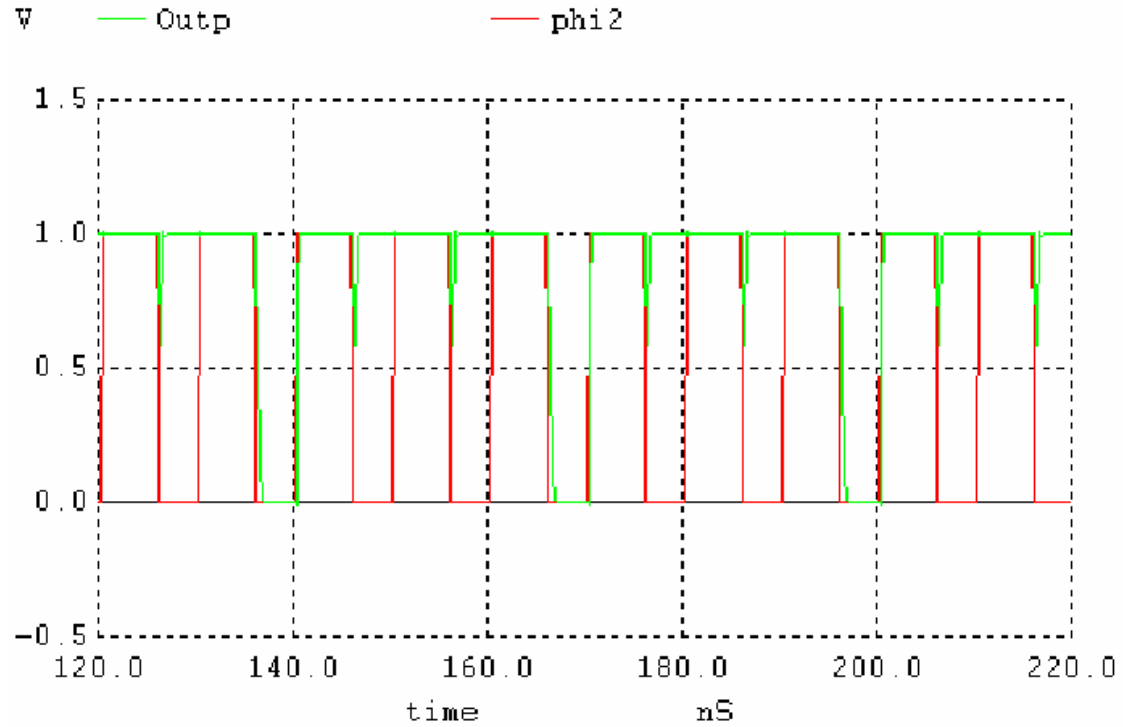
17.8) The following equations and values were chosen for designing DSM circuit that determines the value of resistor that ranges from 100k to 10 MΩ.
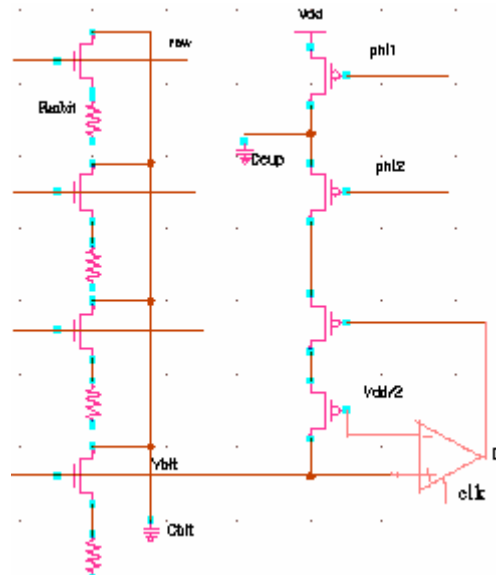
First, the value of Ccup was found by using following equation:

$$Ccup = \frac{Vos.T}{((Vdd-Vthp)*M/N*Rbit))}$$

The Vos value picked as a nominal value of 0.05 V, Vthp= 280 mV and f and where Rbit is picked as 50k.
 By assuming frequency to be 100MHz, we get Ccup to be 90 fF since the offset varies with process, the capacitor is used as 100fF.

Now Rbit = 25k*N/M

The simulation was done by using Ccup less than Cbit(500fF) and using 100k and 10M for Rmbit . The following Rmbit was found by using total clock pulses divided by those clock pulses that go high. The simulation results are shown below. By clocking 100 MHz for 4 us, we get 400 clock pulses.

From sim figure 1

Rmbit = 25k. 400/80 = 125k (the actual value being 100k)

From sim fig 2

Rmbit = 25k. 400/1 = 10M
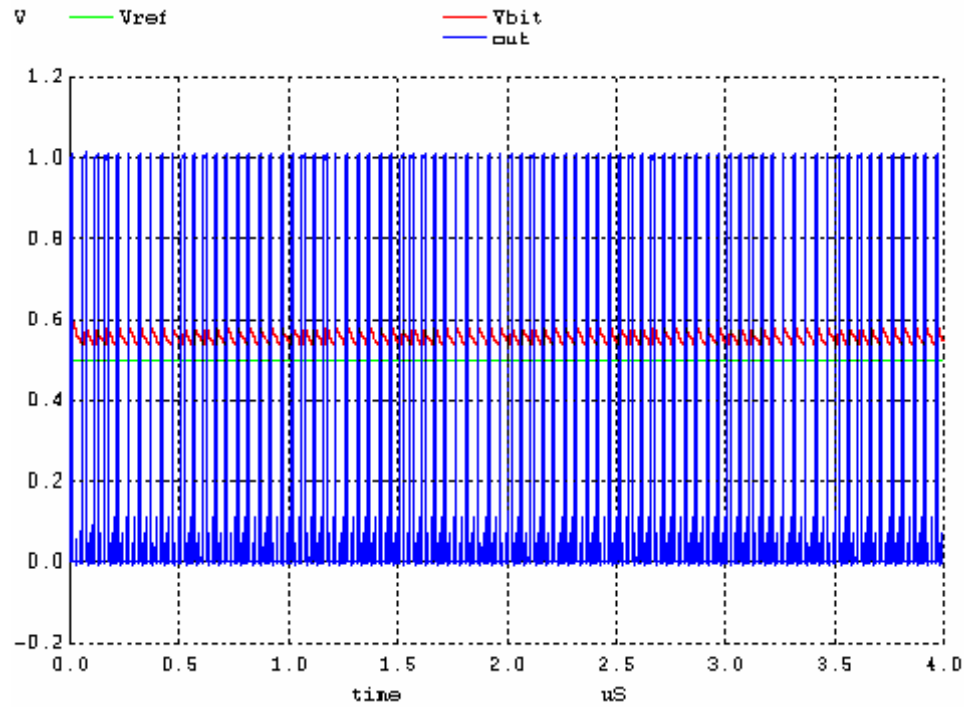
Fig1:For Rmbit = 100K
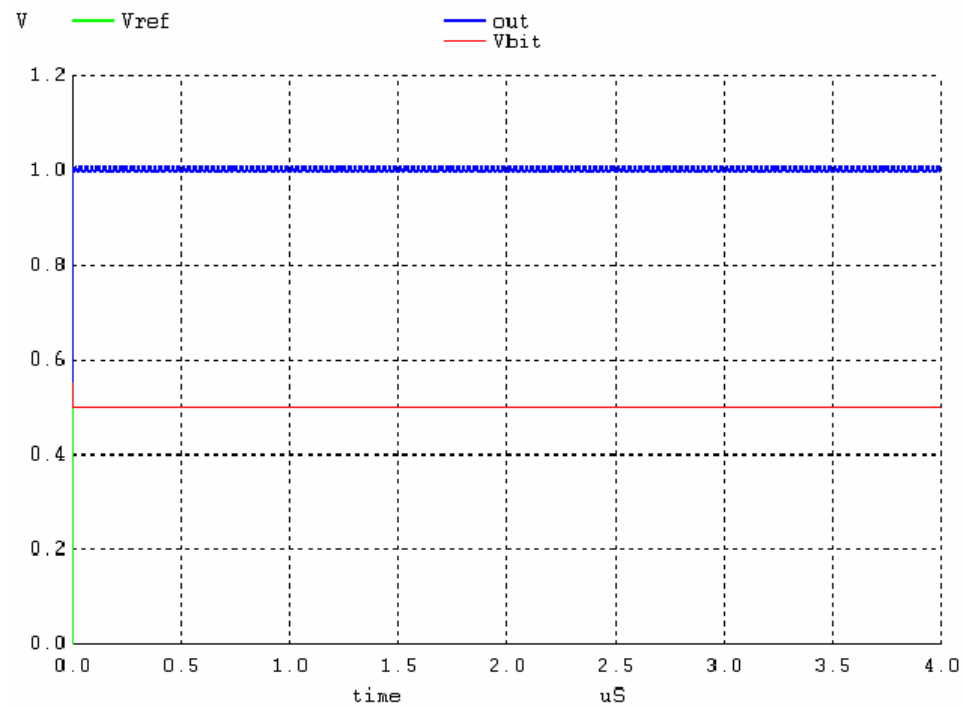
Fig2: For Rmbit= 10M

There will be process variation regarding from the offset voltage and resistance within the MOSFET and threshold voltages that will affect the results. These parameters will affect Ccup since Cbit is always

constant. It will change the clock high pulses (M) thus ultimately giving out the different result. The frequency will also affect the value of Ccup thus changing Rmbit.

Problem 17.9

Suppose, that it is desired to have a noise floor of $100\mu V$ RMS in a CMOS imager. Further suppose the sensing circuit doesn't contribute any noise to the sense (the transformation from the analog column voltage to the digital word). Estimate the size of the hold capacitors used to sample both the reference and intensity signals.

Solution: Referring to Equation 8.24 which is the expression for the RMS noise voltage through a capacitor, famously called the "Kay tee over cee" noise:

$$V_{RMS,noise} = \sqrt{\frac{k \cdot T}{C}}$$

where

k = Boltzmann's constant $= 1.38 * 10^{-23}$ J/K
T = Temperature in Kelvin = 300 K
C = Capacitance in Farads

$$100\mu V = \sqrt{\frac{1.38 * 10^{-23} \cdot 300}{C}}$$

$$\therefore \quad C = 414 fF$$

So the size of the hold capacitors that can be allowed for a noise floor of $100\mu V$ in the imager is $414 fF$.

17.10 - Solution by Eric Booth

Using simulations determine if the linearity of the voltage-to-current converter can be made better by adjuxting the length of the PMOS device seen in Fig 17.28. Why does, or doesn't, the performance get better?

In order to gather data for this problem, I plotted the derivative of the transfer curve of the device using different L & W values. One way of quantifying the linearity is to divide the change in dI/dV by the ideal value of –100nA/V.

For example, the plot below was created with a device of L=1 and W=5. The change in dI/dV over the full range is ~12nA/V or 12%. The linearity is best from 0V to 400mV, so it would be useful to quantify this value as well. For this device it is ~2%
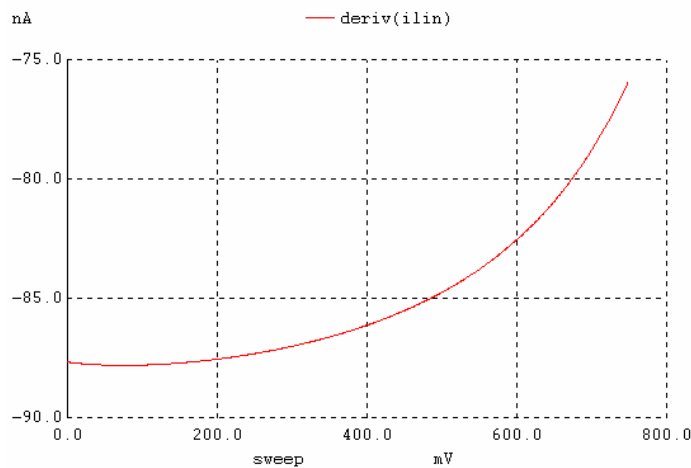
Using this method,

W/L	Linearity (full range)	Linearity (<400mV)
2/1	14%	2%
5/1	12%	2%
10/1	10%	1.5%
20/1	8.5%	1.2%
50/1	7%	1.5%
100/1	6%	3%
20/2	15%	2.5%
20/5	14%	2.5%
20/10	15%	3%
20/20	17%	3%
20/50	20%	4%
20/100	25%	5%

From the table, we can see that as a general rule, increasing W or decreasing L increases the linearity. This is because the linearity of this system requires that the Vgs of the device is a constant, however Id and Vds are changing. A larger β factor ensures that the device will be able to source different currents at different Vds with smaller changes in Vgs.

17.11 Solution

VDD=1V
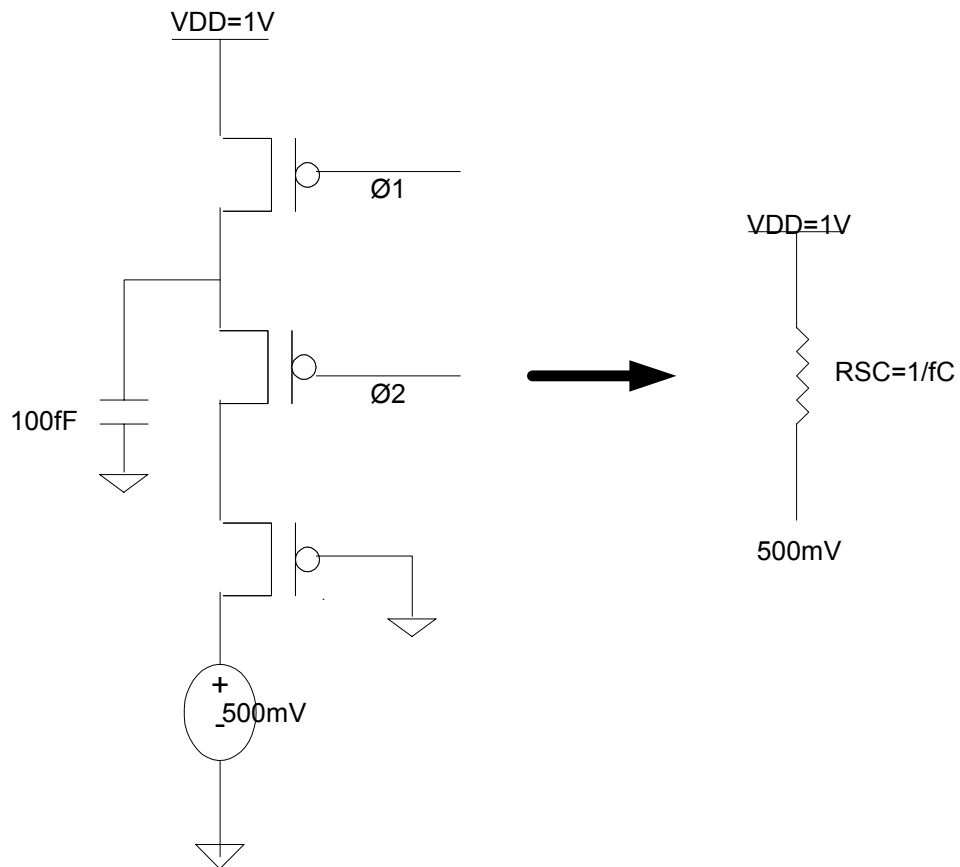
The current that flows through the Resistor R_{SC} is

Iavg=(VDD-0.5)/Rsc

Where Rs=1/fC where f=100Mhz and C=100fF
Therefore Rsc=100K ohms

Therefore Iavg=0.5/100K =5u amps

```
*** Problem 17.11 CMOS: Circuit Design, Layout, and Simulation ***

.control
destroy all
run
plot phi1 phi2+1.25 xlimit 100n 150n
plot Vbit#branch xlimit 15n 20n
plot Vbit#branch
print mean(-vdd#branch)

.endc

.option scale=50n

.tran 100p 500n 10n 100p

VDD    VDD    0    DC    1
Vphi1 phi1  0    DC    0      PULSE 1 0 1n 0 0 4n 10n
```

```
Vphi2 phi2  0     DC    0      PULSE 1 0 6n 0 0 4n 10n
*Add resistors to the sim just to make sure the voltage sources always
have a load.
*Rphi1      phi1  0     1G
*Rphi2      phi2  0     1G
Vbit  Vbit  0     DC    0.5

M1    Vd1   phi1  VDD   VDD    PMOS L=1 W=20
M2    Vd2   phi2  Vd1   vdd    PMOS L=1 W=20
M3    Vbit  0     Vd2   Vdd    PMOS L=1 W=20
Ccup  Vd1   0     100f

Simulation Results
Transient analysis ... 100%
mean(-vdd#branch) = 9.013932e-06
```
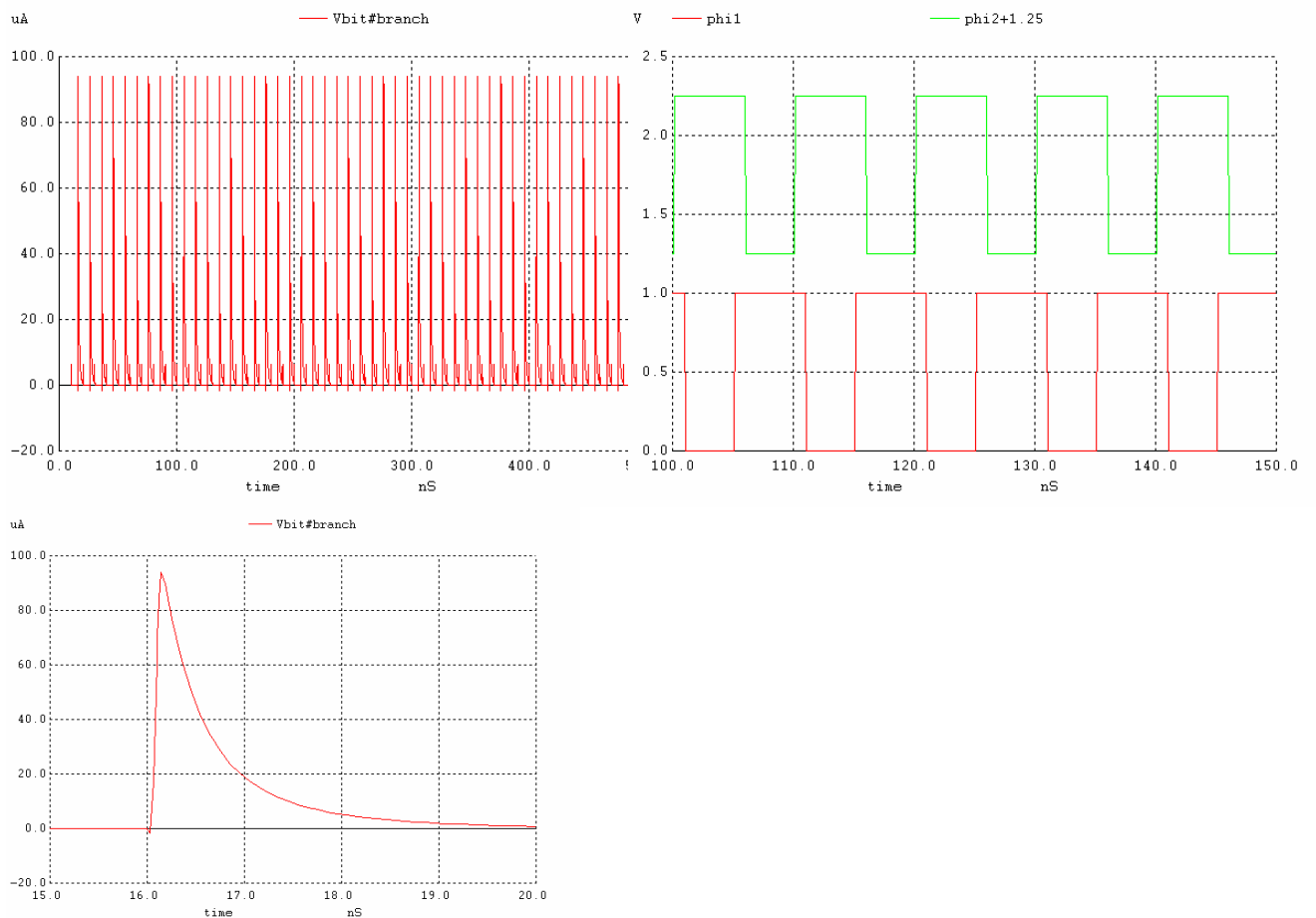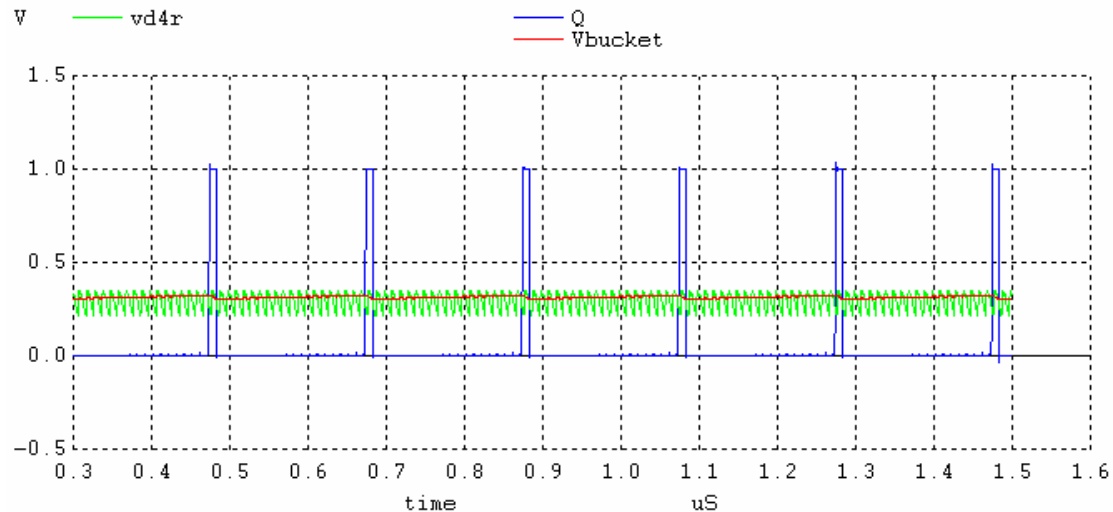
Problem 17.12

What happens to the simulation results seen in Fig. 17.34, if the time step used in the transient simulation is increased to 1ns? How do the nonoverlapping clocks look with this time step?

Lets focus this solution on the results of Figure 17.34(b).
$V_R = 650$ mV
$V_I = 645$ mV

In Figure 17.34(b) the time step is 0.5ns. This results in the following plot of Q vs time;

Examining the plot above, we see that Q goes high 5 times while the counter is enabled (0.5us to 1.5us)

Now if we increase the simulation time step from .5ns to 1ns we get the following plot of Q vs time.
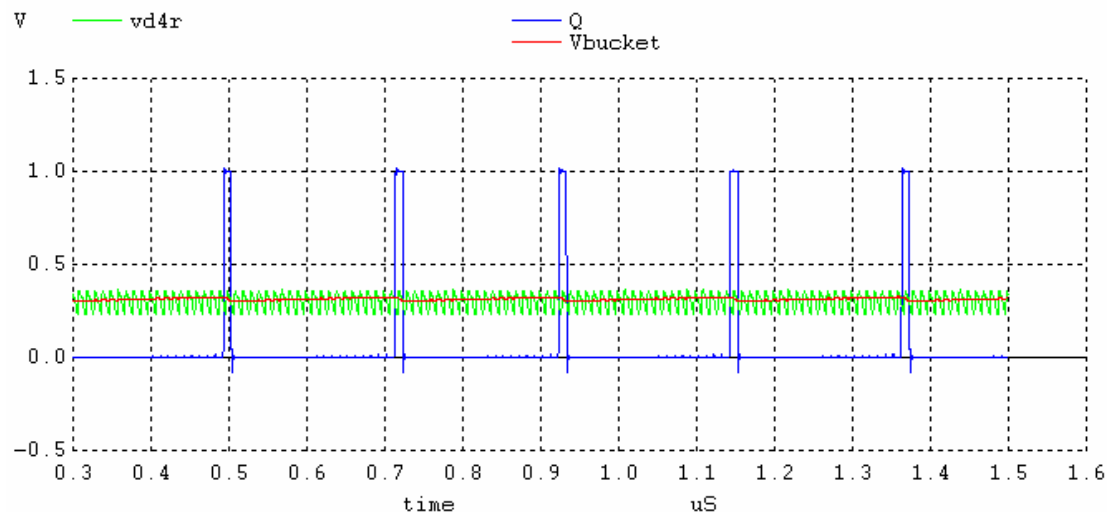
Examining the plot above we see that when the counter is enabled Q goes high 4 times, although when the counter is first enabled, Q is high so depending on the counter the result may be Q high five times. The main point is that Q is going high less frequently. To better understand this, lets take a look at what is happening to the nonoverlapping clocks when the simulation time step is increased (.5ns to 1ns)

time step = 0.5ns

time step = 1ns
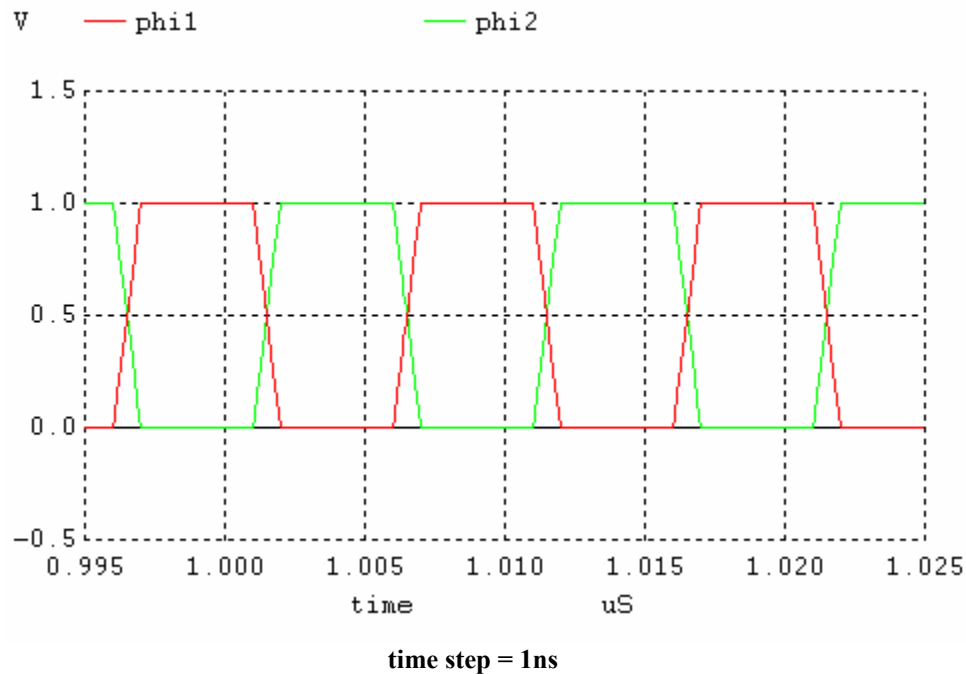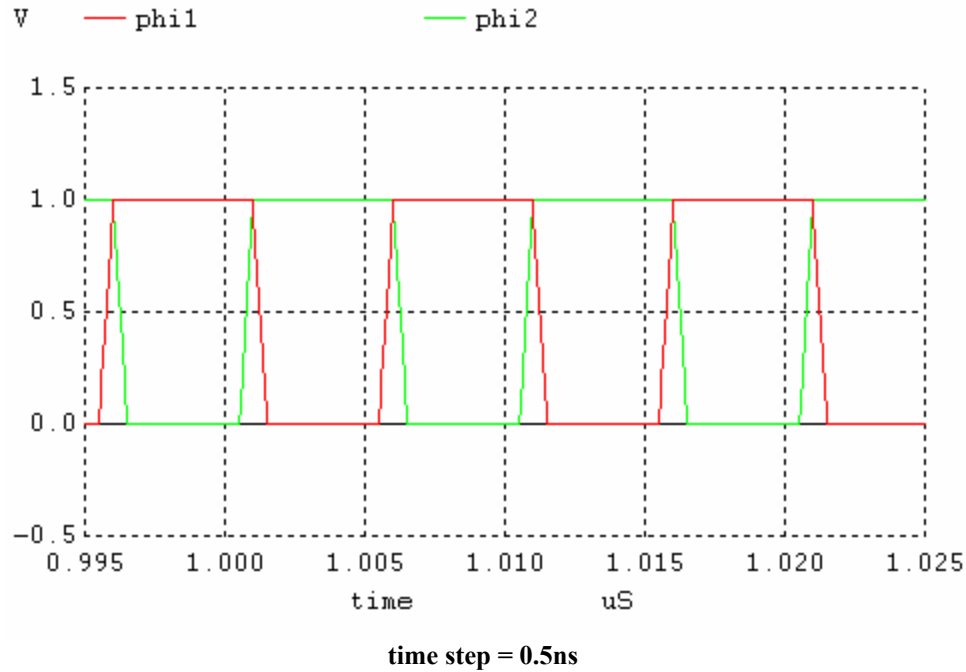
The two plots above show a zoomed in view of **phi1** and **phi2.** In both plots the time period is 10ns with the signal high for 4 ns. The difference between the plots is the rise and fall times of the signals. The rise and fall times default to the simulation time step. So in the top plot we have a rise time = fall time = .5ns. Subtracting the total time period(10ns) by the time high(4ns) and the combined rise and fall times(1ns) leaves 5 ns for the signals to be low. In the second plot we have a rise time = fall time = 1ns. This leaves only 4ns for the signal to be low(10ns-4ns-1ns-1ns).

If we look back at Figure 17.33 we see that **phi1** and **phi2** control the switched capacitors via pmos transistors. Since **phi1** and **phi2 are** low for a less amount of time with the higher time step, less charge will be able to go to the C_{cup} capacitors. This essentially will increase the R_{SC} for each side, which will lower the current that flows through each side.

With a lower current flowing through both sides it takes longer to drain the charge on $C_{bucket.}$. Yes its true that the charge on C_{cup} is also less but in this case the lower current affects the results more than the smaller C_{cup} charge.

Problem 17.13

Figure 1 shows the outputs of the comparator from figure 17.44. As can be seen, the outputs of the comparator do not make full logic levels. They will reach VDD but not 0.

The glitches seen in Figure, will cause switches to turn on, (when they aren't supposed to,) and inadvertently dump some charge. This will affect the resolution of the sense.
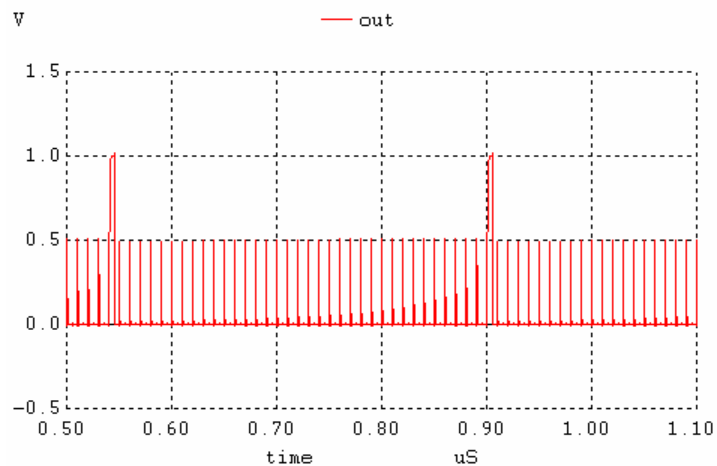

Figure 1.

Adding inverters to the output of the comparator cleans up these glitches (figure 2.). Notice in the netlist, (at the end of this solution,) that the size of the inverter MOSFETS have been adjusted to move the switching point of the inverters to help eliminate the glitches.
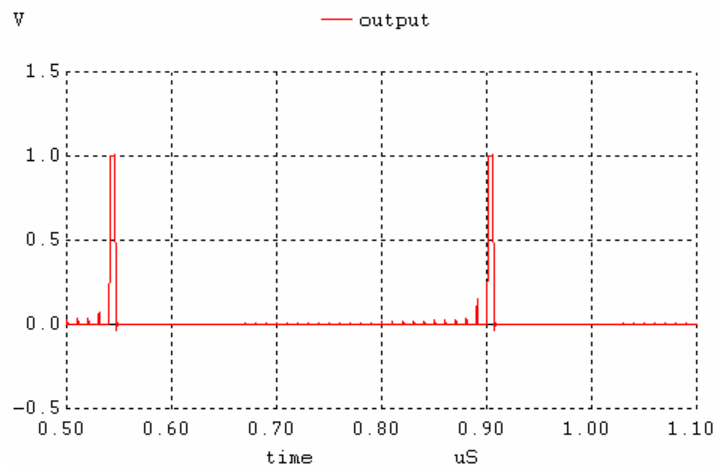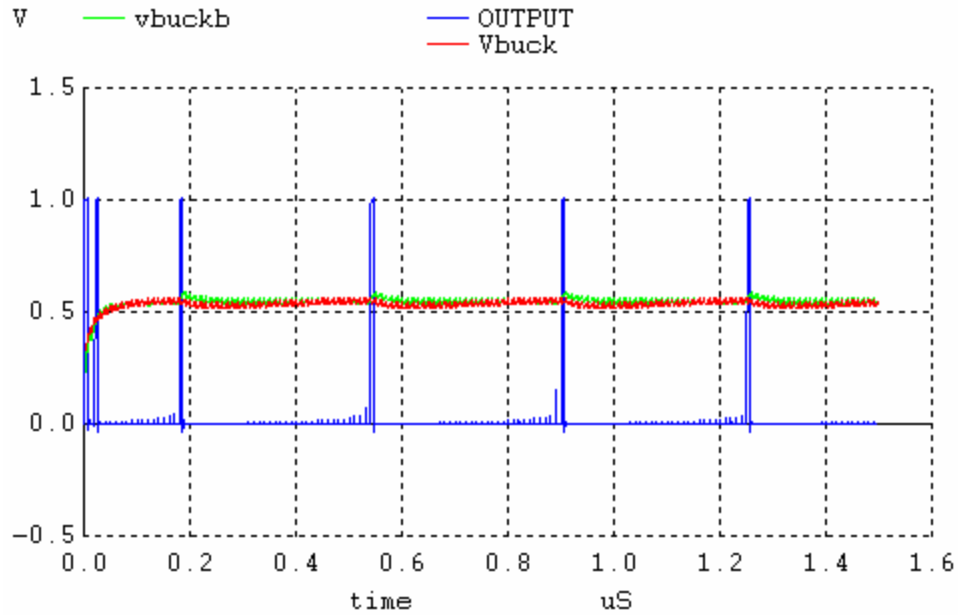

Figure 2.

Figure 17.37a.

The simulation results for figure 17.37a, above show it's comparator making full logic levels, this is because of the SR latch on the outputs it's comparator.

Comparing figures 17.37a through e with figures 17.44a through e, below, we see that:
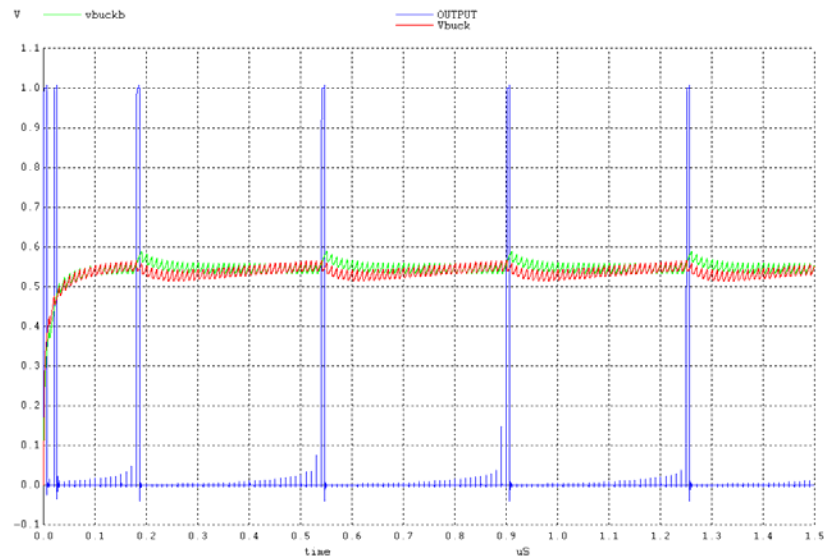

Figure 17.44a

VIshift=640mV-215mV= 425mV, and the sensed value is 435mV*94/100=418mV.
This is compared to 426mV sensed in figure 17.37a.
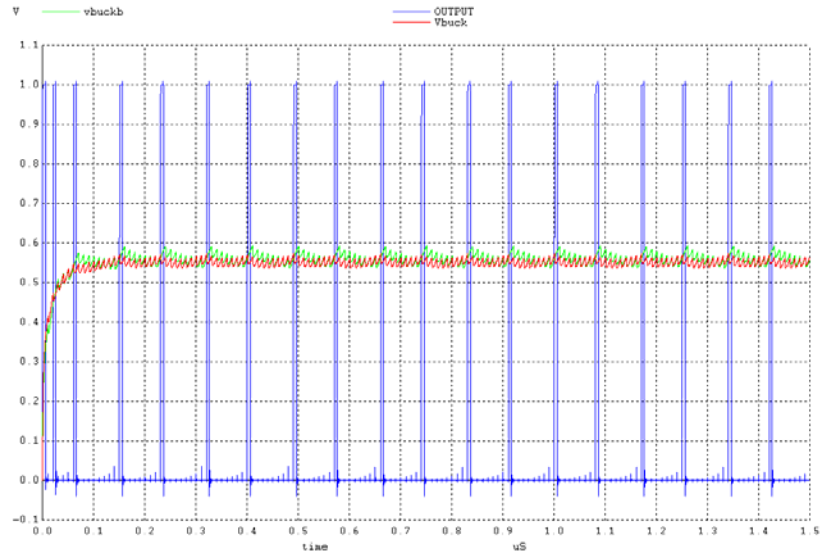
Figure 17.44b

Vishift=600mV-215mV=385mV, and the sensed value is 435mV*89/100=387mV.
Compared to 382mV in figure 17.37b.
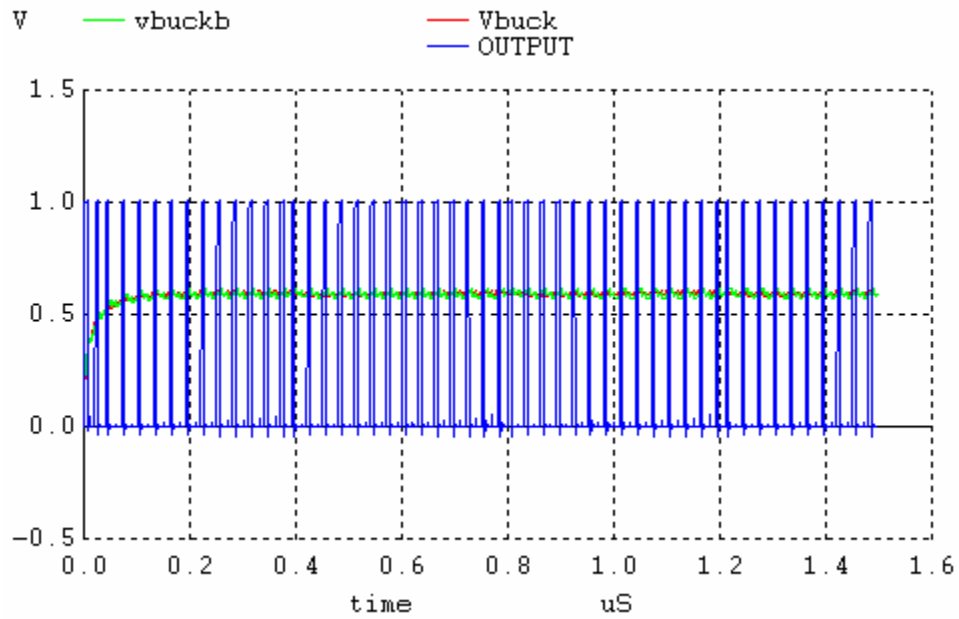
Figure 17.44c

Vishift=500mV-215mV=285mV, and the sensed value is 435mV*66/100=287mV. Compared with 283mV.
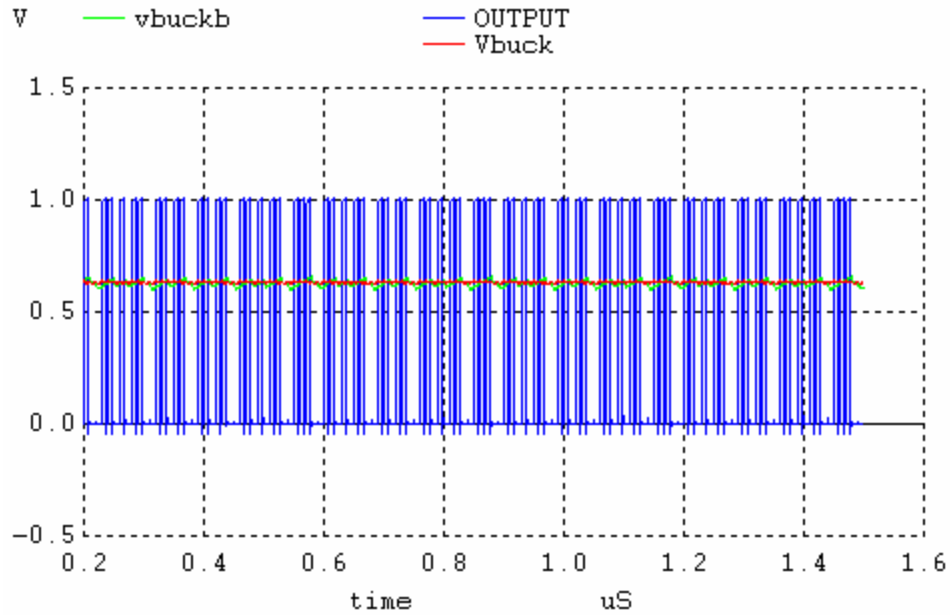
Figure 17.44d

Vishift=400mV-215mV=185mV, and the sensed value is 435mV*44/100=191mV. This is compared to a value of 191mV in figure 17.37d.
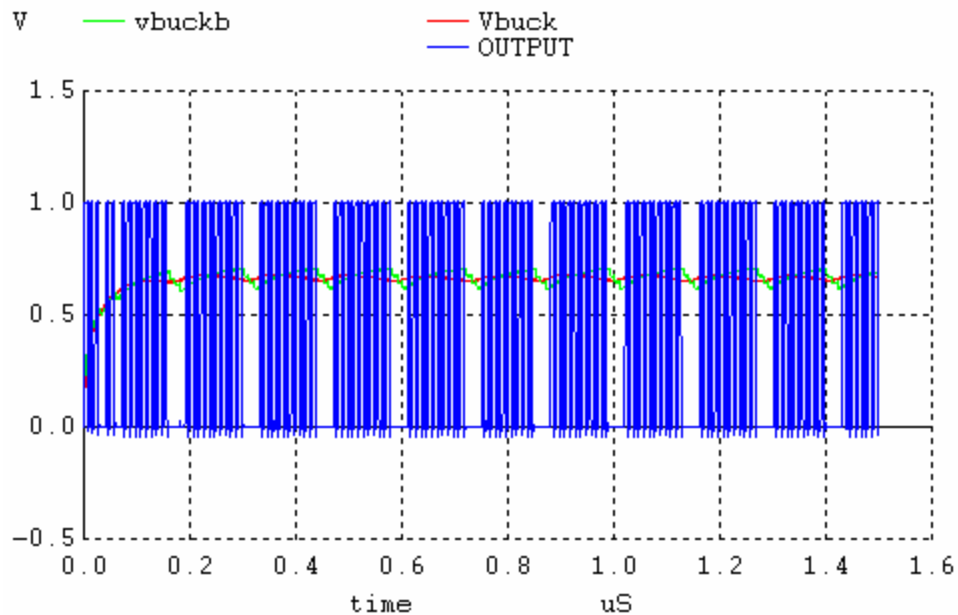
Figure 17.44e

Vishift=300mV-215mV=85mV, and the sensed value is 435mV*22/100=96mV. This is compared to a value of 104 mV.

As can be seen from the figures above, the fact that the comparator doesn't make full logic levels, indicates that our resolution will be off.

*** Figure 17.44 CMOS: Circuit Design, Layout, and Simulation ***

```
.control
destroy all
run
plot Vbuck vbuckb OUTPUT
.endc

.option scale=50n
.tran .25n 1500n 0 .25n UIC

VDD      VDD     0         DC      1
Vphi1    phi1    0         DC      0          PULSE 0 1 1n 0 0 4n 10n
Vphi2    phi2    0         DC      0          PULSE 0 1 6n 0 0 4n 10n

Vblack   Vr      0         DC      650mV
Vinten   Vi      0         DC      300mV

M1r      Vbuckb  vr        vdr2    0          NMOS L=1  W=10
M2r      Vdr2    OUTB      vdr3    0          NMOS L=1  W=10
M3r      Vdr3    phi1      vdr4    0          NMOS L=1  W=10
M4r      Vdr4    phi2      0       0          NMOS L=1  W=10
Mcupr    VDD     vdr4      VDD     VDD        PMOS L=10 W=50

M1i      Vbuck   vi        vdi2    0          NMOS L=1  W=10
M2i      Vdi2    VDD       vdi3    0          NMOS L=1  W=10
M3i      Vdi3    phi1      vdi4    0          NMOS L=1  W=10
M4i      Vdi4    phi2      0       0          NMOS L=1  W=10
Mcupi    VDD     Vdi4      VDD     VDD        PMOS L=10 W=50

M1p      vbuckb  vbuckb    VDD     VDD        PMOS L=10 W=10
M2p      vbuck   Vbuckb    VDD     VDD        PMOS L=10 W=10
Mbuck    0       Vbuck     0       0          NMOS L=10 W=500
Mbuckb   0       Vbuckb    0       0          NMOS L=10 W=500

MCP1     vp1     Vbuck     VDD     VDD        PMOS L=1 W=20
MCP2     vp2     out       vp1     VDD        PMOS L=1 W=20
MCP3     outb    phi2      vp2     VDD        PMOS L=1 W=20
MCP4     vp3     Vbuckb    VDD     VDD        PMOS L=1 W=20
MCP5     vp4     outb      vp3     VDD        PMOS L=1 W=20
MCP6     out     phi2      vp4     VDD        PMOS L=1 W=20

MCN1     outb    phi2      0       0          NMOS L=1 W=10
MCN2     outb    out       0       0          NMOS L=1 W=10
MCN3     out     outb      0       0          NMOS L=1 W=10
MCN4     out     phi2      0       0          NMOS L=1 W=10

MINV1 OUT1_ OUT VDD VDD PMOS L=1 W=2
MINV2 OUT1_ OUT 0  0  NMOS L=1 W=4
MINV3 OUTPUT OUT1_ VDD VDD PMOS L=1 W=2
MINV4 OUTPUT OUT1_ 0  0  NMOS L=1 W=4


* BSIM4 models
```