18.1) Given that we need to design a Schmitt Trigger (refer to Fig 18.3 below for schematic) having a $V_{SPH} = 0.55$ V and $V_{SPL} = 0.35$ V. We start by finding the transconductance ratios for the upper and lower switching point voltages. This is done by using equations (18.4) and (18.6):
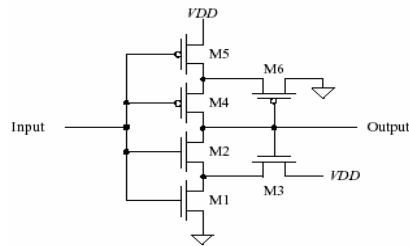

Figure 18.3 Schematic of the Schmitt trigger.

Upper switching point voltage:

$$(18.4) \quad \beta_1/\beta_3 = W_1L_3/W_3L_1 = [(1- 0.55) / (0.55- 0.25)]^2 = 2.25$$

To get the ratio above the following is set for M1 & M3:

$L_1 = L_3 = 2$ and $W_1 = 22.5$, $W_3 = 10$

Lower switching point voltage:

$$(18.6) \quad \beta_5/\beta_6 = W_5L_6/W_6L_5 = [0.35 / (1- 0.35- 0.25)]^2 = .765$$

To get the ratio above the following is set for M5 & M6:

$L_5 = L_6 = 2$ and $W_5 = 15.3$, $W_6 = 20$

For this particular design we set M2 as 70/2 and M4 as 110/2 .

Verified Using Spice: Shown below is the netlist and simulation.
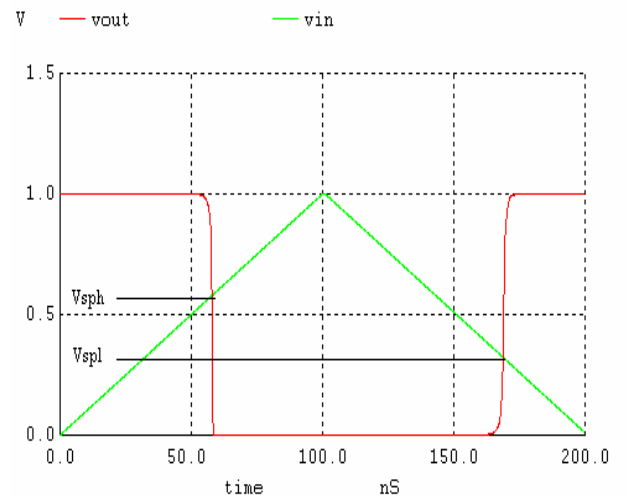
```
.control
destroy all
run
plot vout vin
.endc

.option scale=50n
.tran .1n 200n

VDD    VDD    0      DC      1
Vin    Vin    0      DC      0 PULSE 0 1 0 100n 100n 1n

M1     Vxn    Vin    0       0        NMOS L=2 W=22.5
M2     Vout   Vin    Vxn     0        NMOS L=2 W=70
M3     VDD    Vout   Vxn     0        NMOS L=2 W=10

M4     Vout   Vin    Vxp     VDD      PMOS L=2 W=110
M5     Vxp    Vin    VDD     VDD      PMOS L=2 W=15.3
M6     0      Vout   Vxp     VDD      PMOS L=2 W=20
```
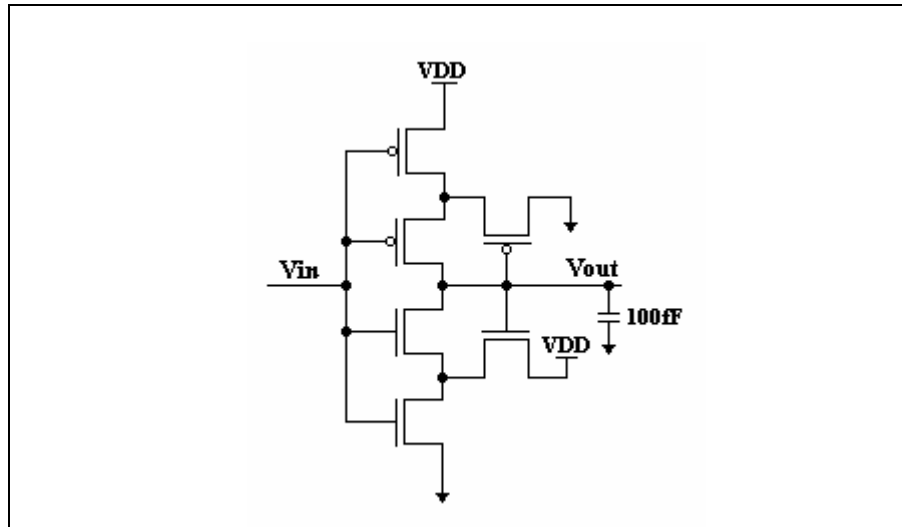
18.2) Estimate t_{phl} and t_{plh} for the Schmitt trigger of Ex.18.1, driving a 100fF load capacitance. Compare your hand calculations to simulation results.

Solution:

Schematic of the Schmitt trigger is shown below:

We can estimate the t_{phl} and t_{plh} by using the following equations:

$t_{phl} = (R_{n1} + R_{n2}) * C_{load}$

$t_{plh} = (R_{p1} + R_{p2}) * C_{load}$

R_n and R_p are found by doing a .op analysis and printing the voltage divided by the current when the MOSFET's are in the saturation region.

We get the following values:
R_n=3.2kΩ and R_p=3.37kΩ

The output capacitance can be found by solving for Cox but since the output capacitance is so much larger in comparison we will use 100fF for the output capacitance in our hand calculations. We get the following values for t_{phl} and t_{plh}.

t_{phl}=**0.6ns**

t_{plh}=**0.7ns**

The simulation of the propagation times is shown below followed by the comparison from hand calculations to simulated values.
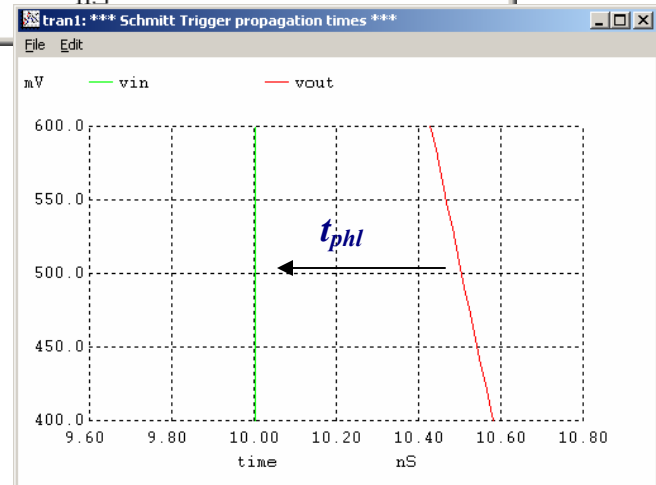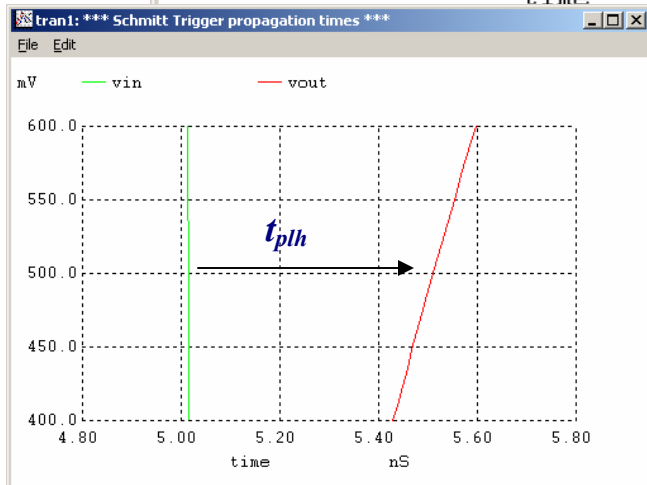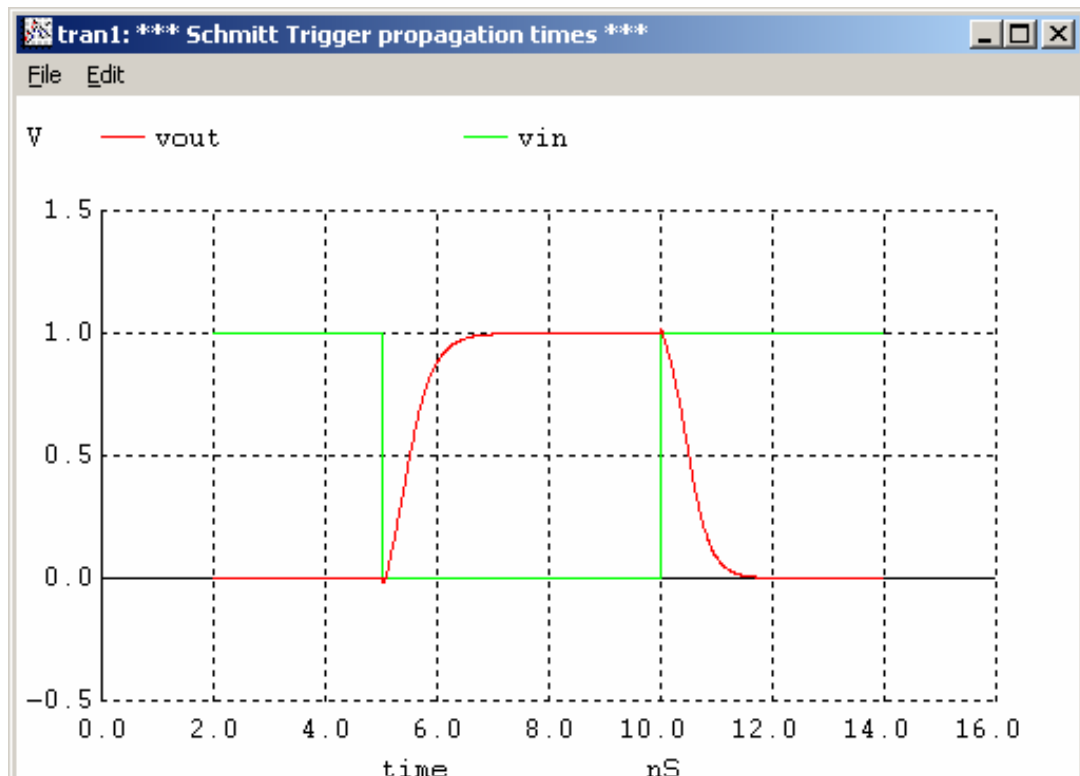
Comparison

Hand calculations: Simulated results:

t_{phl}=**0.6ns** t_{phl}=**0.5ns**

t_{plh}=**0.7ns** t_{plh}=**0.5ns**

Values obtained from the hand calculations are close to the simulated values.

Problem 18.3

Using the Schmitt trigger that was designed in problem #1 I am going to design a Schmitt trigger based oscillator with an output frequency of 10 MHz.
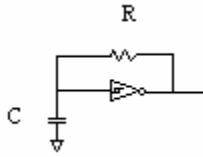
$V_{SPH} = 0.55V$, $V_{SPL} = 0.35V$
$f = 1 / (t_1 + t_2)$
$t_1 = RC \ln (V_{SPH} / V_{SPL})$
$t_1 = .452 RC$
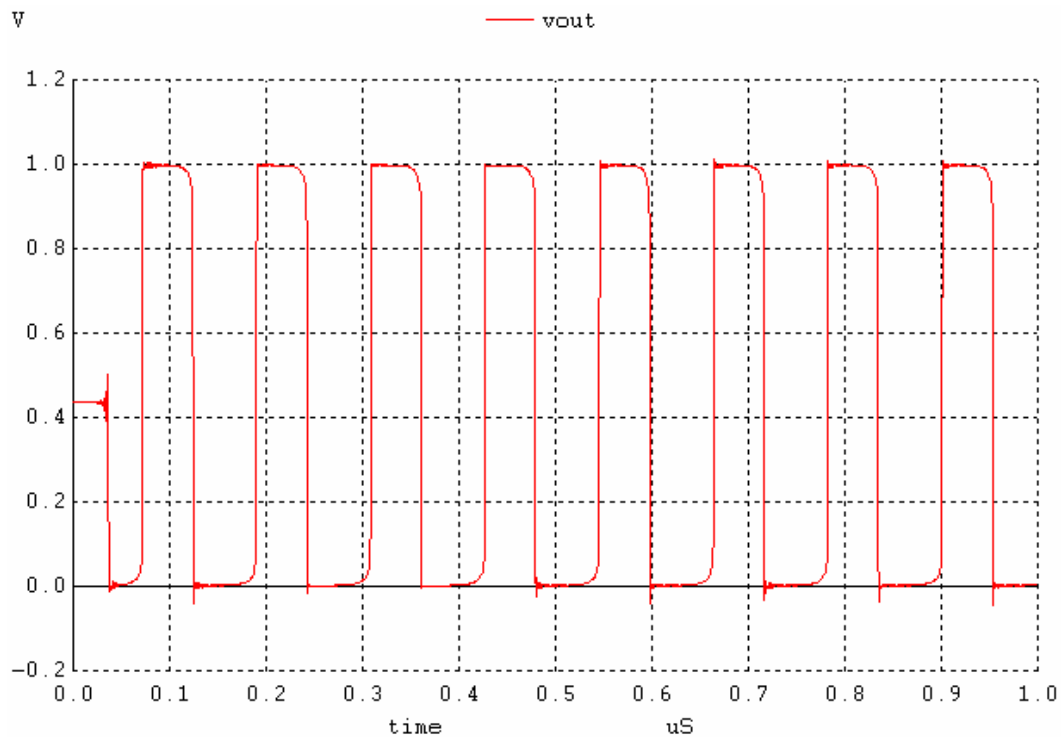$t_2 = RC \ln ((VDD - V_{SPL}) / (VDD - V_{SPH}))$
$t_2 = .368 RC$
$10 \text{ MHz} = 1 / (RC (.368 + .452))$
$RC = 1 / (10MEG * .82)$

Pick R as 1 MEG

$C = 1 / (1 \text{ MEG } 10 \text{ MEG } * .82) = 122fF$

The actual frequency is around 9 MHz.

Net List:

*** Problem 18.3 CMOS: Circuit Design, Layout, and Simulation ***

```
.control
destroy all
run
plot vout
.endc

.option scale=50n
.tran 1n 1u

VDD   VDD   0        DC     1
C1    Vin   0        122fF
R1    Vin   Vout   1MEG

M1    Vxn   Vin    0      0      NMOS L=1 W=22.5
M2    Vout  Vin    Vxn    0      NMOS L=1 W=10
M3    VDD   Vout   Vxn    0      NMOS L=1 W=10

M4    Vout  Vin    Vxp    VDD   PMOS L=1 W=20
M5    Vxp   Vin    VDD    VDD   PMOS L=1 W=15.3
M6    0     Vout   Vxp    VDD   PMOS L=1 W=20
```
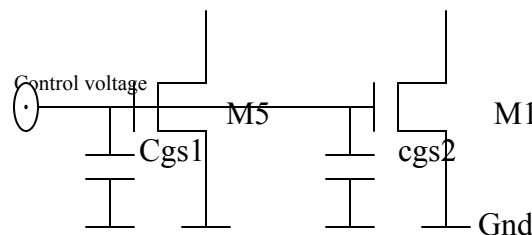
Prob 18.4   Estimate the total input capacitance on the control voltage input for the VCO shown in fig 18.8

Ans:

The M1 and M5 MOSFET's are connected to the control voltage. So mainly the input capacitance on the control voltage is equal to the addition of all the capacitances are associated with the control voltage node.

The gate oxide capacitances of M1 and M5 are the main contributors to the input capacitance at control voltage.

The simplified circuit from fig 18.8 concerning to the input capacitance at the control voltage terminal can be drawn as follows:

Assuming the NMOS transistors are 10/1,with CN20 process:

Cgs1= 2/3 Cox' * W.l= 2/3*800 aF/um2 **10***1 um2
=5.33fF

Cgs2= 2/3 Cox' * W.l= 2/3*800 aF/um2 **10***1 um2
=5.33fF

So the total input capacitance at the control voltage terminal =
Cgs1 +Cgs2 = 5.33*2=10.66fF +2*(CGDO*W)
This estimation is under the consideration that the transistors are in saturation. Otherwise, the cap will be just the addition of the gate ox caps = (Cox'1+Cox'5)*W*l=16.00fF

Problem 18.5

Design an astable multivibrator with an output oscillation frequency of 20MHz.

The block diagram looks like the figure below
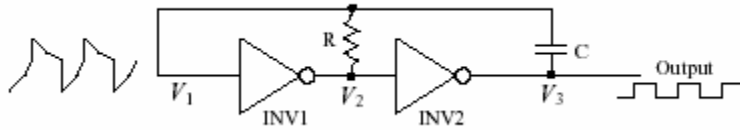
Text book Figure 18.11 Astable multivibrator

Using equation 18.21 $f_{osc} = 1/(2.2\ RC) = 20$MHz to get RC = 22.7ns. We choose 500fF for the capacitor and 45k for the resistor. The simulation results are showed in Figure P18.5 (a) and Figure P18.5 (b) below.
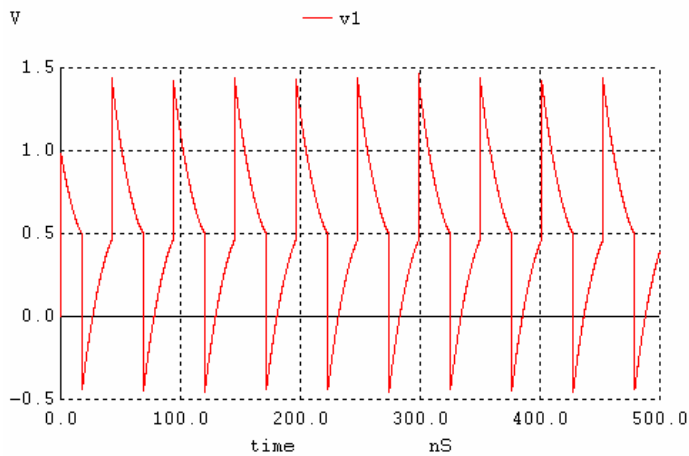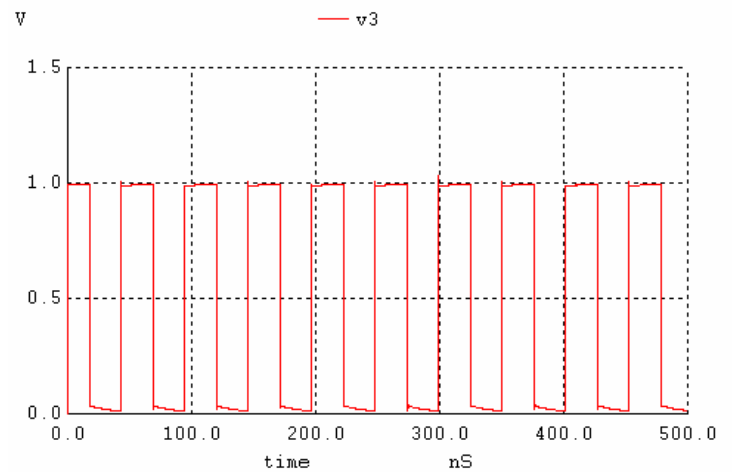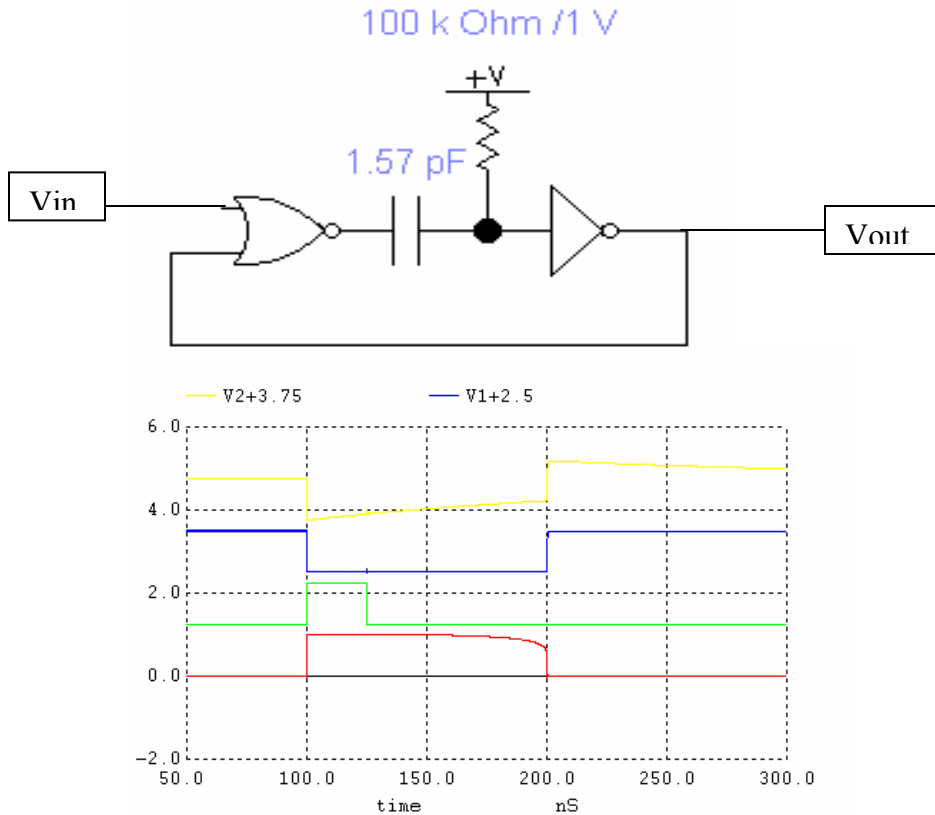

Figure P18.5 (a) Signal at V1

Figure P18.5 (b) 20MHz output (signal at V3)

Netlist

VDD	VDD	0	DC	1	
R1	V1	V2	45k		
C1	V1	V3	500f		
M1	v2	v1	vdd	Vdd	PMOS L=1 W=20
M2	v2	v1	0	0	NMOS L=1 W=10
M3	v3	v2	vdd	Vdd	PMOS L=1 W=60
M4	v3	v2	0	0	NMOS L=1 W=10

Kevin Berkenmeier
Problem 18.6

t=RC ln VDD/(VDD – Vsp) = RC ln (2) = .693RC
t=100ns = .693RC
RC = 1.443 x10-7 (s)   R = 100k C = 1.443pf
(C used = 1.57pf to acquire 100ns pulse through simulation)

*** Figure 18.13 CMOS: Circuit Design, Layout, and Simulation ***

.control
destroy all
run
plot V3 V1+1.25 Vin+2.5 V2+3.75

.endc

.option scale=50n
.tran .1n 500n uic

VDD	**VDD**	**0**	**DC**	**1**
Vin	**Vin**	**0**	**DC**	**0 PULSE 0 1 100n 0.1n 0.1n 25n 1000n**
X1	**VDD**	**V2**	**V3**	**inverter**
Cl	**V1**	**V2**	**1.57p**	
R1	**VDD**	**V2**	**100k**	

M6	Vd6	V3	VDD	VDD	PMOS L=1 W=10
M5	V1	Vin	Vd6	VDD	PMOS L=1 W=10
M4	V1	Vin	0	0	NMOS L=1 W=10
M3	V1	V3	0	0	NMOS L=1 W=10
.subckt inverter VDD A Ai					
M1	Ai	A	0	0	NMOS L=1 W=10
M2	Ai	A	VDD	VDD	PMOS L=1 W=20
.ends					

If the resistor and capacitor are bonded out, the ESD diodes will limit the voltage on the output of the NOR (V1), and input to the inverter, (V2). The voltages cannot go over or under the power supply voltages; you do not want to turn on the ESD clamps. The ESD clamps will have a slow recovery.

The time it takes V2 to decay back down to Vdd limits the rate at which the one-shot can be retriggered. Also note that the trigger input can be longer than the output pulse width. Longer output pulse widths may cause V2 to go as high as 2*Vdd as well as limit the maximum trigger rate.

———

Problem 18.7
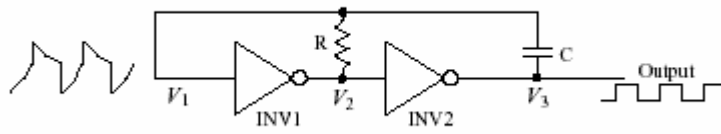
R = 45k and C = 100fF is chosen using equation (18.21) in order to generate a 100MHz square wave output.

Here is the simulation result.
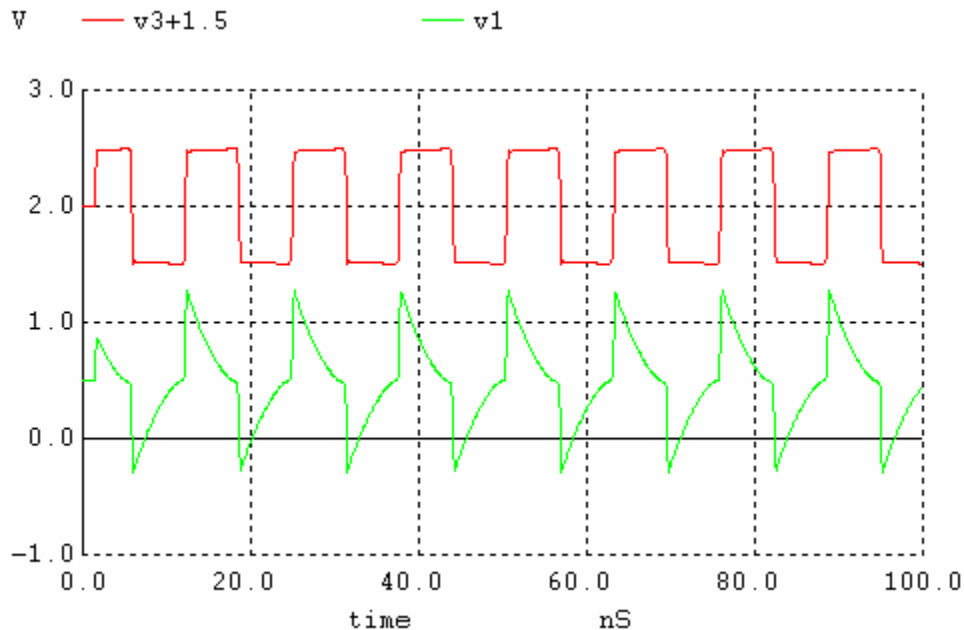

Process shifts in the resistor and capacitor will affect the oscillation frequency since the oscillation frequency is a function of RC. To avoid these possible changes in RC during the process, the resistor and capacitor can be bonded outside of the pads. Whether the ESD diodes affect the circuit's operation depends on the forward bias voltage on the diodes. V1 swing from -1.30V to 1.30V (see above plot). If the ESD diodes have a forward bias voltage 0.7V, it will not affect the circuit's operation because V1 is allowed to swing from −1.7 to 1.7V without turning on the ESD diode.

PROBLEM 18.8)

To simulate the operation of the buffer seen in figure 18.23 driving a load capacitance of 100fF and plot the propagation delays against the Vinp input signal amplitude when Vinm is 250,500 and 700mV (Vinp is centered around Vinm)
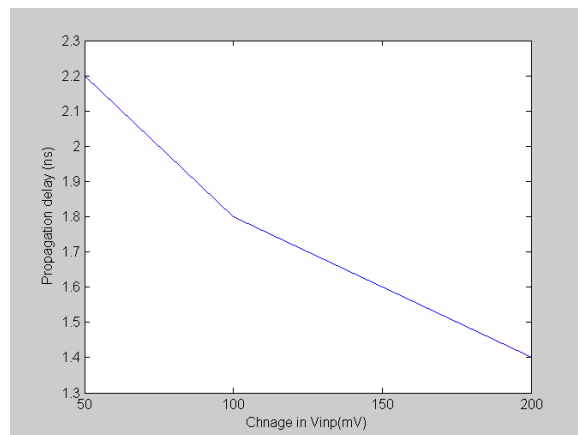
The simulation results of the buffer seen in figure are shown below.
From simulations we can see that the propagation delay decreases for increasing in change in Vinp. The circuit dissipation in the circuit is also shown in the figure
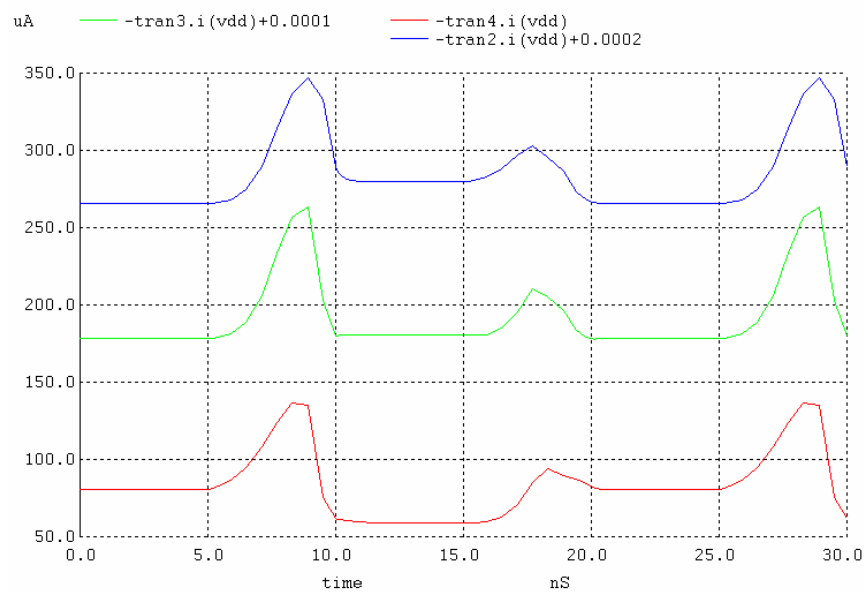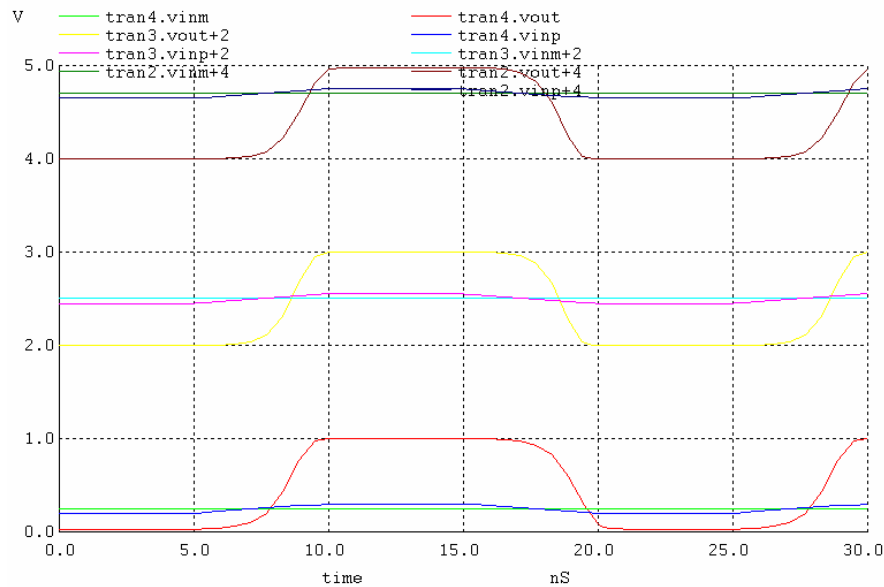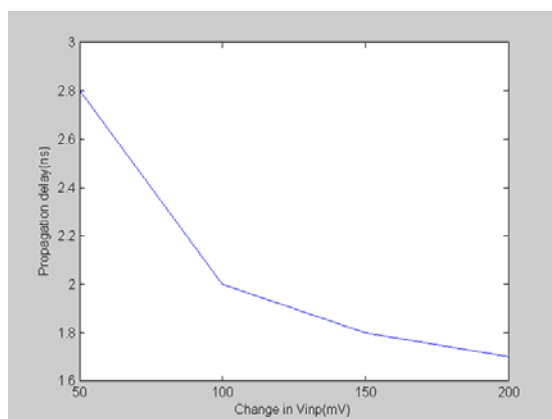
Plot of propagation delays vs. change in Vinp:
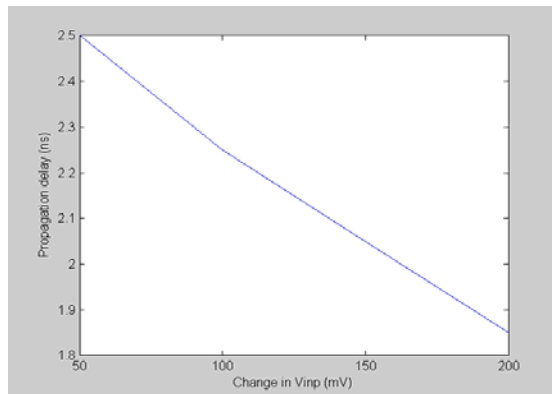
Vinm=250mV

Vinm=500mV

Vinm=700mV

18.11. Comments to the DC restore circuit in Fig. 18.28.
Issue 1: Limitations when long stream of "1" or "0" inputted.

As shown in following sim result, if we have a long "0" ("1"), The output of the buffer will be incorrect. The internal average signal has a big dip that needs some time to recover. This causes the first several bits following the long "0" string has incorrect output.
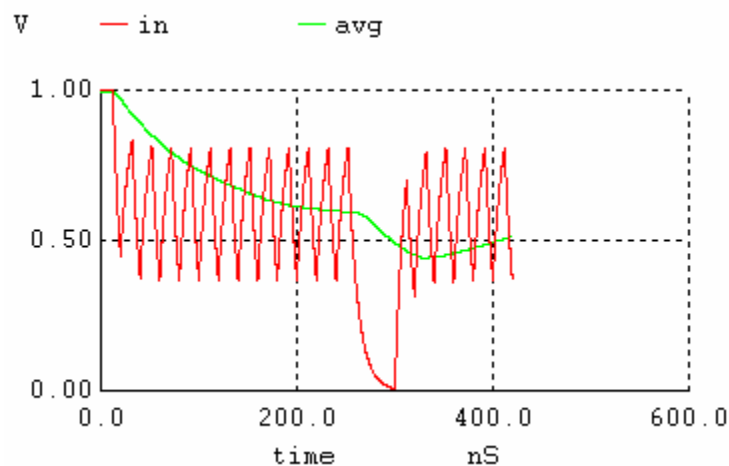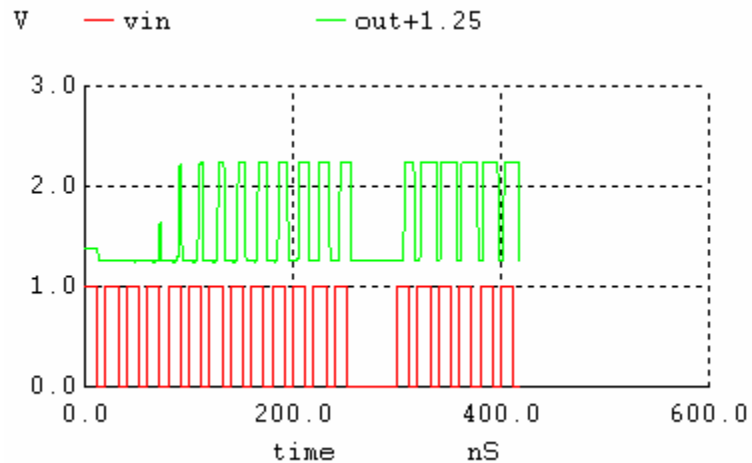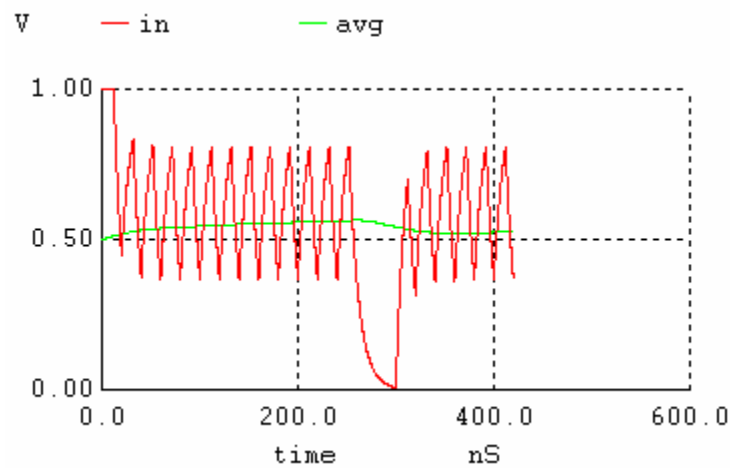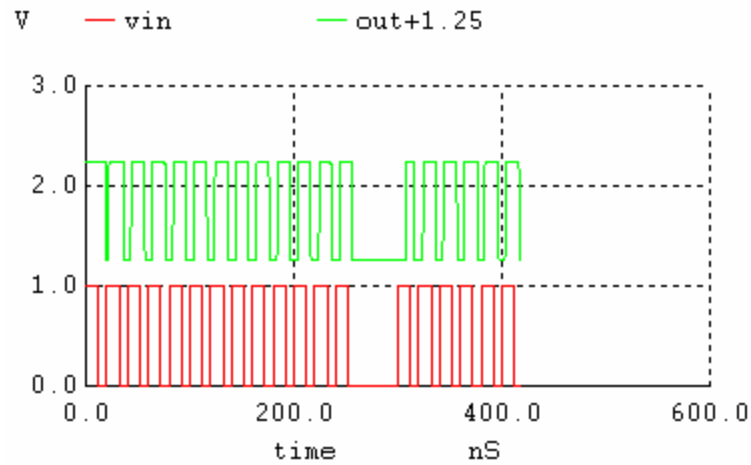

Solution:
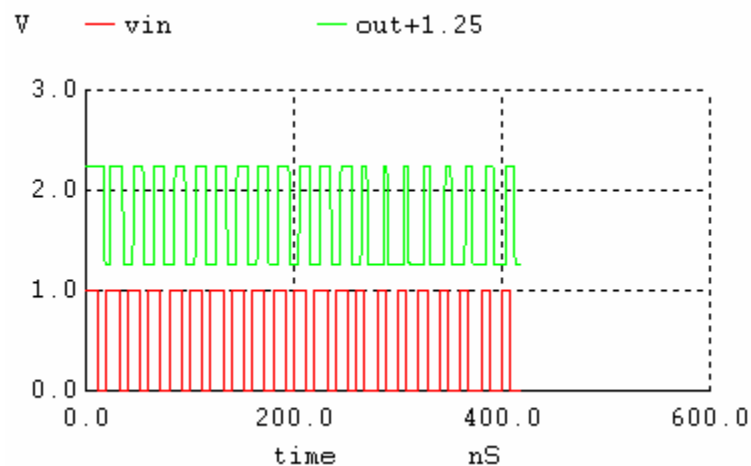>   Increase the RC time constant of the DC generation circuit.
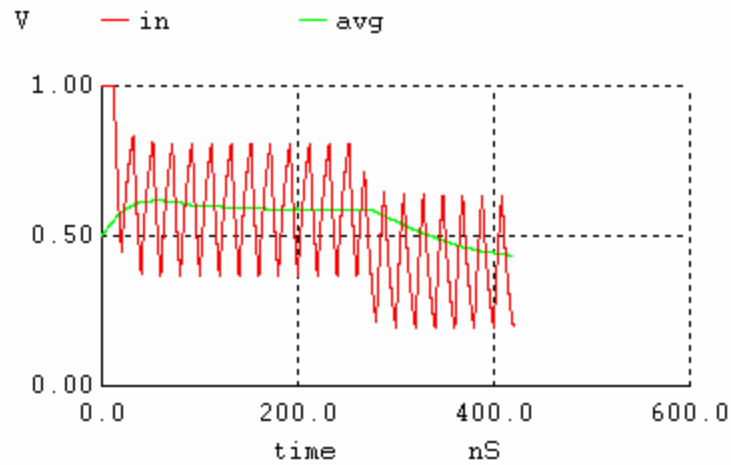>   The following sim shows the result if we increase Cavg from 1pf to 5pf
>   We get much better output.

## Issue 2: **Limitations when input data suddenly changes.**

As shown in following sim result, if the input data changes, the DC generation circuit needs some time to generate the correct average voltage. Thus, the first several bits after input data changes will suffer from the incorrect average voltage

Solution:

Decrease the RC time constant of the DC generation circuit.
The following sim shows the effect if remove the 1P Cavg
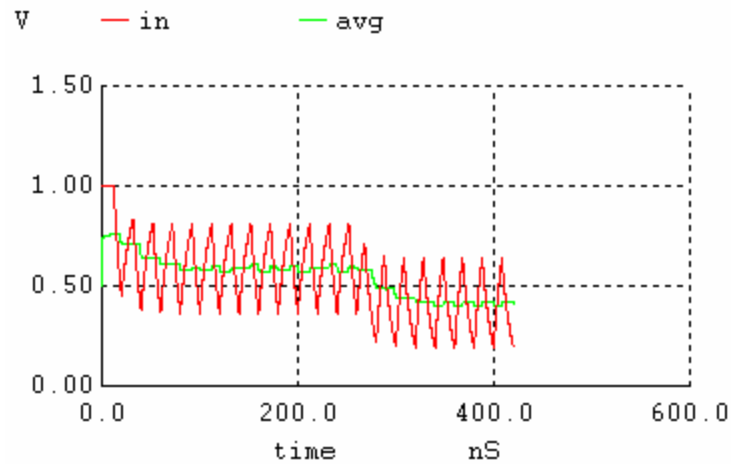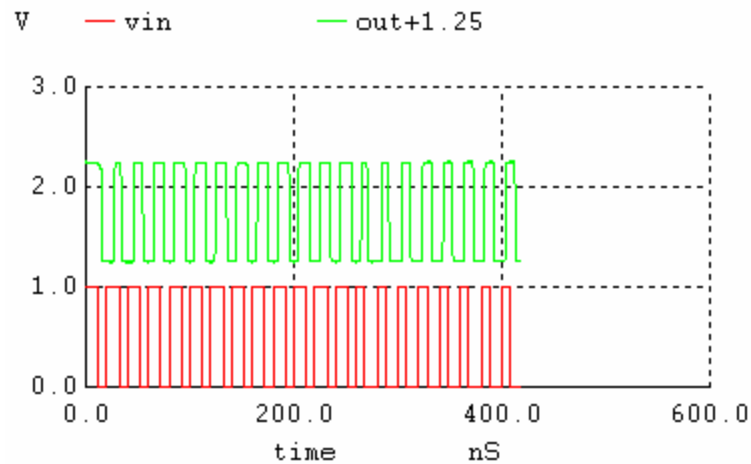
Conclusion: We need to adjust RC time constant of the DC average generation circuit for different input data pattern. This will limit its application in the real circuits.

18.10

```
Vin     Vin     0       DC      0       PULSE 0 1 0 0 0 4n 20n
R1      Vin     b       1K
C1      b       0       10p
R2      b       0       1K
R3      b       VDD     1K
M1      b       b       0       0       NMOS L=1 W=10
M4      b       b       VDD     VDD     PMOS L=1 W=20
M2      a       b       0       0       NMOS L=1 W=10
M5      a       b       VDD     VDD     PMOS L=1 W=20
M3      Vout    a       0       0       NMOS L=1 W=10
M6      Vout    a       VDD     VDD     PMOS L=1 W=20
.include model.txt
```
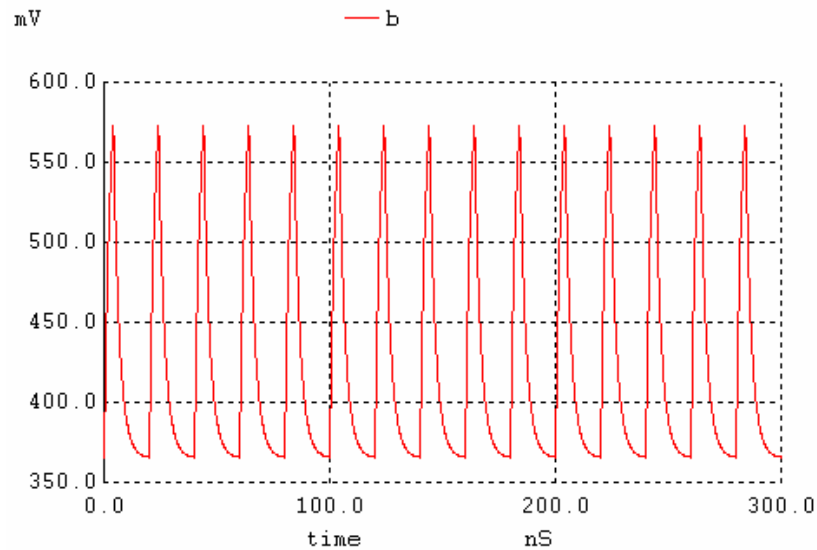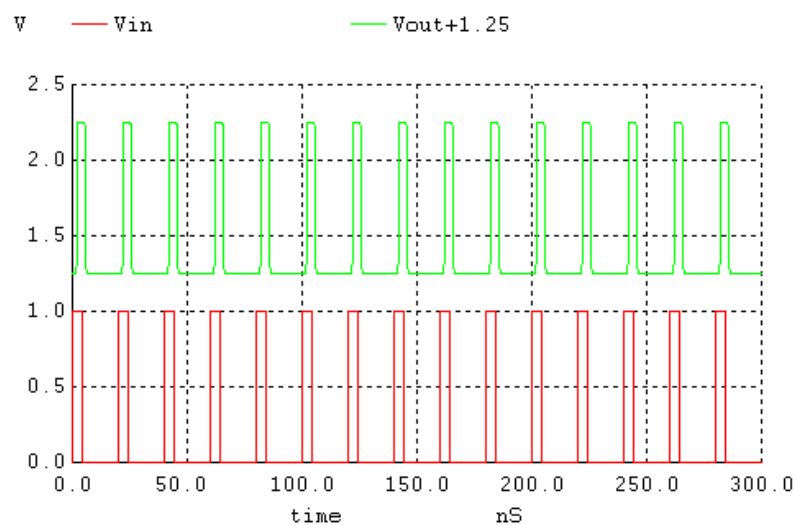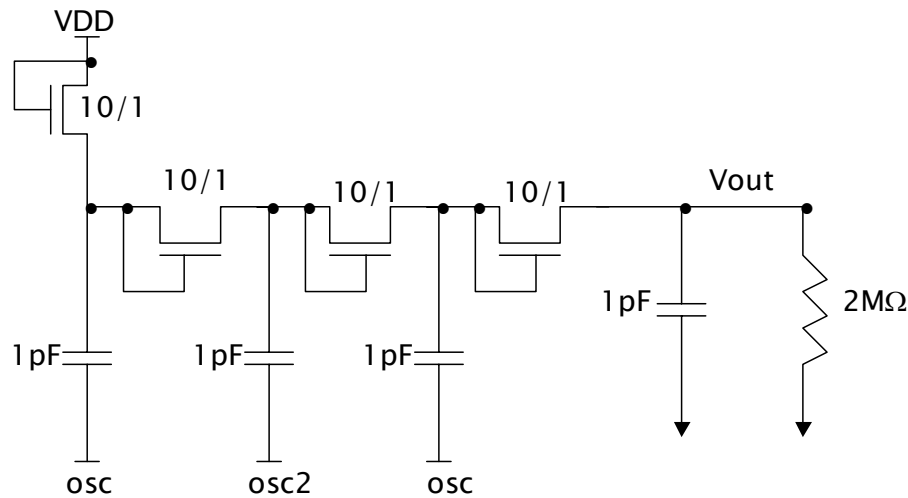
Signal Amplitude is directly affected by the input swing being limited by a Vt from Vdd. The power burnt is dependent on device sizing.

Problem 18.11: Design a nominally 2V voltage generator that can supply at most 1µA of DC current (2 MEG resistor). Simulate the operation of your design with SPICE.

The design of the 3-stage charge pump is shown below.

The signals osc and osc2 are generated with the oscillator shown below. The enable signal (one of the inputs to the NAND gate) is fedback from the regulator circuit to shut the pump off when 2V is achieved. The 10pF capacitors add delay to keep the oscillation frequency low enough that the pump capacitors have time to charge/discharge each cycle. All NMOS are 10/1 and PMOS are 20/1.
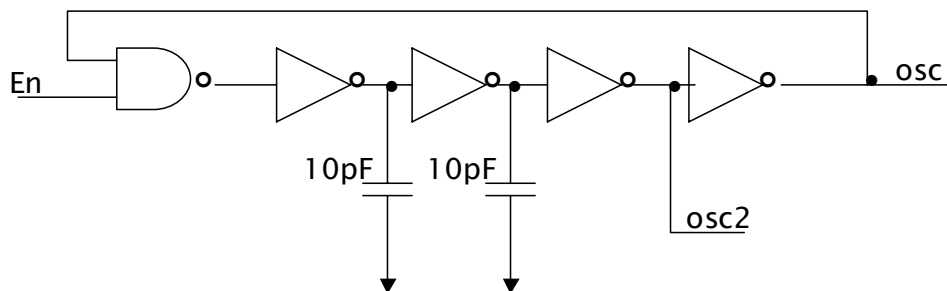
This SPICE simulation shows the unregulated output of the charge pump.
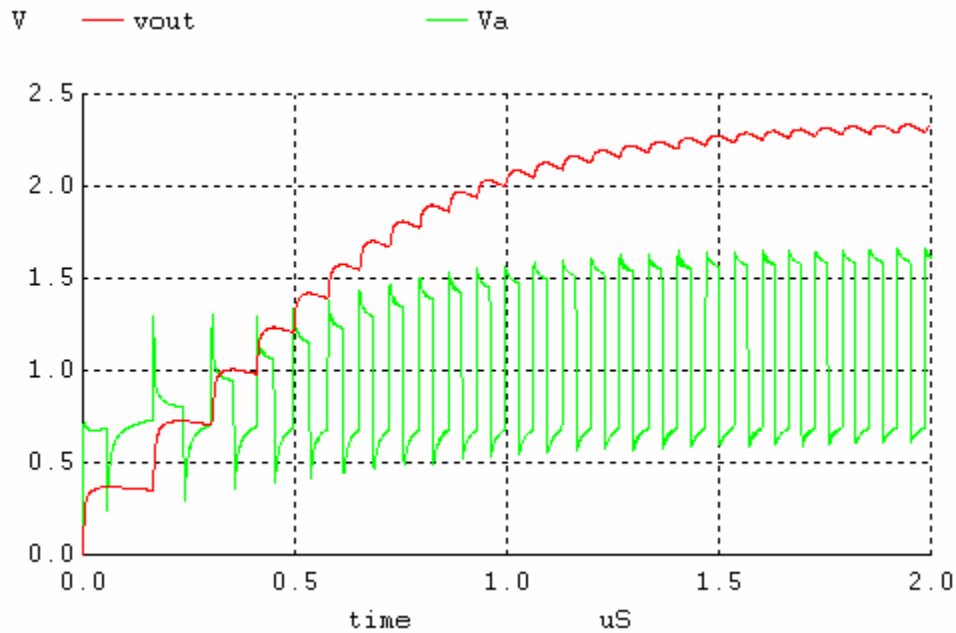
Regulation to 2V is achieved with the following circuit. A resistor voltage divider is used to level-shift the output so that a 2V output corresponds to the switching point of first inverter. Gate-drain connected MOSFETs could also be used to level-shift the output.
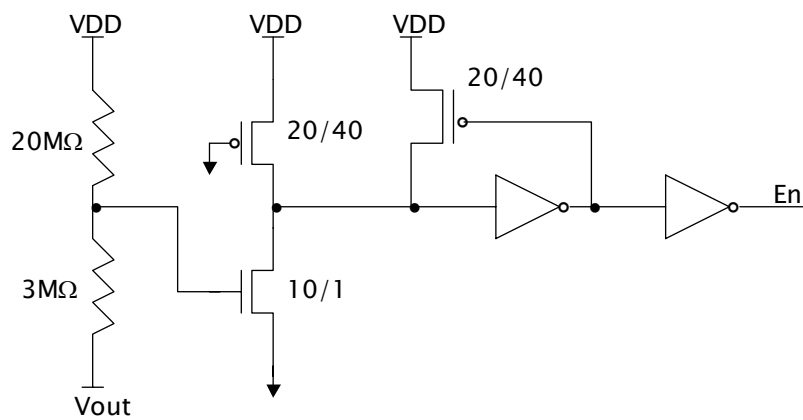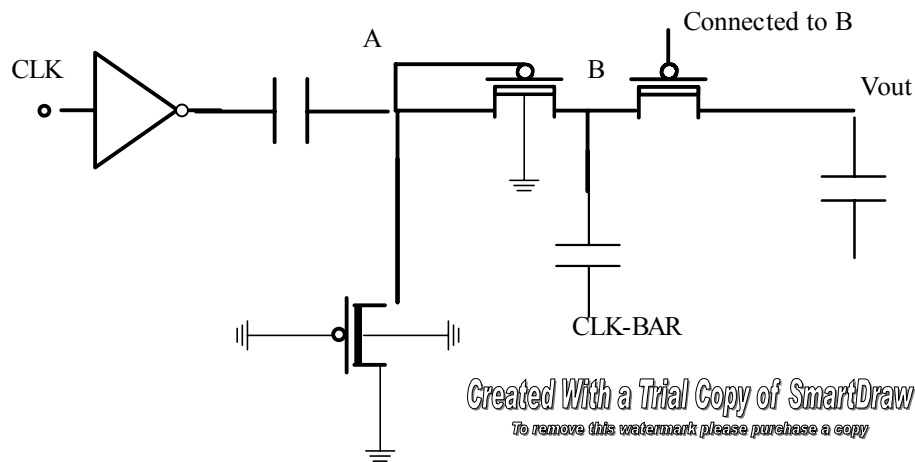
This SPICE simulation shows the output of the regulated pump, along with the Enable control signal. The pump output varies from approximately 2.1V to 1.9V (nominally 2V).
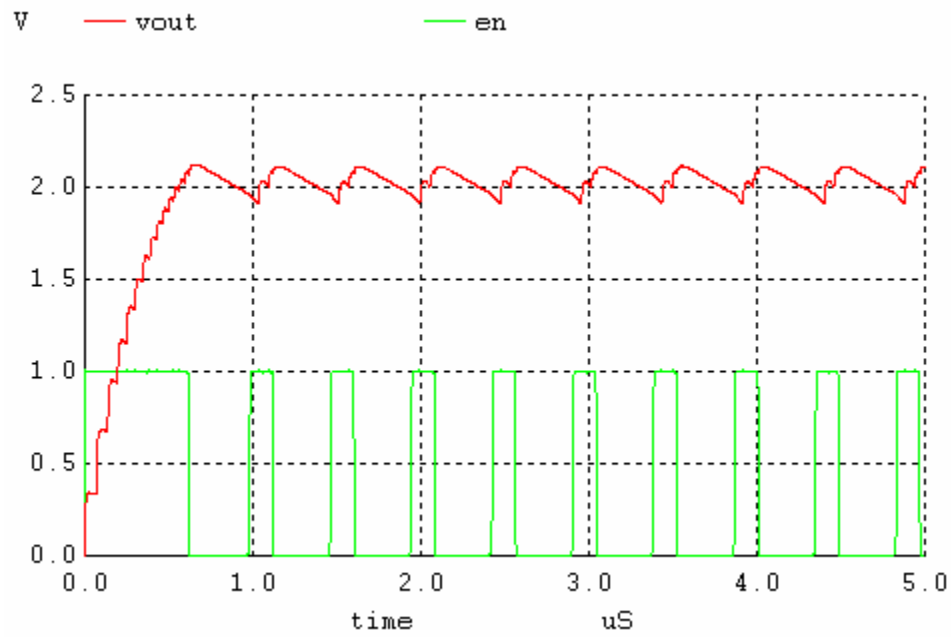
Problem 18.12

Following is the circuit used for this problem:

Following is the netlist for the problem:

```
.control
destroy all
run
plot vout A B
.endc

.option scale=50n
.tran    1n 1.4u UIC

VDD  VDD  0      DC    1
Vosc  osc  0      DC    0      AC    0      PULSE(1 0 0 0 0 50ns 100ns)

M1inv osci   osc   0    0      NMOS L=1 W=10
M2inv osci   osc   VDD  VDD    PMOS L=1 W=20

M11inv        osci1  osci  0    0      NMOS L=1 W=10
M12inv        osci1  osci  VDD  VDD    PMOS L=1 W=20

M1    A    0    0    0      PMOS L=1 W=20
M2    A    A    B    0      PMOS L=1 W=20

M3    B    B    vout  0      PMOS L=1 W=20

C1    osci  A    1p
C2    B    osci1  1p  IC=0
Cload  vout  0      2p  IC=0
```
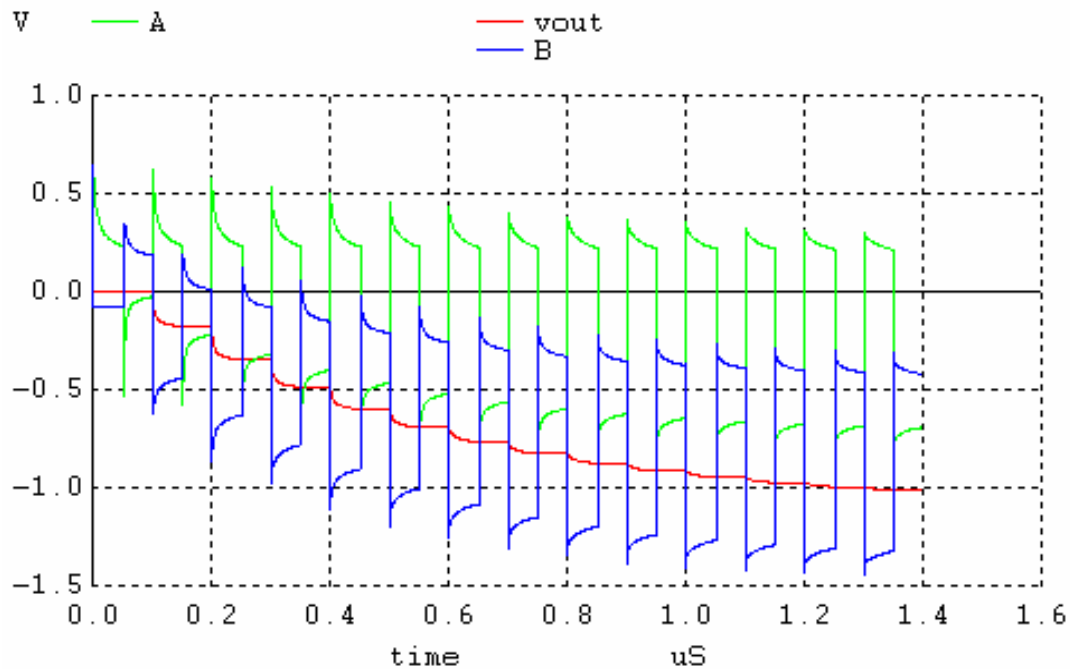
Following is the result for the circuit:

Discussion:

As seen from the graph above, the charge pump produces a voltage of -1 V. If we just use one stage charge pump, than the voltage will not charge -1 V.

Also, if we don't use CLK-BAR for the second capacitor, than the voltage only charges up to – VDD + Vth.