and thus

$$= \frac{V_P}{2j} \cdot [\delta(f-f_1) - \delta(f+f_1)] = 0 + j \cdot \frac{V_P}{2} \cdot [\delta(f+f_1) - \delta(f-f_1)] \qquad (1.84)$$

The magnitude of this equation is

$$\frac{V_P}{2} \cdot [\delta(f+f_1) - \delta(f-f_1)] \qquad (1.85)$$

and the phase response is

$$\tan^{-1} \frac{\frac{V_P}{2} \cdot [\delta(f+f_1) - \delta(f-f_1)]}{0} = \tan^{-1} \infty = 90° \qquad (1.86)$$

Note that using a single-sided spectrum with positive frequencies only we could rewrite the result as

$$= j \cdot V_P \cdot \delta(f-f_1) \qquad (1.87)$$

Note also that

$$Fourier\{V_P \cos(2\pi f_1 t)\} = \frac{V_P}{2} \cdot [\delta(f+f_1) + \delta(f-f_1)] \qquad (1.88)$$

Lastly note that *negative frequencies* shouldn't confuse us since they simply represent a phase shift. For example,

$$\sin(2\pi(-f)t) = -\sin(2\pi f t) = \sin(2\pi f t + \pi) = \sin(2\pi f t - \pi) \qquad (1.89)$$

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[1] M. Weeks, *Digital Signal Processing Using MATLAB and Wavelets*, Infinity Science Press, 2007. ISBN 978-0977858200

[2] S. Haykin and M. Moher, *An Introduction to Analog and Digital Communications*, Second Edition, John Wiley and Sons, 2006. ISBN 978-0471432227

[3] R. G. Lyons, *Understanding Digital Signal Processing*, Second Edition, Prentice-Hall, 2004. ISBN 978-0131089891

[4] P. A. Lynn and W. Fuerst, *Introductory Digital Signal Processing*, Second Edition, John Wiley and Sons, 1998. ISBN 978-0471976318

[5] L. W. Couch, *Modern Communication Systems: Principles and Applications*, Prentice-Hall, 1995. ISBN 978-0023252860

[6] E. P. Cunningham, *Digital Filtering: An Introduction*, John Wiley and Sons, 1995. ISBN 978-0471124757

QUESTIONS

1.1 Suggest an alternate physical example, to the swinging pendulum in Fig. 1.1, of sinusoidal motion.

1.2 Add the *z*-axis (time) to the representations of the sinewave seen in Figs. 1.3b-f as discussed following Eq. (1.4).

1.3 Suppose an *IQ* signal is generated using an in-phase component having an amplitude of 0.5 V and a quadrature component having an amplitude of 1 V. Sketch the resulting waveform, the *IQ* signal, in the time domain.

1.4 Figure 1.7 shows how the magnitude and phase are calculated for an imaginary number that resides in the first quadrant of the plane (both real and imaginary components are positive). Show how we calculate the magnitude and phase of an imaginary number in the other quadrants.

1.5 If the output of a system occurs after the corresponding input to the system, is the phase shift positive or negative? Why? What does linear phase indicate?

1.6 Using the SPICE files found at CMOSedu.com, verify, in the time-domain, the frequency response information seen in Fig. 1.10 for input frequencies of $f = 0$ (DC), $1/4t_d$, and $1/2t_d$.

1.7 Repeat question 1.6 for the digital comb filter (averager) seen in Fig. 1.17 for input frequencies of DC, $f_s/4$, and $f_s/2$.

1.8 Plot the magnitude and phase frequency responses of a discrete-time system having the transfer function $(1+z^{-1})/z^{-2}$. Next, show the location of this system's poles and zeros in the complex plane and verify, using the intuitive method discussed in Sec. 1.2.3, the gain and phase of the response match the frequency response plots when the input signal frequency is 0.

1.9 For the 3 delay element comb filter seen in Fig. 1.25, repeat question 1.6 for input frequencies of 0, $f_s/6$, and $f_s/3$.

1.10 Show how to plot $1/(4+3j)$ in the complex plane. What is the magnitude and phase shift of this complex number?

1.11 Determine the z-domain representation for the circuit seen in Fig. 1.30. Also, plot the frequency response, both magnitude and phase, and the location of poles and zeroes for this system.

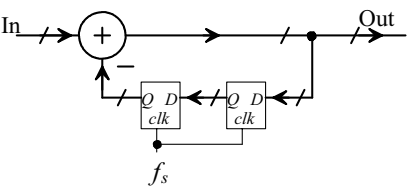

Figure 1.30 Circuit used in question 1.11.

1.12 Repeat question 1.11, and sketch the resulting circuit, if a delay is added to the forward path of the circuit seen in Fig. 1.30.

1.13 Determine the exponential Fourier series representation for the squarewave seen in Fig. 1.29 if it is centered around ground.

1.14 Determine the exponential Fourier series representation for the squarewave seen in Fig. 1.29 for the general case where $T_p \neq T_s/2$.

1.15 What is the Fourier transform of the signal seen in Fig. 1.29?

1.16 What is the area under the Dirac delta function bordered by the x-axis? Why?

1.17 Show how to take the Fourier transform of $\sin(2\pi f_0 t + \theta)$ and $\cos(2\pi f_0 t + \phi)$. Plot the magnitude and phase responses of the transforms.

ADDITIONAL READING

[1] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation, Revised Second Edition*, Wiley-IEEE, 2008. ISBN 978-0470229415

[2] C. C. Enz and G. C. Temes, "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization," *Proceedings of the IEEE*, Vol. 84, No. 11, pp. 1584-1614, November 1996.

[3] L. W. Couch, *Modern Communication Systems: Principles and Applications*, Prentice-Hall, 1995. ISBN 978-0023252860

QUESTIONS

2.1 Qualitatively, using figures, show how impulse sampling a sinewave can result in an alias of the sampled sinewave at a different frequency.

2.2 Re-sketch Figs. 2.12 and 2.13 when decimating by 5. hint: use a counter and some logic to implement the divide by 5 clock divider.

2.3 Explain why returning the output of the S/H to zero reduces the distortion introduced into a signal. What is the cost for the reduced distortion in a practical circuit?

2.4 Sketch the input and output spectrum for the following block diagram. Assume the DC component of the input is 0.5 V while the AC component is a sinewave at 4 MHz with a peak amplitude of 100 mV. Assume the clock frequency is 100 MHz.

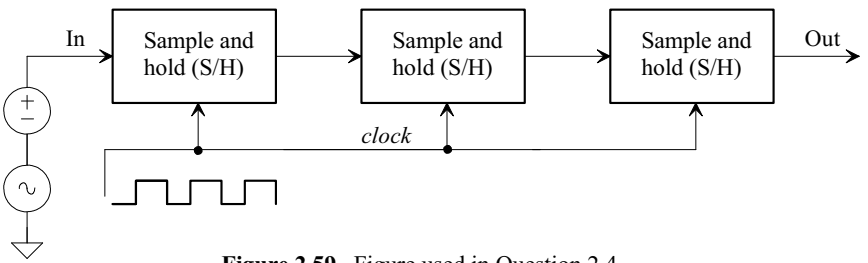

Figure 2.59 Figure used in Question 2.4.

2.5 Repeat Ex. 2.2 with an input sinewave at 30 MHz.

2.6 Re-sketch Fig. 2.22 if the input signal is a sinewave at 10 MHz (no other spectral content).

2.7 Suppose we are interpolating, with $K = 8$, digital data with $f_s = 100$ MHz. Prior to interpolation what is the frequency range of the desired spectrum? After interpolation what is the frequency range of the desired spectrum? What is the interpolator's output clock rate?

2.8 Verify, with simulations, that the topologies seen in Fig. 2.34 are equivalent.

2.9 Determine the transfer function, and verify with simulations, the behavior of 4 paths of the switched-capacitor topology seen in Fig. 2.36.

2.10 In your own words discuss why the ϕ_2 switches are shut off after the ϕ_1 switches in the S/H seen in Fig. 2.39.

2.11 Sketch the op-amp's open loop response, both magnitude and phase, specified by Eq. (2.59).

2.12 What is the voltage across C_F in Fig. 2.41 in terms of the input-referred offset and noise? Verify your answer with simulations commenting on the deviation of the frequency behavior of the input-referred noise to the frequency response of the voltage across the capacitor.

2.13 Provide a quantitative description of how capacitor mismatch will affect the operation of the S/H seen in Fig. 2.46. Verify your descriptions with simulations.

2.14 Is it possible to design a S/H with a gain of 0.5? How can this be done or why can't it be done? Use simulations to verify your answer.

2.15 For the first entry (v_1 = input, $v_2 = V_{CM}$) in Table 2.2 derive the frequency response, magnitude and phase, of the DAI. Use simulations at a few frequencies to verify your derivations.

2.16 Repeat Question 2.15 for the second entry.

2.17 Repeat Question 2.15 for the third entry.

2.18 Does the DAI use CDS? Why or why not? Use simulations to support your answers.

[4] P. R. Gray, B. A. Wooley, and R. W. Brodersen (eds.), *Analog MOS Integrated Circuits II*, Wiley-IEEE, 1989. ISBN 0-87942-246-7

[5] P. A. Lynn, *An Introduction to the Analysis and Processing of Signals*, Hemisphere Publishing Corporation, 1989. ISBN 0-89116-981-4

[6] Y. P. Tsividis and J. O. Voorman (eds.), *Integrated Continuous-Time Filters: Principles, Design, and Applications*, Wiley-IEEE, 1993. ISBN 0-7803-0425-X

[7] B. Nauta, *Analog CMOS Filters for Very High Frequencies*, Kluwer Academic Publishers, 1993. ISBN 0-7923-9272-8

QUESTIONS

3.1 Resketch Fig. 3.2 for the following circuit.

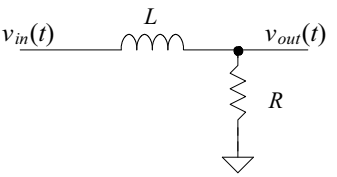

Figure 3.54 First-order lowpass filter using an inductor and a resistor.

3.2 Show that Eq. (3.6) is still valid if the circuit's inputs and outputs are referenced to the common-mode voltage, V_{CM}. (The op-amp inputs should also be at V_{CM}.)

3.3 Sketch the implementation of a first-order lowpass filter using a CAI with a 3 dB frequency of 10 MHz and a DC gain of 6 dB. Simulate your design to verify it works as expected.

3.4 Plot, in the complex plane, the ideal pole location and the actual pole locations due to finite op-amp unity gain frequency for the filter described in Ex. 3.4.

3.5 Plot Eq. (2.59) of the last chapter using SPICE and the op-amp model shown in Fig. 3.8.

3.6 Suppose an antialiasing filter was required for a 12-bit data converter. Further assume the filter is to be implemented using an active-RC topology. If *VDD* = 1.0 V, estimate the minimum value of the integration capacitor that should be used, assuming the filter's noise performance is dominated by thermal noise. Is it wise, for 12-bit system performance, to design the filter so that its SNR is equal to the SNR of the data converter?

3.7 Repeat question 3.6 if the op-amp used in the filter has a linear output swing of 80% of the power supply voltage.

3.8 Derive the transfer function for the filter shown in Fig. 3.16 if the transconductors have different g_ms. Sketch the block diagram, similar to the one seen in Fig. 3.6, for the filter.

3.9 Derive the transfer function for the following first-order transconductor filter.

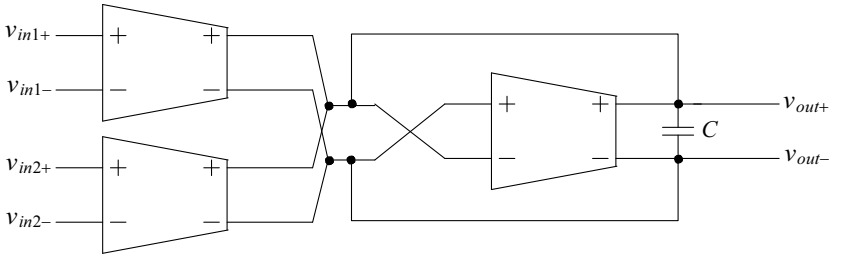

Figure 3.55 A first-order filter with two inputs.

3.10 Show the derivation details that result in Eqs. (3.44) and (3.46).

3.11 Show the details of how the gains, G, are derived in Fig. 3.30.

3.12 Is it possible to tune the gain, Q, and cutoff frequency of the lowpass biquad independently? If so, how? Give examples using the simulation netlist used to generate Fig. 3.38.

3.13 What happens to the poles in the biquadratic equation, Eq. (3.62), if the Q is less than 0.5? (Hint: The filter behaves like the cascade of two first-order filters.) Is the $f_{\max}$ equation in Fig. 3.35 valid?

3.14 Compare the size of the elements used in Exs. 3.8 and 3.9. Is there a benefit to using an active element for monolithic implementation?

3.15 Show, using the simulations from Ex. 3.14, that increasing the switch resistance, and thus the spectral content present in a switched capacitor circuit, can help to stabilize high-Q switched-capacitor bandpass filters.

3.16 Redesign and simulate the operation of the filter discussed in Ex. 3.14, with a Q of 5, while trying to minimize the difference between C_{I1} and C_{F2}. Suggest a possible modification to the filter topology (similar to how we add G_{2Q} in Fig. 3.45) to reduce this component spread.

3.17 Show how to derive the transfer function of the transconductor-C biquad filter seen in Fig. 3.53. Can this filter be orthogonally tuned? If so, how?

3.18 Repeat Ex. 3.9 using the transconductor-based biquad.

3.19 How would a "high-Q" biquad be implemented using transconductors? Repeat Ex. 3.12 using the transconductor-based biquad.

3.20 Show, using biquad sections, how the lowpass ladder filter seen in Fig. 3.56 can be implemented.

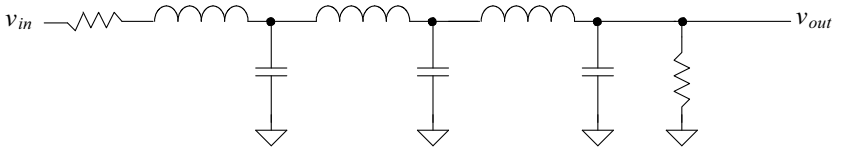

Figure 3.56 Implementing a ladder filter using biquads, see problem 3.20.

QUESTIONS

4.1 If V_{REF+} = 1.0 V and V_{REF-} = 0 regenerate Fig. 4.1 using SPICE. (Design a 3-bit ideal DAC model in SPICE.) The y-axis will be voltages in decimal form.

4.2 If, again, V_{REF+} = 1.0 V and V_{REF-} = 0, sketch Fig. 4.1 for a 1-bit DAC. Note that the digital input code will either be a 0 or a 1 and the analog voltage out of the DAC will be either 0 or 1.0 V. Using Eq. (4.1) what is the voltage value of 1 LSB? How does this compare to the value of 1 LSB we get from the sketch? Is Eq. (4.1) valid for a 1-bit DAC? Why? The 1-bit DAC will be a ubiquitous component in our noise-shaping modulators later in the book (see Fig. 7.15).

4.3 Why do the transfer curves of Fig. 4.3 show a shift of 1/2 LSB to the left? How do we implement this shift in SPICE?

4.4 Use SPICE to implement 4-bit ADC and DAC. If the converters are clocked at 100 MHz (and the outputs of the ADC are connected to the inputs of the DAC), apply an input sinewave (to the ADC) that has an amplitude of 500 mV peak centered around 500 mV DC with a frequency of 5 MHz. Again, use V_{REF+} = 1.0 V and V_{REF-} = 0. Show the DAC's analog output.

4.5 Using SPICE generate the spectrums of the input and output signals in question 4.4.

4.6 Suppose we think of the 1-bit input, 0 or 1, in Fig. 4.9 as +1 or −1 (two's complement numbers). What is the output of the digital filter when the input is always 0? Is the magnitude response seen in Fig. 4.10 correct? Why?

4.7 Suppose the 1-bit input signal seen in Fig. 4.9 is an alternating sequence of 101010... In terms of two's complement numbers, what is the output of the digital filter (what is the output of the counter)? What is the frequency of the input signal? Is the frequency response seen in Fig. 4.10 correct?

4.8 Repeat Ex. 4.3 for a filter with a transfer function of

$$\frac{1-z^{-7}}{1-z^{-1}}$$

Also, plot the location of the filter's poles and zeroes in the z-plane.

4.9 Repeat Ex. 4.3 for a filter with a transfer function of

$$\frac{1-z^{-9}}{1-z^{-1}}$$

4.10 Repeat Ex. 4.5 if L is increased to 3.

4.11 Sketch the impulse response of the filter seen in Fig. 4.19.

4.12 What are the transfer functions of the bandpass filters, indicated in Fig. 4.22, with center frequencies of $f_s/6$ and $f_s/3$? Sketch the frequency responses and the location of their poles and zeroes in the z-plane.

4.13 Simulate, using an ideal 8-bit ADC on the input, and an ideal DAC on the output (calculate the size of the DAC), the operation of the digital resonator seen in Fig. 4.23.

4.14 Qualitatively explain why the desired spectrum of an input signal can't be increased by passing data through an interpolator. Using the simulations given in Ex. 4.8, verify that this is indeed the case.

4.15 In Fig. 4.32, which blocks serve as the AAF and which serve as the S/H?

4.16 For the FIR filter seen in Fig. 4.35 with all coefficients set to 0.25, sketch the filter's frequency response.

4.17 For the filter seen in Fig. 4.57 determine the range of values for a and b where the filter will be stable. What is the filter's transfer function? Sketch the location of the filter's poles and zeroes.

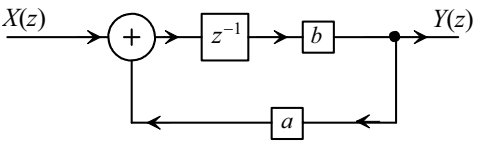

Figure 4.57 A weighted integrating filter.

4.18 Repeat Ex. 4.9 for a filter with a transfer function of

$$\frac{v_{out}}{v_{in}} = \frac{1 + j \cdot \frac{f}{4\ MHz}}{1 + j \cdot \frac{f}{800\ kHz}}$$

4.19 Repeat Question 4.18 using the canonic form of the first-order digital filter.

4.20 Repeat Ex. 4.12 if the Q is increased to 1.

4.21 Show that the filter shown in Fig. 4.58 can be implemented using a single multiplier.

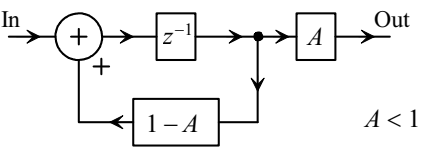

Figure 4.58 Filter used for question 4.21.

4.22 Show that if the values of A and B are restricted to 1, 0.5, 0.25, 0.125, etc. that the circuit of Fig. 4.59 can be used to implement multiplication by coefficients that aren't directly powers of two. How would a multiply by 0.75 be implemented? a multiply-by-0.9375? a multiply-by-0.5625?

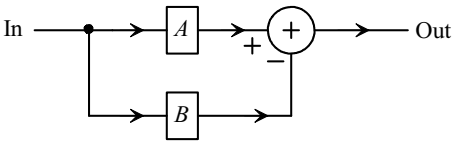

Figure 4.59 A simple multiplier where A and B simply shift the data.

QUESTIONS

5.1 Develop an expression for the effective number of bits in terms of the measured signal-to-noise ratio if the input sinewave has a peak amplitude of 50% of ($V_{REF+} - V_{REF-}$).

5.2 When using Eq. (5.14) what is the assumed ADC input signal? Put your answer in terms of the ADC reference voltages.

5.3 Describe, in your own words, the difference between specifying SNR and SNDR.

5.4 Using SPICE simulations with an ideal ADC and DAC, show how coherent sampling can result in an RMS value of quantization noise larger than what is specified by Eq. (5.3). Comment on the shape of the quantization noise's spectrum.

5.5 Suppose a perfectly stable clock is available (ΔT_s is zero in Eq. [5.21]). Would we still have a finite aperture window if the clock has a finite rise time? Describe why or why not?

5.6 How do the number of bits lost because of aperture jitter change with the frequency of an ADC input sinewave? If the ADC input is a DC signal, is aperture jitter a concern? Why?

5.7 Why must Bennett's criteria be valid for the averaging filter in Fig. 5.29 to reduce the quantization noise in the digital output signal? Give an example input signal where averaging will not reduce quantization noise.

5.8 Assuming Eq. (5.57) is valid, rederive Eq. (5.13) including the effects of averaging K ADC output samples. Is Eq. (5.13) or the equation derived here valid for a slow or DC input signal? Comment on why or why not.

5.9 If Bennett's criteria are valid, does averaging ADC outputs (or DAC inputs) put any restrictions on the bandwidth of the input signal? Why? Give an example.

5.10 How accurate does an 8-bit ADC have to be in order to use a digital filter to average 16 output samples for a final output resolution of 10-bits (see Eq. [5.59])? Assume the ideal LSB of the 8-bit converter is 10 mV. Your answer should be given in both mV and % of the full-scale.

5.11 Show the detailed derivation of Eq. (5.66).

5.12 Summarize, and compare, the advantages and disadvantages of predictive and noise-shaping data converters.

ADDITIONAL READING

[1] J. C. Candy and G. C. Temes (eds.), *Oversampling Delta-Sigma Data Converters*, IEEE Press, 1992. ISBN 0-87942-285-8

[2] S. K. Tewksbury and R. W. Hallock, *Oversampled, Linear Predictive and Noise-Shaping Coders of Order N*>1, IEEE Trans. Circuits and Sys., Vol. CAS-25, pp. 436-447, July 1978.

[3] H. Inose, Y. Yasuda, *A Unity Bit Coding Method by Negative Feedback*, Proc. IEEE, Vol. 51, pp. 1524-1535, November 1963

QUESTIONS

6.1 Suggest a topology for a passive-integrator NS modulator where the input and fed back signals are currents. Derive a transfer function for your design. Does your topology have the extra noise/distortion term seen in Eq. (6.12)? Why or why not? Simulate the operation of your design.

6.2 Simulate the operation of the NS modulator seen in Fig. 6.4a but using a 4-bit quantizer (ADC). Use a 100 MHz clock frequency and an input sinewave at 500 kHz (as used to generate Fig. 6.7).

6.3 Using Eqs. (6.14) and (6.17) compare the noise performance of passive NS modulators using a 1-bit quantizer to those using a 4-bit quantizer.

6.4 Repeat Ex. 6.2 if C is changed to 1 pF and a 1 GHz clock frequency is used. Estimate the frequency where the output of the digital filter is −3 dB (0.707) from the input signal. Verify your answer with simulations.

6.5 Suppose the comparator used in the NS modulator and filter used in Ex. 6.2 has a 50 mV input-referred offset voltage. How will this offset voltage affect the conversion from analog to digital? Verify your answer with SPICE simulations.

6.6 Figure 6.36 shows the implementation of an op-amp using mixed-signal design techniques. Assuming the comparator is powered with a 1 V supply, simulate the circuit in the inverting op-amp configuration with the non-inverting input held at 0.5 V, a 10k resistor connected from the inverting input to the input source, and a feedback resistor of 100k from the op-amp's output back to the inverting input (for a closed loop gain of −10). Set the input source to have a DC offset of 500 mV, and a peak-to-peak amplitude of 20 mV at 500 kHz. Explain how the circuit operates. Note that using an active integrator, instead of the passive integrator results in more ideal behavior (less variation on the op-amp's inputs).

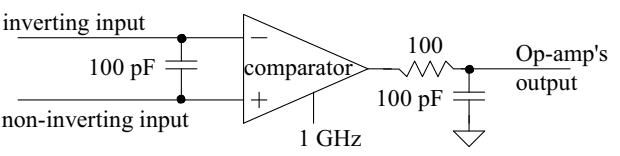

Figure 6.36 An op-amp implemented using mixed-signal techniques.

6.7 In your own words explain why dead zones in the second-order passive modulator seen in Fig. 6.17 are less of a problem than the first-order modulator seen in Fig. 6.4a.

6.8 Verify, using simulations, that the modulator seen in Fig. 6.20 suffers from capacitor mismatch while the one in Fig. 6.22 does not.

6.9 What is a time-interleaved data converter? Why is a time-interleaved converter different from the converter seen in Fig. 6.24?

6.10 Show the details of how to derive the transfer function of the path filter seen in Fig. 6.24.

6.11 Repeat question 6.7 if an active integrator, Fig. 6.28, is used in place of the passive integrator.

6.12 Repeat Ex. 6.5 if K is changed from 16 to 8.

QUESTIONS

7.1 Show how to derive Eqs. (7.1) and (7.2) from the block diagram seen in Fig. 7.1.

7.2 After reviewing Sec. 2.2.3, would it be possible to replace the delaying integrator seen in Fig. 7.2 with a non-delaying integrator? If so, what is the *NTF* and *STF* of the modulator? Is the modulator stable?

7.3 Using SPICE simulations, show how passing the digital signal seen in Fig. 7.3 through an RC lowpass filter will reduce the modulation noise in the signal and help to recover the original analog input signal. What happens to the original signal's amplitude if it's filtered, by the added RC filter, too much?

7.4 Show the spectrums (modulator input, digital output, and analog output after filtering) of the signals in question 7.3. Discuss what the spectrums indicate.

7.5 If an extra delay, z^{-1}, was added to the forward path of the modulator in Fig. 7.2 would the resulting topology be stable? Why or why not?

7.6 Show, using timing diagrams, how Eq. (7.3) is correct.

7.7 For the NS modulator shown in Fig. 7.5 used for digital to analog conversion, what component serves as the ADC? What component serves as the DAC?

7.8 Explain how the quantizer in Fig. 7.5 functions.

7.9 What are we assuming about an input signal if the modulation noise follows Eq. (7.5)?

7.10 What is the magnitude of Eq. (7.5) (plot it against frequency)?

7.11 What is the difference between quantization noise and modulation noise?

7.12 Show the steps and assumptions leading to Eq. (7.12).

7.13 Is the statement on page 238 that "every doubling in the oversampling ratio results in 1.5 bits increase in resolution" really true if K is small? Explain.

7.14 Does noise-shaping work for DC input signals? If so, how?

7.15 Show the steps leading up to Eq. (7.22).

7.16 What is the difference between a NS ADC and a Nyquist ADC?

7.17 In your own words, describe ripple in the output of a digital filter connected to an NS modulator.

7.18 Does adding a dither signal to the input of a NS modulator help reduce the peak-to-peak ripple in the digital filter output? Does it help to break up tones in the filter's output?

7.19 Derive Eq. (7.26).

7.20 Repeat Ex. 7.3 if the integrator's gain is set to 0.5.

7.21 Estimate the range of G_c for the quantizer seen in Fig. 7.16. How does this compare to the range of G_c for the 1-bit quantizer seen in Fig. 7.15? Name two benefits of the 1-bit quantizer over multi-bit quantizers.

7.22 Verify that Eq. 7.30 is correct. Use pictures if needed.

7.23 In your own words, and without equations, describe integrator leakage. How would you relate integrator leakage, found in integrators that use an active element as seen in the NS modulators found in this chapter, to the passive integrators used in the NS modulators discussed in the last chapter?

7.24 Would large parasitic op-amp input capacitance affect the settling time of a DAI? Verify your answer using simulations with ideal op-amps (infinite open-loop gain) and non-ideal op-amps (open-loop gains around the oversampling ratio, K).

7.25 In your own words, how does oversampling affect input-referred offset/noise and the effects of a jittery clock on an NS data converter?

7.26 Determine the transfer function of the DAI shown in Fig. 7.20.

7.27 Derive Eq. (7.51).

7.28 Sketch the implementation of the fully-differential second-order NS modulator.

7.29 Derive Eq. (7.61).

7.30 Sketch the fully-differential equivalent of Fig. 7.33.

7.31 Resimulate the modulator in Ex. 7.4 if the gains are set to one. Comment on the stability of the resulting circuit.

7.32 Resimulate the modulator in Ex. 7.4 if the input is only 50 mV. Comment on the stability of the resulting circuit.

7.33 Regenerate Fig. 7.40 by selecting integrator gains so that the maximum output swing of any op-amp is 800 mV peak-to-peak.

7.34 Comment, in your own words, on why the actual SNR of a NS-based data converter can be worse than the ideal values calculated in the chapter.

7.35 Derive Eq. (7.75). Make sure each step of the derivation includes comments.

7.36 Resimulate Fig. 7.44 using two-bit ADC and DAC.

7.37 Sketch a possible implementation of a quantizer for the error feedback modulator shown in Fig. 7.48.

7.38 What transfer function does the following block diagram implement?

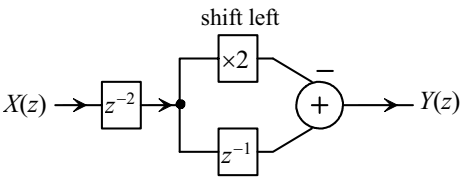

Figure 7.60 Circuit for question 7.38.

7.39 In Fig. 7.54 sketch the block diagram implementation of the circuit in series with the $v_2(z)$ output.

7.40 Derive the transfer function of the topology seen in Fig. 7.61 (show details of your derivation). What is the input common-mode voltage of the op-amp? Is this a concern when not using a negative supply voltage? If the input signals have a common-mode of *VDD*/2, does this affect the common-mode voltage of the circuit's output (remember that the op-amp is part of an integrator). Would it be a good idea, now that the inputs of the op-amp and the top plates of the capacitors are tied to ground or the virtual ground of the op-amp, to swap the bottom and top plates of the capacitors? Why or why not? Use SPICE to support your answers.

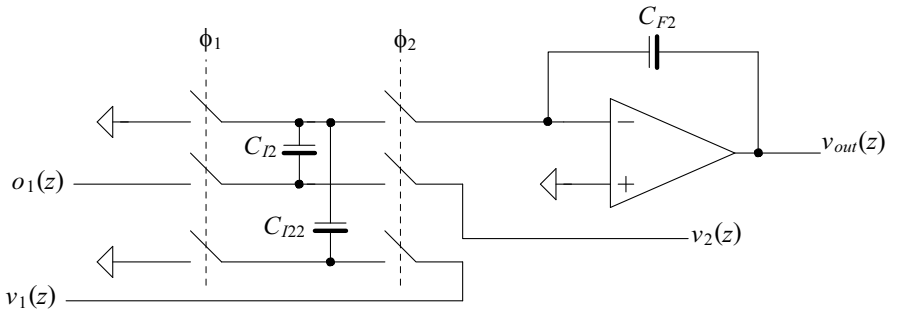

Figure 7.61 Circuit used in question 7.40.

7.41 Repeat question 7.40 for the op-amp circuit seen in Fig. 7.62.

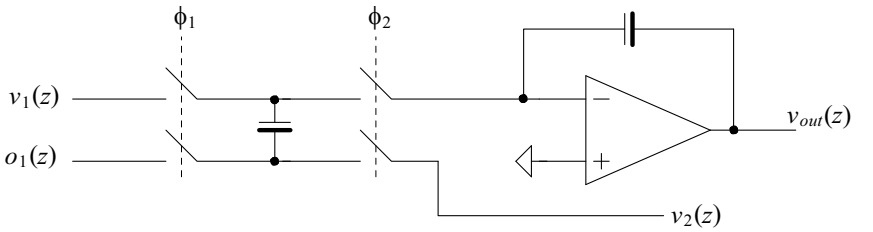

Figure 7.62 Circuit used in question 7.41.

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[5] S. R. Norsworthy, R. Schreier, and G. C. Temes (eds.), *Delta-Sigma Data Converters: Theory, Design, and Simulation*, Wiley-IEEE Press, 1997. ISBN 978-0780310452

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[7] B.-S. Song, "A Fourth-Order Bandpass Delta-Sigma Modulator with Reduced Numbers of Op-Amps," *IEEE Journal of Solid-State Circuits*, Vol. 30, No. 12, pp. 1309-315, December 1995

[8] D. B. Ribner, "Multistage Bandpass Delta Sigma Modulators," *IEEE Circuits and Systems II: Analog and Digital Signal Processing*, Vol. 41, No. 6, pp. 402 - 405, June 1994

[9] S.A. Jantzi, W.M. Snelgrove, and P.F. Ferguson Jr., "A Fourth-Order Bandpass Sigma-Delta Modulator," *IEEE Journal of Solid-State Circuits*, Vol. 28, No. 3, pp. 282 - 291, March 1993

[10] J. C. Candy and G. C. Temes (eds.), *Oversampling Delta-Sigma Data Converters*, Wiley-IEEE Press, 1992. ISBN 978-0879422851

QUESTIONS

8.1 Show, using SPICE, how to adjust the phase and amplitude of the *I* and *Q* signals discussed in the beginning of the chapter to modulate the amplitude and phase of the resulting *I*/*Q* to construct a constellation diagram for 8-level rectangular *QAM*.

8.2 Suggest a topology for the bandpass passive-integrator NS modulator where the input and fed back signals are currents. Derive a transfer function for your design. Does your topology have the extra noise/distortion term seen in Eq. (8.12)? Why or why not? Simulate the operation of your design.

8.3 Show the details of deriving the transfer function for the modulator in Fig. 8.6.

8.4 Repeat question 8.3 for the modulator seen in Fig. 8.8.

8.5 Derive the transfer function for the modulator seen in Fig. 8.9.

8.6 Sketch the implementation of a modulator, based on the topology seen in Fig. 8.9, but using a multi-bit quantizer and feedback DAC.

8.7 Show the details of how Eq. (8.18) is derived.

8.8 Derive the transfer function of the modulator seen in Fig. 8.12.

8.9 Using the modulator topology in Ex. 8.4, show that if we apply a 25 MHz input sinusoid to the modulator we can recover this input signal by passing the output digital data through a bandpass filter with a very small bandwidth (show that the input and output signal amplitudes are equal).

8.10 Derive the transfer function of the topology seen in Fig. 8.17. Verify that the topology is unstable by determining the location of the topology's poles.

8.11 Using a bandpass modulator and digital demodulation (sketch the schematic of your design) show how to recover a 10 kHz sinewave that is amplitude modulated with a carrier frequency of 1 MHz. Use SPICE to verify the operation of your design.

ADDITIONAL READING

[1] F. Borghetti, C.D. Fiore, P. Malcovati, and F. Maloberti, "Synthesis of the Noise Transfer Function in N-path Sigma-Delta Modulators," *5th IEE International Conference on Advanced A/D and D/A Conversion Techniques and their Applications*, Limerick, Ireland, pp. 171-176, July 25-27, 2005.

[2] A. Eshraghi and T. S. Fiez, "A Comparative Analysis of Parallel Delta–Sigma ADC Architectures," *IEEE Trans. on Circuits and Systems - I: Regular Papers*, Vol. 51, No. 3, pp. 450-458, March 2004

[3] A. Eshraghi and T. S. Fiez, "A Time-Interleaved Parallel DS A/D Converter," *IEEE Trans. on Circuits and Systems - II: Analog and Digital Signal Processin*g, Vol. 50, No. 3, pp. 118-129, March 2003

[4] V.-T. Nguyen, P. Loumeau, and J. F. Naviner, "Advantages of High-Pass DS Modulators in Interleaved DS Analog-to-Digital Converter," *Proceedings of the 45th Mid-West Symposium on Circuits and Systems*, August 4-7, Tulsa, OK, pp. I-136-I-139, 2002

[5] M. Kozak, and I. Kale, "Novel Topologies for Time-Interleaved Delta–Sigma Modulators," *IEEE Trans. on Circuits and Systems - II: Analog and Digital Signal Processing*, Vol. 47, No. 7, pp. 639-654, July 2000

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[7] R. Khoini-Poorfard, L. B. Lim, and D. A. Johns, "Time-Interleaved Oversampling A/D Converters: Theory and Practice," *IEEE Trans. on Circuits and Systems - II: Analog and Digital Signal Processing,* Vol. 45, No. 8, pp. 634-645, August 1997

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[9] R. Schreier, G. C. Temes, A. G. Yesilyurt, Z. X. Zhang, Z. Czarnul and A. Hairapetian, "Multibit Bandpass Delta-Sigma Modulators using N-path Structures," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 593-596, May 10-13 1992

QUESTIONS

9.1 What is a time-interleaved data converter? Why is a time-interleaved converter different from the *K*-Delta-1-Sigma converter seen in Fig. 9.4? Sketch the implementation of a time-interleaved data converter implemented with Delta-Sigma modulators. Also sketch the clock signals used in the topology.

9.2 Using the modulator from Ex. 9.1 show that capacitor matching isn't important in the *K*-Delta-1-Sigma topology.

9.3 Repeat question 9.2 but show that the open-loop gain of the amplifier used in the integrator isn't critical (compare, using simulations, the performance of the converter using different gains).

9.4 Show the details of (derive from the time-domain outputs of the *K*-Delta-1-Sigma modulator) how the path filter seen in Fig. 9.4 has a *z*-domain transfer function of

$$\frac{1-z^{-8}}{1-z^{-1}}$$

Explain how this filter performs a moving-average filtering of the modulator's outputs. Does this filter decimate the *K*-Delta-1-Sigma outputs? Why or why not?

9.5 Sketch the decimate by *K*/4 topology similar to the topologies seen in Fig. 9.7. Ensure the proper clock signals are used in your sketch.

9.6 Explain, in your own words, why oversampling (averaging the outputs) using a 3-bit Flash converter (eight comparators), won't result in as significant improvement in SNR as the *K*-Delta-1-Sigma topology.

9.7 What is the frequency response (an equation) of the filter seen in Fig. 9.10?

9.8 What is the frequency response (an equation) of the filter seen in Fig. 9.12?

9.9 What is the frequency response (an equation) of the filter seen in Fig. 9.14?

9.10 What is the frequency response (an equation) of the filter seen in Fig. 9.16?

9.11 Show how the switches on the inputs and outputs of the 8 modulators in parallel seen in Fig. 9.20 can be described using the unit matrix and delays or

$$\begin{bmatrix} 1&0&0&0&0&0&0&0 \\ 0&1&0&0&0&0&0&0 \\ 0&0&1&0&0&0&0&0 \\ 0&0&0&1&0&0&0&0 \\ 0&0&0&0&1&0&0&0 \\ 0&0&0&0&0&1&0&0 \\ 0&0&0&0&0&0&1&0 \\ 0&0&0&0&0&0&0&1 \end{bmatrix} \cdot \begin{bmatrix} z^{-0} \\ z^{-1/8} \\ z^{-2/8} \\ z^{-3/8} \\ z^{-4/8} \\ z^{-5/8} \\ z^{-6/8} \\ z^{-7/8} \end{bmatrix}$$

where $z = e^{j2\pi f \cdot T_s}$. Using these relationships show how to relate the inputs of the *K* paths in parallel, Fig. 9.20, to the transfer function $H(z)$ and the resulting topology's outputs.

9.12 The effective sampling frequency of the *K*-Delta-1-Sigma ADC discussed in Sec. 9.2 is roughly 1.6 GHz. Can any component of the ADC operate at, or be clocked at, 1.6 GHz? Verify your answers using SPICE and the 500 nm, 5 V, CMOS models used to generate these figures. What is the most critical component then, from a timing perspective, (the DFF used to capture the eight bits coming out of the modulators) and what is critical in that component (the DFF's setup and hold times)? What happens if an error is made in the most critical component? (The wrong count is captured. For example, we should capture 6 logic 1s but we actually capture 5 or 7 logic 1s. Since we have a significant amount of averaging in the digital filter the effects should be small. If an equal number of positive and negative errors are made the errors average to zero and don't affect the converter's performance.)