Problem 10.1 **By Vehid Suljic**

Using the parameters in Table 6.1 compare the hand-calculated effective digital switching resistance using Eq. (10.6) to the empirically derived values given in table 10.1.

Using equation 10.6 ,

$Rn = VDD/[0.5\ KPn\ (W/L)\ (VDD-Vthn)^2]$

Pluging in values for the parameters from table 6.1 we obtain switching resistance,

$Rn = 4.7K\ (L/W)$

However, empirically derived Rn in table 10.1 is Rn = 15K (L/W) which is very different from hand calculated results above.
This is due to the mobility (μ, $Kpn = \mu\ Cox'$) that is not constant with applied voltage (electric field).

Problem 10.2 **Justin Wood**

10.2) Regenerate Figure 10.14 for the PMOS device.

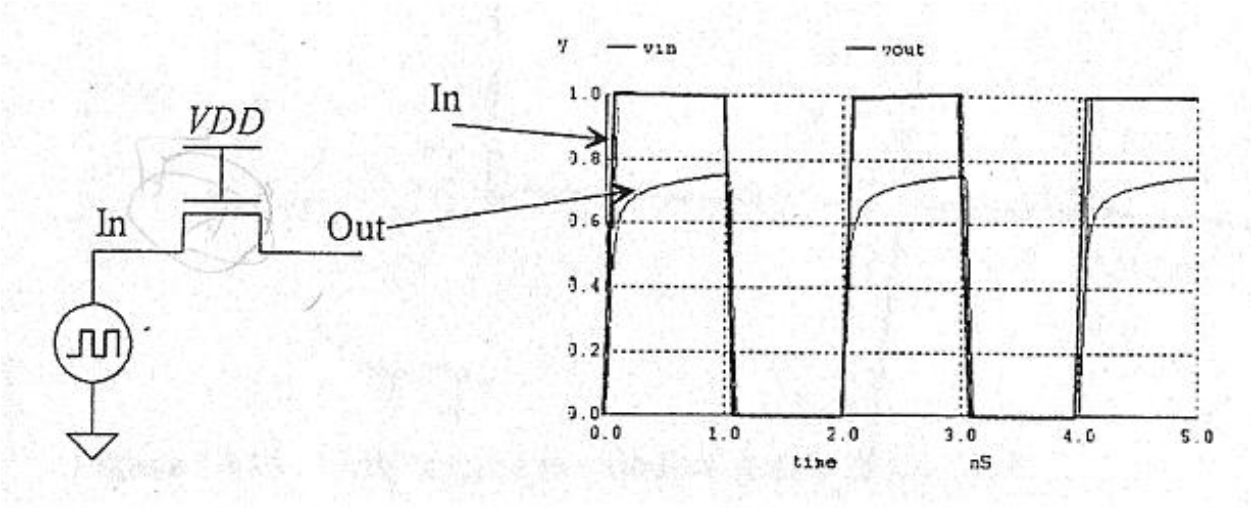
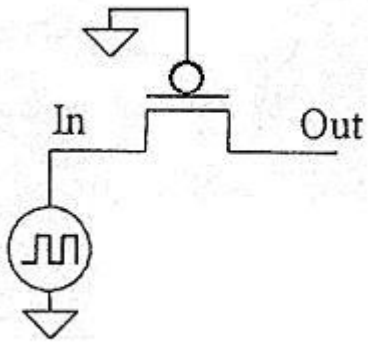


Figure 10.14

Substituting a PMOS for an NMOS, the circuit now becomes:



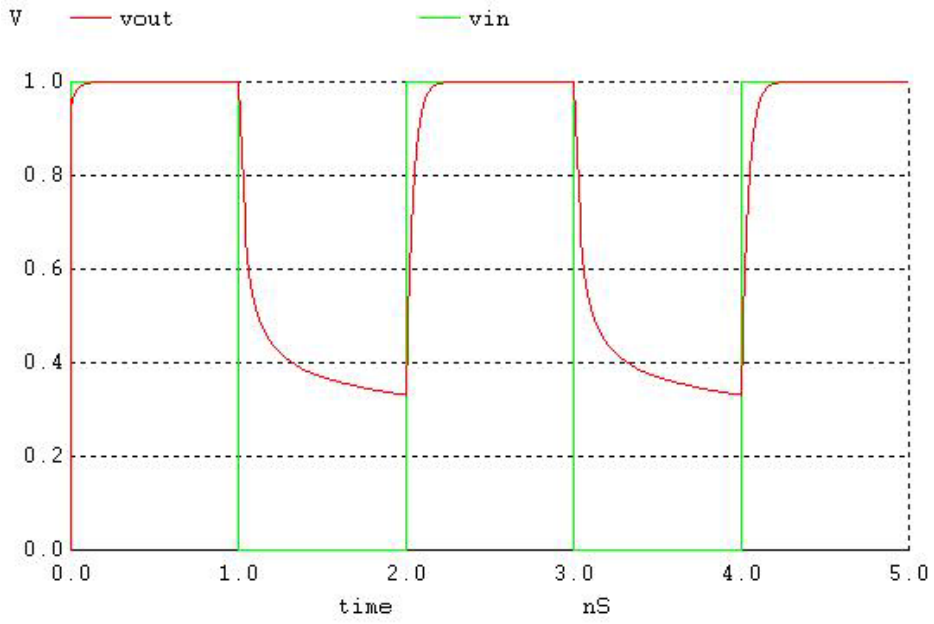
When the pulse source (Vin) is equal to 1, Vsource=Vin and Vdrain=Vout. Which results in the transistor being on (Vsg>Vthp) and Vout is equal to Vin.

When Vin is equal to 0, the source and drain switch and Vout must be equal to Vthp for the transistor to be on.

The spice simulation netlist and plot are shown below.

```
.control
destroy all
run
plot vout vin ylimit 0 1
.ic v(vin)=1          v(vout)=1
.endc
.option scale=50n
.tran 10p 5n UIC
vdd       vdd       0         DC       1
Vin       vin       0         DC       0         pulse 0 1 0 1p 1p 1n 2n
M1        vin       0         vout     Vdd       PMOS L=1 W=10

.model  pmos  pmos  level = 14
+binunit = 1          paramchk= 1          mobmod  = 0
+capmod  = 2          igcmod  = 1          igbmod  = 1          geomod  = 1
+diomod  = 1          rdsmod  = 0          rbodymod= 1          rgatemod= 1
+permod  = 1          acnqsmod= 0          trnqsmod= 0
+tnom    = 27         toxe    = 1.4e-009   toxp    = 7e-010     toxm    = 1.4e-009
+epsrox  = 3.9        wint    = 5e-009     lint    = 1.2e-008
+ll      = 0          wl      = 0          lln     = 1          wln     = 1
+lw      = 0          ww      = 0          lwn     = 1          wwn     = 1
+lwl     = 0          wwl     = 0          xpart   = 0          toxref  = 1.4e-009
+vth0    = -0.22      k1      = 0.39       k2      = 0.05       k3      = 0
+k3b     = 0          w0      = 2.5e-006   dvt0    = 3.9        dvt1    = 0.635
+dvt2    = -0.032     dvt0w   = 0          dvt1w   = 0          dvt2w   = 0
+dsub    = 0.7        minv    = 0.05       voffl   = 0          dvtp0   = 0.5e-008
+dvtp1   = 0.05       lpe0    = 5.75e-008  lpeb    = 2.3e-010   xj      = 2e-008
+ngate   = 5e+020     ndep    = 2.8e+018   nsd     = 1e+020     phin    = 0
+cdsc    = 0.000258   cdscb   = 0          cdscd   = 6.1e-008   cit     = 0
+voff    = -0.15      nfactor = 2          eta0    = 0.15       etab    = 0
+vfb     = 0.55       u0      = 0.0095     ua      = 1.6e-009   ub      = 8e-018
+uc      = 4.6e-013   vsat    = 90000      a0      = 1.2        ags     = 1e-020
+a1      = 0          a2      = 1          b0      = -1e-020    b1      = 0
+keta    = -0.047     dwg     = 0          dwb     = 0          pclm    = 0.55
+pdiblc1 = 0.03       pdiblc2 = 0.0055     pdiblcb = 3.4e-008   drout   = 0.56
+pvag    = 1e-020     delta   = 0.014      pscbe1  = 8.14e+008  pscbe2  = 9.58e-007
+fprout  = 0.2        pdits   = 0.2        pditsd  = 0.23       pditsl  = 2.3e+006
+rsh     = 3          rdsw    = 250        rsw     = 160        rdw     = 160
+rdswmin = 0          rdwmin  = 0          rswmin  = 0          prwg    = 3.22e-008
+prwb    = 6.8e-011   wr      = 1          alpha0  = 0.074      alpha1  = 0.005
+beta0   = 30         agidl   = 0.0002     bgidl   = 2.1e+009   cgidl   = 0.0002
+egidl   = 0.8
+aigbacc = 0.012      bigbacc = 0.0028     cigbacc = 0.002
+nigbacc = 1          aigbinv = 0.014      bigbinv = 0.004      cigbinv = 0.004
+eigbinv = 1.1        nigbinv = 3          aigc    = 0.69       bigc    = 0.0012
+cigc    = 0.0008     aigsd   = 0.0087     bigsd   = 0.0012     cigsd   = 0.0008
+nigc    = 1          poxedge = 1          pigcd   = 1          ntox    = 1
+xrcrg1  = 12         xrcrg2  = 5
+cgso    = 7.43e-010  cgdo    = 7.43e-010  cgbo    = 2.56e-011  cgdl    = 1e-014
+cgsl    = 1e-014     ckappas = 0.5        ckappad = 0.5        acde    = 1
+moin    = 15         noff    = 0.9        voffcv  = 0.02
+kt1     = -0.19      kt1l    = 0          kt2     = -0.052     ute     = -1.5
+ua1     = -1e-009    ub1     = 2e-018     uc1     = 0          prt     = 0
+at      = 33000
```

```
+fnoimod = 1           tnoimod = 0
+jss    = 0.0001      jsws   = 1e-011      jswgs  = 1e-010      njs    = 1
+ijthsfwd= 0.01        ijthsrev= 0.001      bvs    = 10          xjbvs  = 1
+jsd    = 0.0001      jswd   = 1e-011      jswgd  = 1e-010      njd    = 1
+ijthdfwd= 0.01        ijthdrev= 0.001      bvd    = 10          xjbvd  = 1
+pbs    = 1           cjs    = 0.0005      mjs    = 0.5         pbsws  = 1
+cjsws  = 5e-010      mjsws  = 0.33        pbswgs = 1           cjswgs = 3e-010
+mjswgs = 0.33        pbd    = 1           cjd    = 0.0005      mjd    = 0.5
+pbswd  = 1           cjswd  = 5e-010      mjswd  = 0.33        pbswgd = 1
+cjswgd = 5e-010      mjswgd = 0.33        tpb    = 0.005       tcj    = 0.001
+tpbsw  = 0.005       tcjsw  = 0.001       tpbswg = 0.005       tcjswg = 0.001
+xtis   = 3           xtid   = 3
+dmcg   = 5e-006      dmci   = 5e-006      dmdg   = 5e-006      dmcgt  = 6e-007
+dwj    = 4.5e-008    xgw    = 3e-007      xgl    = 4e-008
+rshg   = 0.4         gbmin  = 1e-010      rbpb   = 5           rbpd   = 15
+rbps   = 15          rbdb   = 15          rbsb   = 15          ngcon  = 1
.end
```

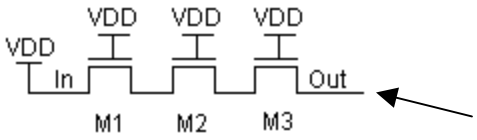


Problem 10.3 **Surendranath .C. Eruvuru**

Using SPICE verify the results of Ex. 10.3.

a)

Ex. 10.3 has been verified using Spice simulations for VDD =1V.

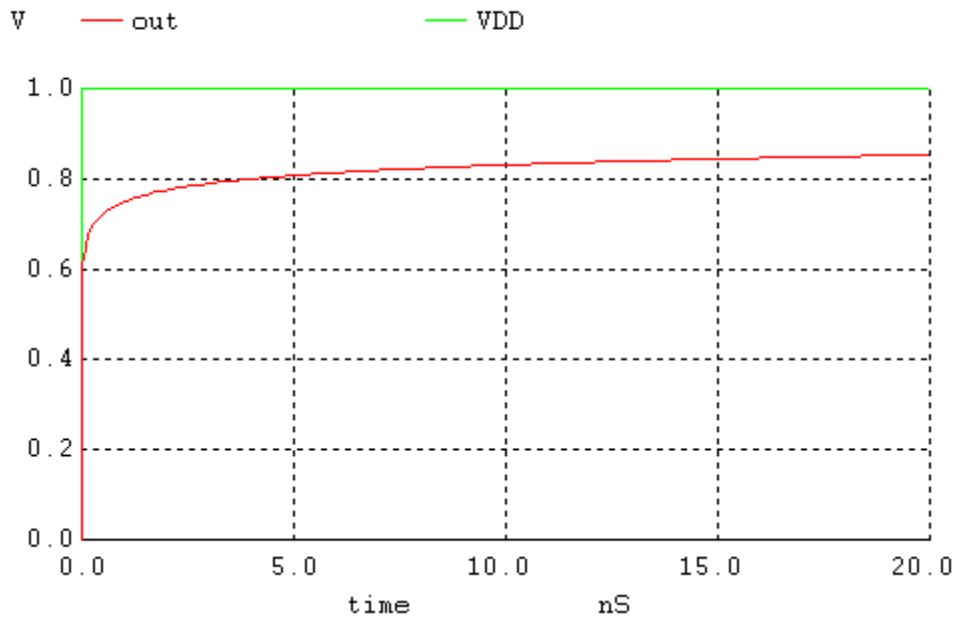


$VDD\text{-}V_{THN}$

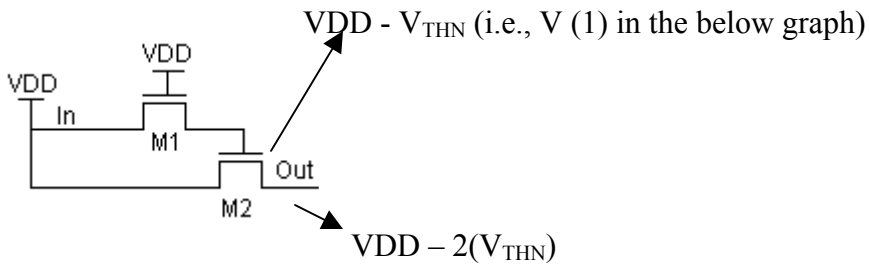
Following is the **Netlist** used for the above circuit.

```
.control
destroy all
run
plot out VDD
.endc
.options scale=50n
.probe
.tran .1n 20n uic
VDD VDD 0 DC 1
M1 VDD VDD 1 0 NMOS L=1 W=10
M2 1 VDD 2 0 NMOS L=1 W=10
M3 2 VDD out 0 NMOS L=1 W=10
```

Simulation:



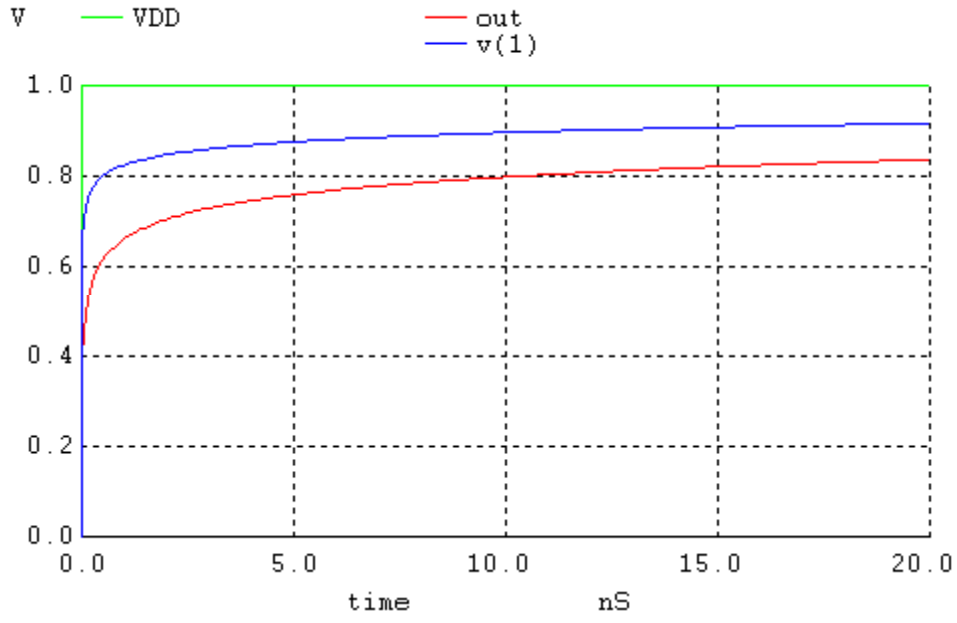
b)
Shown below is the circuit for Ex. 10.3 (b) with VDD=1V.



Following is the **Netlist** used to plot the above graph:

```
.control
destroy all
run
plot out VDD V(1)
.endc
.options scale=50n
.probe
.tran .1n 20n uic
VDD VDD 0 DC 1
M1 VDD VDD 1 0 NMOS L=1 W=10
M2 VDD 1 out 0 NMOS L=1 W=10
```

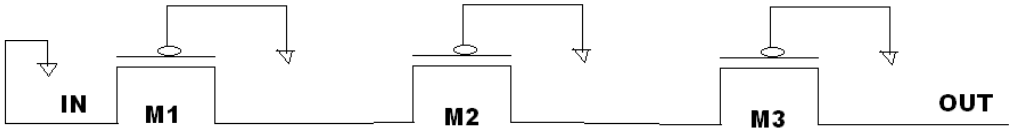
Simulation:



KRISHNAMRAJU KURRA

Problem 10.4: Replacing the NMOS PGs in Fig.10.16 with PMOS and changing the VDD-connected nodes to ground-connected nodes show, and verify with simulations, the outputs of the two modified circuits.

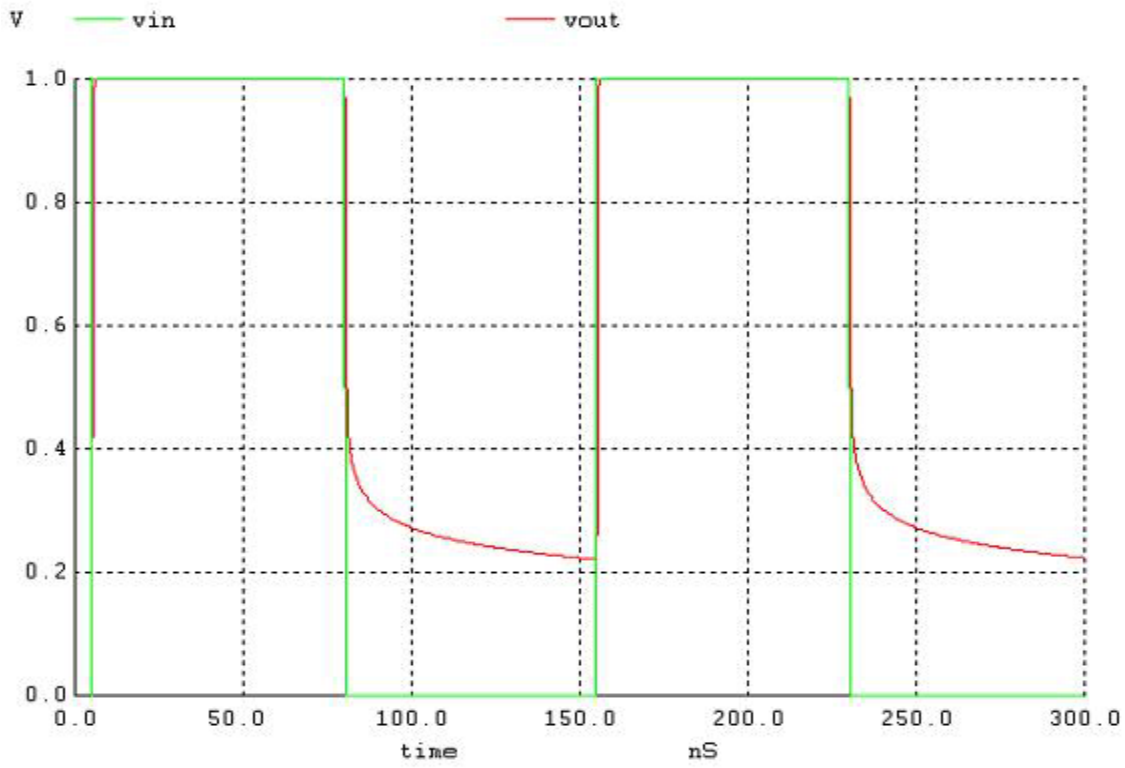
a).



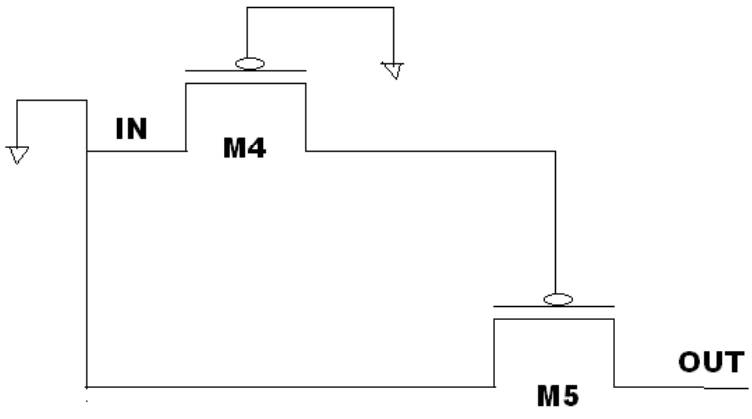
For M1, $V_{SG1} = V_{THP}$, for it to be ON. Since the gates of M2 and M3 are at ground the output of M1 is passed through M2 and M3. The PMOSFETs don't pass the zero, instead they pass V_{THP}. Final output = V_{THP}

*** KRISHNAM-Q:10.4-a ***

```
.control
destroy all
run
plot vout vin ylimit 0 1
.endc
.option scale=50n
.tran 500p 300n 5n UIC

vdd    vdd    0      DC     1
Vin    vin    0      DC     0      pulse 0 1 5n 100p 100p 75n 150n

M1     Vin    0      n1     vdd    PMOS L=1 W=20
M2     n1     0      n2     vdd    PMOS L=1 W=20
M3     n2     0      Vout   vdd    PMOS L=1 W=20

.model  pmos  pmos  level = 14
.end
```



b).

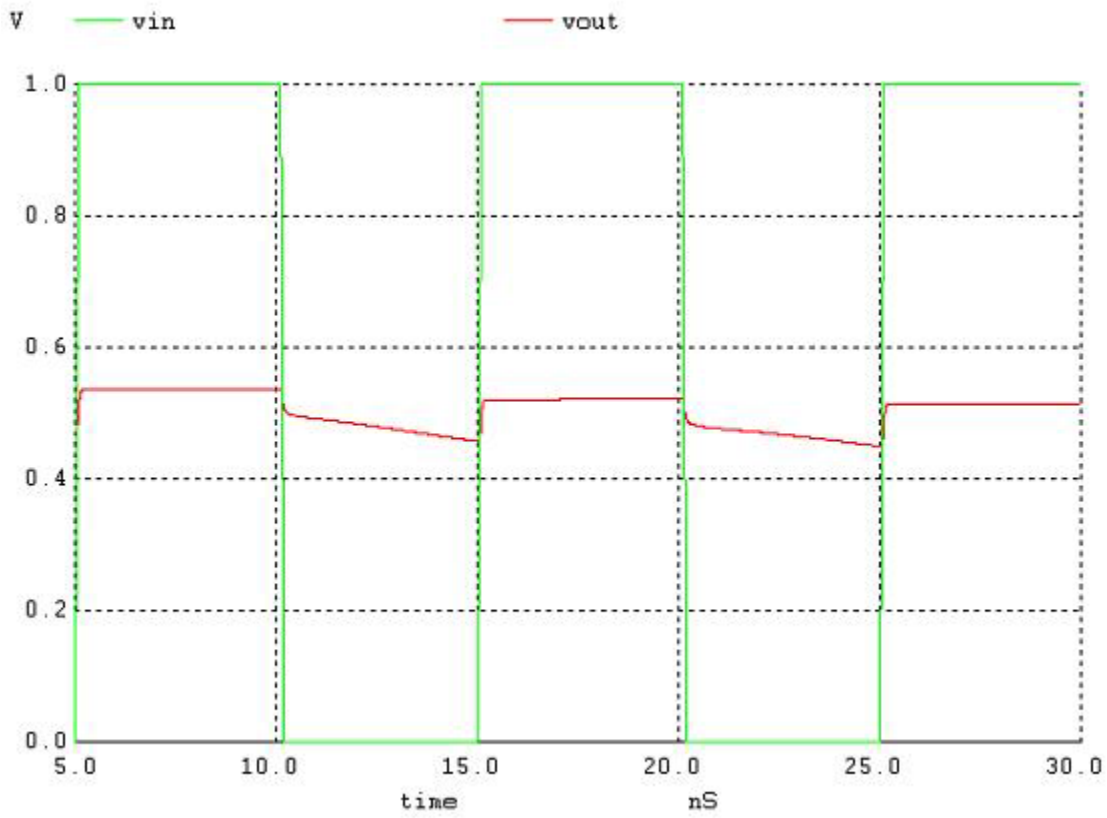


For M4 to be on $V_{S4} = V_{THP,}$ $V_{G5}=V_{THP}$
And for M5 to be on $V_{SG5} = V_{THP}$

$V_{S5} - V_{G5} = V_{THP}$
$V_{S5} = 2\ V_{THP}$
Final Output = $2V_{THP}$

*** KRISHNAM-Q:10.4-b ***

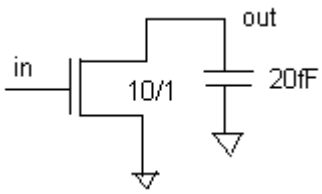
```
.control
destroy all
run
plot vout vin ylimit 0 1
.endc
.option scale=50n
.tran 10p 30n 5n UIC

vdd     vdd     0       DC      1
Vin     vin     0       DC      0       pulse 0 1 5n 100p 100p 5n 10n

M4      vin     0       n5      vdd     PMOS L=1 W=20
M5      vin     n5      vout    vdd     PMOS L=1 W=20

.model  pmos  pmos  level = 14
.end
```



Problem 10.5 **Indira Priyadarshini. Vemula**

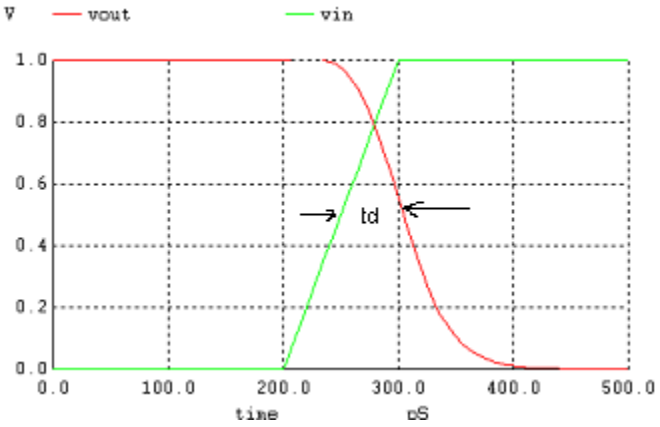
For the following circuits estimate the delay between the input and the output. Use the 50nm (short channel CMOS)process. Verify the estimates with spice?

a)

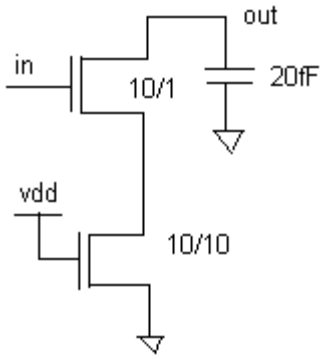


$t_{delay}=0.7*R_n*C_{tot}$
$=0.7*34K/10*(62.5\ aF*10+20\ Ff)$
$=49.08$ ps

```
***PROBLEM 10.5A****
.control
destroy all
run
plot vout vin ylimit 0 1
.endc
.option scale=50n
.ic v(vout)=1
.tran 10p 500p UIC
vin vin 0 dc 0 pulse 0 1 200p 100p
M1 vout vin 0 0 NMOS L=1 W=10
C1 vout 0 20f
**models included
```

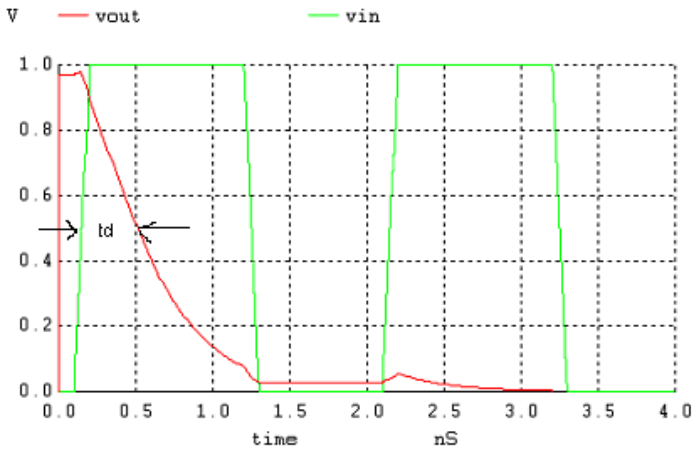


b)



R_n=3.4K+3.4K
=6.8K
t_{delay}=0.7*6.8K*(62.5 Af*10+20 fF)
=98.17 ps

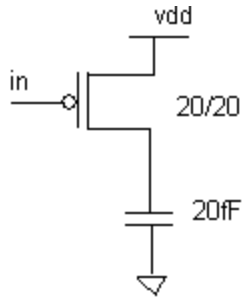
```
***PROBLEM 10.5B****
.control
destroy all
run
plot vout vin ylimit 0 1
.endc
.option scale=50n
.tran 10p 4n UIC
vdd vdd 0 dc 1
vin vin 0 dc 0 pulse 0 1 100p 100p 100p 1n 2n
M1 vout vin n1 0 NMOS L=1  W=10
M2 n1   vdd 0  0 NMOS L=10 W=10
C1 vout 0 20f IC=1
```



**models included

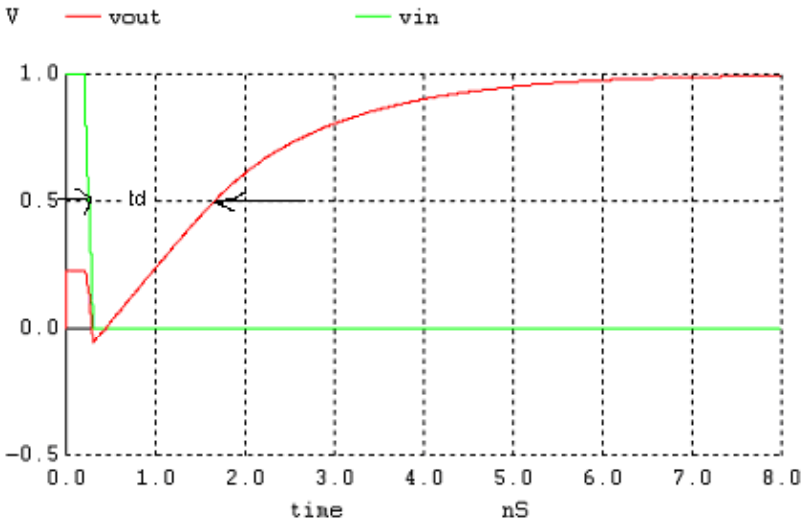
We are doing this problem using short channel process, but here the length of the MOFET is 10 which cause the resistance to increase. This results in increase in time delay when compared to the calculated value.

C)



t_{delay}=0.7*Rp*C_{tot}
=0.7*68K/20(62.5 Af*20*20+20 fF)
=107.1 ps

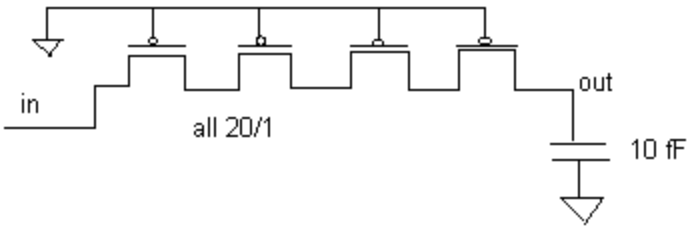
```
***PROBLEM 10.5c****
.control
destroy all
run
plot vout vin
.endc
.option scale=50n
.ic v(vout)=0 v(vin)=1
.tran 10p 8n UIC
vdd vdd 0 dc 1
vin vin 0 dc 0 pulse 1 0 200p 100p
M1 vout vin vdd vdd PMOS L=20  W=20
C1 vout 0 20f
```



**models included

We are doing this problem using short channel process, but here the length of the MOFET is 20 which cause the resistance to increase. This results in increase in time delay when compared to the calculated value.

d)



$t_{delay}=0.35*Rp*C_{ox}*l^2+0.7*Rp*C_L*l$

$=(0.35*3.4K*1.25Ff*16)+(0.7*3.4K*10Ff*4)$

$=119$ ps

```
***PROBLEM 10.5d****
.control
destroy all
run
plot vout vin ylimit 0 1
.endc
.option scale=50n
.tran 10p 12n 5n UIC
vdd vdd 0 dc 1
vin vin 0 dc 0 pulse 0 1 5n 100p 100p 5n 10n
M1 vin 0 n1   vdd PMOS L=1  W=20
M2 n1  0 n2   vdd PMOS L=1  W=20
M3 n2  0 n3   vdd PMOS L=1  W=20
M4 n3  0 vout vdd PMOS L=1  W=20
C1 vout 0 10f
**models included
```