12.1) Design, lay out, and simulate the operation of a CMOS AND gate with a V_{SP} of approximately 500 mV. Use the standard-cell frame discussed in Ch. 4 for the layout.

A CMOS AND gate can be designed using a NAND gate with its output inverted. Therefore, we need a NAND and an Inverter circuit to layout our AND gate.

The switching point of the AND gate will be dominated by the NAND circuit. Since, we are using short-channel process, the NMOS and PMOS can be considered as just resistors. Similar to example 11.3, we can write the switching point equation as:

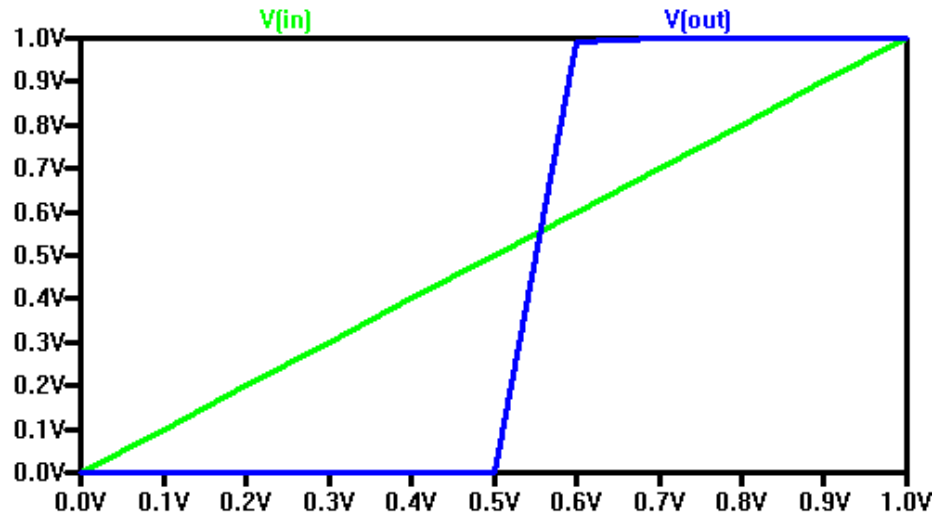$$Vsp = VDD * \left(\frac{Rn + Rn}{(Rn + Rn) + (Rp \text{ // } Rp)} \right).$$
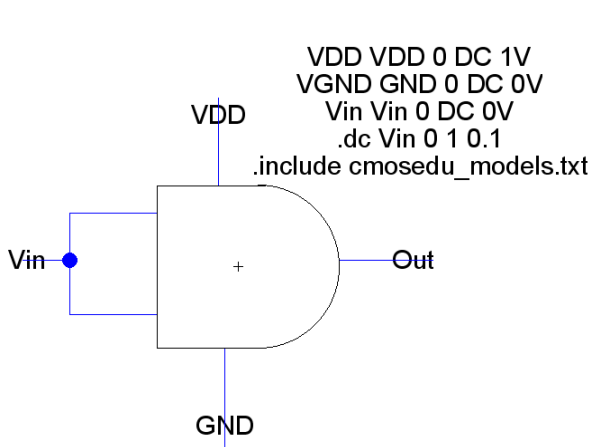
For short-channel, $Rn = \dfrac{34k\Omega}{Wn}$ and $Rp = \dfrac{68k\Omega}{Wp}$, substituting them in the above equation,

we get, $Wn = 2 * Wp$. Choosing the size of NMOS as 10/2 we have the PMOS size as 20/2.
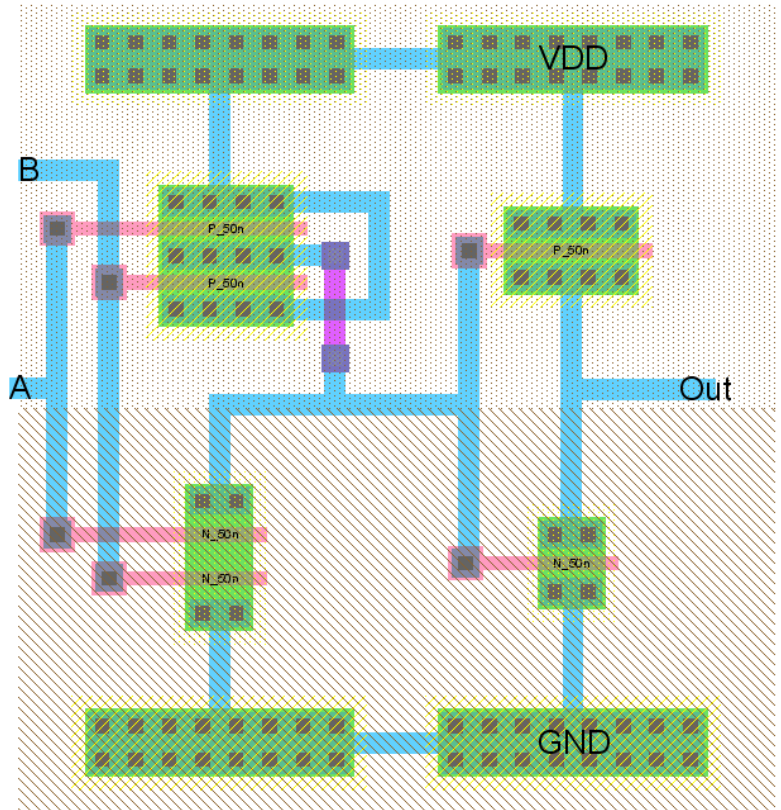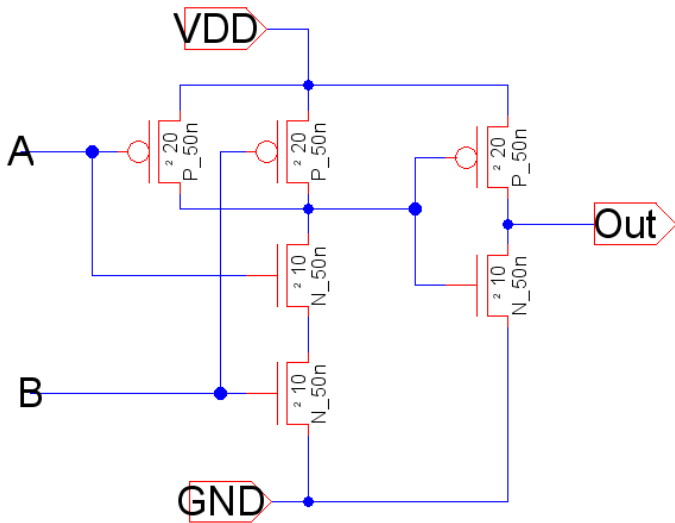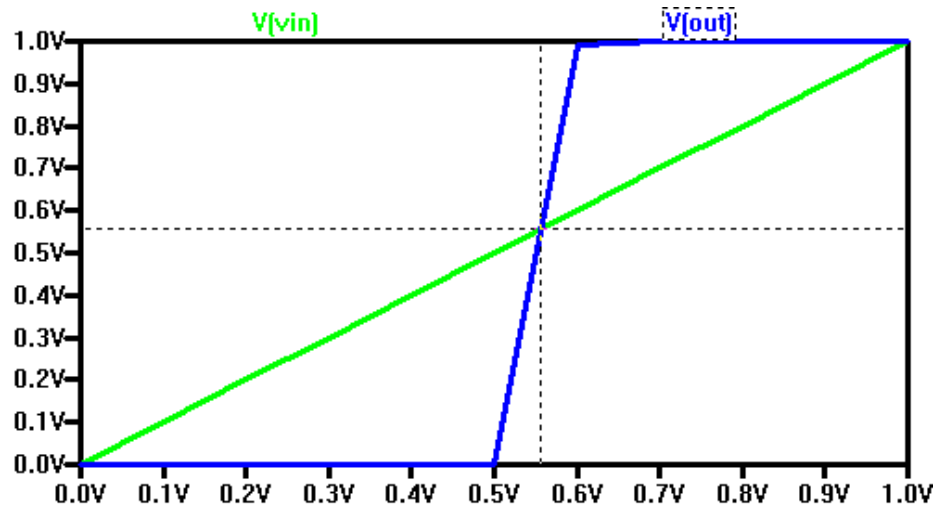

Shown are the circuit Schematic and the Layout of 2-input AND gate using Electric

Simulations Result of Schematic:

```
VDD VDD 0 DC 1V
VGND GND 0 DC 0V
Vin Vin 0 DC 0V
.dc Vin 0 1 0.1
.include cmosedu_models.txt
```


Switching point is measured as 550mV.

Simulations Result of Layout:

```
VDD VDD 0 DC 1V
VGND GND 0 DC 0V
Vin Vin 0 DC 0V
.dc Vin 0 1 0.1
.include cmosedu_models.txt
```
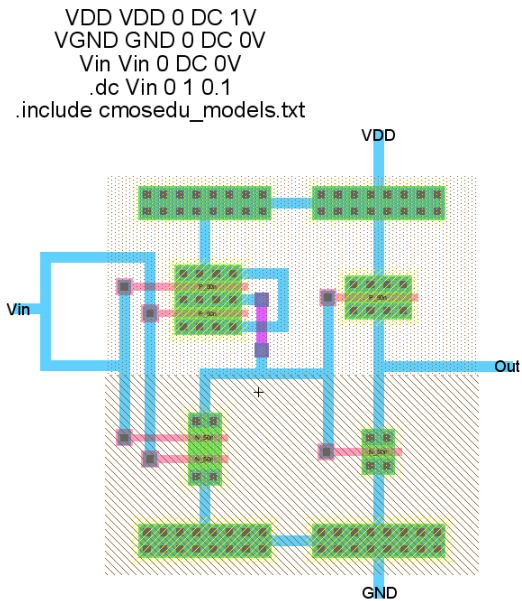

Switching point if found to be 550mV from the above plot, which is comparable to the required 500mV switching-point.

Design and simulate the operation of a CMOS AOI half adder circuit using static logic gates.

Solution: A half adder circuit calculates a half sum (HS) and a carry out (CO). It takes two input bits, A and B. The logic equations for HS and CO are

$$HS = A \oplus B$$
$$CO = A \cdot B = \overline{(\overline{A} + \overline{B})}$$

Figure 1 shows a circuit schematic of a half adder's components. For clarity, the components are not wired together in the figure. The SPICE simulation and code appear on the next page.
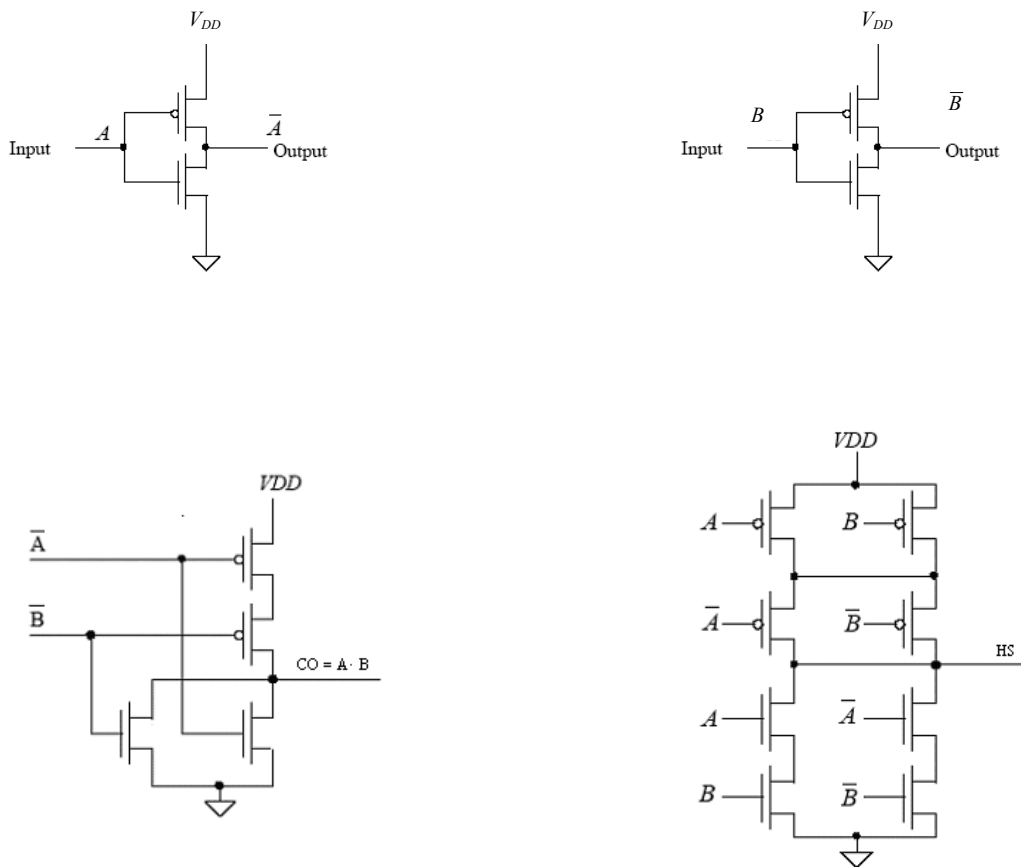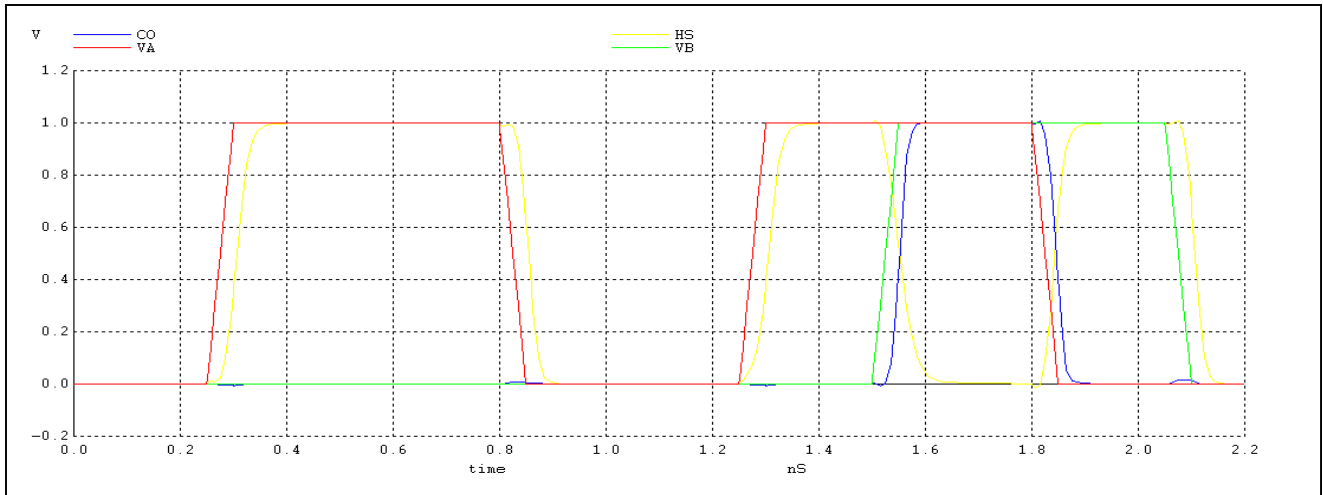

Figure 1: Half adder components

*** Problem 12.2 ***

.control
destroy all
run
plot VA VB CO HS
.endc

.option scale=50n
.tran 10p 2.2n

```
Vdd     Vdd     0           DC      1
VA      VA      0           DC      0       pulse 0 1 250p 50p 50p 0.5n 1n
VB      VB      0           DC      0       pulse 0 1 1.5n 50p 50p 0.5n 1n

*XOR gate -- A XOR B = HS
M12     N3      VB      Vdd     Vdd     PMOS L=1 W=20
M11     HS      B_      N3      Vdd     PMOS L=1 W=20

M10     N3      VA      Vdd     Vdd     PMOS L=1 W=20
M9      HS      A_      N3      Vdd     PMOS L=1 W=20

M8      HS      A_      N2      0       NMOS L=1 W=10
M7      N2      B_      0       0       NMOS L=1 W=10

M6      HS      VA      N1      0       NMOS L=1 W=10
M5      N1      VB      0       0       NMOS L=1 W=10

*A inverter
M2      A_      VA      Vdd     Vdd     PMOS L=1 W=20
M1      A_      VA      0       0       NMOS L=1 W=10

*B inverter
M4      B_      VB      Vdd     Vdd     PMOS L=1 W=20
M3      B_      VB      0       0       NMOS L=1 W=10

*NOR gate -- A_ NOR B_ = AB = CO
M16     N4      A_      Vdd     Vdd     PMOS L=1 W=20
M15     CO      B_      N4      Vdd     PMOS L=1 W=20
M14     CO      B_      0       0       NMOS L=1 W=10
M13     CO      A_      0       0       NMOS L=1 W=10
```

.MODEL NMOS NMOS LEVEL = 14
.MODEL PMOS PMOS LEVEL = 14

.end

Repeat Ex 12.3 for a three-input NOR gate (Use the effective resistances to estimate Vsp)

Ex 12.3 Estimate the intrinsic propagation delays $t_{PHL} + t_{PLH}$, of a three input NAND gate made using 10/1 NMOS and 20/1 PMOS in a short channel process. Estimate and simulate the delay when the gate is driving a load capacitance of 50fF. Assume that inputs are tied together.

Solution:
For a 3 input NOR when it goes from high to low the load is charged through 3 NMOS is parallel and when output goes from low to high it has 3 PMOS resistances in series, So

$$t_{PHL} = 0.7 \frac{R_n}{3} (3.C_{outn} + \frac{C_{outp}}{3} + C_{load})$$

$$t_{PLH} = 0.7.3.R_p (3.C_{outn} + \frac{C_{outp}}{3} + C_{load}) + 0.35 R_p C_{oxp}.3^2$$

Using the values of resistances and capacitances for a short channel process from table 10.2

$$t_{PHL} = 0.7 \frac{3.4k}{3} (3.0.625 fF + \frac{1.25 fF}{3} + 50 fF) = 41.4 ps$$

$$t_{PLH} = 0.7.3.3.4k(3.0.625 fF + \frac{1.25 fF}{3} + 50 fF) + 0.35.3.4k.1.25 fF.3^2 = 386.7 ps$$

delay = 41.4+386.7=428.1ps

Vsp can vary from $\dfrac{3.R_p}{3.R_p + \dfrac{R_n}{3}}$ to $\dfrac{3.R_p}{3.R_p + R_n}$ ie 900mV to 750mV

*** Sol 12.3 ***

```
.control
destroy all
run
plot vin out ylimit 0 1
.endc

.option scale=50n
.tran 10p 2n 10p

vdd     vdd    0       DC     1
Vin     vin    0       DC     0        pulse   0 1 200p 0 0 0.5n 4n

x1      vin    vin     vin     out     vdd     NOR_3
```
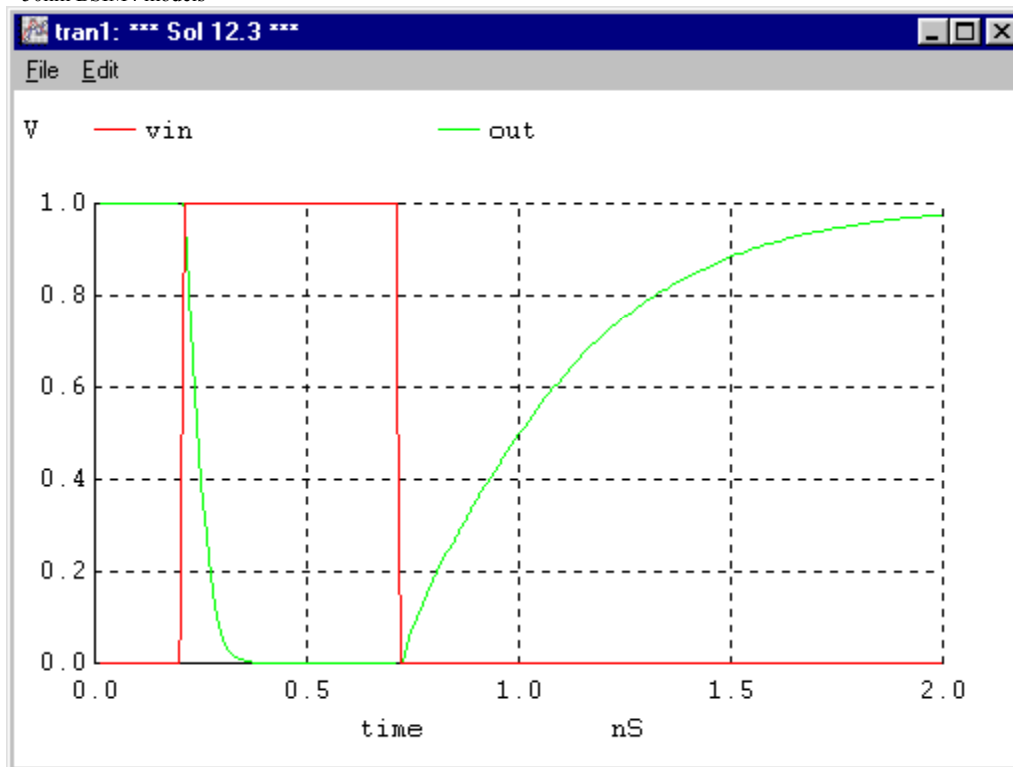
```
cl      out     0       50f

.subckt NOR_3          A       B       C       out     VDD
M1      n1      A       VDD     VDD     PMOS L=1 W=20
M2      n2      B       n1      VDD     PMOS L=1 W=20
M3      out     C       n2      VDD     PMOS L=1 W=20
M4      out     A       0       0       NMOS L=1 W=10
M5      out     B       0       0       NMOS L=1 W=10
M6      out     C       0       0       NMOS L=1 W=10
.ends
```
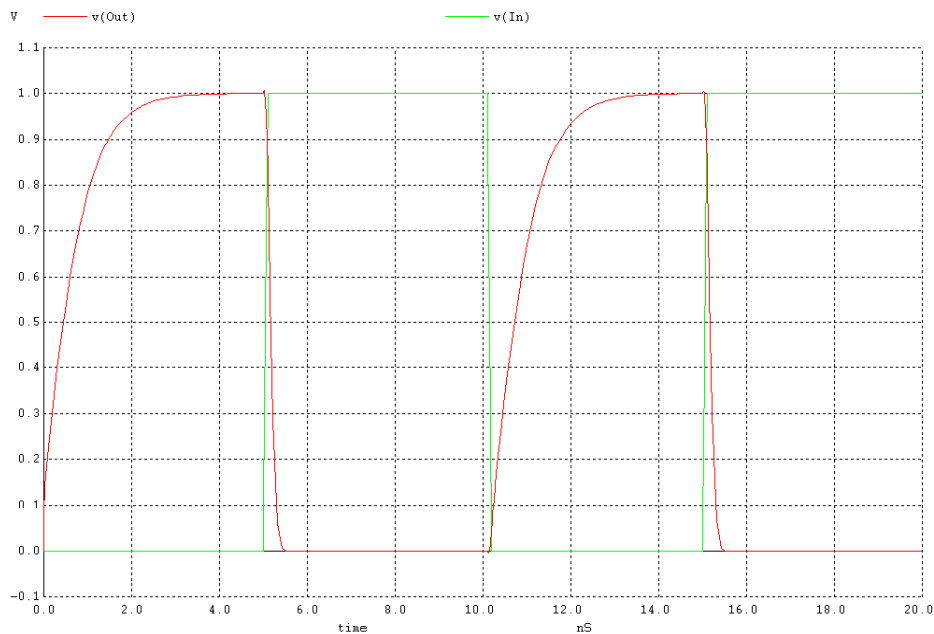
* 50nm BSIM4 models

Repeat Ex. 12.4 for a three-input NOR gate. (Use the effective resistances to estimate the V_{SP})

Solution:

$t_{PHL} = 0.7 \ (R_n)(C_{load})$
$t_{PHL} = 0.7 \ (3.4K)(50fF)$
$t_{PHL} = 119ps$

$t_{PLH} = 0.7 \ (N)(R_n)(C_{load})$
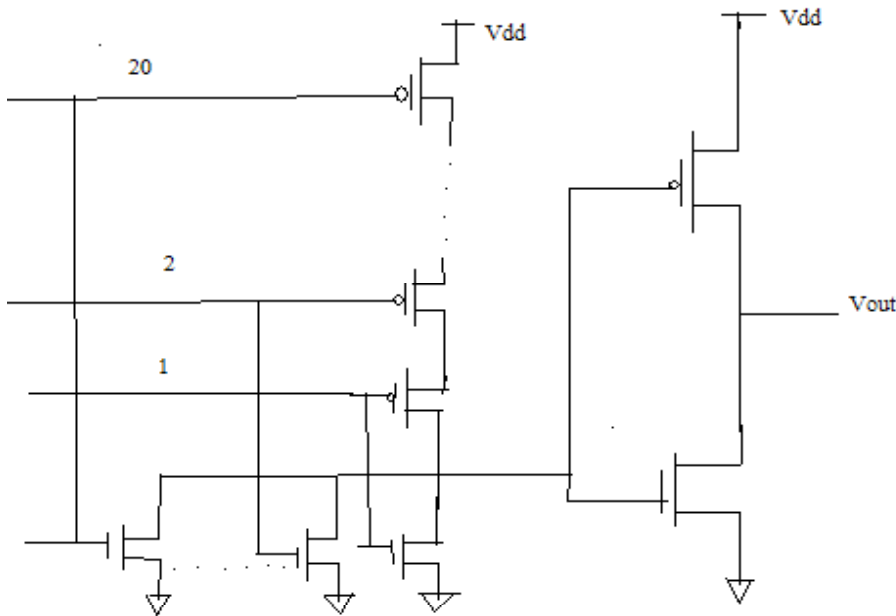$t_{PLH} = 0.7 \ (3)(3.4K)(50fF)$
$t_{PLH} = 357ps$

Simulations Results

$t_{PHL} = 118ps$ (Which is equal to hand calculations)

$t_{PLH} = 566ps$ (Considerably longer Since single NMOS device is pulling the output high.

12.5 Sketch the schematic of an OR gate with 20 inputs. Comment on your design.

OR gate with 20 inputs can be drawn with a 20 input NOR gate and inverter as shown

In this case there are 20 PMOS in series in the NOR gate. Hence low to high propagation delay of the NOR gate is high.

(In case of equal sized NMOS and PMOS devices, $R_p > R_n$ and here the PMOS are in series. Hence here t_{pLH} of NOR gate is very high. Also here the delay t_{pLH} of NOR gate increases as the square of N, where N is number of inputs which are 20.)

Also 21 PMOS and 21 NMOS including the inverter for a total of 42 Mosfets are needed.

Hence above schematic is hard to implement.

So the following schematic can be used which again uses a 20 input NOR gate and an inverter.
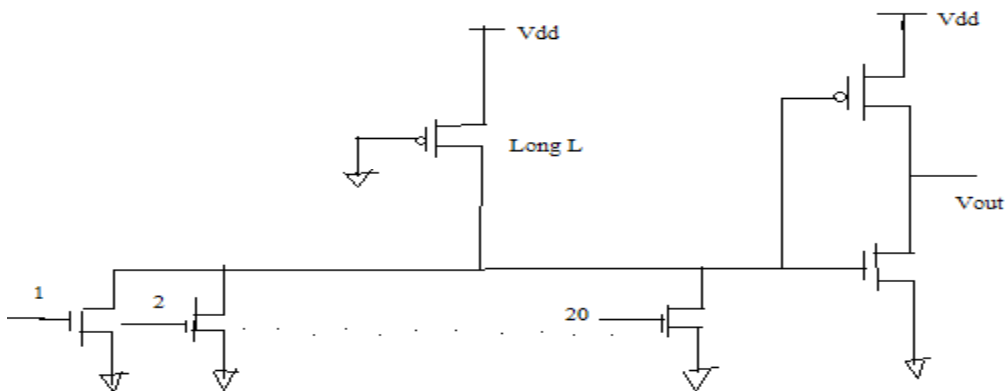
Here also the low to high propagation delay of the NOR gate would be considerably high due to the large resistance of the long length pull up device and also due to the large output capacitance of the parallel NMOS. But here only 23 Mosfets are needed.

In order to ensure that the output of the NOR gate gets pulled low enough (V_{OL}=0), the resistance of the Long L PMOS has to be atleast four times the resistance of the NMOS in the NOR gate.

For the simulation shown below, the size of all NMOS devices in the NOR gate has been taken as 10/1, the size of long L PMOS in the NOR gate has been taken as 20/10, the size of NMOS in the inverter is 10/1 and size of PMOS in the inverter is 20/1.
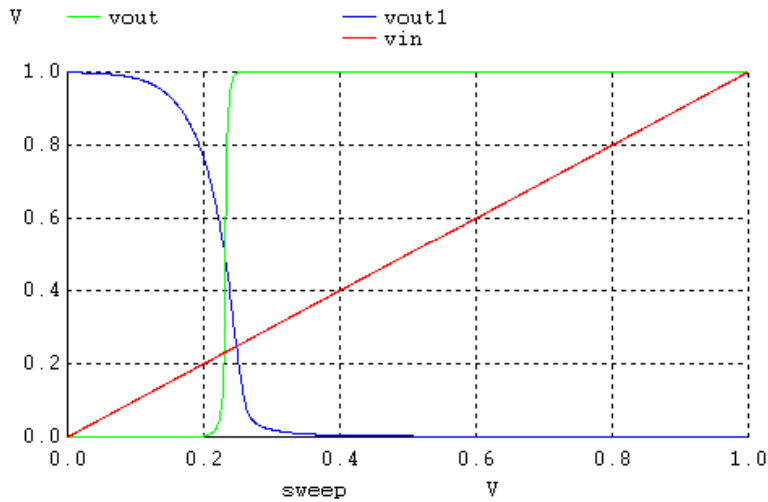
Thus by using a long value for L in the PMOS, the output vout1 of the NOR gate is pulled to zero as seen in the simulation.

Sketch the schematic of a static logic gate that implements $(A+B.\overline{C}).D$. Estimate the worst case delay delay through the gate when driving a 50fF load capacitance?

Solution:

$$Z=(A+B.\overline{C}).D$$

$$\overline{Z}=\overline{(A+B.\overline{C}).D}$$

$$\overline{Z}=\overline{A}.(\overline{B}+C)+\overline{D}$$

$$\overline{\overline{Z}}=\overline{\overline{A}.(\overline{B}+C)+\overline{D}}$$

$$Z=\overline{\overline{A}.(\overline{B}+C)+\overline{D}}$$

which is also equal to $(A+B.C).D$

PMOS=20/1   NMOS=10/1

$C_{OUT}=2/3C_{OXN} + C_{OXN} + 3/5C_{OXP} + C_{LOAD}$

$C_{OUT}=2/3(0.625Ff) + 0.625Ff + 3/5(1.25Ff) + 50Ff$
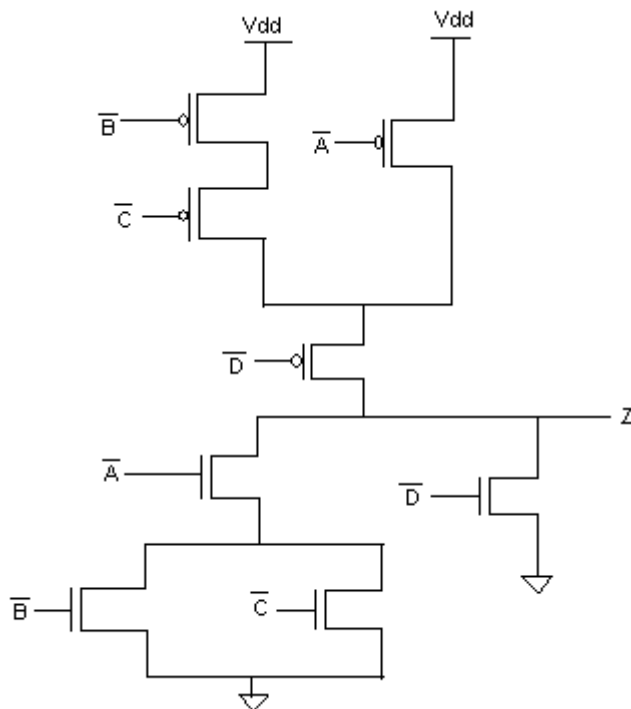
$C_{OUT}=51.78Ff$

Worst-case delay is when all the $\overline{B}$, $\overline{C}$ and $\overline{D}$ (PMOS) are ON. We will have three resistors in series. Therefore we get,

$3R_p=3(68K/20)$

$=10.2K$

$t_{PLH}=0.7*10.2K*51.78Ff$

$t_{PLH}=369.7ps$

KRISHNAMRAJU KURRA

PROBLEM 12.7
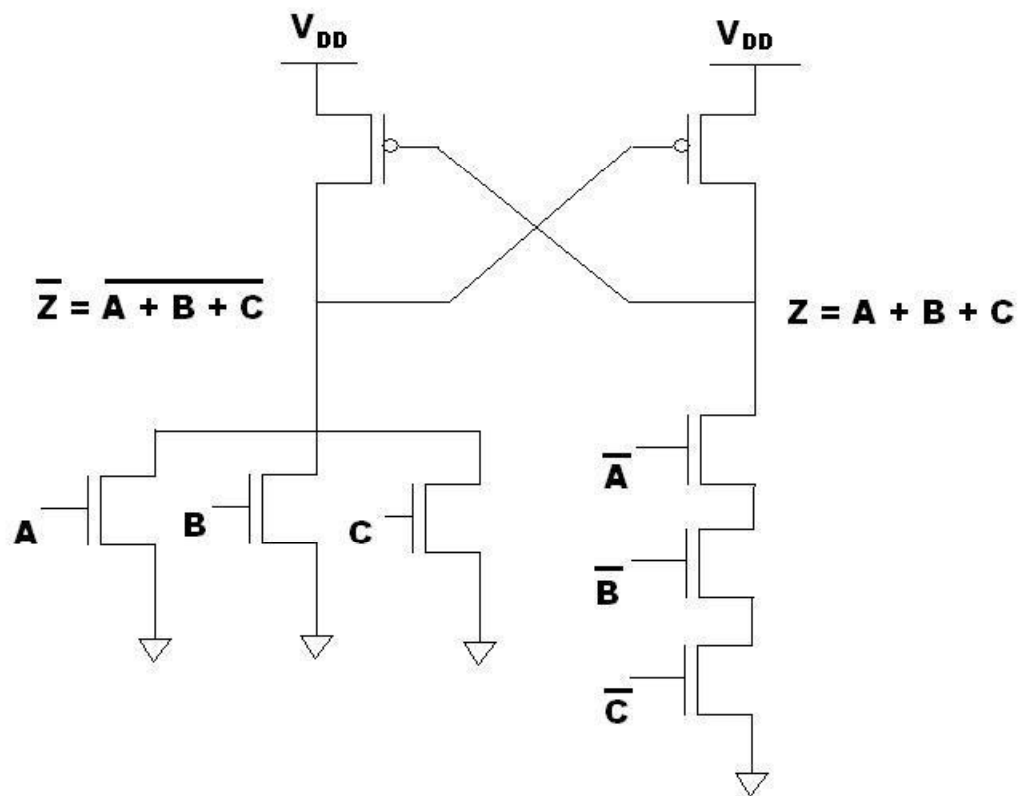**Design and simulate the operation of a CVSL OR gate made with minimum size devices.**

```
*** KRISHNAM Q:12.7 ***
.control
destroy all
run
plot vA VB+1 VC+2 vout+3
plot vAI vBI+1 VCI+2 VIN+3
.endc
.option scale=50n
.tran 110P 40n
vdd     vdd    0       DC      1
VA      vA     0       DC      0       pulse   0 1 200p 0 0 5n 10n
VB      vB     0       DC      0       pulse   0 1 200p 0 0 10n 20n
VC      vC     0       DC      0       pulse   0 1 200p 0 0 15n 30n
VAI     vAI    0       DC      0       pulse   1 0 200p 0 0 5n 10n
VBI     vBI    0       DC      0       pulse   1 0 200p 0 0 10n 20n
VCI     vCI    0       DC      0       pulse   1 0 200p 0 0 15n 30n
x1      vA     vB      vC      vIN     vdd     NOR_31
x2      vAI    vBI     vCI     vout    vdd     NOR_32
.subckt NOR_31   A      B       C       vout1   VDD
M4      vout1  A       0       0       NMOS L=1 W=10
M5      vout1  B       0       0       NMOS L=1 W=10
M6      vout1  C       0       0       NMOS L=1 W=10
.ends
.subckt NOR_32   A      B       C       vout2   VDD
M1      vout2  A       n1      0       NMOS L=1 W=10
M2      n1     B       n2      0       NMOS L=1 W=10
M3      n2     C       0       0       NMOS L=1 W=10
.ends
M7      vout   vIN     VDD     VDD     PMOS L=2 W=20
M8      vIN    vOUT    VDD     VDD     PMOS L=2 W=20

.model  nmos nmos  level = 14
.end
```

By using minimum size devices the output was being pulled by the PMOS devices to high before it reached zero. The out put can be pulled down to zero by increasing the strength of the NMOS(increase width of NMOS)or by decreasing the strength of the PMOS(increase length of PMOS).
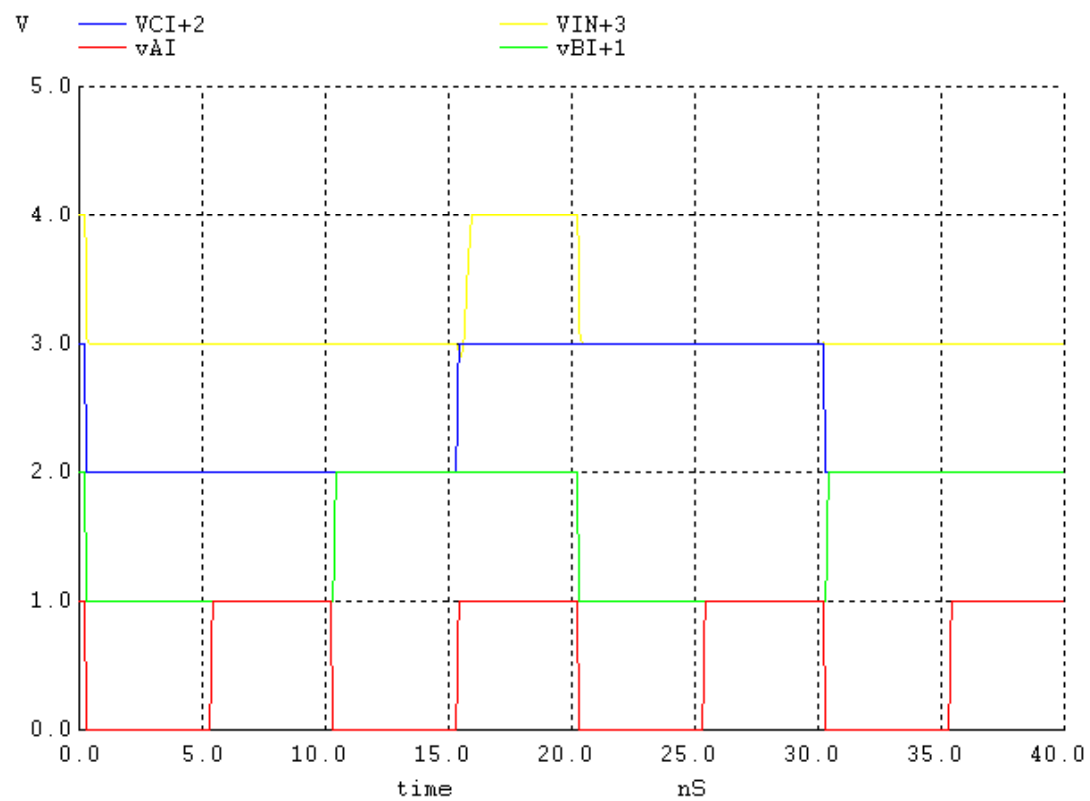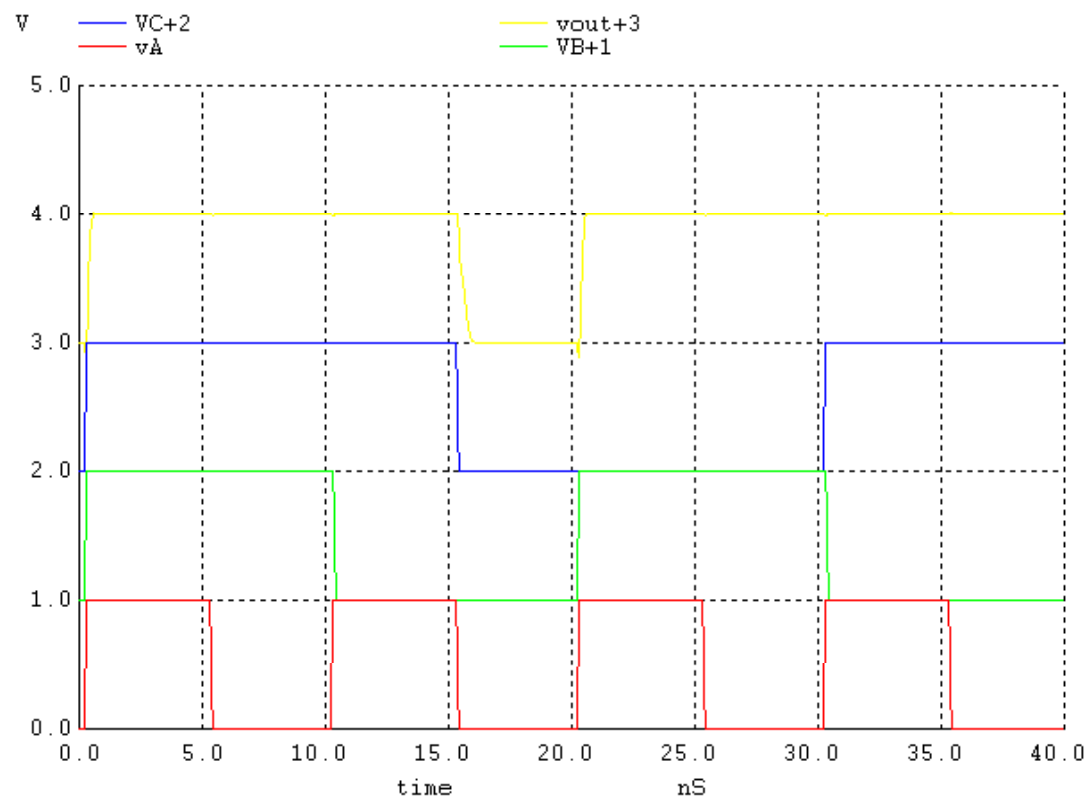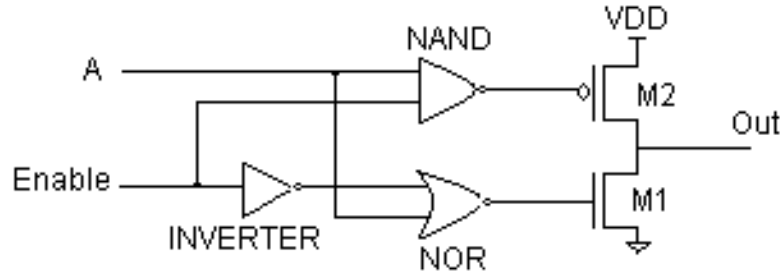
$$\overline{Z} = \overline{A + B + C}$$

$$Z = A + B + C$$

$$\overline{A}$$

$$\overline{B}$$

$$\overline{C}$$

【CVSL OR gate Schematic】

Design and simulate the operation of a tri-state buffer that has propagation delays under 5ns when driving a 1 pF load. Assume that the maximum input capacitance of the buffer is 100fF.

In tri – state buffer if *enable* is low, then the output will be high impedance state. If *enable* is high, then the output will have the same logic value as A. According to the question, input capacitance can't exceed 100fF. So, the total input capacitance can be written as follows:

$$C_{in} = 3/2(\underline{C_{ox,n} + C_{ox,p}} + \underline{C_{ox,n} + C_{ox,p}}) = 100fF$$
$$\qquad\qquad\quad \text{Inverter} \qquad\quad \text{NAND}$$

We know that C_{ox} = .0625fF. So,

$$100fF > 3\ (C_{ox}\ (W_n\ L_n + W_p\ L_p\ ))$$

To solve the above inequality, considering $W_n = 2W_p$ & $L_n = L_p$, we can obtain a better result than any other assumption in short channel process.

After solving,
$$W_n\ L_n \sim 178\ \&\ W_p\ L_p \sim 356.$$

Approximating above values in the following net list, a Tri-state buffer that has propagation delay under 5ns has been obtained.

Net list:

.CONTROL
DESTROY ALL
RUN
Plot V(A) V(out)

.ENDC

.option scale=50n
.tran .1n 50n UIC
*.IC V(BOUT)=1

VDD	Vdd	0	DC	1	
VA	A	0	DC	0	PULSE 0 1 0 0.1n 0.1n 10n 20n
VEn	En	0	DC	1	

XNand	A	En	Vdd	1	Nand
XNor 3	A	Vdd	2	Nor	
XINV En	3	Vdd	INV		
M1	out	1	Vdd	Vdd	PMOS L=1 W=20
M2	out	2	0	0	NMOS L=1 W=10

C1	out	0	1p

*****SUBCKT 1******
.SUBCKT   INV in1   out1   Vdd
M1   out1 in1   Vdd Vdd PMOS L=1 W=20
M2   out1 in1   0   0   NMOS L=1 W=10
.ENDS

*****SUBCKT 2 ******
.SUBCKT   Nand A   B   Vdd   out
M1   1   B   0   0   NMOS L=5 W=40
M2   out   A   1   0   NMOS L=5 W=40
M3   out   A   Vdd   Vdd   PMOS L=5 W=80

M4   out   B   Vdd   Vdd   PMOS L=5 W=80

.ENDS

*****SUBCKT 3 ******
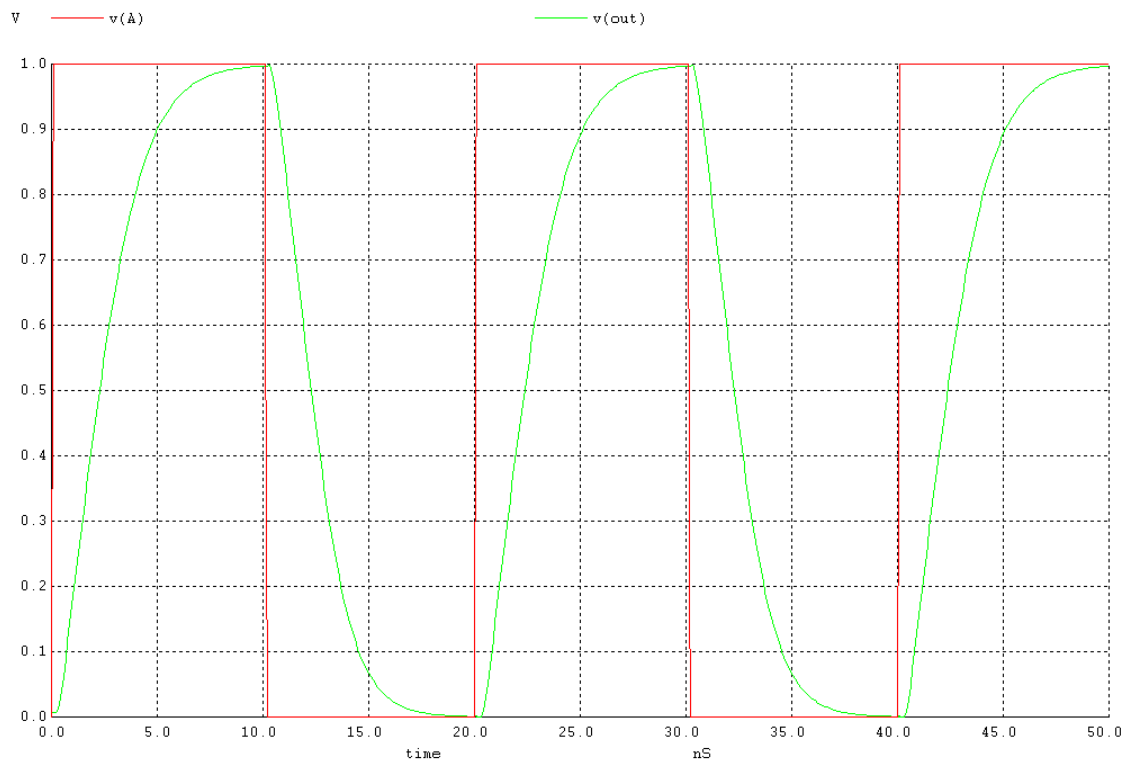.SUBCKT   Nor   A   B   Vdd   out
M1   out   B   0   0   NMOS L=5 W=40
M2   out   A   0   0   NMOS L=5 W=40
M3   1   A   Vdd   Vdd   PMOS L=5 W=80
M4   out   B   1   Vdd   PMOS L=5 W=80
.ENDS

.model nmos nmos Level=14
.model pmos pmos Level=14

Delay from simulation:

$T_{PHL} = 2.1$ns
$T_{PLH} = 2.3$ns

Sketch the schematic of a three-input XOR gate implemented in AOI logic.

The truth table for the three-input XOR gate is as follows:

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

By applying Boolean math, an AOI logic function can be developed. (See Below.)

$$Z = A \oplus B \oplus C = A \bullet \bar{B} \bullet \bar{C} + B \bullet \bar{A} \bullet \bar{C} + C \bullet \bar{A} \bullet \bar{B}$$

$$\bar{Z} = (\bar{A} + B + C) \bullet (\bar{B} + A + C) \bullet (\bar{C} + A + B)$$

$$Z = \overline{(\bar{A} + B + C) \bullet (\bar{B} + A + C) \bullet (\bar{C} + A + B)}$$

$$Z = \overline{(\bar{A} + B + C)} \bullet \overline{(\bar{B} + A + C)} \bullet \overline{(\bar{C} + A + B)}$$

$$Z = \overline{(\bar{A} + B + C)} + \overline{(\bar{B} + A + C)} + \overline{(\bar{C} + A + B)}$$

The schematic can then be drawn as shown below.
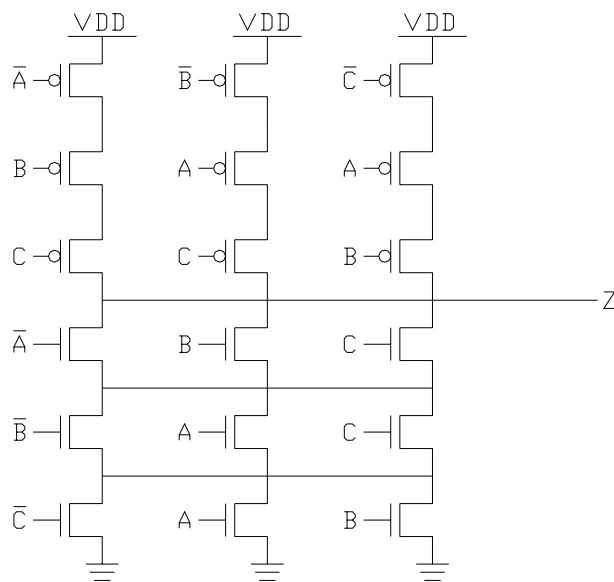
The circuit shown in Fig. 12.27 is an edge detector. Discuss and simulate the operation of the circuit.

Xor gate gives us logic 1 out any time we have 2 different signals at the input of the gate (logic 1 and logic 0). Other logic combination inputs gives us output of logic 1. So if we have same inputs just one delayed then for the time of the delay inputs are going to be different whenever input signal changes for 0 to 1 (rising edge) or from 1 to 0 (falling edge). Basically, we generate pulse at each edge with the width of the delay at the input signals.
Figure bellow shows simulation of the circuit in Fig. 12.27. Input signals was delayed with 8 stage buffers that gave about 200 psec delays. Simulation shows that we generated pulse at output at each edge of input signal with the width of about 200 psec.
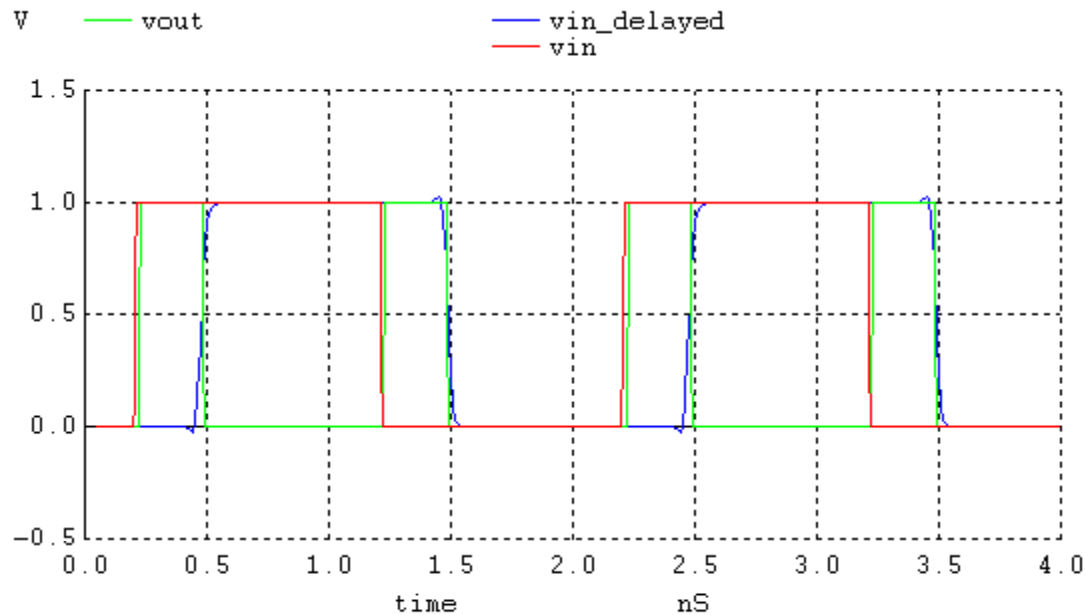
```
.control
destroy all
run
plot vin vout vin_delayed
.endc

.option scale=50n
.tran 10p 4n 50p

vdd     vdd     0       DC      1
Vin     vin     0       DC      0       pulse   0 1 0.2n 10p 10p 1n 2n

x1      vin     vin_delayed     out     vdd     Xor_2

X2      vin     vin1    VDD     inverter
X3      vin1    vin2    VDD     inverter
X4      vin2    vin3    VDD     inverter
X5      vin3    vin4    VDD     inverter
X6      vin4    vin5    VDD     inverter
X7      vin5    vin6    VDD     inverter
X8      vin6    vin7    VDD     inverter
X9      vin7    vin_delayed     VDD     inverter
.subckt inverter        in      out     VDD
M1      out     in      0       0       NMOS L=1 W=10
M2      out     in      VDD     VDD     PMOS L=1 W=20
.ends

.subckt Xor_2 A         B       out     vdd
xx1     A       notA    VDD     inverter
xx2     B       notB    VDD     inverter
M1      P3      B       0       0       NMOS L=1 W=10
M2      out     A       p3      p3      NMOS L=1 W=10
M3      P4      notB    0       0       NMOS L=1 W=10
M4      out     notA    p3      p3      NMOS L=1 W=10

M5      out     notA    p1      p1      PMOS L=1 W=20
M6      p1      A       vdd     VDD     PMOS L=1 W=20
M7      out     notB    P1      p1      PMOS L=1 W=20
M8      p1      B       vdd     VDD     PMOS L=1 W=20
.ends
```