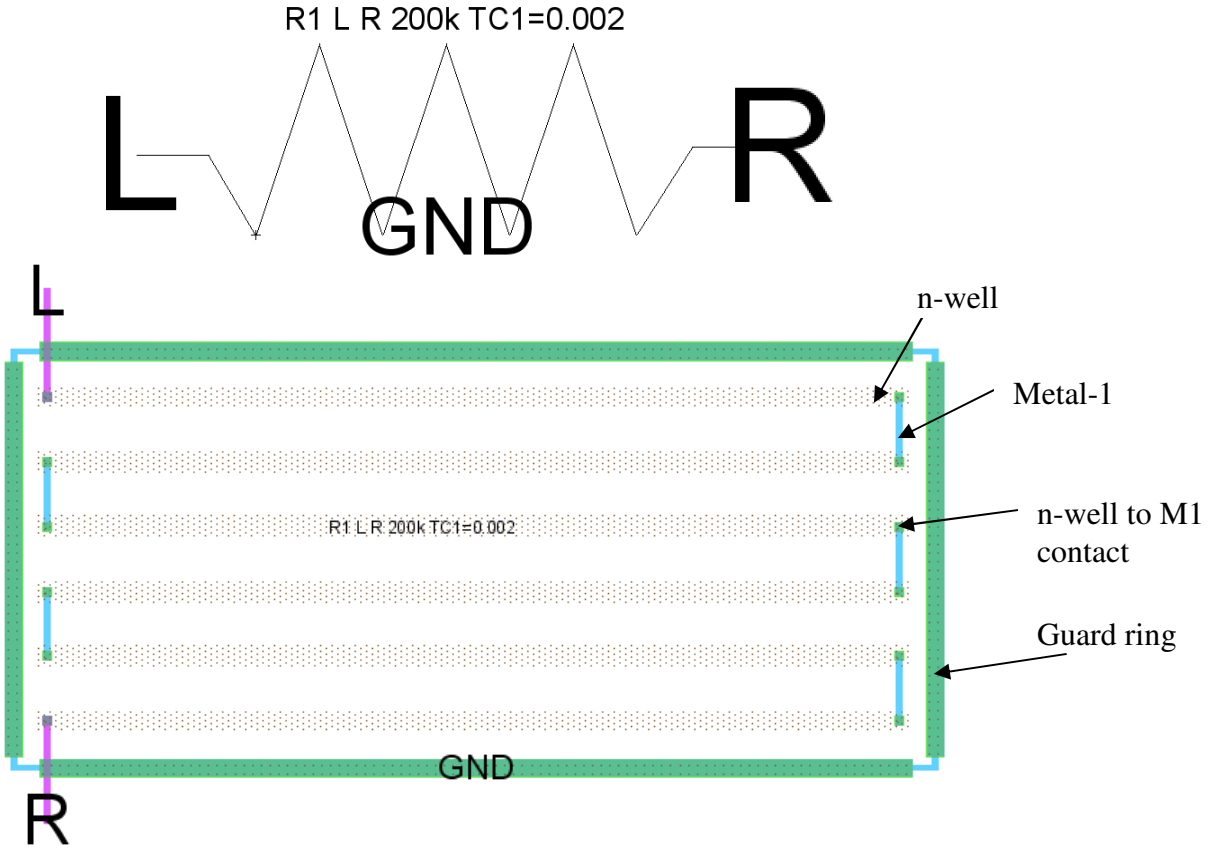
4.1) Lay out a nominally 200 kΩ resistor with metal1 wire connections. DRC your layout. What would happen if the layout did not include n+ under the contacts? Use the sheet resistances from Table 4.1.

The sheet resistance for a n-well from Table 4.1 is 500Ω/□. The total resistance is calculated by, $R = Rs * \frac{L}{W}$. Using R=200k, Rs=500 and W = 12 (min) we get L =4800. We can layout 6 resistors with a width of 12 and length of 800 in series to make a total length of 4800 and total resistance of 200kΩ.



A guard ring is included around the n-well resistor, to reduce the substrate noise affecting the resistance of the n-well resistor. The guard ring is made up of p-well to metal contacts and it is connected to ground.

If the n+ is not included under the contacts, then the metal-1 is directly connected to the n-well, this forms a rectifying contact or a Schottky diode. Unless we need a schottky diode, one should never connect metal directly to the substrate or a well.

Vinay Dindi

4.2) Sketch the cross-sectional view along the line indicated in Fig 4.x.

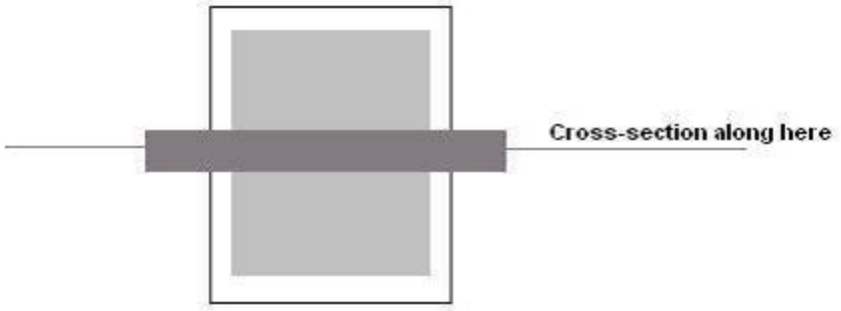
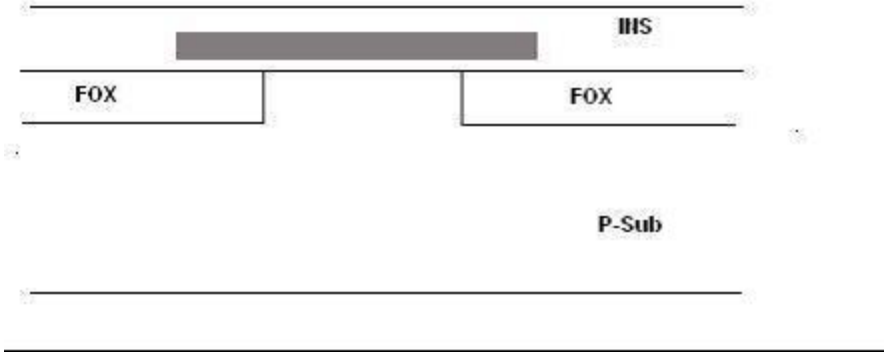


Fig 4.x Layout used in problem 4.2



Problem 4.3 **Satish Dulam**

<u>Question</u>: Sketch the cross-sectional views across the VDD and GROUND power buses in the standard cell frame in Figure 4.15.

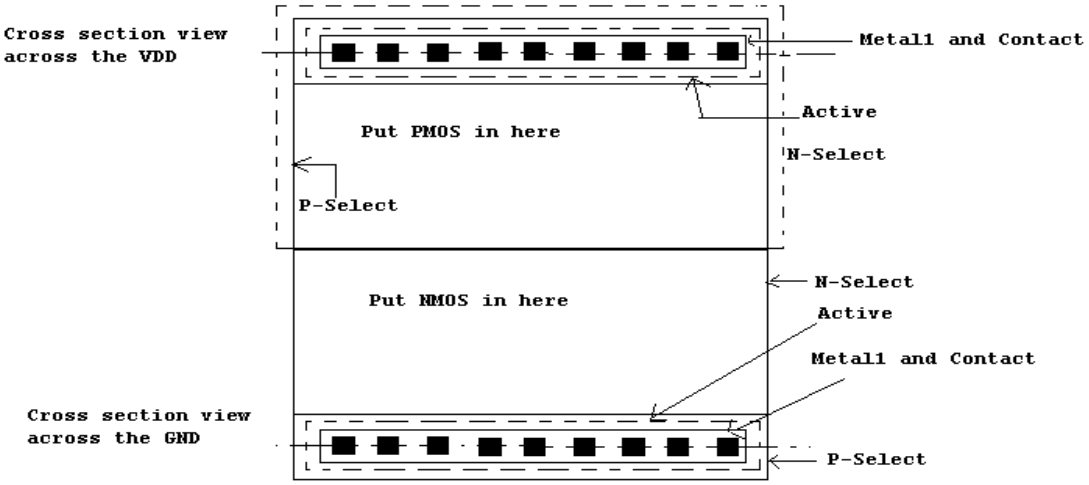
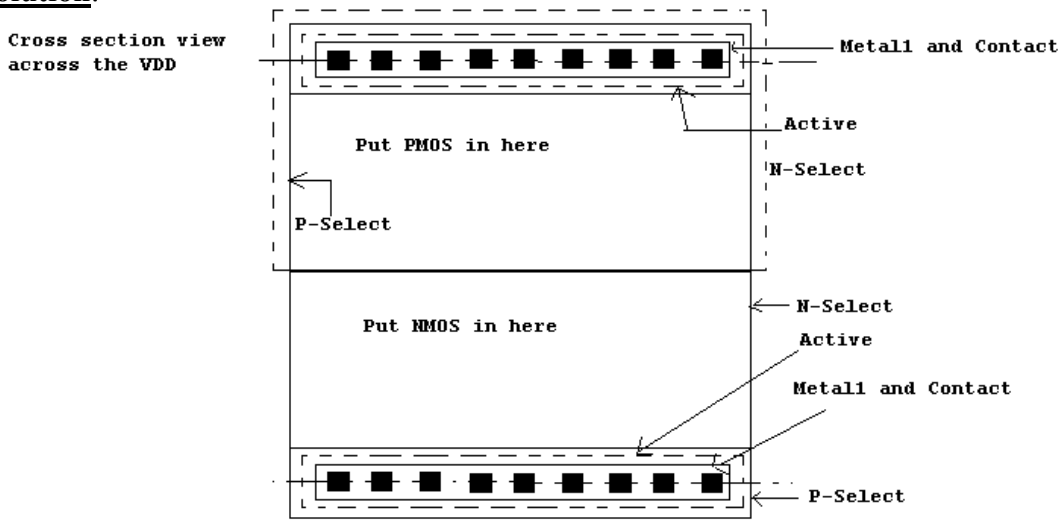
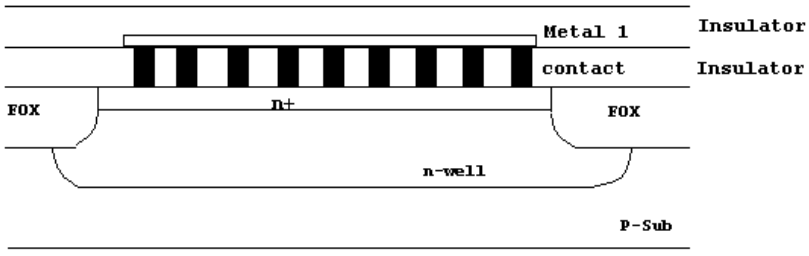


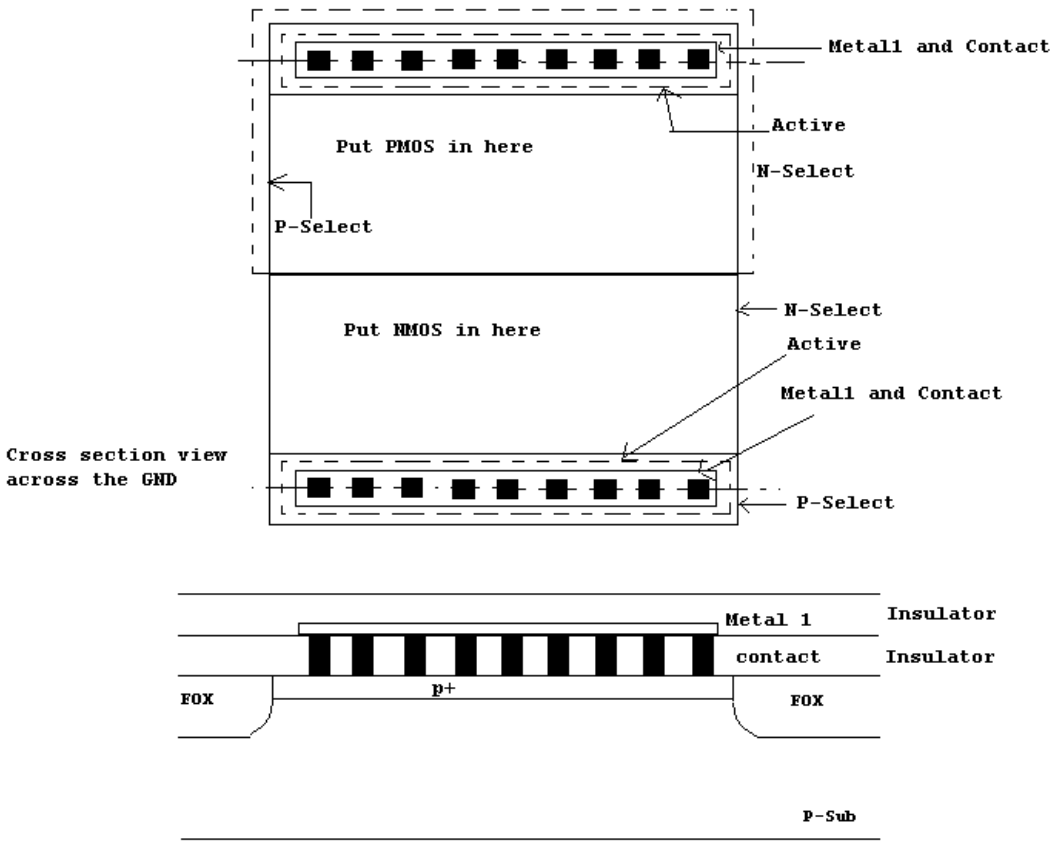
Figure 4.15 (a)

<u>Solution</u>:



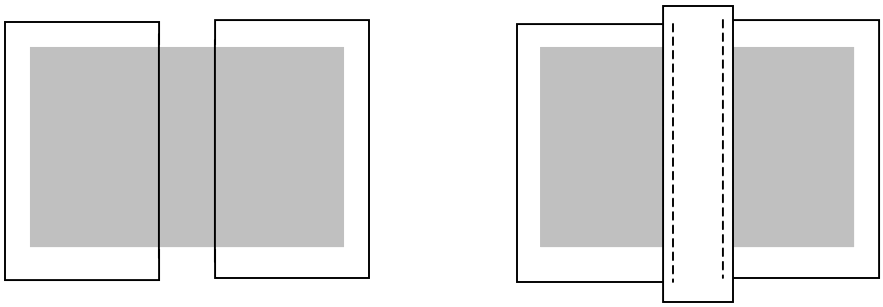


Problem 4.3 Cross section across the VDD



Problem 4.3 Cross section across the GND

4.4 Suppose the "bad" layout seen in Fig. Ex4.1 is used to fabricate an NMOS device. Will the poly be doped? Why or why not?



(a) Drawing active and select for MOSFET (bad).

(b) Placing poly over the layout in (a) (bad).

Figure Ex4.1: Bad layout examples (what NOT to do)

Solution

Only the section of the polysilicon that overlaps the select mask will be doped. This is because the select mask defines the area that will be bombarded with the implants. In this case there are two select masks and while laying out the MOSFETs, we have some overlap of poly and active areas for source and drain (seen as dotten lines in **Figure Ex4.1.b)**. So, sections of the polysilicon that cross over or overlap the select mask will be exposed to the implants and the area exposed will be doped.

Justin Wood
Problem 4.5 Solution

4.5) Why is polysilicon's parasitic capacitance larger than metal1s?

Polysilicon's parasitic capacitance is larger than metal1s because the polysilicon is located on a lower level of insulation, which is closer to the substrate. As given by the following formula:

$C=\varepsilon A/d$ ε=permittivity of dielectric material
A=plate area
d=distance between plates

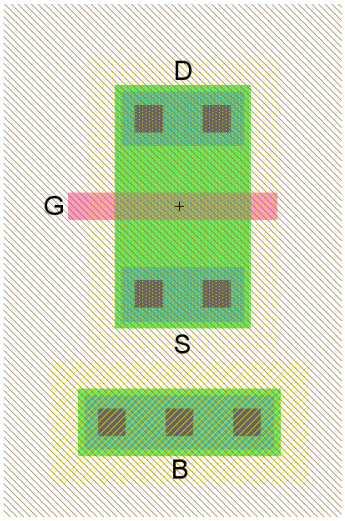
When the distance between the plates (in this case polysilicon and p-substrate) decreases, the capacitance increases.

Harikrishna Rapole

4.6. Lay out an NMOS device with a length of 1 and width of 10. Label all four terminals of the MOSFET terminals.

Sol: Electric is used for layout. The minimum length of NMOS or PMOS in electric is 2 units. Hence NMOS device with length 2 and width 10 is laid out.

S, D, G connections:
Go to component menu in electric, select **mocmos** from the dropdown menu. Use Cntrl+N to create a new cell. Select NMOS from the list of available components. Drag and drop NMOS to the new cell. Extend poly of the NMOS and create export selecting the pin on the extended poly. Name the export as G (gate). Place N-active contact from the components and place it as close to the upper N-active of the MOSFET as possible, so that DRC errors are avoided. Increase the width of N-active to 10, connect to the drain, and then overlap the connected N-active on the drain. Export the N-active contact as D (drain).Repeat the step for the bottom N-active of the MOSFET. Export this N-active contact as S (source).

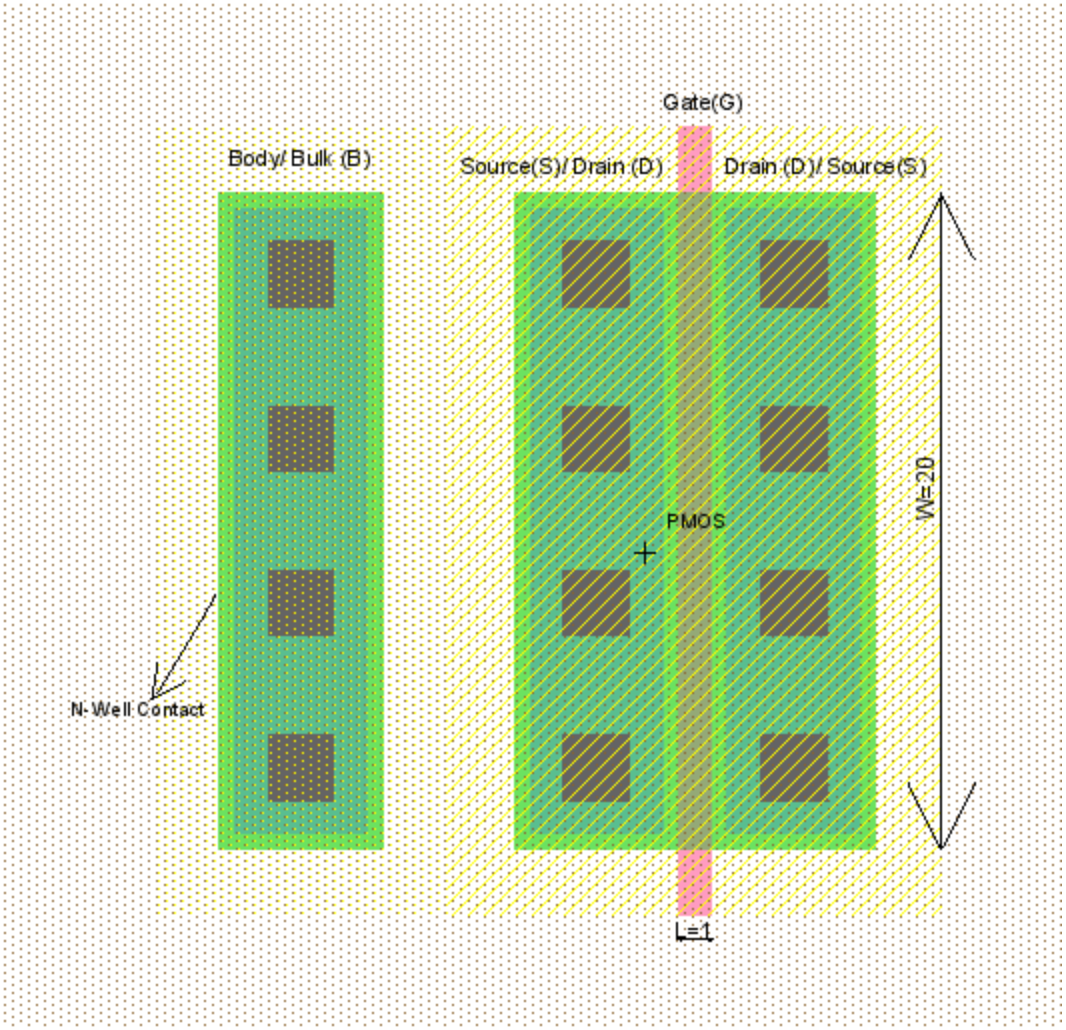


Body connection:
Go to component menu in electric, in **pure** select P-well node of 25x40 size. Place p-well contacts at the bottom of the P-well node. Place the p-well contact at the bottom of the p-well node, so that there are no drc overlapping errors. Increase the x dimension to 15. Export the contact as **B** (body).

Aruna Vadla

Problem (4.7): Layout a PMOS device with a length of 1 and a width of 20. Label all four of the MOSFET's terminals.

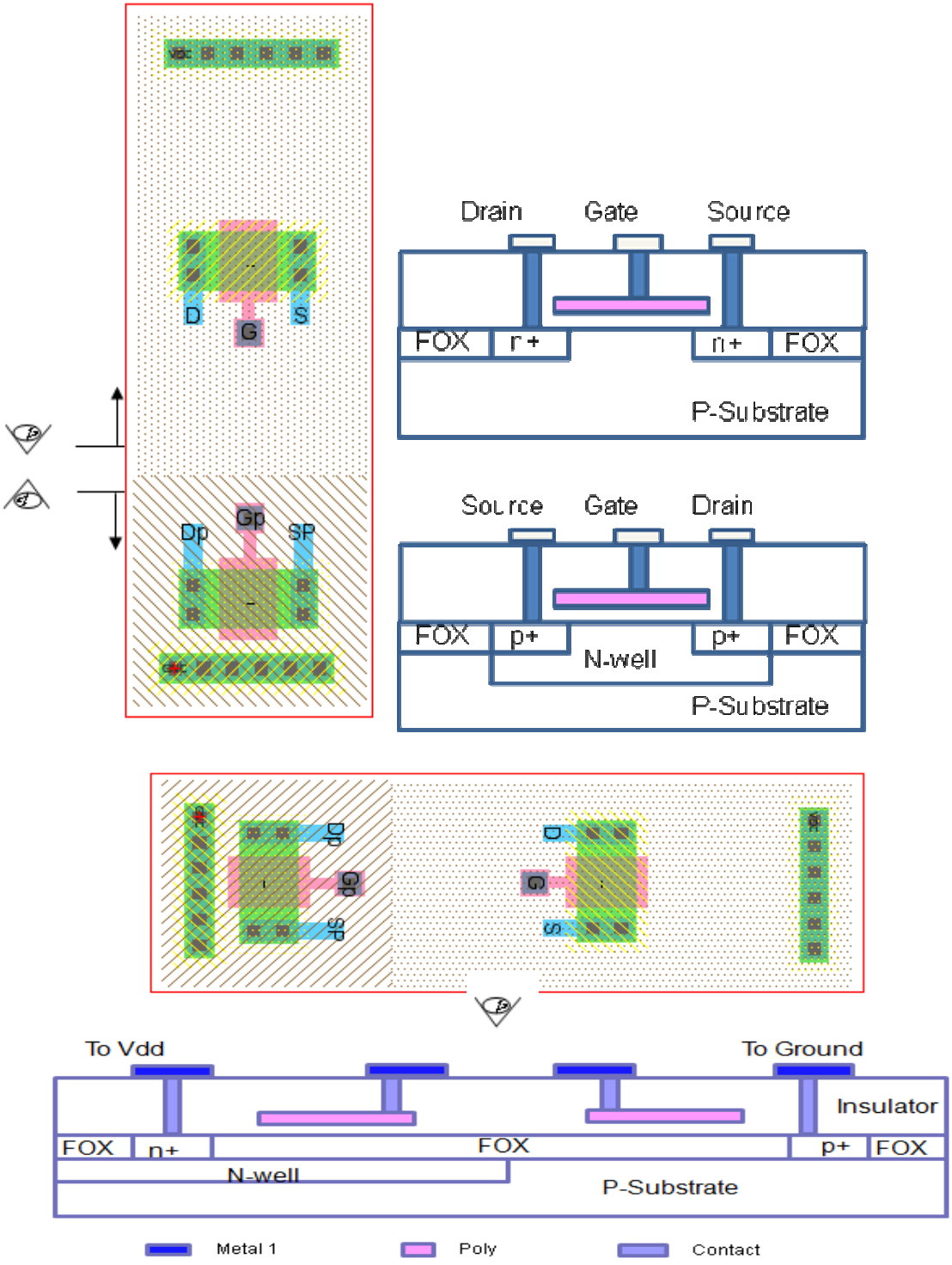
Solution:
Layout of a PMOS device with L = 1 and W = 20 is as shown below:



4.8 Using the standard cell frame, lay out 10 (length) by 10 (width) NMOS and PMOS transistors. Sketch several cross-sectional views of the resulting layouts showing all four terminals of the MOSFETs.

Solutions:

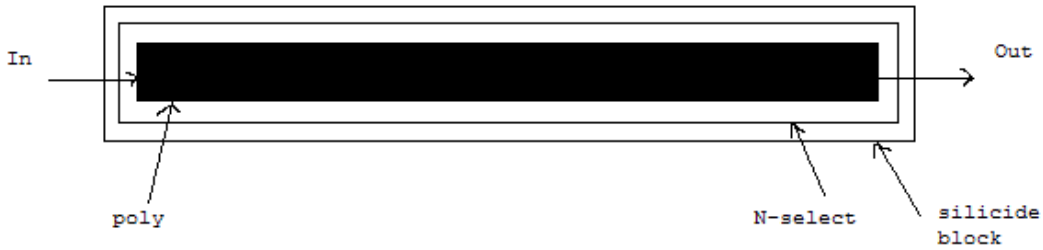
10 by 10 NMOS and PMOS are laid out in Electric, and its snapshot is shown in the following figure. To highlight the use of standard cell frame, the cell can be selected as a unity. The cross-sectional views are drawn as well.



KRISHNA DUVVADA

PROBLEM 4.9

Estimate the delay through the poly wire in the following figure with and without silicide. The width is 5 and the length is 1,000. Use a scale factor of 50nm and the values for capacitance in table 3.1. Simulate the delay using SPICE?



SOLUTION: -
Length of the wire is 1,000
Width is 5 and the scale factor is given as 50ns
The capacitance of the poly wire doesn't depend on the presence or absence of the silicide.
Capacitance of poly to substrate is

$C_{poly} = (C_{plate})^* (\text{Drawn area}) (\text{Scale})^2 + (C_{fringe})(\text{drawn perimeter})(\text{scale})$

From the table 3.1, C_{plate} =58aF
C_{fringe}=88aF

C_{poly}= (58aF)(1000* 5) $(.05)^2$ + (88aF) (2010)(0.05)
=9.569fF

Resistance=R_{square}* L/W

Without silicide, R_{square}= 200 ohms/square…(from table 4.1)
R= 200* (1000/5)=40K ohms
With silicide, R_{square}= 5 ohms/square
R=5*(1000/5)=1K ohms
Delay through the poly wire without silicide,

Delay though the poly wire with silicide,

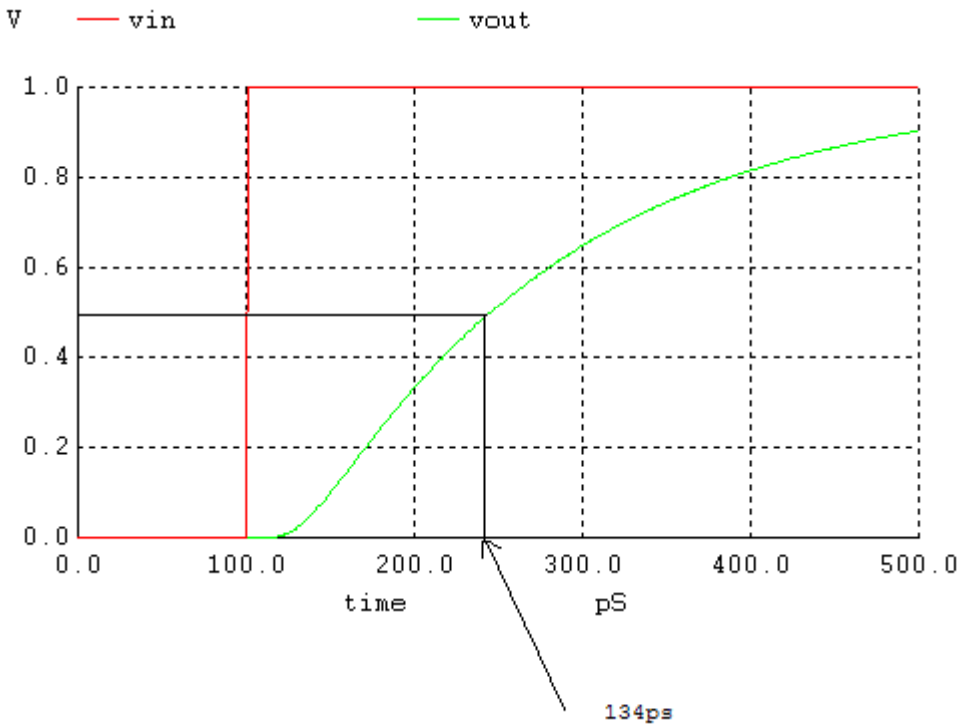
t_d =0.35 RC

=(0.35)(1K)(9.569fF)
=3.345ps

Simulation using SPICE:--

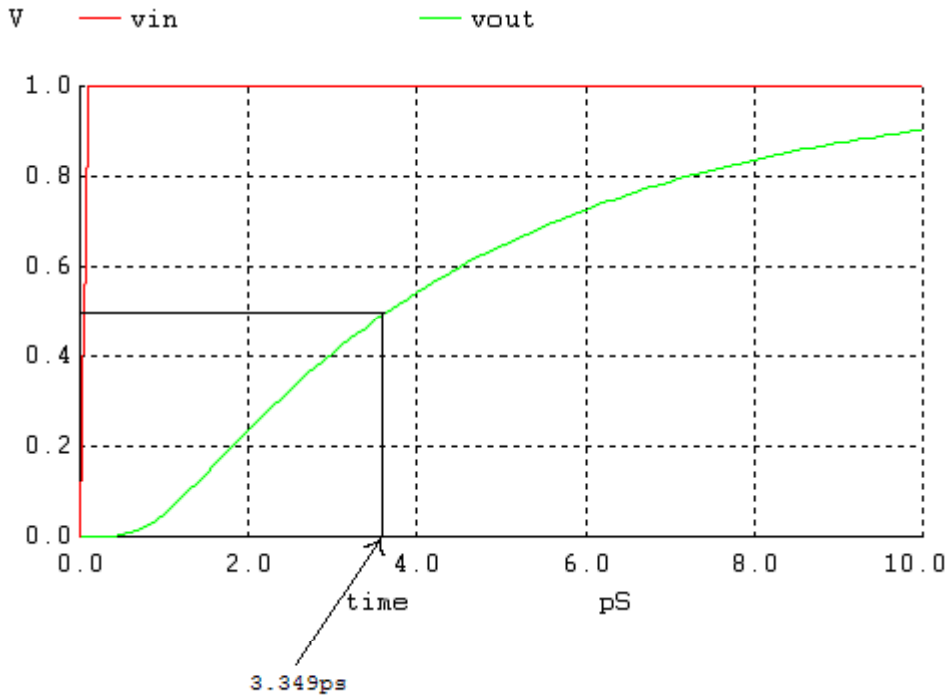
1) Delay with out silicide,

```
** Delay through poly with out silicide
.control
destroy all
run
plot vin vout
.endc
.tran 1p 500p
o1 Vin 0 vout 0 TRC
**Rload vout 0 1G
Vin vin 0 DC 0 pulse 0 1 100p 0
.model TRC ltra R=200 C=47.8e-18 len=200
.end
```



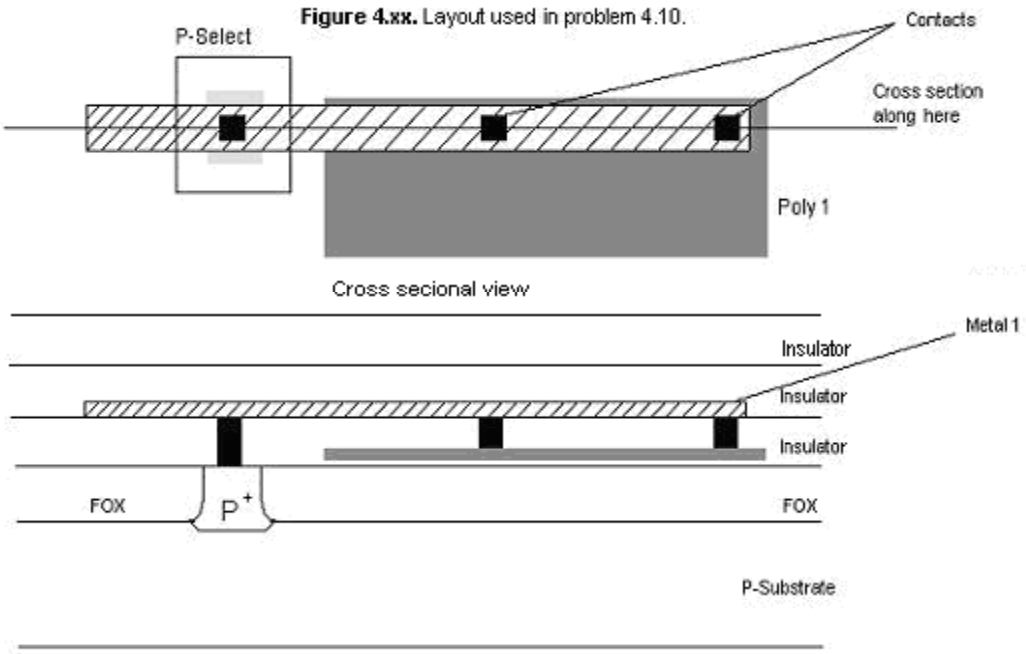
** *Delay through poly with silicide*

```
.control
destroy all
run
plot vin vout
.endc
.tran .1p 10p UIC
o1 Vin 0 vout 0 TRC
Rload vout 0 1G
Vin vin 0 DC 0 pulse 0 1 0 0
.model TRC ltra R=5 C=47.8e-18 len=200
.end
```



4.10)

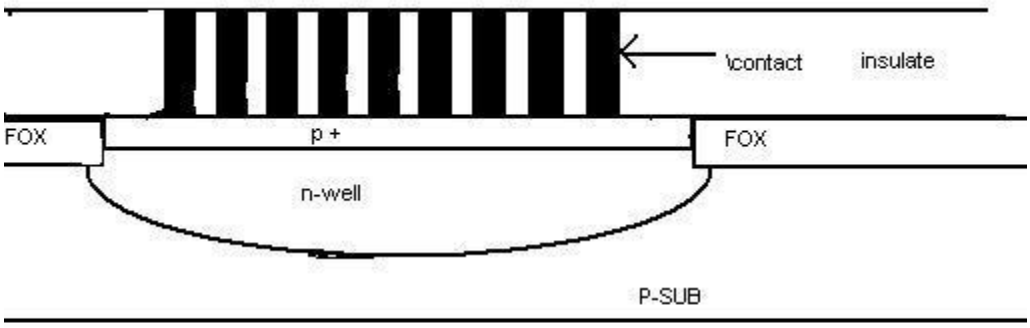
Sketch the cross-sectional views at the line indicated in Fig. 4.xx.



Edward Kunz

Problem 4.11

Sketch the cross sectional views across the lines shown in figure 4.xxx.



KRISHNAMRAJU KURRA

Q.12: The layout of a PMOS device is seen in Fig.4.24 is incorrect. What is the (fatal) problem?

A.

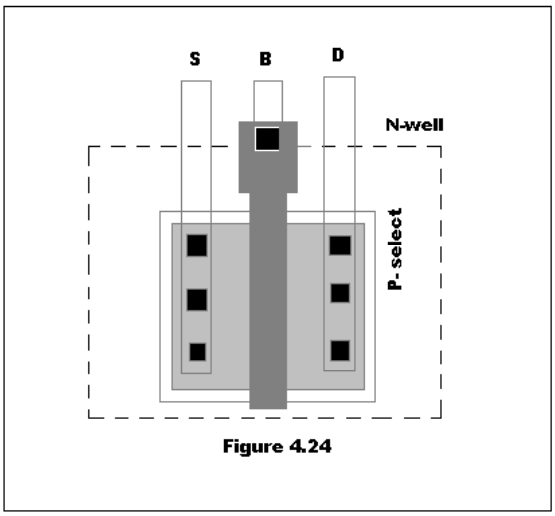


Figure 4.24

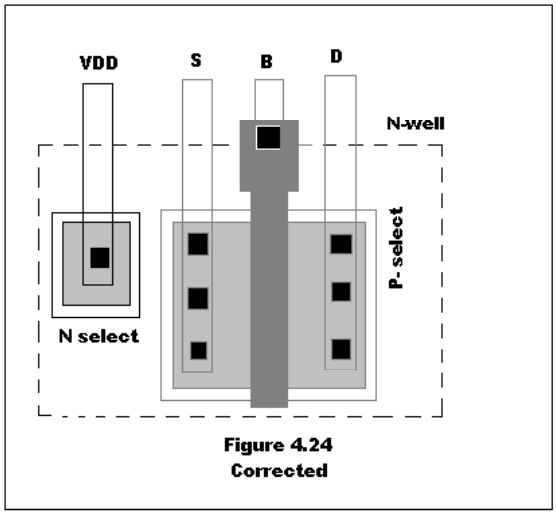


Figure 4.24
Corrected

For PMOS N-well is the body of the MOSFET. In the figure the N-well is not connected. The error is that the body is floating. To correct the error the body should be connected to VDD. (To make the Mosfet symmetric may be we can connect drain also to VDD)