1.1 What would happen to the transfer function analysis results for the circuit in Fig.1.11 if a capacitor were added in series with R1? Why? What about adding a capacitor in series with R2?

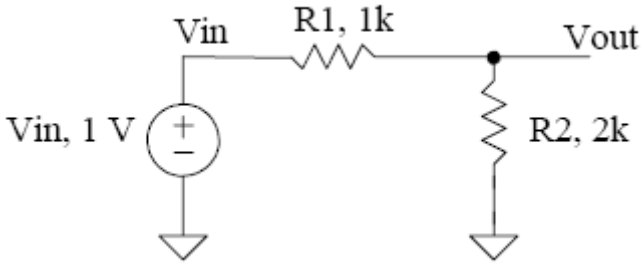
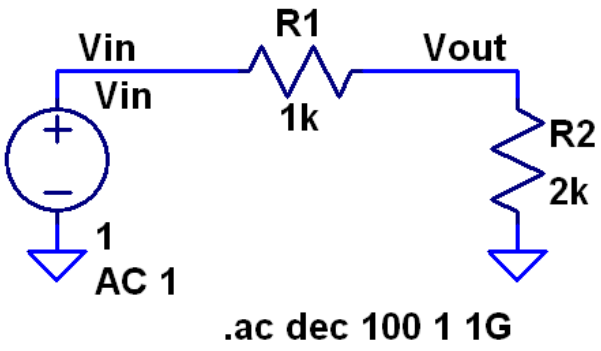
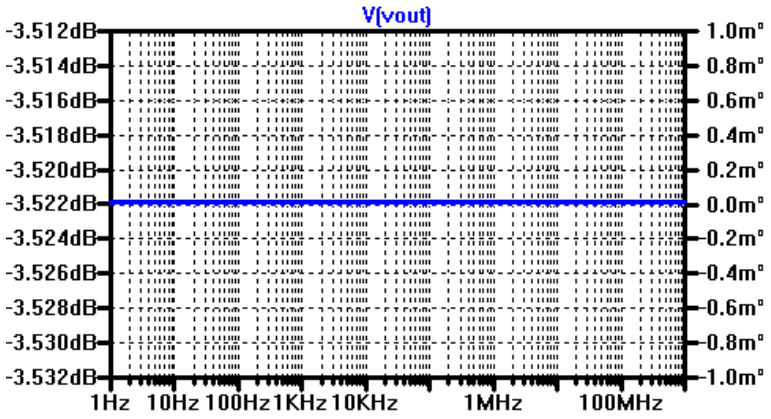


Fig1.11

Soln: $Vout = \frac{R2}{R2+R1}\text{Vin}$ => $\frac{2k}{1k+2k}*1$ => Vout = 0.66V or -3.52dB

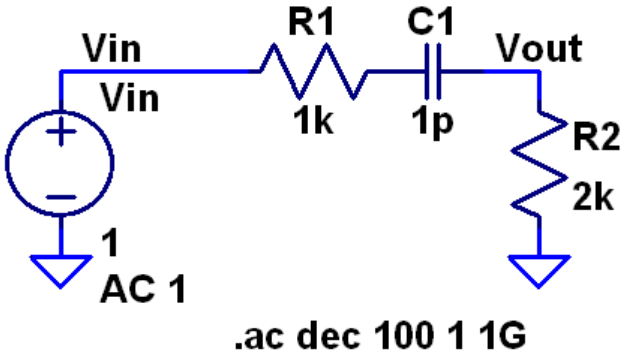


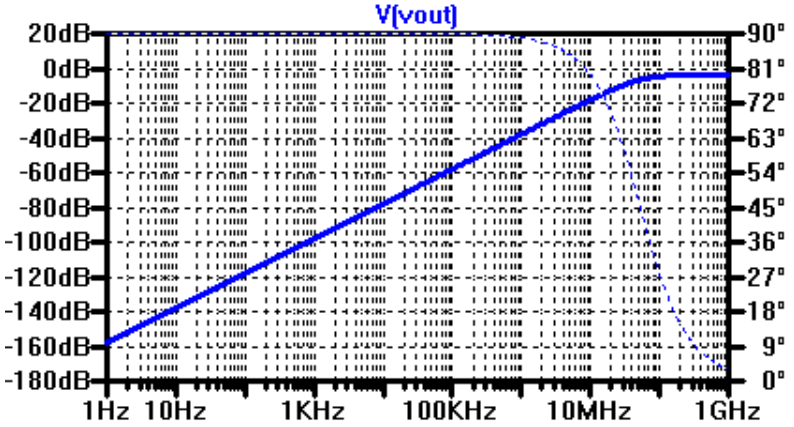


Case 1: When a capacitor is added in series with R1

$$\frac{Vout}{Vin} = \frac{R2}{R2+R1+\frac{1}{j\omega C}} \Rightarrow \frac{Vout}{Vin} = \frac{j\omega CR2}{j\omega C(R2+R1)+1}$$

This becomes a CR circuit and hence behaves like a High pass filter. The capacitor attenuates the signal in low frequency and passes signal in high frequency.

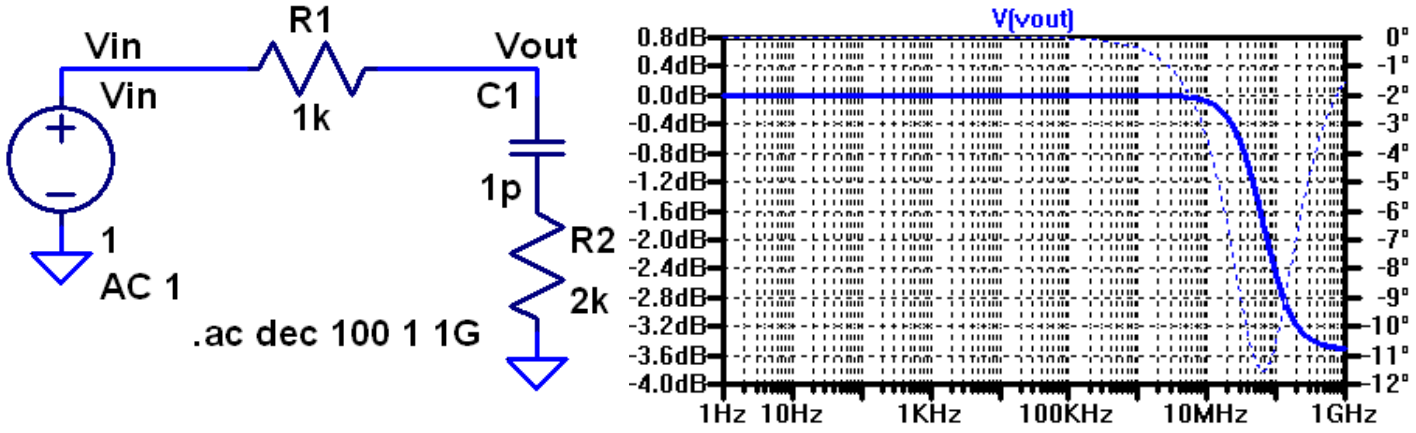




Case 2: When capacitor is added in series with R2

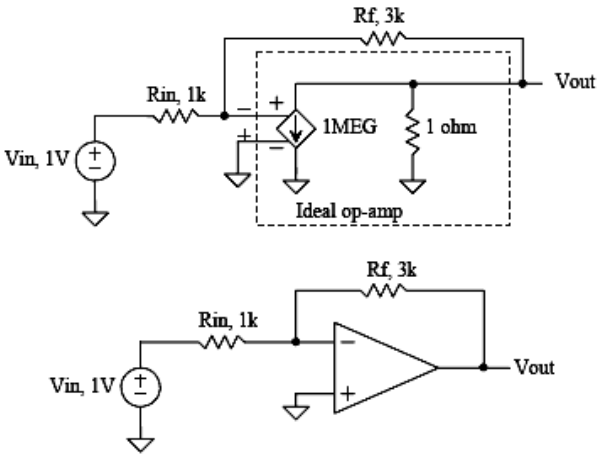
$$\frac{Vout}{Vin} = \frac{R2 + \frac{1}{j\omega C}}{R2 + \frac{1}{j\omega C} + R1} \quad => \quad \frac{Vout}{Vin} = \frac{j\omega CR2 + 1}{j\omega C(R2 + R1) + 1}$$

This circuit acts like a low pass filter. The circuit passes low frequency signal and attenuates high frequency signals.

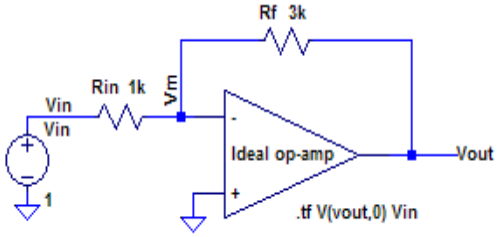


1.2) Resimulate the op-amp circuit in Fig. 1.15 if the open-loop gain is increased to 100 million while, at the same time, the resistor used in ideal op-amp is increased to 100Ω. Does the output voltage move closer to the ideal value.

Sol: - With the configuration of Fig. 1.15



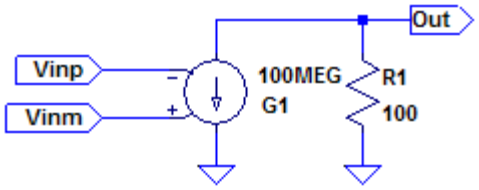
The open loop gain of op-amp will be given as 1MEG × 1 Ω = 1MEG. When circuit is simulated the transfer function of circuit is given as

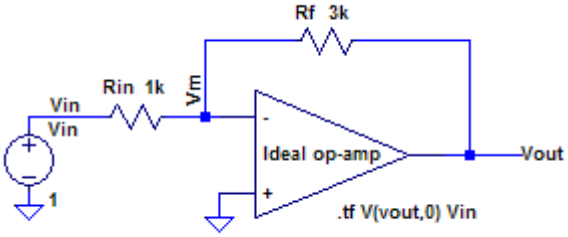



```
--- Transfer Function ---

Transfer_function:                -2.99999        transfer
vin#Input_impedance:              1000            impedance
output_impedance_at_V(vout,0):                    3.99998e-006    impedance
```

Now when value of G (voltage controlled current source) was changed to 100 MEG and value of resistor to 100Ω and circuit was simulated. The output is as shown below






```
--- Transfer Function ---

Transfer_function:                -3              transfer
vin#Input_impedance:              1000            impedance
output_impedance_at_V(vout,0):                    4e-008          impedance
```

Transfer function or the closed loop gain of op-amp is exactly -3 (ideal value) and with the input at 1V; Output = |Gain| × Vin = 3V, an ideal value. The reason behind output or transfer function going to ideal value is that the open loop gain of op-amp became = 100MEG × 100 Ω = 10 Gig (very large). Also in closed loop inverting configuration the close loop gain of op-amp is related to open loop gain as $A_{CL} = -\dfrac{(R_2/R_1)}{1+(1+R_2/R_1)/A_{OL}}$. Thus with very large value of A_{OL}, gain (transfer function or also output) became ideal.

-Shantanu Gupta

1.3) Simulate the op-amp circuit in Fig. 1.15 if Vin is varied from -1 to +1V. Verify, with hand calculations, that the simulation output is correct.

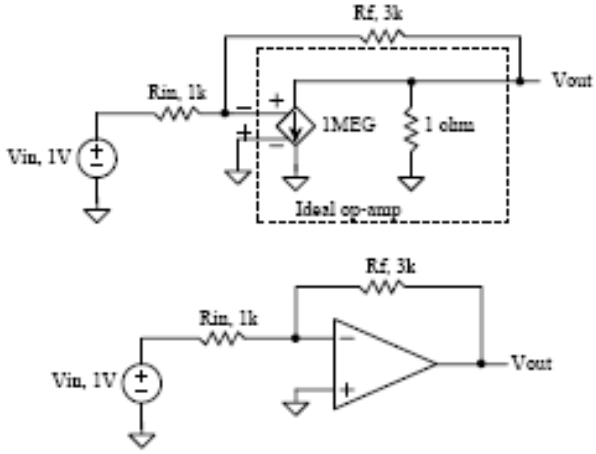


Figure 1.15 An op-amp simulation example.

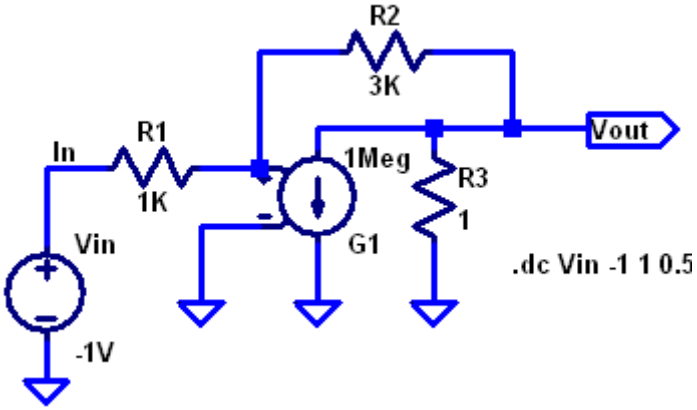
In the op-amp shown, the positive input is grounded and the negative input is connected to the input voltage, this is the closed-loop inverting configuration of an op-amp. In this configuration, the closed-loop gain is given by $\frac{Vout}{Vin} = -\frac{Rf}{Rin}$.

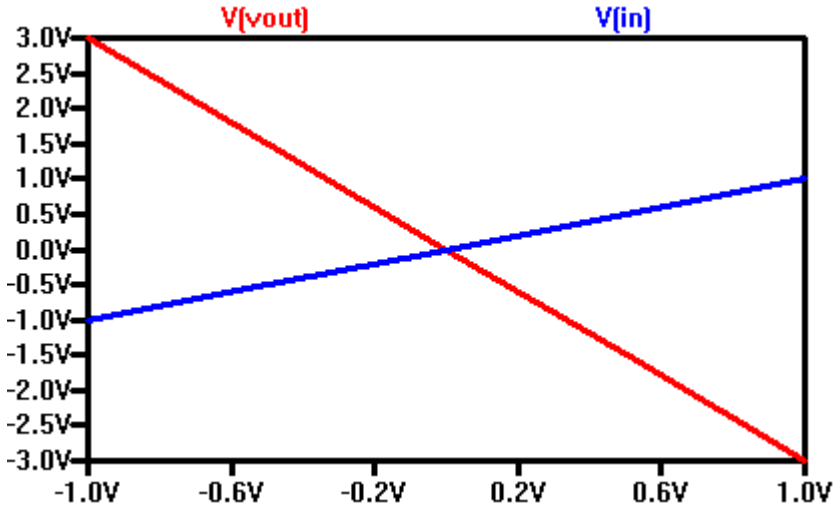
Substituting the values, we get Vout = -3 * Vin. If the input voltage, Vin is swept from -1V to 1V with an increment of 0.5V, then we get the following results for Vout.

Vin	Vout
-1V	**3V**
-0.5V	**1.5V**
0V	**0V**
0.5V	**-1.5V**
1V	**-3V**

Hand Calculation results

LTSpice used for Simulation results check:

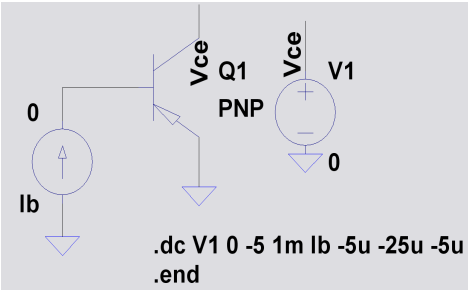




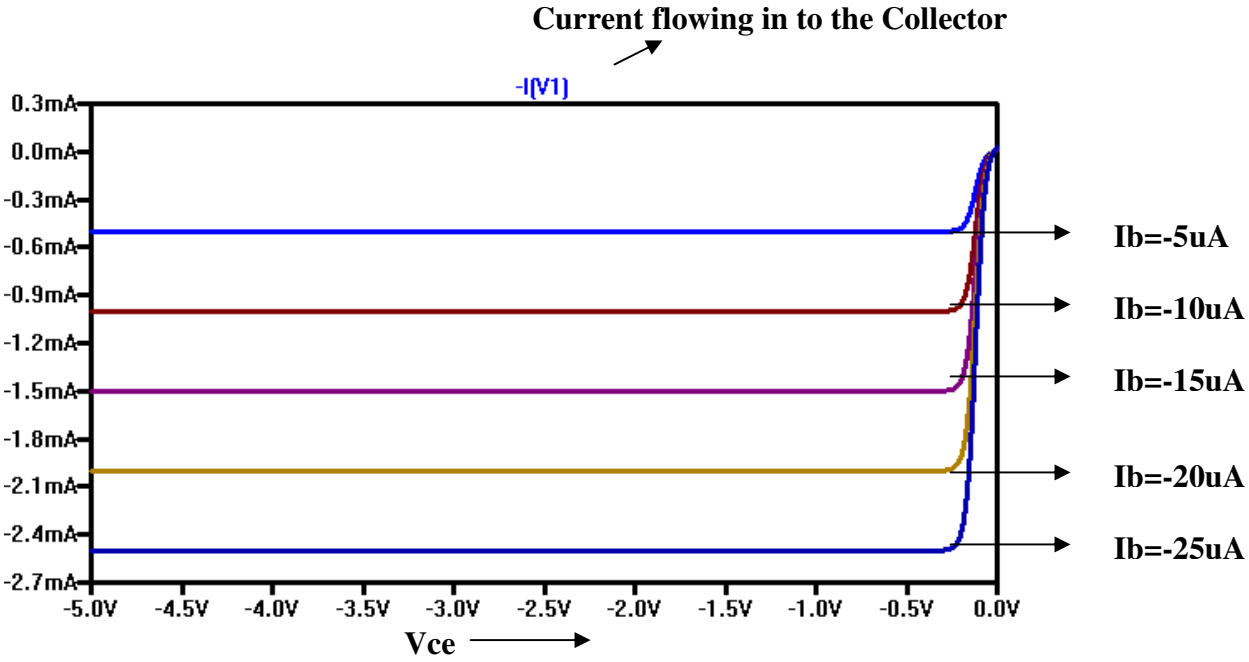
Harikrishna Rapole

1.4. Regenerate the IV curves as seen in Fig 1.18 for a PNP transistor.

Sol: In this simulation we start out by setting the bias currents to -5uA and sweeping the collector-emitter voltage from 0 to -5V in 1mV steps. The output data for the particular simulation is the trace with label Ib=-5uA. Again base current is increased by -5uA and the collector-emitter voltage is again increased to -10v. This continues until the final iteration when Ib=-25uA.



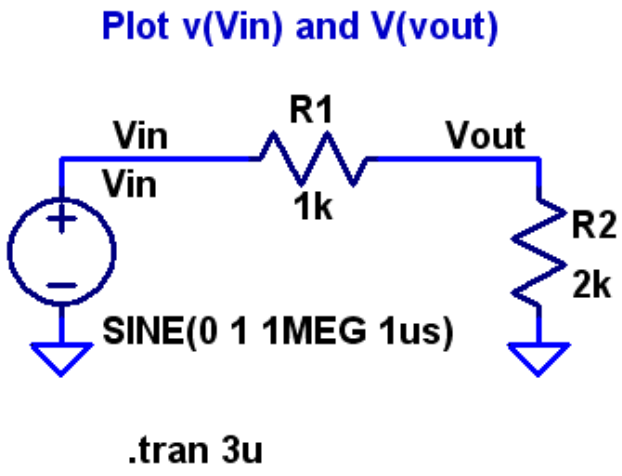
Plot Vce, Collector current (-I(V1))



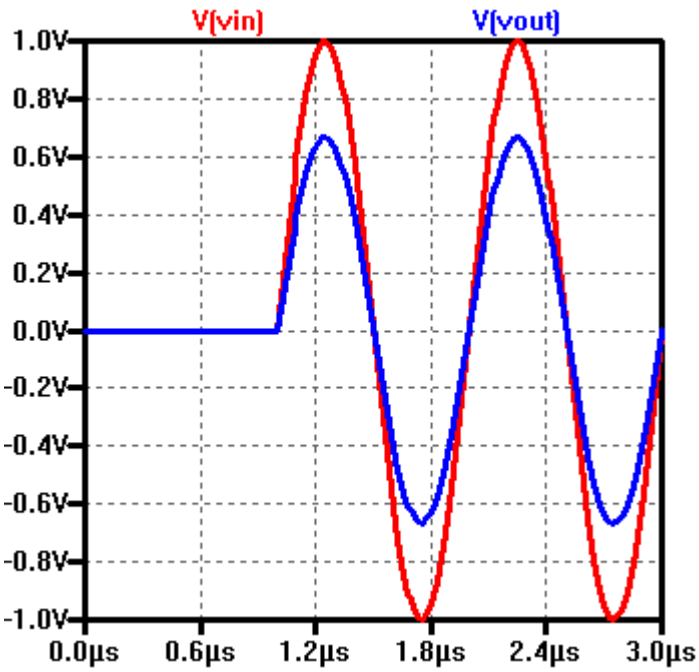
Aruna Vadla

(Problem 1.5): Resimulate the circuit in Fig. 1.20 if the sinewave doesn't start to oscillate until 1us after the simulation starts.

Solution: Fig. 1.20 in the textbook is as seen below:

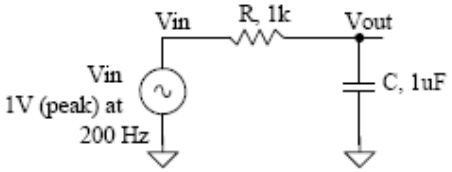


In order that the sinewave doesn't start to oscillate until 1 us after the simulation starts, a time delay of 1 us was added in the input sinewave. So, the sinewave doesn't start to oscillate until 1 us after the simulation starts. The circuit is simulated and the output is shown in the figure below:



1.6 At what frequency does the output voltage, in Fig. 1.21, become half of the input voltage? Verify your answer with SPICE

Solutions:



The transfer function for the RC circuit seen in Fig 1.21 can be written by

$$\frac{V_{OUT}}{V_{IN}} = \frac{1/j\omega C}{1/j\omega C + R} = \frac{1}{1 + j\omega CR}$$

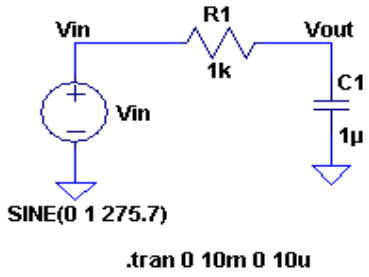
Making the magnitude of this equation equal one half gives

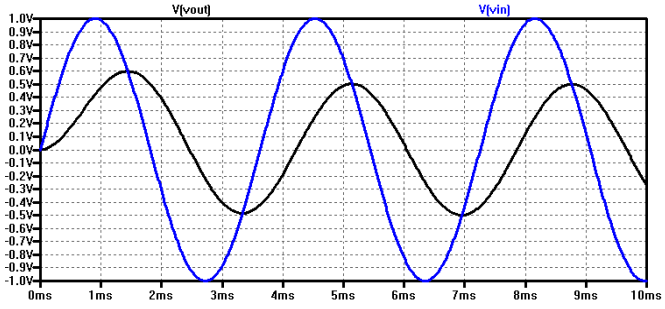
$$\left|\frac{V_{OUT}}{V_{IN}}\right| = \frac{1}{\sqrt{1+(\omega RC)^2}} = \frac{1}{2} \quad \text{or} \quad \omega RC = \sqrt{3}$$

Then the frequency can be determined by

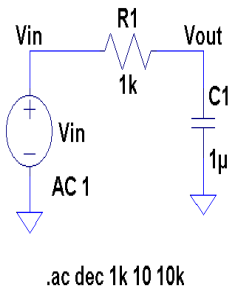
$$f = \frac{\sqrt{3}}{2\pi RC} = \frac{\sqrt{3}}{(2\pi)(1k)(1\mu)} = 275.7Hz$$

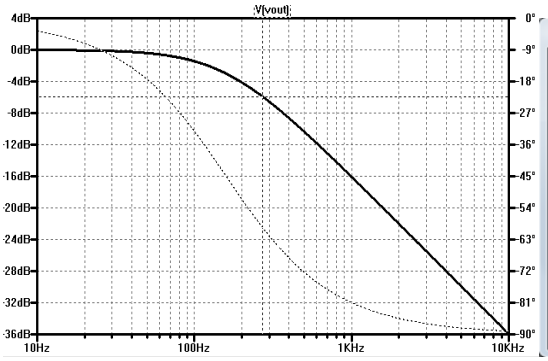
For SPICE verification, there are two ways of doing it. One is transient analysis and the other is AC analysis as are shown as following.
The LTSpice simulation results are shown as below.

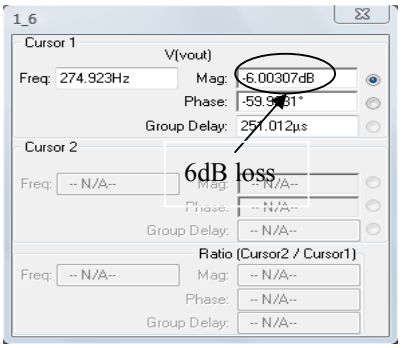




Transient Analysis







AC Analysis

The 6dB loss is because the relationship between dB and magnitude is given by

$$20\log_{10}\left(\frac{1}{2}\right) = -20\log_{10} 2 = -20 \times 0.3 = -6dB$$

Submitted by L. Bollschweiler
Lincolnbollschweiler@gmail.com

1.7 ***Determine the output of the circuit seen in Fig 1.22 if a 1kΩ resistor is added from the output of the circuit to ground. Verify your hand calculations using SPICE.***

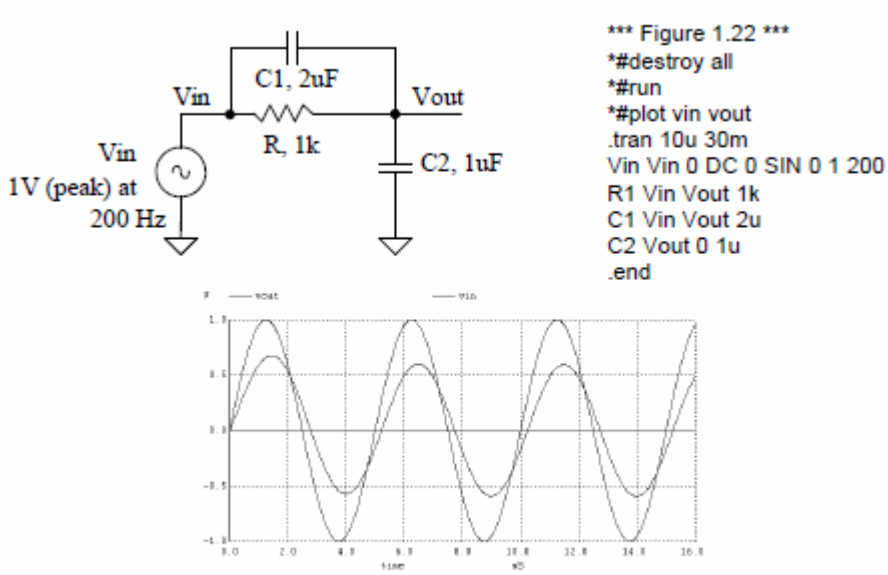


Figure 1.22 Another RC circuit example.

First show the parallel combination of the capacitors and resistors.

$C_1//\mathrm{R}=\dfrac{1}{\dfrac{1}{\mathrm{R}}+j\omega C_1}\left(\dfrac{R}{R}\right)=\dfrac{R}{1+j\omega RC_1}$. By the same algebra $C_2//\mathrm{R}_{\mathrm{out}}=\dfrac{R_{out}}{1+j\omega R_{out}C_2}$.

To solve for $\mathrm{V}_{\mathrm{out}}$ we can use the voltage division $\dfrac{V_{out}}{V_{in}}=\dfrac{C_2//R_{out}}{C_2//R_{out}+C_1//R}$.

$$\frac{V_{out}}{V_{in}}=\frac{\dfrac{R_{out}}{1+j\omega R_{out}C_2}}{\dfrac{R_{out}}{1+j\omega R_{out}C_2}+\dfrac{R}{1+j\omega RC_1}}=\frac{\dfrac{R_{out}}{1+j\omega R_{out}C_2}}{\dfrac{R_{out}+j\omega RR_{out}C_1+R+j\omega RR_{out}C_2}{\left(1+j\omega R_{out}C_2\right)\left(1+j\omega RC_1\right)}}$$

$$=\frac{R_{out}}{1+j\omega R_{out}C_2}\cdot\frac{\left(1+j\omega R_{out}C_2\right)\left(1+j\omega RC_1\right)}{R+R_{out}+j\omega RR_{out}\left(C_1+C_2\right)}$$

$$=\frac{R_{out}\left(1+j\omega RC_1\right)}{R+R_{out}+j\omega RR_{out}\left(C_1+C_2\right)}$$

$$=\frac{R_{out}+j\omega RR_{out}C_1}{R+R_{out}+j\omega RR_{out}\left(C_1+C_2\right)}.$$

Submitted by L. Bollschweiler
Lincolnbollschweiler@gmail.com

Substituting in values R = R_{out} = 1k, C1 = 2µ, C_2 = 1µ, ω = 2πf = 2π*200 = 1.26E3

$$= \frac{1E3 + j \cdot 1.26E3 \cdot 1E3 \cdot 1E3 \cdot 2E\text{-}6}{1E3 + 1E3 + j \cdot 1.26E3 \cdot 1E3 \cdot 1E3 \cdot (2E\text{-}6 + 1E\text{-}6)}$$

$$= \frac{1E3 + j2.51E3}{2E3 + j3.77E3}$$

We know that if $\frac{V_{out}}{V_{in}} = \frac{a + jb}{c + jd}$ then $\left\| \frac{V_{out}}{V_{in}} \right\| = \frac{\sqrt{a^2 + b^2}}{\sqrt{c^2 + d^2}}$ and $\measuredangle \frac{V_{out}}{V_{in}} = \tan^{-1}\left(\frac{b}{a}\right) - \tan^{-1}\left(\frac{d}{c}\right)$.

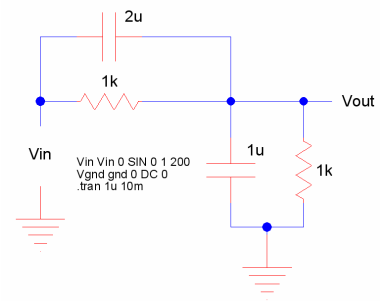
$$\left\| \frac{V_{out}}{V_{in}} \right\| = \frac{\sqrt{1E3^2 + 2.51^2}}{\sqrt{2E3^2 + 3.77E3^2}} = 0.629 .$$

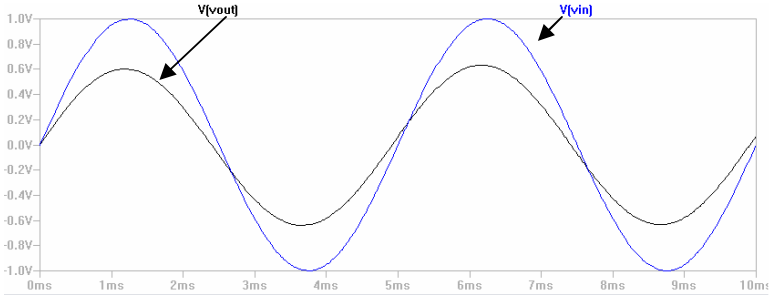
$$\measuredangle \frac{V_{out}}{V_{in}} = \tan^{-1}\frac{2.51}{1} - \tan^{-1}\frac{3.77}{2} = 68.3° - 62.1° = 6.22° .$$

V_{out} leads V_{in} by 6.22°. This is

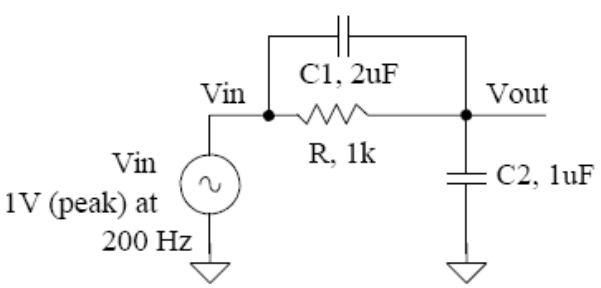
$\frac{6.22}{360} \cdot T$, $T = 1/f = 1/200 = 5ms$. So V_{out} leads V_{in} by $\frac{6.22}{360} \cdot 5ms = 0.086ms$.

Simulation





1.8 Using an AC analysis, verify the time domain results in Fig1.22.




```
*** Figure 1.22 ***
*#destroy all
*#run
*#plot vin vout
.tran 10u 30m
Vin Vin 0 DC 0 SIN 0 1 200
R1 Vin Vout 1k
C1 Vin Vout 2u
C2 Vout 0 1u
.end
```

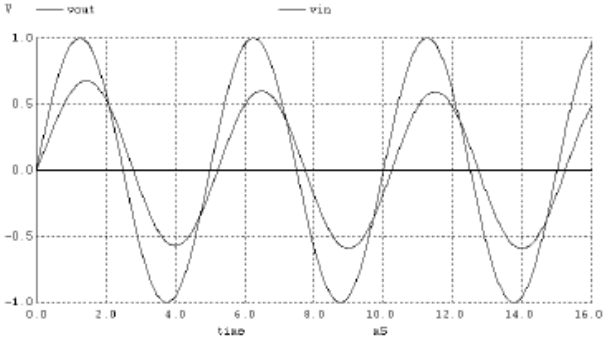
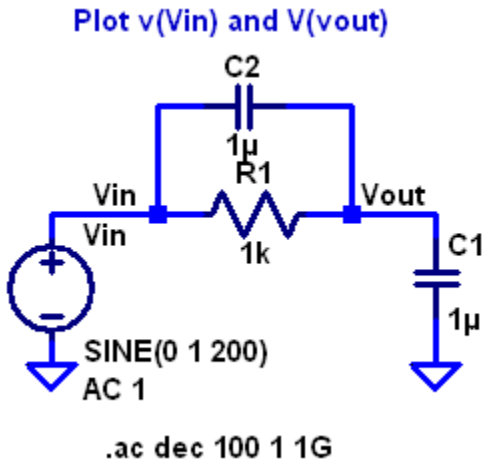
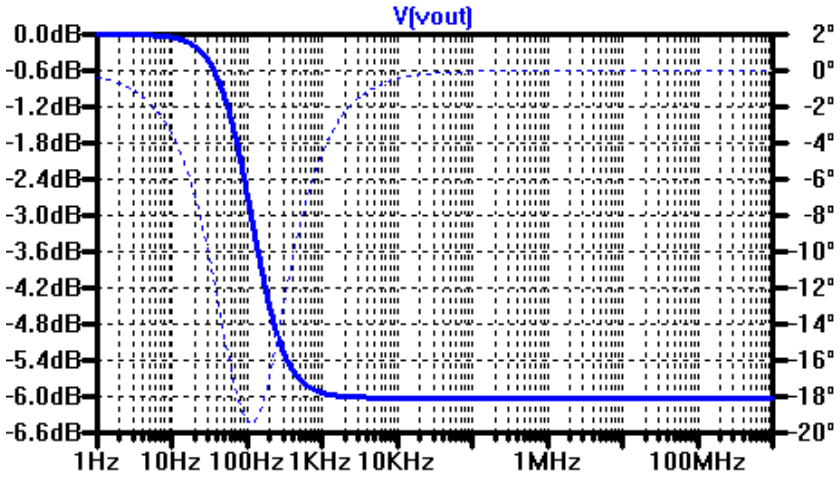


Figure 1.22 Another RC circuit example.

Soln:





1. Since the o/p is lagging the input, the phase is negative which is confirmed by the AC analysis.

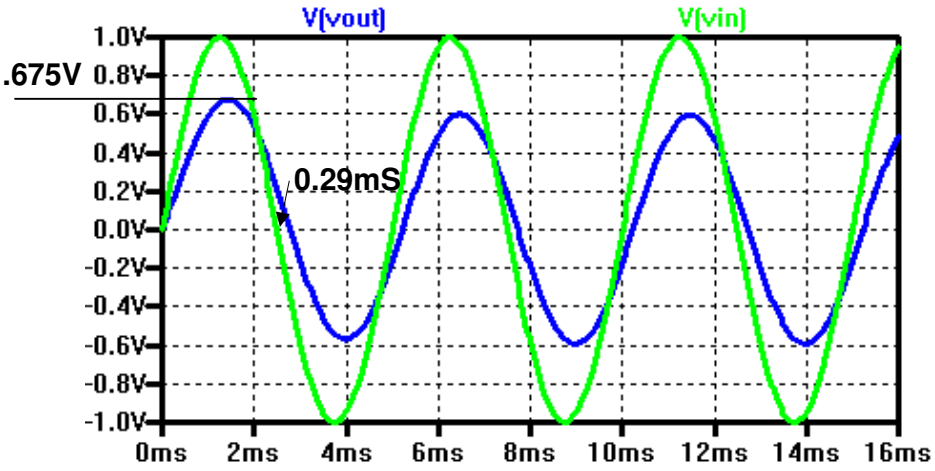
$$@\ 200Hz \quad \angle Av = -17^o$$

$$-17^o = \frac{360}{T} t_d \Rightarrow t_d = 0.236mS$$

2. @ $200Hz$ $|A_v| = -4.48dB$

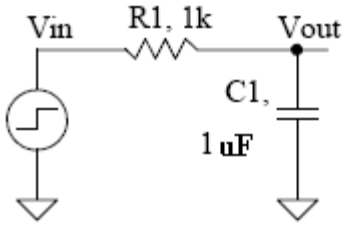
$$Vout = 10^{\frac{-4.48}{20}}$$

Vout = 0.597V



1.9) If the capacitor in Fig. 1.24 is increased to 1µF simulate, similar to Fig. 1.26 but with a longer time scale, the step response of the circuit. Compare the simulation results to the hand-calculated values using Eqs. (1.10) and (1.11)

Sol: Equations 1.10 and 1.11 states that:-



t_d (delay time) $\approx$ 0.7RC

t_r (rise time) $\approx$ 2.2RC

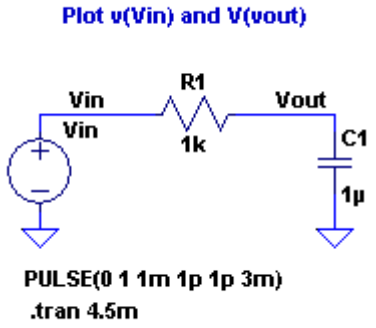
by hand calculations $t_d = 0.7 \times 1k \times 1 \times 10^{-6} F$

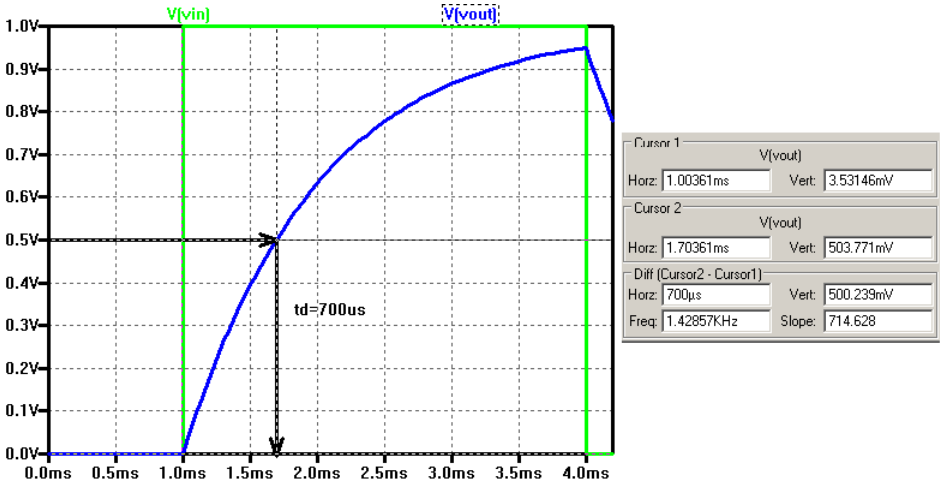
$= 700$ µsec or 0.7 msec

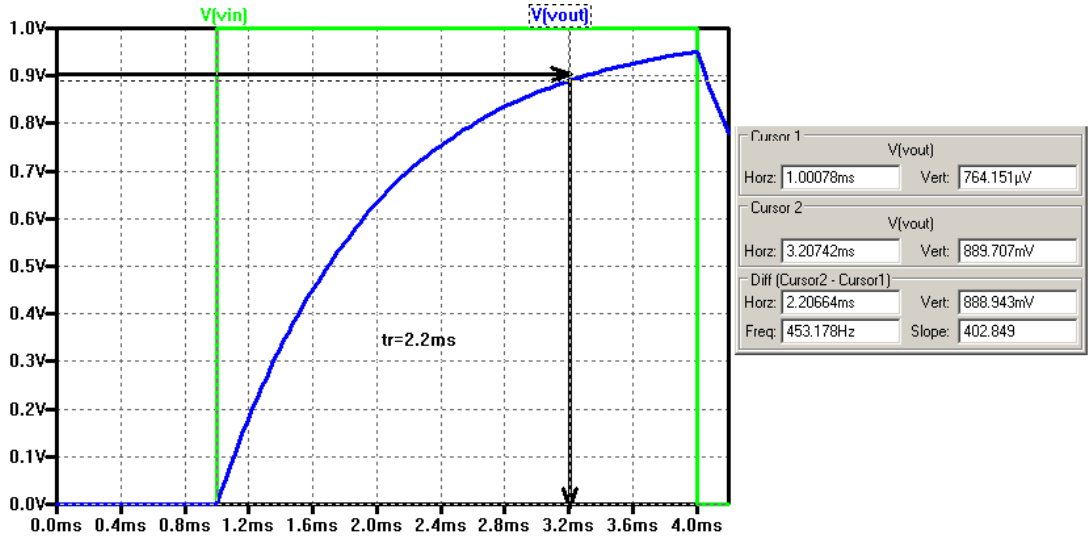
$t_r = 2.2 \times 1k \times 10^{-6} F$

$= 2.2$ msec

From LTSpice simulation







-Shantanu Gupta

1.10) Using a PWL source (instead of a pulse source), regenerate the simulation data seen in Fig. 1.26.

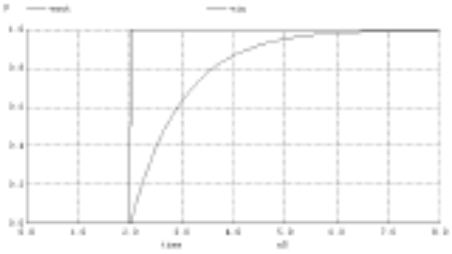
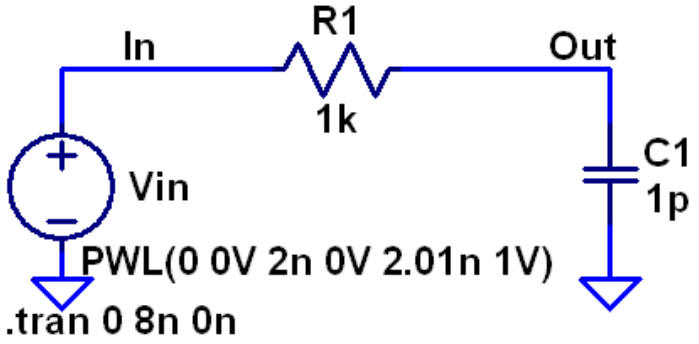
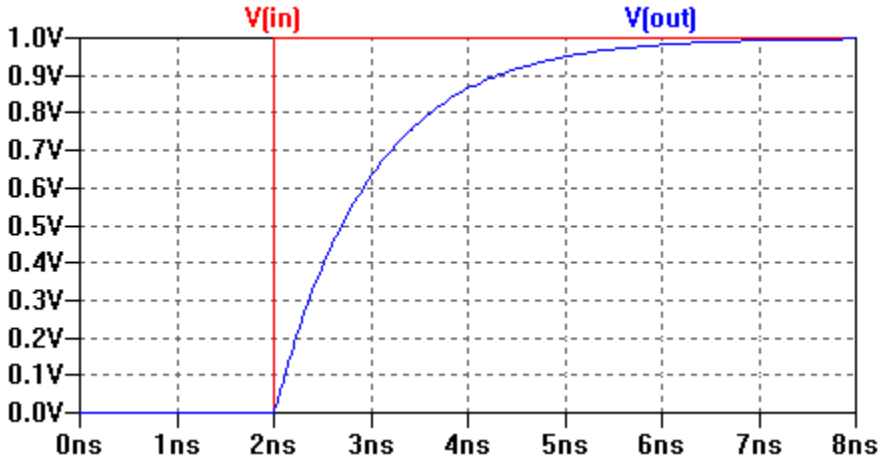


Figure 1.26 Step response of an RC circuit.

With a rise time of 10psec, the input starts at 2nsec and goes to 1V. This can be described using PWL source as *PWL(0 0V 2n 0V 2.01n 1V)*. Using that in LTSpice, we get:





Harikrishna Rapole

1.11. Using the values seen in Fig 1.32 for the inductor and capacitor determine the Q of a series resonant LC tank with a resistor value of 10 ohms. Note that the resistor is in series with the LC and that an input voltage source should be used (the voltage across the LC tank goes to zero at resonance).

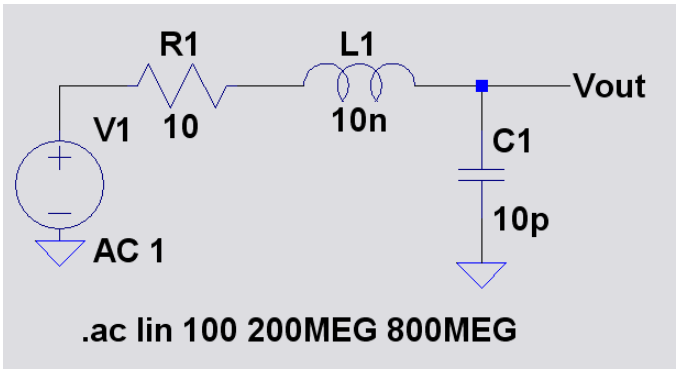
Sol: Used LTSPICE for the simulation.

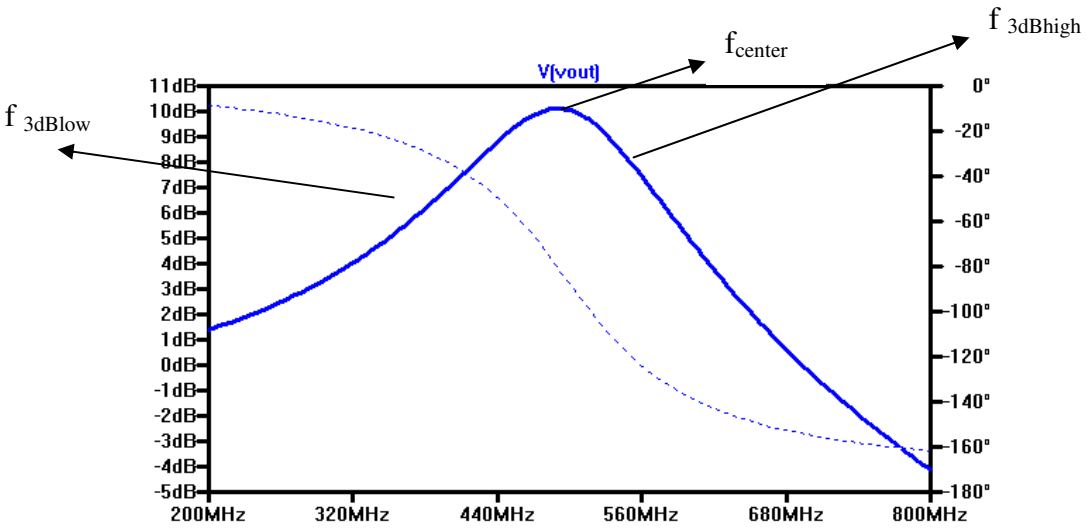
$$Q = f_{center}/BW = f_{center}/(f_{3dBhigh} - f_{3dBlow})$$

$f_{center} = 490MHZ$
$f_{3dBhigh} = 565MHZ$
$f_{3dBlow} = 402MHZ$

$Q = 490/(565-402) = 3.0061$
Q = 3

Schematic in LTSPICE





Priyanka Parikh

1.12 Suppose the input voltage of the integrator in Fig. 1.34 is zero and that the op-amp has a 10 mV input-referred offset voltage. If the input-referred offset voltage is modeled using a 10 mV voltage source in series with the non-inverting (+) op-amp input then estimate the output voltage of the op-amp in the time-domain. Assume that at $t = 0$ $V_{out} = 0$. Verify your answer with SPICE.

Solution:

The output voltage of the given integrator can be determined by using the following formula,

$$\frac{dv_{out}}{dt} = Voffset \frac{V_{in}}{RC} \quad \textbf{(a)}$$ or

$$V_{out} = Voffset \int_0^t \frac{V_{in}}{RC} dt + c \quad \textbf{(b)}$$

Where,

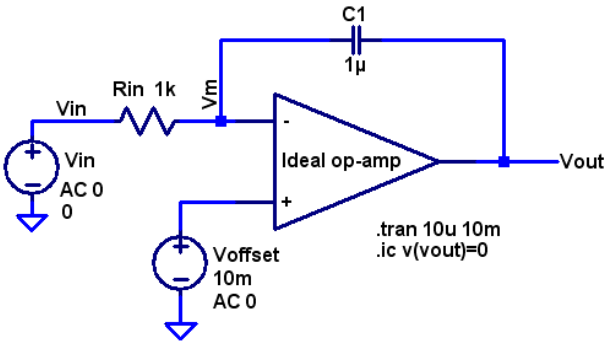
c = output voltage (Vout) at start time.

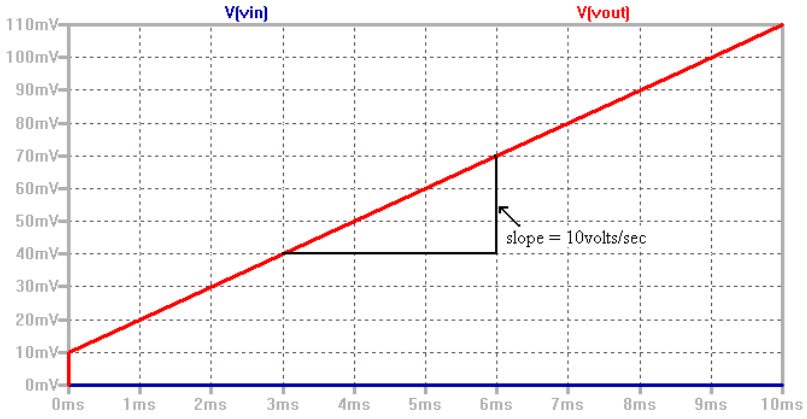
For the given circuit configuration, Vin = 0v and Voffset = 10mV. Because of offset voltage, at t = 0, Vout transits from 0 to 10mV (from (b)). For every millisecond increase in time, Vout increases by a factor of 10mV. i.e.

t (mS)	Vout (mV)
0	0 ->10mV
1	20mV
2	30mV
3	40mV
4	50mV

And so on.

The Spice simulation circuit and resulting waveforms are shown in the following figures.





Spice verifies the hand calculated results.