Cory Eskridge
Qawi Harvard
EE411

Problem 22.1

Figure 22.36 Diff-amp used in problem 22.1

Assuming that the MOSFETs M1 and M3 are biased are such that they operating in saturation region. KVL from the ground of v_{I1} to the ground of v_{I2} gives equations 1 and 2. Recognizing that all the current from M1 and M2 must equal I_{ss} gives equation 3. Equation 4 is the calculation of v_{gs}, using the square law equation for a MOSFET operating in the saturation, given i_D and neglecting body effect.

(1) $$-v_{I1} + v_{GS1} - v_{GS2} + v_{I2} = 0$$

(2) $$v_{I1} - v_{I2} = v_{GS1} - v_{GS2}$$

(3) $$i_{D1} + i_{D2} = I_{SS}$$

(4) $$v_{GS} = v_{THN} + \sqrt{\frac{2i_D}{\beta}}$$

Combining equations 2 and 4 and assuming equal size NMOS devices.

$$v_{I1} - v_{I2} = \sqrt{\frac{2i_{D1}}{\beta}} - \sqrt{\frac{2i_{D2}}{\beta}} = \sqrt{\frac{2}{\beta}}(\sqrt{i_{D1}} - \sqrt{i_{D2}})$$

$$\therefore \sqrt{\frac{\beta}{2}}(v_{I1} - v_{I2}) = \sqrt{i_{D1}} - \sqrt{i_{D2}}$$

Squaring both sides and using equation 3.

$$I_{SS} - \frac{\beta}{2}(v_{I1} - v_{I2})^2 = 2\sqrt{i_{D1}i_{D2}}$$

Squaring again gives:

$$I_{SS}^2 - I_{SS}\beta(v_{I1} - v_{I2})^2 + \frac{\beta^2}{4}(v_{I1} - v_{I2})^4 = 4i_{D1}i_{D2}$$

Using equation 3 and solving for i_{D1}

$$\sqrt{-\frac{I_{SS}^{2}}{4}+\frac{I_{SS}\beta(v_{I1}-v_{I2})^{2}}{4}-\frac{\beta^{2}(v_{I1}-v_{I2})^{4}}{16}}=i_{D1}$$

As v_{I1} gets much larger than v_{I2}, M2 shuts off and all the bias current is pulled through M1, making i_{D1} go to I_{SS}.

P22.2
Kloy Debban
Roger Porter.
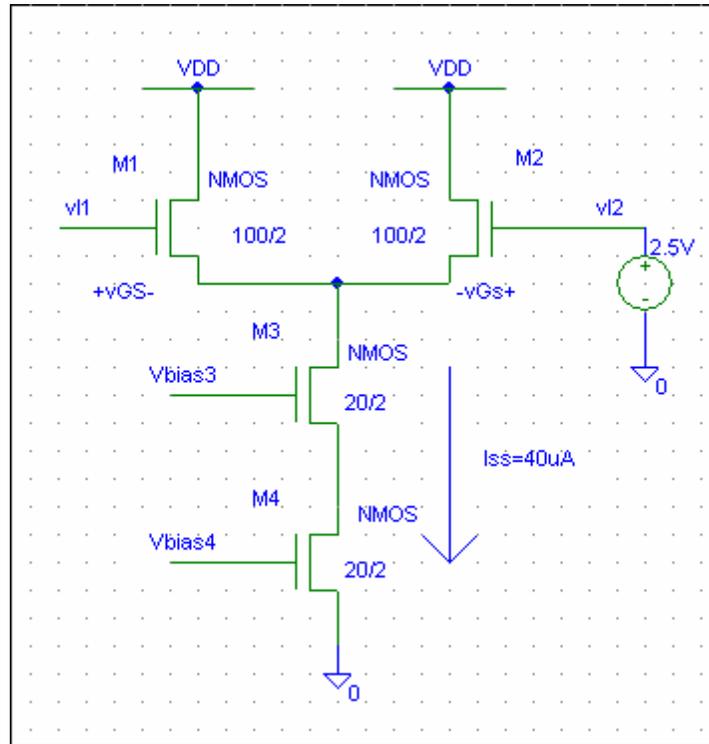
Figure 1.

Iss=40µA
$$v_{DI} = v_{I1} - v_{I2}$$

In saturation a MOSFETS drain current is :

$$i_D = \frac{\beta_n}{2} * (v_{GS} - Vthn)^2 \Rightarrow v_{GS} = v_I = \sqrt{\frac{2 * i_D}{\beta_n} + Vthn}$$

This means that $v_{DI} = v_{I1} - v_{I2}$ can be written as:

$$v_{DI} = \sqrt{\frac{2}{\beta_n}} * (\sqrt{i_{D1}} - \sqrt{i_{D2}})$$

The maximum difference on the input voltage happens when M1 is conducting all of the current and M2 is off. This is equivalent to saying, $i_{D1} = Iss$ and $i_{D2} = 0$. So,

$$v_{D\,Im\,ax} = v_{I1\max} - 2.5V = \sqrt{\frac{2 * L * Iss}{K_{pn} * W}} \Rightarrow v_{I1\max} = 2.5V + \sqrt{\frac{2 * 2 * 40}{120 * 100}} = 2.615V$$

The minimum difference on the input voltage happens when M1 is off and M2 is conducting of the current. This is equivalent to saying, $i_{D1} = 0$ and $i_{D2} = Iss$. So,

$$v_{D\,Im\,in} = -v_{D\,Im\,ax} = -(v_{I1} - v_{I2}) = -\sqrt{\frac{2*L*Iss}{K_{pn}*W}} \Rightarrow 2.5V - \sqrt{\frac{2*2*40}{120*100}} = 2.384V$$

This means that our range is

$$2.384V < v_{DI} < 2.615V .$$

Comparing these values to those found in Example 22.1,

$$2.135V < v_{DI} < 2.865V .$$

It can be said that by increasing the Width of M1 and M2, the differential input range is decreased. This is verified in the figure 2.
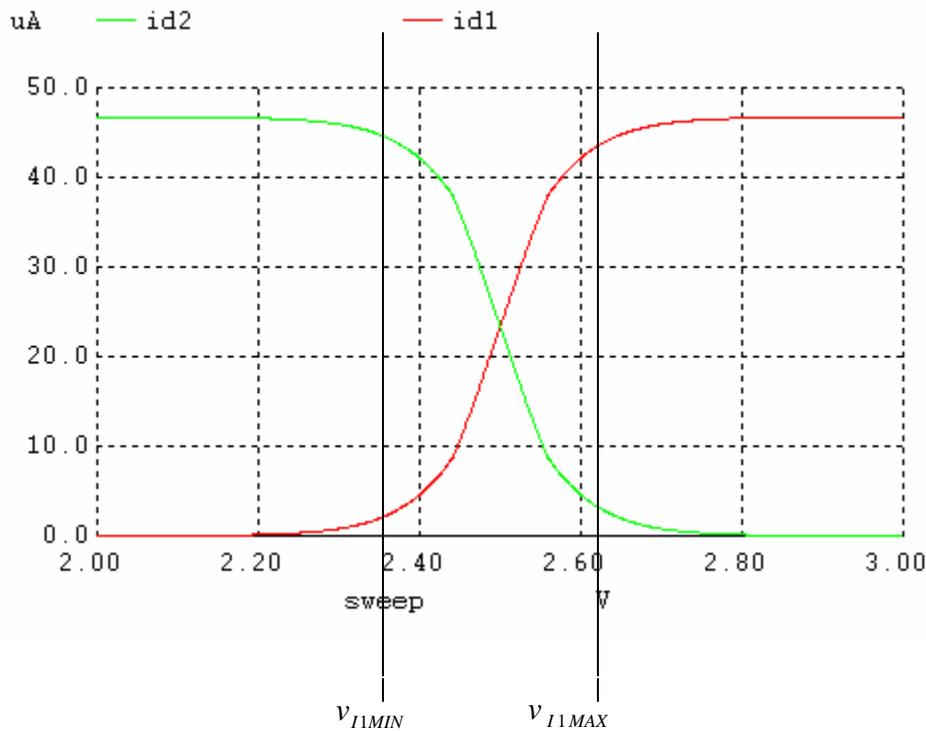

Figure 2.

To find the transconductance of the diff-amp, use equation 9.22.

$$g_{m1} = g_{m2} = g_m = \sqrt{\frac{2*K_{pn}*W \& *I_D}{2}} = 490 \,\mu A\big/V .$$

Below in figure3, is the small signal model.
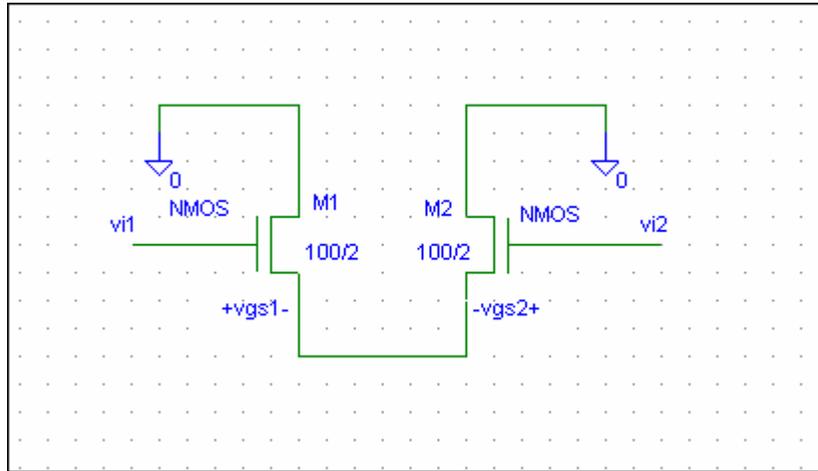
Figure3

From this figure we can write a KVL starting at v_{I1}.

$$v_{i1} = v_{gs1} - v_{gs2,} \text{ and knowing that } i_{d1} = g_m * v_{gs1} \text{ and } v_{gs1} = -v_{gs2},$$

$$v_{i1} = 2 * v_{gs1} \Rightarrow v_{gs1} = \frac{v_{i1}}{2}$$

$$\Rightarrow i_{d1} = gm * \frac{v_{i1}}{2} = 490 \frac{\mu A}{V} * \frac{v_{i1}}{2}$$

If we now have $V_{I1} = AC$ ground we have the same current, but in the opposite direction. Since $v_{gs1} = -v_{gs2}$ we can write

$$\Rightarrow i_{d2} = -gm * \frac{v_{i2}}{2} = -490 \frac{\mu A}{V} * \frac{v_{i2}}{2}$$

Finally if we want to write id with respect to $V_{DI=}(V_{I1} - V_{I2})$ we can write the KVL starting at V_{I1}.

$v_{i1} - v_{gs1} - (-v_{gs2}) - v_{i2} = 0$ and knowing that $v_{gs1} = -v_{gs2}$ this becomes

$$v_{i1} - v_{i2} + 2 \cdot v_{gs1} = 0, \text{ solving for } v_{gs1} \text{ gives us,}$$

$$v_{gs1} = \frac{-(v_{i1} - v_{i2})}{2}, \text{ plugging } v_{gs1} \text{ into our equation for } i_{d1},$$

$$\Rightarrow i_{d1} = \frac{-(v_{i1} - v_{i2})}{2} \cdot gm$$

*** Problem 22.2 CMOS: Circuit Design, Layout, and
Simulation ***

.control
destroy all
run
let id1=i(vid1)
let id2=i(vid2)
plot id1 id2
.endc

.option scale=1u
.dc Vi1 2 5 1m
**.op

VDD	VDD	0	DC	5
Vi1	vi1	0	DC	3.5
Vi2	vi2	0	DC	3.5
vid1	VDD	vd1	DC	0
Vid2	VDD	vd2	DC	0

M1	Vd1	vi1	vs1	0
	NMOS L=2 W=100			
M2	Vd2	vi2	vs2	0
	NMOS L=2 W=100			
M3	0	vb2	vs1	VDD
	PMOS L=2 W=30			
M4	0	vb1	vs2	VDD
	PMOS L=2 W=30			

M11	VDD	vi1	vs11	0
	NMOS L=2 W=10			
M41	vb1	vb1	vs11	VDD
	PMOS L=2 W=30			
MB1	vb1	Vbias3	vdb1	0
	NMOS L=2 W=10			
MB2	vdb1	vbias4	0	0
	NMOS L=2 W=10			

M21	VDD	vi2	vs22	0
	NMOS L=2 W=10			
M31	vb2	vb2	vs22	VDD
	PMOS L=2 W=30			
MB3	vb2	Vbias3	vdb2	0
	NMOS L=2 W=10			
MB4	vdb2	vbias4	0	0
	NMOS L=2 W=10			

Xbias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow
Vncas Vpcas bias

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow
Vncas Vpcas

MN1	Vbias2	Vbiasn	0	0
	NMOS L=2 W=10			
MN2	Vbias1	Vbiasn	0	0
	NMOS L=2 W=10			
MN3	Vncas	Vncas	vn1	0
	NMOS L=2 W=10			
MN4	vn1	Vbias3	vn2	0
	NMOS L=2 W=10			
MN5	vn2	vn1	0	0
	NMOS L=2 W=10			
MN6	Vbias3	Vbias3	0	0
	NMOS L=10 W=10			
MN7	Vbias4	Vbias3	Vlow	0
	NMOS L=2 W=10			
MN8	Vlow	Vbias4	0	0
	NMOS L=2 W=10			
MN9	Vpcas	Vbias3	vn3	0
	NMOS L=2 W=10			
MN10	vn3	Vbias4	0	0
	NMOS L=2 W=10			

MP1	Vbias2	Vbias2	VDD	VDD
	PMOS L=10 W=30			
MP2	Vhigh	Vbias1	VDD	VDD
	PMOS L=2 W=30			
MP3	Vbias1	Vbias2	Vhigh	VDD
	PMOS L=2 W=30			
MP4	vp1	Vbias1	VDD	VDD
	PMOS L=2 W=30			
MP5	Vncas	Vbias2	vp1	VDD
	PMOS L=2 W=30			
MP6	vp2	Vbias1	VDD	VDD
	PMOS L=2 W=30			
MP7	Vbias3	Vbias2	vp2	VDD
	PMOS L=2 W=30			
MP8	vp3	Vbias1	VDD	VDD
	PMOS L=2 W=30			
MP9	Vbias4	Vbias2	vp3	VDD
	PMOS L=2 W=30			
MP10	vp4	vp5	VDD	VDD
	PMOS L=2 W=30			
MP11	vp5	Vbias2	vp4	VDD
	PMOS L=2 W=30			
MP12	Vpcas	Vpcas	vp5	VDD
	PMOS L=2 W=30			

MBM1	Vbiasn	Vbiasn	0	0
	NMOS L=2 W=10			
MBM2	Vbiasp	Vbiasn	Vr	0
	NMOS L=2 W=40			
MBM3	Vbiasn	Vbiasp	VDD	VDD
	PMOS L=2 W=30			
MBM4	Vbiasp	Vbiasp	VDD	VDD
	PMOS L=2 W=30			

Rbias	Vr	0	6.5k	

MSU1	Vsur	Vbiasn	0	0
	NMOS L=2 W=10			
MSU2	Vsur	Vsur	VDD	VDD
	PMOS L=100 W=10			
MSU3	Vbiasp	Vsur	Vbiasn	0
	NMOS L=1 W=10			

.ends

Q) Determine the maximum and minimum common mode voltages for the PMOS version of the diff-amp seen in Fig. 22.4.
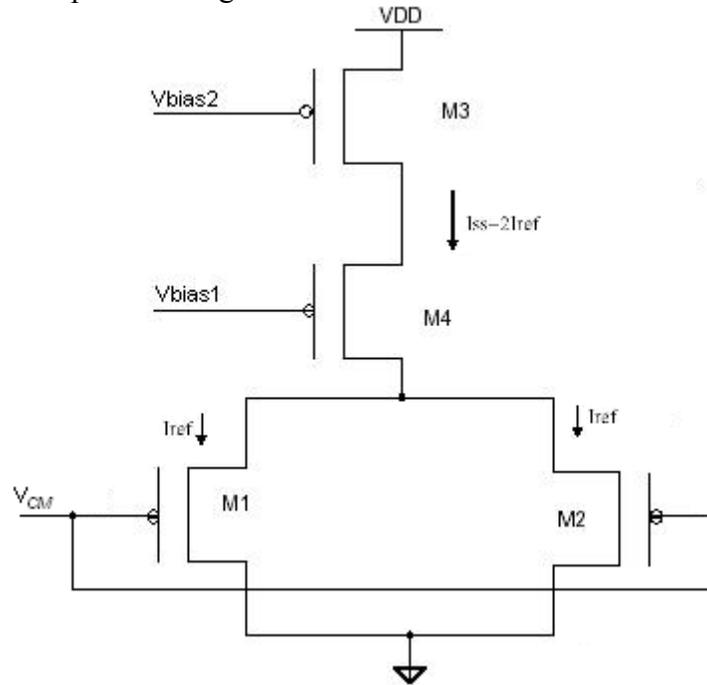
Solution: The minimum voltage at which the transistors M1 and M2 will operate in saturation
(That is, the transistors will just enter the saturation region). This voltage is called Minimum Common Mode voltage V_{CMMIN}. From the above figure, For M1 and M2 to be in saturation

$V_{SD} >= V_{SG} - V_{THP}$

$V_D <= V_G + V_{THP}$, V_D is nothing but Ground and V_G is V_{CMMIN}

$V_{CMMIN} = 0 - V_{THP} = -V_{THP}$

For long channel $V_{CMMIN} = -0.9V = -0.9V$ (From table 9.1)
For Short channel $V_{CMMIN} = -0.28V = -0.28V$ (From Table 9.2)

Maximum Common Mode voltage on gates of M1 or M2 can be written as minimum gate to source voltage on M1 or M2 plus the minimum voltage on source of M1 or M2 to maintain the I_{SS} current to flow and keep M3 and M4 in saturation. That turns out to be

$V_{CMMAX} = V_{DD} - V_{SG1or2} - 2 V_{SD, sat}$

$V_{CMMAX} = 5 - 1.15 - 2*0.25 = 3.35V$ (From table 9.1)
$V_{CMMAX} = 1 - 0.35 - 2*0.05 = 0.55V$ (From table 9.2)

Prepared by: Sandeep Pemmaraju and Vijay Srinivasan.

PROBLEM 22.4: To find the AC currents in all the branches of figure 22.5 with an ac voltage of 1mV applied to the gate of M2.

SOLUTION:
The small signal equivalent circuit may be represented as shown in the figure below:
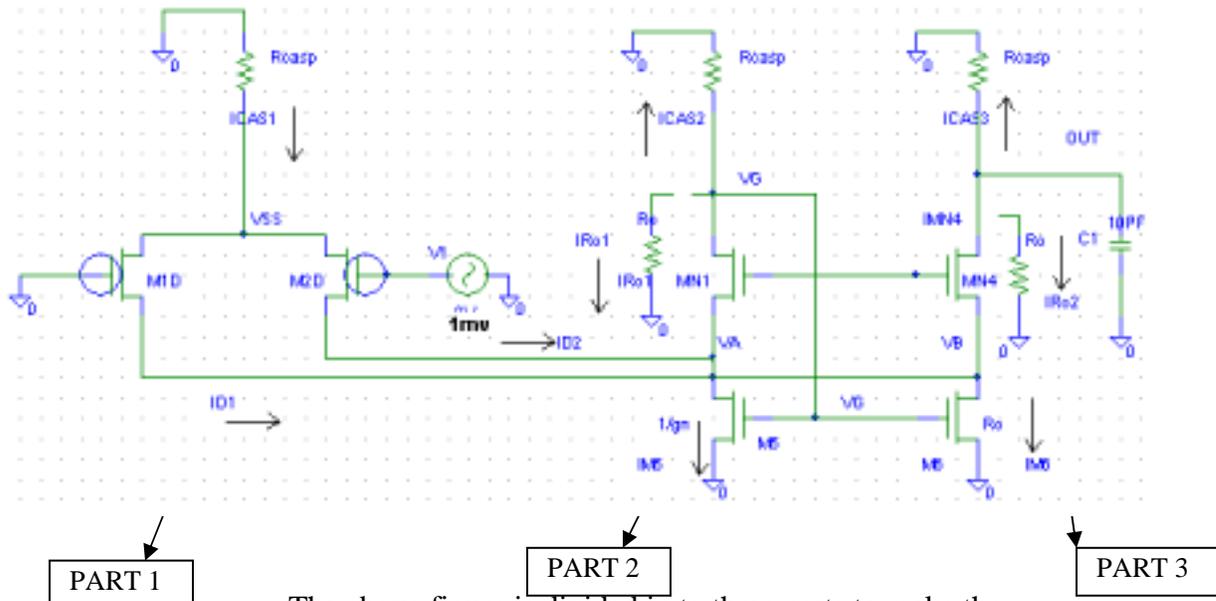
The above figure is divided in to three parts to make the calculations more clear to the reader. Here the voltage is assumed as 1mV peak to peak (since nothing is mentioned in the problem).

PART 1:
Part 1 deals with basic differential amplifier. An ac voltage source is applied to the gate of M2D. Simple KCL equations can be written at the node Vss to derive the currents entering the and leaving the node.

KCL @ node Vss:
Current flowing from Vss to VA via M2D $=I_{D2}$
Current flowing from Vss to VB via M1D $=I_{D1}$
Current flowing form ground to Vss via Rcasp$=I_{CAS1}$
Sum of Currents entering the node=Sum of Currents leaving the node

$\Rightarrow$ $I_{CAS1} = I_{D2} + I_{D1}$; where $I_{D2}= g_m .V_{sg}= g_m.(Vss-1mV)$

Similarly $I_{D1}=g_m. (Vss -0)=g_m. Vss$ and $I_{CAS1}= -Vss / Rcasp$.

$$Rcasp = g_{mp} \cdot rop^2 = 2.4 Gohms$$

So, $\qquad -\dfrac{Vss}{Rcasp1} = g_m.(Vss - 1mV) + g_m.Vss$

$$Vss(2.g_m + \dfrac{1}{Rcasp1}) = g_m.(1mV) \quad ; \quad \Rightarrow Vss(300u + 4.8n) = (150u).(1mV) ;$$

$\Rightarrow \qquad\qquad\qquad\qquad\quad Vss= +0.5\text{mV}\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots.(1)$

Simulated value = 0.45mV.

So, $\qquad$ Icasp1= -(Vss/Rcasp)=-(0.5m/2.4G)= -0.208pA…………………(2)

Simulated value=0.1pA. refer to figure 2.

Again, $\qquad I_{D1}= g_m. Vss=(150u).(0.5m)=75nA.$

$\qquad$ So, we can estimate I_{D2} as almost equal to I_{D1} as I_{CAS1} is very small compared to I_{D1}. $\Rightarrow I_{D2}=-I_{D1}=-75nA\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots.(3)$

Simulate values for I_{D1}, I_{D2} are both the same which being equal to 79nA.

Simulated values for PART 1 are as shown below:
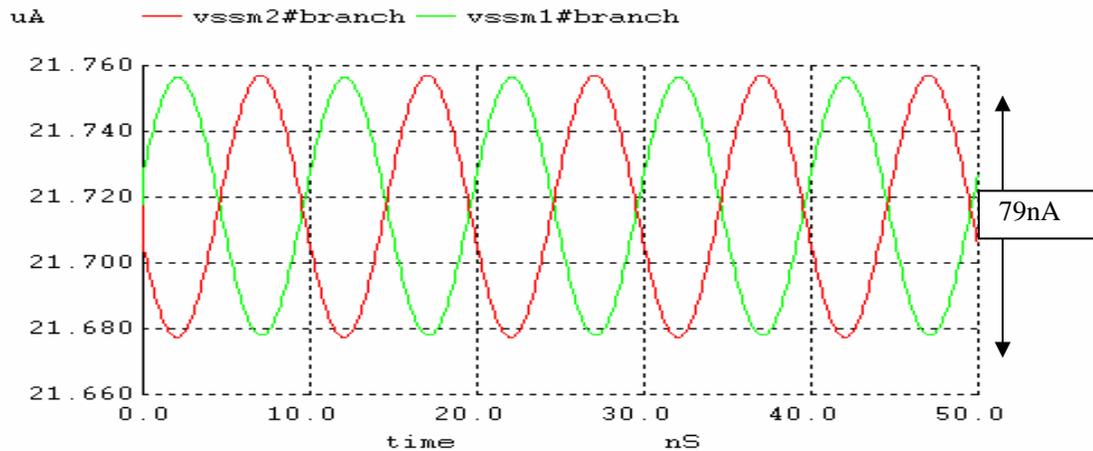
figure1: I_{D2} in green and I_{D1} in red
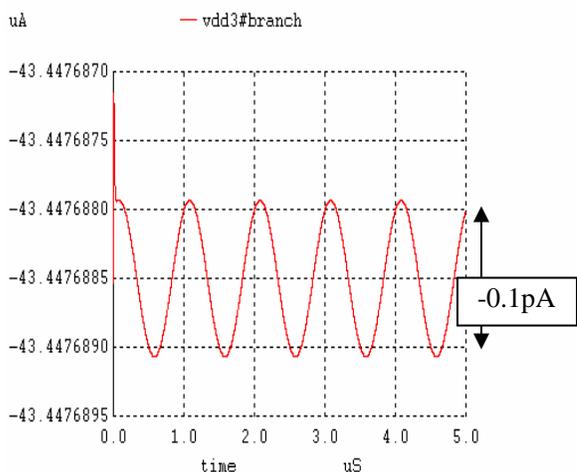
figure 2: I_{CAS1}
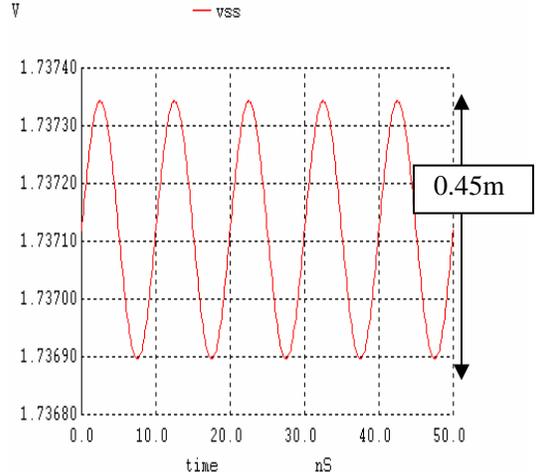

Figure 3: Vss

PART 2:
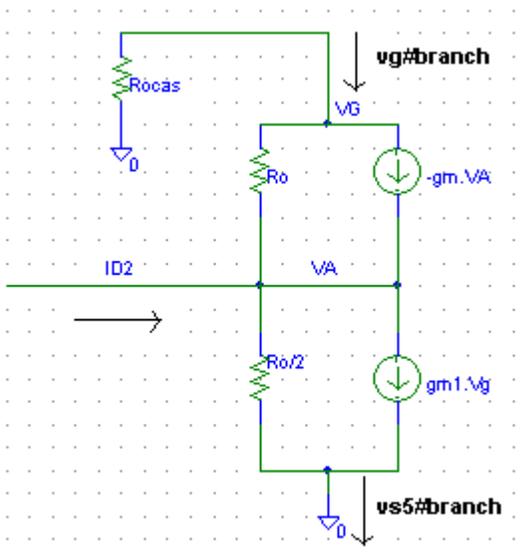
4. Figure showing the small signal equivalent of PART 2

The small signal equivalent circuit is usd to derive the currents in the respective branches of part2.

Writing KCL at node VA:

$$\frac{Vg - Vs}{Ro} - g_m.Vs - I_{d2} = \frac{2.Vs}{Ro} + \sqrt{2}g_mVg \dots\dots\dots\dots\dots\dots(4)$$

$$\frac{Vg}{Rocas} + \frac{Vg - Va}{Ro} - g_m Va = 0$$

$$Vg\left(\frac{1}{Ro} + \frac{1}{Rocas}\right) = Va\left(\frac{1}{Ro} + g_m\right) \quad \text{since } Rocas \gg Ro \text{ and } g_m \gg 1/Ro$$

$$Vg = \frac{Va.(g_m)}{(1/Ro)} = g_m.Ro.Va \dots \dots \dots \dots \dots \dots (5)$$

Substituting the value of (5) in equation (4)

$$\frac{Va(g_m Ro - 1)}{Ro} - g_m Va + Id2 = \frac{2.Va}{Ro} + \sqrt{2}g_m^2 Ro Va$$

$$Id2 = Va\left(\frac{2}{Ro} + \sqrt{2}g_m^2 Ro\right) \qquad \text{Since } 2/Ro \ll \text{ the second term}$$

$$Va = \frac{-75nA}{\sqrt{2}.(112500uA/V)} = -0.47uV$$

Simulated value for Va= -0.5uV refer to figure 6.b.Here the simulation is at 100KHz,this is because there were some iteration problems during the simulation and hance shifted the frequency,the frequency will not matter much as far as it is not changed a lot.Remaining simulations were done at 100MegHz.

Substituting the value of Va in equation (5)

Vg=-0.353mV……………………………..(6)

Simulated value for Vg=-0.35mV as shown in figure 7.

Simulations showing the currents in PART 2.
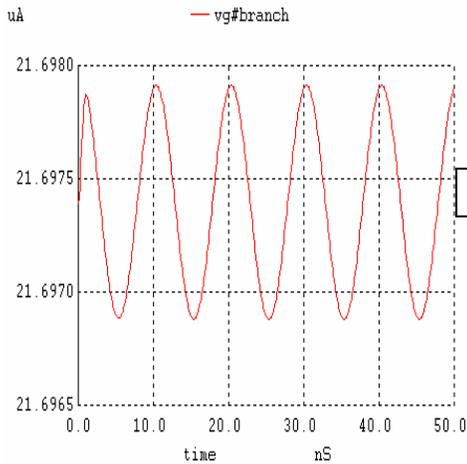
Figure 5. Current through MN1
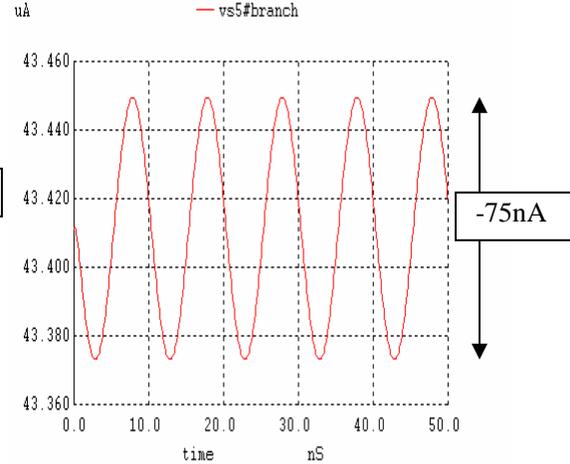
Figure6. Current through M5.
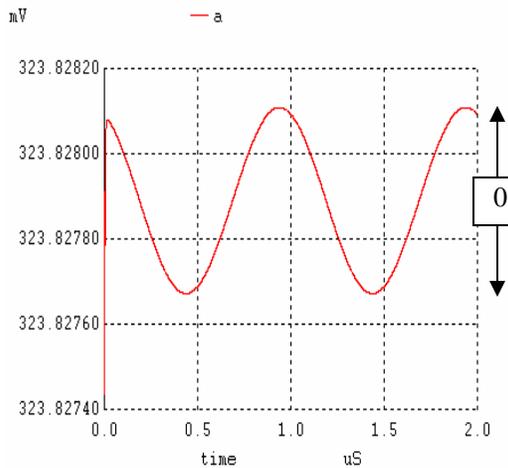
Figure6.b Showing the value of V_a.
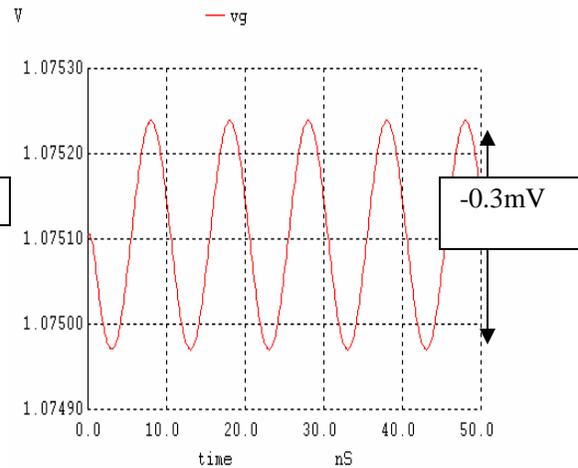
Figure 7 showing the voltage at node VG

Current through M5 is then given by:

$$IM5 = g_{m5}.Vg = \sqrt{2}.(150uA/V).(-0.353mV) = -74.8nA$$

Simulated value for I_{m5}=75nA Refer to figure 6.

.

PART 3:
Referring to the main circuit,the current flowing through M6 can be written as:

$I_{m6} = g_{m6}.V_{gs6}$; but as derived for the M6 the g_m is √2 times the normal MOSFET g_m. Also referring to equation (6) Vg=-0.353mV,

$\Rightarrow$ $I_{m6} = \sqrt{2}.(150uA/V).(-0.353mV) = 74.87nA$ Observe that the currents IM5 and Im6 are equal . Simulated value for I_{m6} =75nA as shown in figure 7.

Writing KCL at node B,
$$I_{D1} = IM5 - Iro2. \Rightarrow Iro2 = 75nA + 74.87nA = 149.87nA.$$

Simulated value for I_{ro2}=151nA as shown in figure 8.

The simulated currents are as shown in the figure below:
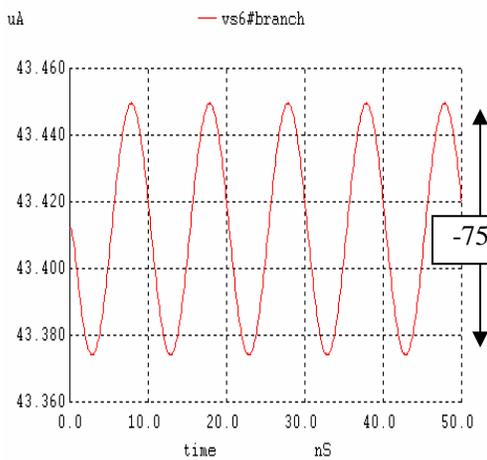

Figure7. Current through M6 (I_{m6})   Figure8.Current through the MN4(I_{ro2})
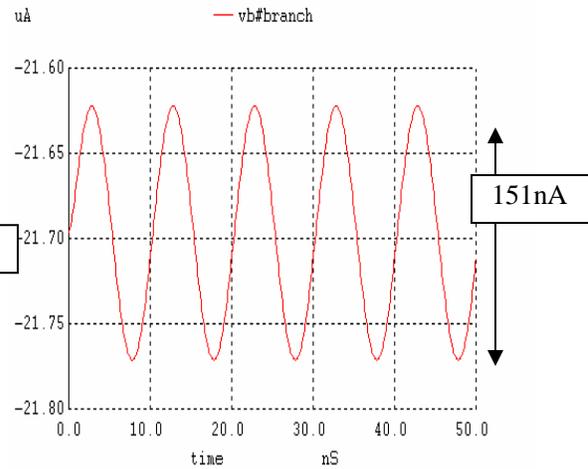
NETLIST:
****** Figure 20.44_NMOS CMOS: Circuit Design, Layout, and Simulation ***
.control
destroy all
run
.endc

.option scale=1u reltol=1u rshunt=1e9
.TRAN .1N 50n
*.OP

VDD	VDD	0	DC	5	
VG	VG1	VG	DC	0	
VPLUS	VPLUS	0	DC	0	SIN 0 0.5M 100MEG
VAA1	A	DC	0		
VBB	B1	DC	0		
VS5	S5	0	DC	0	
VS6	S6	0	DC	0	
VSSCAS	VSS	VSSCAS	DC	0	
VSSM1	VSS	VSSM1	DC	0	
VSSM2	VSS	VSSM2	DC	0	
vdd1	vdd	vdd1	dc	0	
vdd2	vdd	vdd2	dc	0	

```
vdd3        vdd     vdd3    dc      0
CLOAD       OUT     0       10P
Xbias       VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

MPx1        VC1     VBIAS1      VDD1    VDD         PMOS L=2 W=30
MPx2        VG1     VBIAS2      VC1     VDD         PMOS L=2 W=30
MNx1        VG      VBIAS3      A1      0           NMOS L=2 W=10
M5          A       VG          S5      0           NMOS L=2 W=20
M6          B       VG          S6      0           NMOS L=2 W=20
MNx4        OUT     VBIAS3      B1      0           NMOS L=2 W=10
MPx3        OUT     VBIAS2      VC2     VDD         PMOS L=2 W=30
MPx4        VC2     VBIAS1      VDD2    VDD         PMOS L=2 W=30

M4C         CAS1        VBIAS1      VDD3    VDD     PMOS L=2 W=60
M3C         VSSCAS      VBIAS2      CAS1    VDD     PMOS L=2 W=60
M1D         B           0           VSSM1   VDD     PMOS L=2 W=30
M2D         A           VPLUS       VSSM2   VDD     PMOS L=2 W=30

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas
MN1         Vbias2 Vbiasn 0         0           NMOS L=2 W=10
MN2         Vbias1 Vbiasn 0         0           NMOS L=2 W=10
MN3         Vncas  Vncas  vn1       0           NMOS L=2 W=10
MN4         vn1    Vbias3 vn2       0           NMOS L=2 W=10
MN5         vn2    vn1    0         0           NMOS L=2 W=10
MN6         Vbias3 Vbias3 0         0           NMOS L=10 W=10
MN7         Vbias4 Vbias3 Vlow      0           NMOS L=2 W=10
MN8         Vlow   Vbias4 0         0           NMOS L=2 W=10
MN9         Vpcas  Vbias3 vn3       0           NMOS L=2 W=10
MN10        vn3    Vbias4 0         0           NMOS L=2 W=10

MP1         Vbias2 Vbias2 VDD   VDD     PMOS L=10 W=30
MP2         Vhigh  Vbias1 VDD   VDD     PMOS L=2 W=30
MP3         Vbias1 Vbias2 Vhigh VDD     PMOS L=2 W=30
MP4         vp1    Vbias1 VDD   VDD     PMOS L=2 W=30
MP5         Vncas  Vbias2 vp1   VDD     PMOS L=2 W=30
MP6         vp2    Vbias1 VDD   VDD     PMOS L=2 W=30
MP7         Vbias3 Vbias2 vp2   VDD     PMOS L=2 W=30
MP8         vp3    Vbias1 VDD   VDD     PMOS L=2 W=30
MP9         Vbias4 Vbias2 vp3   VDD     PMOS L=2 W=30
MP10        vp4    vp5    VDD   VDD     PMOS L=2 W=30
MP11        vp5    Vbias2 vp4   VDD     PMOS L=2 W=30
MP12        Vpcas  Vpcas  vp5   VDD     PMOS L=2 W=30

MBM1        Vbiasn Vbiasn 0         0           NMOS L=2 W=10
MBM2        Vbiasp Vbiasn Vr        0           NMOS L=2 W=40
MBM3        Vbiasn         Vbiasp VDD   VDD   PMOS L=2 W=30
```

```
MBM4       Vbiasp Vbiasp VDD   VDD   PMOS L=2 W=30

Rbias      Vr     0       6.5k

MSU1       Vsur   Vbiasn 0       0       NMOS L=2   W=10
MSU2       Vsur   Vsur   VDD   VDD   PMOS L=100 W=10
MSU3       Vbiasp Vsur   Vbiasn 0       NMOS L=1   W=10
.ends
```

Problem 20.5 solution:
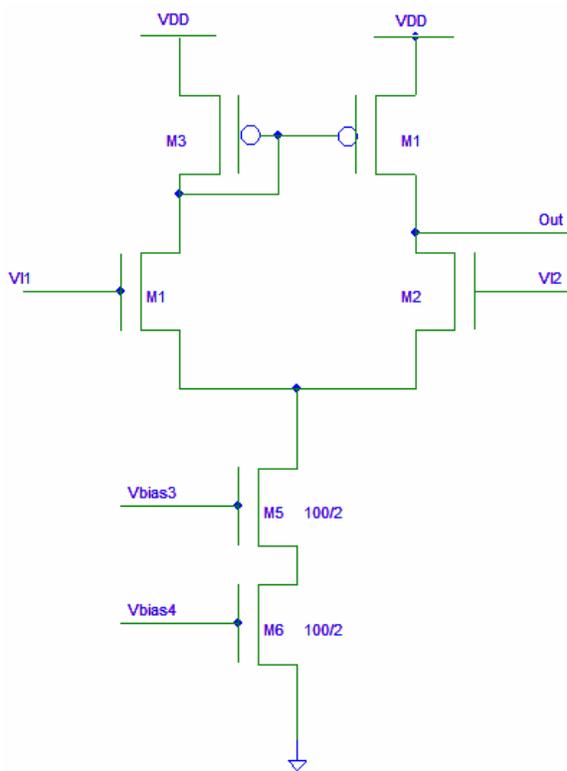
Fig 5a. Diff -Amp
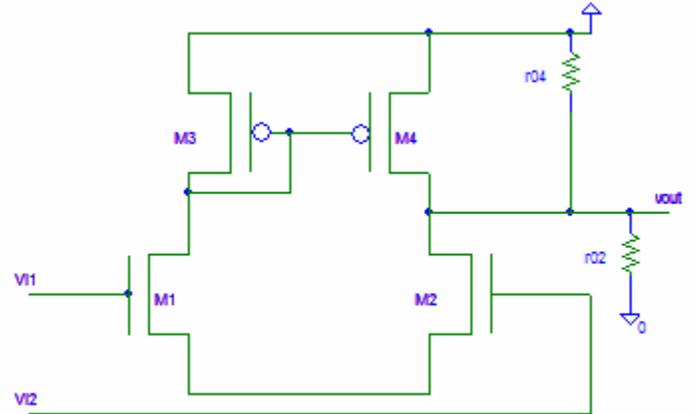
Fig 5b. AC circuit of diff -amp

NMOS Diff – Amp:

To determine the AC gain of the differential amplifier (diff amp) with current mirror load shown in Fig 5a, consider the small signal model shown in Fig 5b. Since M3 is a diode connected MOSFET, it can be replaced by a resistor of value 1/gm3. Also the resistance looking into the output of the diff amp is ro4 || ro2. Since the current in M4 is mirrored from the current in M3 and the current in M3 is equal to the current in M1, we can define the current in M4 as being equal to the current in M1, or id4 = id1. Since the total current current supplied by M1 and M2 is a constant value set by the current source devices M5 and M6, any changes in id1 will be equal and opposite to id2, or id1 = -id2. Therefore the output voltage can be written as:

$$v_{out} = (i_{d1} - i_{d2}) \cdot (r_{o4} \| r_{o2})$$

Since id1 = -id2 = id

$$v_{out} = 2i_{d} \cdot (r_{o4} \| r_{o2}).$$

Using KVL between the gate of M1 and the gate of M2 in Fig 5b:

$$v_{in1} = v_{gs1} - v_{gs2} + v_{in2}$$

$$v_{in1} - v_{in2} = v_{di} = v_{gs1} - v_{gs2}$$

Since id1 = -id2, any change in vgs1 will be equal and opposite in vgs2 or vgs1 = -vgs2

$$v_{in1} - v_{in2} = v_{di} = 2v_{gs1} = \frac{2i_d}{g_{mn}}$$

Therefore the differential mode gain, Ad is:

$$A_d = \frac{vout}{vdi} = g_{mn}.(ro2 \parallel ro4)$$

Plugging in g_{mn} = 150 uA/V, r_{o2} = 167 kohms, and r_{o4} = 333 kohms from Table 9.2 yields:

$$A_d = 16.7 \text{ V/V}$$

Another method to calculate the AC small signal gain of the diff amp involves converting transistors M2 and M4 into a current source of current gm * vgs in parallel to a resistor with a resistance equal to the output resistance of the MOSFET in saturation, ro. Applying KCL to the output node yields:

Vout / (ro4 || ro2) + gmn * vgs2 - gmp * vsg4 = 0

Since we know from Table 9.2 that gmn = gmp, we will replace both with gm. Also, since id is equal to gm * vgs and id4 is equal to id1, and taking into consideration that gmn = gmp, we know that:

gmn * vgs2 – gmp * vsg4 = gm * (vgs2 – vgs1) = gm * -vdi

Vout / (ro4 || ro2) = gm * vdi

Ad = Vout / vdi = gm * (ro4 || ro2) = 16.7 V/V

Determining the input CMR or the minimum and maximum gate voltage that can be applied simultaneously to both gates and still keep the diff amp transistors in saturation. When a maximum gate voltage is being applied, the head room between the source of M1 and M2 (VS12) and VDD is compressed. The minimum voltage difference between VDD and VS12 to keep M1 and M3 out of the triode region will be equal to Vovn + Vsg3 for the short channel process.

VDD – VS12 = Vovn + Vsg3

VS12 = VI2 – Vgs2 = VCMmax – Vgs2

Combining these two equations:

VDD – (VCMmax – Vgs2) = Vovn + Vsg3
VCMmax = VDD + Vgs2 – Vovn – Vsg3 = VDD + Vthn – Vsg3

Using these values from Table 9.2 - VDD = 1V, VGS = 0.35V, and Vovn = 70 mV:

VCMmax = 1V + 0.28V – 0.35V = 0.93V

When a minimum gate voltage is being applied, the head room between the source of M1 and M2 (VS12) and VSS is compressed. The minimum voltage difference between VS12 and VSS to keep M5 and M6 out of the triode region will be equal to 2 * Vovn for the short channel process.

VS12 = 2 * Vovn = VI2 – VGS2 = VCMmin – VGS2
VCMmin = VGS2 + 2 * Vovn

Using these values from Table 9.2 - VDD = 1V, VGS = 0.35V, and Vovn = 70 mV:

VCMmin = 0.35V + 2 * 0.07V = 0.49V

Another method to calculate VCMmax is to find the maximum vi that limits my M1 and M2 from going into the triode region. In order to keep M1 and M2 in saturation

$$V_{DS} \geq V_{GS} - V_{THN}$$
$$V_{D} \geq V_{G} - V_{THN} \quad \text{where} \quad V_{G} = V_{CMMAX}$$
$$V_{CMMAX} = V_{D} + V_{THN} ; \text{where drain of M1 and M2 are at } V_{DD} - V_{SG} \text{ of PMOS.}$$

Therefore
$$V_{CMMAX} = V_{DD} - V_{SG} + V_{THN}$$

Since $V_{DD} = 1V$, $V_{THN} = 280$ mV and $V_{SG} = 350$ mV

Therefore
$$V_{CMMAX} = 0.93V$$

Minimum vi is limited my M5 and M6 going into triode region. In order to keep M5 and M6 in saturation
$$v_{in} \geq V_{GS1,2} + 2.V_{OVN}$$
$$V_{CMMIN} = V_{GS1,2} + 2.V_{OVN}$$

Therefore
$$V_{CMMIN} = 0.49V$$

***Problem 22.5 N-MOS CMOS: Circuit Design, Layout, and Simulation ***
.control
destroy all
run
plot vout xlimit 300n 500n ylimit 620m 680m
.endc
.option scale=50n ITL1=300
.tran 5n 500n UIC

VDD	VDD	0	DC	1	
Vi1	Vi1	0	DC	0	sin 0.5 0.5m 10MEG
Vi2	Vi2	0	DC	0	sin 0.5 -0.5m 10MEG

M1	vd1	vi1	vsn	0	NMOS L=2 W=50
M2	vout	vi2	vsn	0	NMOS L=2 W=50
M3	vd1	vd1	VDD	VDD	PMOS L=2 W=100
M4	vout	vd1	VDD	VDD	PMOS L=2 W=100
Mb3	vsn	Vbias3	vn1	0	NMOS L=2 W=100
Mb4	vn1	Vbias4	0	0	NMOS L=2 W=100

Xbias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

******* THIS IS THE BIAS GENERATOR SUBCIRCUIT NETLIST ********
.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1	Vbias3	Vbiasp	VDD	VDD	PMOS L=2 W=100
MP2	Vbias4	Vbiasp		VDD	VDD	PMOS L=2 W=100
MP3	vp1	vp2	VDD	VDD	PMOS L=2 W=100
MP4	vp2	Vbias2	vp1	VDD	PMOS L=2 W=100
MP5	Vpcas	Vpcas	vp2	VDD	PMOS L=2 W=100
MP6	Vbias2	Vbias2	VDD	VDD	PMOS L=10 W=20
MP7	Vhigh	Vbias1	VDD	VDD	PMOS L=2 W=100
MP8	Vbias1	Vbias2	Vhigh	VDD	PMOS L=2 W=100
MP9	vp3	Vbias1	VDD	VDD	PMOS L=2 W=100
MP10	Vncas	Vbias2	vp3	VDD	PMOS L=2 W=100

MN1	Vbias3	Vbias3	0	0	NMOS L=10 W=10
MN2	Vbias4	Vbias3	Vlow	0	NMOS L=2 W=50
MN3	Vlow	Vbias4	0	0	NMOS L=2 W=50
MN4	Vpcas	Vbias3	vn1	0	NMOS L=2 W=50
MN5	vn1	Vbias4	0	0	NMOS L=2 W=50
MN6	Vbias2	Vbias3	vn2	0	NMOS L=2 W=50
MN7	vn2	Vbias4	0	0	NMOS L=2 W=50
MN8	Vbias1	Vbias3	vn3	0	NMOS L=2 W=50
MN9	vn3	Vbias4	0	0	NMOS L=2 W=50

```
MN10  Vncas  Vncas  vn4    0      NMOS L=2 W=50
MN11  vn4    Vbias3 vn5    0      NMOS L=2 W=50
MN12  vn5    vn4    0      0      NMOS L=2 W=50

MBM1 Vbiasn Vbiasn 0      0      NMOS L=2 W=50
MBM2 Vreg   Vreg   Vr     0      NMOS L=2 W=200
MBM3 Vbiasn Vbiasp VDD    VDD    PMOS L=2 W=100
MBM4 Vreg   Vbiasp VDD    VDD    PMOS L=2 W=100

Rbias  Vr     0      5.5k

*amplifier
MA1   Vamp  Vreg   0      0      NMOS L=2 W=50
MA2   Vbiasp Vbiasn 0     0      NMOS L=2 W=50
MA3   Vamp  Vamp   VDD    VDD    PMOS L=2 W=100
MA4   Vbiasp Vamp  VDD    VDD    PMOS L=2 W=100

MCP   VDD   Vbiasp VDD    VDD    PMOS L=100 W=100

*start-up stuff
MSU1  Vsur   Vbiasn 0     0      NMOS L=2  W=50
MSU2  Vsur   Vsur   VDD   VDD    PMOS L=20 W=10
MSU3  Vbiasp Vsur   Vbiasn 0     NMOS L=1  W=10

.ends
```

SIMULATION RESULTS FOR AC GAIN
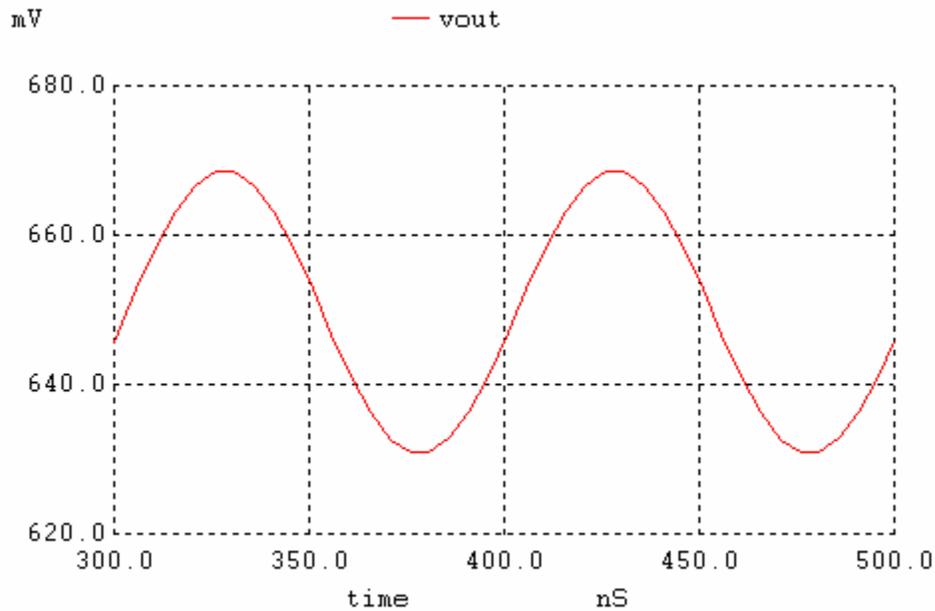
The input voltage differential between the two gates of M1 and M2 for the simulation was set at 1 mV. From the graph, the amplitude of the vout waveform is 18mV for a gain, vout / vin of 18 V/V. This value verifies our 16.7 V/V calculated value.

CMR SIMULATION RESULTS
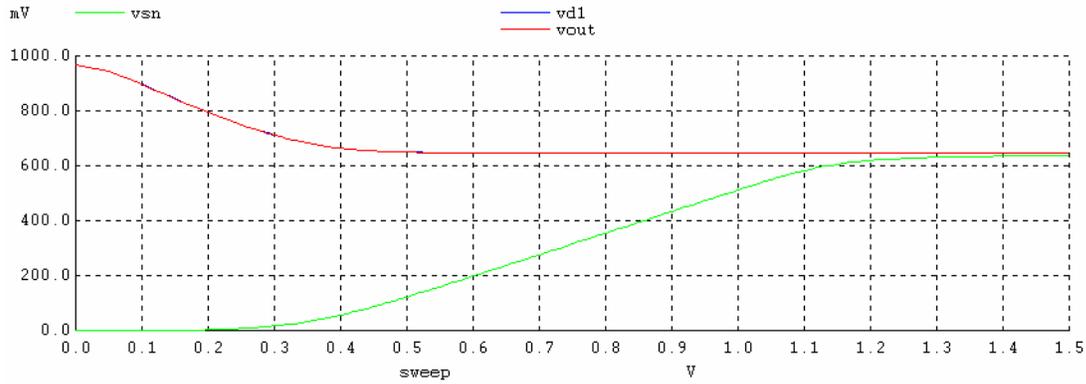
VOUT, VD1, AND VSN (VS12) VERSUS VI1 (GATE OF M1 & M2
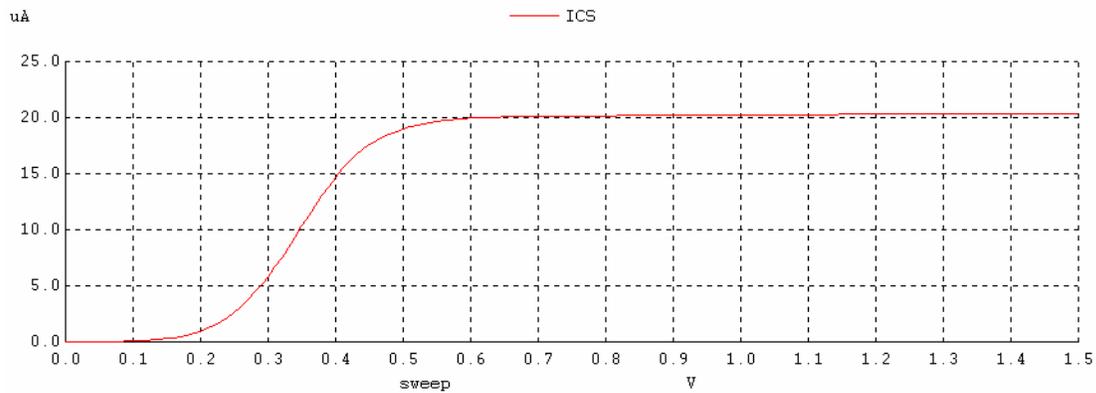
CURRENT SOURCE CURRENT VERSUS VI1

The VCMmin is the voltage where the current source (M5 & M6) enters the saturation region. From the ICS versus VI1 plot, the ICS switch from the triode to the saturation at approximately 0.54V. Also notice that vout flattens off at approximately 0.52V. The VCMmax can be measured by determining where vsn stops linearly following VI1 which was at 1.13V. Notice that vsn minus vout at this point is approximately Vovn. The VCMmax was calculated to be 0.93V and VCMmin was calculated to be 0.49V.

PMOS Diff – Amp:
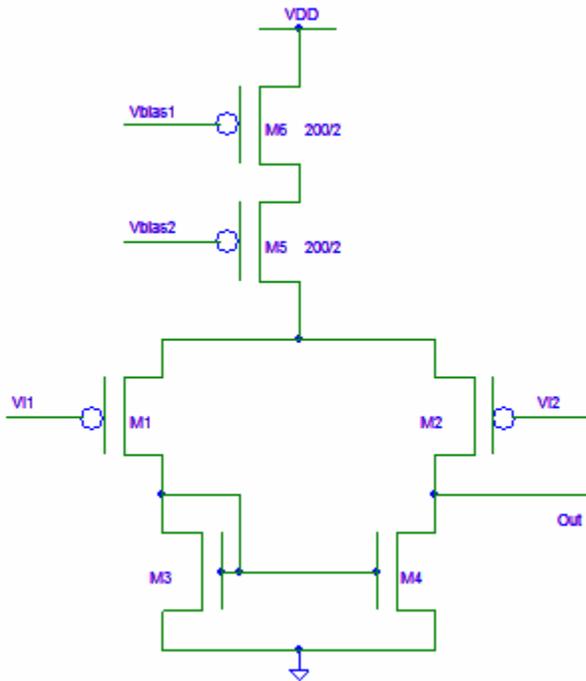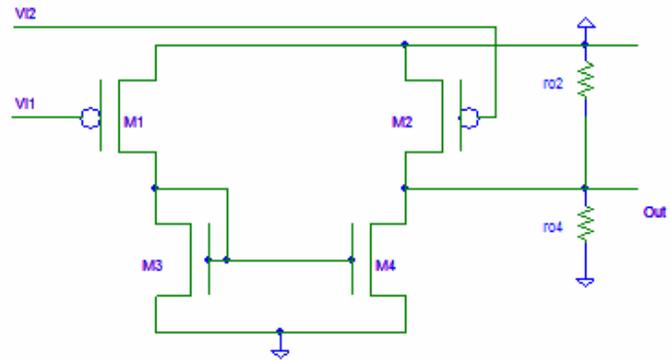
Fig 5c. PMOS Diff –Amp   Fig 5d. AC circuit of PMOS diff -amp

To determine AC gain of diff amp with current mirror load shown in Fig 5c, consider the small signal model seen in Fig 5d. Since M3 is a diode connected MOSFET, it can be replaced by a resistor of value 1/gm3. Also the resistance looking into the output of the diff amp is ro4 || ro2. Since the current in M4 is mirrored from the current in M3 and the current in M3 is equal to the current in M1, we can define the current in M4 as being equal to the current in M1, or id4 = id1. Since the total current current supplied by M1 and M2 is a constant value set by the current source devices M5 and M6, any changes in id1 will be equal and opposite to id2, or id1 = -id2. Therefore the output voltage can be written as:

$$v_{out} = (i_{d1} - i_{d2}).(r_{o4} \| r_{o2})$$

Since id1=-id2=id

$$v_{out} = 2i_d . (r_{o4} \| r_{o2}).$$

Using KVL between the gate of M1 and the gate of M2 in Fig 5d:

$$v_{in1} = v_{sg1} - v_{sg2} + v_{in2}$$

$$v_{in1} - v_{in2} = v_{di} = v_{sg1} - v_{sg2}$$

Since id1=-id2, therefore vsg1= -vsg2

$$v_{in1} - v_{in2} = v_{di} = 2v_{sg1} = \frac{2i_d}{g_{mp}}$$

Therefore differential mode gain is

$$A_d = \frac{vout}{vdi} = g_{mp}.(ro2 \parallel ro4)$$

Since $g_{mn} = 150$ uA/V and $r_o = 333$ kohms

$$A_d = 16.7 \text{ V/V}$$

Another method to calculate the AC small signal gain of the diff amp involves converting transistors M2 and M4 into a current source of current gm * vgs in parallel to a resistor with a resistance equal to the output resistance of the MOSFET in saturation, ro. Applying KCL to the output node yields:

Vout / (ro4 || ro2) + gmn * vgs2 - gmp * vsg4 = 0

Since we know from Table 9.2 that gmn = gmp, we will replace both with gm. Also, since id is equal to gm * vgs and id4 is equal to id1, and taking into consideration that gmn = gmp, we know that:

gmn * vgs2 – gmp * vsg4 = gm * (vgs2 – vgs1) = gm * -vdi

Vout / (ro4 || ro2) = gm * vdi

Ad = Vout / vdi = gm * (ro4 || ro2) = 16.7 V/V

Determining the input CMR or the minimum and maximum gate voltage that can be applied simultaneously to both gates and still keep the diff amp transistors in saturation. When a maximum gate voltage is being applied, the head room between the source of M1 and M2 (VS12) and VDD is compressed. The minimum voltage difference between VDD and VS12 to keep M5 and M6 out of the triode region will be equal to 2 * Vovp for the short channel process.

VDD – VS12 = 2 * Vovp

VS12 = VI2 + VSG2 = VCMmax + VGS2

Combining these two equations:

VDD – (VCMmax + VGS2) = 2 * Vovp

VCMmax = VDD - VGS2 – 2 * Vovp

Using these values from Table 9.2 - VDD = 1V, VGS = 0.35V, and Vovp = 70 mV:

VCMmax = 1V - 0.35V – 2 * 0.07V = 0.51V

When a minimum gate voltage is being applied, the head room between the source of M1 and M2 (VS12) and VSS is compressed. The minimum voltage difference between VS12 and VSS to keep M1 and M3 out of the triode region will be equal to Vovp + Vgs1 for the short channel process.

VS12 = Vovp + Vgs1 = VI2 + VGS2 = VCMmin + VGS2

VCMmin = Vovp + Vgs1 – VGS2

Using these values from Table 9.2 - VDD = 1V, VGS = 0.35V, and Vovn = 70 mV:

VCMmin = 0.07V + 0.35 – 0.35V = 70 mV

Here is another method to calculate the input CMR or the minimum and maximum gate voltage that can be applied simultaneously to both gates and still keep the diff amp transistors in saturation. When a maximum gate voltage is being applied, the head room between the source of M1 and M2 (VS12) and VDD is compressed. The minimum voltage difference between VDD and VS12 to keep M2 and M4 out of the triode region will be greather than or equal to 2 * Vovn for the short channel process.

$$V_{DD} - V_{S12} \geq 2\ V_{OVP}$$

Where $V_{S12} = V_{I1} - V_{GS1}$,and $V_{I1} = V_{CMMAX}$

Therefore
$$V_{I1} \leq V_{DD} - 2V_{OVP} - V_{SG1}$$
Therefore
$$V_{CMMAX} = V_{DD} - 2V_{OVP} - V_{SG1}$$

Therefore
$$V_{CMMAX} = 0.51V$$

Minimum vi is limited my M1 and M2 going into triode region. In order to keep M1 and M2 in saturation
$$V_{SD1} \geq V_{SG1} - V_{THP}$$
$$V_{D1} \leq V_{G1} + V_{THP} \text{ where } V_{G1} = V_{CMMIN}$$

Therefore

$$V_{CMMIN} = V_{D1} - V_{THP} \quad ;where \ V_{D1} = V_{GS3}$$
$$where \ V_D = 350mV \ and \ V_{THP} = 280mv$$

Therefore
$$V_{CMMIN} = 70mV$$

This folowing netlist was used to simulate the gain:

```
***Problem 22.5 PMOS CMOS: Circuit Design, Layout, and Simulation ***
.control
destroy all
run
plot vout xlimit 300n 500n ylimit 300m 400m
.endc
.option scale=50n ITL1=300
.tran 5n 500n UIC


VDD   VDD   0        DC    1
Vi1   Vi1   0        DC    0        sin 0.5 0.5m 10MEG
Vi2   Vi2   0        DC    0        sin 0.5 -0.5m 10MEG


Mb1   vdb1  Vbias1 vdd    vdd      PMOS L=2 W=200
Mb2   vsn   Vbias2 vdb1   vdd      PMOS L=2 W=200


M1    vd1   vi1    vsn    vdd      PMOS L=2 W=100
M3    vd1   vd1    0      0        NMOS L=2 W=50


M2    vout  vi2    vsn    vdd      PMOS L=2 W=100
M4    vout  vd1    0      0        NMOS L=2 W=50


Xbias   VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

*** INSERT THE BIAS GENERATOR SUBCIRCUIT AND MODELS HERE ***
```

SIMULATION RESULTS FOR AC GAIN
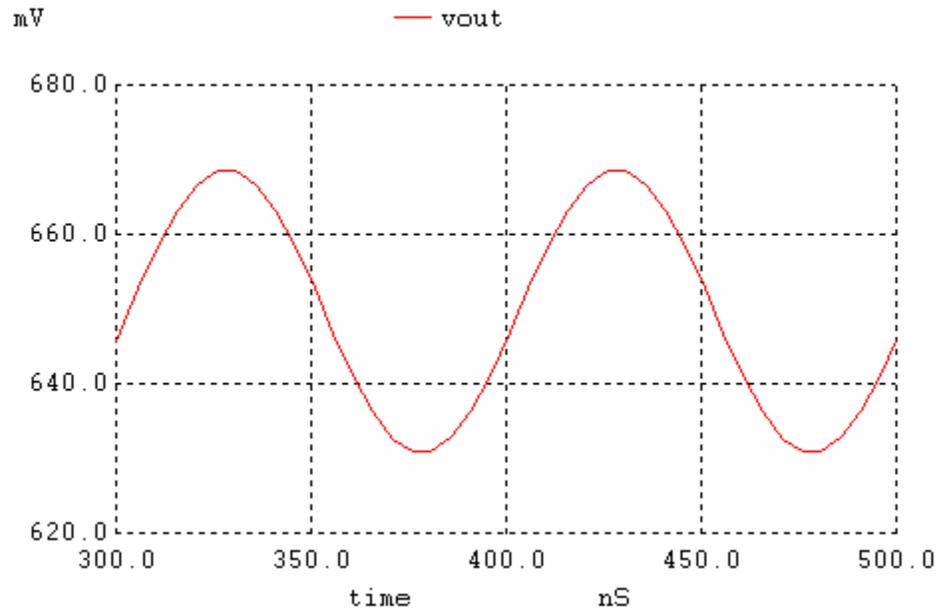

The input voltage differential between the two gates of M1 and M2 for the simulation was set at 1 mV. From the graph, the amplitude of the vout waveform is 18mV for a gain, vout / vin of 18 V/V. This value verifies our 16.7 V/V calculated value.

## CMR SIMULATION RESULTS
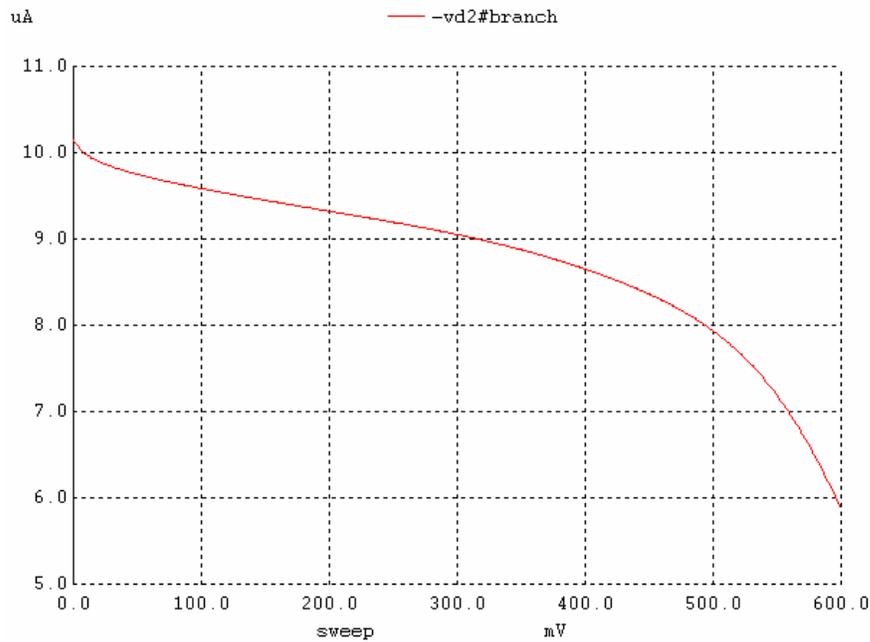
Above figure shows sweeping of Vin1 from 0 to 600 mV with Vin2=0 V_{CMMIN}=20 mv (calculated shows 70 mv) and VCMMAX=530 mV(Calculated shows 510 mV)
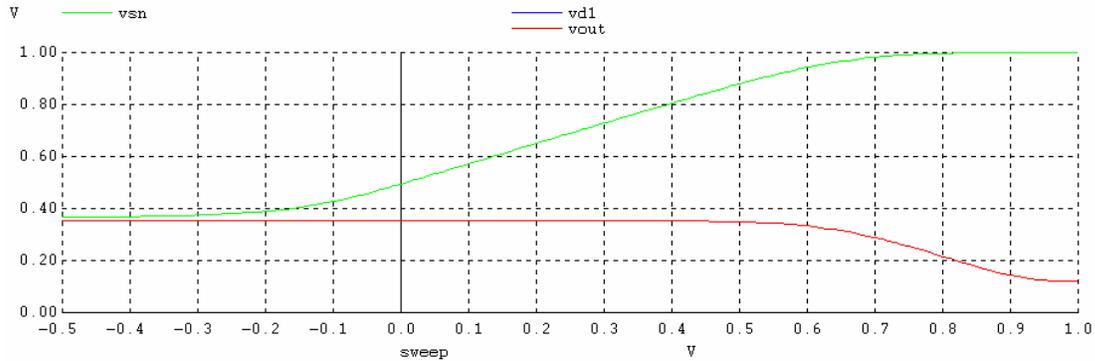
Vout, VD1, AND Vsn (VS12) VERSUS VI1 (GATE OF M1 & M2
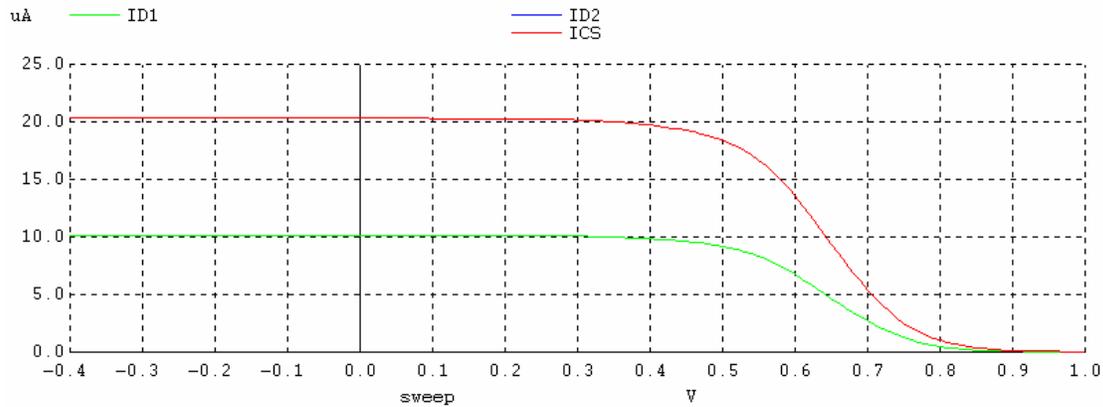
CURRENT SOURCE CURRENT VERSUS VI1

If we measure the VCMmax from the plot of Vout versus VI1, we pick the point where Vout remains constant or VI1 equal to 0.52V. If we measure the VCMmax from the plot of Ics versus VI1, we pick the point where Ics moves out of the triode region and into the saturation region or 0.47V. The VCMmin is measured in the Vout versus VI1 plot as the point where the difference between Vout and Vsn is approximately 70mV or the Vovp voltage. This point is at approximately –0.1V. The calculated value for VCMmax was 0.53V and VCMmin was 70mV.

Problem 22.6 Solution by Russell A. Benson – CNS and Robert J. Hanson, CNS:

Show that the capacitance on the sources of M1/M2 in example 22.6 causes the CMRR to roll off quicker with increasing frequency.

From equation 22.27:
CMRR = 20*log (|Ad/Ac|) = 20*log(gm1,2*(ro2//ro4)*2gm3,4*Ro)
Where Ad = gm1,2*(ro2//ro4) and Ac = 1/(2gm3,4*Ro)

However when a capacitance (Csource) is added on the source of M1/M2 the common mode gain (Ac) increases at higher frequencies, while the differential gain (Ad) remains unchanged:

Adding a Csource and using KCL yields the following, where vss is the voltage on the source of M1/M2:

(vss-0) / Ro + (vss-0) / (1 / jwCsource) = 2*id

Solving for vss yields:

vss = 2id/(1/Ro + jwCsource)

Solving for vc (used to determine Ac with a Csource added) yields:
vc = vgs1,2 + vss = id/gm1,2 + 2id/(1/Ro + jwCsource) =
= vc = id*(1/gm1,2 + 2/(1/Ro + jwCsource)

And knowing that vout = id / gm3,4 due to symmetry.

Solving for Ac yields the following result:

Ac = vout / vc = (id / gm3) / [id*(1/gm1,2 + 2/(1/Ro + jwCsource)]

Assuming that Ro is much larger than 1/gm1,2 simplifies Ac to:

Ac = (1/gm3) / [2/(1/Ro + jwCsource)]

Now plugging Ac into the CMRR equation results in:

CMRR = 20*log (|Ad/Ac|) = 20*log(gm1,2*(ro2//ro4)*2gm3,4*1/[1/Ro + jwCsource])

• This shows that for a Csource added, the CMRR rolls off quicker with increasing frequency. Note that when Csource is very large it can cause CMRR to roll off at even lower frequencies.

• The best way to limit the parasitic capacitances at the source is with a good layout design that minimizes the size (area) of the shared source regions of M1/M2.

SIMULATIONS:
The SPICE simulations below illustrate the concept of the CMRR roll off by adding a different Csource capacitor in each example.

• The spice simulations below illustrate the CMRR of the circuit in Example 22.6 driving a load of 1pF, here Csource=0. CMRR roll off begins at approximately 10 MHz.
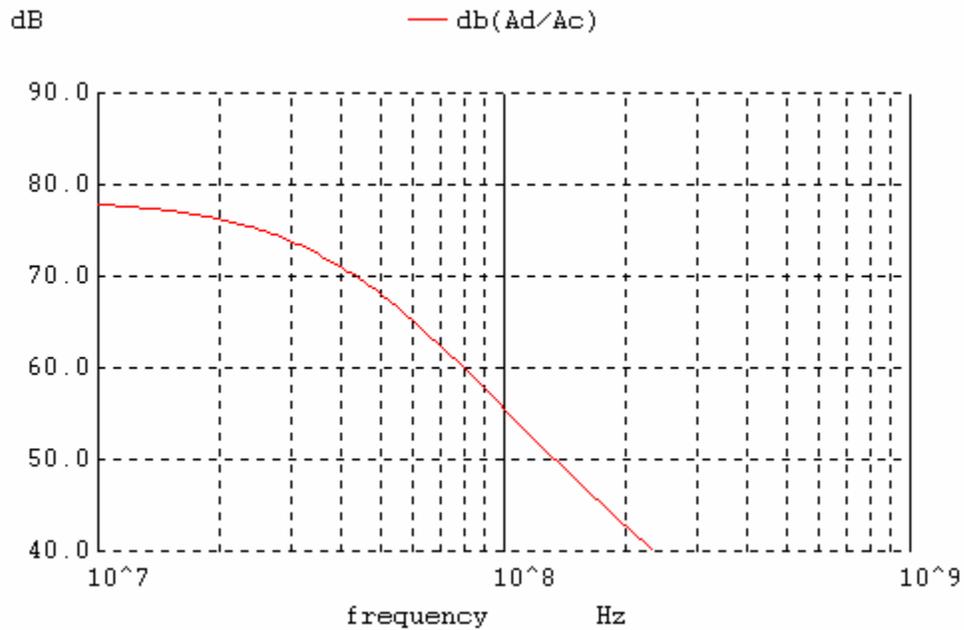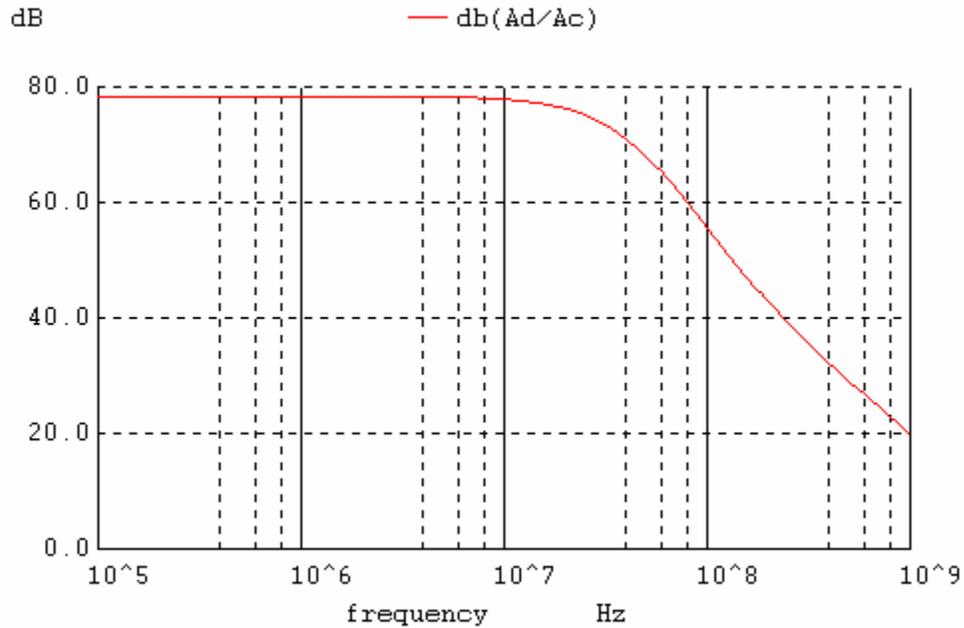
● The spice simulations below illustrate the CMRR of the circuit in Example 22.6 driving a load of 1pF with a Csource of 3fF added at the source of M1/M2. Notice that the CMRR roll off begins earlier than in the previous simulation, at about 9 MHz. Note that at a high frequency of 1GHz the CMRR is about 16.5, which is less than it was in the above simulations (20dB @ 1GHz),
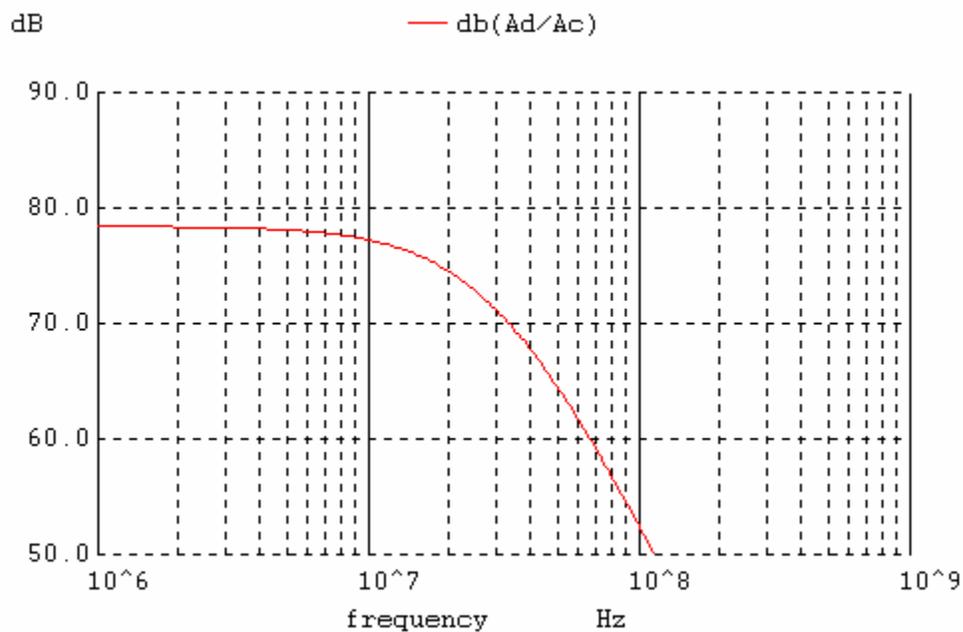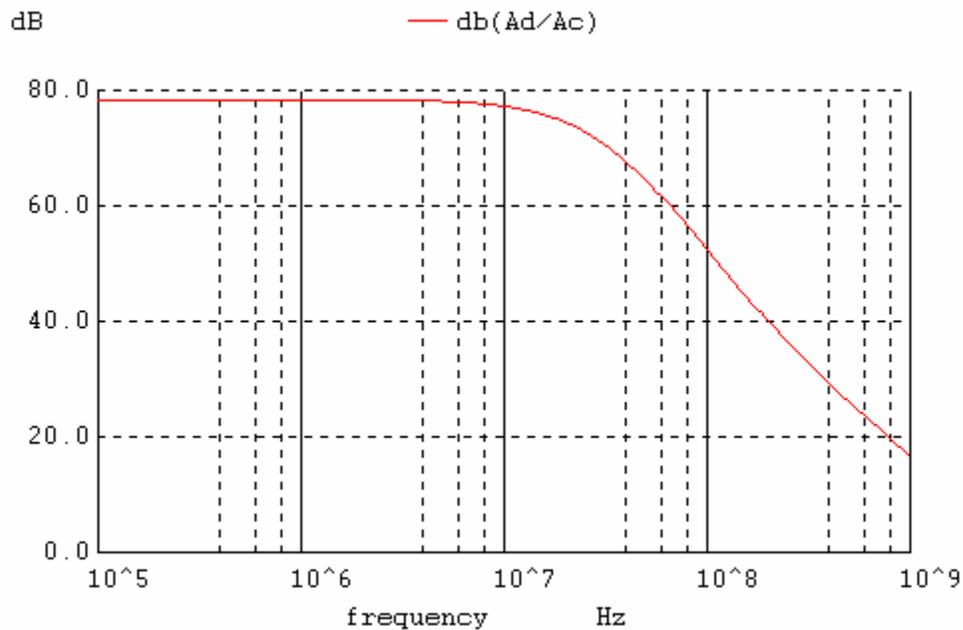
- The spice simulations below illustrate the CMRR of the circuit in Example 22.6 driving a load of 1pF with a larger Csource of 30fF added at the source of M1/M2. Notice that the CMRR roll off begins quite a bit earlier than in the previous simulations, at about 2 MHz. That is because a much larger capacitance of 30fF is used in this example. The high frequency CMRR at 1GHz is also much less than the above 2 examples, it is approximately 6dB.
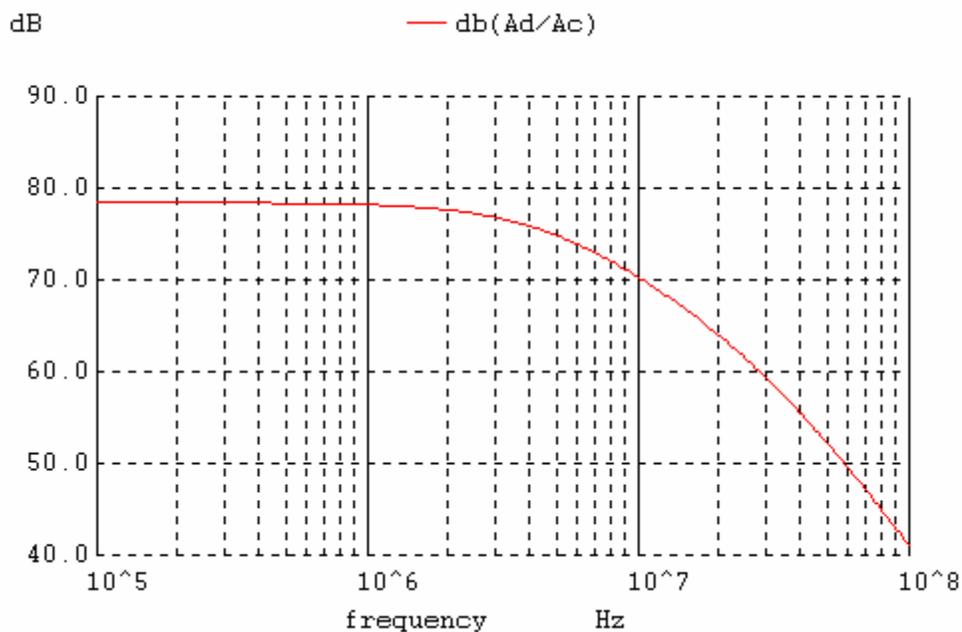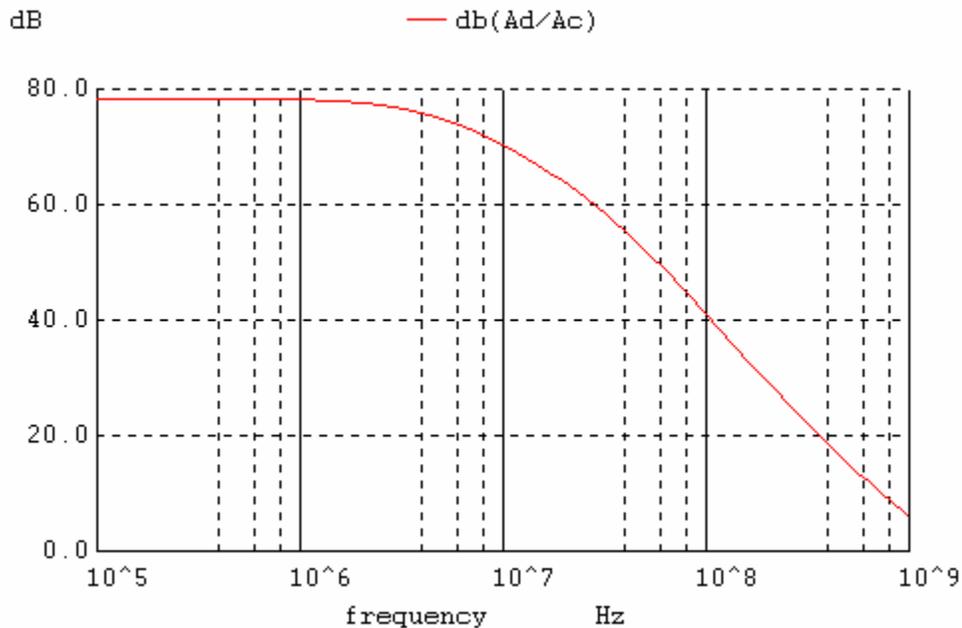
The SPICE netlist for the above simulation is provided below for reference (note that it excludes the BSIM4 50nm model parameters to make the netlist shorter):

*** Problem 22.6 Solution by Russ Benson - CNS and Robert Hanson, CNS ***

```
.control
destroy all
run
plot db(Ad/Ac)
.endc

.option scale=50n ITL1=300 rshunt=1e8
.ac dec 100 100k 1000MEG

VDD      VDD     0        DC      1

Vi1      Vi1     0        DC      0.7      AC 1
Vi2      Vi2     0        DC      0.7

Vc       Vc      0        DC      0.7      AC 1


Xbias    VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias
X1       VDD      Vbias3   Vbias4   vc       vc       Ac        diff_amp
X2       VDD      Vbias3   Vbias4   vi1      vi2      Ad        diff_amp

.subckt diff_amp VDD       Vbias3   Vbias4   vi1      vi2       vout

M1       vd1     vi1      vss      0        NMOS L=2 W=50
M2       vout    vi2      vss      0        NMOS L=2 W=50
MB1      Vdb1    Vbias4   0        0        NMOS L=2 W=100
MB2      vss     Vbias3   vdb1     0        NMOS L=2 W=100
M3       vd1     vd1      VDD      VDD      PMOS L=2 W=100
M4       vout    vd1      VDD      VDD      PMOS L=2 W=100

Cload    vout    0        1p
Csource  vss     0        30f

.ends

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1      Vbias3   Vbiasp   VDD      VDD      PMOS L=2 W=100
MP2      Vbias4   Vbiasp   VDD      VDD      PMOS L=2 W=100
MP3      vp1      vp2      VDD      VDD      PMOS L=2 W=100
MP4      vp2      Vbias2   vp1      VDD      PMOS L=2 W=100
MP5      Vpcas    Vpcas    vp2      VDD      PMOS L=2 W=100
MP6      Vbias2   Vbias2   VDD      VDD      PMOS L=10 W=20
MP7      Vhigh    Vbias1   VDD      VDD      PMOS L=2 W=100
MP8      Vbias1   Vbias2   Vhigh    VDD      PMOS L=2 W=100
MP9      vp3      Vbias1   VDD      VDD      PMOS L=2 W=100
MP10     Vncas    Vbias2   vp3      VDD      PMOS L=2 W=100

MN1      Vbias3   Vbias3   0        0        NMOS L=10 W=10
MN2      Vbias4   Vbias3   Vlow     0        NMOS L=2 W=50
MN3      Vlow     Vbias4   0        0        NMOS L=2 W=50
MN4      Vpcas    Vbias3   vn1      0        NMOS L=2 W=50
MN5      vn1      Vbias4   0        0        NMOS L=2 W=50
MN6      Vbias2   Vbias3   vn2      0        NMOS L=2 W=50
MN7      vn2      Vbias4   0        0        NMOS L=2 W=50
MN8      Vbias1   Vbias3   vn3      0        NMOS L=2 W=50
MN9      vn3      Vbias4   0        0        NMOS L=2 W=50
MN10     Vncas    Vncas    vn4      0        NMOS L=2 W=50
MN11     vn4      Vbias3   vn5      0        NMOS L=2 W=50
MN12     vn5      vn4      0        0        NMOS L=2 W=50

MBM1     Vbiasn   Vbiasn   0        0        NMOS L=2 W=50
MBM2     Vreg     Vreg     Vr       0        NMOS L=2 W=200
MBM3     Vbiasn   Vbiasp   VDD      VDD      PMOS L=2 W=100
MBM4     Vreg     Vbiasp   VDD      VDD      PMOS L=2 W=100

Rbias    Vr      0        5.5k
```

```
*amplifier
MA1     Vamp    Vreg    0       0       NMOS L=2 W=50
MA2     Vbiasp  Vbiasn  0       0       NMOS L=2 W=50
MA3     Vamp    Vamp    VDD     VDD     PMOS L=2 W=100
MA4     Vbiasp  Vamp    VDD     VDD     PMOS L=2 W=100

MCP     VDD     Vbiasp  VDD     VDD     PMOS L=100 W=100

*start-up stuff
MSU1    Vsur    Vbiasn  0       0       NMOS L=2  W=50
MSU2    Vsur    Vsur    VDD     VDD     PMOS L=20  W=10
MSU3    Vbiasp  Vsur    Vbiasn  0       NMOS L=1  W=10

.ends
```

Problem 22.7)

To estimate the slew rate limitations in charging and discharging a 1pF tied to the outputs of the circuits shown below:
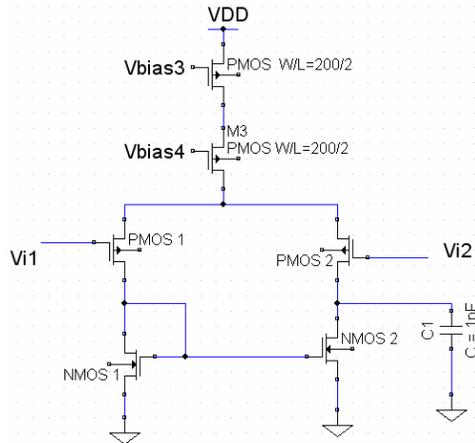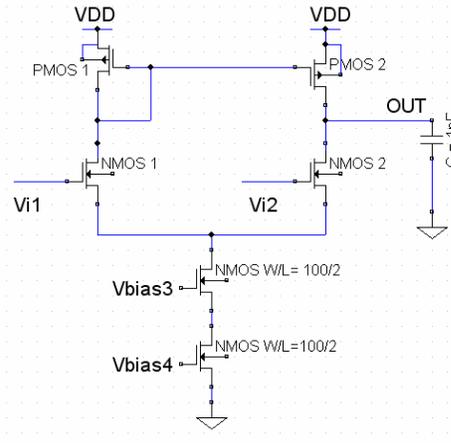
Fig 1.   Fig 2.

Circuit operation:
When the two gate voltages of PMOS1 and PMOS2 (in fig 1) and NMOS1 and NMOS2 (fig 2) are equal then the current through each branch would be 10µA each respectively. (Assuming in saturation). In fig 1 when the vi1 increases the V_{SG} of the PMOS 1 starts increasing thus shutting off the transistor. As a result the total current now flows through the PMOS 2 and charges the capacitor and increasing the output voltage. Thus the terminal vi1 is also called non-inverting input of the diff amp. Similarly vi2 is called inverting input of the diff amp since increasing the vi2 results in shutting off the PMOS 2 and now the total current flows through the PMOS 1. NMOS 2 mirrors the current in NMOS1 and thus the capacitor gets discharged.

When the two gate voltages of PMOS1 and PMOS2 (in fig 1) and NMOS1 and NMOS2 (fig 2) are equal then the current through each branch would be 10µA each respectivley. (Assuming in saturation).

Slew rate can be defined as the maximum rate of change of output voltage i.e maximum rate, which the output capacitor gets charged or discharged.

Similar to class A amplifiers diff amp also exhibits slew rate limitations because for proper operation all the MOSFETS should be conducting.

Now when PMOS 1 in fig 1. is OFF then the current available to charge the capacitor is 20µA. Similarly when PMOS 2 is OFF then the total current available to discharge the capacitor is 20µA. (i.e current through source)

$$\therefore \text{ slew rate } = \frac{dV}{dt} = \frac{I_{total}}{C_L} = \frac{20\mu A}{1pF} = 20\frac{mV}{ns}$$

Similarly in figure 2 when NMOS 1, NMOS 2 is OFF then the capacitor would discharge or charge accordingly and the corresponding slew rate is given by

$$\frac{dV}{dt} = \frac{I_{total}}{C_L} = \frac{20\mu A}{1pF} = 20\frac{mV}{ns}$$

Common mode operation range:
In order to find the common mode voltage range that can be applied to the diff amp given in the fig.

In fig 1. the maximum common mode voltage is given by
$V_{CMMAX} = V_{DD} - V_{SG} - 2V_{SDSAT} = 1 - 0.35 - 0.1 = 0.55V$

Similarly the minimum common mode voltage is given by
$V_{CMMIN} = V_{DSSAT} - V_{THP} = 0.05 - 0.28 = -0.23V$

Similarly for fig 2. following eq 22.12 from the text and table 9.2 we get

$V_{CMMAX} = VDD - V_{SG} + V_{THN} = 0.93V$ and

$V_{CMMIN} = 2VD_{SAT} + V_{GS} = 0.450V$

Simulation results for figure 1.
Charging of a capacitor:
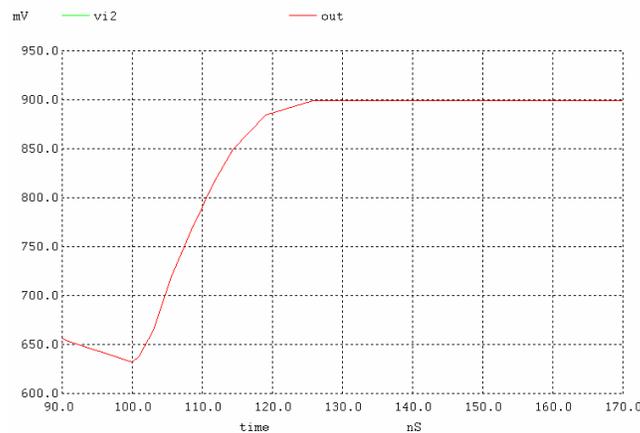
From figure above the slope is 17.82mV/ns

Discharging of a capacitor:
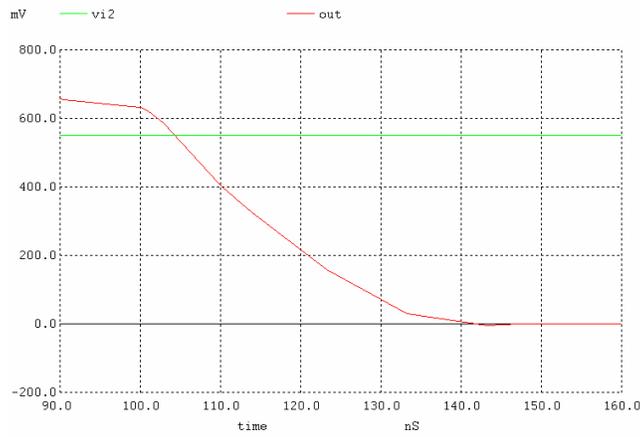
From the figure above the slope is 18.8 V/μs

Simulation results for figure 2.
 Charging of a capacitor:
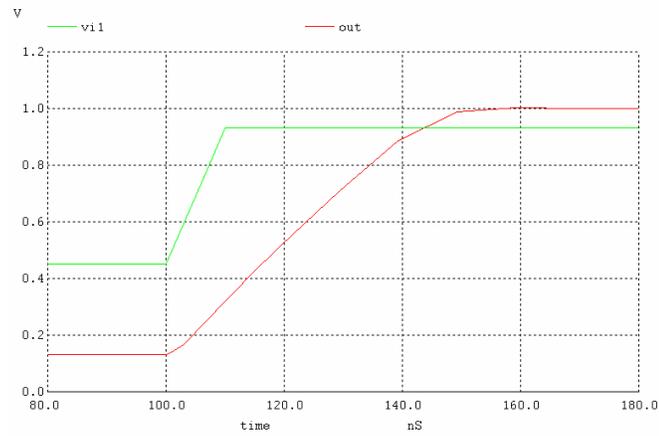
From figure above the slope is 19.40mV/ns
Discharging of a capacitor:
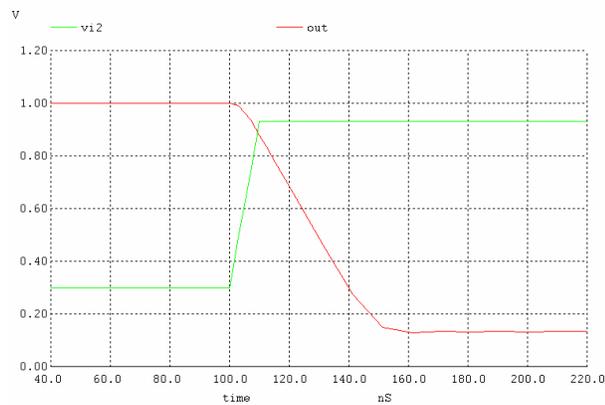
From the figure above the slope is 19.55 mV/ns

Note: Slew rate limitations can be eliminated by employing a source cross coupled pair differential amplifier. The circuit diagram and the operation is given in the text. (Fig 22.22 ,page 22-18).

22.8)
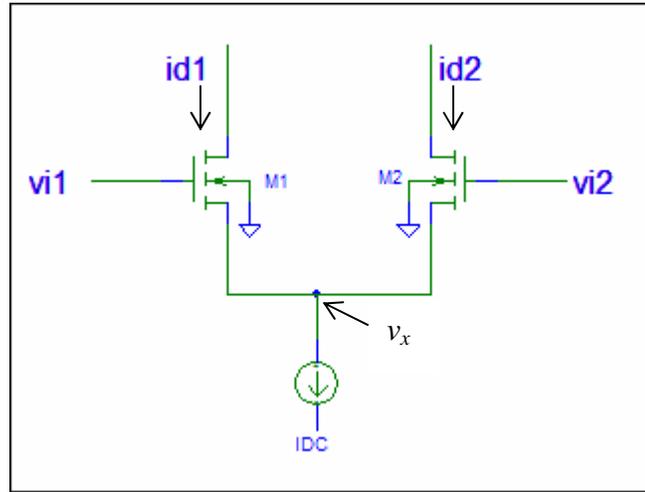
For the n-channel differential pair, without considering the body effect,

$$v_{gs1} = -v_{gs2}$$

$$v_{i1} - v_x = v_{i2} - v_x$$

$$v_x = \frac{v_{i1} + v_{i2}}{2}$$

From fig. 21.40 and the associated discussion, we observe that body effect reduces the gain of a SF.

$$v_{out} = v_{in} \cdot \frac{g_m}{g_m + g_{mb}}$$

So for the NMOS differential pair,

$$v_x = \frac{(v_{i1} + v_{i2})}{2} \cdot \frac{g_m}{g_m + g_{mb}}$$

The equation for the current would be [considering body effect]

$$i_{d1} = g_m \cdot v_{gs1} - g_{mb} \cdot v_{sb}$$

$$i_{d1} = g_m \cdot [v_{i1} - \frac{(v_{i1} + v_{i2})}{2} \cdot \frac{g_m}{g_m + g_{mb}}] - g_{mb} \cdot \frac{(v_{i1} + v_{i2})}{2} \cdot \frac{g_m}{g_m + g_{mb}}$$

$$i_{d1} = g_m \cdot [v_{i1} - \frac{(v_{i1} + v_{i2})}{2} \cdot \frac{g_m}{g_m + g_{mb}}] - \frac{(v_{i1} + v_{i2})}{2} \cdot \frac{g_m g_{mb}}{g_m + g_{mb}}$$

$$i_{d1} = \frac{g_m}{2} \cdot [v_{i1} \cdot (2 - \frac{g_m}{g_m + g_{mb}}) - v_{i2} \cdot \frac{g_m}{g_m + g_{mb}}] - \frac{(v_{i1} + v_{i2})}{2} \cdot \frac{g_m g_{mb}}{g_m + g_{mb}} \longrightarrow A$$

$$i_{d2} = g_m \cdot v_{gs2} - g_{mb} \cdot v_{sb}$$

$$i_{d2} = g_m \cdot [v_{i2} - \frac{(v_{i1} + v_{i2})}{2} \cdot \frac{g_m}{g_m + g_{mb}}] - g_{mb} \cdot \frac{(v_{i1} + v_{i2})}{2} \cdot \frac{g_m}{g_m + g_{mb}}$$

$$i_{d2} = g_m \cdot [v_{i2} - \frac{(v_{i1} + v_{i2})}{2} \cdot \frac{g_m}{g_m + g_{mb}}] - \frac{(v_{i1} + v_{i2})}{2} \cdot \frac{g_m g_{mb}}{g_m + g_{mb}}$$

$$i_{d2} = \frac{g_m}{2} \cdot [v_{i2} \cdot (2 - \frac{g_m}{g_m + g_{mb}}) - v_{i1} \cdot \frac{g_m}{g_m + g_{mb}}] - \frac{(v_{i1} + v_{i2})}{2} \cdot \frac{g_m g_{mb}}{g_m + g_{mb}} \longrightarrow B$$

So the given equations for the currents i_{d1} and i_{d2} are valid.

Problem 22.9

Determine: (a) the transconductance of the diff-amp, (b) the AC small-signal drain currents of all transistors in terms of the input voltages and g_{mn}, (c) and the small-signal voltage gain $(v_{o+} - v_{o-})/(v_{I+} - v_{I-})$

Solution:

For this problem reference the diff-amp in Fig 22.39. Let's label the four NMOS transistors (from left to right) as M1, M2, M3, and M4 respectively. The four PMOS transistors will be labeled as M5, M6, M7, and M8 from left to right as well. Finding the small signal voltage gain makes solving for the transconductance and the small signal drain currents very easy so we will derive the gain first.

The first step is to write a voltage loop around the inputs and across the gate-source of M1 and M4. The following equation results: $\mathbf{v_{I+} - v_{I-} = v_{gs1} - v_{gs4}}$. Next, find the source voltage of the NMOS transistors, v_x: $v_x = v_{I+} - v_{gs1}$ and $v_x = v_{I-} - v_{gs4}$. Since $v_{gs1} = -v_{gs4}$, these two equations combine to yield: $\mathbf{vx = (v_{I+} + v_{I-})/2}$. This result makes intuitive sense because the source of the NMOS transistors is simply a voltage divider between two equivalent arms in the diff-amp. We would expect that v_x be divided evenly because the diff-amp is a symmetrical circuit.

The next step is to solve for v_{gs1}. The gate voltage of M1 is v_{I+} and the source voltage is v_x. Thus: $\mathbf{v_{gs1} = v_{I+} - v_x = (v_{I+} - v_{I-})/2}$. Next is to solve for the output voltages, v_{o+} and v_{o-}. This configuration of diff-amp is somewhat unique in the sense that the pair of diode connected PMOS transistors (M6 and M7) act as a constant current source and inhibit any small signal current in the other PMOS transistors (M5 and M8). The effect of this is that M5 and M8 will not sink or source any additional current to the output like the convention diff-amp. In the conventional diff-amp when the non-inverting input terminal is raised a small-signal current is created in the PMOS current load that is mirrored to the load and then sourced to the output terminal. For the case of the fully differential diff-amp any small signal chance on M5 is not mirrored to M8 because the diode pair prevents them.

The positive output will see an output resistance of $r_{o8}\|r_{o4}$ or in general terms $r_{op}\|r_{on}$. On the positive output terminal v_{o+} the small signal current $g_{mn}v_{gs}$ is pulled from the output load. Therefore: $\mathbf{v_{o+} = g_{mn}v_{gs}(r_{op}\|r_{on})}$. Conversely, v_{o-} will source current from the diff-amp, and $\mathbf{v_{o-} = -g_{mn}v_{gs}(r_{op}\|r_{on})}$. Substituting $v_{gs} = (v_{I+} - v_{I-})/2$ into these two equations produce $\mathbf{v_{o+}/(v_{I+} - v_{I-}) = g_{mn}(r_{op}\|r_{on})/2}$ and $\mathbf{v_{o-}/(v_{I+} - v_{I-}) = -g_{mn}(r_{op}\|r_{on})/2}$. Subtracting these gives us the small signal voltage gain: $\mathbf{(v_{o+} - v_{o-})/(v_{I+} - v_{I-}) = g_{mn}(r_{op}\|r_{on})}$. Note that this gain is identical to that of the conventional diff-amp. This amplifier is a valid alternative when a differential output signal is desired.

The transconductance of the entire diff-amp is that of the amplifying device, which is just a single n-type MOSFET. Thus, the transconductance of this diff-amp is simply $\mathbf{g_{mn}}$. From previous diff-amp experience it should be obvious that $i_{d1} = i_{d2} = -i_{d3} = -i_{d4}$. Since $id = g_{mn}v_{gs}$ then $\mathbf{i_{d1} = i_{d2} = -i_{d3} = -i_{d4} = g_{mn}v_{gs} = g_{mn}(v_{I+} - v_{I-})/2}$.

Simulation:

To simulate this circuit it is necessary to apply a 1mV input AC voltage to each input terminal (+1mV to v_{I+} and –1mV to v_{I-}). The gain can be observed by comparing the input voltages to the output voltages. The following two graphs show these.
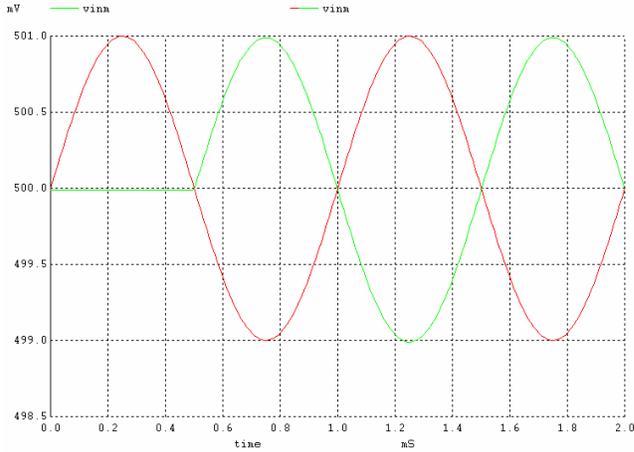
Figure 1. V_{I+} and V_{I-} $\Delta V=1mV$
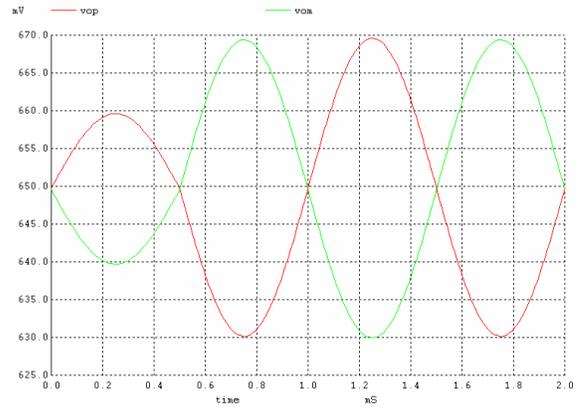
Figure 2. V_{o+} and V_{o-} $\Delta V=19.5mV$

The gain of the diff-amp can be determined by measuring the amplification on the output terminal with respect to the input terminal. Thus, in simulation the gain is approximately 19.5V/V.

When comparing the currents 0v voltage sources were inserted between the drains of the NMOS devices and the PMOS current source loads. From Figure 3 below the following information can be determined. $i_{d1} = -i_{d4}$ and $i_{d2} = -i_{d3}$.
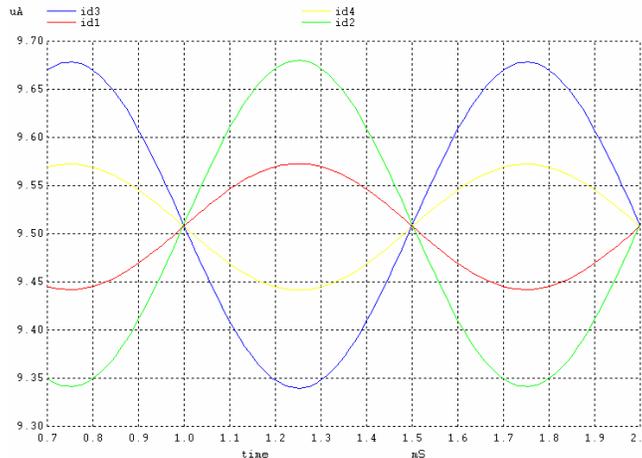
Figure 3. Winspice AC current summary

One disconcerting thing about this graph is that the magnitude of i_{d1} and i_{d4} is not equal to i_{d2} and i_{d3}. A possible reason for this is that the set of diode connected PMOS attenuate the signal swing on transistors M1 and M4 while allowing M2 and M4 to swing to the expected levels. The expected swing is about 150nA (150nA = $g_{mn}v_{gs}$ = (150uA/V)(1mV)). For M1 and M4 the swing is only about one third of 150nA.

Netlist:

```
.control
destroy all
run
let vindif=vinp-vinm
let voutdif=vop-vom
let gain=voutdif/vindif
let id1=i(vid1)
let id2=i(vid2)
let id3=i(vid3)
let id4=i(vid4)
plot id1 id2 id3 id4 xlimit .8m 2m
plot gain ylimit 16 20
plot vop vom
plot vinp vinm
.endc

.option scale=50n
.tran 10u 2m
```

VDD	VDD	0	DC	1		
Vinp	vinp	0	DC	0	AC	SIN 0.5 1m 1k
Vinm	vinm	0	DC	0	AC	SIN 0.49999 1m 1k 500u
vid1	vom	vd1	DC	0		
vid2	center	vd2	DC	0		
vid3	center	vd3	DC	0		
vid4	vop	vd4	DC	0		
Vbias3	Vbias3	0	DC	.544		
Vbias4	Vbias4	0	DC	.362		

M1	vd1	vinp	vx	0	NMOS L=2 W=50
M2	vd2	vinp	vx	0	NMOS L=2 W=50
M3	vd3	vinm	vx	0	NMOS L=2 W=50
M4	vd4	vinm	vx	0	NMOS L=2 W=50
M9	vx	Vbias3	vy	0	NMOS L=2 W=200
M10	vy	Vbias4	0	0	NMOS L=2 W=200

M5	vom	center	VDD	VDD	PMOS L=2 W=100
M6	center	center	VDD	VDD	PMOS L=2 W=100
M7	center	center	VDD	VDD	PMOS L=2 W=100
M8	vop	center	VDD	VDD	PMOS L=2 W=100

* BSIM4 models

Problem 22.11
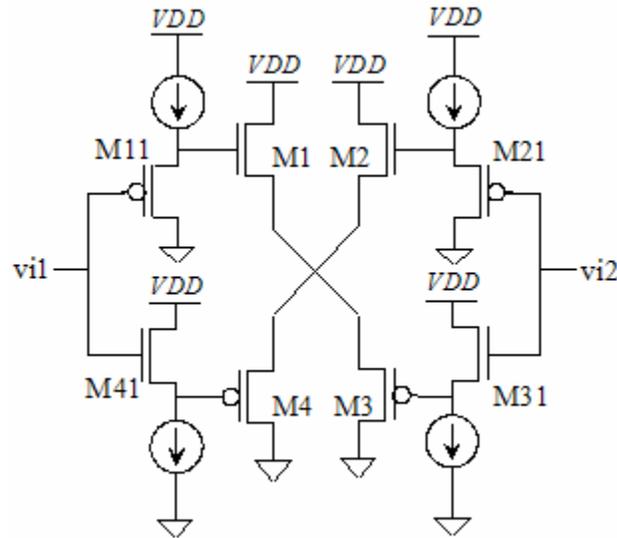
Net list

*** Figure 22.26 CMOS: Circuit Design, Layout, and Simulation ***
.control
destroy all
run
print all
.endc

.option scale=1u
.op

VDD	VDD	0	DC	5			
Vi1	vi1	0	DC	3.5			
Vi2	vi2	0	DC	3.5			
vm13	vmeas1		vmeas3	dc	0		
vm24	vmeas2		vmeas4	dc	0		
iss1	vdd	vs11	DC	20u			
iss2	vdd	vs21	DC	20u			
iss3	vs31	0	DC	20u			
iss4	vs41	0	DC	20u			
M1	vdd	vs11	vmeas1	vmeas1	NMOS	L=2	W=10
M2	vdd	vs21	vmeas2	vmeas2	NMOS	L=2	W=10
M3	0	vs31	vmeas3	vmeas3	PMOS	L=2	W=30
M4	0	vs41	vmeas4	vmeas4	PMOS	L=2	W=30

```
M11   0      vi1    vs11   vs11   PMOS L=2 W=30
M41   VDD    vi1    vs41   vs41   NMOS L=2 W=10

M31   VDD    vi2    vs31   vs31   NMOS L=2 W=10
M21   0      vi2    vs21   vs21   PMOS L=2 W=30
```

vm13 and vm24 are the zero voltage sources to measure the current in M1-M4

DC Operating Point ... 100%
vm13#branch = 1.973939e-05
vm24#branch = 1.973939e-05

From the operating point analysis it can be seen that the currents in M1-M4 is 19.73µA without body effect(i.e, source of the MOSFETS tied to the body) which is almost the same as the biasing currents (20µA) in the source followers.

With body effect(i.e body of NMOS tied to ground & body of PMOS tied to VDD) the currents are

vm13#branch = 5.706939e-07
vm24#branch = 5.706939e-07

The currents in M1-M4 are 0.57µA. Hence a large mismatch in the currents can be seen due to body effect.

Problem 22.12

Using the parameters from table 9.1 and equation 22.48, the gain is approximated as
$A_d = g_{m1}\left(g_{m2} \cdot r_{o2}^2 \parallel g_{m4} \cdot r_{o4}^2\right) = 219kV/V$ for low frequencies. The simulated gain of the circuit is
actually about 77.5 kV/V when the frequency is less than 10 kHz as seen in Figure 22.1 below.
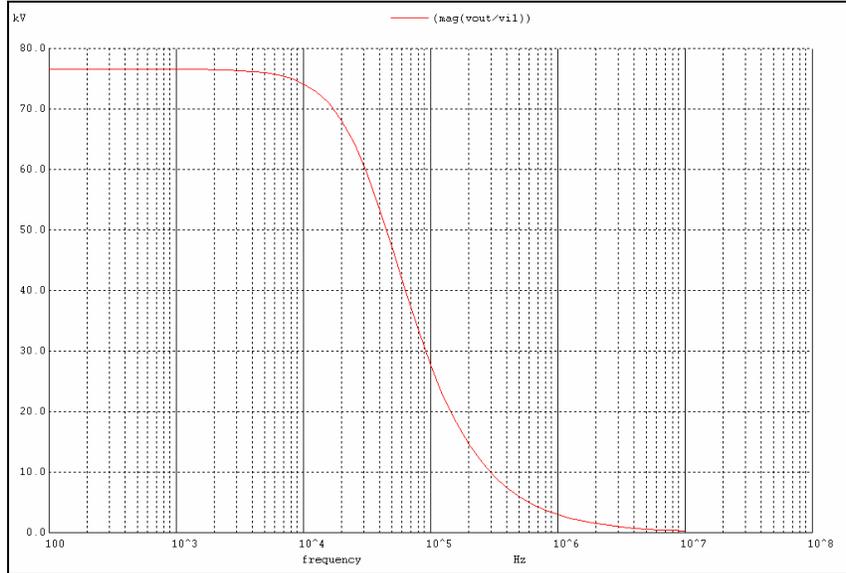
Figure 22.1: Plot of vout/vin showing gain versus frequency

As seen in example 22.9 (page 22-25), the minimum input voltage (VCMMIN) is about 1.55V and the
maximum input voltage (VCMMAX) is about 4.45V. By choosing a DC bias input voltage of 2.5V, we
guaranteed that the circuit would work. A plot of the input voltages is shown in Figure 22.2.
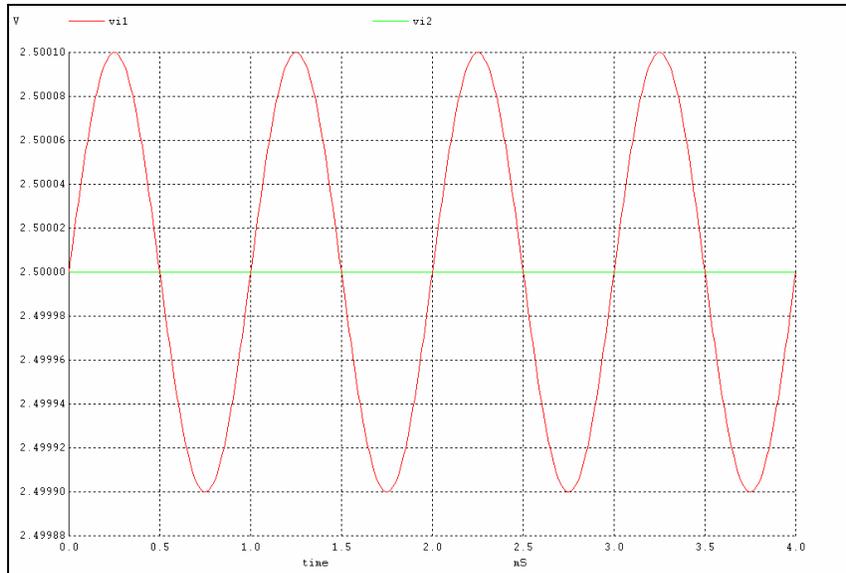
Figure 22.2: Plot of vi1 and vi2 vs. time

The maximum output voltage is calculated by the following:

$$V_{out\ max} = VDD - 2V_{DS,sat} \cong 4.5V$$

The minimum output voltage is calculated by the following:

$$V_{out\min} = V_{I2} - V_{GS2} + 2V_{DS,sat} \cong 1.9V$$

For our problem parameters Vin=100uV @ 1KHz and Vcm=2.5 V we would expect to see output voltage

magnitude of $Vout = A_d \cdot v_{in} = 77.5\dfrac{kV}{V} \cdot 100uV \cong 7.75V$.

From our simulation plots (Figure 22.3) we can see that our output voltage is between 1.7V and 4.5V because we are limited by $V_{out\ max}$ and $V_{out\ min}$. Output voltage is still sinusoidal (only cut off at $V_{out\ max}$ and $V_{out\ min}$) and at 1KHz frequency.
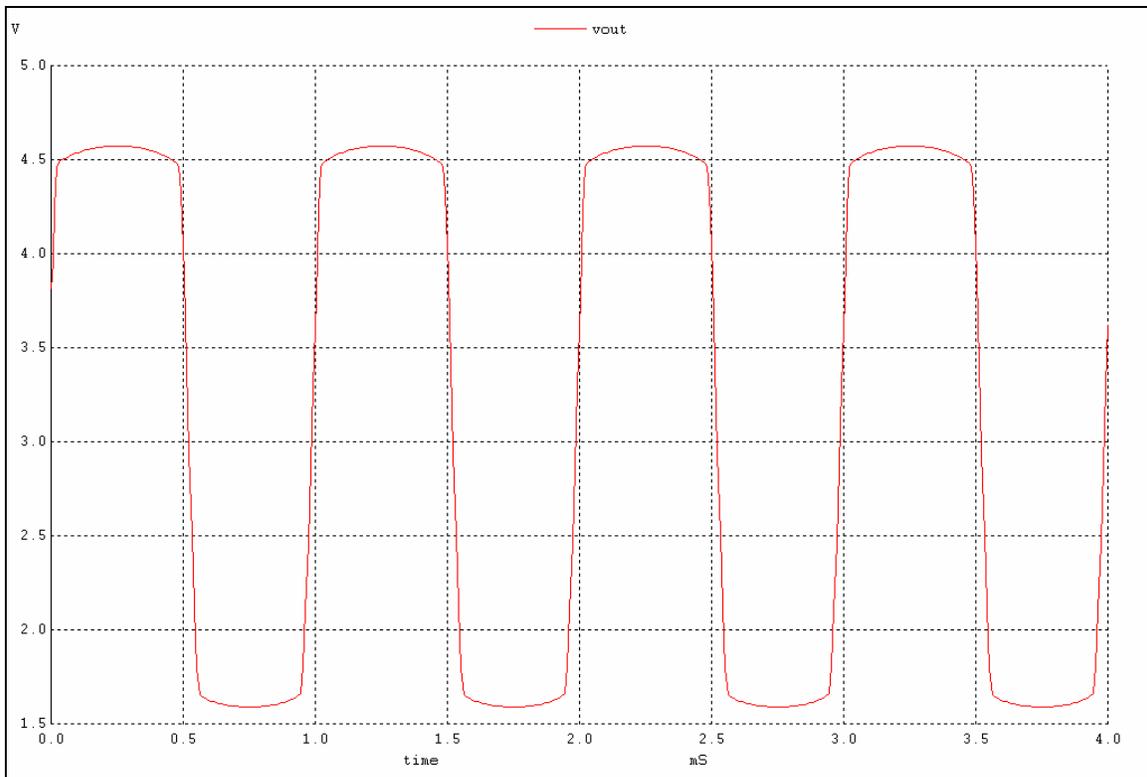

Figure 22.3: Plot of vout showing maximum and minimum output voltage

```
*** Problem 22.12 (Figure 22.31) CMOS: Circuit Design, Layout, and Simulation ***

.control
destroy all
run
plot vout/vi1
*plot vi1 vi2
*plot vout
*print vtest#branch dm1 dmb3 vout
.endc

.option scale=1u
.ac DEC 10 100 10MEG
*.tran 10u 4m

VDD       VDD       0         DC        5
vi1       vi1       0         DC        2.5       AC        100u sin 2.5 100u 1k
vi2       vi2       0         DC        2.5
vtest     vtest     0         DC        0

M1        dm1       vi1       dmb3      0         NMOS L=2 W=10
M2        dm2       vi2       dmb3      0         NMOS L=2 W=10
M3        dm3       gm3       vdd       vdd       PMOS L=2 W=30
M4        dm4       gm3       vdd       vdd       PMOS L=2 W=30
M6        gmc1      gmc1      dmb3      0         NMOS L=8 W=10

MC1       gm3       gmc1      dm1       0         NMOS L=2 W=10
MC2       vout      gmc1      dm2       0         NMOS L=2 W=10
MC3       gm3       vbias2    dm3       vdd       PMOS L=2 W=30
MC4       vout      vbias2    dm4       vdd       PMOS L=2 W=30

MB1       dmb1      vbias1    vdd       vdd       PMOS L=2 W=30
MB2       gmc1      vbias2    dmb1      vdd       PMOS L=2 W=30
MB3       dmb3      vbias3    dmb4      0         NMOS L=2 W=30
MB4       dmb4      vbias4    vtest     0         NMOS L=2 W=30

Xbias     VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas
MN1       Vbias2    Vbiasn    0         0         NMOS L=2 W=10
MN2       Vbias1    Vbiasn    0         0         NMOS L=2 W=10
MN3       Vncas     Vncas     vn1       0         NMOS L=2 W=10
MN4       vn1       Vbias3    vn2       0         NMOS L=2 W=10
MN5       vn2       vn1       0         0         NMOS L=2 W=10
MN6       Vbias3    Vbias3    0         0         NMOS L=10 W=10
MN7       Vbias4    Vbias3    Vlow      0         NMOS L=2 W=10
MN8       Vlow      Vbias4    0         0         NMOS L=2 W=10
MN9       Vpcas     Vbias3    vn3       0         NMOS L=2 W=10
MN10      vn3       Vbias4    0         0         NMOS L=2 W=10

MP1       Vbias2    Vbias2    VDD       VDD       PMOS L=10 W=30
MP2       Vhigh     Vbias1    VDD       VDD       PMOS L=2 W=30
MP3       Vbias1    Vbias2    Vhigh     VDD       PMOS L=2 W=30
MP4       vp1       Vbias1    VDD       VDD       PMOS L=2 W=30
MP5       Vncas     Vbias2    vp1       VDD       PMOS L=2 W=30
MP6       vp2       Vbias1    VDD       VDD       PMOS L=2 W=30
MP7       Vbias3    Vbias2    vp2       VDD       PMOS L=2 W=30
MP8       vp3       Vbias1    VDD       VDD       PMOS L=2 W=30
MP9       Vbias4    Vbias2    vp3       VDD       PMOS L=2 W=30
MP10      vp4       vp5       VDD       VDD       PMOS L=2 W=30
MP11      vp5       Vbias2    vp4       VDD       PMOS L=2 W=30
MP12      Vpcas     Vpcas     vp5       VDD       PMOS L=2 W=30

MBM1      Vbiasn    Vbiasn    0         0         NMOS L=2 W=10
MBM2      Vbiasp    Vbiasn    Vr        0         NMOS L=2 W=40
MBM3      Vbiasn    Vbiasp    VDD       VDD       PMOS L=2 W=30
MBM4      Vbiasp    Vbiasp    VDD       VDD       PMOS L=2 W=30

Rbias     Vr        0         6.5k

MSU1      Vsur      Vbiasn    0         0         NMOS L=2  W=10
MSU2      Vsur      Vsur      VDD       VDD       PMOS L=100 W=10
MSU3      Vbiasp    Vsur      Vbiasn    0         NMOS L=1  W=10
.ends
```

Problem 22.13

This problem shows the operation of the current differential amplifier in figure 22.33 of the text using SPICE with current sources for inputs. The values from table 9.2 will be used.

We'll start by building the netlist.

We will use 3 separate current sources, and call them Iss1 - 3.

If we want to display the current through each transistor, 0V voltage sources can be added as well. These are labeled Vmeas1 - 4 in the netlist.

We shall sweep a current in I1 in the circuit in figure 22.33 from -10μ to 10μA, and hold I2 constant at 0A.

The output current can be measured by adding a 350mV source to the drain of M4, then plotting the current through that source. 350mV is used to hold the drain at ~V_{GS}.

Netlist

```
.control
destroy all
run
let IM1=vmeas1#branch
let IM2=vmeas2#branch
let IM3=vmeas3#branch
let IM4=vmeas4#branch
let Iout=vout#branch
plot Iout IM1 IM2 IM3 IM4
.endc

.option scale=50n
.DC i1 -10u 10u 10n

I1      0      Iss1    DC      0
I2      0      Iss2    DC      0

Vout    Iss3   0       DC      350m

VDD     VDD    0       DC      1
Iss1    VDD    Iss1    DC      10u     AC      0
Iss2    VDD    Iss2    DC      20u     AC      0
Iss3    VDD    Iss3    DC      10u     AC      0

M1      Iss1   Iss1    Imeas1  0       NMOS L=2 W=50
M2      Iss2   Iss1    Imeas2  0       NMOS L=2 W=50
M3      Iss2   Iss2    Imeas3  0       NMOS L=2 W=50
M4      Iss3   Iss2    Imeas4  0       NMOS L=2 W=50

Vmeas1 Imeas1  0       DC      0
Vmeas2 Imeas2  0       DC      0
Vmeas3 Imeas3  0       DC      0
Vmeas4 Imeas4  0       DC      0
```

We notice in the simulation shown in figure 1 that when we input zero current in I1, $I_d =$ 10μA for all MOSFETs as expected. When we pull 10μA out of node I1, M1 is off. All the current supplied by Iss1 is pulled out to I1. M2 is off so M3 must sink all of Iss2 (20μA here). The 20μA in M3 is mirrored over to M4, and the output is ~I1 = 10μA. The results are similar but opposite when we input current into I1.
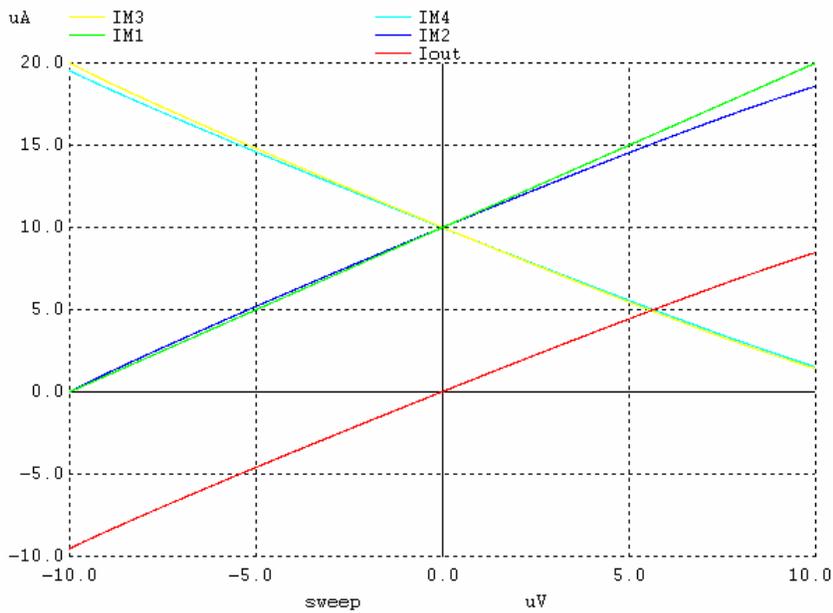
Figure 1. SPICE simulation of figure 22.33 from the text.

If we want to give the diff amp gain or scale the input currents we can change the size of M1-4. In the following example we'll double the width of M1 and M4. This simulation is shown in figure 2. We see that with the width of M1 and 4 increased we can scale the input current down. When I1= -10μ to 10μA, the output is scaled down by roughly 20μA, so we get -30μ to -10μA.
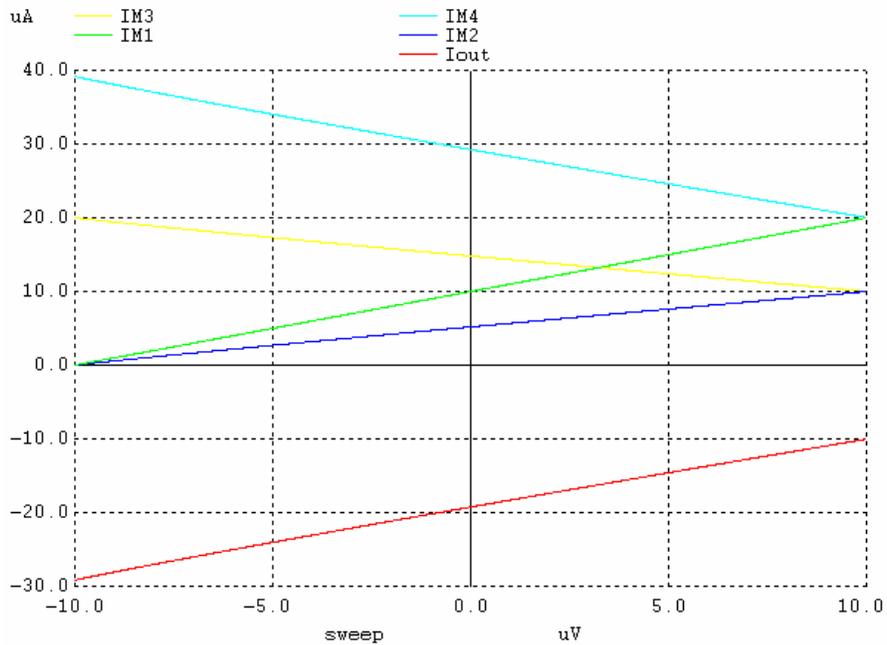

Figure 2. SPICE simulation of figure 22.33 from the text with M4s width doubled.

P22_14.
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Below in, figure 1 is the schematic of the circuit that is discussed and simulated in this problem.
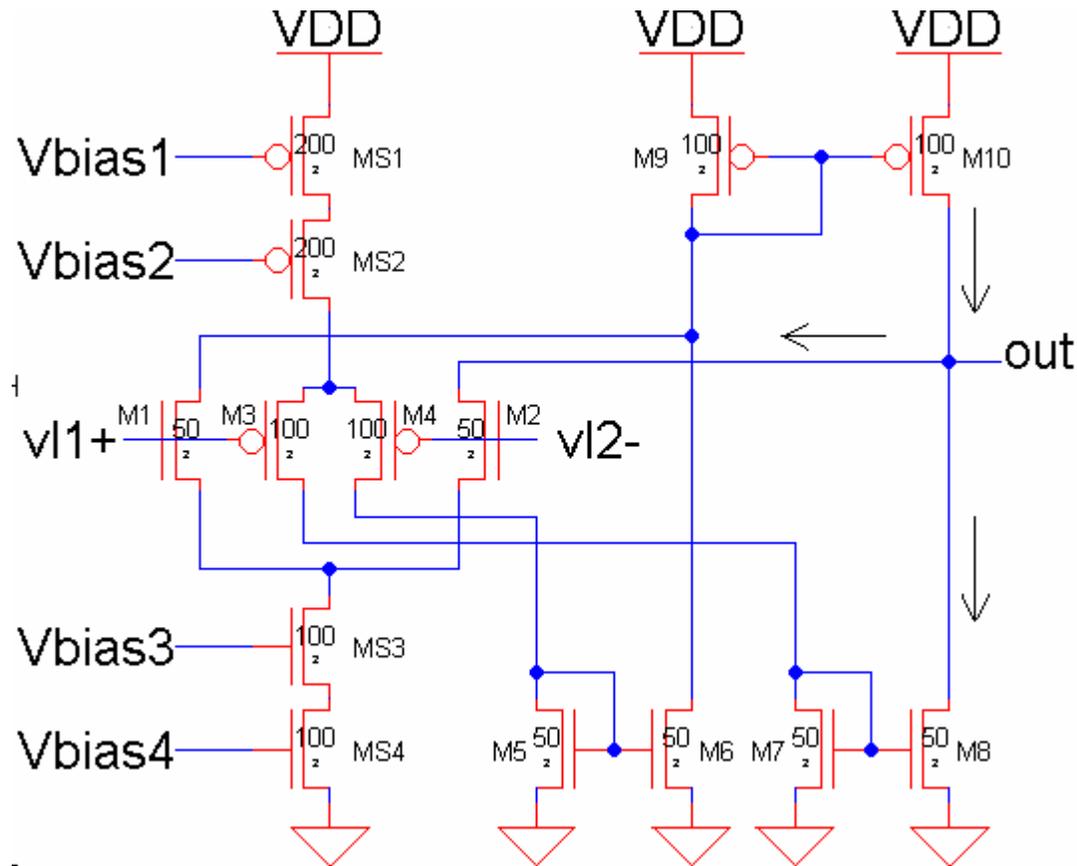
Figure 1

To begin to explain how this circuit works, we will start by considering what happens when the common mode input signal is such that both the PMOS and NMOS diff-amps are both on, (and the gate voltages of diff-amps are equal.) If this is true, both the PMOS and the NMOS diff-amps are conducting a current.   If the PMOS is set up to source a current, we'll call Ip, and the NMOS source is set up to sink a current, we'll call In, then M1 and M2 are pulling $\dfrac{In}{2}$ from the drains of M9 and M10. At the same time, M3 and M4 are each sourcing $\dfrac{Ip}{2}$. M4's current is being pushed down the drain of M5, which is mirrored over onto M6. M3's current is being pushed through M7, which is then mirrored in M8. This puts the drain current of M8 at $\dfrac{Ip}{2}$. Since M8's drain is connected to the drain of M10, M8's current is also being pulled through M10. This puts the current

sourced by M10 at $\frac{In}{2} + \frac{Ip}{2}$. If Ip=In=I, then M10's current is the sum of the current through M2 and M8. In the figures below we have set Ip=In=20µ. In the following figure the current on the drain of M10 is clearly the sum of the currents through M2 and M8.
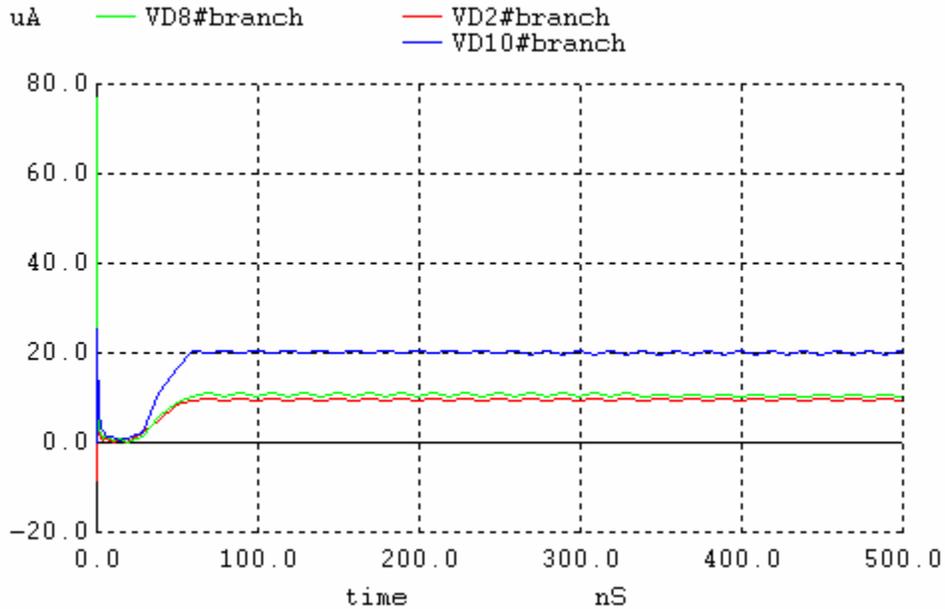

Figure 2

Now lets turn on only the NMOS diff-amp by setting $V_{I1} = V_{I2} = 1V$ and look at the currents flowing through the same branches. We notice that all the current from M10 is flowing through M2 and none through M8. This is because The PMOS diff-amp is off and therefore not forcing current down M5, M6, M7 and M8. This means that since M8 is not sinking a current, M10 only sources $\frac{I}{2}$, (since In=Ip.) This can be seen in Figure 3.
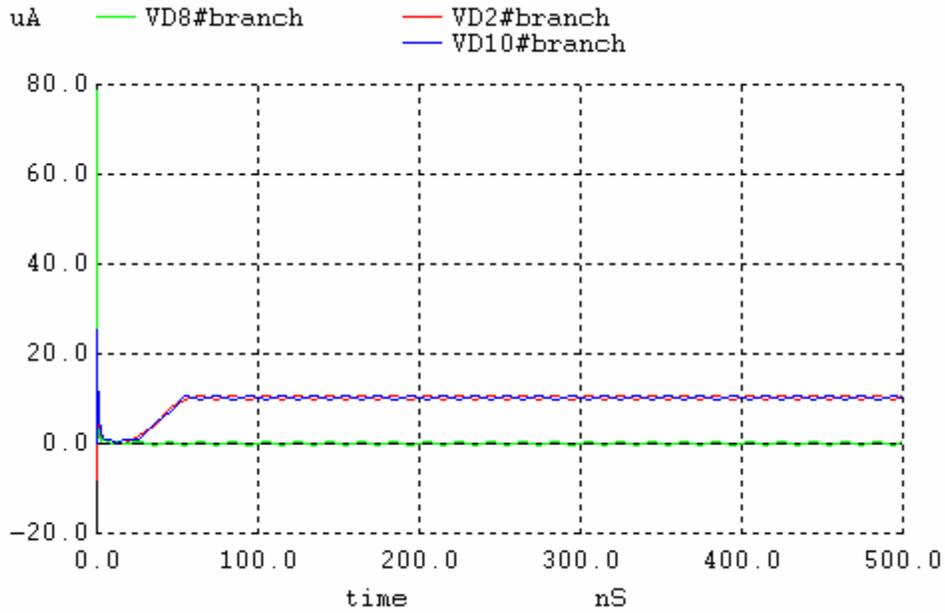
Figure 3

Now lets turn on only the PMOS diff-amp by seting $V_{I1} = V_{I2} = 0V$ and look at the same currents. We see that all the current from M10 in now flowing through M8. This is because the NMOS diff-amp is off and M2 is not sinking and current. This means that again, M10 only needs to source $\dfrac{I}{2}$. This is seen in figure 4.
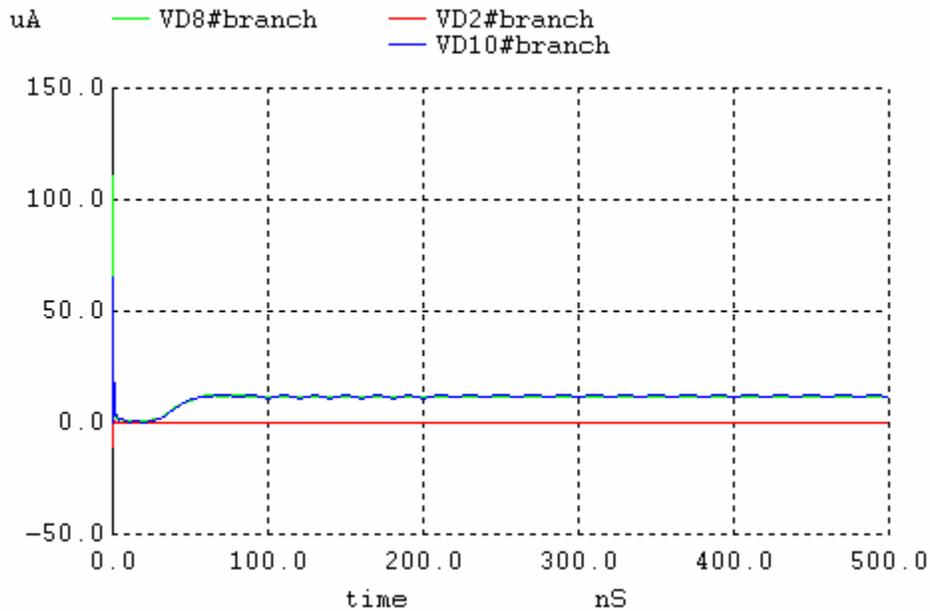

Figure 4

Similar behavior is happening at the other summing junction of M9, M6, and M1.

To verify that the common-mode voltage range goes beyond the power rails, we can connect V_{I1} and V_{I2} and sweep the now common input voltage of the differential amplifiers. Lets sweep it from below zero and above VDD (–0.2 to 1.2). When the common input is below 0.5 we will look at the PMOS diff-amp to verify that the V_{SD} of the PMOS transistors are above V_{SDsat}. When above 0.5 we will look to verify that the V_{DS} of the NMOS diff-amp transistors are above V_{DSsat}. This is seen in Figure 5.
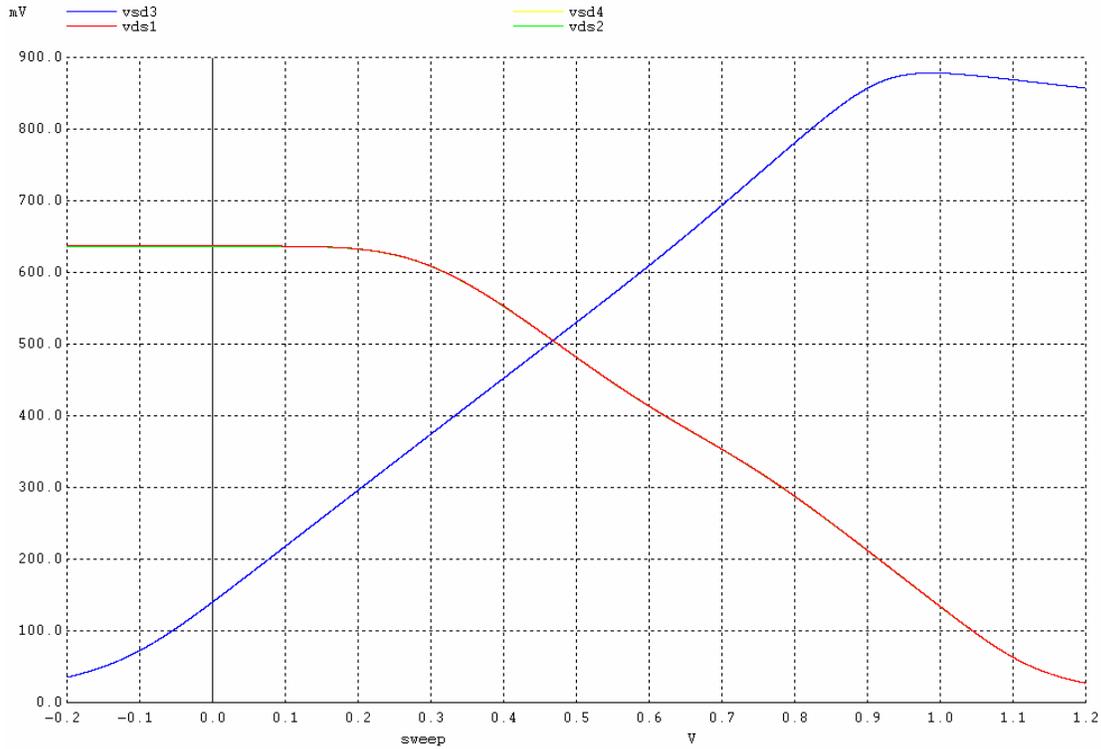

Figure 5

We see from figure 5 that V_{SD} of the PMOS diff-amp, (transistors M3 and M4,) do not go below V_{Sdsat} (50mV) until the common input voltage goes below –0.15V. V_{DS} of the NMOS diff-amp, (transistors M1 and M2,) do not go below V_{Dssat} (50mV) until the common input voltage goes above 1.125 V.

Figure 6, below, was produced by tying the inverting input to the output of the diff-amp,
This was done to prove that the common mode output range reaches the power supply
rails, (but does not exceed them, as the common mode input range does.)
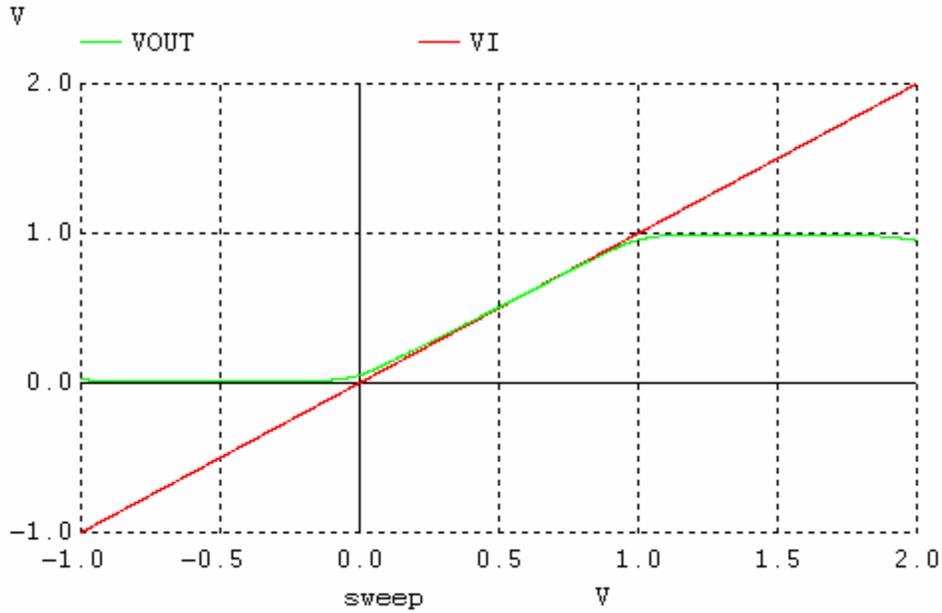
Figure 6

*** Problem 22.14 CMOS: Circuit Design, Layout, and Simulation ***

```
.control
destroy all
run
LET
PLOT VD10#BRANCH VD8#BRANCH VD2#BRANCH
*LET VOUT=OUT
*PLOT VI VOUT
.endc

.option scale=50n ITL1=300
.tran 10n 500n UIC
*.DC VI -1 2 .001

VDD      VDD      0          DC        1
VI       VI       0          DC        .5

VD2  OUT    D2    DC   0
VD8  OUT    D8    DC   0
VD10  D10    OUT    DC    0


MS1 A   VBIAS1 VDD  VDD PMOS L=2 W=200
MS2 PS    VBIAS2 A    VDD PMOS L=2 W=200
MS3 PN  VBIAS3 B    0  NMOS L=2 W=100
MS4 B     VBIAS4 0   0  NMOS L=2 W=100

M1  D1  VI    PN  0  NMOS L=2 W=50
M2  OUT  VI    PN  0  NMOS L=2 W=50
M3  D3  VI    PS  VDD  PMOS L=2 W=100
M4  D4  VI    PS  VDD  PMOS L=2 W=100
```

```
M5  D4  D4   0   0  NMOS L=2 W=50
M6  D1  D4   0   0  NMOS L=2 W=50
M7  D3  D3   0   0  NMOS L=2 W=50
M8  D8  D3   0   0  NMOS L=2 W=50
M9  D1  D1    VDD  VDD PMOS L=2 W=100
M10 D10  D1     VDD  VDD PMOS L=2 W=100


Xbias      VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias


.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1     Vbias3    Vbiasp    VDD     VDD     PMOS L=2 W=100
MP2     Vbias4    Vbiasp    VDD     VDD     PMOS L=2 W=100
MP3     vp1       vp2       VDD     VDD     PMOS L=2 W=100
MP4     vp2       Vbias2    vp1     VDD     PMOS L=2 W=100
MP5     Vpcas     Vpcas     vp2     VDD     PMOS L=2 W=100
MP6     Vbias2    Vbias2    VDD     VDD     PMOS L=10 W=20
MP7     Vhigh     Vbias1    VDD     VDD     PMOS L=2 W=100
MP8     Vbias1    Vbias2    Vhigh   VDD     PMOS L=2 W=100
MP9     vp3       Vbias1    VDD     VDD     PMOS L=2 W=100
MP10    Vncas     Vbias2    vp3     VDD     PMOS L=2 W=100

MN1     Vbias3    Vbias3    0       0       NMOS L=10 W=10
MN2     Vbias4    Vbias3    Vlow    0       NMOS L=2 W=50
MN3     Vlow      Vbias4    0       0       NMOS L=2 W=50
MN4     Vpcas     Vbias3    vn1     0       NMOS L=2 W=50
MN5     vn1       Vbias4    0       0       NMOS L=2 W=50
MN6     Vbias2    Vbias3    vn2     0       NMOS L=2 W=50
MN7     vn2       Vbias4    0       0       NMOS L=2 W=50
MN8     Vbias1    Vbias3    vn3     0       NMOS L=2 W=50
MN9     vn3       Vbias4    0       0       NMOS L=2 W=50
MN10    Vncas     Vncas     vn4     0       NMOS L=2 W=50
MN11    vn4       Vbias3    vn5     0       NMOS L=2 W=50
MN12    vn5       vn4       0       0       NMOS L=2 W=50

MBM1    Vbiasn    Vbiasn    0       0       NMOS L=2 W=50
MBM2    Vreg      Vreg      Vr      0       NMOS L=2 W=200
MBM3    Vbiasn    Vbiasp    VDD     VDD     PMOS L=2 W=100
MBM4    Vreg      Vbiasp    VDD     VDD     PMOS L=2 W=100

Rbias    Vr       0        5.5k

*amplifier
MA1     Vamp      Vreg      0       0       NMOS L=2 W=50
MA2     Vbiasp    Vbiasn    0       0       NMOS L=2 W=50
MA3     Vamp      Vamp      VDD     VDD     PMOS L=2 W=100
MA4     Vbiasp    Vamp      VDD     VDD     PMOS L=2 W=100

MCP     VDD       Vbiasp    VDD     VDD     PMOS L=100 W=100

*start-up stuff
MSU1    Vsur      Vbiasn    0       0       NMOS L=2  W=50
MSU2    Vsur      Vsur      VDD     VDD     PMOS L=20  W=10
MSU3    Vbiasp    Vsur      Vbiasn  0       NMOS L=1  W=10

.ends


* BSIM4 models
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Problem 22.15

Small signal equivalent for the circuit in fig. 22.41:
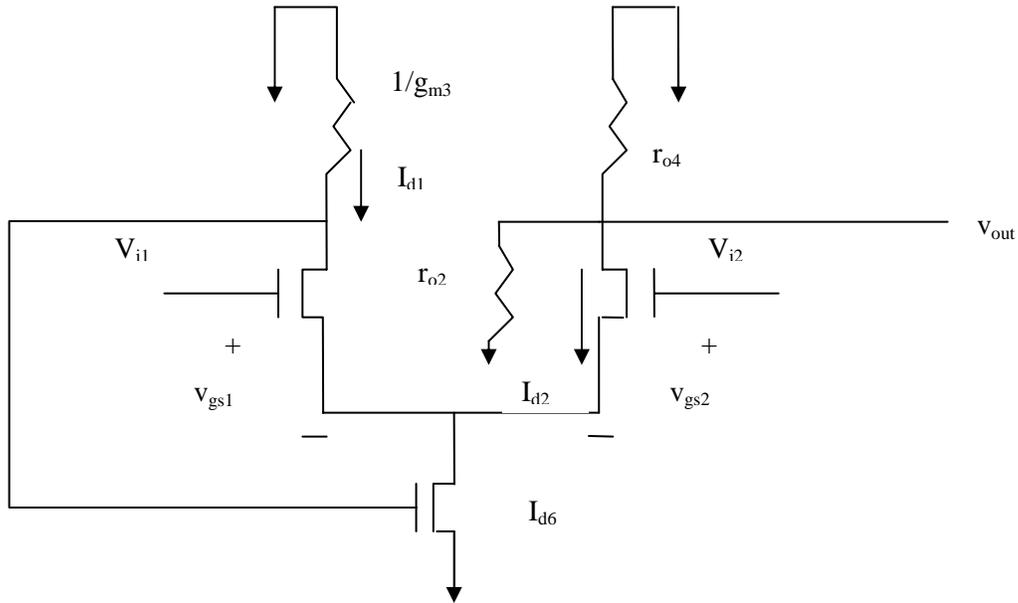
From the figure, the resistance looking into the output node is $r_{o2} \, // \, r_{o4}$ and the current flowing is $i_{d1} - i_{d2}$, since the current flowing in M1 is i_{d1}, M2 is i_{d2} and M6 is i_{d6}.

and $i_{d6} = i_{d1} + i_{d2}$

$\therefore v_{out} = (i_{d1} - i_{d2}) * (r_{o2} \, // \, r_{o4})$ ---- (1)

At M1 and M2 we have,

$v_{i1} - v_{gs1} + v_{gs2} - v_{i2} = 0$

$\Rightarrow v_{i1} - v_{i2} = v_{gs1} - v_{gs2}$

$v_{gs1} = \dfrac{i_{d1}}{g_{m1}}$

$v_{gs2} = \dfrac{i_{d2}}{g_{m2}}$

assuming $g_{m1} = g_{m2} = g_{mn}$

$$v_{gs1} - v_{gs2} = \frac{\left(i_{d1} - i_{d2}\right)}{g_{mn}}$$

$$\therefore v_{i1} - v_{i2} = \frac{\left(i_{d1} - i_{d2}\right)}{g_{mn}} \qquad\qquad\qquad -----(2)$$

Small-signal gain $A_d = \dfrac{v_{out}}{v_{i1} - v_{i2}}$

Using (1) and (2), we have

$$A_d = \frac{v_{out}}{v_{i1} - v_{i2}} = \frac{\left(i_{d1} - i_{d2}\right) * \left(r_{o4} // r_{o2}\right)}{\dfrac{\left(i_{d1} - i_{d2}\right)}{g_{mn}}}$$

$$\therefore A_d = g_{mn} * \left(r_{o4} // r_{o2}\right)$$