25.1) Using **SPICE** simulations, show the effects of clock feedthrough on the voltage across the load capacitor for the switch circuits shown in Fig 25.40. How does this voltage change if the capacitor value is increased to 100fF?

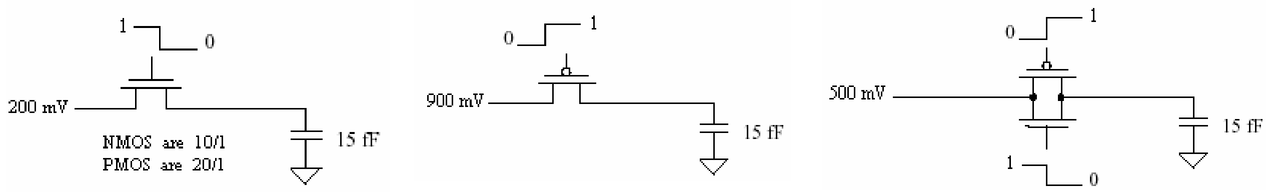
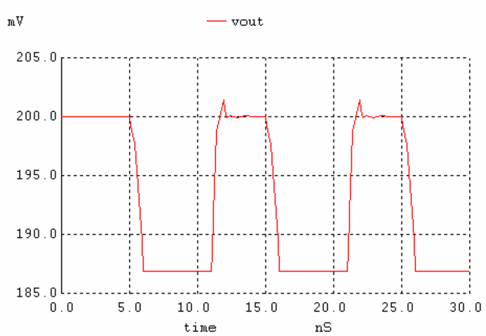


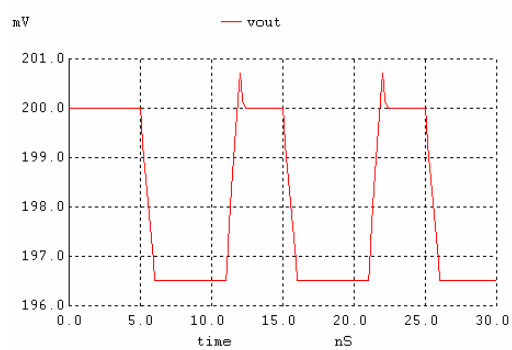
Fig 25.40

The simulations to follow show the clock feedthrough on each of the switch circuits shown (above) with the two different cap sizes.

<u>Sim showing clock feedthrough across cap for C = 15fF & 100fF with 200 mV applied:</u>



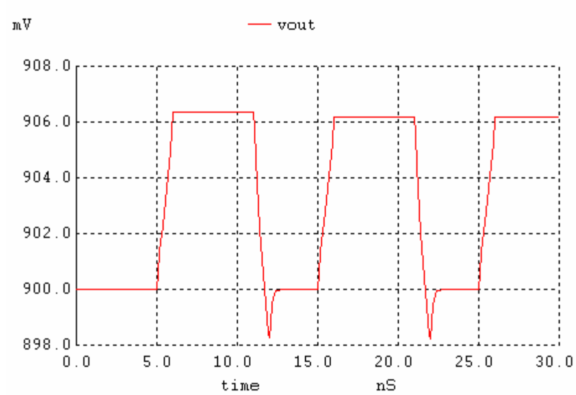
C = 15fF



C = 100fF

<u>Sim showing clock feedthrough across cap for C = 15fF & 100fF with 900 mV applied:</u>

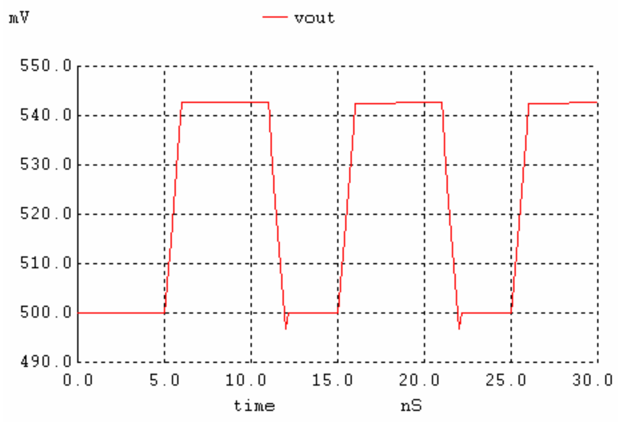
C = 15fF

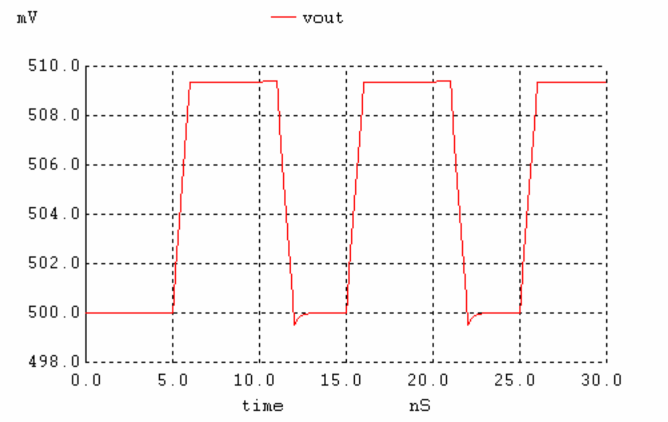


C = 100fF

25.1) cont'd

<u>Sim showing clock feedthrough across cap for C = 15fF & 100fF with 500 mV applied:</u>





C = 15fF

C = 100fF

If the capacitor is increased to 100fF the voltage change across the capacitor is decreased and voltage comes closer to the applied voltage. The result is due to the voltage change experienced between the switch's overlap capacitance and 100fF is less significant than for the15fF cap.

<u>Netlist</u>

```
.control
destroy all
run
plot vout
.endc

.tran 1n 30n
.options scale=50n

vinp    vinp    0       DC      .2

Vphi1   phi1    0       DC      0       PULSE 1   0 5n 0 0 5n 10n
Vphi2   phi2    0       DC      0       PULSE 0   1 5n 0 0 5n 10n

 *M1    vinp    phi1    vout    0       NMOS L=1 W=10
 M2     vinp    phi2    vout    VDD     PMOS L=1 W=20

C1      vout    0       15fF
*C2     vout    0       100f
*50nm BSIM4 models
```

Prob 25.2: Repeat (1) if dummy switches are used. Show schematics of how the dummy switches are added to the schematics.

[Ans]: Simulations w/ half-sized dummy switch attached to output (drain) of the transistor are shown below.

Fig 25.2-1 Clock Feedthrough Dummy switches schematics

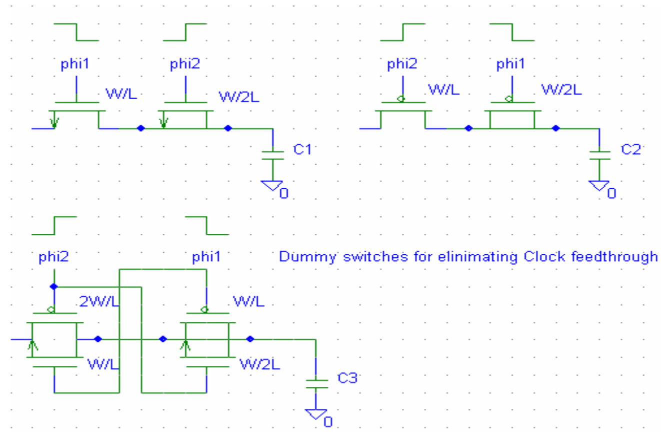


Fig 25.2-2 Clock Feedthrough performance simulation on NMOS, PMOS, and TG
With Dummy switches (left) w/o (right)

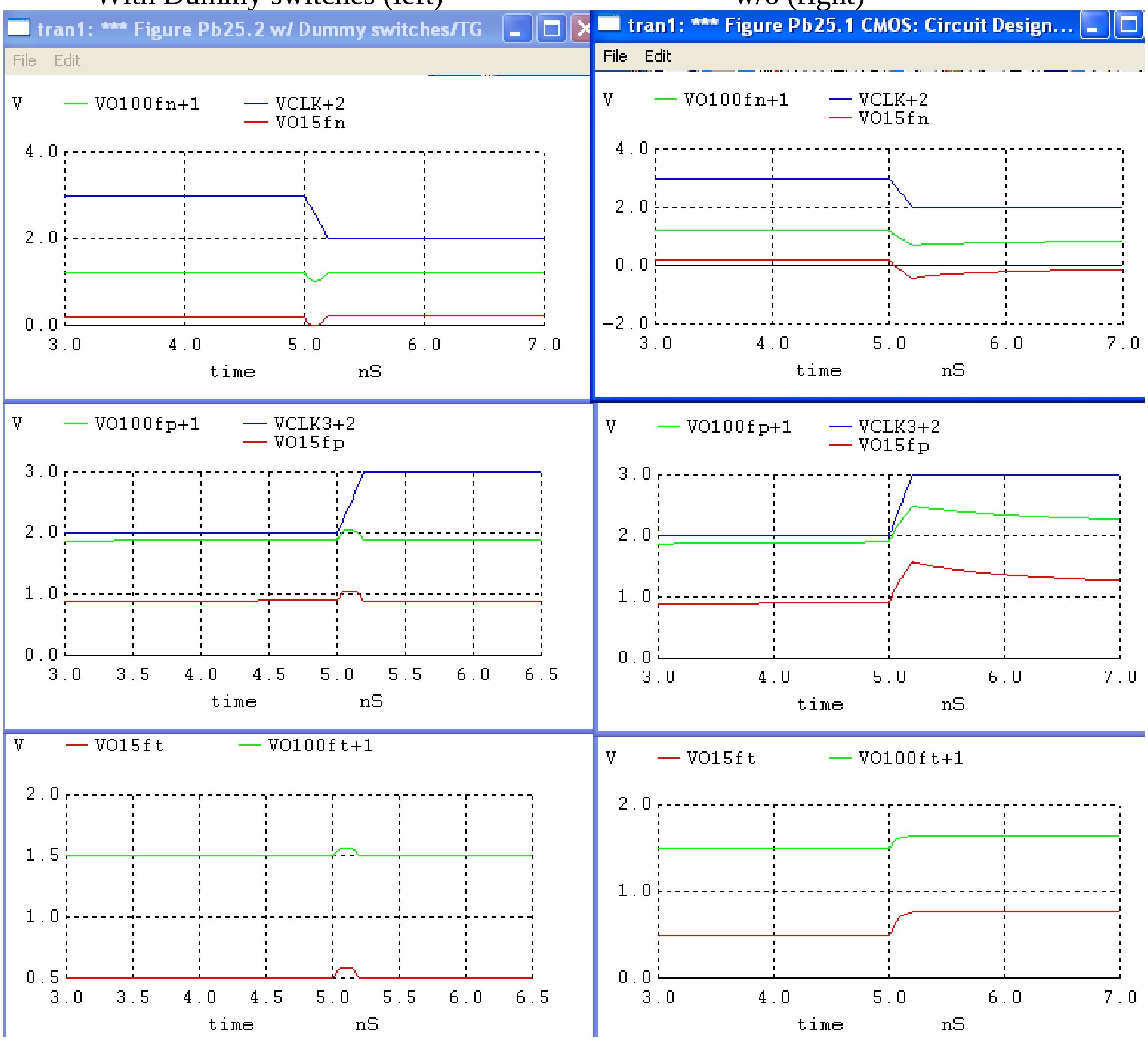
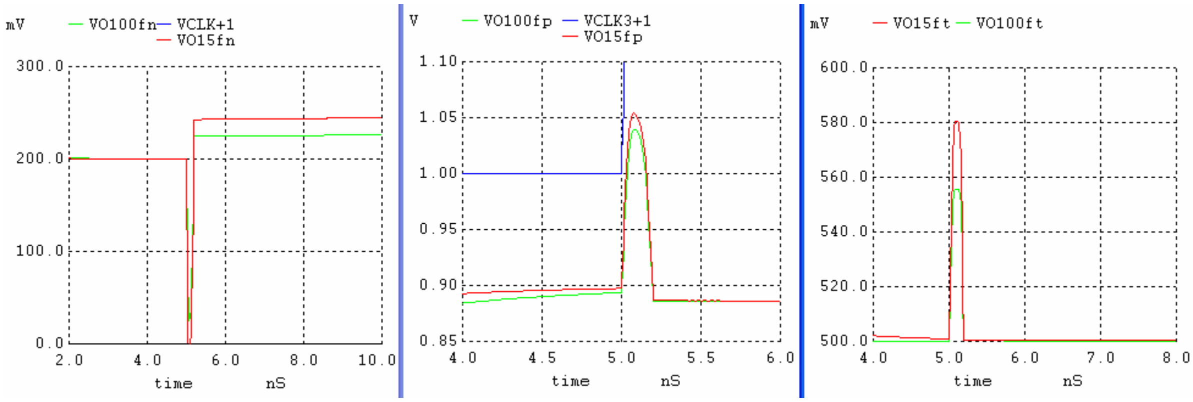


Fig 25.2-2 Clock Feedthrough performance on NMOS, PMOS, and TG
w/ CL=50fF (red), 100fF (green)



Conclusion:

1. Clock Feedthrough results from voltage divider Cgd and Cload. The larger CL is, the less voltage drops on CL. Therefore, better immune to clock Feedthrough.
2. TG gate has much less clock feedthrough than either PMOS or NMOS switch in both cases of w/ and w/o dummy compensation.
3. Pulse width equals to clock rising or falling time in practical means imperfect switching.

SPICE *** Figure Pb25.2 w/ Dummy switches/TG

```
.control
destroy all

run
plot VO15fn VO100fn VCLK+1
plot VO15fp VO100fp VCLK3+1
plot VO15ft VO100ft
.endc

.option scale=1u
.TRAN   20p     20n     0.5n    UIC
VDD     VDD     0       1

****** Nswitch ****
VIN     VIN     0       0.2
VCLK    VCLK    0       PULSE(1 0 5NS 0.2NS 0.2NS 20NS 100NS)
VCLK3   VCLK3   0       PULSE(0 1 5NS 0.2NS 0.2NS 20NS 100NS)

VCLK2   VCLK2   0       PULSE(1  0 5NS 0.2NS 0.2NS 20NS 100NS)
VCLK4   VCLK4   0       PULSE(0 1 5NS 0.2NS 0.2NS 20NS 100NS)

MN1     VO15fn  VCLK    VIN     0       NMOS L=1 W=10
MND1    VO15fn  VCLK3   VO15fn  0       NMOS L=1 W=5
CL      VO15fn  0       15f     IC=0

MN2     VO100fn VCLK2   VIN     0       NMOS L=1 W=10
MND2    VO100fn VCLK4   VO100fn 0       NMOS L=1 W=5
CL2     VO100fn 0       100f    IC=0

****** Pswitch ****
VIP     VIP     0       0.9
MP1     VO15fp  VCLK3   VIP     VDD     PMOS L=1 W=20
MPD1    VO15fp  VCLK    VO15fp  VDD     PMOS L=1 W=10
```

```
CL3      VO15fp   0        15f      IC=0

MP2      VO100fp  VCLK4    VIP      VDD      PMOS L=1 W=20
MPD2     VO100fp  VCLK2    VO100fp  VDD      PMOS L=1 W=10
CL4      VO100fp  0        100f     IC=0

****** TG ******
VI       VI       0        0.5
VCLKTP   VCLKTP   0        DC 1 PULSE(0 1 5NS 0.2NS 0.2NS 20NS 100NS)
VCLKTN   VCLKTN   0        DC 1 PULSE(1 0 5NS 0.2NS 0.2NS 20NS 100NS)
CL5      VO15ft   0        15f      IC=0
XTG15    VDD      VCLKTP   VCLKTN   VI       VO15ft   TG
XTGD15   VDD      VCLKTP   VCLKTN   VO15ft   TGDUM

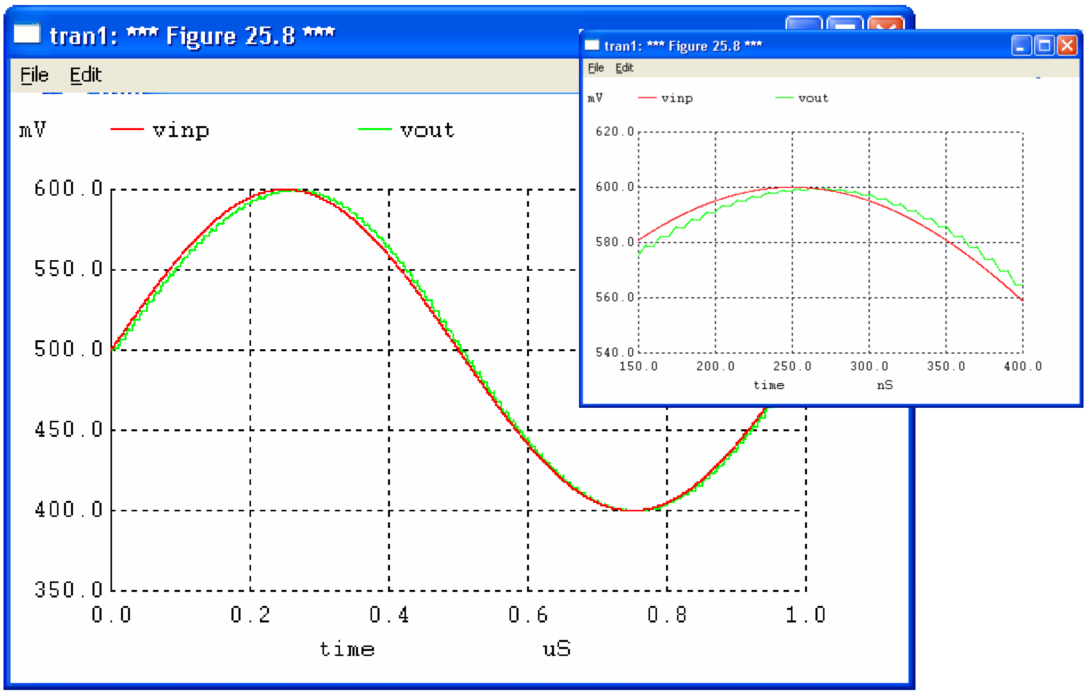
VI100    VI100    0        0.5
VCLKTP2 VCLKTP2 0        DC 1 PULSE(0 1 5NS 0.2NS 0.2NS 20NS 100NS)
VCLKTN2           VCLKTN2           0        DC 1 PULSE(1 0 5NS 0.2NS 0.2NS 20NS 100NS)
CL6      VO100ft  0        100f     IC=0
XTG100   VDD      VCLKTP2 VCLKTN2            VI100    VO100ft  TG
XTGD100 VDD       VCLKTP2 VCLKTN2            VO100ft  TGDUM

.subckt  TG       VDD      pg       ng       in       out
M1       out      pg       in       VDD      PMOS L=1 W=20
M2       out      ng       in       0        NMOS L=1 W=10
.ends

.subckt  TGDUM    VDD      pg       ng       io
M1       io       ng       io       VDD      PMOS L=1 W=10
M2       io       pg       io       0        NMOS L=1 W=5
.ends
```

25.3) Using a voltage controlled voltage source for the op-amp with an open-loop gain of 10^6 use SPICE to show how the track-and-hold seen in Fig. 25.8 operates with a sinewave input. What happens if the input sinewaves's amplitude is above VDD-V_{thn}? Use a 100MHz clock (strobe) pulse with a 50% duty cycle and an input sinewave frequency of 5MHz. Note the input sinewave should be centered around V_{cm} (=500mV).

First we'll show the operation of the track-and-hold with an input sinewave amplitude below VDD-V_{thn}.



The second part of the problem asked for an input sinewave above VDD-Vthn. From the graphs we can see that the output voltage gets clipped, this is due to the strobe pulse, input of the NMOS gate, only going to 1V so the max voltage passed through the NMOS is VDD-Vthn.

```
*** Figure 25.8 ***

.control
destroy all
run
plot vinp vout
.endc

.tran 100p 1000n
.options scale=50n

* clock signals
Vphi1  phi1   0    DC   0    PULSE 1    0 5n 0 0 5n 10n

* input signals
*vinp  vinp   0    DC   0    SIN 500m 100m    1MEG
vinp   vinp   0    DC   0    SIN 500m 500m    1MEG

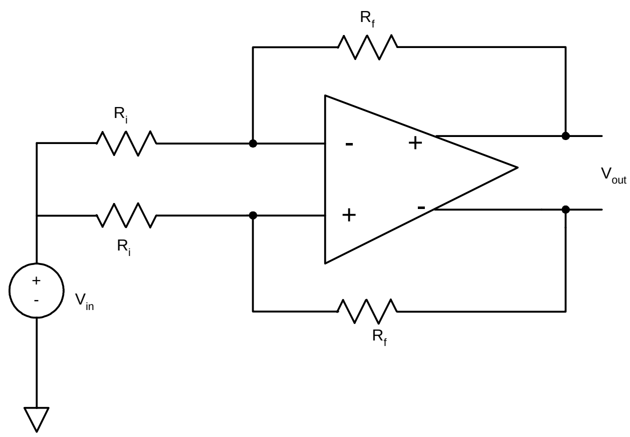
* op-amp model
E1     vout   0    vp   vout 1e6

* capacitors
Ch     vp     0    1p

* MOSFET switches
M1     vinp   phi1 vp   0    NMOS L=1 W=10

* 50nm BSIM4 models
```

25.4)   The simple differential topology is shown in the figure below:



The netlist for the above figure is shown below:

```
*** Question 25.4 ***

.control
destroy all
run
plot vp+0.1 vm
plot vop+0.1 vom-0.1 vcm
.endc

*.DC Vin 0.0 1.0 0.01
.tran 10n 0.1n
.options scale=50n



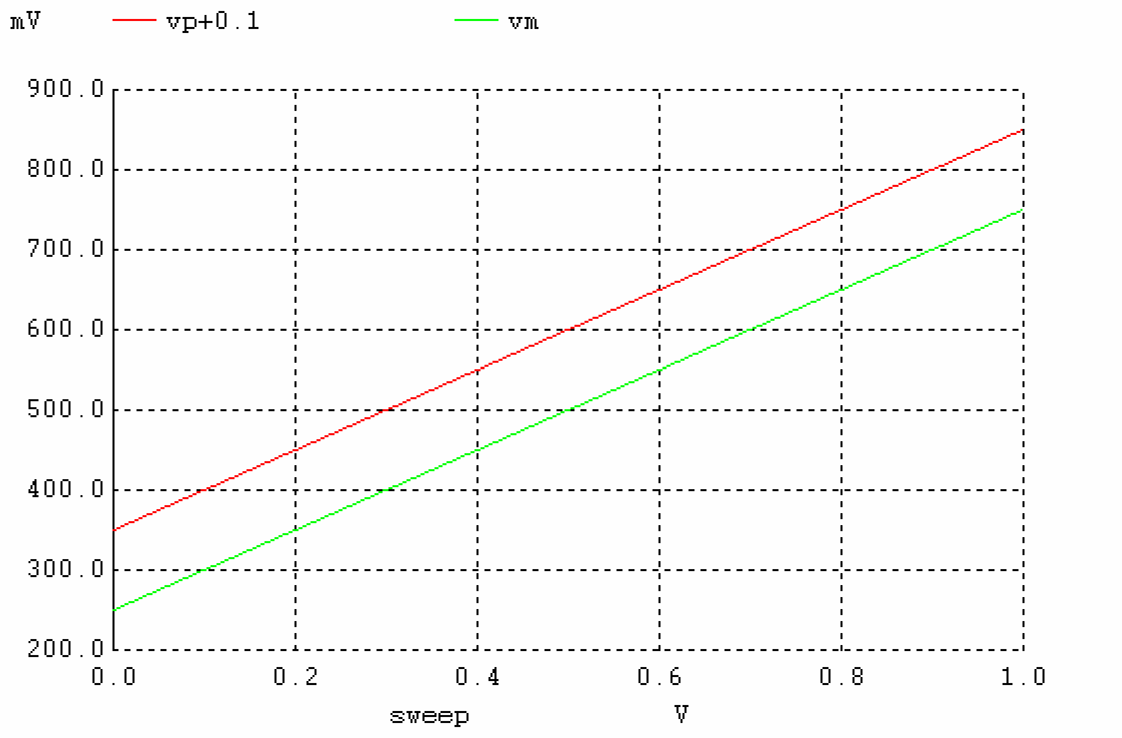
* input signals
Vin inp 0 DC 0.1


* op-amp model
E1  vop vcm vp vm 1e6
E2  vcm vom vp vm 1e6
Vcm vcm 0   DC    500m

*Feedback Resistors
Rfm vop vm 10k
Rfp vom vp 10k

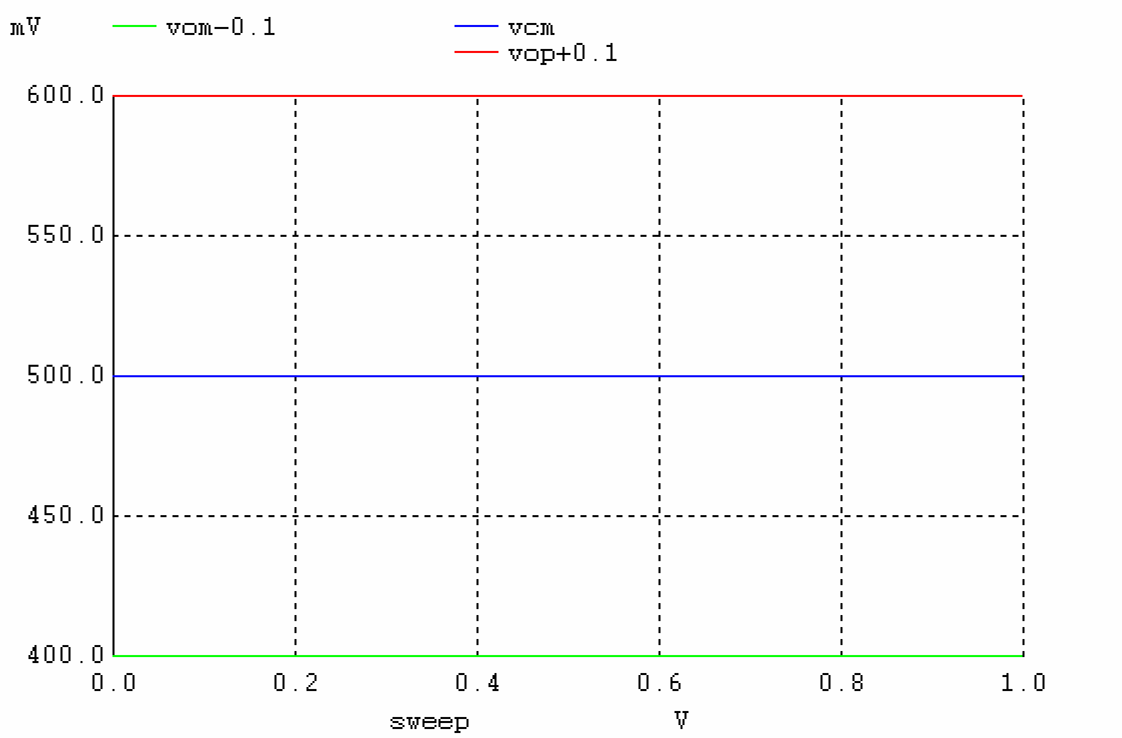
*Input Resistors
Rim vm inp 10k
Rip vp inp 10k
```

When Vin is swept, the output looks like the following:



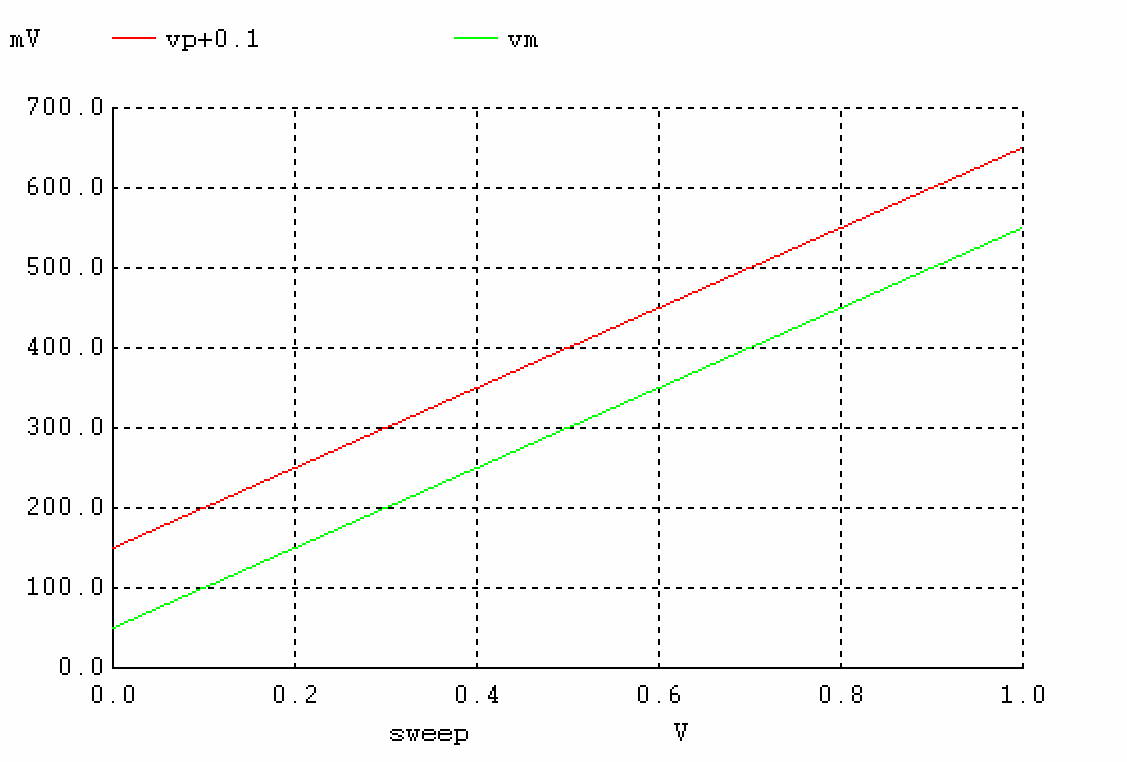
The input terminals are equal at all voltages.

The output of the differential amplifier is:



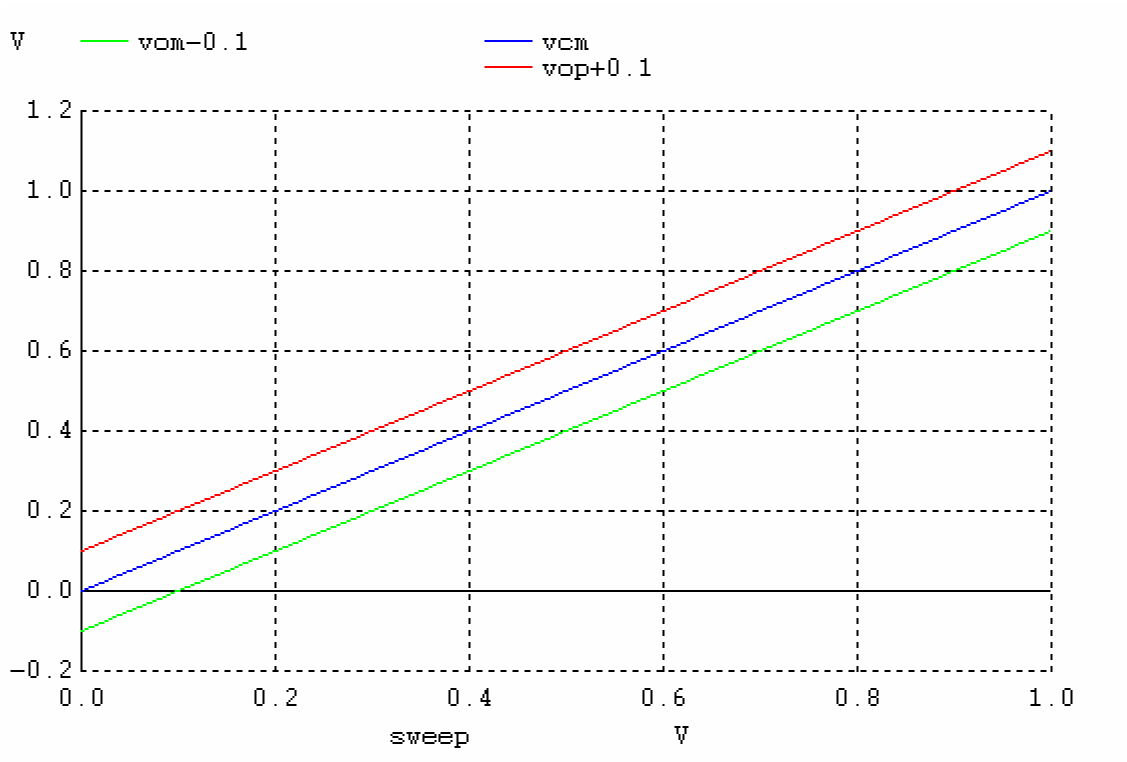
Note that the output is exactly at the common mode voltage.

When Vcm is swept:



Note that once again that the input terminals though varying are still the same.

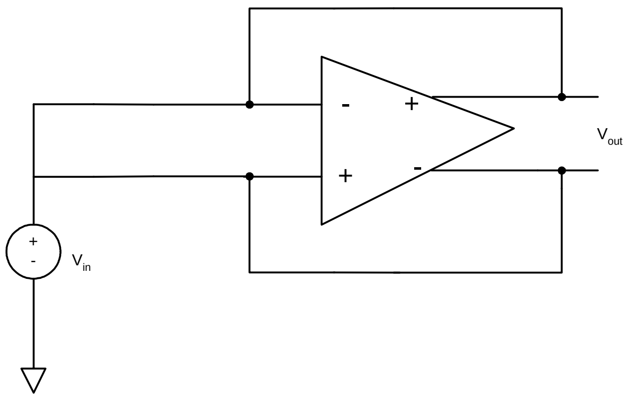
The output of the differential amplifier is shown below:



Once again it should be noted that though the output voltages are different, they are still equal to the common mode voltage.

This is to be expected since the output always referenced to the common mode voltage and not ground. Thus, since the gain of the voltage controlled voltage sources are high, they change the input voltages such that the output is always at the common mode voltage. The currents flowing through the resistors maybe different but it will not be possible to setup a situation such that the output common voltage is not the same as what was defined in the SPICE circuit model.

Note however, that a circuit like the following will cause the output voltage not to be at the common mode:



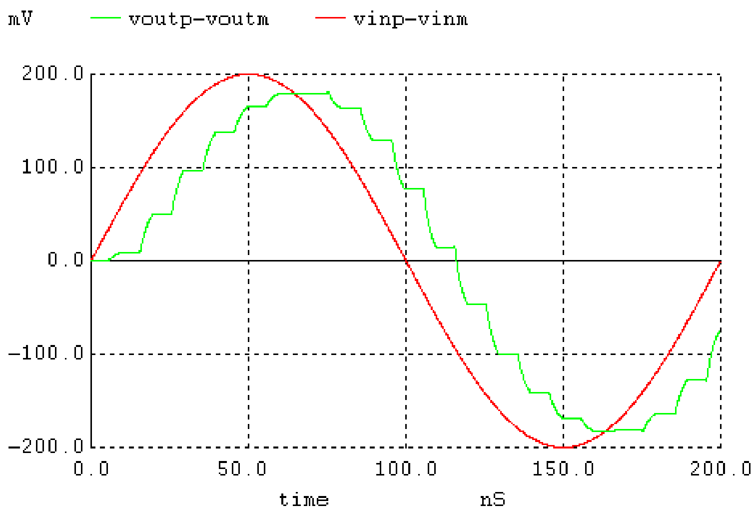
However this is unpractical and will cause simulation problems.

Problem 25.5

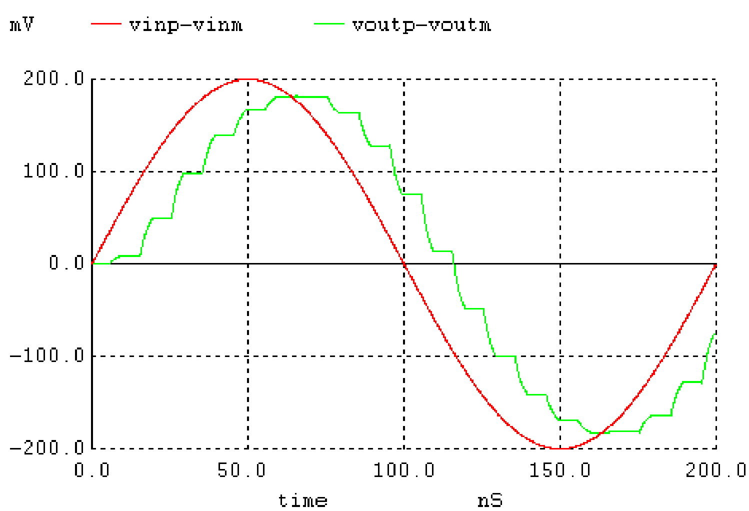
Suppose in Fig 25.19,that instead of the two input sine waves being connected to ground they are tied (together) to a common mode signal (say a noise voltage). Show, that a common mode signal (like a sine wave) won't change the circuits output signals. The amplitude of the common mode signal shouldn't be so large that the NMOS switches shut off.

Solution

When the two input sine waves in Fig 24.19 are tied together to a common mode signal (a noise signal of 5mV amplitude) instead of connecting them to ground the output signals won't change as seen in the simulations below.



Simulation with sine wave inputs connected to a common mode (noise) signal



Simulation with sine wave inputs connected to ground

```
*** Simulation for Figure 25.19
.control
destroy all
run
plot phi1+2.5 phi2+1.25 phi3
plot vinp-vinm voutp-voutm
.endc

.tran 100p 200n
.options scale=50n

* clock signals
Vphi1  phi1   0     DC   0    PULSE 1      0 5n 0 0 5n 10n
Vphi2  phi2   0     DC   0    PULSE 1      0 5.2n 0 0 5n 10n
Vphi3  phi3   0     DC   0    PULSE 0 1 5.4n 0 0 4n 10n
* input signals
vinp   vinp   vcom  DC   0    SIN 500m 100m     5MEG
vinm   vinm   vcom  DC   0    SIN 500m -100m    5MEG

vcom   vcom   0     DC   0    SIN 5m 5m    5MEG

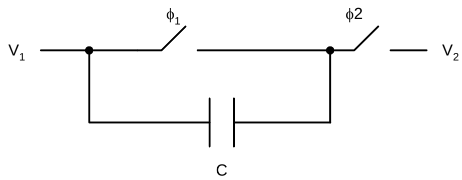
* op-amp model
E1     vop    vcm   vp   vm   1e6
E2     vcm    vom   vp   vm   1e6
Vcm    vcm    0     DC   500m

* capacitors
Ct     t1     vm    1p
Cb     b1     vp    1p
Coutp  voutp  0     1p
Coutm  voutm  0     1p

* MOSFET switches
M1     vinp   phi2  t1    0    NMOS L=1 W=10
M2     vinm   phi2  b1    0    NMOS L=1 W=10
M3     t1     phi3  vop   0    NMOS L=1 W=10
M4     b1     phi3  vom   0    NMOS L=1 W=10
M5     vm     phi1  vop   0    NMOS L=1 W=10
M6     vp     phi1  vom   0    NMOS L=1 W=10
M7     vop    phi3  voutp 0    NMOS L=1 W=10
M8     vom    phi3  voutm 0    NMOS L=1 W=10

*50nm Spice models
```

25.6a) For the following diagram:



In the ϕ_1 phase:

$$q_1 = 0$$

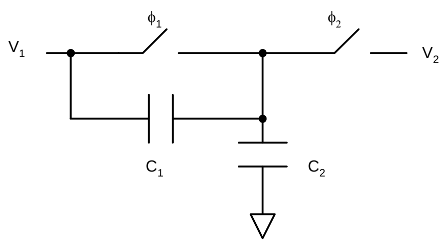
In the $\phi 2$ phase

$$q_2 = (v_2 - v_1)C$$

Therefore:

$$I_{avg} = \frac{q_1 - q_2}{T} = \frac{(v_1 - v_2)C}{T} \Rightarrow R_{SC} = \frac{1}{C \cdot f_{clk}}$$

25.6b) For the following diagram:



In the ϕ_1 phase:

$$q_1 = v_1 C_2$$

In the $\phi 2$ phase

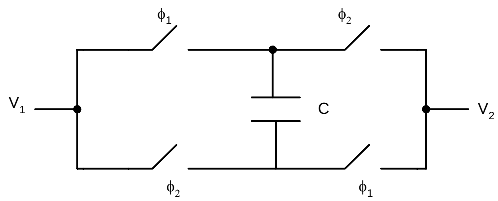
$$q_2 = (v_2 - v_1)C_1 + v_2 C_2$$

Therefore:

$$q_1 - q_2 = (C_1 + C_2)(v_1 - v_2)$$

$$I_{avg} = \frac{q_1 - q_2}{T} = \frac{(C_1 + C_2)(v_1 - v_2)}{T} \Rightarrow R_{SC} = \frac{1}{(C_1 + C_2) \cdot f_{clk}}$$

25.6c) For the following diagram:



Just prior to ϕ1 closing the charge on C is equal to $(v_2 - v_1)$. After ϕ1 closes, C is charged to $(v_1 - v_2)$. Therefore

$$q_1 = C(v_1 - v_2) - C(v_2 - v_1) = 2C(v_1 - v_2)$$

Simlarly in the ϕ2 phase

$$q_2 = C(v_2 - v_1) - C(v_1 - v_2) = 2C(v_2 - v_1)$$

$$I_{avg} = \frac{q_1 - q_2}{T} = \frac{4C(v_1 - v_2)}{T} \Rightarrow R_{SC} = \frac{1}{4C \cdot f_{clk}}$$

Problem 25.7

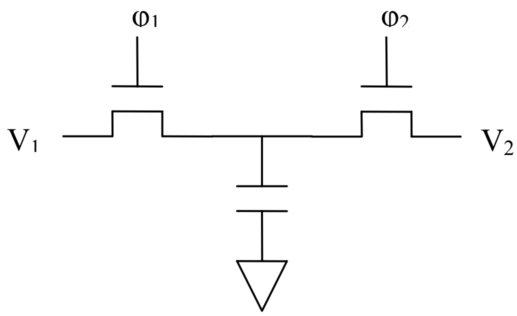


Figure 1

The switched-capacitor circuit seen in figure 1 can be used as a frequency-controlled resistor. The effective resistance of the circuit is given in *equation 25.18*

Rsc = $1/C*f_{clk}$

For this circuit to work, the clocks need to be non-overlapping and their periods long enough for the capacitor to fully charge and discharge.

Figure 2 is a plot of the actual current through the circuit. In this simulation we have used following values.

f_{clk} = 100 MHz. (non-overlapping)
V_1 = 600 mV
V_2 = 400 mV
C = 100 fF

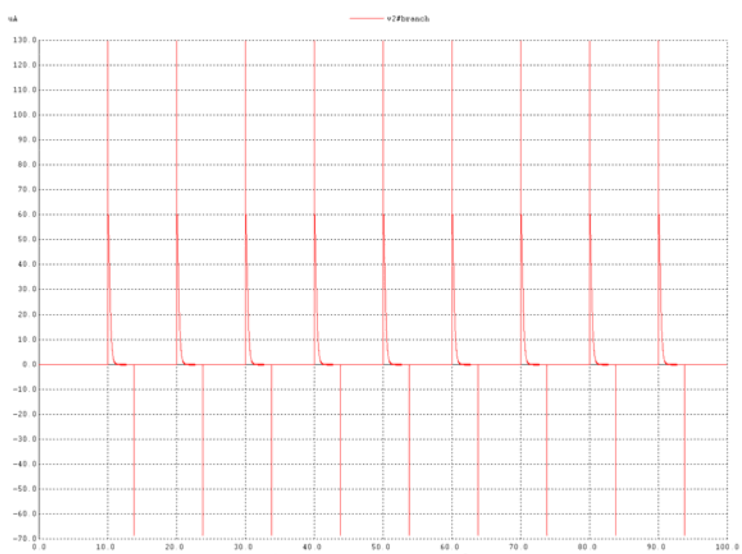


Figure 1 Actual current

If we take the mean of the actual current we get the plot below. (Iavg = 1.96uA)

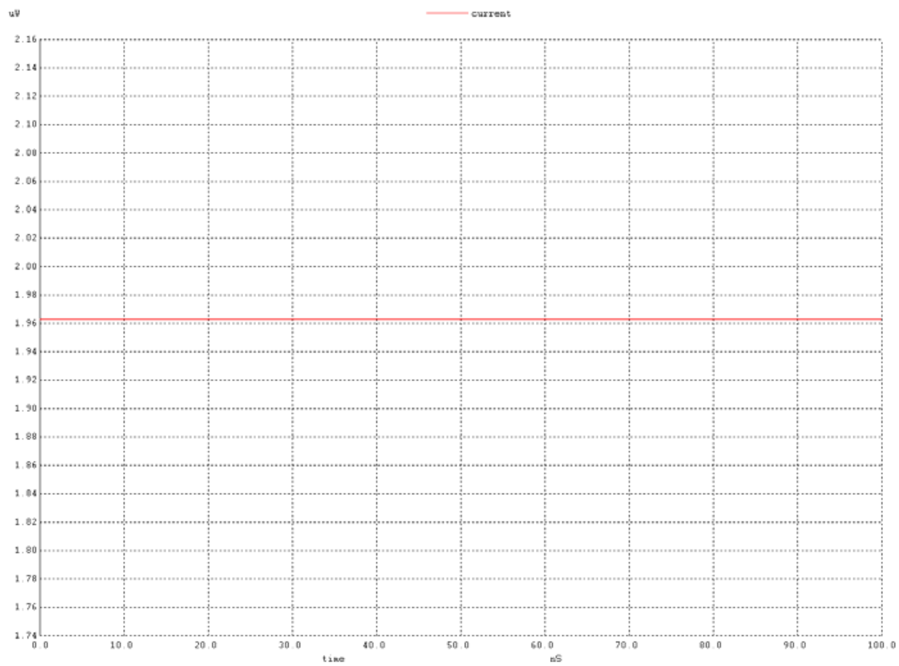


Figure 2 Mean current

Lets also look at what is happening with the voltage potential of the capacitor and the non-overlapping clocks(scaled-down).

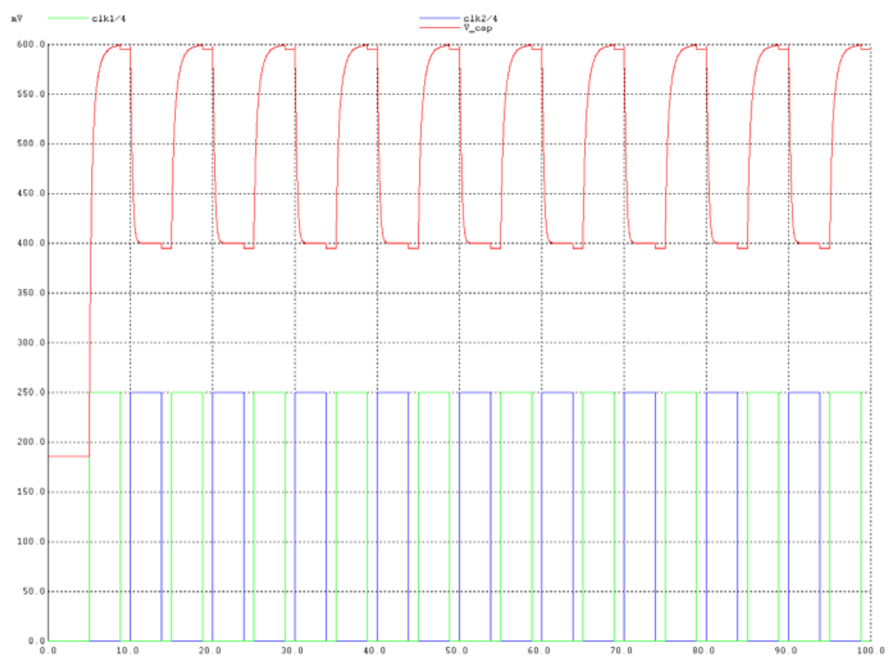


Figure 3 capacitor voltage and the non-overlapping clocks

If we calculate Rsc and the expected current we get,

$Rsc = 1/(100fF)(100MHz) = 100k\Omega$, then,

$I = (V_1 - V_2)/Rsc = (.6-.4)/100k = 2\ \mu A$

This current value is very close to the simulation results. The difference in the values may be caused by clock feedthrough. In figure 3, if we look at the voltage on the capacitor when φ_1 goes low, we see it drop slightly.

The bottom plate of the capacitor should be connected to ground. This will avoid having the parasitic substrate capacitance from being in parallel with the switched capacitor. With the bottom plate connected to ground, both sides of the parasitic substrate capacitance are at ground.

The netlist:

```
problem 25.7
.control
destroy all
run
let current = unitvec(length(v2))*mean(v2#branch)
let V_cap = n1
plot V_cap clk1/4 clk2/4
plot current
.endc

.option scale=50n
.tran    10p     100n

vclk1   clk1    0       DC=0 pulse(0 1 5n 0 0 3.8n 10n)
vclk2   clk2    0       DC=0 pulse(0 1 10n 0 0 3.8n 10n)

V1      v1      0       DC=.6
V2      V2      0       DC=.4

M1      v1      clk1    n1      0       NMOS L=1 W=10
M2      v2      clk2    n1      0       NMOS L=1 W=10

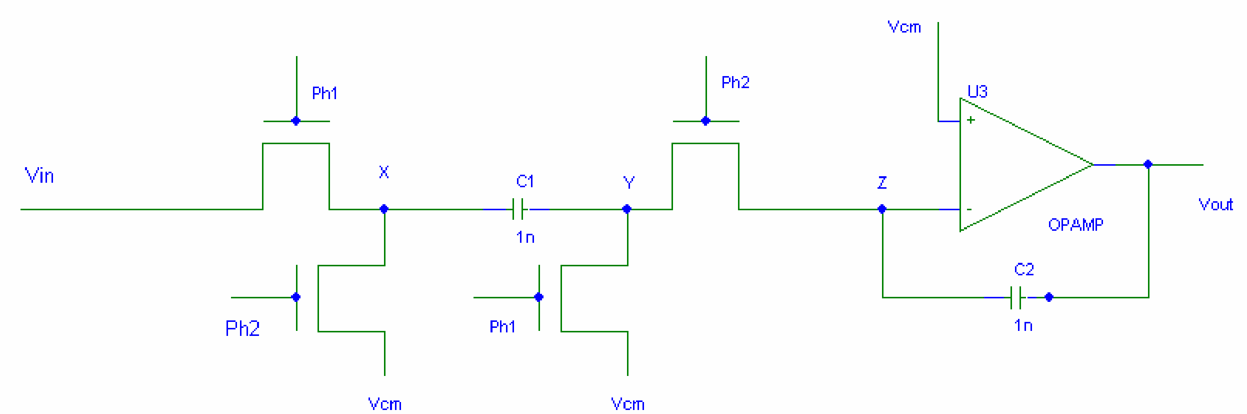
C1      n1      0       100f

.include .\50nm_models.txt
.end
```

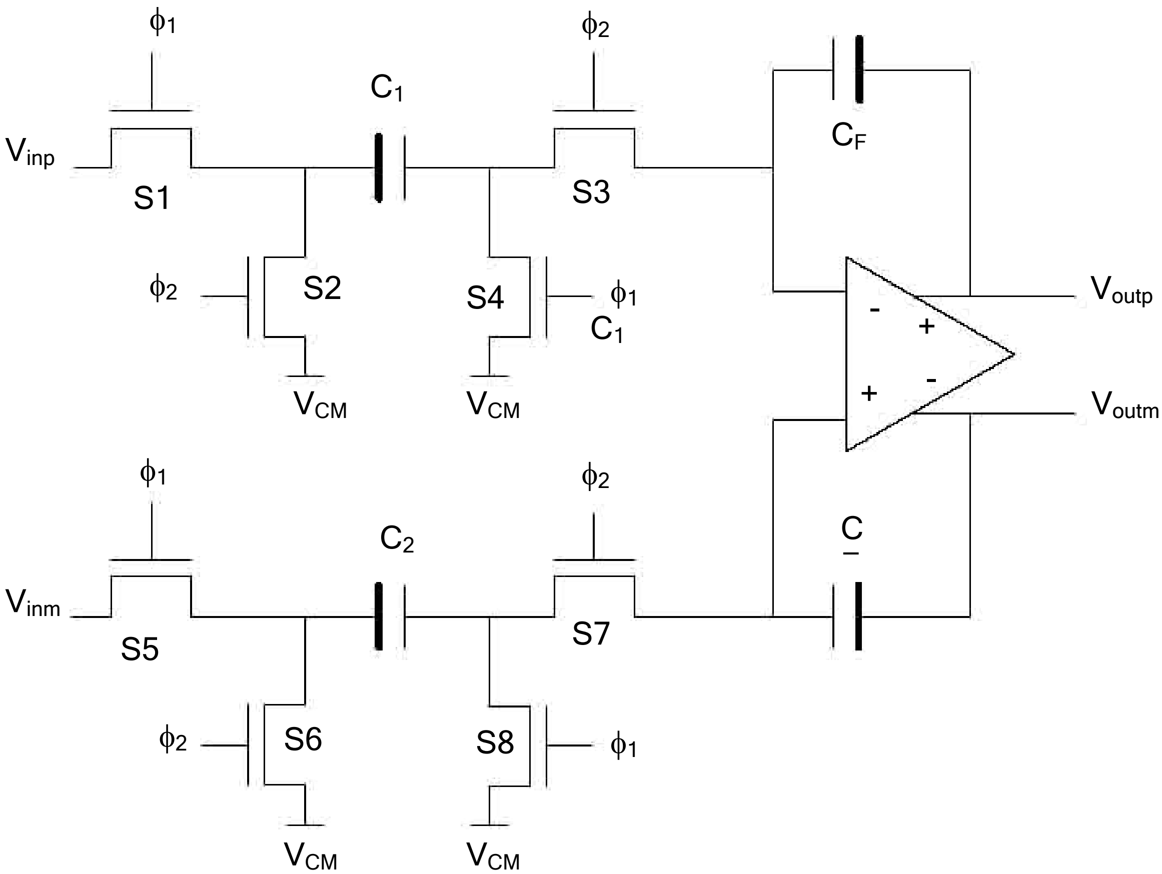
Problem 25.8 Comment on the selection of bottom plate of Cf in the given figure:

The bottom plate capacitor on the input capacitor is connected to X, as any change on the substrate voltage doesn’t feed into the input of the opamp. Consider the case when Ph1 is ON, during this time any substrate noise doesn’t feed to the top plate, but gets coupled on the i/p voltage source which is a low impedance node. On the other hand when Ph2 is ON and ph1 is off, the noise feeds on to the i/p voltage source Vcm and doesn’t get coupled to the opamp i/p.
Now consider the case where the bottom plate is connected to node Y. Here when Ph1 is ON it doesn’t affect the opamp input, but when Ph2 is ON it couples the substrate noise to the opamp input.

Moving to the capacitor on the feedback section. It is very obvious that we don’t want any noise from the substrate to feed on to the i/p, to be amplfied by the opamp. Which explains why we connect the bottom plate to the o/p node.



Problem 25.9



The transfer function is given by:

$$\frac{\text{V}_{\text{inp}}}{v_{in}} : \frac{v_{outp}-v_{outm}}{v_{inp}-v_{inm}} = \frac{v_{outp}-v_{outm}}{V_{CM}} = \frac{\left(\frac{1}{j\omega C_F}\right)}{R_I}$$

where

$$R_I = \frac{1}{j\omega C_I\, f_{CLK}}$$

and f_{CLK} is the frequency of the clock signals φ_1 and ϕ_2.

$$\frac{v_{out}}{v_{in}} = \frac{\left(\frac{1}{j\omega C_F}\right)}{\left(\frac{1}{j\omega C_I\, f_{CLK}}\right)} \Rightarrow \frac{1}{j\omega\left(\frac{C_F}{C_I}\frac{1}{f_{CLK}}\right)}$$

P25_10

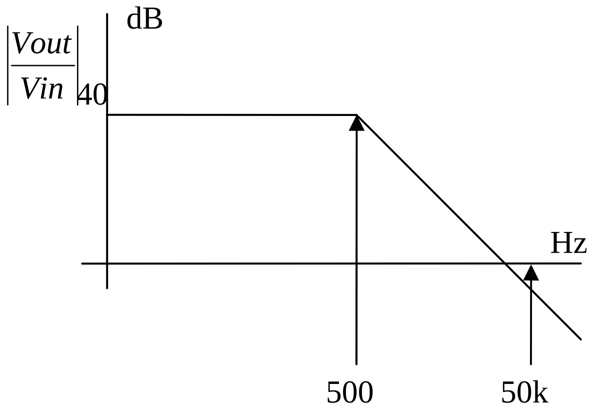


Figure 1.

The low frequency gain is:

$$20*\log(gain) = 40 \Rightarrow gain = 10^2 = 100$$
$$\frac{C3}{C4} = 100$$

The pole and the zero are given by:

$$f_p = \frac{1}{2*\pi*\left(\frac{C2}{C4}*\frac{1}{fclk}\right)} = 500 \text{ and } f_z = \frac{1}{2*\pi*\left(\frac{C1}{C3}*\frac{1}{fclk}\right)} = 5000$$

Using fclk=100kHz and C4=100fF $\Rightarrow$ C3=10pF, C2=3.2pF and C1=.32pF

Problem 25.11

The transfer function given by equation (25.29) is:

$$\frac{v_{out}(j\omega)}{v_{in}(j\omega)} = \frac{1}{j\omega\left(\frac{C_F}{C_I}\frac{1}{f_{CLK}}\right)}\left(\frac{\frac{\pi \cdot f}{f_{CLK}}}{\sin\left(\frac{\pi \cdot f}{f_{CLK}}\right)} e^{\frac{-j\omega f}{f_{CLK}}}\right)$$

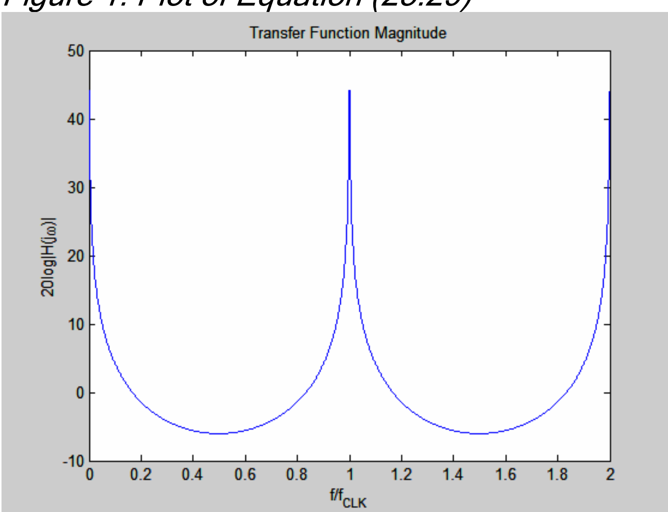
The magnitude of this function is:

$$\left|\frac{v_{out}(j\omega)}{v_{in}(j\omega)}\right| = \frac{1}{\omega\left(\frac{C_F}{C_I}\frac{1}{f_{CLK}}\right)}\frac{\frac{\pi \cdot f}{f_{CLK}}}{\sin\left(\frac{\pi \cdot f}{f_{CLK}}\right)}$$

If we normalize our function about $f_{CLK} = 1$, and let our capacitance ratio equal unity, we arrive at:

$$\left|\frac{v_{out}(j\omega)}{v_{in}(j\omega)}\right| = \frac{1}{2\pi \cdot f}\frac{\pi \cdot f}{\sin(\pi \cdot f)} = \frac{1}{2 \cdot \sin(\pi \cdot f)}$$

Figure 1: Plot of Equation (25.29)



Several observations can be made from Figure 1. The gain goes infinite at input frequencies of DC, f_{CLK}, $2f_{CLK}$, and so on. This makes sense, and this a characteristic of all digital filters. Basically, the space between DC and f_{CLK} is repeated indefinitely along the spectrum. The minimal gain occurs at half the sampling frequency, and that is represented as -6dB on the plot.

EE597 HW 25.12 Dong Pan

25.12 For Fig 25.28, if Ci is 5pf and fclk is 100Khz, estimate the Min. Slew rate requirements for the opamp providing Vin

T=1/f = 10u. We need to charge the Ci in half cycle.

For worst input condition, we need to charge the capacitor to VDD or GND, which the difference between the voltages of the cap is +/- VDD/2.

V= input slewrate * t

Min input slew rate = V/t = 0.5 /5 u =0.1 V/ us

Geng Zheng

Problem 25.13

Problem: Suppose the op-amp in problem 25.12 is used with a feedback factor of 0.5. Estimate the minimum unity gain frequency (fun) that the op-amp must possess.

Solution:

The op-amp has to charge the C_I to the desired input voltage in half clock cycle. Thus the settling time of the op-amp, t_{set}, should be less than half of the clock period. i.e.,

$$t_{set} \leqslant \frac{1}{2 f_{clk}}$$

The input voltage of the SC circuit, or the output voltage of the op-amp, can be estimated as (see Eq. 25.34 on page 853)

$$v_{\mathrm{in}} = V_{\mathrm{in,final}} (1 - e^{-t_{set}/\tau})$$

where $\tau = \frac{1}{2\pi f_{un} \beta}$ (Eq. 25.33 on page 853) is the close-loop time constant of the op-amp circuit.

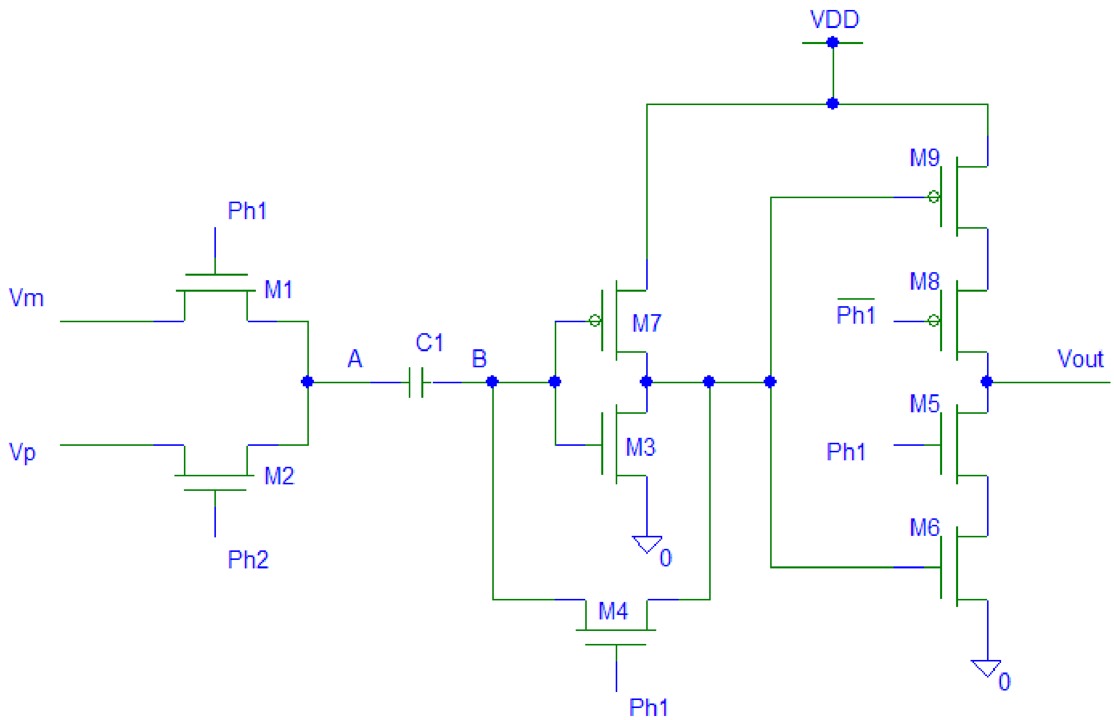
Assume v_{in} is required to settle to less than 1% of its final value, then

$$V_{\mathrm{in,final}} (1 - e^{-t_{set}/\tau}) = V_{\mathrm{in,final}} (1 - 1\%) \quad \rightarrow \quad t_{set} \approx 5\tau$$

Thus we have

$$5 \cdot \frac{1}{2\pi f_{un} \beta} \leqslant \frac{1}{2 f_{clk}} \quad \rightarrow \quad f_{un} \geqslant \frac{5 \cdot f_{clk}}{\pi \beta} = \frac{5 \cdot 100\, kHz}{\pi \cdot 0.5} \approx 318.3\, kHz$$

Problem 25.14: Solution

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*** PROBLEM 25.14 CMOS: Circuit Design, Layout, and Simulation ***

.control
destroy all
run
plot vp vm vout
.endc
.tran  100p 1u 0.1n
.options scale=50n

vp     vp     0      dc     0      pulse 0 1 0 1u
vm     vm     0      dc     0.5
VDD    VDD    0      DC     1

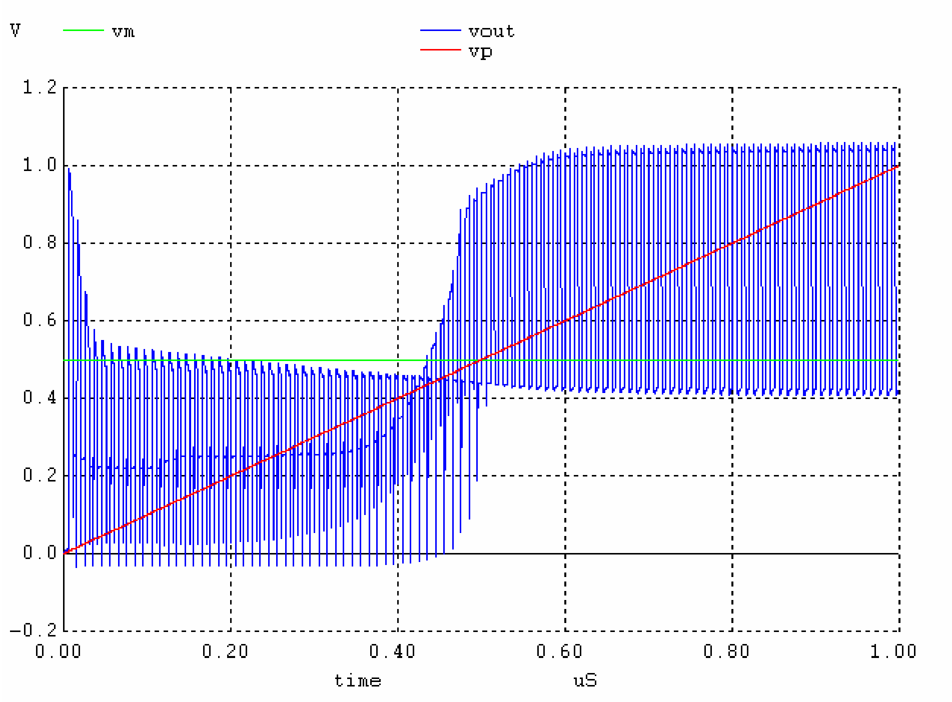
Vphi1  phi1   0      DC     0      PULSE 0      1 5.2n 0 0 5n 10n
Vphi2  phi2   0      DC     0      PULSE 1      0 5n   0 0 5n 10n

X1     vtout  vb     vdd    inverter
Ca     va     vb     1p
Ma     vm     phi1   va     0      NMOS L=1 W=10
Mb     vp     phi2   va     0      NMOS L=1 W=10
Mc     vb     phi1   vtout  0      NMOS L=1 W=10

****output Latch****************

X1L    phi1bar phi1  vdd    inverter
M1PT   VDTP1  vtout  VDD    VDD    PMOS L=1 W=20
M1PB   VOUT   PHI1BAR       VDTP1  VDTP1  PMOS L=1 W=20
M1NT   VOUT   PHI1   VDTN1  VDTN1  NMOS L=1 W=10
M1NB   VDTN1  vtout  0      0      NMOS L=1 W=10

.subckt inverter vout      vin    vdd
M1     vout   vin    0      0      NMOS L=1 W=10
M2     vout   vin    vdd    vdd    PMOS L=1 W=20
.ends
```



V
vm
vout
vp
1.2
1.0
0.8
0.6
0.4
0.2
0.0
−0.2
0.00
0.20
0.40
0.60
0.80
1.00
time
uS