5.1   Suppose a current in a circuit is given by

$$I = \frac{V_{REF}}{R}$$

        If the voltage V_{REF} comes from a precision voltage reference and doesn't change with temperature determine the temperature coefficient of the current in terms of the resistor's temperature coefficient. If the resistor is fabricated using the n-well plot, similar to Fig 5.1, the current's change with temperature. Use the TCR1 given in table 4.1.

Sol:

$$TCI1 = \frac{1}{I}\frac{dI}{dT} = \frac{1}{I}\frac{dI}{dR}\frac{dR}{dT} = \frac{1}{I}\frac{dI}{dR}.TCR1.R$$

$$I = \frac{V_{REF}}{R}$$

$$\frac{dI}{dR} = -\frac{V_{REF}}{R^2} = -\frac{I}{R}$$

$$TCI1 = -\frac{1}{I}.\frac{I}{R}TCR1.R.$$

$$= -TCR1$$

So the temperature coefficient of the current = -TCR1 or the –ve of the resistor's temperature coefficient.
For a resistor fabricated in n-well from TCR1 = 500ppm/C

$$I = \frac{V_{REF}}{R}(1 + 0.0005.(T - T_0))^{-1} \text{ OR } \frac{V_{REF}}{R}(1 - 0.0005.(T - T_0))$$
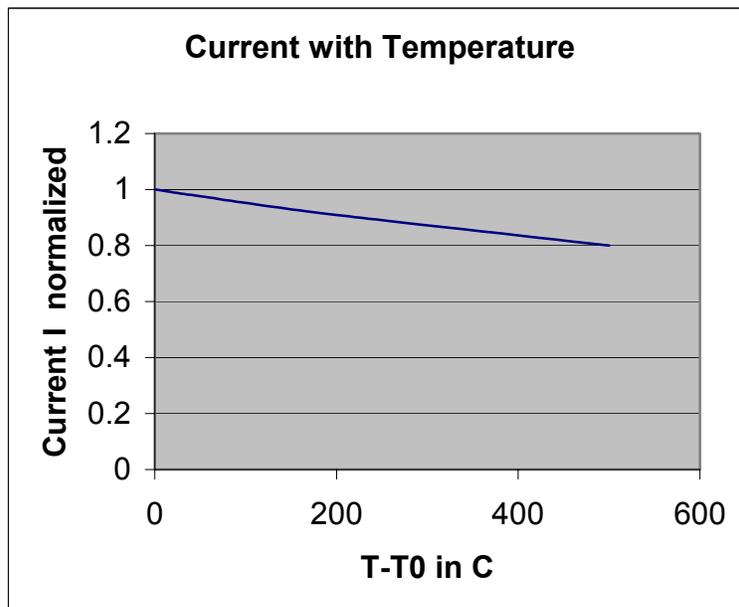
Harish Reddy Singidi

5.2) Suppose a silicided n^+ resistor is used with a value of 100Ω. Using the data from Table 4.1. Sketch the layout and cross-sectional views of the resistor. The current in the resistor flows mainly in silicide. Suppose the mobility of free carriers in the silicide is constant with increasing temperature. Would the temperature coefficient of the resistor positive or negative? Why?

Solution:

Resistance = 100 Ω
Sheet resistance of silicided n+ resistor = 10 Ω/square. [From Table 4.1]
# of squares = 10

N-Select

Active

Silicide

FOX n^+ FOX

p-substrate
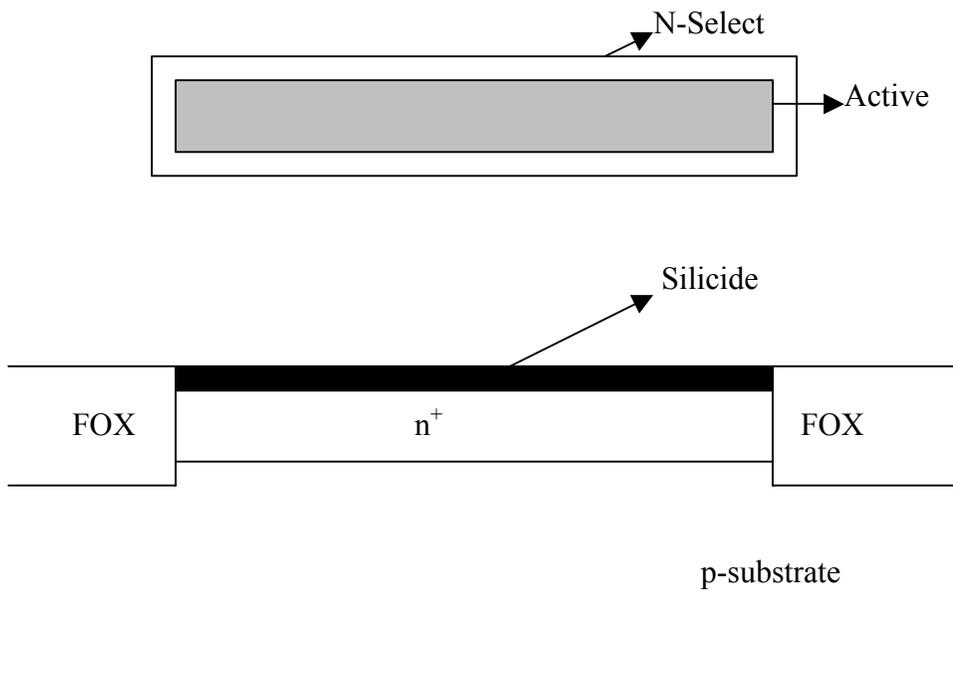
It the mobility of free carriers in the silicide is constant with increasing temperature, the temperature coefficient of the resistor is negative, because as the temperature increases the number of thermally generated carriers in silicided n^+ resistor increase which decrease the resistivity.

Submitted by L. Bollschweiler
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5.3 Using a layout program make a schematic and layout for the 1/5 voltage divider seen if Fig. 5.4 if the resistor's value is 5k. Use n-well resistors and DRC/LVS the final layout and schematic.


(a) A unit cell.

Input

Output (4/5 divider)

(b) A 4/5 voltage divider.

To ground
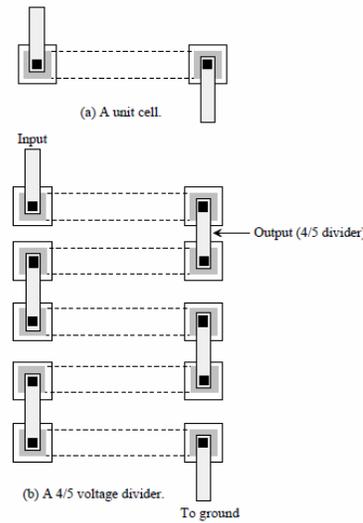
Figure 5.4 (a) Layout of a unit resistor cell, and (b) layout of a divider.

N-well sheet resistance = 796Ω/□. See: http://www.mosis.com/cgi-bin/cgiwrap/umosis/swp/params/ami-c5/t85r-params.txt

5kΩ/796Ω/□ = 6.28□. Minimum n-well width = 12. Length = 6.28*12=75.4. Each resistor will be 75.4 long in between the M1 to n-well contacts. Using MOSIS C5 process design rules this is 75.4units * 0.3µm/unit = 22.6µm.

12(dx=0, dy=12)

75.5(dx=75.5, dy=0)

NCC Message
"No Errors Found"

Vin

V_80_percent
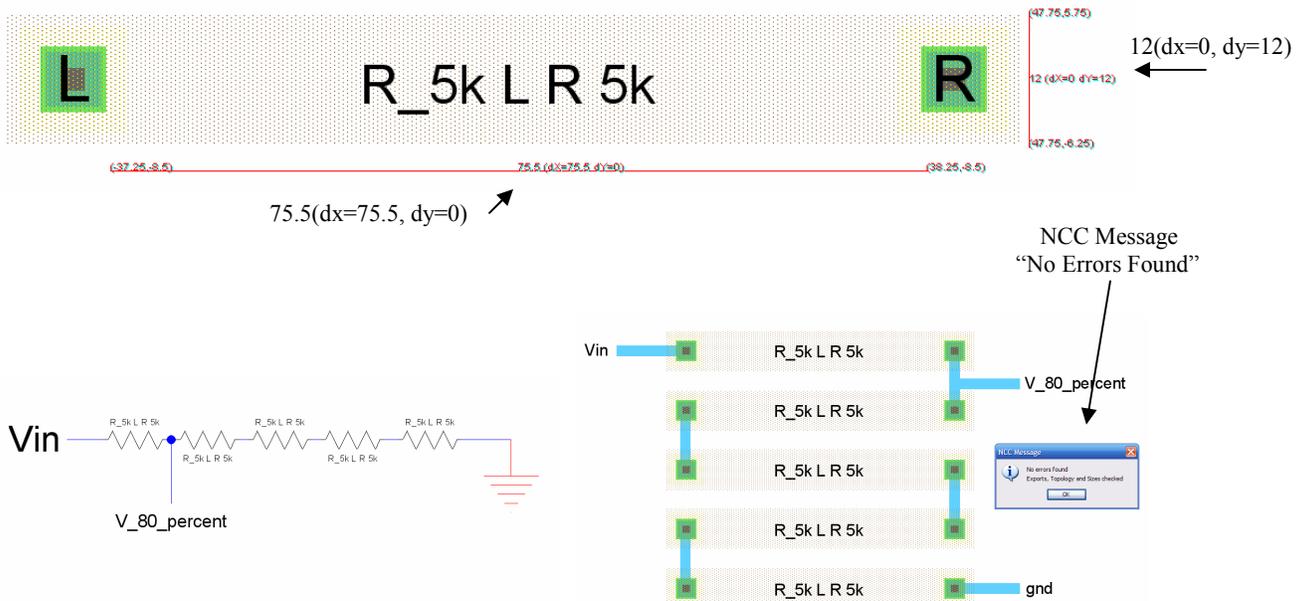
5.4 Using a layout program, make a schematic and layout for an RC lowpass circuit where the resistor's value is 10k and the poly-poly capacitor's value is 100fF. Use the 50nm process (see Table 5.1). DRC/LVS the final layout and schematic. Simulate the operation of the circuit with a pulse input (see Fig 1.27).

Vin Vin 0 DC 0 Pulse 0 1 6n 0 0 3n 10n
.tran 100p 30n

10k

Vin————/\/\/\————Vout

100f

SCHEMATIC

R1 X Y 10k

Vout

Vin

Vin Vin 0 DC 0 Pulse 0 1 6n 0 0 3n 10n
VGND GND 0 DC 0
.tran 100p 30n

NCC Message

ⓘ No errors found
Exports, Topology and Sizes checked

OK

C1 A B 100f

gnd

LAYOUT (**LVS** result shown)

Electric Messages

```
Checking cell 'Cap_100f{lay}'
        No errors/warnings found
Checking cell 'Res_1k{lay}'
        No errors/warnings found
Checking cell 'RC_Lowpass{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.032 secs)
```
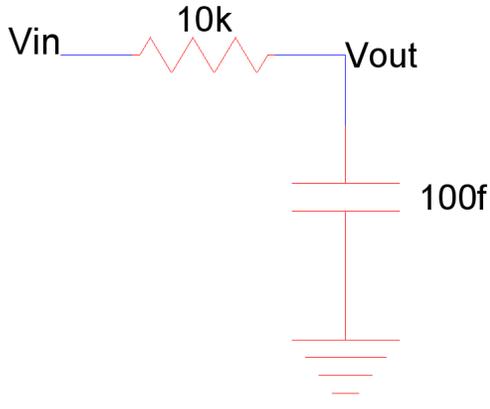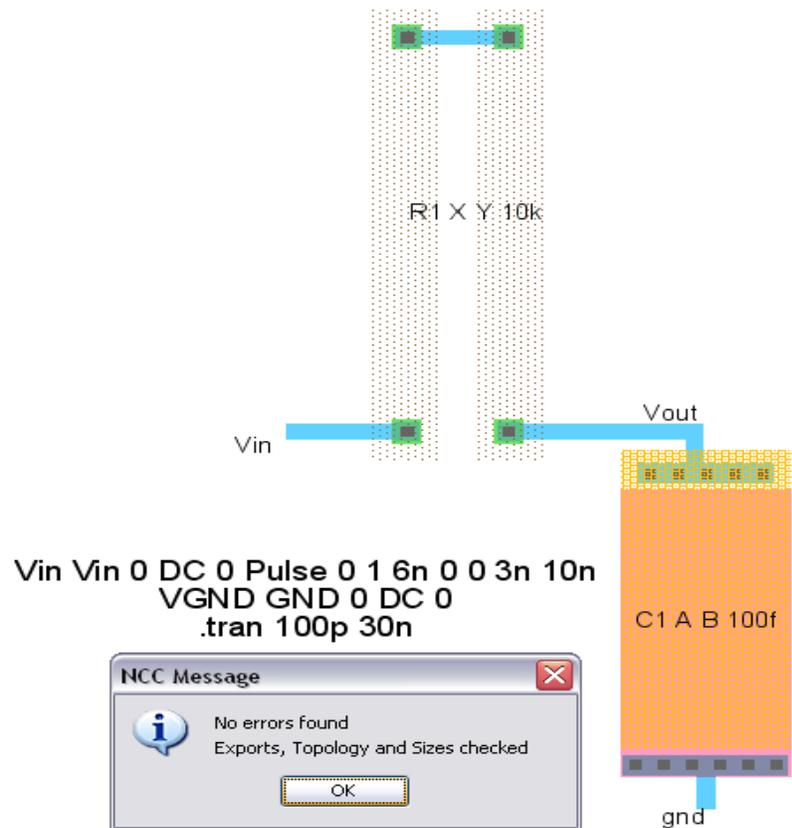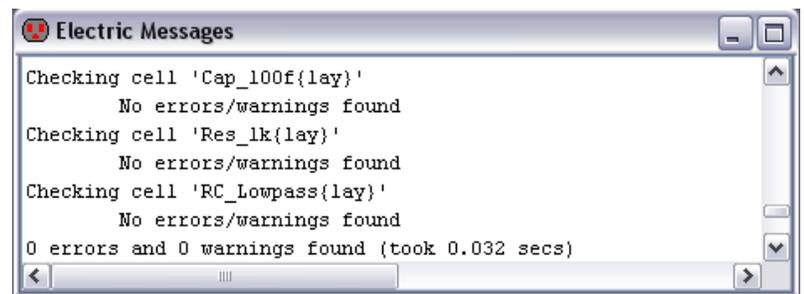
DRC of the layout showing 0 errors

C'ox = 25fF *(From table 5.1)*

For 100fF the capacitors dimension was selected as 55 by 30

$C = C'ox.A.(scale)^2$

$C = 25 \text{ fF/um}^2 . 55 . 30 . (0.05 \text{ um})^2 => C = 103fF$

Sheet resistance of n-well = 800Ω/sq *(From MOSIS)*
No. of squares for 10k resistor = 12
R = 12 . 800 = 9.6kΩ.

Delay Calculations:

td = 0.7. R. C => td = 0.7 . 10kΩ . 100fF
td = 0.7nS

Simulation Results:
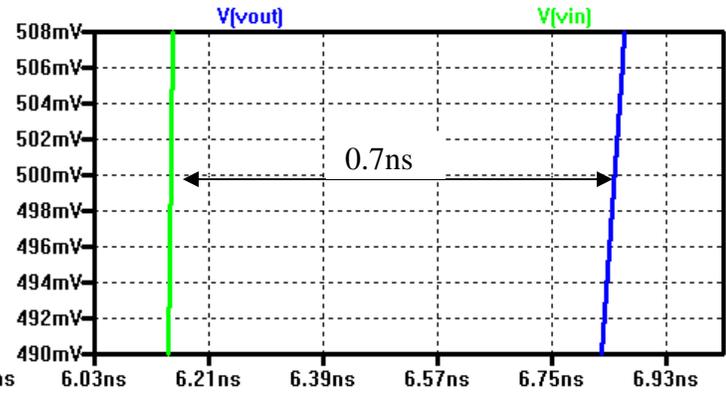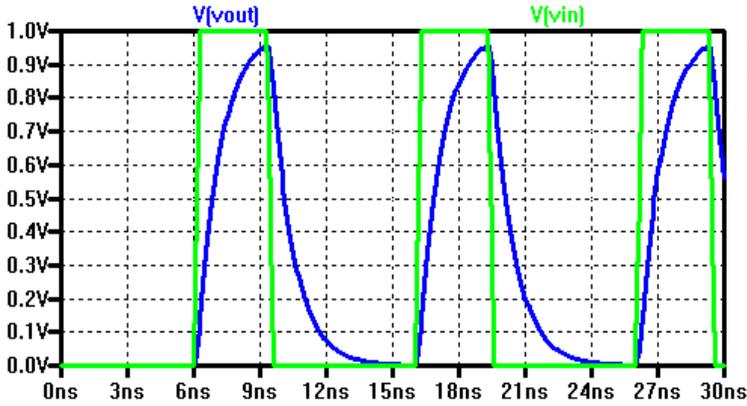
From Schematic: td = 0.7ns
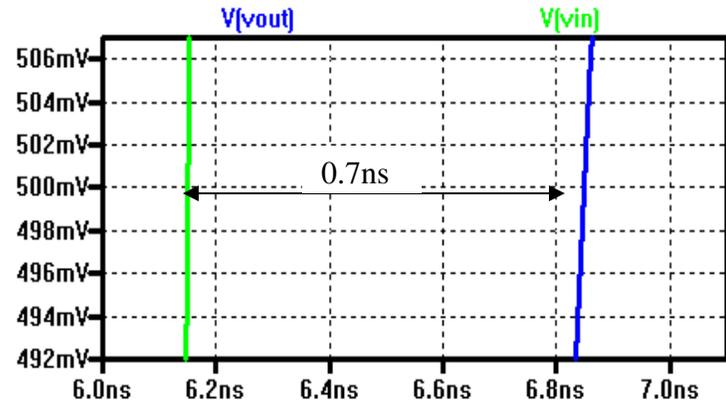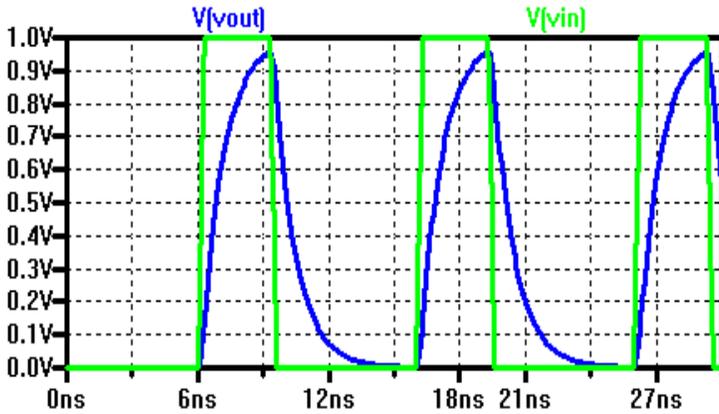
From Layout: td = 0.7ns

Figure 3 shows that LVS (layout vs. schematic) comparison run with 0 errors.
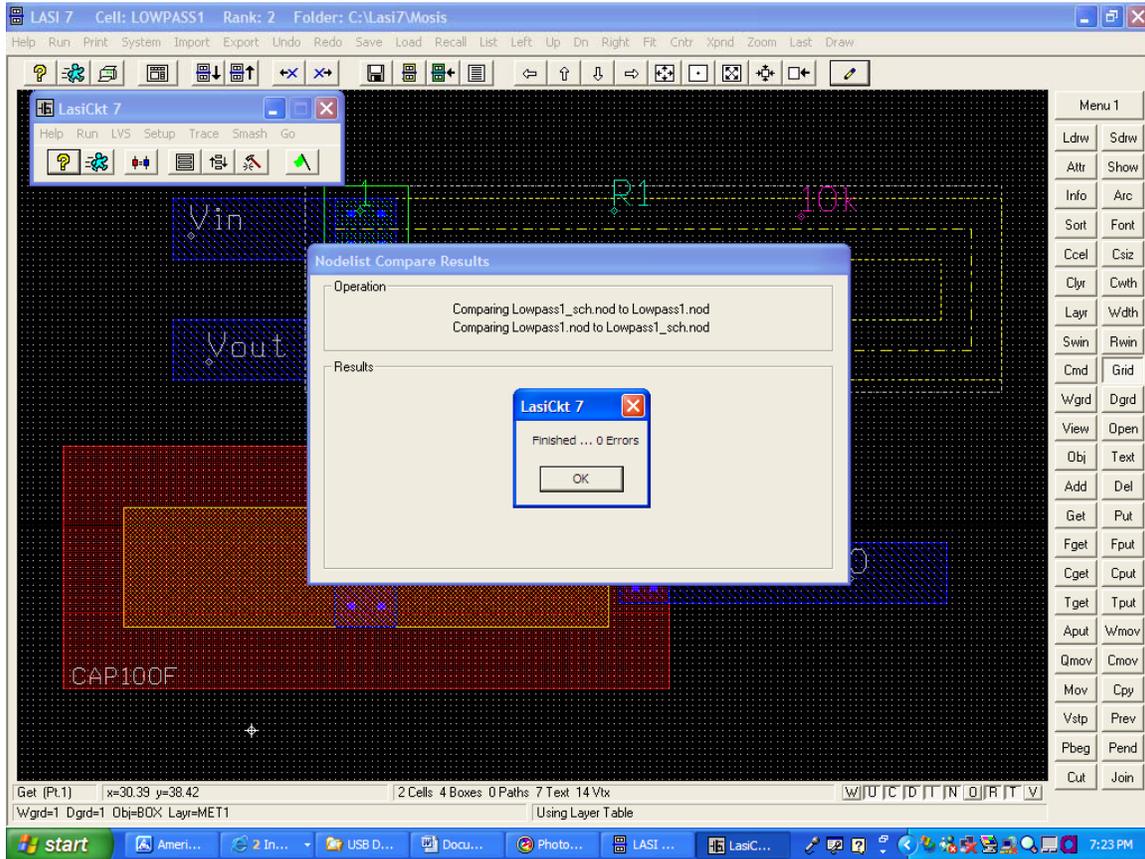
Figure 3. LVS of lowpass circuit

From layout using LASIckt, top level netlist file was created as show Figure 4.

```
*** SPICE Circuit File of LOWPASS1  02/29/04 18:53:08
* Start of C:\Lasi7\Mosis\Header_lp.txt
.control
destroy all
run
plot vin vout
.endc
.tran 100p 5n
Vin     Vin     0       DC      0       pulse 0 1 2n 10p 10p 0.5n 5n
* End of C:\Lasi7\Mosis\Header_lp.txt
* MAIN LOWPASS1
C1 Vout 0 0.1p
R1 Vin Vout 10k
.END
```

Figure 4. Top level netlist file for lowpass circuit

R C= 1 ns

F_{3db}=1/(2 π R C) = 159 Mhz

Since this is lowpass circuit, for low frequencies (<159 Mhz or pulse width > 1 ns) Vout/Vin ≥ 0.707. Figure 5 shows simulation results for 5ns pusle width. There is enough time for capacitor to be charged through resistor.
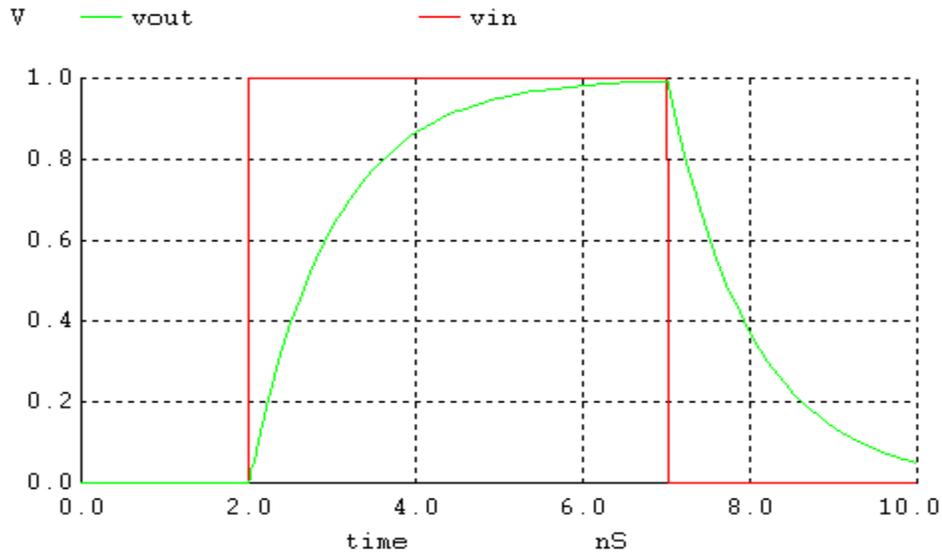

Figure 5. Spice simulation for 5ns pulse

Figure 6 shows simulation results for 1ns pulse. Output voltage is about 700 mv which is at about 3db frequency.
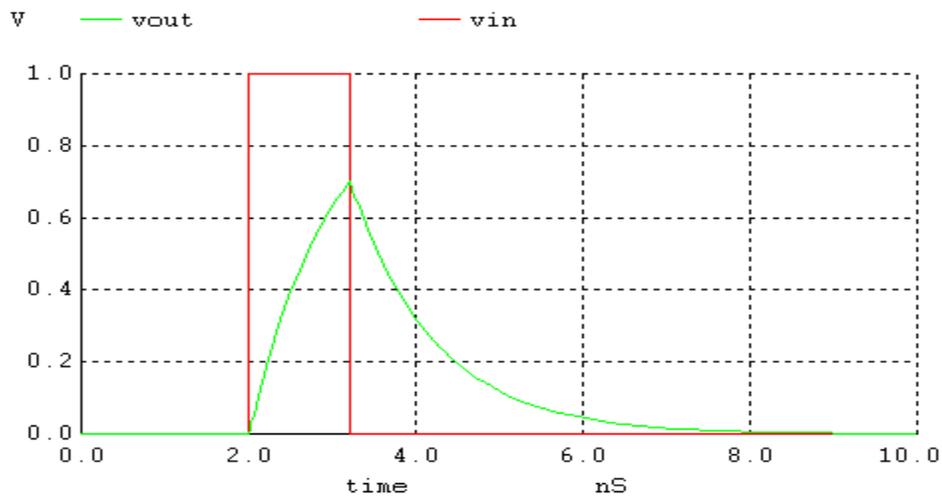

Figure 6. Spice simulation for 1ns pulse

Figure 7 shows simulation results for ½ ns pulse. There is not enough time for capacitor to be charges. Output voltage charges up to 400mv.
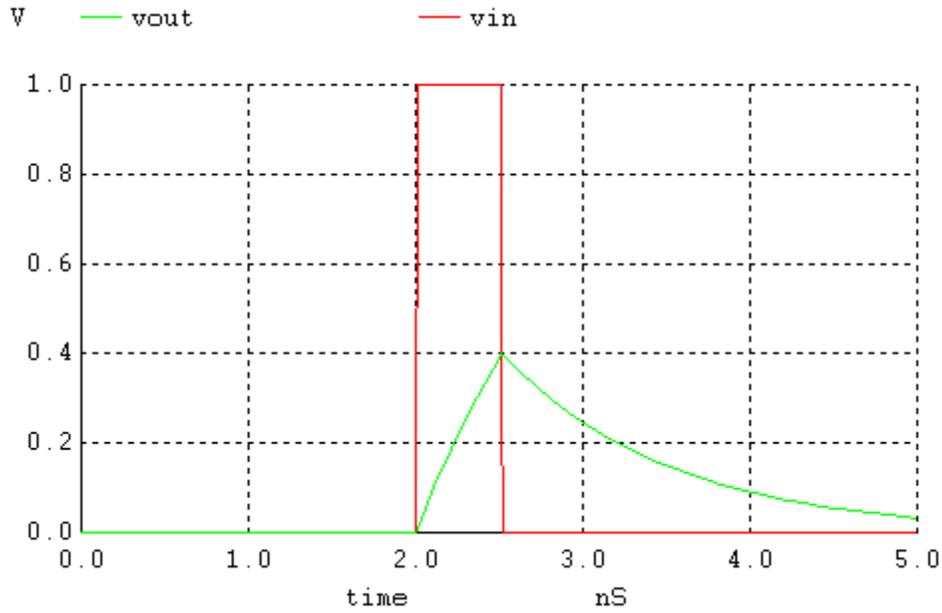

Figure 7. Spice simulation for ½ ns pulse

If we continued this process for narrower pulses (very high frequencies) output voltage Vout would approach to 0 V.

5.5) Estimate the areas and perimeters of the source/drain in the layout seen in Fig. 5.18 if the length of the device, L, is 2 and the width of a finger, W, is 20.

Source:

Figure 5.18 Layout of a large MOSFET.
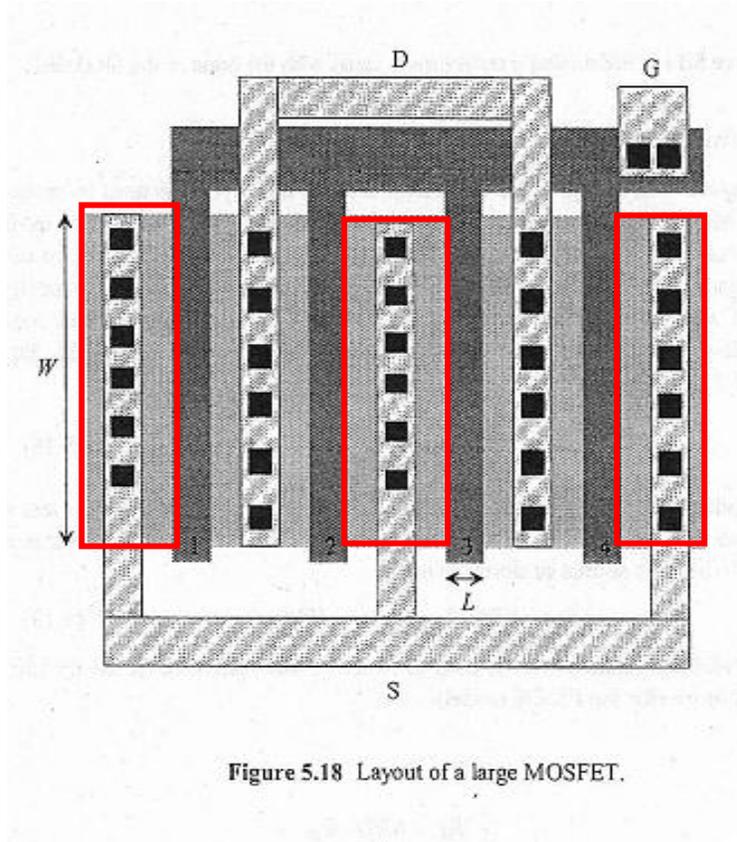
The source consists of three separate sections, which have been highlighted in red above. Based on the information given in the problem (L=2 and W=20), the three sections were estimated to be Wx2L each. Therfore, the total area of the source was estimated to be

$$3*(W*2L) = 3*(20*2(2)) = \textbf{240 units}^2$$

The total source perimeter was estimated to be

$$3*(2W+2(2L)) = 3*(2*20+2(2*2)) = \textbf{144 units}$$

Drain:
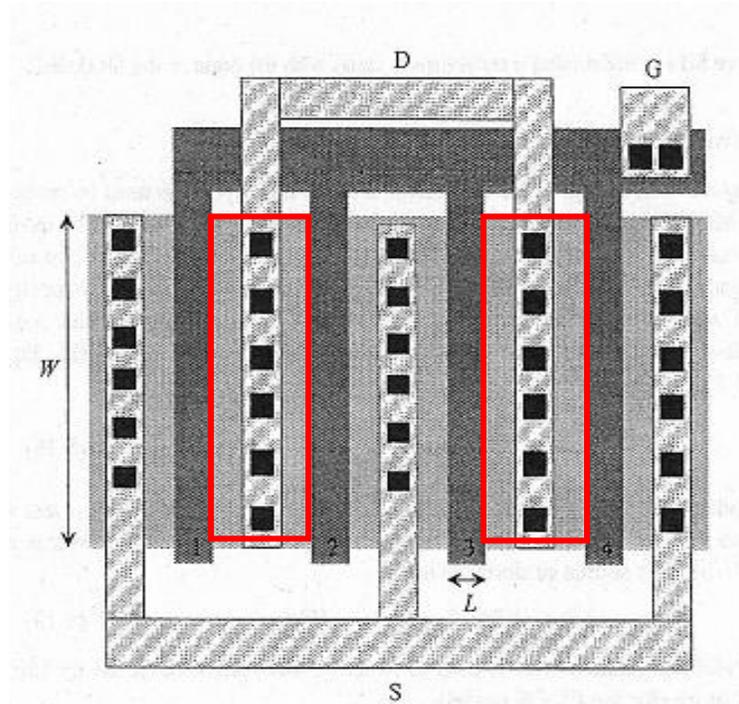
Figure 5.18 Layout of a large MOSFET.

The drain consists of two separate sections, which have been highlighted in red above. Based on the information given in the problem (L=2 and W=20), the two sections were also estimated to be Wx2L each. Therfore, the total area of the drain was estimated to be

$$2*(W*2L) = 2*(20*2(2)) = \textbf{\textit{160 units}}^2$$

The total drain perimeter was estimated to be

$$2*(2W+2(2L)) = 2*(2*20+2(2*2)) = \textbf{\textit{96 units}}$$

S. Bard

Problem 5.6

Question: Provide a qualitative discussion for the capacitances of the PMOS device similar to the discussion associated with Fig. 5.21 for the NMOS device. Make sure the descriptions of the operation in the strong inversion and depletion regions are clear. Draw the equivalent (to Fig. 5.21) figure for the PMOS devices.

Solution: PMOS operates in strong inversion when a negative or 0 potential is applied to the gate. That potential attracts positively charged holes to the channel region, as shown in figure 1 below. This continuous channel of holes brings about a gate capacitance of $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \cdot W \cdot L$, where L is the channel length and W is the device width. The capacitance changes when the device operates in depletion. In that case, shown in figure 2, a positive gate voltage repels holes and prevents a channel from forming. Carriers from the p+ regions, which form the drain and source, diffuse laterally in the n-well underneath the gate. This diffusion area, of length L_{diff}, now is responsible for the gate capacitances. The gate-drain and gate-source capacitances become $C_{gd} = C_{gs} = C'_{ox} \cdot L_{diff} \cdot W$, where

$C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$.

These capacitances are called the gate-drain overlap capacitance (CGDO) and the gate-source overlap capacitance (CGSO), respectively. They are given by $CGDO = CGSO = C'_{ox} \cdot L_{diff}$. According to the text, they are an important component of the capacitance at a MOSFET's gate terminal.
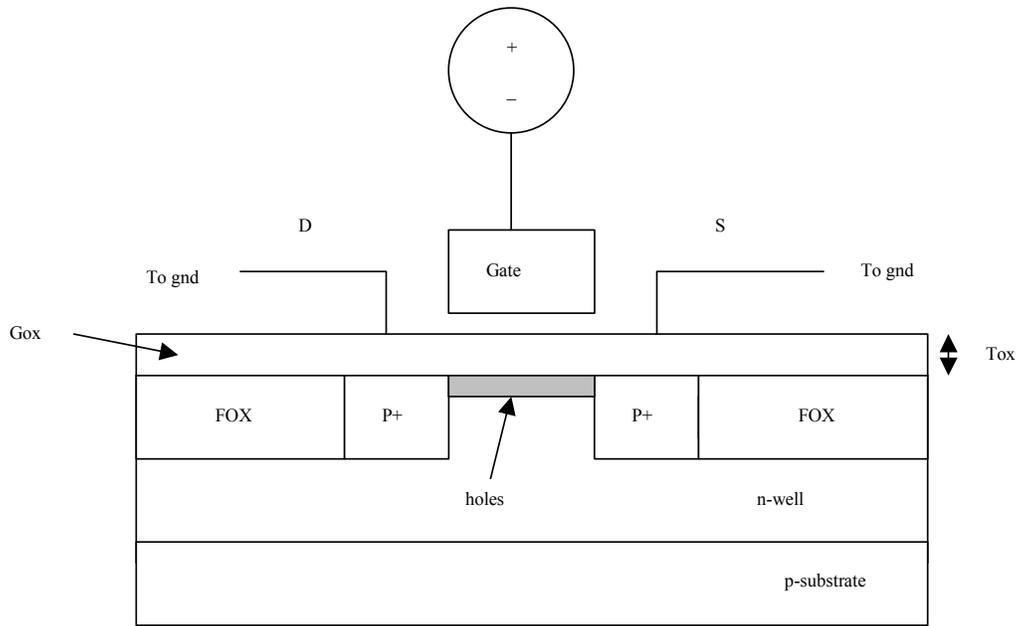
Fig. 1: PMOS device in strong inversion
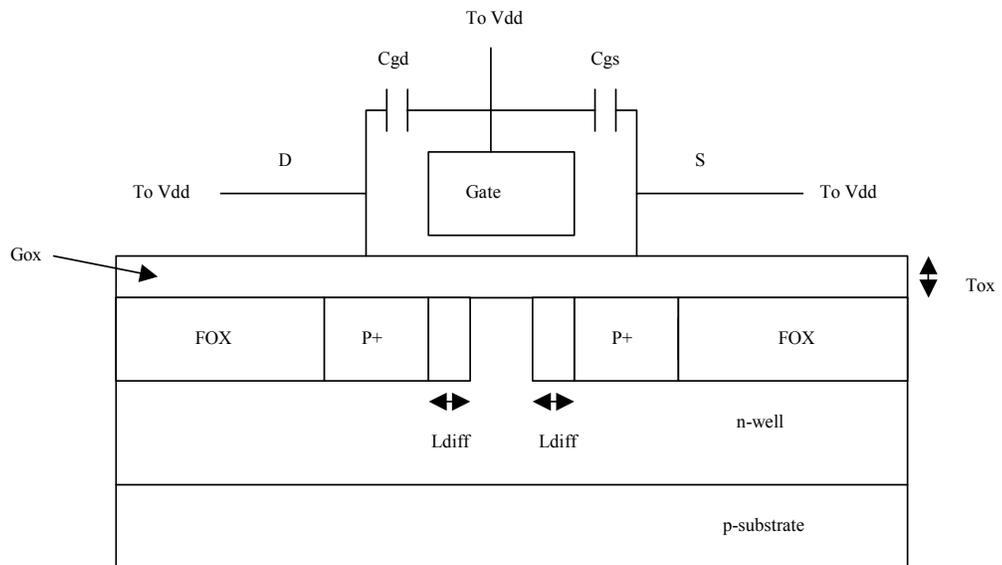
Fig. 2: PMOS device in depletion