Problem 20.1

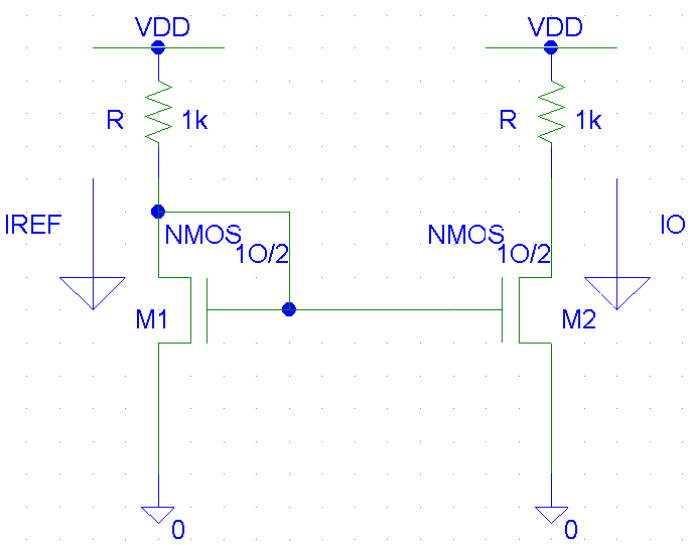


Figure 1.

Since the Drain Resistors and M1 and M2 are the same size, it can be said that:

$$VDS1 = VGS1 = VGS2 = VDS2$$

Since, M1 is diode connected, and a current IREF is running through it, M1 is in saturation, and:

$$IREF = \frac{KP_N}{2} * \frac{W_1}{L_1} * (VGS1 - VTH_N)^2$$

And from Figure 1,

$$IREF = \frac{(VDD - VGS1)}{100K}$$

Setting these two equal and solving for VGS1 gives,

$$30 * VGS1^2 - 47 * VGS1 + 14.2 = 0 \Rightarrow VGS1 = 1.15V \text{ OR } .409V .$$

For M1 to be in Saturation VGS1 must equal 1.15V. Putting this value into the equation for IREF, gives:

$$IREF = \frac{VDD - VGS1}{R} = \frac{5 - 1.15}{100K} = 38\mu A$$

If we don't concern ourselves with channel length modulation:

$$\Rightarrow \frac{IO}{IREF} = \frac{W1}{W2} \Rightarrow IO = \frac{10\mu}{10\mu} * 38\mu A = 38\mu A \qquad \text{(EQ.20.4)}$$

These results are verified with the following SPICE netlist and Figure 2.

```
*** hw_20_1

.control
destroy all
run
LET IREF=VREF#BRANCH
let Io=Vo#branch
plot IREF Io
.endc

.option scale=1u
*.dc Vo 0.1 10 1m
.tran 1ns 1us

VDD     VDD     0       DC      5
VREF    VR1     VGS1    DC      0
Vo      vo      vd2     DC      0


R1      VDD     VR1     100k
R2   VDD        VO      100K

M1      VGS1  VGS1  0  0  NMOS L=2 W=10
M2      VD2   VGS1  0  0  NMOS L=2 W=10
**models excluded
```

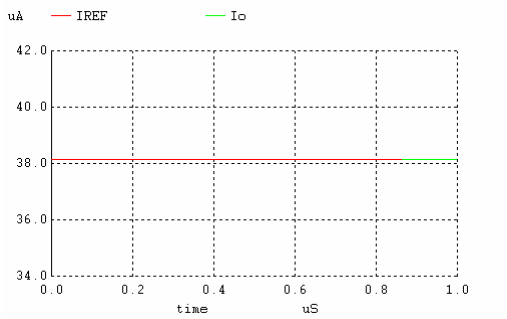


Figure 2

Problem 20.2 Solution by Robert J. Hanson, CNS

Problem Statement:

Repeat Problem 20.1 for when M2 has VDS2=VDS1=VGS1. Can M1 and M2 be replaced with a single MOSFET? If so how and what size? If not why?

From the figure for Problem 20.2 we see that W/L=10/2 for both MOSFETs. We also know that VDS1=VGS1=VDS2=VGS2. We also know that this is a long channel process and VDD=5V, VTHN=0.8V for NMOS devices, CLM Labmda=0.01, and KPN=120u and R is given as 100k.

Since the same current flows in the resistor as the sum of both MOSFETs (the MOSFETs are in parallel with each other and in series with a resistor.

We have 2 diodes in saturation so the ID equation in saturation will be used.

(5-VGS1)/R = KPN/2*W/L*(VGS1-VTHN)^2*(1+Lambda(VDS-VDS,SAT))

Here VGS1=VDS=VGS, VDS,SAT=VGS-VTHN and Since IR=IM1+IM2=2IM1=2IM2

Substituting gives:

(5-VGS)/100k = 2*(120u/2)*10/2*(VGS-0.8)^2(1+0.01*(VGS-(VGS-VTHN)))

(5-VGS)/100k = 2*(120u/2)*10/2*(VGS-0.8)^2(1+0.01*VTHN)

(5-VGS)/100k = 2*(120u/2)*10/2*(VGS-0.8)^2(1+0.01*0.8)

(5-VGS)/100k = 604.8u*(VGS-0.8)^2

By quadratic equation: VGS = [95.768+/-(95.768^2-4*60.48*33.71)^.5] / (2*60.48)

Therefore VGS=1.055V or 0.528V (less than VTHN so this is not the correct answer)

→ VGS=1.055V

Plug Back into I equation and IR=39.3 uA

Spice simulation uses the following net list:

```
*** Homework Problem 20.1 RJHANSON ***
.control
destroy all
run

print vmeas1#branch vmeas2#branch VGS1
.endc
.option scale=1u
```

```
.op

*** My Voltages ***
VDD       VDD       0          DC        5
VMEAS1    VR        VGS1       DC        0
VMEAS2    VS1       0          DC        0

*** My Devices in the Circuit ***
R1        VDD       VR         100K
M1        VGS1      VGS1       VS1       0          NMOS L=2 W=10
M2        VGS1      VGS1       0         0          NMOS L=2 W=10

*** These are the MOSFET Models***
.MODEL NMOS NMOS LEVEL  = 3
+ TOX    = 200E-10       NSUB   = 1E17         GAMMA  = 0.5
+ PHI    = 0.7           VTO    = 0.8          DELTA  = 3.0
+ UO     = 650           ETA    = 3.0E-6       THETA  = 0.1
+ KP     = 120E-6        VMAX   = 1E5          KAPPA  = 0.3
+ RSH    = 0             NFS    = 1E12         TPG    = 1
+ XJ     = 500E-9        LD     = 100E-9
+ CGDO   = 200E-12       CGSO   = 200E-12      CGBO   = 1E-10
+ CJ     = 400E-6        PB     = 1            MJ     = 0.5
+ CJSW   = 300E-12       MJSW   = 0.5
*
.MODEL PMOS PMOS LEVEL  = 3
+ TOX    = 200E-10       NSUB   = 1E17         GAMMA  = 0.6
+ PHI    = 0.7           VTO    = -0.9         DELTA  = 0.1
+ UO     = 250           ETA    = 0            THETA  = 0.1
+ KP     = 40E-6         VMAX   = 5E4          KAPPA  = 1
+ RSH    = 0             NFS    = 1E12         TPG    = -1
+ XJ     = 500E-9        LD     = 100E-9
+ CGDO   = 200E-12       CGSO   = 200E-12      CGBO   = 1E-10
+ CJ     = 400E-6        PB     = 1            MJ     = 0.5
+ CJSW   = 300E-12       MJSW   = 0.5

.end
```

And the output IR=39.3 uA (Pretty good calculation by hand)

Now if we are to establish the same IR with 1 MOSFET it must have 2x the W to allow 2x current flow. Following is the SPICE simulation result for the same circuit as above with W/L=20/2.

IR=39.4 uA
VGS1=1.059

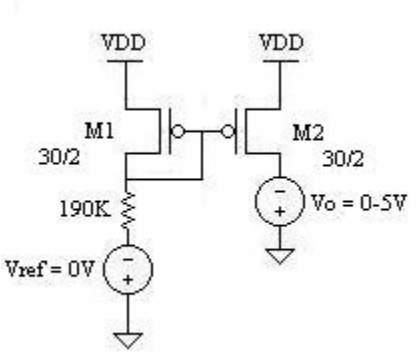
It is possible to get the equivalent IR using only 1 MOSFET, however, the circuit designer needs to be aware of what they are designing and what it is to be used for to optimize ones designs. This merely illustrates that by changing the W of an NMOS device that the same IR could be obtained after eliminating M2 from the circuit. Rjh

Problem 20.3 Russell Benson, CNS

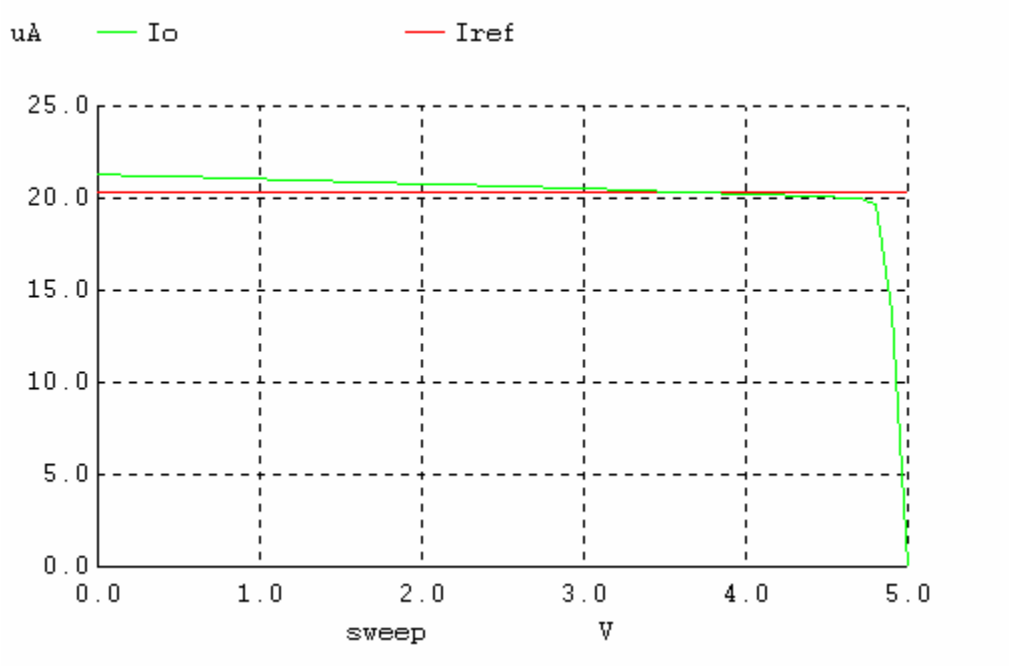
Show the SPICE simulations for the PMOS devices in Ex. 20.1.

Using Table 9.1 values, we know that for a PMOS in saturation, that Vsg = 1.15V in order to have a current of 20μA flowing. Therefore, the resistor size needed can be calculated by the following equation:

Iref = (VDD-Vsg)/R Setting Iref = 20μA and solving for R we get R ~ 190KΩ. Below is the circuit used to show the SPICE simulation.



Note Vref is a dummy voltage (0V) only needed to monitor the current through M1. Below is the SPICE simulation for the above circuit sweeping Vo from 0 to 5V.



As Vo increases, Io decreases due to the finite output resistance due to channel length modulation. Note that at 3.85V, Vsd for M2 is equal to Vsd of M1 and the two currents are equal. As Vo continues to increase the transistor moves into the triode region and begins to shut off. Below is the netlist for the above circuit.

```
*** Problem 20_3             Homework #2    Russell Benson

.control
destroy all
run

** Display Data **
let Iref = vref#branch
let Io = vo#branch

plot Iref Io
plot vsg1
.endc

.option scale=1u

** only need operating point analysis
.dc     Vo      0       5       .1

** Voltages
VDD     VDD     0       DC      5
Vo      Vo      0       DC      0
Vref    Vref    0       DC      0
** Resistors
R1      VD1      Vref    190000

** Transistors
M1      VD1     VD1     VDD     VDD     PMOS L=2 W=30
M2      VDD     VD1     Vo      VDD     PMOS L=2 W=30

.MODEL NMOS NMOS LEVEL  = 3
+ TOX    = 200E-10          NSUB   = 1E17            GAMMA  = 0.5
+ PHI    = 0.7              VTO    = 0.8             DELTA  = 3.0
+ UO     = 650              ETA    = 3.0E-6          THETA  = 0.1
+ KP     = 120E-6           VMAX   = 1E5             KAPPA  = 0.3
+ RSH    = 0                NFS    = 1E12            TPG    = 1
+ XJ     = 500E-9           LD     = 100E-9
+ CGDO   = 200E-12          CGSO   = 200E-12         CGBO   = 1E-10
+ CJ     = 400E-6           PB     = 1               MJ     = 0.5
+ CJSW   = 300E-12          MJSW   = 0.5
*
.MODEL PMOS PMOS LEVEL  = 3
+ TOX    = 200E-10          NSUB   = 1E17            GAMMA  = 0.6
+ PHI    = 0.7              VTO    = -0.9            DELTA  = 0.1
+ UO     = 250              ETA    = 0               THETA  = 0.1
+ KP     = 40E-6            VMAX   = 5E4             KAPPA  = 1
+ RSH    = 0                NFS    = 1E12            TPG    = -1
+ XJ     = 500E-9           LD     = 100E-9
+ CGDO   = 200E-12          CGSO   = 200E-12         CGBO   = 1E-10
+ CJ     = 400E-6           PB     = 1               MJ     = 0.5
+ CJSW   = 300E-12          MJSW   = 0.5

.end
```

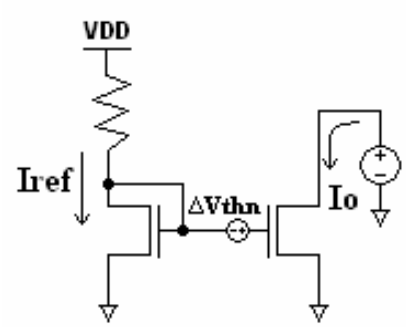
Problem 20.4)

Solution:

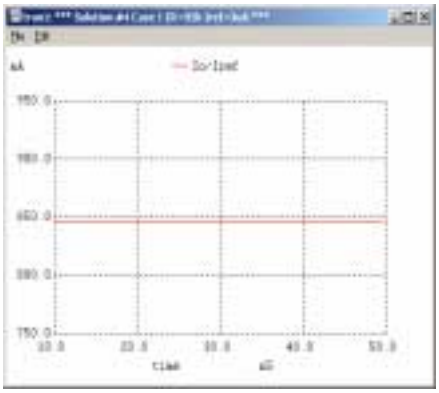
We want to show, using SPICE, that the following equation is valid:

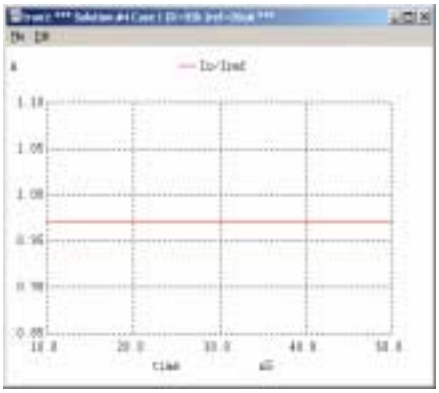
$$\frac{Io}{Iref} \approx 1 - \frac{2\Delta V_{thn}}{V_{GS} - V_{thn}}$$

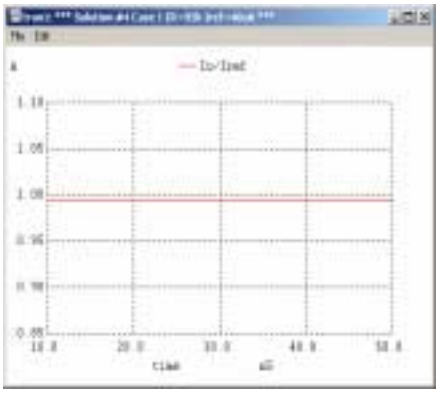
Using the following circuit we'll use three different values for V_{GS} and simulate.



VGS=	***0.9V***	***1.05V***	***1.2V***
Io/Iref= (hand calculated)	***0.8***	***0.92***	***0.95***
Io/Iref= (simulated)	***0.85***	***0.97***	***0.99***







The values obtained from the sims differ slightly from the calculated values, this is due to the higher order terms being ignored in Eq. 20.8. We can see from the sims, and Eq. 20.8, increasing VGS will minimize threshold voltage mismatches.

*** Solution #4 Case 1 (R=95k Iref=3uA ***

```
.control
destroy all
run
let Io=-VI#branch
let Iref=-VDD#branch
plot Io/Iref
plot Io Iref
.endc

VDD VDD 0 DC 5
VI  VI  0 DC 0.9
Vth VG1 VG2 10m

R1 VDD VG1 95k
*R1 VDD VG1 197.5k
*R1 VDD VG1 1.367MEG

M1 VG1 VG1 0 0 NMOS W=10u L=2u
M2 VI  VG2 0 0 NMOS W=10u L=2u


*** Control Statements ***
*.OPTION ABSTOL=1u ITL4=100 RELTOL=0.01 VNTOL=.1mv
.tran .01n 50n 10n
```

Problem 20.5

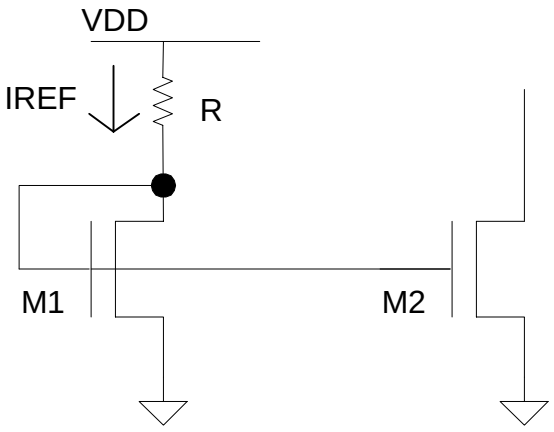
Question:

Show, using simulations and hand-calculations, that by using a larger value of $V_{DS,Sat}$ when designing bias circuit results in the MOSFETs entering the triode region earlier.

Solution:

By definition, $V_{DS,sat}$ is the V_{DS} at which the MOSFET transitions from the triode region to the saturation region of operation, when $V_{GS}>V_{THN}$. So, we would expect the MOSFET to enter the triode region earlier when designing with a higher $V_{DS,sat}$. For long-channel operation, $V_{DS,sat} = V_{GS}-V_{THN}$.

Using the following circuit, it can be shown that using a larger $V_{DS,sat}$ in the design will cause the MOSFETs to enter the triode region earlier.



For long channel operation in saturation, neglecting channel-length modulation,

$$I_{REF} = KP_N \cdot \frac{W}{2L}(V_{GS} - V_{THN})^2 = KP_N \cdot \frac{W}{2L}(V_{DS,sat})^2$$

Solving for W yields,

$$W = \frac{2 \cdot I_{REF} \cdot L}{KP_N \cdot (V_{DS,sat})^2}$$

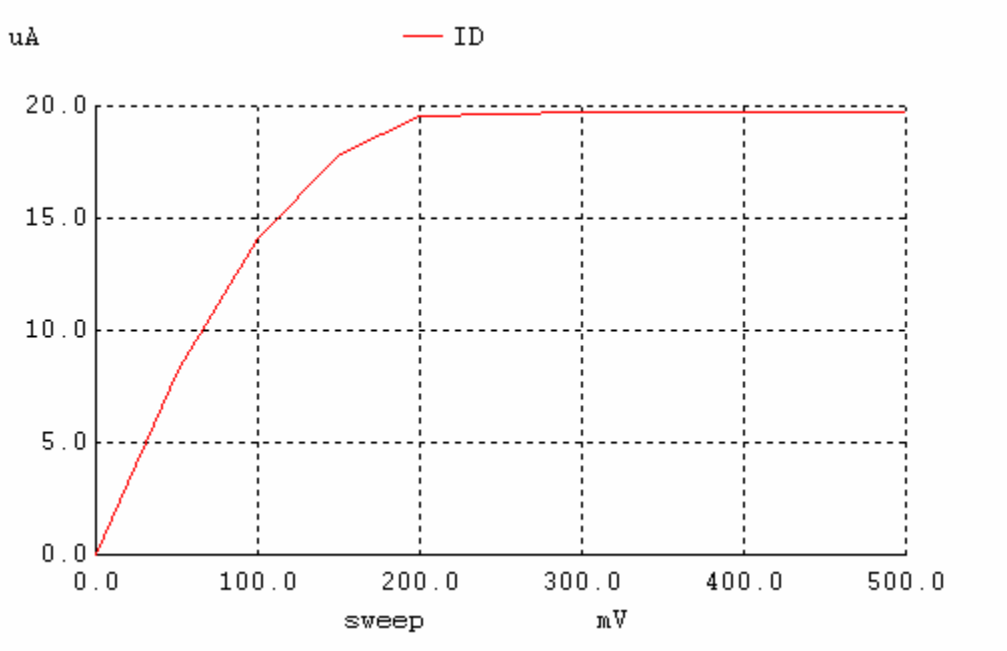
For the first design, we will use a $V_{DS,sat}$=0.25V.

Solving for W using values of I_{REF}=20uA, L=2um, KP_N=120uA/V^2, and $V_{DS,sat}$=0.25V, results in W=11um.

Also, we need to find the value of the resistor that will work with this circuit.

$$R = \frac{V_{DD} - V_{GS}}{I_{REF}} = \frac{5 - 1.05}{20uA} = 197.5k\Omega$$

Using the values of W=11um and R=197.5k yields the following SPICE results. In this design, the M2 enters the triode region around V_{DS}=200mV.



Plot for design using $V_{DS,sat}$ = 0.25V

For the second design, we will use a $V_{DS,sat}$=0.15V.

Remember,

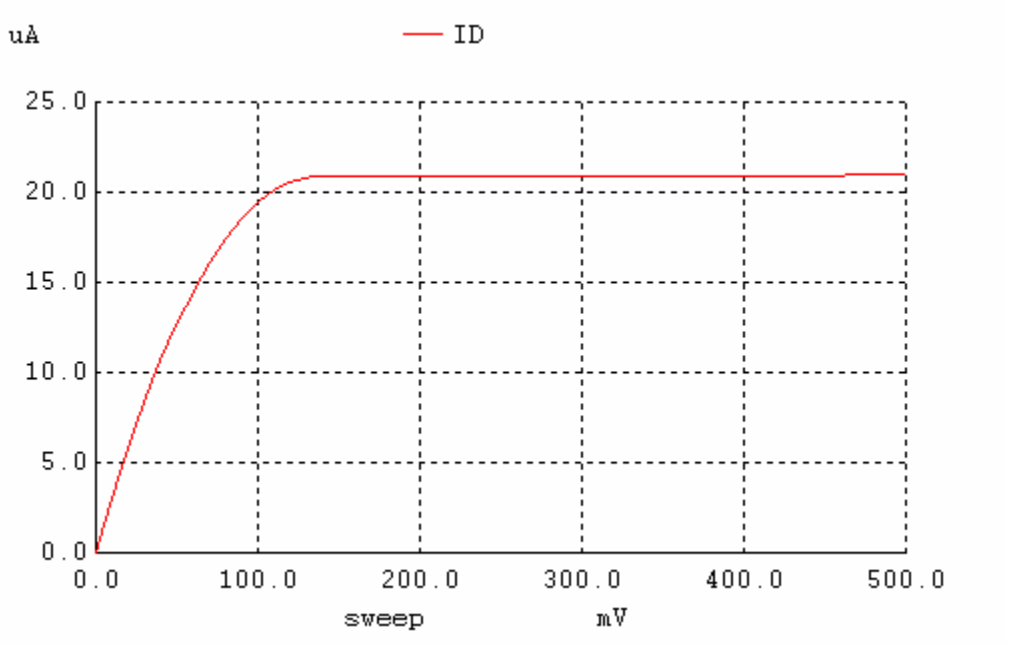
$$W = \frac{2 \cdot I_{REF} \cdot L}{KP_N \cdot (V_{DS,sat})^2}$$

Solving for W using values of I_{REF}=20uA, L=2um, KP_N=120uA/V^2, and $V_{DS,sat}$=0.25V, results in W=30um.

Also, we need to find the value of the resistor that will work with this circuit.

$$R = \frac{V_{DD} - V_{GS}}{I_{REF}} = \frac{5 - 0.95}{20uA} = 192.5k\Omega$$

Using the values of W=30um and R=192.5k yields the following SPICE results. For this design, M2 enters the triode region around 120mV. Therefore, designing with a higher $V_{DS,sat}$ results in the MOSFET entering the triode region earlier.



Plot for design using $V_{DS,sat}$ = 0.15V

SPICE netlists are shown on the following pages.

```
*            EE511 Problem 20.5a

.control
destroy all
run
let ID=-Vd2#branch
plot ID
.endc


.options scale=1u
.DC         Vd2         0           0.5         0.05

Vdd         Vdd         0           DC          5
Vd2         Vd2         0           DC          0

M1          Vg1         Vg1         0           0           nmos        W=11 L=2
M2          Vd2         Vg1         0           0           nmos        W=11 L=2
R1          Vdd         Vg1         197.5k



.MODEL NMOS NMOS LEVEL  = 3
+ TOX    = 200E-10        NSUB   = 1E17          GAMMA  = 0.5
+ PHI    = 0.7            VTO    = 0.8           DELTA  = 3.0
+ UO     = 650            ETA    = 3.0E-6        THETA  = 0.1
+ KP     = 120E-6         VMAX   = 1E5           KAPPA  = 0.3
+ RSH    = 0              NFS    = 1E12          TPG    = 1
+ XJ     = 500E-9         LD     = 100E-9
+ CGDO   = 200E-12        CGSO   = 200E-12        CGBO   = 1E-10
+ CJ     = 400E-6         PB     = 1             MJ     = 0.5
+ CJSW   = 300E-12        MJSW   = 0.5
*
.MODEL PMOS PMOS LEVEL  = 3
+ TOX    = 200E-10        NSUB   = 1E17          GAMMA  = 0.6
+ PHI    = 0.7            VTO    = -0.9          DELTA  = 0.1
+ UO     = 250            ETA    = 0             THETA  = 0.1
+ KP     = 40E-6          VMAX   = 5E4           KAPPA  = 1
+ RSH    = 0              NFS    = 1E12          TPG    = -1
+ XJ     = 500E-9         LD     = 100E-9
+ CGDO   = 200E-12        CGSO   = 200E-12        CGBO   = 1E-10
+ CJ     = 400E-6         PB     = 1             MJ     = 0.5
+ CJSW   = 300E-12        MJSW   = 0.5

.end
```

```
*            EE511 Problem 20.5b


.control
destroy all
run
let ID=-Vd2#branch
plot ID
.endc
```

```
.options scale=1u
.DC        Vd2        0          0.5        0.005

Vdd        Vdd        0          DC         5
Vd2        Vd2        0          DC         0

M1         Vg1        Vg1        0          0          nmos       W=30 L=2
M2         Vd2        Vg1        0          0          nmos       W=30 L=2
R1         Vdd        Vg1        192.5k



.MODEL NMOS NMOS LEVEL  = 3
+ TOX    = 200E-10        NSUB   = 1E17          GAMMA  = 0.5
+ PHI    = 0.7            VTO    = 0.8           DELTA  = 3.0
+ UO     = 650            ETA    = 3.0E-6        THETA  = 0.1
+ KP     = 120E-6         VMAX   = 1E5           KAPPA  = 0.3
+ RSH    = 0              NFS    = 1E12          TPG    = 1
+ XJ     = 500E-9         LD     = 100E-9
+ CGDO   = 200E-12        CGSO   = 200E-12        CGBO   = 1E-10
+ CJ     = 400E-6         PB     = 1             MJ     = 0.5
+ CJSW   = 300E-12        MJSW   = 0.5
*
.MODEL PMOS PMOS LEVEL  = 3
+ TOX    = 200E-10        NSUB   = 1E17          GAMMA  = 0.6
+ PHI    = 0.7            VTO    = -0.9          DELTA  = 0.1
+ UO     = 250            ETA    = 0             THETA  = 0.1
+ KP     = 40E-6          VMAX   = 5E4           KAPPA  = 1
+ RSH    = 0              NFS    = 1E12          TPG    = -1
+ XJ     = 500E-9         LD     = 100E-9
+ CGDO   = 200E-12        CGSO   = 200E-12        CGBO   = 1E-10
+ CJ     = 400E-6         PB     = 1             MJ     = 0.5
+ CJSW   = 300E-12        MJSW   = 0.5

.end
```

Problem 20.6:

In Ex. 20.2 how does the gate voltage of M1/M2 change as V_{DD} is decreased? How does the V_{SG} change? Use SPICE to verify your answers.

Solution:

The following graph shows the I_o variation vs. V_{DD} for the circuit if Fig 20.11. It behaves as expected because once V_{DD} is large enough to supply a decent gate overdrive voltage V_{ovn} and force both M1 and M2 to operate in the saturation region.

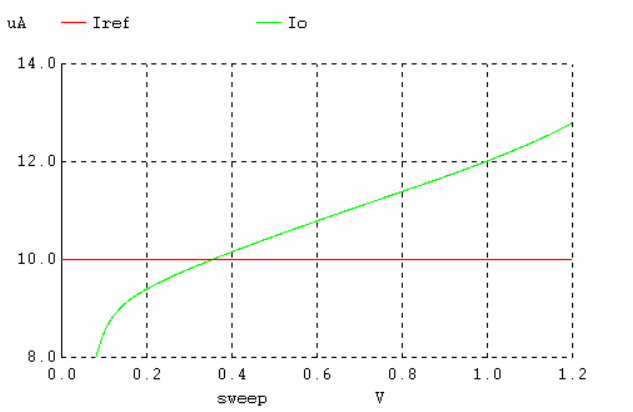


Figure 1. I_o and I_{ref} vs. V_{DD}

Since the I_{REF} current source is forcing M1 to provide a constant V_{SG} across M1 and M2, we would expect that V_{SG} would not change across V_{DD}. Figure 2 plots the gate voltage of M1 and M2 (V_{D1}) vs. V_{DD}. Notice that at any given point on the graph that $V_{DD} - V_{D1} = 350mV$. It is also apparent from the figure that VD1 (gate voltage of M1 and M2) linearly increases with V_{DD}.

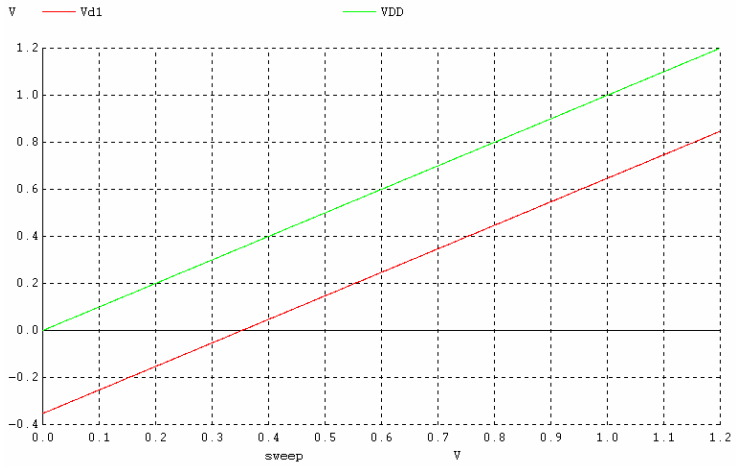


Figure 2. V_{D1} vs. V_{DD}

Netlist:

*** Problem 20.6 CMOS: Circuit Design, Layout, and Simulation ***

```
.control
destroy all
run
let Iref=Vmeas#branch
let Io=Vo#branch
plot Iref Io ylimit 8u 14u
plot Vd1 VDD
.endc

.option scale=50n
.dc VDD 0.0 1.2 1m


VDD     VDD     0       DC      1
Vo      Vo      0       DC      0
Vmeas   Vmeas   0       DC      0

Iref    VD1     Vmeas   DC      10u
M1      VD1     VD1     VDD     VDD     PMOS L=2 W=100
M2      Vo      VD1     VDD     VDD     PMOS L=2 W=100


* BSIM4 models
.model  pmos  pmos  level = 14
.end
```

Problem 20.7

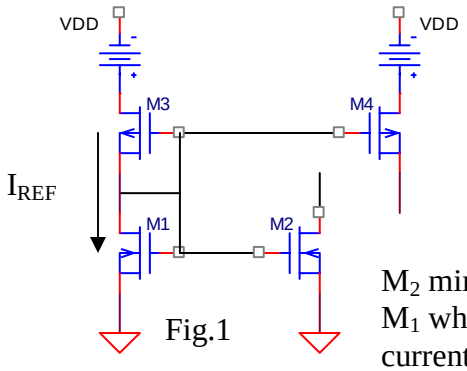


Fig.1

M_2 mirrors the current in M_1 while M_4 mirrors the current in M_3

Assuming the long channel behavior we have

$$VDD = V_{SG3} + V_{GS1}$$

$$VDD = \sqrt{\frac{2.I_{REF}}{KP_P \frac{w_3}{l_3}}} + V_{THP} + \sqrt{\frac{2.I_{REF}}{KP_N \frac{w_1}{l_1}}} + V_{THN}$$

Thinking M_3 as a resistor in fig.1 to mirror the current in M_1 we solve for the size of M_3.

If minimum lengths MOSFETs are used we have L= 1µm and substituting the values from table 9.1 we get

$$5 = \sqrt{\frac{2.20}{40.\frac{w_3}{l_3}}} + 0.9 + \sqrt{\frac{2.20}{120.\frac{10}{1}}} + 0.8$$

$$\frac{w_3}{l_3} \approx 0.1 \quad => \quad \frac{w_3}{l_3} \approx \frac{10}{100}$$

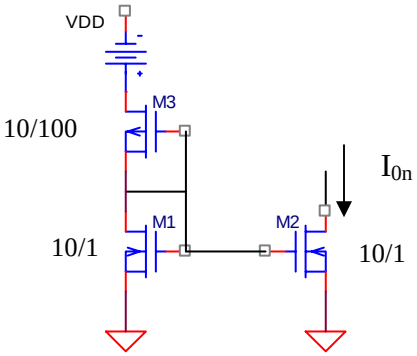


Fig.2 thinking M_3 (PMOS) as resistor

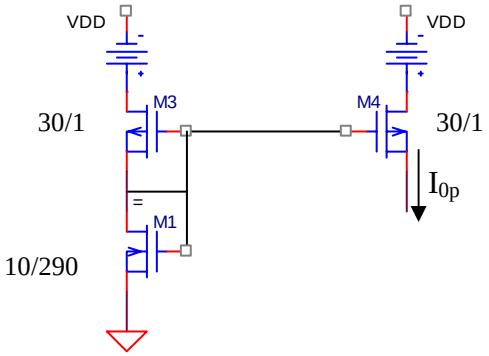


Fig.3 thinking M_1 (NMOS) as resistor

Thinking M_1 as a resistor in fig.1 to mirror the current in M_3 we solve for the size of M_1 (L= 1μm)

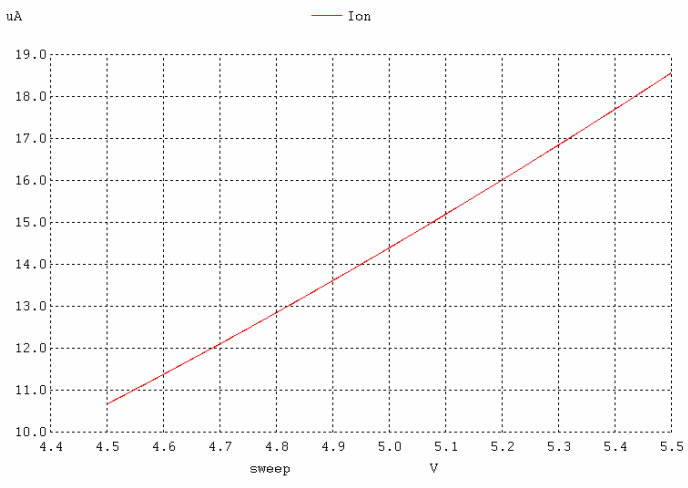
$$5 = \sqrt{\frac{2.20}{40.\frac{30}{1}}} + 0.9 + \sqrt{\frac{2.20}{120.\frac{w_1}{l_1}}} + 0.8$$

$$\frac{w_1}{l_1} \approx 0.0342 \quad => \quad \frac{w_1}{l_1} \approx \frac{10}{290}$$

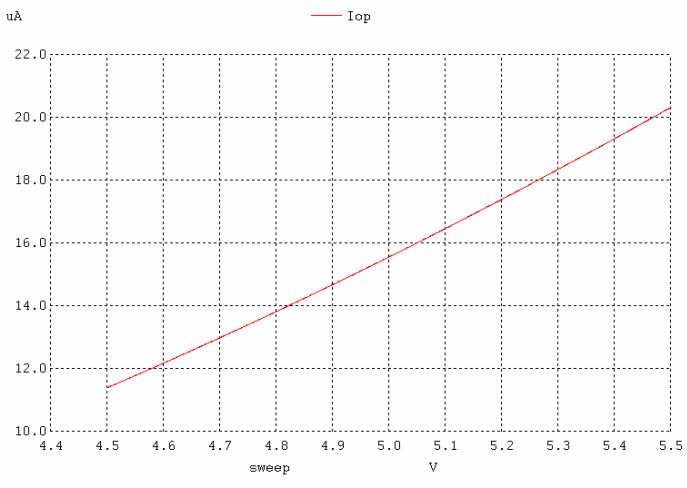
SIMULATIONS

SOURCE CODE

```
.control
destroy all
run
let Iop=Vop#branch
let Ion=Von#branch
plot Iop
plot Ion
.endc

.option scale=1u
.dc VDD 4.5 5.5 1m

VDD   VDD   0      DC    5
Vop   Vop   0      DC    0
Von   VDD   Von    DC    0

M1n   Vbiasn Vbiasn 0     0     NMOS L=1 W=10
M2n   Vbiasn Vbiasn VDD   VDD   PMOS L=100 W=10


M1p   Vbiasp Vbiasp 0     0     NMOS L=290 W=10
M2p   Vbiasp Vbiasp VDD   VDD   PMOS L=1 W=30

Mn    Von    Vbiasn 0     0     NMOS L=1 W=10

Mp    Vop    Vbiasp VDD   VDD   PMOS L=1 W=30
```



Thinking M_3 (PMOS) as resistor



Thinking M_1 (NMOS) as resistor

Problem 20.8

The main portion of the circuit that could cause this anomaly is the '*Start Up Circuit*'. There are two possible stable conditions in which the voltage reference beta multiplier might be operating…

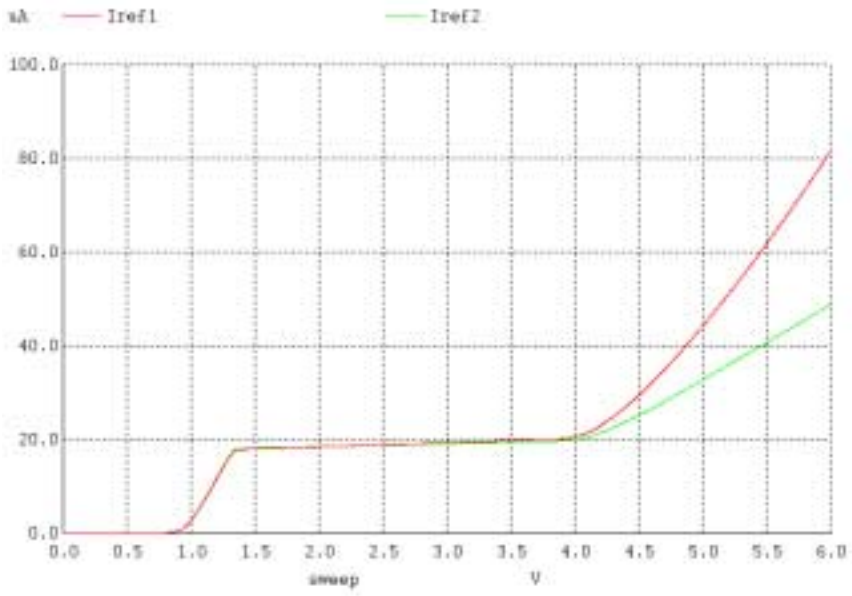
(1) The normal stable condition for which the circuit was designed.

(2) When the gates of M3/M4 are at Vdd and the gates of M1/M2 are at 0(zero).

Refer to figure 20.14 for circuit.

When the gates of M3/M4 are at V_{DD} and the gates of M1/M2 are at 0(zero). When in this state the gate of MSU1 is at ground and so it is off. The gate of MSU2 would be somewhere around Vthp (because long L Pmos would have large drop across it) which would turn on MSU3. The function of MSU3 is to discharge the voltage on the gates of M3/M4 to the gates of M1/M2.Thus the circuit comes back to the desired operating point for which it was designed. In other words it can be said that the voltage at the PMOS gates leaks through the resistor (MSU3) to charge the capacitors at the gates of M1/M2. Thus the gate terminal of M1 increases and turns on the Mosfet MSU1, which would pull gate of MSU3 to ground and turn it off. But when the length of MSU2 is decreased there would a large voltage at the gate of MSU3, which MSU1 can't pull it to ground in order to turn it off because of which MSU3 would be always on and I_{ref} would be increasing with V_{DD}.

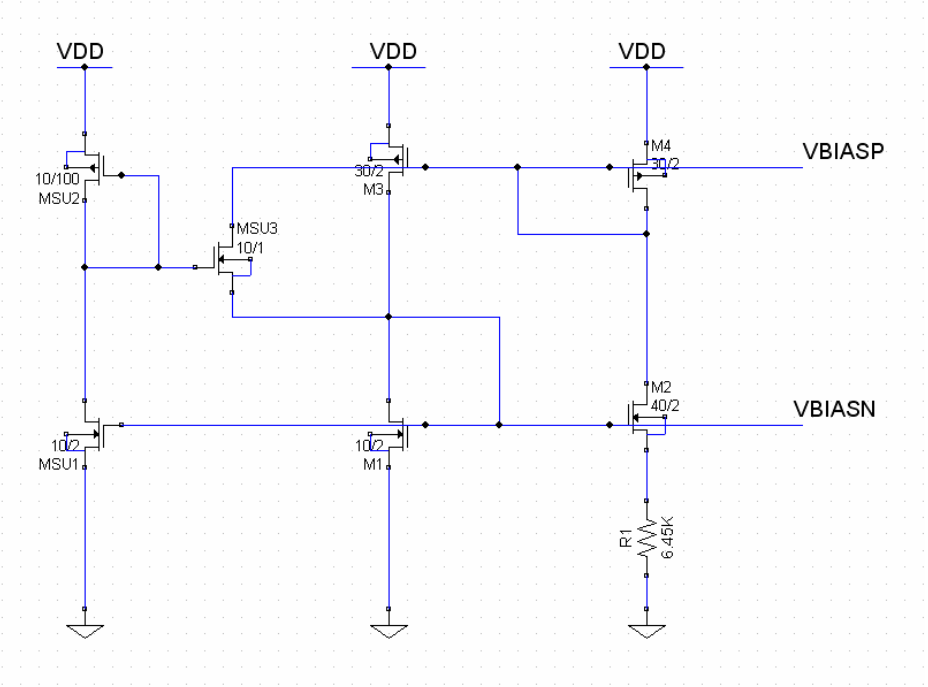
<u>Simulation Results obtained when MSU2 length is decreased to 10um.</u>



```
.control
destroy all
run
let Iref1=Vmeas1#branch
let Iref2=Vmeas2#branch
plot Iref1 Iref2
.endc
.option scale=1u
.dc VDD 0 6 1m

VDD       VDD     0       DC      5
Vop       Vop     0       DC      0
Von       VDD     Von     DC      0
Vmeas1    Vmeas1          0       DC      0
Vmeas2    Vmeas2          0       DC      0

M1 Vbiasn Vbiasn Vmeas1         0       NMOS L=2 W=10
M2 Vbiasp Vbiasn Vr     0       NMOS L=2 W=40
M3 Vbiasn Vbiasp VDD    VDD     PMOS L=2 W=30
M4 Vbiasp Vbiasp VDD    VDD     PMOS L=2 W=30

Rbias     Vr      vmeas2        6.5k

MSU1      Vsur    Vbiasn  0       0       NMOS L=2   W=10
MSU2      Vsur    Vsur    VDD     VDD     PMOS L=10 W=10
MSU3      Vbiasp  Vsur    Vbiasn  0       NMOS L=1   W=10
```

PROBLEM 20.9

To estimate the value of voltage across resistor in the circuit below by hand calculations.



Lets first estimate the value of resistor for a bias current of 20µA.
Since the resistor is connected to source, we can see from the circuit that the gate to source voltage of M1 is the sum of voltage drop across the resistor *R1* and gate to source voltage of M2.

$$\text{i.e.} \qquad V_{GS1} = V_{GS2} + I_{REF} \,.\, R_1 \quad \text{--------(1)}$$

For long channel we can write V_{GS} to be

$$V_{GS} = \sqrt{\frac{2.I_D L}{KP_n W}} + V_{THN}$$

The MOSFET M2 is scaled such that the excess voltage is dropped across the resistor R_1, i.e $W_2 = K.W_1$. Since width of M2 is increased it requires less VGS to conduct the same I_{REF}, and excess voltage drop occurs across the resistor R_1 .

Therefore eq(1) can be written as

$$\sqrt{\frac{2.I_{REF} L_1}{KP_n W_1}} + V_{THN} = \sqrt{\frac{2.I_{REF} L_2}{KP_n .K.W_2}} + V_{THN} + .I_{REF} .R_1$$

Solving for I_{REF} we get

$$I_{REF} = \frac{2}{R^2 KP_n \dfrac{W_1}{L_1}} \left(1 - \frac{1}{\sqrt{K}}\right)^2$$

Solving for R1, we can rewrite the above equation as

$$R_1 = \sqrt{\frac{2}{I_{REF} KP_n \frac{W_1}{L_1}}}\left(1 - \frac{1}{\sqrt{K}}\right)$$

If we bias the transistor M1 with a reference current of 20µA and Choosing K=4 i.e. W2= 4.W1 and solving our circuit for R1 by substituting the values of KP_n, W_1, L_1 we get

$$R_1 = \sqrt{\frac{2}{20\mu A.120\frac{\mu A}{V^2}\frac{10}{2}}}\left(1 - \frac{1}{\sqrt{4}}\right) = 6.45K\Omega$$

Having determined the value of resistor then the voltage drop across it is given by $I_{REF}\ X\ R_1$

$$20\mu A\ .\ 6.45K\Omega = 0.129V$$

From simulations :

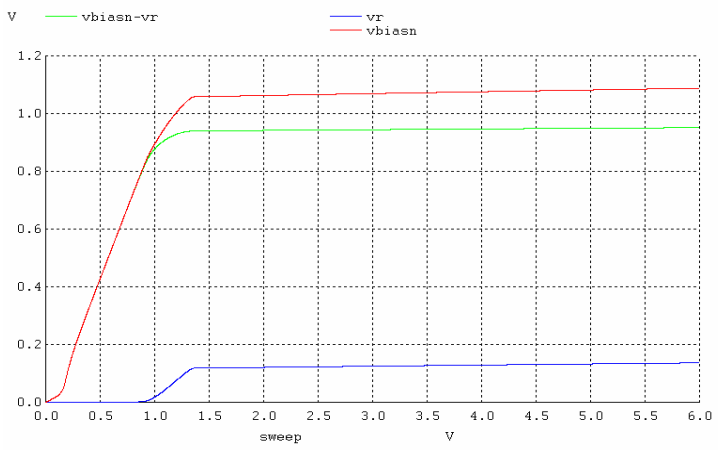
Voltage drop across the resistor = $0.1279V$

Voltage drop across the gate and source of M2 = 0.945 V

Voltage drop across the gate and source of M1 = 1.070 V

$$\therefore \quad V_{GS1} = V_{GS2} + I_{REF}\ .\ R_1$$

$$1.07 = 0.945 + 0.1279$$



NOTE:

For a particular value of K = 4 we can also call this β multiplier circuit as constant g_m bias circuit because the value of R then becomes

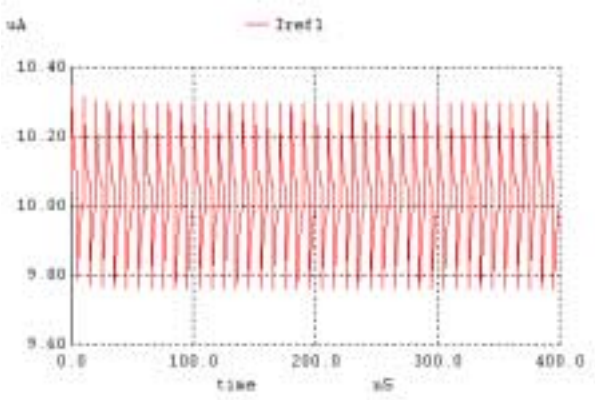
$$R = \sqrt{\frac{2}{I_{REF} KP_n \frac{W_1}{L_1}}}\left(1 - \frac{1}{\sqrt{4}}\right) = \sqrt{\frac{1}{2.I_{REF} KP_n \frac{W_1}{L_1}}} = \frac{1}{g_m}$$

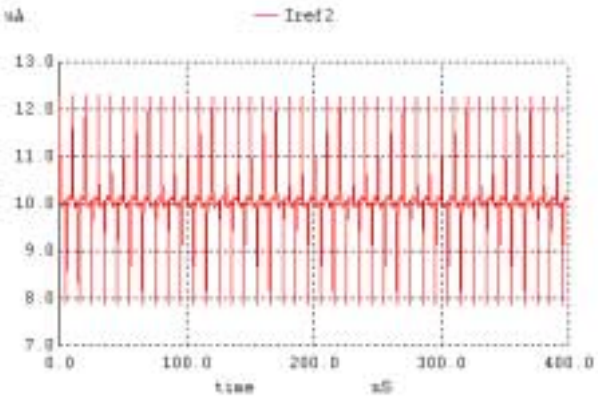
Problem 10)

The reference circuit in Fig. 20.22 provides improved current reference for short channel devices. To see the stability of this circuit with changes in VDD, we couple a 50mv square wave signal at 100 MHz to VDD. So we have a square wave VDD oscillating between 1 and 1.05v at 100MHz.

Net list

```
*prob20.10*
.control
destroy all
run
let Iref1=Vmeas1#branch
let Iref2=Vmeas2#branch
plot Iref1
plot Iref2
.endc
.option scale=50n
.tran .1n 400n

VDD    VDD    0       DC      1  pulse 1 1.05 0 0 0 5n 10n
Vop    Vop    0       DC      0
Von    VDD    Von     DC      0
Vmeas1         Vmeas1          0       DC      0
Vmeas2         Vmeas2          0       DC      0

M1     Vbiasn Vbiasn  Vmeas1          0       NMOS L=2 W=50
M2     Vreg   Vreg    Vr              0       NMOS L=2 W=200
M3     Vbiasn Vbiasp  VDD             VDD     PMOS L=2 W=100
M4     Vreg   Vbiasp  VDD             VDD     PMOS L=2 W=100
Rbias  Vr     vmeas2  5.5k

*amplifier
MA1    Vamp   Vreg    0       0       NMOS L=2    W=50
MA2    Vbiasp Vbiasn  0       0       NMOS L=2    W=50
MA3    Vamp   Vamp    VDD     VDD     PMOS L=2    W=100
MA4    Vbiasp Vamp    VDD     VDD     PMOS L=2    W=100
Mcp    VDD    Vbiasp  VDD     VDD     PMOS L=100 W=100
Mcn    0      Vbiasn  0       0       NMOS L=100 W=100

*start-up stuff
MSU1   Vsur   Vbiasn  0       0       NMOS L=2   W=50
MSU2   Vsur   Vsur    VDD     VDD     PMOS L=20  W=10
MSU3   Vbiasp Vsur    Vbiasn  0       NMOS L=1   W=10

* BSIM4 models
.model  nmos  nmos  level = 14
----------------
.model  pmos  pmos  level = 14
----------------
.end
```

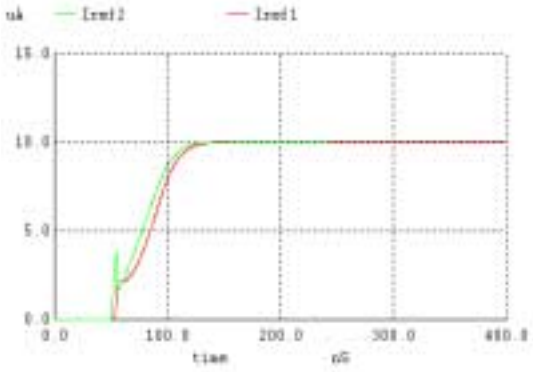


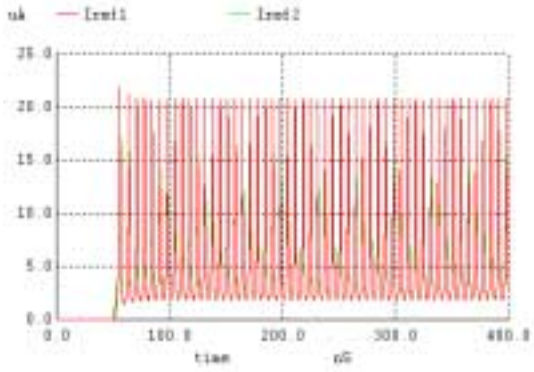


We can observe the effects of high-frequency noise causing huge variations in Iref1 and Iref2. So the reference circuit is very unstable with changes is VDD.

Effect of size of MCP and MCN

To see the effect of size of MCP and MCN, lets reduce both sizes from 100/100 to 100/2. We can clearly see that reducing the size of MCP and MCN makes the circuit unstable.





Size – 100/100

Size – 100/2

20.11

If we assume, as we did in Example 20.4,
that dVSG/dT is approximately equal
to dVTHP/dT, the answer is
basically - 0.6 mV per degree C.

No lengthy derivations are needed.

Problem 20.12
I used the beta-multiplier in Fig 20.22 (Pg 20.17) except I changed the value of the resistor to 1.67K which I calculated by substituting values used in Table 9.2 in Equation 20.38((Pg 20.22)

The equation is as follows:

$$R = \frac{2}{(-.6E-3*120E-6*50/2)}[1-\frac{1}{2}][2E-3+(\frac{-1.5}{300})]$$

R=1.67K which I used in my simulations for Fig 20.22

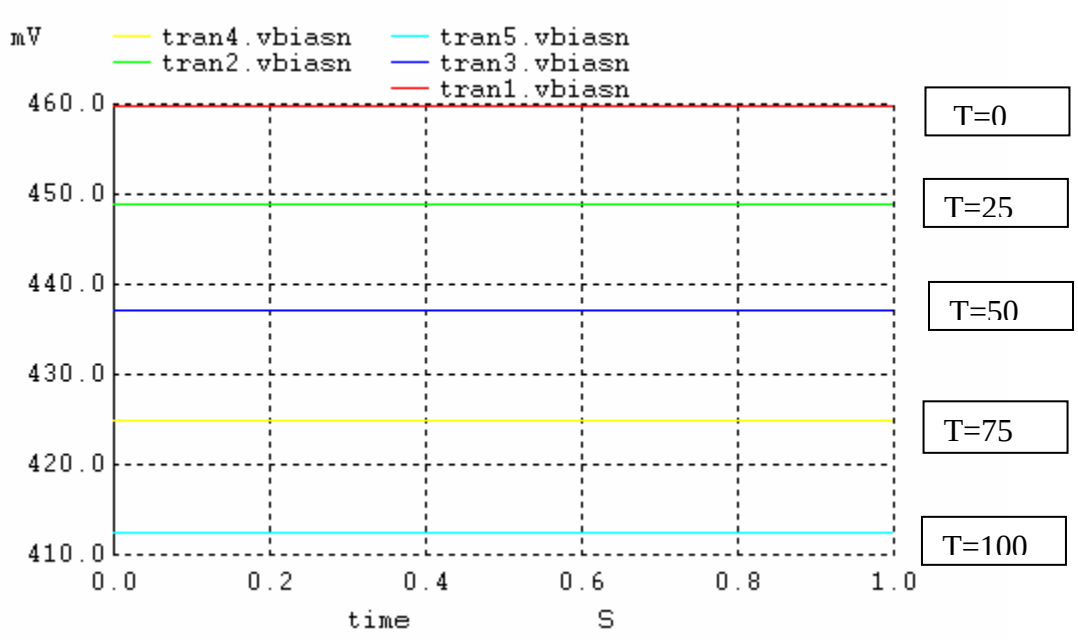
SPICE STATEMENTS

```
*** Problem 20.12 CMOS: Circuit Design, Layout, and Simulation ***

.control
destroy all
set temp=0
run
set temp=25
run
set temp=50
run
set temp=75
run
set temp=100
run
plot tran1.vbiasn tran2.vbiasn tran3.vbiasn tran4.vbiasn tran5.vbiasn
.endc

.option scale=50n
.tran 1m 1

VDD   VDD   0       DC    1
*Vop  Vop   0       DC    0
*Von  VDD   Von     DC    0
Vmeas1        Vmeas1        0       DC    0
Vmeas2        Vmeas2        0       DC    0

M1    Vbiasn Vbiasn Vmeas1        0       NMOS L=2 W=50
M2    Vreg   Vreg   Vr     0     NMOS L=2 W=200
M3    Vbiasn Vbiasp VDD    VDD   PMOS L=2 W=100
M4    Vreg   Vbiasp VDD    VDD   PMOS L=2 W=100

Rbias Vr      vmeas2        1.67k RMOD
```

.model RMOD R TC1=0.002

*amplifier
MA1 Vamp Vreg 0 0 NMOS L=2 W=50
MA2 Vbiasp Vbiasn 0 0 NMOS L=2 W=50
MA3 Vamp Vamp VDD VDD PMOS L=2 W=100
MA4 Vbiasp Vamp VDD VDD PMOS L=2 W=100

*start-up stuff
MSU1 Vsur Vbiasn 0 0 NMOS L=2 W=50
MSU2 Vsur Vsur VDD VDD PMOS L=20 W=10
MSU3 Vbiasp Vsur Vbiasn 0 NMOS L=1 W=10



The variation is around -50mV/100C or 500uV/C
Because we do not consider the effect of velocity saturation at lower temperatures the long channel equations can be used for the calculations.

Problem Solution for 20.13 :

Including threshold offset voltage in equation 20.42 we have:

Vgs1=n Vt ln[(Iref L1)/(Ido W1)] + Vthn + ΔVthn and

Vgs2=n Vt ln[(Iref L1)/(Ido K W1)] + Vthn

Now Iref=(Vgs1-Vgs2)/R

Iref = [n Vt ln(K) + ΔVthn] / R

Using value for K= 4 and n = 1 and we obtain

Iref = (1/R) (35mV + ΔVthn)

If we want to tolerate 30% of current change it means we can tolerate ΔVthn = 10.5 mV change in threshold voltage. Figure 1 shows simulation results for beta multiplier (Iref=10 nA) including threshold voltage mismatch. From the figure we can see that at 30% tolerance of current (13 nA) we have a threshold voltage mismatch at about 10 mV.

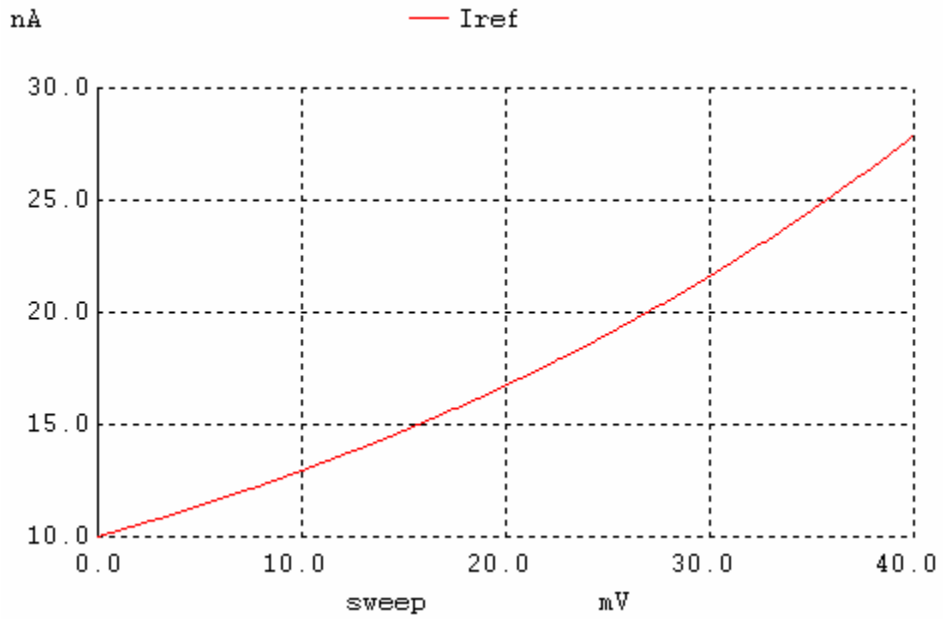


Figure 1: WinSpice simulation results for Beta multiplier with threshold voltage mismatch form 0 to 40 mV.

Problem 20.14)

Before applying a test voltage, we can estimate the output resistance by plotting the DC current versus the voltage. From this plot, the output resistance is the inverse of the slope of I_D. Using spice to plot r_o ($r_o = 1/\text{deriv}(I_D)$) we find that r_o is approximately 164k ohms. These two plots are seen below in figures 1 & 2.

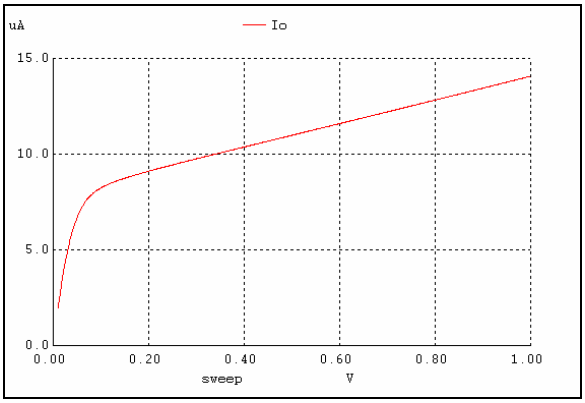


Figure 1: I_o vs V_o.

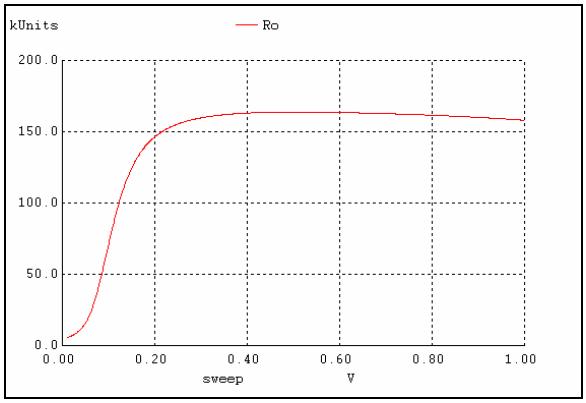


Figure 2: r_o vs V_o.

Next we apply the AC test voltage. In this case $r_o = \frac{v_T}{i_T}$. Using spice, the output resistance is about 158k ohms as seen in figure 3 below. (The AC test voltage must be placed in series with the DC voltage source.)

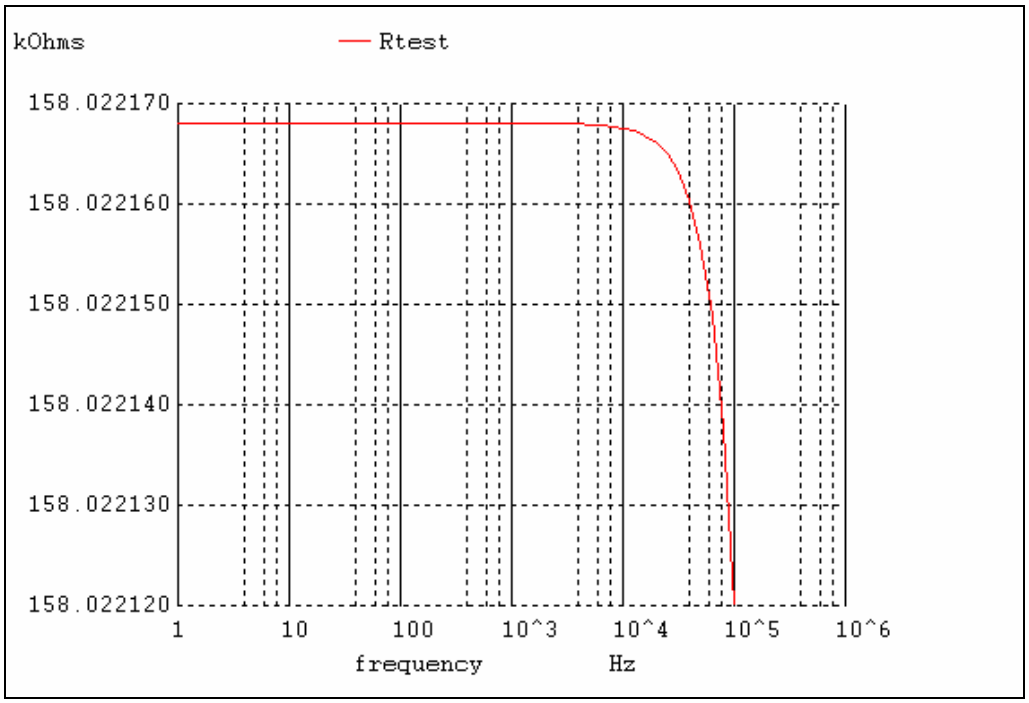


Figure 3: r_o as a function of v_T/i_T (ac).

```
*** Problem 20.14 ***

.control
destroy all
run
let Itest = abs(Vtest#branch)
plot Itest
let Rtest = (Vtest/Itest)
plot Rtest
.endc

.option scale=50n
.ac      DEC   10      1       100K

VDD   VDD   0       DC      1
Vo    Vo    Vtest   DC      1       AC      0
Vtest Vtest 0       DC      0       AC      10m

X1    VDD   Vbiasp        Vbiasn        bmrefs
M1    Vo    Vbiasn        0             0       NMOS L=2 W=50

.subckt bmrefs        VDD   Vbiasp        Vbiasn
M1    Vbiasn Vbiasn 0       0       NMOS L=2 W=50
M2    Vreg   Vreg   Vr      0       NMOS L=2 W=200
M3    Vbiasn Vbiasp VDD     VDD     PMOS L=2 W=100
M4    Vreg   Vbiasp VDD     VDD     PMOS L=2 W=100

Rbias Vr      0       5.5k

*amplifier
MA1   Vamp  Vreg   0       0       NMOS L=2 W=50
MA2   Vbiasp Vbiasn 0       0       NMOS L=2 W=50
MA3   Vamp  Vamp   VDD     VDD     PMOS L=2 W=100
MA4   Vbiasp Vamp  VDD     VDD     PMOS L=2 W=100

*start-up stuff
MSU1 Vsur   Vbiasn 0       0       NMOS L=2   W=50
MSU2 Vsur   Vsur   VDD     VDD     PMOS L=20  W=10
MSU3 Vbiasp Vsur   Vbiasn  0       NMOS L=1   W=10
.ends
```

Figure 4: Netlist used when applying a test voltage to find r_o.

20.15. Find the voltages on the drain, gate, and source terminals of M1 – M4 in Figure 20.29 using the data in Table 9.1.

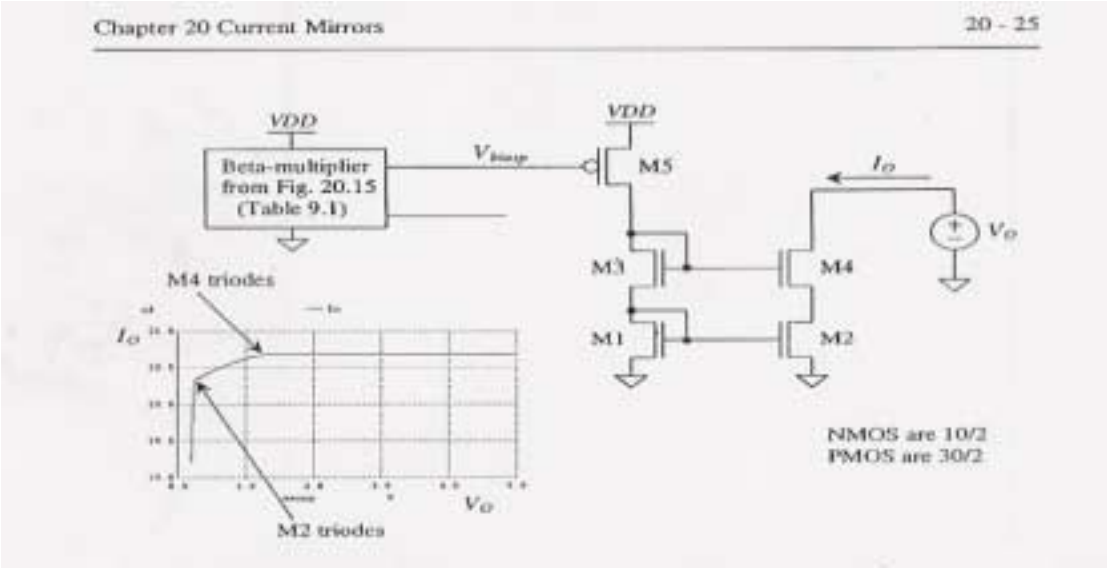


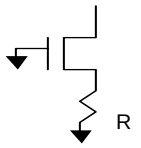
Figure 20.29

Vbiasp is at VDD – 1.15V which sets the VSG of M5 at 1.15V and ID for M5 at 20uA since it is a 30/2 PMOS (Table 9.1). Since both M1 and M2 are connected in a diode configuration with 20uA of current, their VGS voltages will be 1.05V. This sets the gate voltage for M1 and M2 at 1.05V and the gate voltage of M3 and M4 and the drain voltages of M5 and M3 at 2.1V. The drain voltage of M2 and the source voltage of M4 will be 1.05V or a VGS voltage (1.05V) below the gate voltage of M4. To keep M4 operating in the saturation region, the VDS for M4 must be greater than or equal to a VDSSAT voltage (0.25V). The drain of M4 will be greater than or equal to 1.3V and the IV plot for this node is shown in the graph in Figure 20.29.

Simulation results had Vbiasp at 3.85V, gate voltage of M1 and M2 at 1.08V, and the gate voltage of M3 and M4 at 2.4V. The VGS of M3 and M4 are slightly higher than the table values due to the body effect because the bulk is more negatively biased than the source. The drain of M2 is at 1.08V and the IV plot for the drain of M4 is shown in Figure 20.29. The drain of M4 must be greater than or equal to 1.29V to remain in saturation.

20.16)

If the MOSFET below is operating in the saturation region determine the small-signal resistance looking into its drain



Apply a test voltage v_t to the drain of the MOSFET then calculate the current (i_t) in the MOSFET. Then solve for $v_{t/}$ $i_{t:}$

$$i_t = V_{GS} gm + \frac{V_t + V_{GS}}{r_o}$$

$$V_{GS} = -i_t R$$

$$i_t = -i_t R \cdot gm + \frac{V_t - i_t R}{r_o}$$

$$i_t - \frac{V_t}{r_o} = -i_t R \cdot gm - \frac{i_t R}{r_o}$$

$$-\frac{V_t}{i_t} = -R \cdot gm \cdot r_o - R - r_o$$

$$\frac{V_t}{i_t} = +R \cdot gm \cdot r_o + R + r_o$$

$$R_o = \frac{V_t}{i_t} = r_o(1 + gmR) + R \approx r_o(1 + gmR)$$

20.17) To calculate the size of the MWS transistor when the transistor M3 enters the triode region using long channel values in figure 20.38.

We know the *Id3* =20uA, and the *Vd3=Vgs*, so when the transistor is in triode we have

$$Id3= KPn*(W/L)*[(Vgs-Vthn)Vds-((Vds^2)/2)]$$

We know all the values except for *Vgs*, so solving the above equation by substituting values from Table 9.1, we get

$$Vgs= 1.6V$$

Now using this value of *Vgs* we find the size of MWS transistor

$$Wmws/Lmws= 1/5 \text{ (approx.)}$$

So we take a value of **10/10 or 10/9 for the W/L for the MWS transistor.**

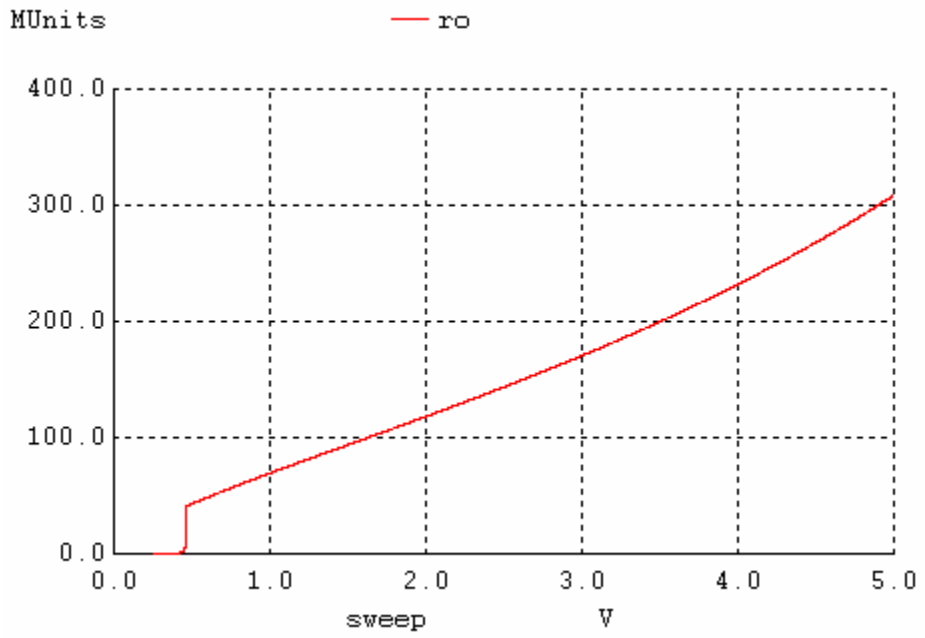
On the sim, I calculated the value of the o/p resistance for w=7 and w=10 to show how this affects the o/p resistance.

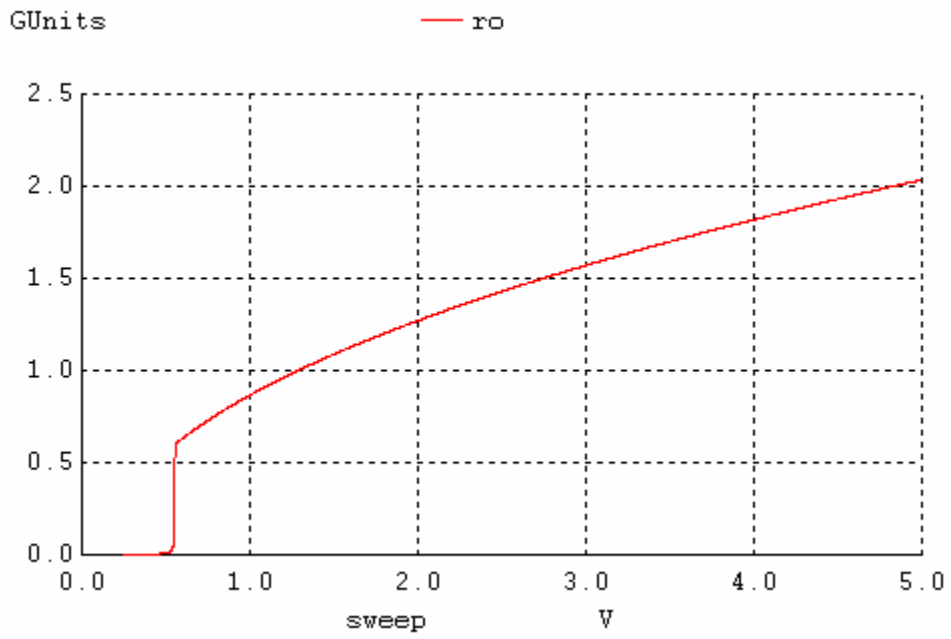
Netlist

*** Hw 20.17_a CMOS: Circuit Design, Layout, and Simulation ***

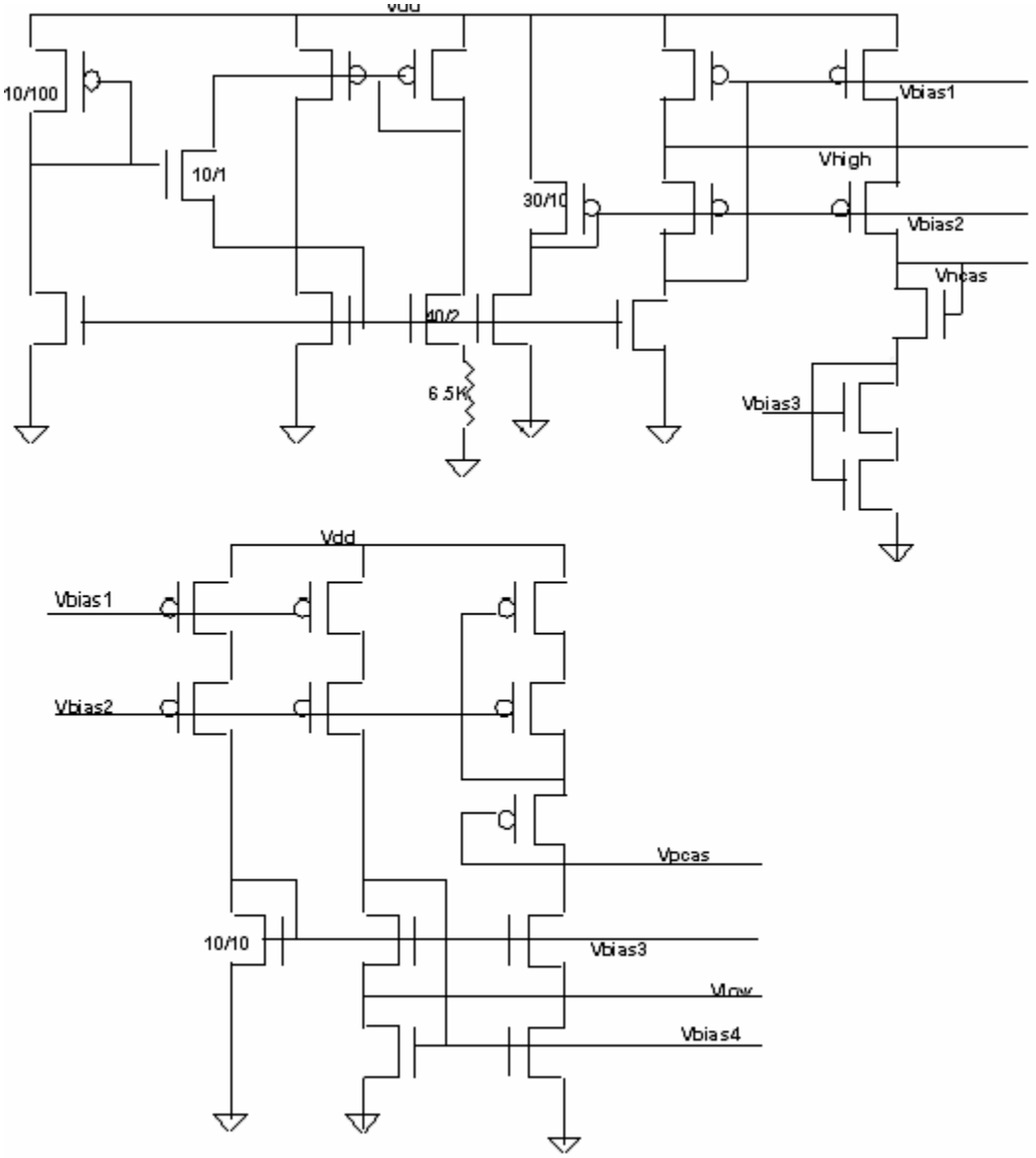
```
.control
destroy all
run
let Io=-Vo#branch
let ro=1/deriv(Io)
let Id3=vdummy#branch
let rd3=1/deriv(Id3)
plot ro
plot Io
.endc

.option scale=1u
.dc Vo 0.25 5 1m

VDD    VDD    0       DC     5
Vo     Vo     0       DC     0
vdummy vd5b   vd3     DC     0

X1     VDD    Vbiasp  Vbiasn bmrefl

M1     Vd1    Vd3     0      0      NMOS L=2  W=10
M2     Vd2    Vd3     0      0      NMOS L=2  W=10
M3     Vd3    Vg3     Vd1    0      NMOS L=2  W=10
MWS    Vg3    Vg3     0      0      NMOS L=7  W=10
M4     Vo     Vg3     Vd2    0      NMOS L=2  W=10

M5a    Vg3    Vbiasp  VDD    VDD    PMOS L=2 W=30
M5b    Vd5b   Vbiasp  VDD    VDD    PMOS L=2 W=30

.subckt bmrefl VDD Vbiasp Vbiasn
M1     Vbiasn Vbiasn  0      0      NMOS L=2 W=10
M2     Vbiasp Vbiasn  Vr     0      NMOS L=2 W=40
```

```
M3      Vbiasn  Vbiasp  VDD     VDD     PMOS L=2 W=30
M4      Vbiasp  Vbiasp  VDD     VDD     PMOS L=2 W=30

Rbias   Vr      0       6.5k

MSU1    Vsur    Vbiasn  0       0       NMOS L=2   W=10
MSU2    Vsur    Vsur    VDD     VDD     PMOS L=100 W=10
MSU3    Vbiasp  Vsur    Vbiasn  0       NMOS L=1   W=10
.ends
```





20.18 Solution:



From above figure in order to keep circuit in saturation

Vbias1 = Vdd-Vsgp	=5-1.15	= 3.58v
Vhigh = Vdd-Vsdsat	=5-0.25	=4.75v
Vbias2 = Vdd-(Vsgp+Vsdsat)	=5-1.4	=3.6v
Vncas = Vgsn+Vgsn	=1.05+1.05	= 2.1v
Vpcas = Vdd-(Vsgp+Vsgp)	=5-2.3	= 2.7v
Vbias3 = Vgsn+Vdssat	= 1.05+0.25	= 1.3v
Vlow = Vdssat		= 0.25v
Vbias4 = Vgs		=1.05v

```
*** Assign 20.18  CMOS: Circuit Design, Layout, and Simulation ***
.control
destroy all
run
print vbias1 vhigh vbias2 vncas vpcas vbias3 vlow vbias4
.endc
.option scale=1u rshunt=1e9
.op
VDD   VDD   0     DC    5
Vop   Vop   0     DC    5
Xbias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias
M2P   Vdp2  Vbias1      VDD   VDD   PMOS L=2 W=30
M4P   Vop   Vbias2      Vdp2  VDD   PMOS L=2 W=30
.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas
MN1   Vbias2      Vbiasn      0     0     NMOS L=2 W=10
MN2   Vbias1      Vbiasn      0     0     NMOS L=2 W=10
MN3   Vncas Vncas vn1   0     NMOS L=2 W=10
MN4   vn1   Vbias3      vn2   0     NMOS L=2 W=10
MN5   vn2   vn1   0     0     NMOS L=2 W=10
MN6   Vbias3      Vbias3      0     0     NMOS L=10 W=10
MN7   Vbias4      Vbias3      Vlow  0     NMOS L=2 W=10
MN8   Vlow  Vbias4      0     0     NMOS L=2 W=10
MN9   Vpcas Vbias3      vn3   0     NMOS L=2 W=10
MN10  vn3   Vbias4      0     0     NMOS L=2 W=10

MP1   Vbias2      Vbias2      VDD   VDD   PMOS L=10 W=30
MP2   Vhigh Vbias1      VDD   VDD   PMOS L=2 W=30
MP3   Vbias1      Vbias2      Vhigh VDD   PMOS L=2 W=30
MP4   vp1   Vbias1      VDD   VDD   PMOS L=2 W=30
MP5   Vncas Vbias2      vp1   VDD   PMOS L=2 W=30
MP6   vp2   Vbias1      VDD   VDD   PMOS L=2 W=30
MP7   Vbias3      Vbias2      vp2   VDD   PMOS L=2 W=30
MP8   vp3   Vbias1      VDD   VDD   PMOS L=2 W=30
MP9   Vbias4      Vbias2      vp3   VDD   PMOS L=2 W=30
MP10  vp4   vp5   VDD   VDD   PMOS L=2 W=30
MP11  vp5   Vbias2      vp4   VDD   PMOS L=2 W=30
MP12  Vpcas Vpcas vp5   VDD   PMOS L=2 W=30

MBM1  Vbiasn      Vbiasn      0     0     NMOS L=2 W=10
MBM2  Vbiasp      Vbiasn      Vr    0     NMOS L=2 W=40
MBM3  Vbiasn      Vbiasp      VDD   VDD   PMOS L=2 W=30
MBM4  Vbiasp      Vbiasp      VDD   VDD   PMOS L=2 W=30

Rbias Vr    0     6.5k

MSU1  Vsur  Vbiasn      0     0     NMOS L=2   W=10
MSU2  Vsur  Vsur  VDD   VDD   PMOS L=100 W=10
MSU3  Vbiasp      Vsur  Vbiasn      0     NMOS L=1   W=10
.ends
```

Simulation Outputs:

DC Operating Point ...100%
vbias1 = 3.840356e+00
vhigh = 4.678606e+00
vbias2 = 3.430383e+00
vncas = 2.414760e+00
vpcas = 2.412956e+00
vbias3 = 1.493566e+00
vlow = 3.238476e-01
vbias4 = 1.086655e+00

Motheeswara Salla
Hw3, Problem 20.19

Figure 20.44, Problem 20.19
In the figure below both P-channel transistors are 30/2 size initially.
The circuit is designed to mirror 20ua with Vsg of 1.15V.

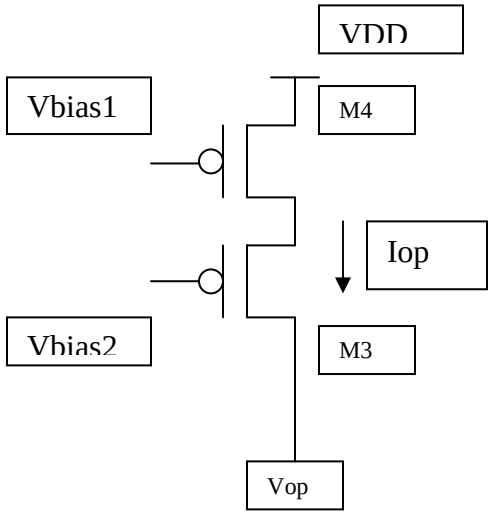
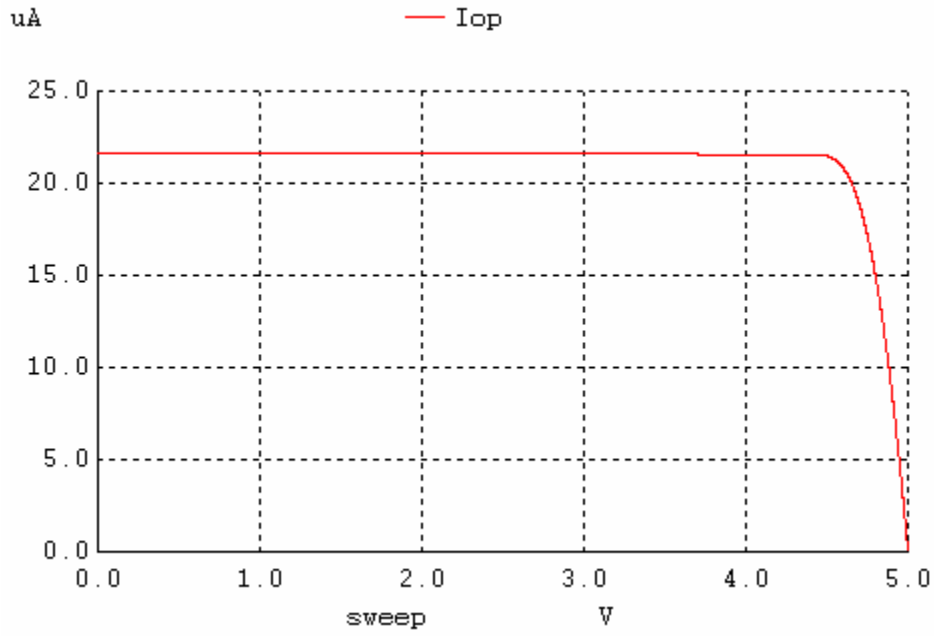
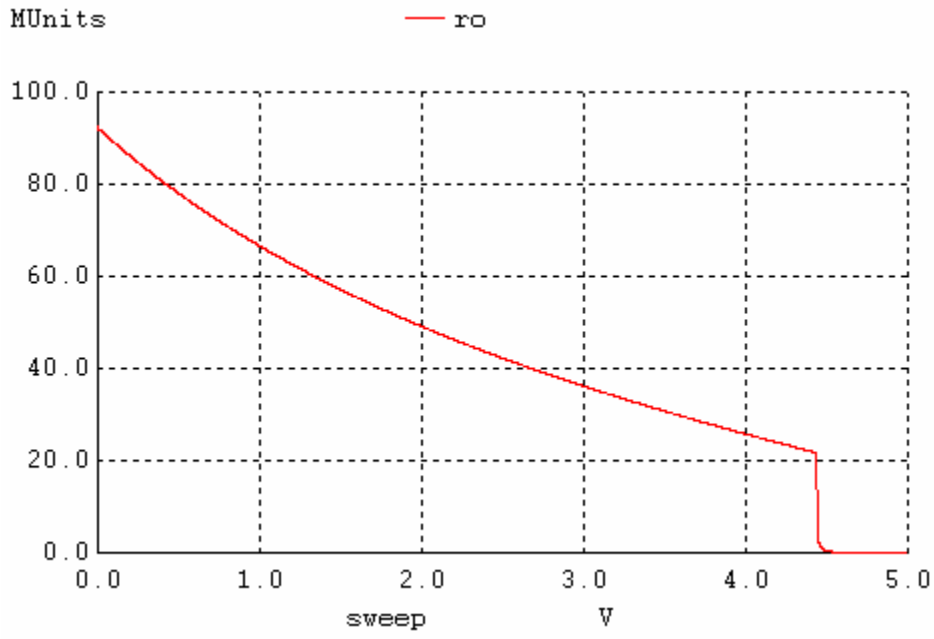
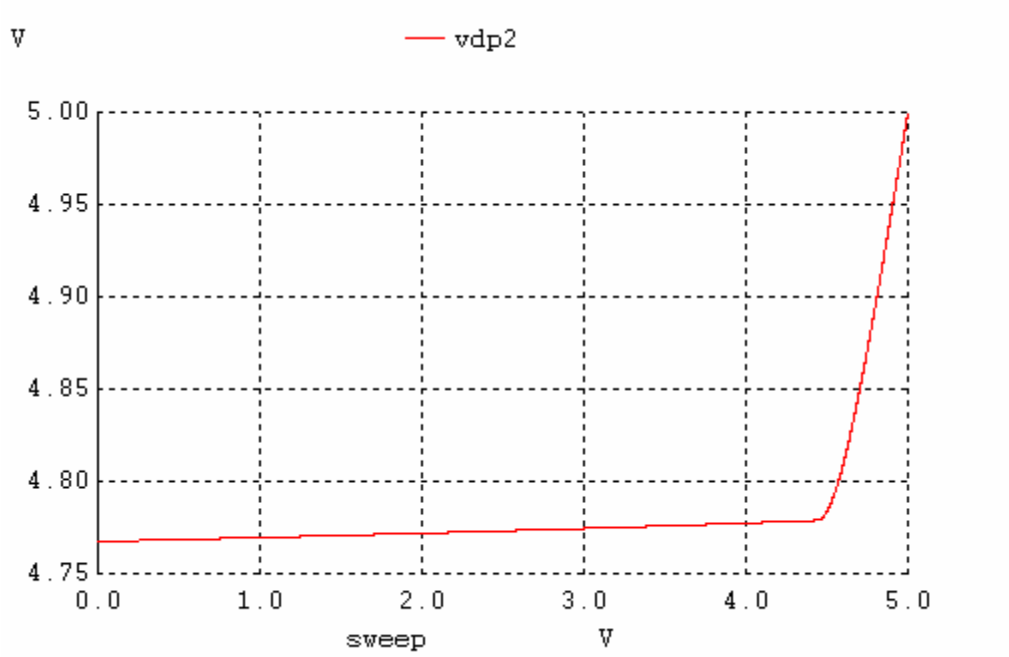


Figure 20.44

Case1: Reduce the size of M3, say15/2
When we reduce the size of the transistor M3, the source voltage of M3 will go up and so does Vgs3 and Vds3. since Id is proportional to 1/L and proportional to Vds^2 the overall current will be constant (since the transistors are in saturation). However since Vgs has increased the transistor M3 will enter in saturation earlier.

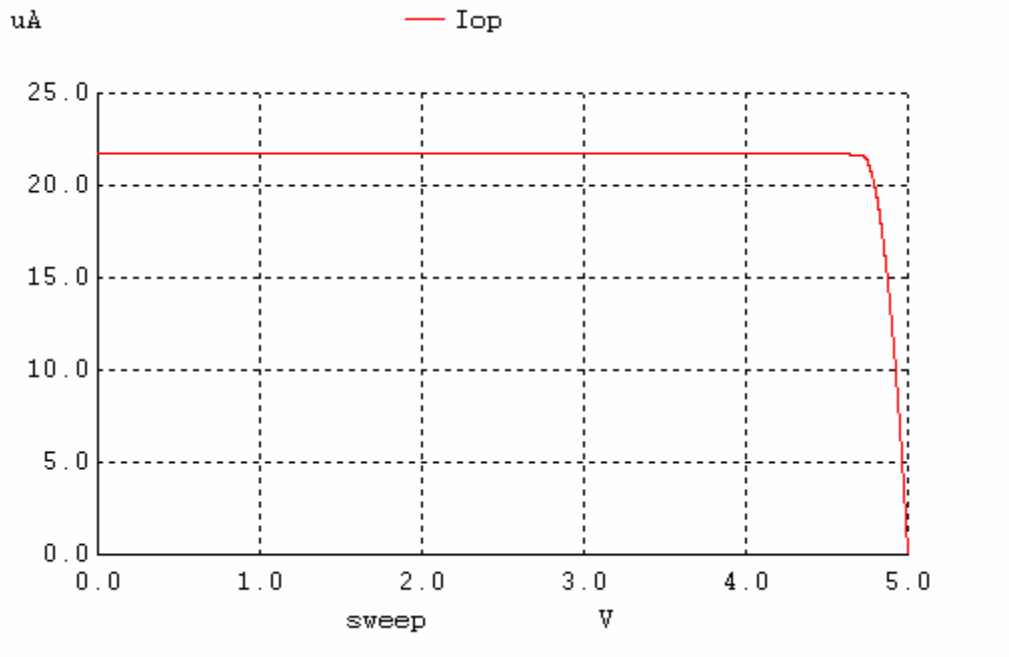


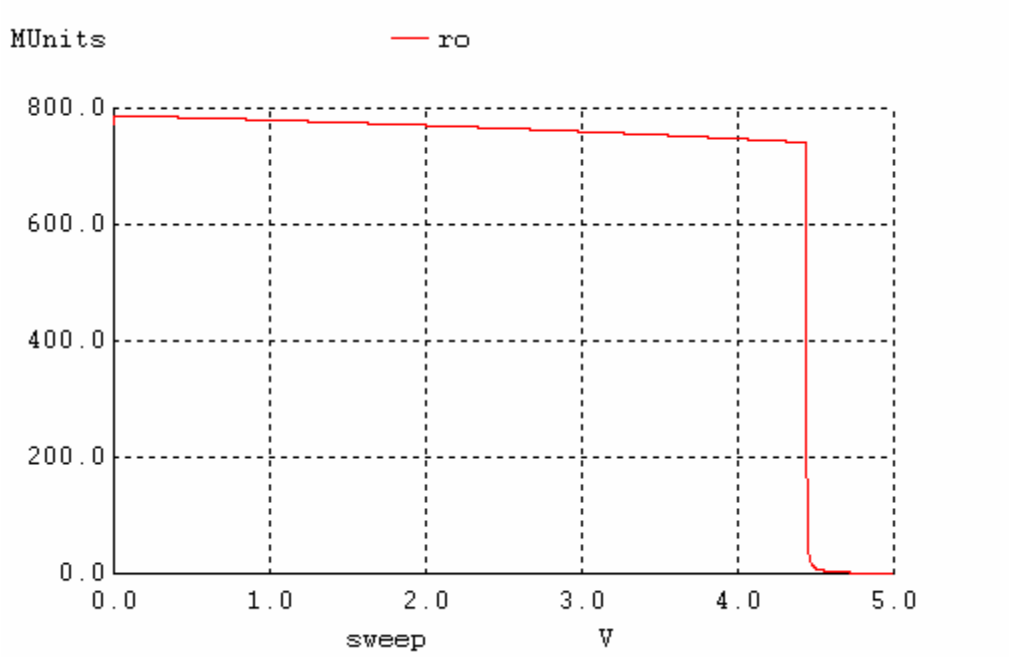


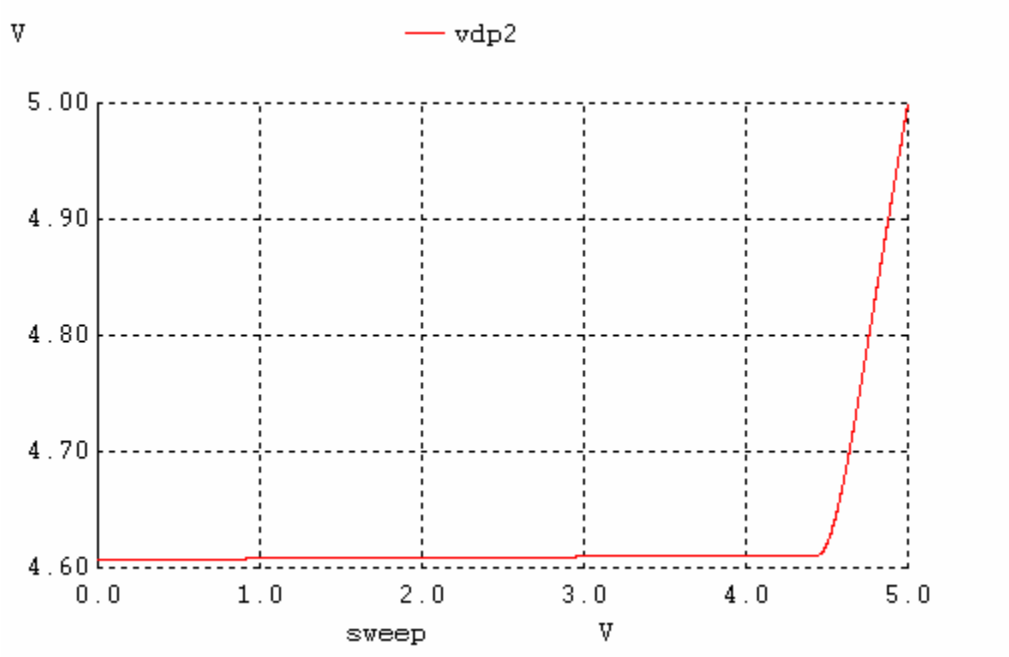


In Vdp2 plot, for 15/2 device, we see the source voltage of the transistor is varying with changing Vop which is causing the output resistance of the cascode to vary with varying Vop.

Case2: Increase the size of M3, say 60/2
When we increase the size of the transistor M3, the source voltage will decrease. since Id is proportional to 1/L and proportional to Vds^2 , the overall current will be constant. However since Vgs has decreased the transistor M3 will enter in saturation later.







Vdp2 plots are source voltage of M3.

*** Figure 20.44_PMOS CMOS: Circuit Design, Layout, and Simulation ***

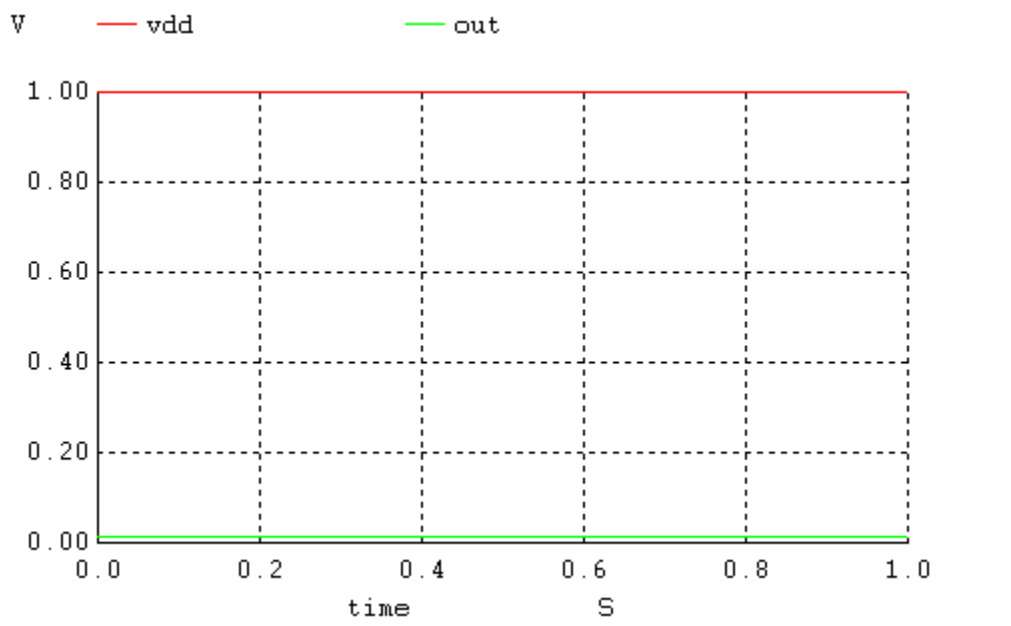
```
.control
destroy all
run
let Iop=Vop#branch
let ro=abs(1/deriv(Iop))
plot ro
plot Iop ylimit 0 25u
.endc

.option scale=1u rshunt=1e9
.dc vop 0 5 1m

VDD   VDD   0       DC     5
Vop   Vop   0       DC     2.5

Xbias  VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

M2P   Vdp2  Vbias1 VDD   VDD   PMOS L=2 W=30
M4P   Vop   Vbias2 Vdp2  VDD   PMOS L=2 W=15

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MN1   Vbias2 Vbiasn 0       0       NMOS L=2 W=10
MN2   Vbias1 Vbiasn 0       0       NMOS L=2 W=10
MN3   Vncas  Vncas  vn1     0       NMOS L=2 W=10
MN4   vn1    Vbias3 vn2     0       NMOS L=2 W=10
MN5   vn2    vn1    0       0       NMOS L=2 W=10
MN6   Vbias3 Vbias3 0       0       NMOS L=10 W=10
MN7   Vbias4 Vbias3 Vlow    0       NMOS L=2 W=10
MN8   Vlow   Vbias4 0       0       NMOS L=2 W=10
MN9   Vpcas  Vbias3 vn3     0       NMOS L=2 W=10
MN10  vn3    Vbias4 0       0       NMOS L=2 W=10

MP1   Vbias2 Vbias2 VDD   VDD   PMOS L=10 W=30
MP2   Vhigh  Vbias1 VDD   VDD   PMOS L=2 W=30
MP3   Vbias1 Vbias2 Vhigh VDD   PMOS L=2 W=30
MP4   vp1    Vbias1 VDD   VDD   PMOS L=2 W=30
MP5   Vncas  Vbias2 vp1   VDD   PMOS L=2 W=30
MP6   vp2    Vbias1 VDD   VDD   PMOS L=2 W=30
MP7   Vbias3 Vbias2 vp2   VDD   PMOS L=2 W=30
MP8   vp3    Vbias1 VDD   VDD   PMOS L=2 W=30
MP9   Vbias4 Vbias2 vp3   VDD   PMOS L=2 W=30
MP10  vp4    vp5    VDD   VDD   PMOS L=2 W=30
```

```
MP11  vp5     Vbias2 vp4     VDD   PMOS L=2 W=30
MP12  Vpcas   Vpcas  vp5     VDD   PMOS L=2 W=30

MBM1 Vbiasn Vbiasn 0        0       NMOS L=2 W=10
MBM2 Vbiasp Vbiasn Vr       0       NMOS L=2 W=40
MBM3 Vbiasn         Vbiasp VDD   VDD   PMOS L=2 W=30
MBM4 Vbiasp Vbiasp VDD   VDD   PMOS L=2 W=30

Rbias   Vr       0        6.5k

MSU1  Vsur    Vbiasn 0        0       NMOS L=2   W=10
MSU2  Vsur    Vsur    VDD   VDD   PMOS L=100 W=10
MSU3  Vbiasp Vsur    Vbiasn 0        NMOS L=1   W=10

.ends

.MODEL NMOS NMOS LEVEL  = 3
+ TOX    = 200E-10       NSUB   = 1E17          GAMMA  = 0.5
+ PHI    = 0.7           VTO    = 0.8           DELTA  = 3.0
+ UO     = 650           ETA    = 3.0E-6        THETA  = 0.1
+ KP     = 120E-6        VMAX   = 1E5           KAPPA  = 0.3
+ RSH    = 0             NFS    = 1E12          TPG    = 1
+ XJ     = 500E-9        LD     = 100E-9
+ CGDO   = 200E-12       CGSO   = 200E-12       CGBO   = 1E-10
+ CJ     = 400E-6        PB     = 1             MJ     = 0.5
+ CJSW   = 300E-12       MJSW   = 0.5
*
.MODEL PMOS PMOS LEVEL  = 3
+ TOX    = 200E-10       NSUB   = 1E17          GAMMA  = 0.6
+ PHI    = 0.7           VTO    = -0.9          DELTA  = 0.1
+ UO     = 250           ETA    = 0             THETA  = 0.1
+ KP     = 40E-6         VMAX   = 5E4           KAPPA  = 1
+ RSH    = 0             NFS    = 1E12          TPG    = -1
+ XJ     = 500E-9        LD     = 100E-9
+ CGDO   = 200E-12       CGSO   = 200E-12       CGBO   = 1E-10
+ CJ     = 400E-6        PB     = 1             MJ     = 0.5
+ CJSW   = 300E-12       MJSW   = 0.5

.end
```

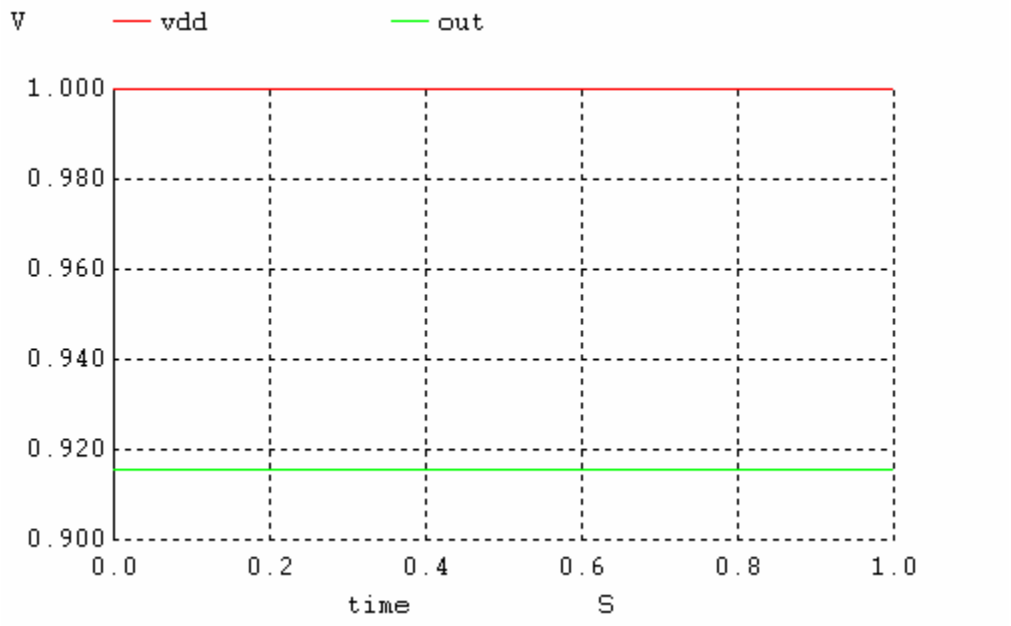
Problem 20.20

Should the voltage labeled “Out” in Fig. 20.49 be at a specific value? Why or Why not.

No, it doesn’t need to be at a specific value. It will be pulled towards either VDD or GND depending on whether MOP or MON is stronger.



Plot where NMOS is stronger(NMOS W=500, PMOS W=1000)



Plot where PMOS is stronger (NMOS W=100, PMOS W=5000)

Changing the W/L ratios of MON and MOP will effect the current through stage 2 which is expected but it won’t effect the reference current in stage 1.