6.1) Suggest a topology for a passive-integrator NS modulator where the input and fed back signals are currents. Derive a transfer function for your design. Does your topology have the extra noise/distortion term seen in Eq. (6.12)? Why or why not? Simulate the operation of your design.

We can feed a current into the passive integrator with an ideal current source and we can remove current with a combination of an ideal current source and some MOSFET gates. Referring to Fig. 6.1.1, I have elected to use three NMOS gates from a 1µm process. M1 is the switch which gates the removal of current from the sigma bucket (passive integrator). M3 is gate-drain connected to set the V_{GS} of M2, which mirrors the current in M3. The topology is very similar to that of the delta-sigma modulator seen in *CMOS: Circuit Design, Layout and Simulation,* chapter 17. The major differences are that here we are gating the output current, not the input, and the input is a periodic signal.

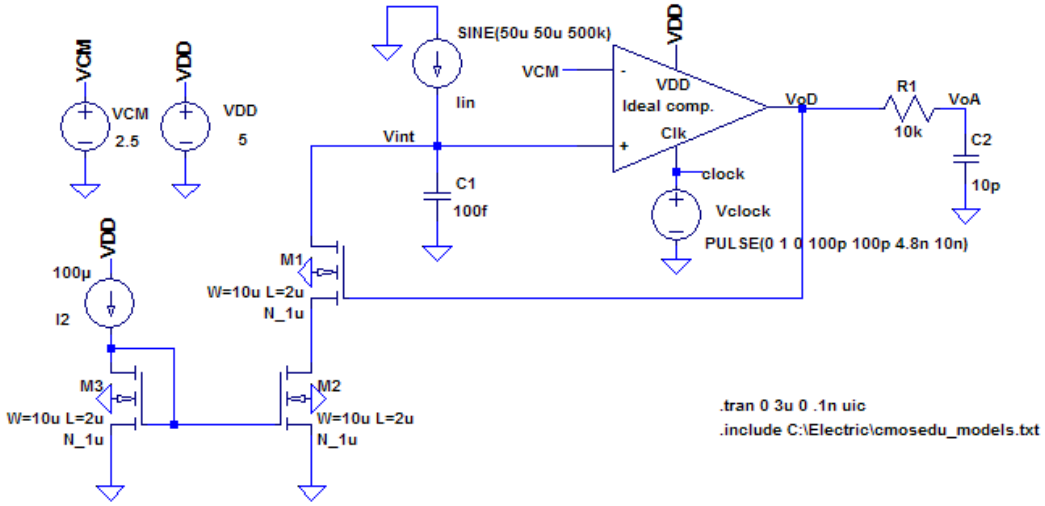


Figure 6.1. 1. Passive-integrator noise-shaping (NS) modulator with input and fed-back signals as currents.

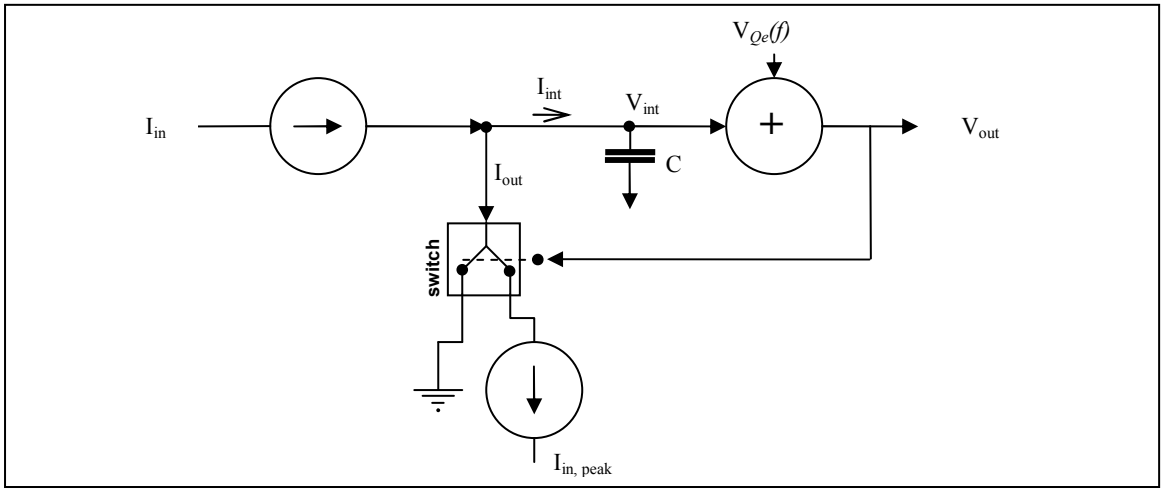


Figure 6.1. 2. Block diagram for Fig. 6.1.1.

Following the block diagram (and switching the polarity of the I_{in} and $V_{out} * I_{in,p}$ signals), we can derive the transfer function:

$$I_{\text{int}} = I_{in} - I_{out}; \qquad I_{out} = V_{out} \cdot I_{in,peak} \ (V_{out} = \{0,1\}); \qquad V_{\text{int}} = \frac{I_{\text{int}}}{j\omega C}$$

$$V_{\text{int}} + V_{Qe} = V_{out}$$

$$\frac{I_{in} - I_{out}}{j\omega C} + V_{Qe} = V_{out}$$

$$\frac{I_{in} - V_{out} \cdot I_{in,peak}}{j\omega C} + V_{Qe} = V_{out}$$

$$V_{out}\left(I_{in,peak} + j\omega C\right) = I_{in} + V_{Qe} \cdot j\omega C$$

$$V_{out} = \underbrace{\frac{I_{in}}{I_{in,peak}} \cdot \frac{1}{1 + j\omega C / I_{in,peak}}}_{\text{STF}(f)} + \underbrace{\frac{V_{Qe}}{I_{in,peak}} \cdot \frac{1}{1 + j\omega C / I_{in,peak}}}_{\text{NTF}(f)}.$$

Notice that the transfer function does not contain a component due to extra noise / distortion. This is due to the removal of the resistors, which couple to the circuit as noise sources.

The simulation for the circuit in Fig. 6.1.1 is seen in Fig. 6.1.3. Displayed signals are the input (I_{in}) in red, the digital output (V_{oD}) in blue, and the reconstructed analog output (V_{oA}) in brown. The analog output was reconstructed through a crude RC filter; not pretty, but good enough to see the results.

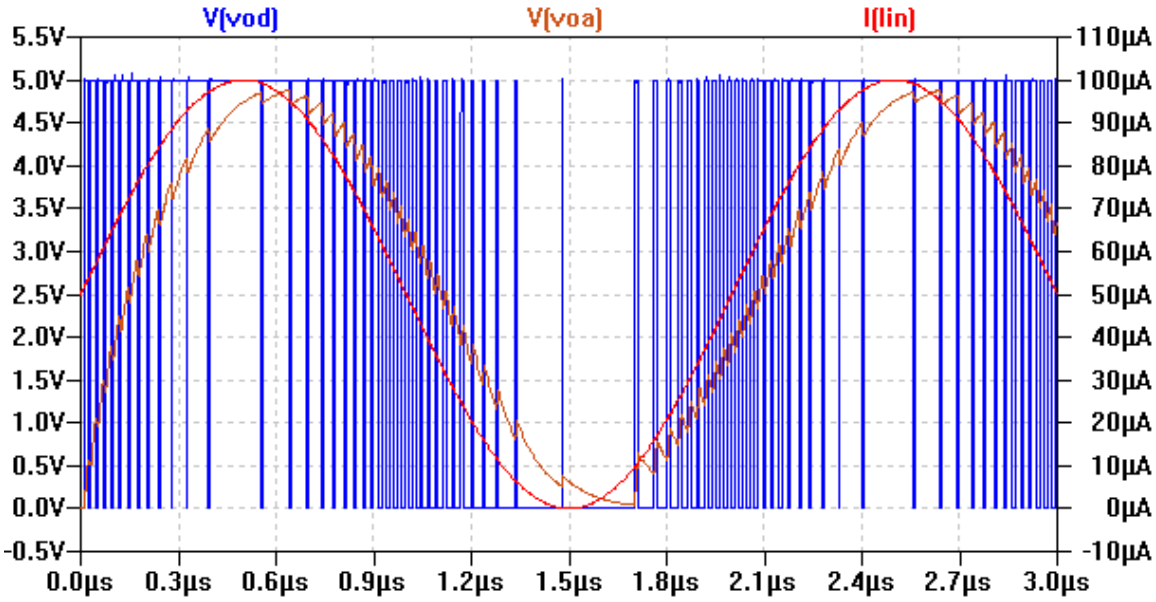
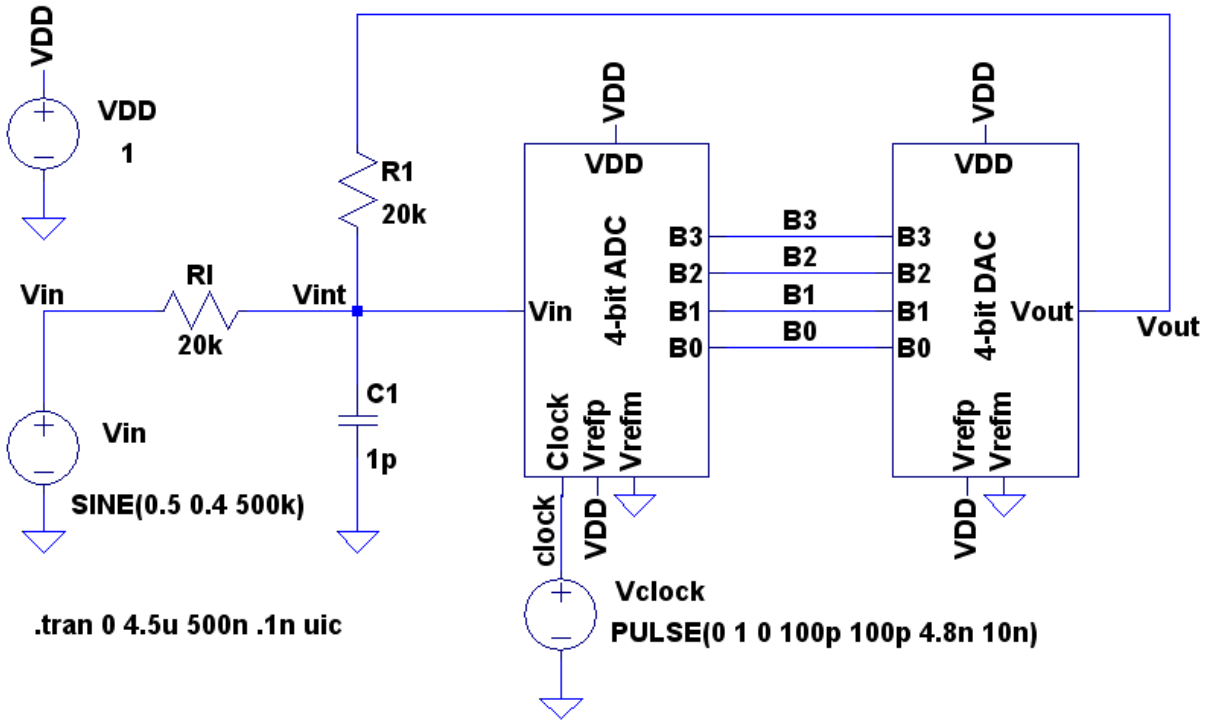


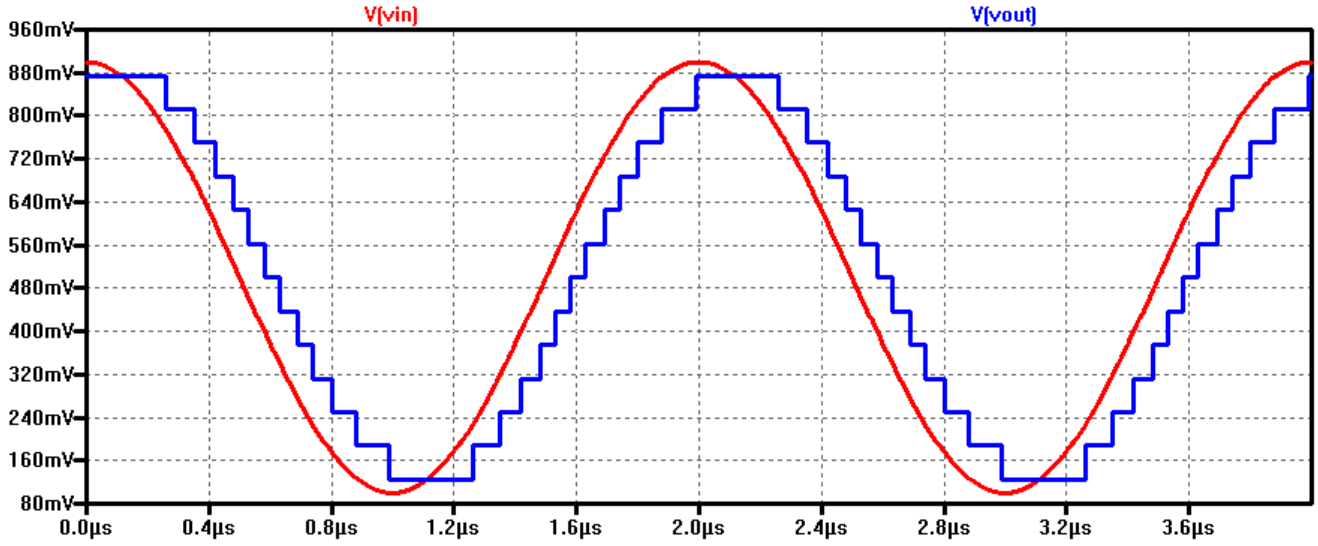
Figure 6.1. 3 Simulation output for the passive-integrator NS modulator of Fig. 6.1.1.

Jason Durand

Problem 6.2 – Simulate the operation of the NS modulator seen in Fig 6.4a but using a 4-bit quantizer (ADC). Use a 100MHz clock frequency and an input sinewave at 500kHz.



Above is the modified figure 6.4a, a passive NS modulator with a 4-bit ADC on the integration node instead of a one bit quantizer (clocked comparator). The clock signal is 100MHz.



The red signal is Vin, and the quantized signal is the output of the modulator, hopefully with better averaging.

Question 6.3

Using Eqs (6.14) and (6.17) compare the noise performance of passive NS modulators using a 1-bit quantizer to those using a 4-bit quantizer.

Solution

Equations 6.14 and 6.17 (page 208 – 209) are given as

$$V^2_{noise,RMS} = 2 \cdot \frac{V^2_{LSB}}{12 f_s} \cdot (2\pi RC)^2 \cdot \frac{B^3}{3} \tag{6.14}$$

$$SNR_{ideal} = 20 \cdot \log \frac{V_p / \sqrt{2}}{V_{noise,RMS}} = 6.02N + 1.76 - 18.06 + 30 \log K \tag{6.17}$$

where B is the signal bandwidth of interest for first equation. In second equation N is the bit resolution of a quantizer, effects of which will be discussed in the solution and K is the oversampling ratio $K = \frac{f_s}{2B}$.

Equation 6.14 V_{LSB} can be expanded as $V_{LSB} = \frac{V_{REF+} - V_{REF-}}{2^N}$ for $N \geq 2$ where V_{REF+} and V_{REF-} are assumed as the maximum and minimum input voltages of the system respectively. Also peak amplitude of input signal is limited by these reference voltages as $V_p = \frac{V_{REF+} - V_{REF-}}{2}$. Thus putting the value of V_{LSB} in first equation we get

$$V^2_{noise,RMS} = 2 \cdot \left(\frac{V_{REF+} - V_{REF-}}{2^N} \right)^2 \cdot \frac{1}{12 f_s} \cdot (2\pi RC)^2 \cdot \frac{B^3}{3} \tag{1}$$

in case of a 4-bit quantizer or $N = 4$. For a 1-bit quantizer value of V_{LSB} is given as $V_{LSB} = V_{REF+} - V_{REF-}$. As already mentioned, N is the bit resolution of the quantizer used in passive NS modulators. Looking at equation 1 we can say that the $V^2_{noise,RMS}$ will be lower by $1/2^8$ for N = 4 bit quantizer as compared to $N = 1$ bit or $V_{noise,RMS}$ is lowered by $1/2^4$ which is a significant lowering.

In case of equation 6.17 it is straight forward after looking at the equation that increasing the value of N or the bit resolution of the quantizer the value of SNR_{ideal} will increase.

Note: Although, increasing the value of N or quantizer bit resolution the noise performance of the passive NS modulator increases, there is a strict restriction on the linearity of the quantizer if it is more than 1-bit. In case of 1-bit, the quantizer will be linear always because of only two output level.

Tyler Hansen

6.4 – Repeat Ex. 6.2 if C is changed to 1 pF and a 1GHz clock frequency is used. Estimate the frequency where the output of the digital filter is -3 dB (0.707) from the input signal. Verify your answer with simulations.

Example 6.2 uses a NS modulator that is discussed in Ex. 6.l. Ex. 6.1 simulates the operation a passive NS modulator as seen in book figure 6.4. The schematic is reproduced below in figure 6.4.1:

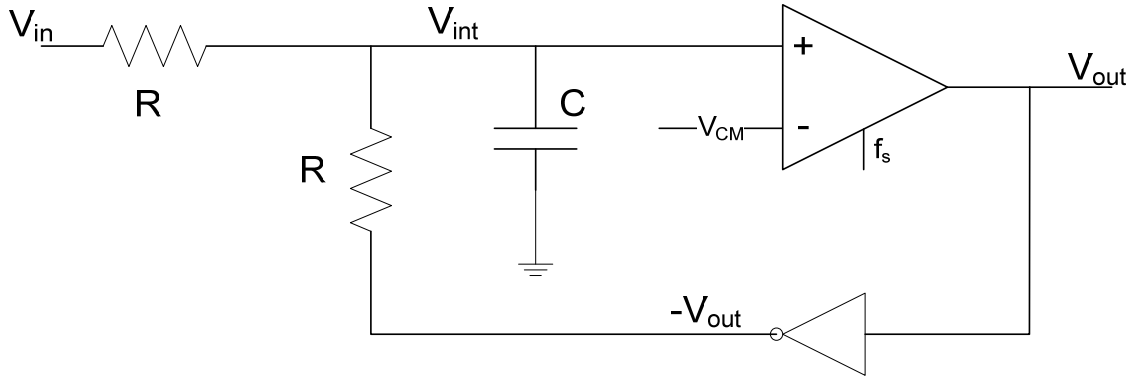


Figure 6.4.1: Reproduction of book figure 6.4 -> a circuit implementation of a passive NS modulator.

Originally example 6.1 uses values for R and C of 10kΩ and 10pF respectively. Problem 6.4 asks us to use a capacitance of 1pF. What does this do to the STF (signal transfer function)? What does it do to the NTF (noise transfer function)? To answer these questions, let's look at book equation 6.12 (reproduced here as equation 6.4.1):

$$v_{out} = \frac{1}{1 + j\omega RC} \cdot v_{in} + \frac{j\omega RC}{1 + j\omega RC} \cdot V_{Qe} + \frac{-2 \cdot v_{\text{int}}}{1 + j\omega RC} \qquad \text{Equation 6.4.1}$$

Note that the coefficient for our input signal defines a lowpass frequency response. The 3dB frequency occurs when the imaginary component of the pole (jωRC) is equal to the real component in the pole (1), or at f=1/2πRC. With the new capacitor value provided in the problem definition, we can calculate the 3dB frequency as 1/2π*10kΩ*1pF = 15.9MHz. In an attempt to prove this with a clean simulation, I will start with the simulation for the book figure 6.7, and modify it for my changes. I will make the 1GHz clock a bit more ideal by reducing the rise and fall time to 1ps, and I will modify the RC "reconstruction" filter to exhibit the same frequency response as that of the STF mentioned above. The modified schematic and associated simulation results at the 3dB frequency of 15.9MHz can be seen in figure 6.4.2a and 6.4.2b.

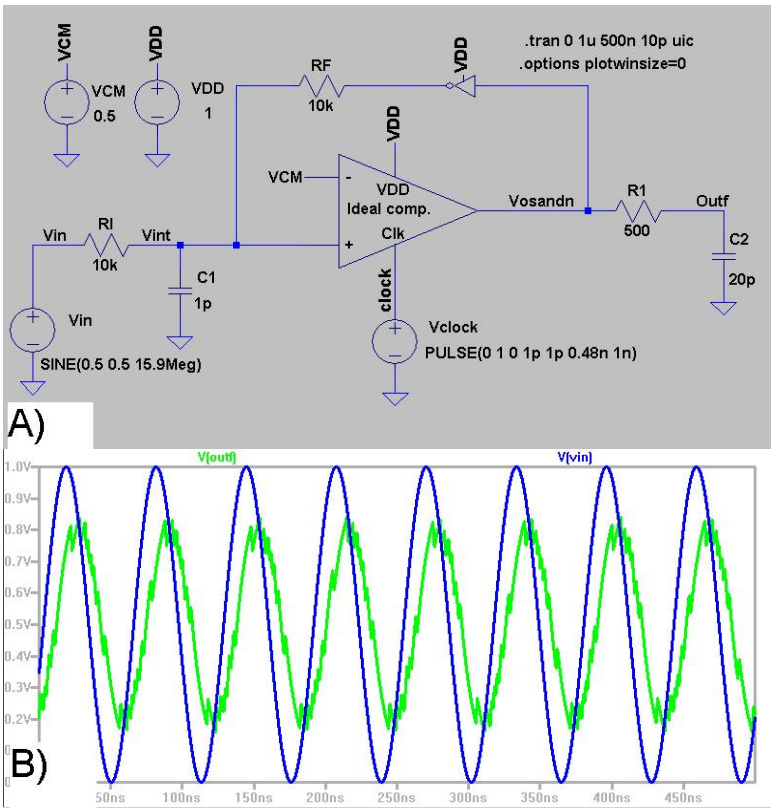


Figure 6.4.2: Simulation of a passive NS modulator as in book figure 6.4, substituting 1pF for the previous 10pF value of capacitance, along with an increased sampling frequency from 100MHz to 1GHz.

As can be seen from reviewing figure 6.4.2b, our estimated 3dB frequency seems to be pretty accurate. Now, to complete the solution we need to swap a K=16 decimating filter for the basic RC reconstruction filter that we used in figure 6.4.2a. This is done in figure 6.4.3 below.

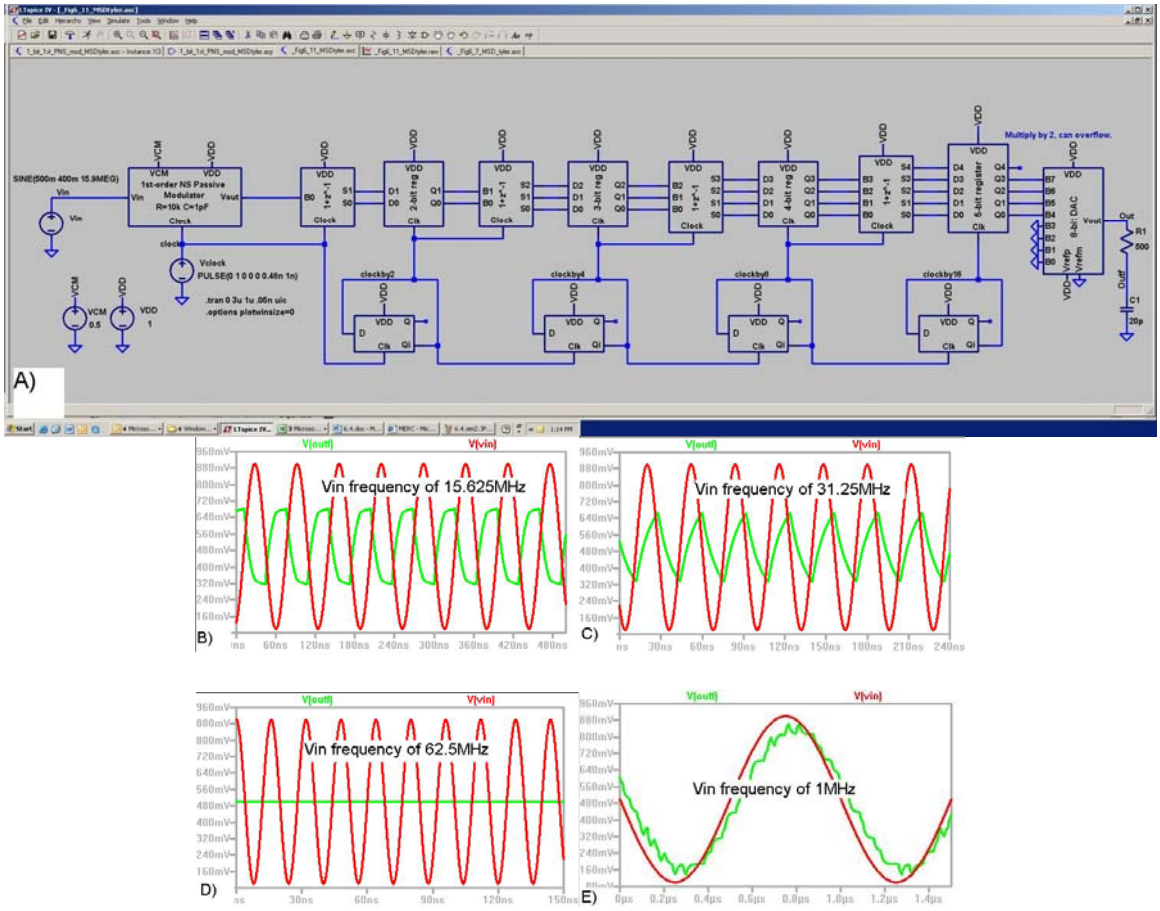


Figure 6.4.2: Simulation of a passive NS modulator connected to a K=16 decimating filter.

As can be seen in the simulation results of varying input signal frequencies, at 62.5MHz, or f_s/K, the input signal is attenuated to 0. At the Nyquist frequency of 31.25MHz, or $f_s/2K$, the output signal peaks at ~650mV. By the same token, we see in figure 6.4.2e that an input signal with a frequency of 1MHz is only slightly attenuated.

What about the SNR? If we look at the book figure 6.8, we can see that if we increase the clock frequency, the Nyquist frequency also goes up. That means that we are spreading a fixed amount of quantization noise over a larger bandwidth, and the SNR of our system should go up. Let's use the equations derived in section 6.1.1 to estimate the change in SNR as a result of the clock frequency increase from 100MHz to 1GHz. Using the book equation 6.17 with our values of R, C, and f_s, we can approximate the ideal SNR.

$$SNR_{ideal} = 20 \cdot \log \frac{V_p / \sqrt{2}}{V_{noise,RMS}} = 6.02N + 1.76 - 20 \cdot \log \frac{2\pi RC \cdot f_s}{\sqrt{12}} + 20 \cdot \log K^{3/2}$$

$$SNR_{ideal} = 6.02N + 1.76 - 20 \cdot \log \frac{2\pi (10k\Omega)(1pF) \cdot 1GHz}{\sqrt{12}} + 20 \cdot \log 16^{3/2}$$

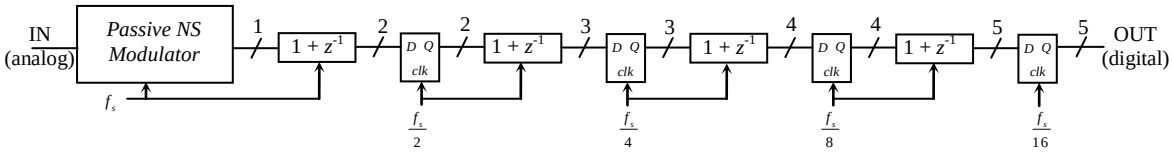
$$SNR_{ideal} = 6.02 + 1.76 - 25.17 + 36.1236$$

$$SNR_{ideal} = 18.7336[dB]$$

Equation 6.4.2

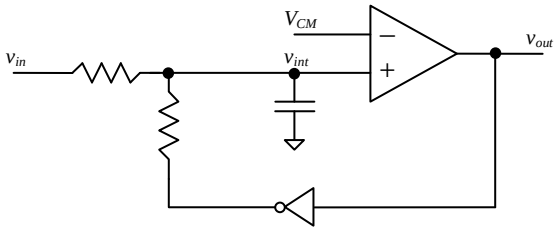
QAWI HARVARD – ECE615 (CMOS Mixed Signal Design) HW6

6.5 *Suppose the comparator used in the NS modulator and filter used in Ex. 6.2 has a 50 mV input-referred offset voltage. How will this offset voltage affect the conversion from analog to digital? Verify your answer with SPICE simulations.*



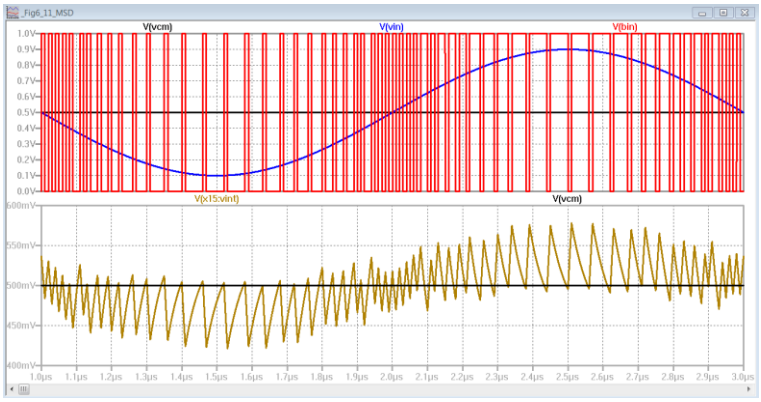
F-1 ADC using a passive noise shaping (NS) modulator along with a low-pass and decimation (CIC) filter

The answer to this question is stated clearly in the first paragraph of section 6.1.3 (Offset, Matching, and Linearity), but let's examine it here. Consider the passive NS modulator seen in F-2.



F-2 Passive NS modulator

The output of the one bit passive NS modulator is a one bit representation of the input signal. The output stays high for as many clock cycles as it takes for the v_{int} node to move below V_{CM}. The simulation results below show how the output bit toggles every T_s (the output is the busiest) when the input signal is close to V_{CM}.



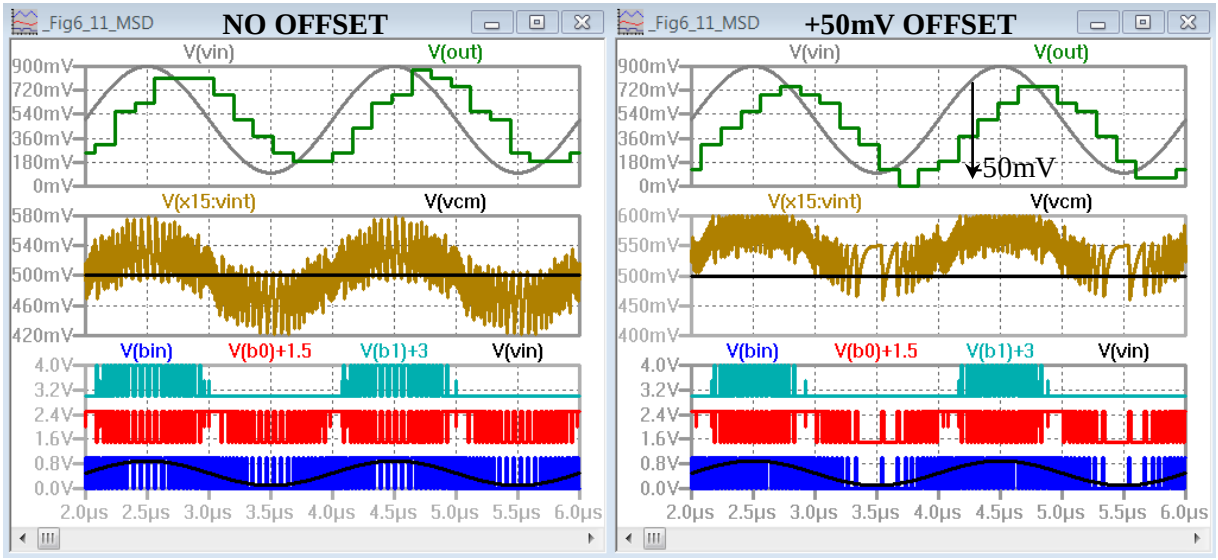
The passive NS modulator converts the input voltage into a current. When there is no input referred offset voltage the input current representation of the input voltage is:

$$\frac{v_{in} - V_{CM}}{R}$$

When this current is present the output will average to V_{CM} (or v_{in}). However, when we refer the comparators offset voltage back to its input the current representation of the input changes to:

$$\frac{v_{in} - (V_{CM} + V_{OS})}{R} = \frac{(v_{in} - V_{OS}) - V_{CM}}{R}$$

The output will now averages to $v_{in} - V_{OS}$. The simulation results below were perfomed by using _Fig6_11_MSD. They show that when an input referred offset voltage of +50mV is applied to the input the output (after DAC) will shift down by 50mV, as perdicted by the equations above.



Kaijun Li
Problem 6.6
Figure 6.36 shows the implementation of an op-amp using mixed-signal design technique. Assuming the comparator is powered with a 1V supply, simulate the circuit in the inverting op-amp configuration with the non-inverting input held at 0.5 V, a 10k resistor connected from the inverting input to the input source, and a feedback resistor of 100k from the op-amp's output back to the inverting input (for a closed loop gain of -10). Set the input source to have a DC offset of 500mV, and a peak-to-peak amplitude of 20mV at 500kHz. Explain how the circuit operates. Note that using an active integrator, instead of the passive integrator results in more ideal behavior (less variation on the op-amp's inputs).

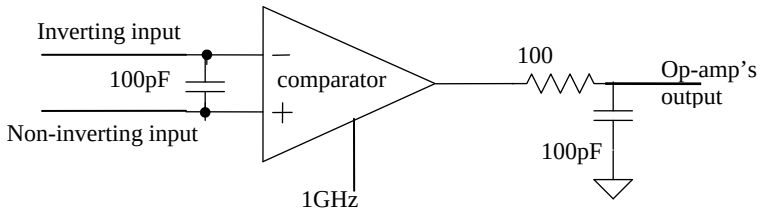


Figure 6.36 An op-amp implemented using mixed-signal design technique

Solution:
First, let's draw the closed-loop configuration of the op-amp which is seen in Fig. 6.6-1.

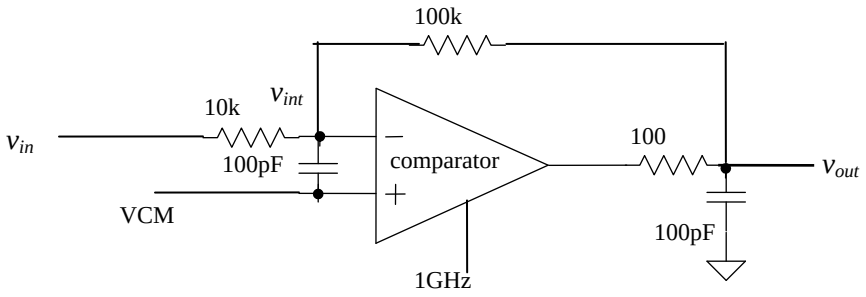


Fig. 6.6-1 Closed-loop configuration for the op-amp

It is noted that the 100pF capacitor across the comparator's inputs can be seen as a "bucket" in the classic delta-sigma structure, and comparator is also know as a one-bit quantizer. The comparator's output is passed through a RC low-pass filter and then fed back to the inverting input of the comparator. So the block diagram is drawn in Fig. 6.6-2. (R=10kOhm)

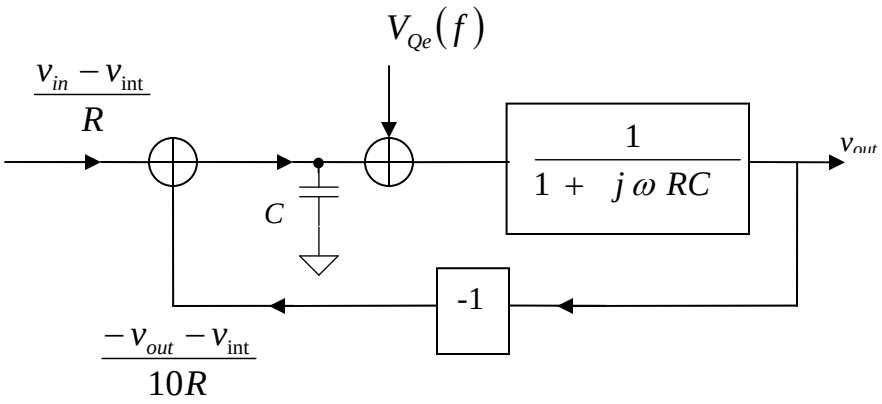


Fig. 6.6-2 Block diagram for the passive-integrator NS modulator

It is also known that

$$\left(V_{Qe}(f)+v_{\text{int}}(f)\right)\frac{1}{1+j\omega RC}=v_{out}(f) \tag{1}$$

Also by applying KCL to inverting input node for the comparator, we have

$$\frac{v_{in}-v_{\text{int}}}{R}+\frac{-v_{out}-v_{\text{int}}}{10R}=\frac{v_{\text{int}}}{1/(j\omega\cdot C)} \tag{2}$$

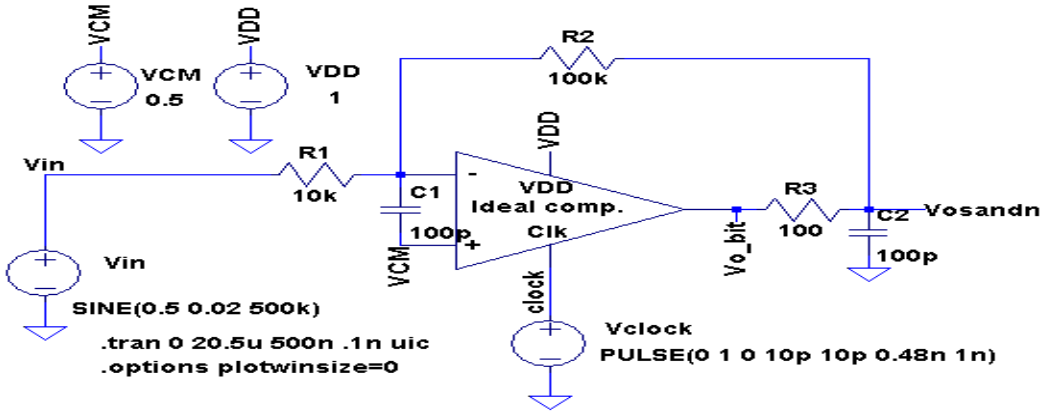
Combining (1) and (2), we have

$$10v_{in}-v_{out}-11v_{\text{int}}+j\omega 10RCV_{Qe}(f)=j\omega 10RCv_{out}$$

Or

$$\frac{10}{1+j\omega 10RC}v_{in}+\frac{j\omega 10RC}{1+j\omega 10RC}V_{Qe}+\frac{-11}{1+j\omega 10RC}v_{\text{int}}=v_{out}$$

After all these analysis, it is obvious that it is a passive-integrator noise-shaping (NS) modulator, and it is important to keep v_{int} from varying to eliminate extra distortion. Simulation is performed in LTSpice, and the results are shown as follows.



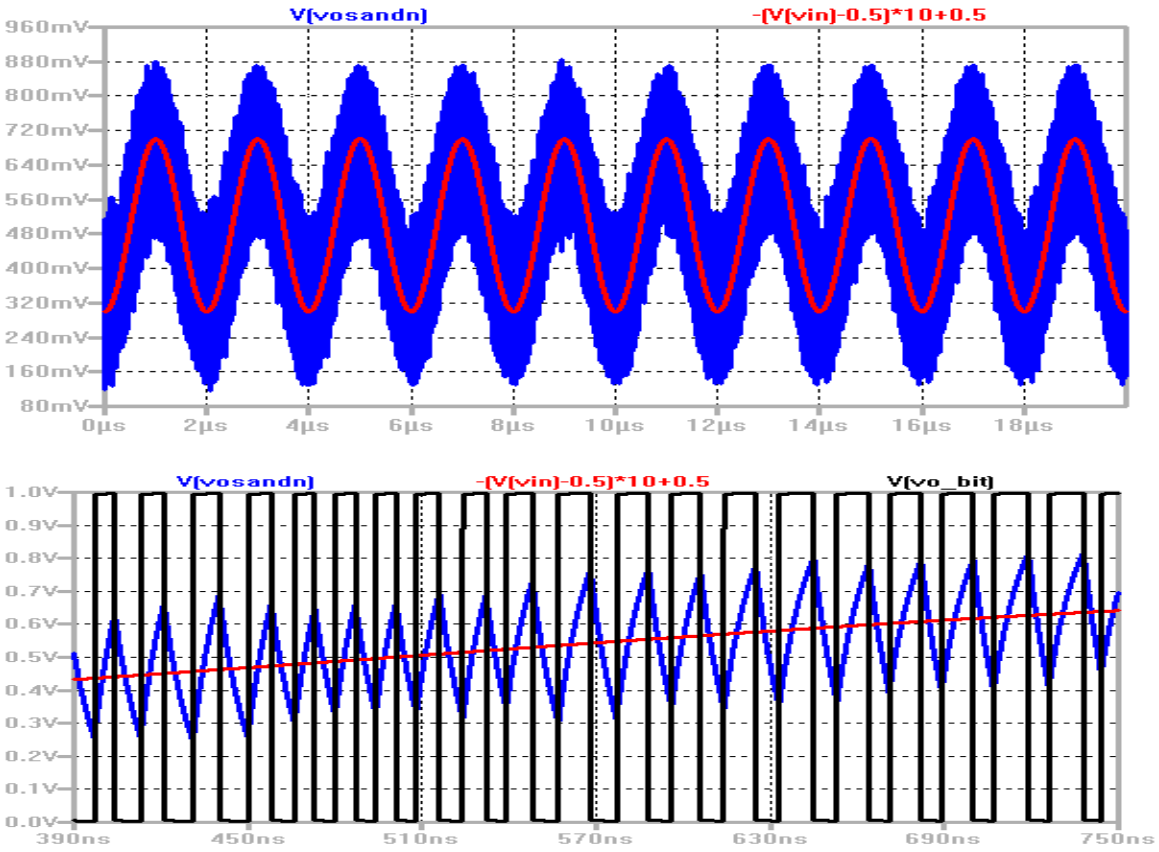


Fig. 6.6-3 Time-domain results

It is noted that the output of the comparator is a single bit stream, and the output of the op-amp is charging or discharging depending on this bit stream's value which is '0' or '1'. The overall closed-loop op-amp has a gain of -10.

To further illustrate what is happening in the frequency domain, a FFT plot is shown in following figure. It is seen that the noise spectrum is pushed out to higher frequency, and if a low-pass filter is applied to the output of the op-amp a high signal-to-noise ratio (SNR) can be achieved.

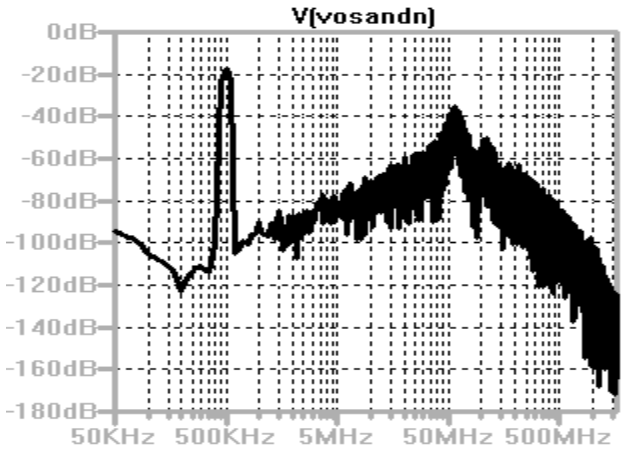


Fig. 6.6-4 FFT plot for the output

6.7. In your own words explain why dead zones in the second-order passive modulator seen in Fig 6.17 are less of a problem than the first-order modulator seen in Fig. 6.4a.

Sol. In a first order passive modulator the noise sees only one path from output to the V_{int} node and hence noise is less randomized. This leads to the output code being less randomized. Hence we have more dead zones.

In the second-order passive modulator in Figure 1, the noise sees two paths from output to node v_1, v_2 respectively. Hence the noise is randomized. This results in the output code being randomized. This translates to a reduction of dead zones.

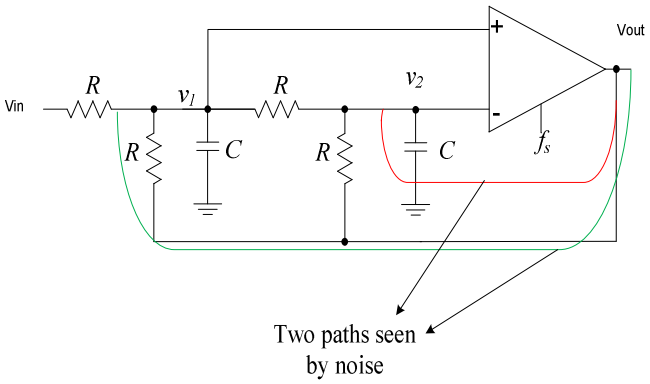


Figure 1. Second-order passive modulator

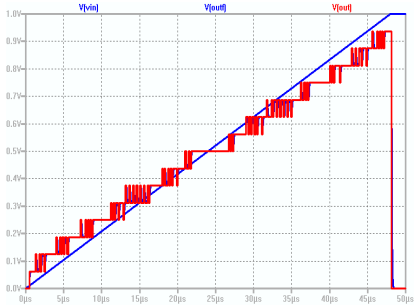


Figure 2. Dead zones in a First-order passive modulator

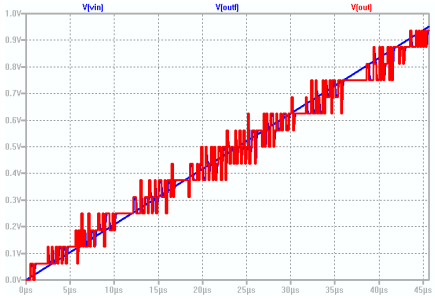


Figure 3. Dead zones in a Second-order passive modulator

From figure 3 we see that the dead zones are reduced in Second-order passive modulator compared to dead zones in First-order passive modulator (see figure 2).

Tyler Hansen

6.8 – Verify, using simulations, that the modulator seen in Fig. 6.20 suffers from capacitor mismatch while the one in Fig. 6.22 does not.

I will begin by reproducing the competing topologies in figure 6.8.1:

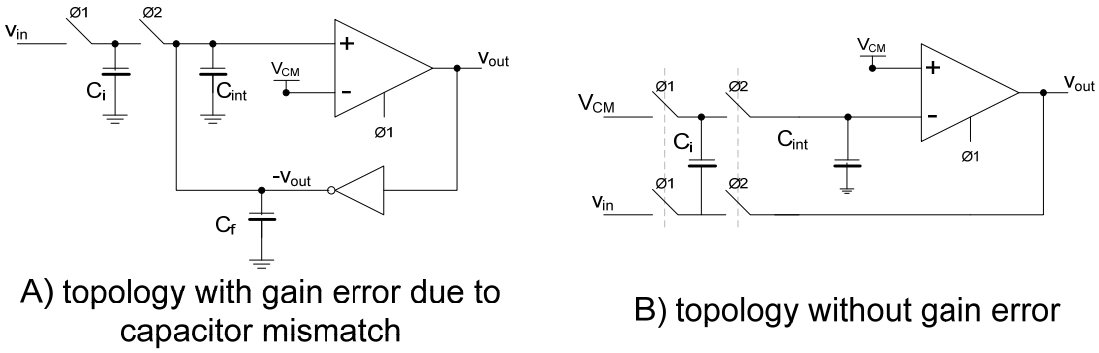


Figure 6.8.1: First-order passive modulator competing topologies.

First let's simulate topology A. We will introduce a mismatch of 10% in each direction for C_i and C_f and display the simulation results in figure 6.8.2.

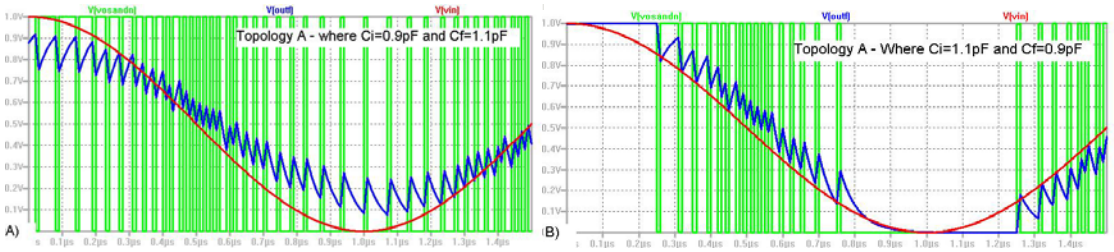


Figure 6.8.2: Back to back simulations of topology A in figure 6.8.1 with everything common except the toggle in capacitor mismatch.

Observing the difference between figure 6.8.2a and 6.8.2b, it is obvious that topology A is not immune to gain error caused by capacitor mismatch. Now let's turn to the simulations of topology B.

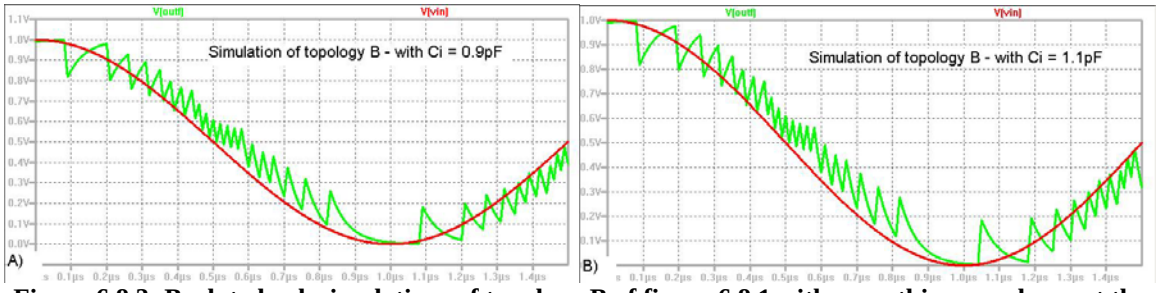


Figure 6.8.3: Back to back simulations of topology B of figure 6.8.1 with everything equal except the toggle in Ci capacitance from 0.9pF to 1.1pF representing a 10% mismatch in either direction.

Unlike the simulations displayed in figure 6.8.2, it is difficult to tell the difference between figure 6.8.3a and 6.8.3b, even though they represent separate simulations run with C_i values of 0.9pF and 1.1pF respectively.

Just for fun, let's push it a little farther. I will now run the same simulations that were run in figure 6.8.3, but with C_i values of 0.75pF and 1.25pF. The results are displayed in figure 6.8.4 below:

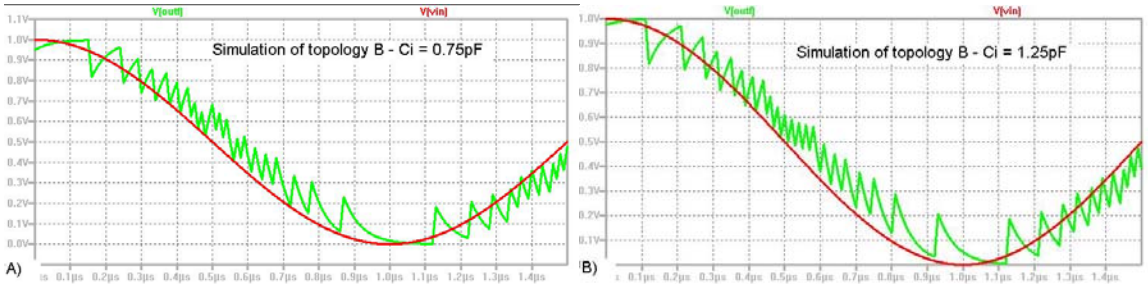


Figure 6.8.4: Back to back simulations of topology B of figure 6.8.1 with everything equal except the toggle in Ci capacitance from 0.75pF to 1.25pF representing a 25% mismatch in either direction.

Magic? No. These results aren't surprising when you consider equation 6.8.1 representing the signal gain:

$$\frac{R_f}{R_i} = \frac{C_i}{C_f}$$ Equation 6.8.1

If we are in effect using the same capacitor for C_i and C_f, it will be difficult *not* to get a gain of 1.

Question 6.9

What is time-interleaved data converter? Why is a time-interleaved converter different from the converter seen in Fig. 6.24?

Solution

As discussed and referenced many times in the text; the quantization noise $\frac{V^2_{LSB}}{12}$ in a data converter is constant and independent of sampling frequency. The PSD of quantization noise on the other hand is given by $PSD_{Qe} = \frac{V^2_{LSB}}{12 f_s}$, from which we can infer that by increasing the sampling rate f_s, we can spread the quantization noise out over a wider frequency range (page 190, fig 5.26). Based on discussion (page 220) if we use multiple path or *K*-paths we can increase the effective sampling from f_s to $f_{s,new} = K_{path} \cdot f_s$ so the new PSD of the quantization noise is given as $PSD_{Qe} = \frac{V^2_{LSB}}{12 \cdot K_{path} \cdot f_s}$. Thus just considering the averaging by *K* path the *SNR* of data converter is increased. Figure 1 shows the simple block diagram of data converter implemented with *K*-path.

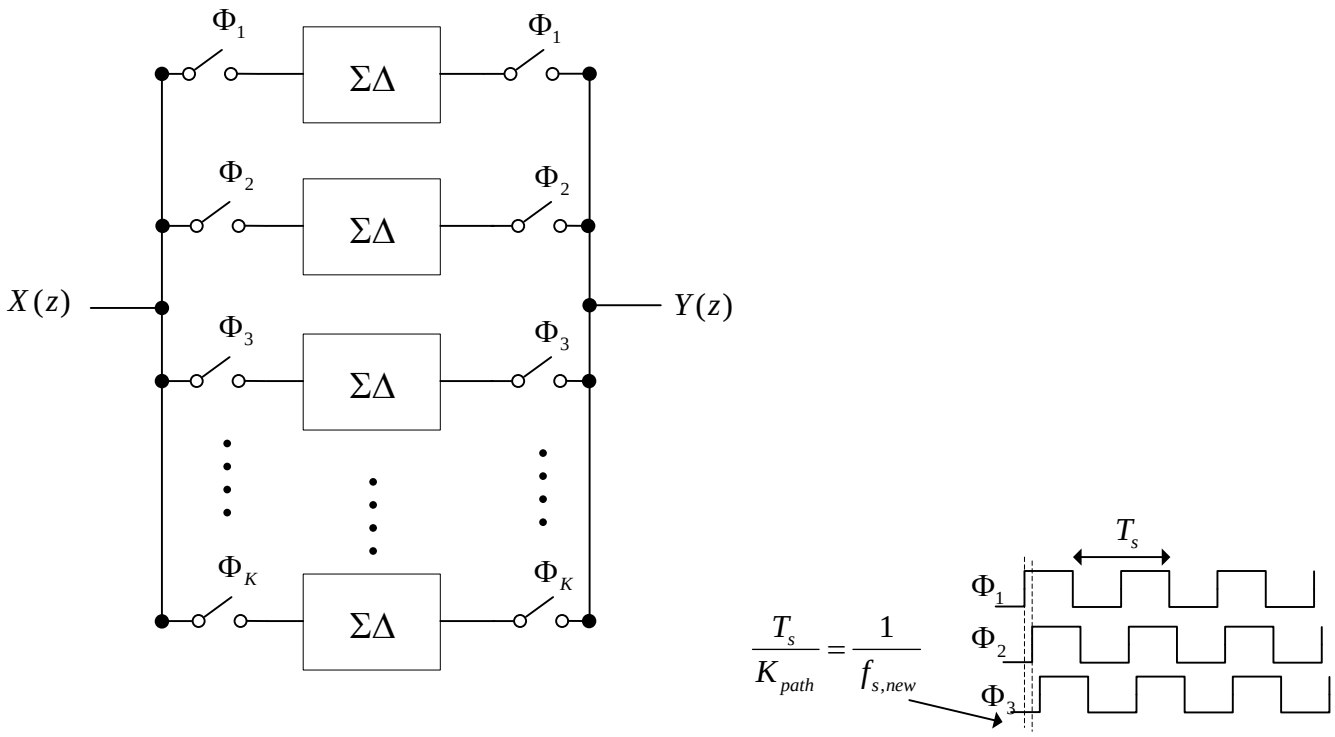


Figure.1 *K*-path delta sigma modulator or time interleaved delta-sigma modulator

In the topology above the *K* – path configuration can also be used with other Nyquist rate data converters (e.g. flash or pipeline) but all of them would have to meet the Bennett's criteria. Each block of delta-sigma modulator acts as a individual ADC and data is first manipulated at clock Φ_1 and then after delay of $\frac{T_s}{K_{path}}$, at clock Φ_2 and so on. Thus an effective sampling of $K_{path} \cdot f_s$ is achieved. Institutively we can say that, there is

a time interval between each ADC's responses since the input signal is clocked by each at different times. Thus this *K*-path topology is also referred to as *time interleaved data converter*. For more see page 221.

The data converter topology in Figure 6.24 (page 222) is as shown below

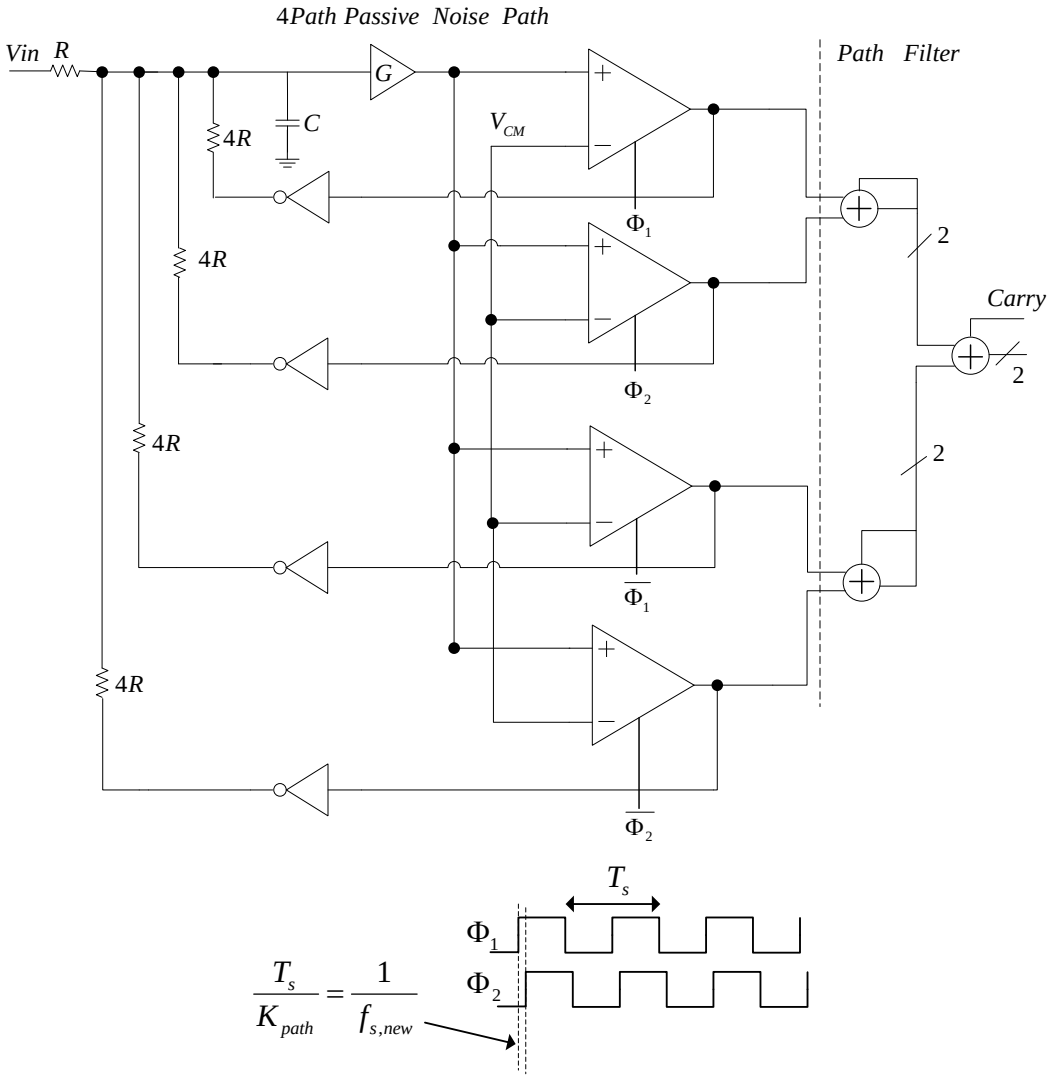


Figure 6.24 Four path passive modulator. It doesn't behave like time interleaved since the integrator is common to all feed back bath.

The above topology is different from the *time interleaved* converter in ways that all the quantizer or comparators are connected to the common output node of op-amp; the outputs (delta) from all the feedback path is summed at single capacitor (sigma) node of the integrator. Thus the A-D conversion is dependent between the *K* paths even though the clocks are polyphase. Advantage of this topology over *time interleaved* is small layout area, lower power and avoiding the path mismatch as in Figure 1 topology.

6.10. Show the details of how to derive the transfer function of the path filter seen in Fig 6.24.

Sol. The K-path passive modulator followed by K-path filter is shown in Figure 1. The clock phases of $Ø_1$, $Ø_2$ is shown in Figure 2.

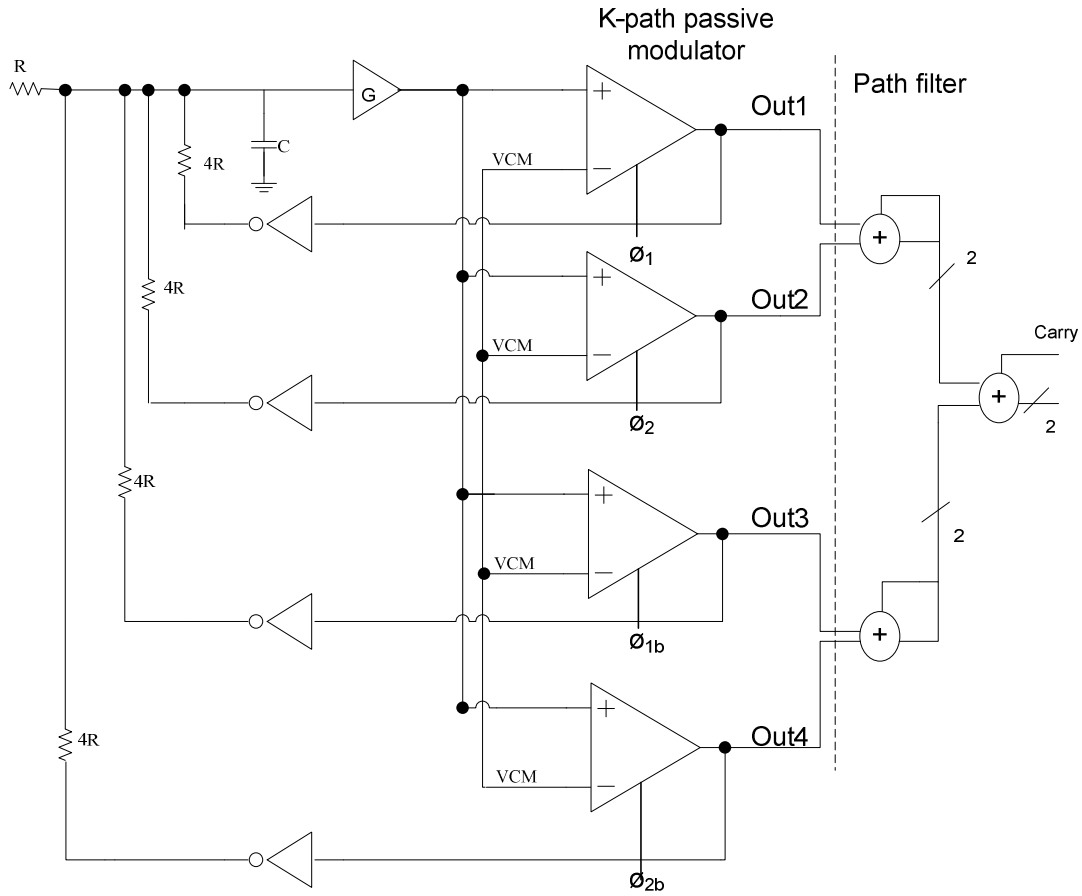


Figure 1. K-path passive modulator (K=4) followed by path filter

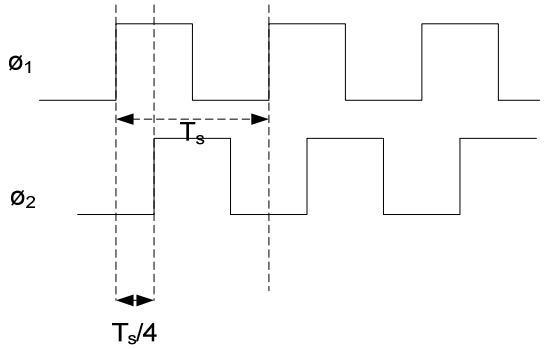


Figure 2. Clocks $Ø_1$, $Ø_2$. $Ø_{1b,}$ $Ø_{2b}$ are inverted versions of $Ø_1$, $Ø_2$

The clock period of $Ø_1$, $Ø_2$ is given by T_s. The comparators in the passive modulator are clocked at clocking frequency fs with a time delay of $T_s/4$ between each clock. Hence the effective sampling frequency of the 4-path passive modulator becomes $4f_s$. The outputs at the comparators have a delay difference of $T_s/4$ or z^{-1}. We can see that the path filter is 4-bit adder with transfer function given by

$$H(z) = \sum_{K=0}^{3} z^{-K} \tag{1}$$

$$H(z) = 1 + z^{-1} + z^{-2} + z^{-3} \tag{2}$$

The width of bits at output of the path filter is $\log_2 K+1$. In this case K=2 and hence output is 3-bit wide.

Multiply numerator and denominator of H (z) by $1 - z^{-1}$ we get

$$H(z) = \frac{1 + \cancel{z^{-1}} + \cancel{z^{-2}} + \cancel{z^{-3}} - \cancel{z^{-1}} - \cancel{z^{-2}} - \cancel{z^{-3}} - z^{-4}}{1 - z^{-1}} \tag{3}$$

H (z) reduces to

$$H(z) = \frac{1 - z^{-4}}{1 - z^{-1}} \tag{4}$$

In general the transfer function for the path filter for a K-path passive modulator is given by

$$H(z) = \frac{1 - z^{-K}}{1 - z^{-1}} \tag{5}$$

Avinash Rajagiri
Spring 2009

6.11) **Repeat question 6.7 if an active integrator, Fig. 6.28, is used in place of the passive integrator**.

6.7) In your own words explain why dead zones in the second-order passive modulator seen in Fig. 6.17 are less of a problem than the first-order modulator seen in Fig. 6.4a.

Sol) Shown below are figures of passive integrator and active integrator connected to a comparator.

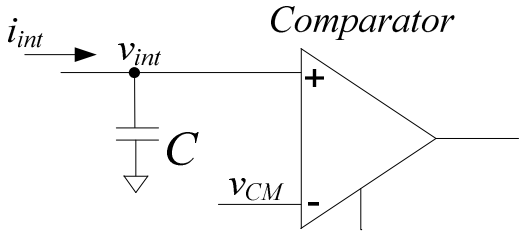


Figure 1: Passive Integrator connected to a comparator

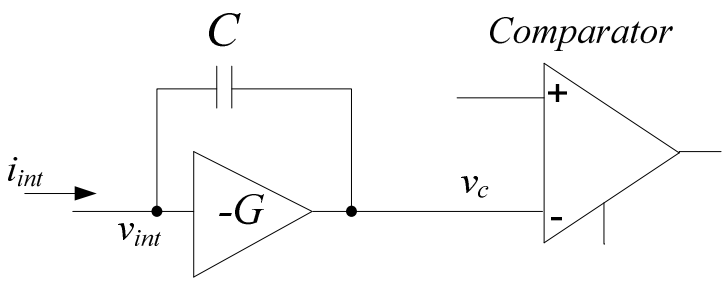


Figure 2: Active integrator connected to a comparator (Fig. 6.28 in Book)

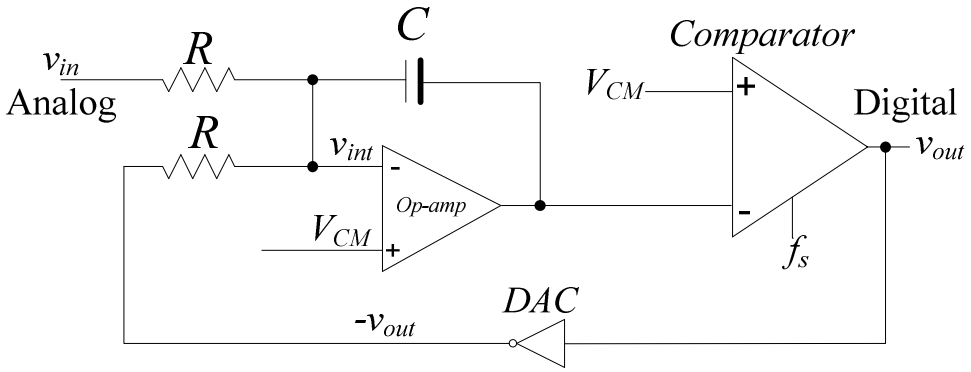


Figure 3: Noise - Shaping modulator with an active integrator

The purpose of the feedback in the NS modulator circuit is to hold the positive terminal (Fig.1) of the comparator equal to V_{cm} voltage, while the negative terminal is at V_{cm} too. Suppose that the input voltage connected to the comparator through the integrator circuit (capacitor) changes, the voltage at the positive terminal of the comparator (v_{int}) does not change instantaneously as there is a RC time associated with this voltage. During this time, it is possible for the average current being supplied from the input equals the fed back current and the output of the comparator does not change. The comparator does not make a decision during this time and the output remains constant, causing *dead zones*.

These dead zones can be eliminated by replacing the passive integrator with an active integrator (See Fig. 2). By using an active integrator (Op-amp with a feedback capacitor), we basically introduced a gain stage before our comparator.

Let's see how using an active integrator eliminates dead zones. Using the LTSpice examples from cmosedu.com, let's simulate Fig6_31.spi, which is a Noise-shaping modulator with an active integrator, as seen in Fig. 3.

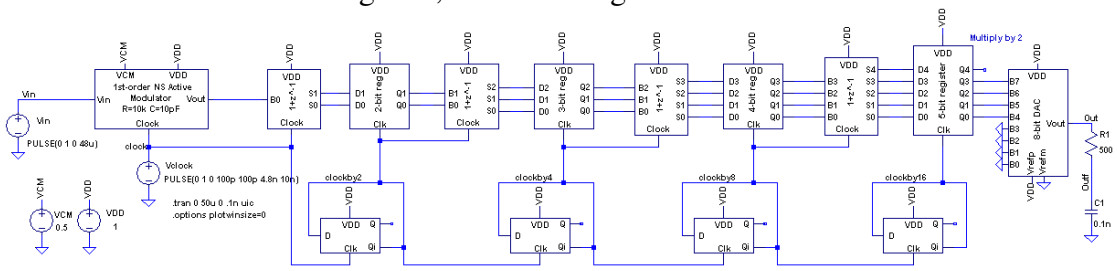


Figure 4: Circuit implementation of 1st order NS Active Modulator with a $(1+z^{-16})$ digital filter

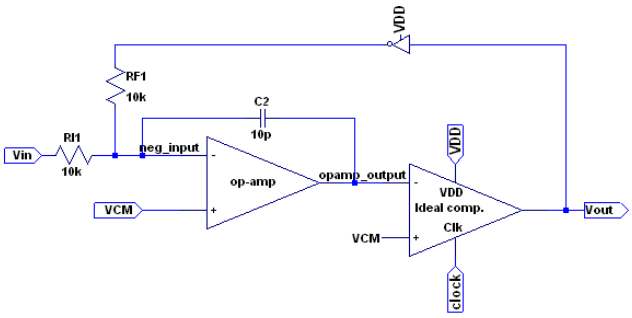


Figure 5: NS modulator with Active integrator used in Fig. 4

The op-amp is going to hold both its terminals at a constant potential of V_{cm}. Any minor change in the input voltage (connected to the negative terminal of the op-amp Fig. 3) is reflected at the V_{int} node instantaneously (or *neg_input* terminal in Fig. 5). Then, the output of the amplifier is an amplified version of the minor difference in its positive and negative input terminals. Shown below is the V_{int} node being held constant by the op-amp in Fig. 6.

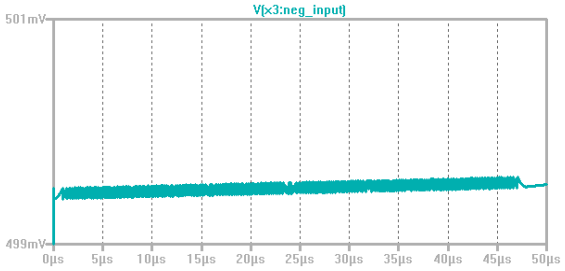


Figure 6: V_{int} node being held constant by the op-amp

The amplified version of this minor wiggle in the input voltage is shown in Fig. 7.

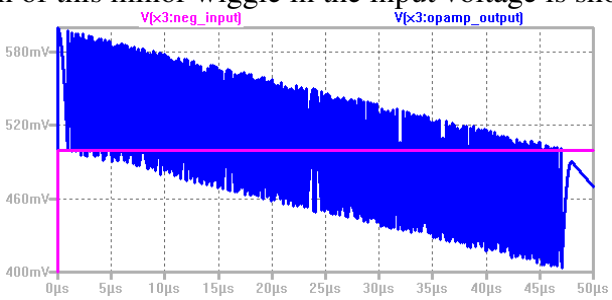


Figure 7: Plot showing the output of the op-amp change due to the wiggle on its input

As the output of the op-amp is connected as input into the negative terminal of the comparator while its positive terminal is held at V_{cm}, there is going to be a significant voltage difference between the input terminals of the comparator. Now, it will be easy for the comparator to resolve this huge difference at its input terminals. Therefore, using this topology we avoid the situation where the input terminals of the comparator are so close to each other that it is hard for the comparator to take a decision. Therefore, using the active integrator configuration, we can eliminate dead zones as seen in the figure below.

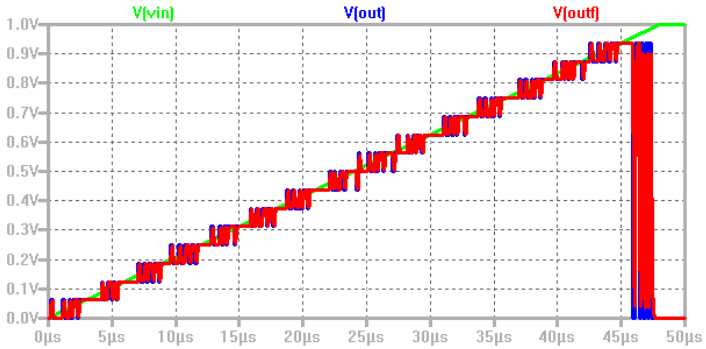


Figure 8: Output of the DAC connected to the NS modulator with active integrator seen in Fig. 4. Shows the output is always valid and deadzones are eliminated

6.12 Repeat Ex. 6.5 if K is changed from 16 to 8.

Simulate the operation of the second-order NS modulator in Fig. 6.34 clocked at 100 MHz, with RC = 20 ns, and decimated with a filter having a transfer function

$$\left[\frac{1-z^{-8}}{1-z^{-1}}\right]^2 \tag{1}$$

Estimate the bandwidth, B, of the output signal, the increase in the number of bits N_{inc}, and SNR_{ideal}.

Solution:

The schematic of the second-order NS modulator is shown in Fig. 1.

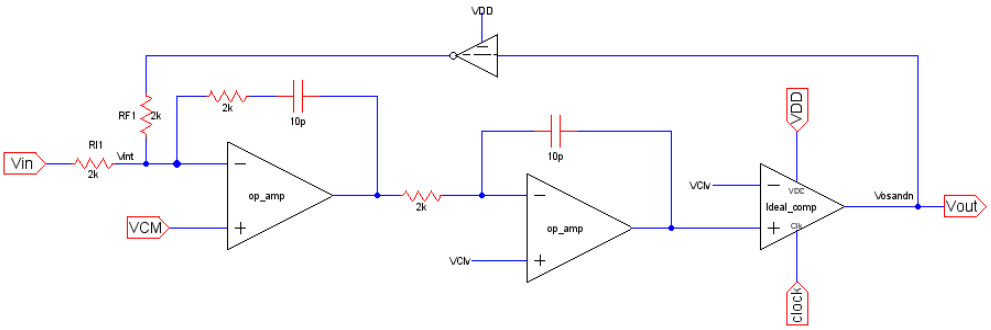


Figure 1 The schematic of the second-order NS modulator.

A filter with a transfer function of

$$\left[\frac{1-z^{-K}}{1-z^{-1}}\right]^L \tag{2}$$

can be implemented by cascading L Sinc-response filters. Specifically, K = 8 and L = 2 in this problem. Fig. 2 shows the frequency responses of this filter.

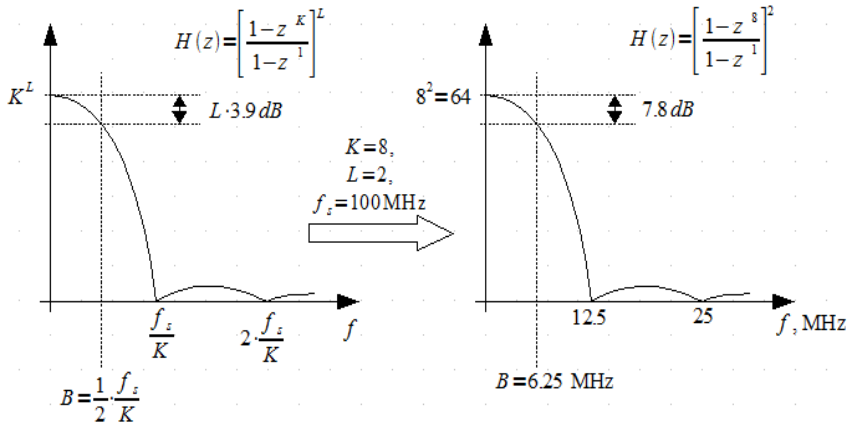


Figure 2 Frequency response of cascaded Sinc-filters

As shown in Fig. 2, the final output clock frequency is 12.5 MHz and the desired signal bandwidth, B, is 6.25 MHz. Using Eqs. (6.79) and (6.80) in [1] and knowing that a 1-bit comparator is used in modulator (N=1), we can estimate the increase in the number of bits

$$N_{inc} = \frac{50\log 8 - 30.10}{6.02} = 2.5 \text{ bits} \tag{3}$$

and

$$SNR_{ideal} = 6.02\,(1+2.5) + 1.76 = 22.83\,\text{dB} \tag{4}$$

Fig. 3 shows the simulation.

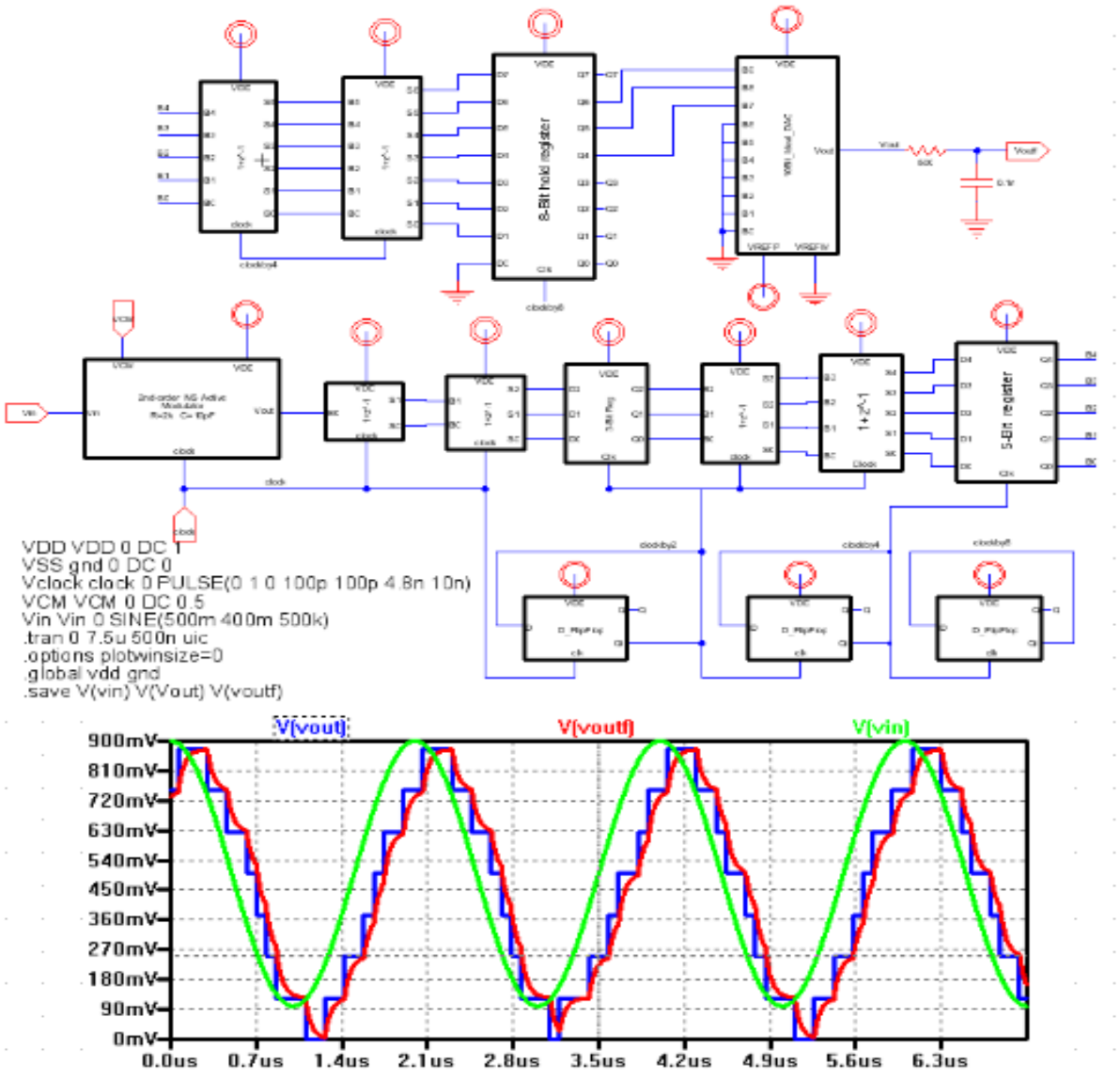


Figure 3 Simulation for K=8 and L=2.

Reference:

[1] R. J. Baker, *CMOS Mixed-Signal Circuit Design, Second Edition*, Wiley-IEEE, 2009.