9.1)

Calucalate and simulate the values of ID and VGS in the Following circuit

$$KPn = 120\frac{\mu F}{V}$$

$$V_{THN} = .8V$$

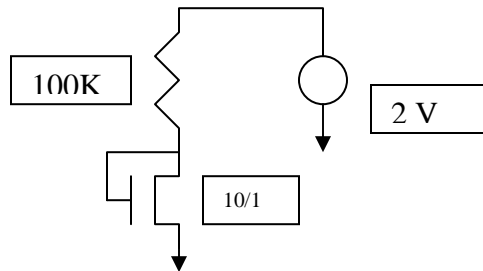$$V_{DS} = 2 - 100k * I_D \Rightarrow I_D = \frac{KPn}{2} * \frac{w}{l} * (V_{GS} - V_{THN})^2$$

$$V_{GS} = V_{DS}$$

$$V_{DS} = 2 - 100k * (ID = KPn/2 * w/l * (V_{DS} - V_{THN})^2)$$

$$V_{DS} = 2 - 60 * V_{DS}^2 + 95 * V_{DS} - 36.4$$

$$V_{DS} = .934V$$

$$I_D = 10.8\mu A$$

Circuit: *** Example 9.5 CMOS: Circuit Design, Layout, and Simulation ***

DC Operating Point ... 100%
vdd = 2.000000e+00
vdd#branch = -1.10055e-05
vdr = 2.000000e+00
vdr#branch = 1.100551e-05
vr = 8.994494e-01

.control
destroy all
run
print all
.endc

.option scale=1u
.op

VDD	VDD	0	DC	2	
VDR	VDD	VDR	DC	0	
R1	VDR	VR	100K		
M1	VR	VR	0	0	NMOS L=1 W=10

```
.MODEL NMOS NMOS LEVEL = 3
+ TOX   = 200E-10     NSUB  = 1E17      GAMMA = 0.5
+ PHI   = 0.7         VTO   = 0.8       DELTA = 3.0
+ UO    = 650         ETA   = 3.0E-6    THETA = 0.1
+ KP    = 120E-6      VMAX  = 1E5       KAPPA = 0.3
+ RSH   = 0           NFS   = 1E12      TPG   = 1
+ XJ    = 500E-9      LD    = 100E-9
+ CGDO  = 200E-12     CGSO  = 200E-12   CGBO  = 1E-10
+ CJ    = 400E-6      PB    = 1         MJ    = 0.5
+ CJSW  = 300E-12     MJSW  = 0.5
*
.MODEL PMOS PMOS LEVEL = 3
+ TOX   = 200E-10     NSUB  = 1E17      GAMMA = 0.6
+ PHI   = 0.7         VTO   = -0.9      DELTA = 0.1
+ UO    = 250         ETA   = 0         THETA = 0.1
+ KP    = 40E-6       VMAX  = 5E4       KAPPA = 1
+ RSH   = 0           NFS   = 1E12      TPG   = -1
+ XJ    = 500E-9      LD    = 100E-9
+ CGDO  = 200E-12     CGSO  = 200E-12   CGBO  = 1E-10
+ CJ    = 400E-6      PB    = 1         MJ    = 0.5
+ CJSW  = 300E-12     MJSW  = 0.5

.end
```

Problem9.2

A MOSFET with its drain connected to gate and a current flowing through it is always in saturation. The current flowing through the MOSFET can be written as:

$$I_D = \frac{1}{2} * KPn * \frac{W}{L} * (V_d - V_{thn})^2 \quad \ldots\ldots\ldots\ldots\ldots..(1) \text{ Also,}$$

$$I_D = \frac{2 - V_d}{100K} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots...(2)$$

Substituting the values of KPn =120uA/V, V_{thn} =0.8V(from table 9.1) and W=L=10um, and equating equations (1) and (2), the following quadratic equation is obtained.

$$\frac{1}{2} * (120uA/V) * \frac{10}{10} * (V_d - 0.8)^2 = \frac{2 - V_d}{100K}$$

$\Rightarrow \quad 6V_d^2 - 8.6V_d + 1.84 = 0$

$\Rightarrow \quad$ Values of V_d = 0.2617V or 1.17V.

$\Rightarrow$

At V_d= 0.2617V, the MOSFET is not in saturation.

Therefore V_d =1.622V.Corresponding value of I_D =8.3uA (from eq. (2)).

Simulated values are:

V_d=1.215V and I_D=7.847uA.

```
*Circuit spice scripts.
.options scale=1u
. Control
Destroy all
Run
Print all
.endc

*Basic circuit net list
m1    d    d    0  0  nmos l=10 w=10

R1      vdd    d    100k

Vdd    vdd    0      DC    2

. op
```
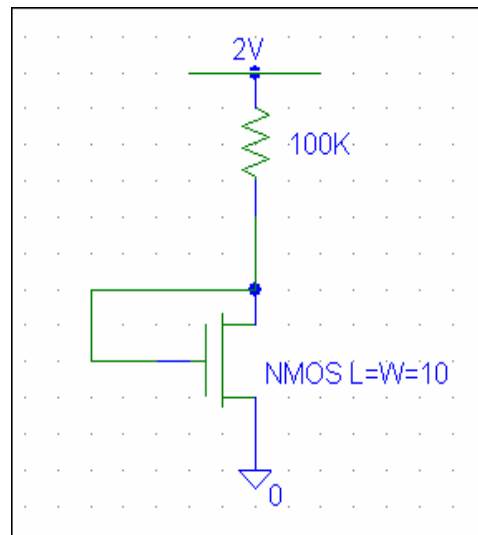
Problem 9.3:-

Calculate and simulate the values of I_D and V_{SG} in the following circuit (use long-channel process information given in table 9.1).
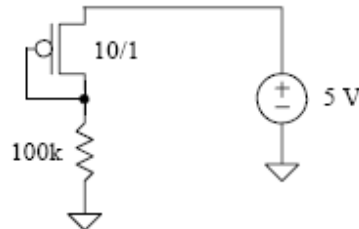

Figure 9.39 Circuit used in Problem 9.3

Solution:-

The above PMOS is gate-drain connected. It will be in *saturation* if $V_{SG} \geq V_{THP}$.

We know for saturation, $I_D = \dfrac{KP_p}{2} \dfrac{W}{L} (V_{SG} - V_{THP})^2$

$$I_D = \frac{40}{2} \frac{\mu A}{V^2} \frac{10}{1} (V_{SG} - 0.9)^2 \qquad \rightarrow (1)$$

Also by KVL, $I_D = \dfrac{(5 - V_{SG})}{100k} \qquad \rightarrow (2)$

Equating (1) and (2), $\dfrac{(5 - V_{SG})}{100k} = \dfrac{40}{2} \dfrac{\mu A}{V^2} \dfrac{10}{2} (V_{SG} - 0.9)^2$

By solving the above quadratic equation, we get two values for V_{SG} *(1.33V or 0 .42v).* As the MOSFET is in *saturation region,* current I_D flows in the circuit if $V_{SG} \geq V_{THP}$.

Therefore, $[\mathbf{V_{SG} = 1.33v}]$ & $[\mathbf{I_D = 36.7 \mu A}]$

Spice Netlist:-

```
**Problem#9.3
.control
destroy all
run
print all
.endc
.option scale=1u
.op
VDD     VDD     0       DC      5

R1      VD      0       100K
M1      VD      VD      VDD     VDD     PMOS L=1 W=10
```

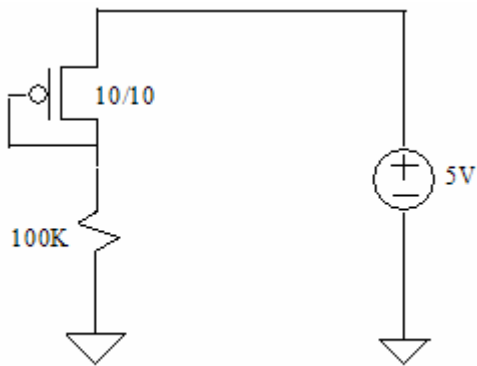*Simulation Results:-*
DC Operating Point ... 100%
vd = 3.713491e+00
vdd = 5.000000e+00
vdd#branch = -3.71349e-05
Vsg = 1.286509e+00

```
vds        -1.2865
vbs         0.
vth      -834.8123m
vdsat    -345.5119m
beta      396.4747u
gam eff   521.2973m
gm        147.9632u
gds         2.3812u
gmb         0.
cdtot       2.0237f
cgtot      13.4667f
cstot      11.2084f
cbtot     234.5729a
cgs        11.2084f
cgd         2.0237f
```

Problem 9.04

Since the above figure is a gate drain connected mosfet and current is flowing its operating in saturation region.

Using KVL
$5-I_D.100k = V_{SG}$
$5-K_{PP}.W/2L.(V_{SG}-V_{THP})^2 . 100K = V_{SG}$;where $K_{PP}=40uA/V^2$, $V_{THP}=0.9V$

solving for V_{SG} we have $V_{SG} =2.1v$ and $–0.8v$,since mosfet is in saturation therefore $V_{SG}=2.1v$
$I_D= K_{PP}.W/2L.(V_{SG}-V_{THP})^2$

Solving for I_D with $V_{SG}=2.1v$ results in $I_D =28.8uA$

Spice simulations
**Problem 9.04
.control
destroy all
run
let vsg=vdd-vd1
print vd1
print vsg
print mag(vdd#branch)
.endc
.option scale=1u
M1 vd1 vd1 vdd vdd PMOS W=10 L=10
Vdd vdd 0 DC 5
R1 vd1 0 100k
*.dc Vdd 0 5 1m
.op

Results:
DC Operating Point ... 100%
vd1 = 2.732722e+00
vsg = 2.267278e+00
mag(vdd#branch) = 2.732722e-05

Problem 9.5:-

Calculate I_D, V_{DS}, and estimate the small-signal resistance looking into the drain of the MOSFET in the following circuit.
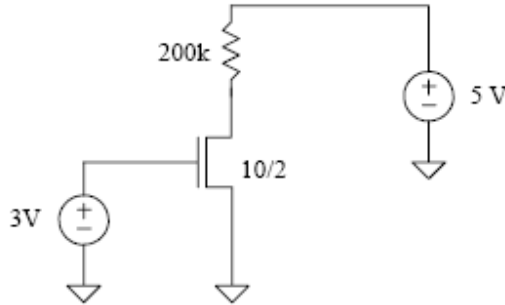

Figure 9.40 Circuit used in Problem 9.5

Solution:-

From the above figure, the gate overdrive voltage is high and the resistor value is also large. It is a good indication that the transistor may be in *triode* (because even if a small current flows in the circuit, the voltage drop across the resistor is high). So let's start with the assumption that the MOSFET is in triode.

$$I_D = KP_n \frac{W}{L}\left[(V_{GS} - V_{THN})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$I_D = 120\frac{\mu A}{V^2}\frac{10}{2}\left[(3-0.8)V_{DS} - \frac{V_{DS}^2}{2}\right] \longrightarrow(1)$$

But, $I_D = \dfrac{(5-V_{DS})}{200k} \longrightarrow(2)$

From (1) and (2), $\dfrac{(5-V_{DS})}{200k} = 120\dfrac{\mu A}{V^2}\dfrac{10}{2}\left[(3-0.8)V_{DS} - \dfrac{V_{DS}^2}{2}\right]$.

By solving the above quadratic equation, we get two values for V_{DS} *(4.39V or 19mv).* As the MOSFET is in *triode region,* $\left[\mathbf{V_{DS} = 19mv}\right]$ and $\left[\mathbf{I_D = 24.9\mu A}\right]$.

As the MOSFET is in *triode* region, the small signal resistance looking into the drain of the MOSFET will be its *channel resistance*.

$$R_{ch} \approx \frac{1}{KP_n \dfrac{W}{L}(V_{GS} - V_{THN})}$$

$$\Rightarrow \left[\mathbf{R_{ch} = 757.5\Omega}\right]$$

9.5 & 9.6 Simulations

9.5)   DC operating conditions

DC Operating Point ... 100%
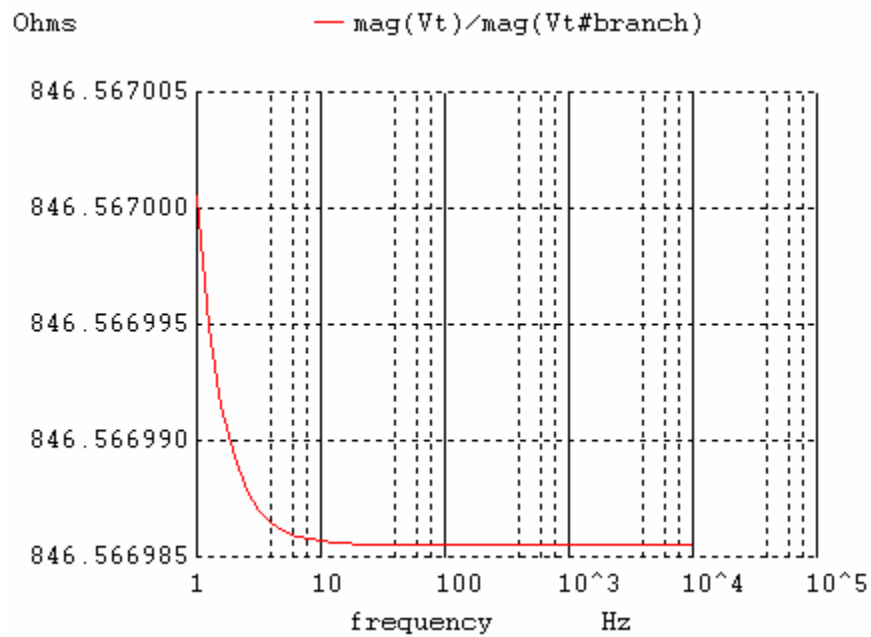V_{DS}=d1 = 2.091701e-02
g1 = 3.000000e+00
vdd = 5.000000e+00
I_D= ABS(vdd#branch) = 2.48954e-05
vg1#branch = 0.000000e+00
vt = 0.000000e+00
vt#branch = 0.000000e+00

9.6) Small signal resistance looking into the drain

R_{Ch} =846 Ohms from simulations.

```
* SPICE command scripts

.control
destroy all
run
 print all
* plot VD1#branch

.endc


Vdd Vdd 0 DC 5.0


* ======================================
M11 d1 g1 0 0 nmos W=10 L=2
R1 d1 Vdd 200k
Cbig d1 Vt 1
Vt Vt 0 DC 0 AC 1m
VG1 g1 0 DC 3.0




* ======================================
* .AC DEC 10 1 10K
.options scale=1u
* ABSTOL=1u VNTOL=1mv RELTOL=0.01
 .op



* Level 3 models
*
* 1 um models created by RJB. These models are for educational purposes only! They are *not*
* extracted from actual silicon.
*
* Don't forget the .options scale=1u if using an Lmin of 1
* 1<Ldrawn<200   10<Wdrawn<10000 Vdd=5V

.MODEL NMOS NMOS LEVEL  = 3
+ TOX   = 200E-10       NSUB  = 1E17         GAMMA  = 0.5
+ PHI   = 0.7         VTO   = 0.8         DELTA  = 3.0
+ UO    = 650         ETA   = 3.0E-6       THETA  = 0.1
+ KP    = 120E-6        VMAX  = 1E5          KAPPA  = 0.3
+ RSH   = 0           NFS   = 1E12         TPG    = 1
```
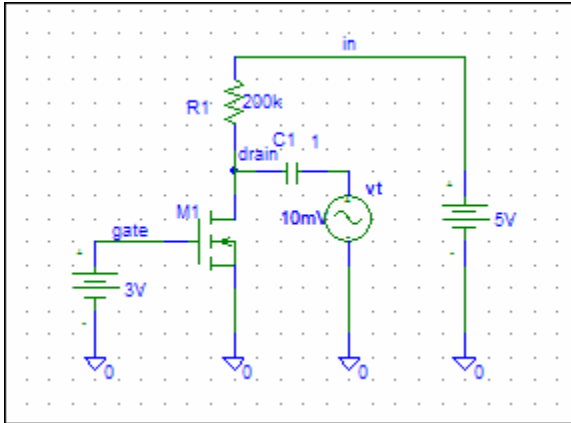
```
+ XJ     = 500E-9        LD     = 100E-9
+ CGDO  = 200E-12      CGSO  = 200E-12      CGBO  = 1E-10
+ CJ     = 400E-6       PB     = 1           MJ     = 0.5
+ CJSW  = 300E-12       MJSW  = 0.5
*
.MODEL PMOS PMOS LEVEL  = 3
+ TOX   = 200E-10       NSUB  = 1E17          GAMMA  = 0.6
+ PHI   = 0.7           VTO   = -0.9          DELTA  = 0.1
+ UO    = 250           ETA   = 0             THETA  = 0.1
+ KP    = 40E-6         VMAX  = 5E4           KAPPA  = 1
+ RSH   = 0             NFS   = 1E12          TPG    = -1
+ XJ    = 500E-9        LD    = 100E-9
+ CGDO  = 200E-12      CGSO  = 200E-12      CGBO  = 1E-10
+ CJ    = 400E-6        PB    = 1             MJ     = 0.5
+ CJSW  = 300E-12       MJSW  = 0.5

.end
```
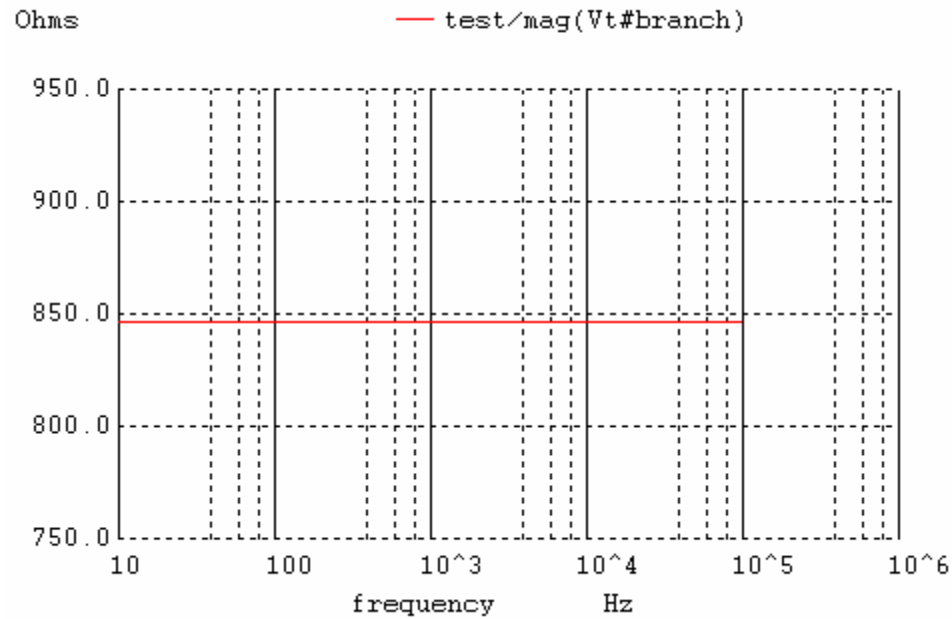
Problem 9.6

To determine the small signal resistance we can run an AC analysis in spice and then plot
the ratio of the drain voltage divided by the current through the 10mV AC source "vt".
We sweep the frequency from 10Hz to 1MHz. The netlist for this circuit is shown below.
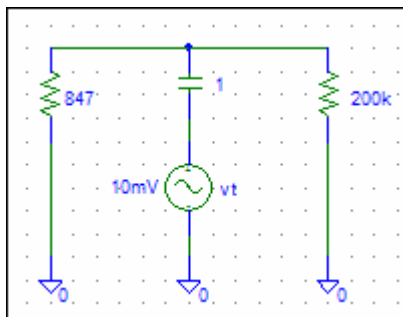
```
Problem 9.6
.opt scale=1u
.control
destroy all
run
plot test/I(Vt)
plot I(Vt)
plot I(Vin)
.endc
.ac     DEC   10      100    1MEG
Vin    in      0       DC=5
Vg     gate    0       DC=3
Vt     test    0       DC=0  AC=10m
C1     drain   test    1
R1     in      drain   200k
M1     drain gate      0 0     nmos L=2.00 W=10.00
.include C:\ 1u_models.txt
```

The first plot is of the v_d/i_d and is shown in the plot below.

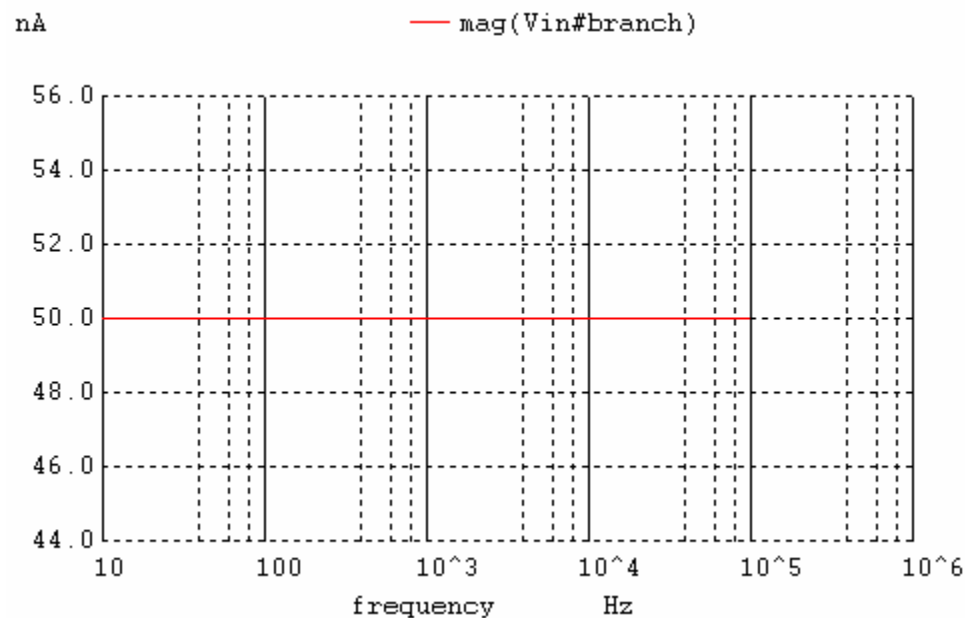Looking at the plot we can see that the small signal resistance is 847 Ω.

To determine how the 200kΩ resistor effects the circuit, we can see that the 200kΩ resistor is in parallel with the small signal resistance when we do AC analysis.

Lets look at how much current is flowing through the capacitor branch. This is shown in the plot below.

There is about 11.8 uA flowing through the capacitor. Now lets look at how much current is flowing through the 200kΩ branch

There is about 50nA flowing through the 200kΩ resistor. The current through the 200kΩ resistor is much smaller than the current flowing through the capacitor. Thus we can neglect the effect of the 200kΩ resistor to the current through the capacitor.
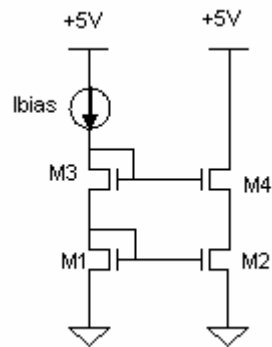
Problem #9.7

Figure 9.42

When Ibias is increased, VS3 and VGS3 increase. When VGS3 is increased, VGS4 also
increases because their gates are tied together. When VGS increases, the Drain to Source
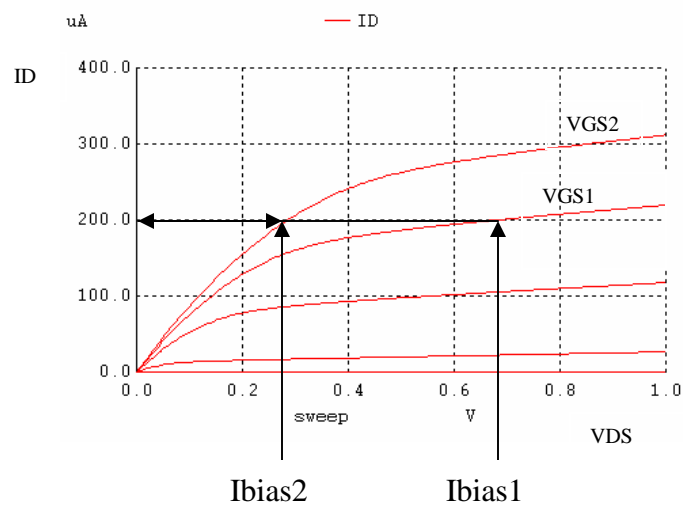Voltage decreases, as illustrated below in Figure 9.42.A.   Therefore VDS4 decreases.
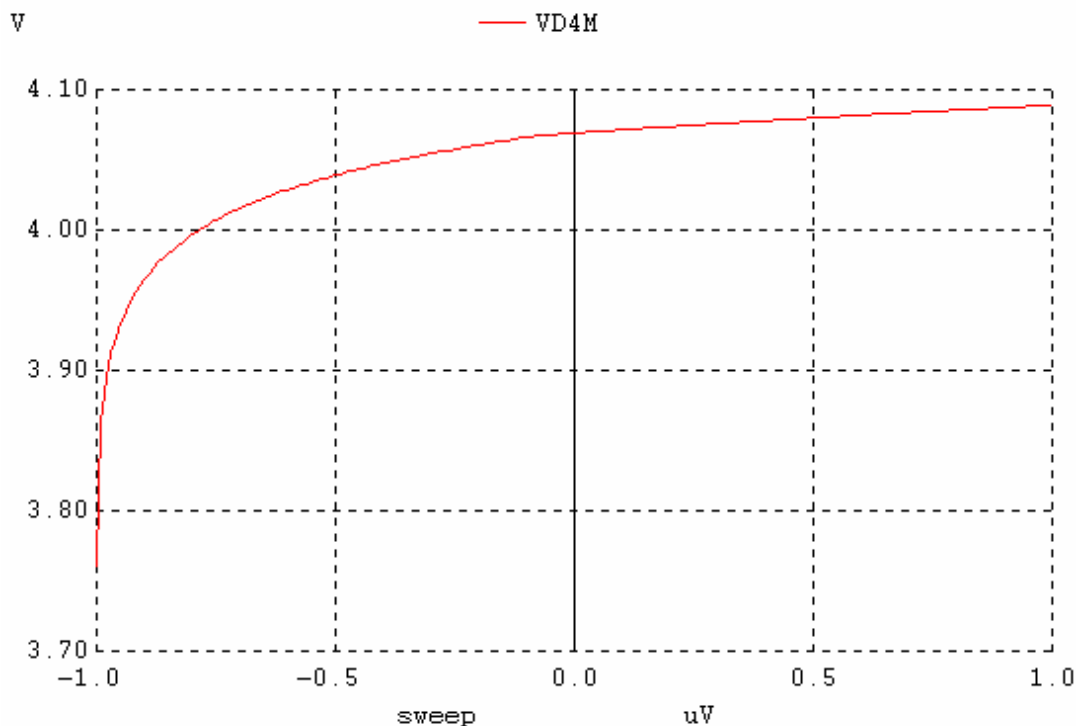

Figure 9.42.A.

9.8.) Describe qualitatively what happens if we steal or inject current at the point indicated in Fig 9.43. How does this affect the operation of M1 and M2? Verify your answer with SPICE. (See Fig 9.43 for circuit schematic).
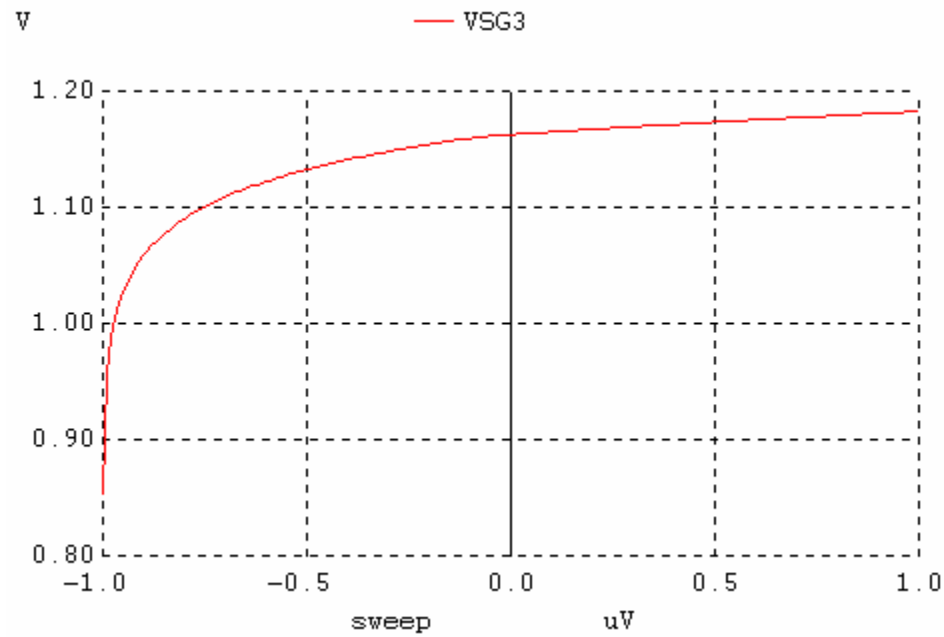
Solution (by Robert J. Hanson, CNS):

We will use a long channel model for this problem.

Since the gates of M2 and M4 are tied together and the sources of M2 and M4 are tied together, VSG2=VSG4. Additionally, since we will assume a current of 1µA for Ibias at the drain of M1, that current must flow through both M1 and M2, as well as M4 and M3. Hence VSD2=VSG2=VSG4=VSD4 and VSD1=VSG1=VSG3 since all the PMOS devices are assumed to be sized the same (we will assume W/L=30/2 for the simulations).
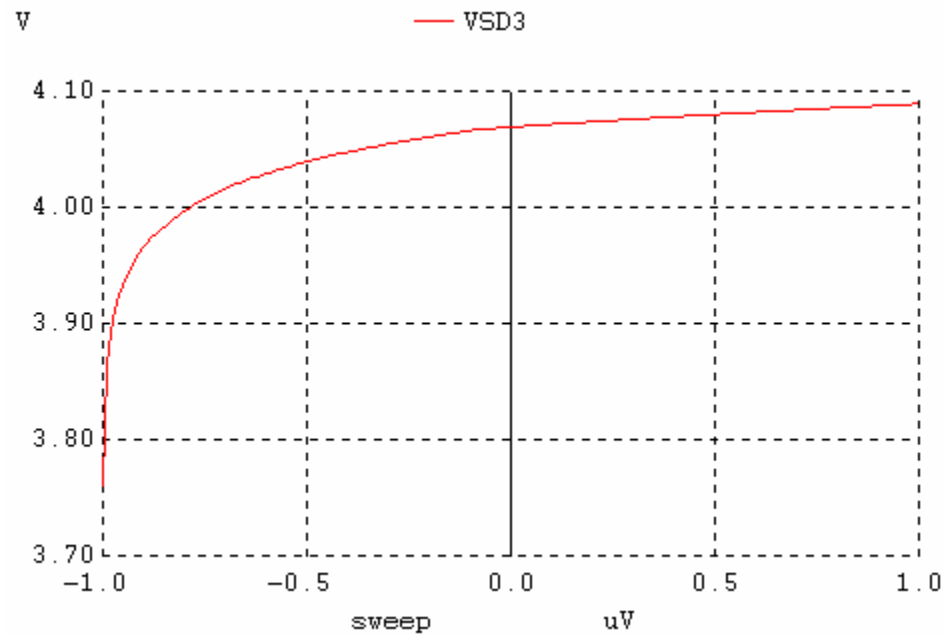
When current is stolen from the drain of M4, it causes the drain voltage node (here called VD4M, which is also the source voltage of M3, VS3) to decrease which results in a decreased VSD3 (i.e. M3 begins to lose its ability to pass current, VSG3 also goes down). If 1 µA of current is stolen, M3 completely shuts off and all of the 1 µA flows through M4 on that side of the circuit. (Note that the x-coordinate should be labeled in units of µA as it is a sweep of -1µA of injected current to +1µA of injected current).
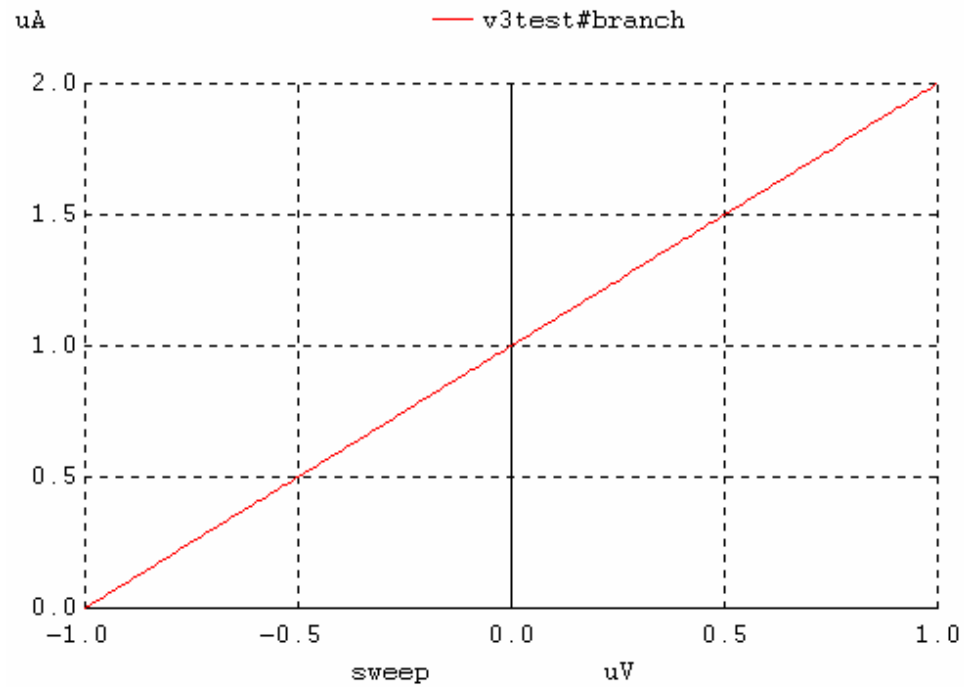

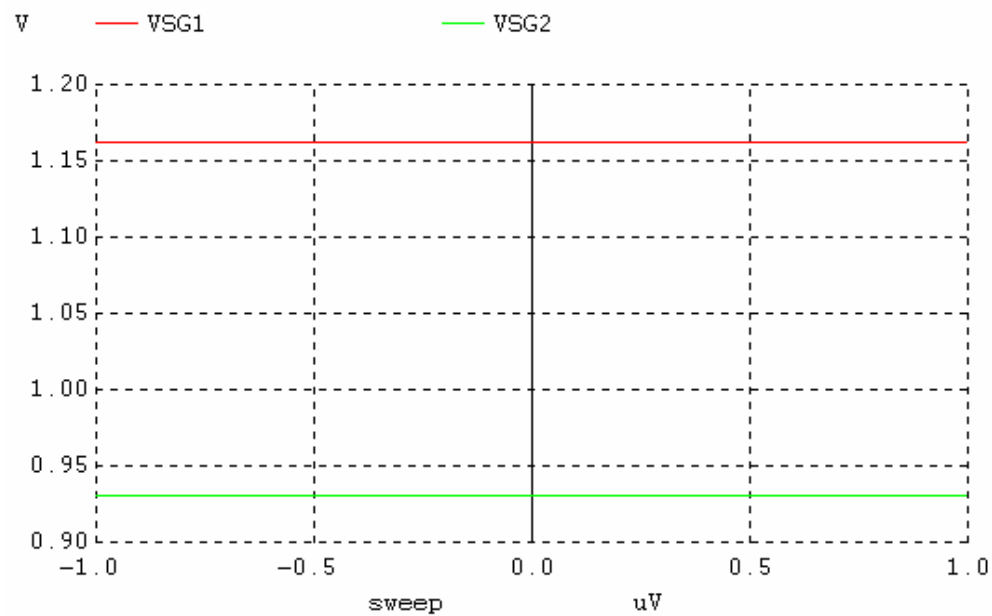In the plot below VSG3 decreases due to VS3 decreasing when current is stolen from the node at VD4M.

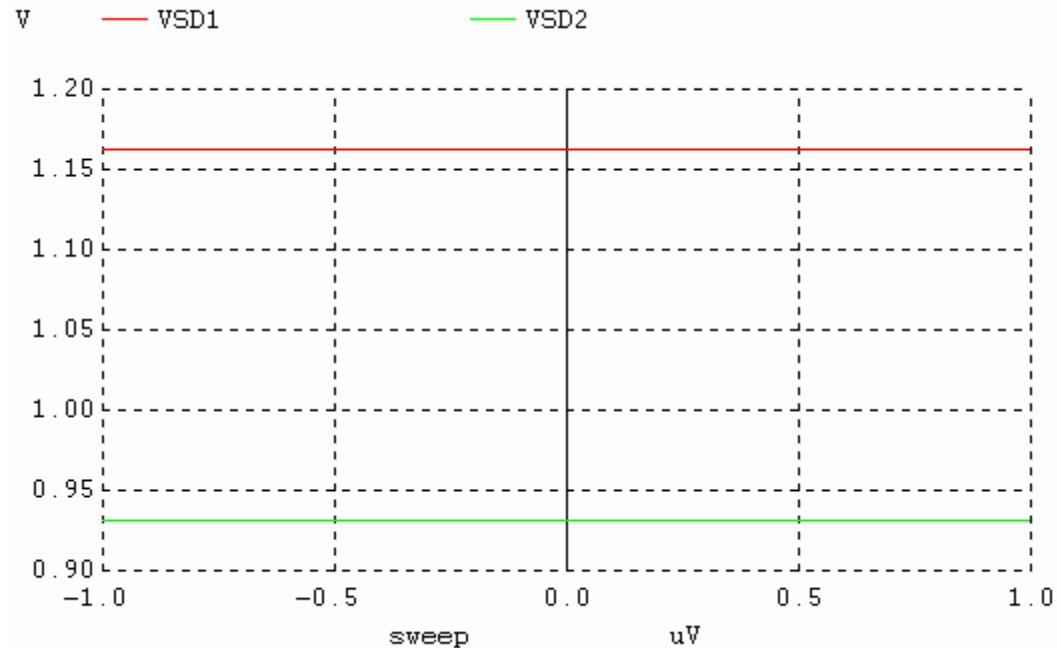VSD3 is actually the same as VD4M since VSD3=VS3-VD3=VS3-0=VD4M

Conversely, if current is injected into the node mentioned above, it will cause the voltage VD4M to increase to the point where the current flowing through M3 will be 2μA when the injected current has reached 1μA (1μA provided by Iinject and 1μA by M4).

The simulation results below show what happens to VSG1 and VSG2 due to Iinject, note that they do not change.

Similar results are obtained for VSD1 and VSD2, since current and VSG is constant, VSD must also be constant.

The SPICE NetList for this simulation is provided below with the Long Channel Simulation Model that was used:

```
*** Problem 9.8 Solution ***
.control
destroy all
run

let VSG1=VG2-VG1
let VSG2=VDD-VG2
let VSG3=VD4M-VG1
let VSG4=VDD-VG2

let VSD1=VG2-VG1
let VSD2=VDD-VG2
let VSD3=VD4M-V3S
let VSD4=VDD-VD4

plot vmeas#branch
plot v3test#branch
plot VD4M
plot VSG1
plot VSG2
plot VSG3
plot VSG4
plot VSD1
plot VSD2
plot VSD3
plot VSD4
plot VG1
```

```
plot VG2
*print all
.endc
.option scale=1u
*.OP
.dc        Iinject    -1uA      1uA        10nA

VDD    VDD    0        DC       5
Ibias   VG1    0        DC       1u
Iinject  0       VD4M  DC       1u
VMEAS VD4    VD4M  DC       0
VTEST2          VG2    VG2M   DC       0
V3TEST          V3S     0        DC       0

M1      VG1    VG1     VG2M   VDD      PMOS L=2 W=30
M2      VG2    VG2     VDD      VDD      PMOS L=2 W=30
M3      V3S     VG1     VD4M   VDD      PMOS L=2 W=30
M4      VD4    VG2     VDD      VDD      PMOS L=2 W=30

.MODEL NMOS NMOS LEVEL  = 3
+ TOX   = 200E-10        NSUB  = 1E17          GAMMA = 0.5
+ PHI   = 0.7          VTO   = 0.8         DELTA = 3.0
+ UO    = 650           ETA   = 3.0E-6        THETA = 0.1
+ KP    = 120E-6        VMAX  = 1E5          KAPPA = 0.3
+ RSH   = 0            NFS   = 1E12         TPG   = 1
+ XJ    = 500E-9        LD    = 100E-9
+ CGDO  = 200E-12       CGSO  = 200E-12       CGBO  = 1E-10
+ CJ    = 400E-6        PB    = 1          MJ    = 0.5
+ CJSW  = 300E-12        MJSW  = 0.5
*
.MODEL PMOS PMOS LEVEL  = 3
+ TOX   = 200E-10        NSUB  = 1E17          GAMMA = 0.6
+ PHI   = 0.7          VTO   = -0.9         DELTA = 0.1
+ UO    = 250           ETA   = 0          THETA = 0.1
+ KP    = 40E-6         VMAX  = 5E4          KAPPA = 1
+ RSH   = 0            NFS   = 1E12         TPG   = -1
+ XJ    = 500E-9        LD    = 100E-9
+ CGDO  = 200E-12       CGSO  = 200E-12       CGBO  = 1E-10
+ CJ    = 400E-6        PB    = 1          MJ    = 0.5
+ CJSW  = 300E-12        MJSW  = 0.5

.end
```

Problem 9.9:-
Using simulations, generate the plot seen in Fig. 9.12 for both NMOS and PMOS devices.

Solution:-

Fig:-Schematics of NMOS and PMOS showing the variation of threshold voltage with respect to their changes in source to body potentials.

For the MOSFETs shown in the above figure, a current source of 1uA is connected at the drain so that the gate overdrive voltage is less. (Then V_{GS} or V_{SG} will be almost equal to the threshold voltage. The plots below show the variation of the *threshold voltage* with respect to the variation of *source to bulk potential* for both NMOS and PMOS devices.
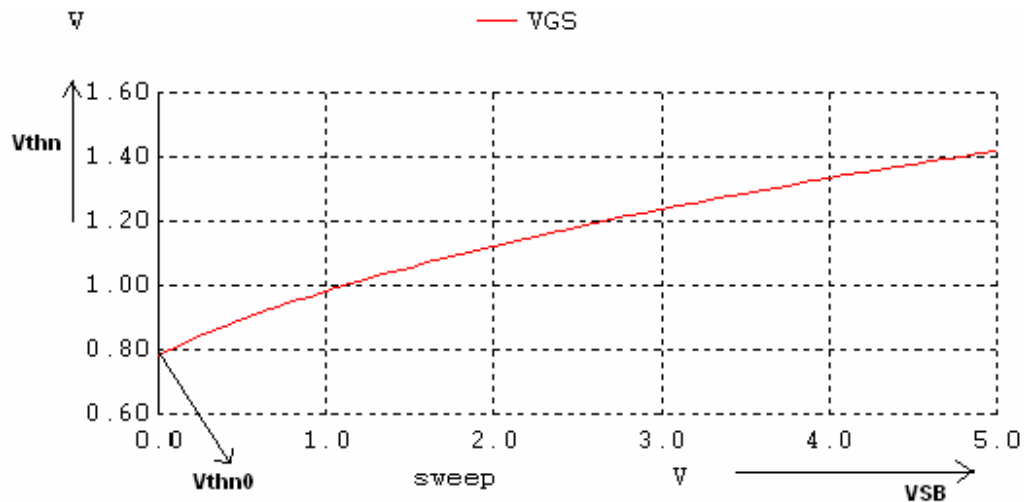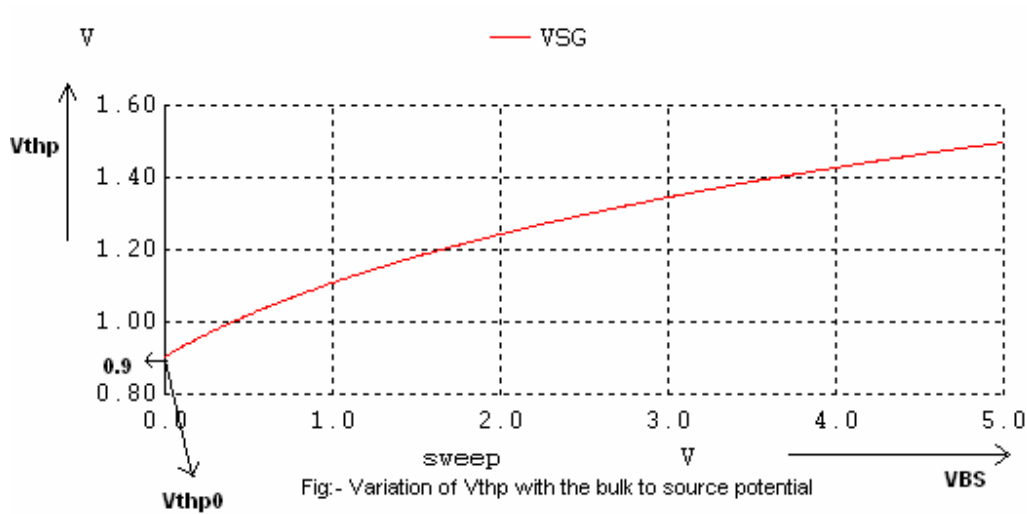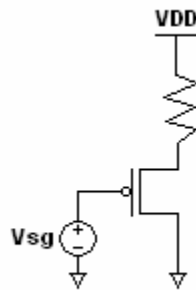

Fig:- Variation in threshold voltage with VSB

Fig:- Variation of Vthp with the bulk to source potential

Spice Netlists:-

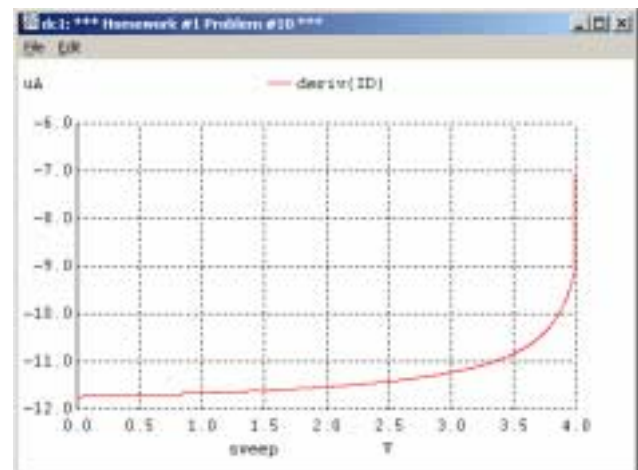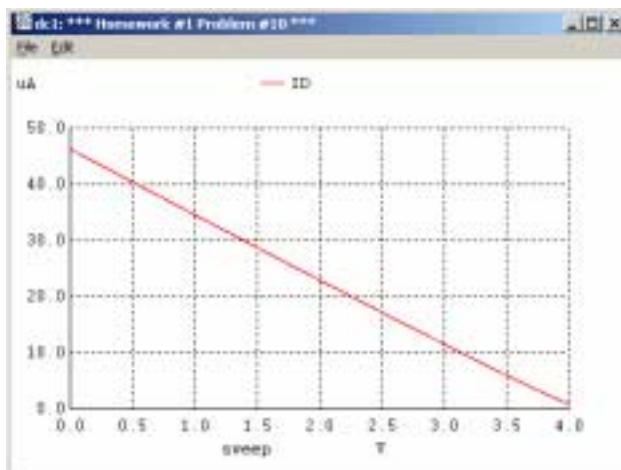| ***NMOS***	***PMOS***
.control	*.control*
destroy all	*destroy all*
run	*run*
plot VGS	*let VSG=VDD-VG*
.endc	*plot VSG*
.option scale=1u	*.endc*
	.option scale=1u
.dc VSB 0 5 .01	
	.dc VBS 0 5 .01
VDD VDD 0 DC 5	
VSB 0 VSB DC 0	*VDD VDD 0 DC 5*
IBIASP VDD VGS DC 1u	*VBS VBS VDD DC 0*
	IBIASP VG 0 DC 1u
M1 VGS VGS 0 VSB NMOS L=1 W=10	*M1 VG VG VDD VBS PMOS L=1 W=10*

9.10) Design a circuit that will linearly convert an input voltage that ranges from 0 to 4V into a current that ranges from roughly 50µA to 0. Simulate the operation of the design showing the linearity of the voltage to current conversion. How does the MOSFET's length affect the linearity?

Solution: For voltage to current conversion we use an inactive, (resistor tied to the source) source follower. With this configuration the source of our PMOS transistor is not held to a fixed voltage so to reduce the source to body potential difference we tie the body of the transistor to the source of the PMOS.

For a quick sizing of the resistor we assume that our V_{thp}, transistor must stay in the saturation region, is approximately 1V which gives us a resistor value of 80k if we are to source 50µA.
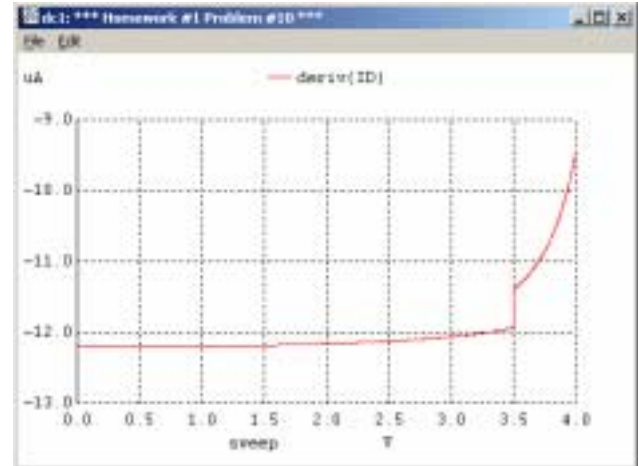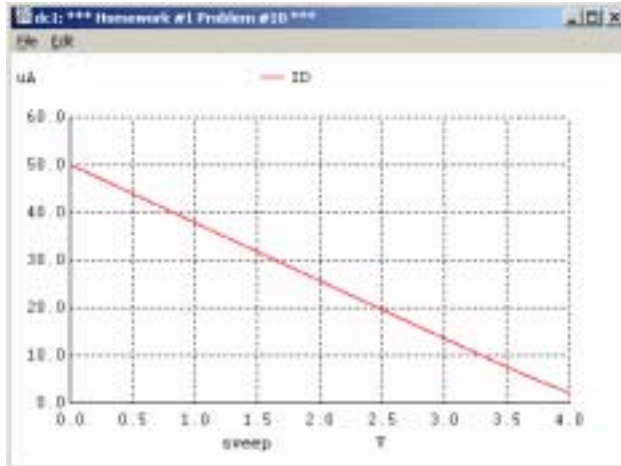
For the sizing of the PMOS let's start with the values in the book and run a simulation to see what our linearity is. We will plot the ID vs VSG and the derivative of ID to see the linearity. W=30µ L=2µ

From the ID plot we see that we are almost at 50uA with the 80k resistor, a value of 74k would have got us to 50uA but we'll leave the 80k for comparison as we change the

sizing of the PMOS to improve linearity. From the plot of the slope of ID we see that we have a variation of around 24%.

To improve the voltage to current linearity we'll push out the point at which the PMOS starts to enter the subthreshold region, we want to keep the PMOS in the saturation or linear region as long as possible. We do this by increasing our W and decreasing our L.

We can clearly see from the log of ID plot that the linearity is almost ideal until around 3.5V, where the MOSFET starts to turn off and enter the subthreshold region. Plotting the voltage at the source of the PMOS confirms this at the swept gate voltage of 3.5V the source voltage is around 4.4V which is right at the expected point where the PMOS enters the subthreshold region.

Problem 9.11:-

Using a PMOS device, discuss and show with simulations how it can be used to implement a 10k resistor. Are there any limitations to the voltage across the PMOS resistor? Explain.
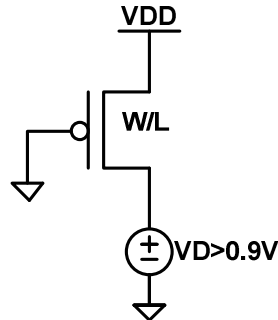
Solution:-

Fig: - PMOS with V_{SG}=5V and V_D>V_{THP}

The MOSFET looks like a resistor when we are using in a triode region. The equation for the channel resistance is given as below

$$R_{ch} = \frac{1}{KP_p \frac{W}{L}(V_{SG} - V_{THP} - V_{SD})}$$. If $V_{SG} - V_{THP} >> V_{SD}$, this equation can be written as,
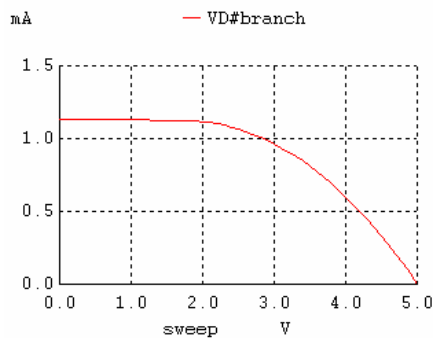
$$R_{ch} \approx \frac{1}{KP_p \frac{W}{L}(V_{SG} - V_{THP})}$$. Use V_{SG} =5V so that the bias is fixed and also gives a

maximum range of $V_{SD,sat}$. Given R_{ch}=10K.

$$R_{ch} = \frac{1}{40\frac{\mu A}{V^2}\frac{W}{L}(5-0.9)} = 10k \Rightarrow \frac{W}{L} = 0.61.$$ If **L=10, then W=61**.

Limitations: - One end of the resistor should be V_{DD} and the other end should be V_D>V_{THP}. Though we V_D>V_{THP}, the simulation shows that V_D>2.5V for better linearity of the resistor.

Simulation:-


```
.control
destroy all
run
plot VD#branch
.endc
.option scale=1u

.dc VD 0 5 .1

VDD VDD 0 DC 5
VD  VD      0 DC 0

M1 VD 0 VDD VDD PMOS L=10 W=61
```

Problem 9.12

Using SPICE (and ensuring the MOSFET is operating in the saturation region with sufficient V_{DS}) generate the i_D vs. v_{GS} curve seen in Fig 9.15. Using SPICE take the derivative of i_D to plot the device's g_m (versus V_{GS}). How does the result compare to Eq. 9.22? Does the level 3 model used in the simulation show a continuous change form sub-threshold to strong inversion?

Solution:

The first step to completing this task is to create a netlist that enables will allow us to supply a specific V_{DS} to the part and allow us to vary V_{GS}. V_{GS} will be our main x-axis variable because g_m is defined as the derivate of I_D with respect to V_{GS}. Therefore, in our netlist we will supply a constant V_{DS} and using a DC sweep vary V_{GS}. V_{DS} should be well above $V_{DS,sat}$ so we will arbitrarily choose 250mV. The .DC statement varies V_{GS} from 0 to 2.5V in 10mV increments.

Netlist
```
.control
destroy all
run
*** DC Analysis ***
let ID=-VDS#branch
let gm=deriv(ID)
let gmcalc=(120E-6*(10/2)*(VGS-0.8))
plot ID gm gmcalc
*plot gm
.endc

.option scale=1u
.DC     VGS    0       2.5      10m

VDS    VDS    0       DC      250m
VGS    VGS    0       DC      0       AC      1
M1     VDS    VGS     0       0       NMOS L=2 W=10

.MODEL NMOS NMOS LEVEL = 3
+ TOX   = 200E-10         NSUB   = 1E17         GAMMA  = 0.5
+ PHI   = 0.7             VTO    = 0.8          DELTA  = 3.0
+ UO    = 650             ETA    = 3.0E-6       THETA  = 0.1
+ KP    = 120E-6          VMAX        = 1E5     KAPPA  = 0.3
+ RSH   = 0               NFS    = 1E12         TPG    = 1
+ XJ    = 500E-9          LD     = 100E-9
+ CGDO  = 200E-12         CGSO   = 200E-12      CGBO   = 1E-10
+ CJ    = 400E-6          PB     = 1            MJ     = 0.5
+ CJSW  = 300E-12         MJSW   = 0.5
.end
```

Next, three definitions are issued with 'let' statements to define I_D, g_m, and calculated g_m. $g_{m,calc}$ is merely equation 9.22 using the parameters from the level 3 NMOS model for β_n and V_{THN}. Figure 1 shows the results when this netlist is run.

The red line is I_D. I_D behaves as expected because there is almost no current until $V_{GS} > V_{THN}$ (~0.8V) and then there is a rapid increase in the I_D for an increase in V_{GS}. The green line is gm and also behaves as expected. gm is defined as the rate of change of i_d with respect to v_{gs}. This definition is only value for the area of the I_D vs V_{GS} curve around the V_{GS} bias point. For this particular case the V_{GS} is approximately 1.05V.

The blue line is the calculated value of g_m. It is obvious that the calculated value of g_m correlated very well with the simulated version for the immediate region surrounding the V_{GS} bias point.
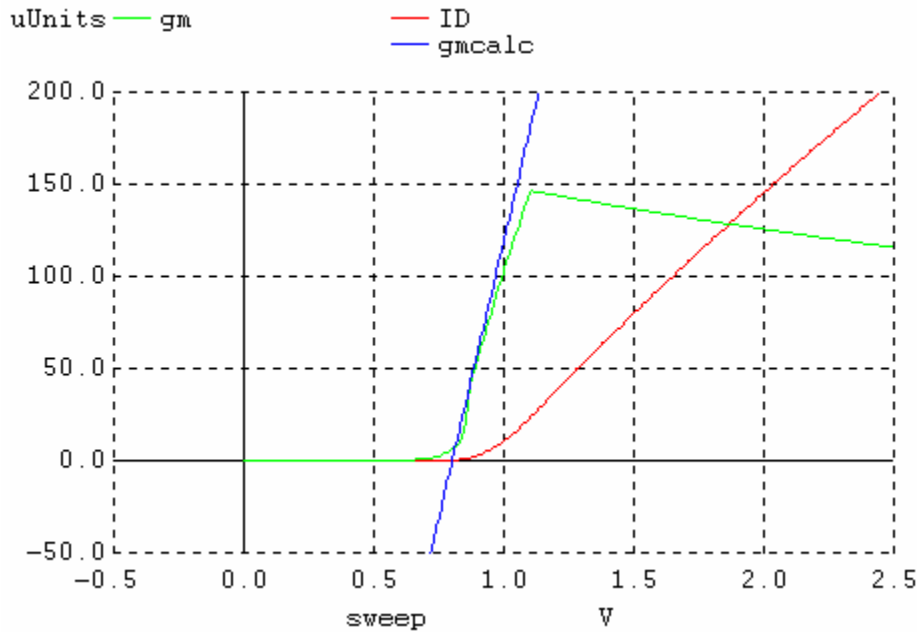

Figure 1. I_D, g_m, and $g_{m,calc}$ vs. V_{GS}

This model shows a very continuous change from the subthreshold to the strong inversion regions. This can be seen in Figure 2 by observing I_D and g_m with no discontinuities below for $V_{GS} < V_{THN}$.
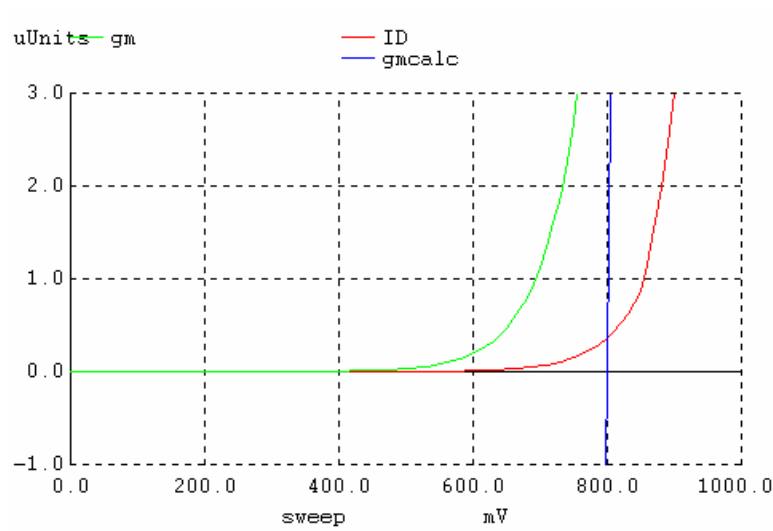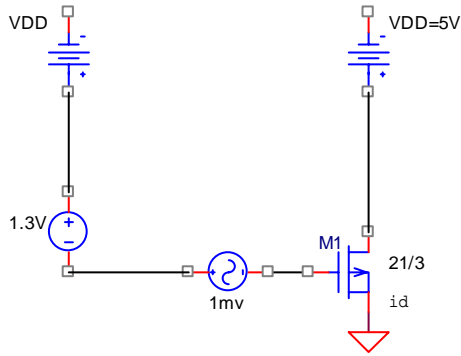

Figure 2. Zoomed in version of Figure 1. to show the subthreshold region

9.13)

To find weather the MOSFET is in saturation or triode we need to check the following two conditions

$V_{SG} > V_{THP}$ => $1.3V > 0.9V$

$V_{SD} > V_{SG} - V_{THP}$ => $5V > 1.3V - 0.9V$. (Were V_{SG}= 1.3 V; V_{THP}= 0.9V)

As both the conditions are satisfied the MOSFET is in Saturation.

The relation between the AC gate voltage to the AC drain current is given by

$i_d = g_m \times v_{gs.}$

And the value of g_m is given by

$$g_m = K_{pp} \times W/L \, (V_{SG} - V_{THP})$$
$$g_m = 40\mu A/V \times 21/3 \times (1.3-0.9) = 112 \; \mu A/V.$$

$i_d = g_m \times v_{gs} = 112 \; \mu A/V \times 1mV = 112 \; nA.$

The AC drain current $_{id}$ = 112 nA Sin2Πf.

And $I_D = K_{pp}/2 \times W/L \, (V_{SG} - V_{THP})^2$ = $40/2 \times 21/3 \times (1.3-0.9)^2 = 22.4 \; \mu A.$

SPICE SIMULATIONS

1.A) AC Simulations Source Code :

*** Problem 9.13 CMOS: Circuit Design, Layout, and Simulation ***

```
* AC ANALYSIS
.control
destroy all
run
plot -VDD#BRANCH
.endc
```
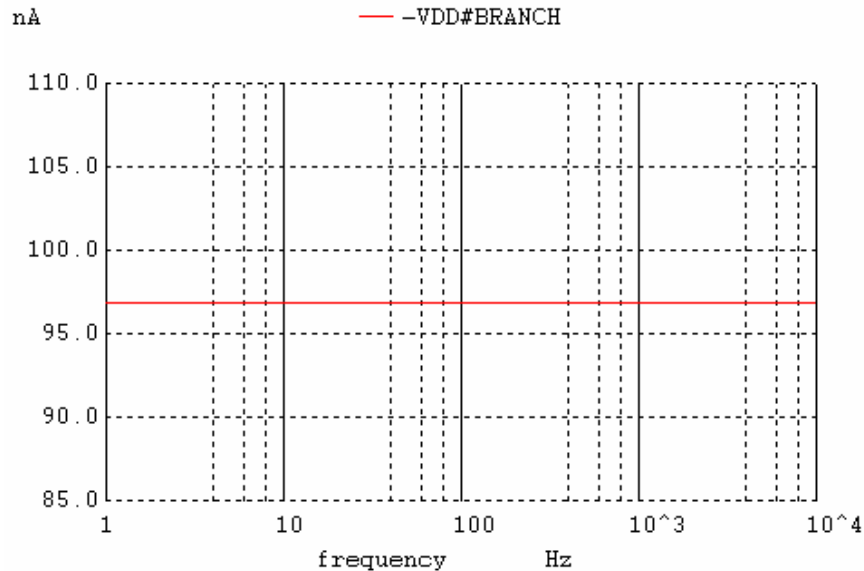
```
.option scale=1u
.ac dec 100 1 10k
VDD   VDD   0       DC      5
VG1   VDD   VG1   DC      1.3 AC 1m      SIN 2.5 1m
M1      0         VG1   VDD   VDD   PMOS L=3 W=21
```

Simulation result:

Simulation Result: i_d = 97 nA. (Hand Calculation : i_d = 112 nA).

1.B) The Transient Analysis Source Code

*** Problem 9.13 CMOS: Circuit Design, Layout, and Simulation ***

```
*  The Transient Analysis
.control
destroy all
run
.endc
.option scale=1u
.op

VDD   VDD   0       DC      5
VG1   VDD   VG1   DC      1.3 AC 1m      SIN 2.5 1m
M1      0         VG1   VDD   VDD   PMOS L=3 W=21
```

Result of Simulation : I_D = 2.1 x 10^-5 = 21 μA. (Hand Calculation I_D = 22.4 μA)

Overall Result: The Spice Simulations and Hand Calculations are close.

Problem: 9.14
The gates and sources of both M1 and M2 are both physically connected $V_{GS1}=V_{Gs2}$ and $I_{D1}=I_{D2}=20uA$
Assuming both M1 and M2 are operating in saturation

$$V_{GS1}=V_{Gs2}= \sqrt{2I_{D}.L \Big/ KP_{n}.W} + V_{thn}$$

$$= \sqrt{\frac{2.20.2}{120.10}} + 0.8 = 1.06v$$

$V_{GS1}=V_{G}-V_{s1}$ therefore $V_{s1}= V_{G}- V_{GS1}=2.5-1.06=1.44v$
Since V_{G} and gate source voltages of both mosfets (M1 and M2) are same the source voltages are also same.

Assuming M3 and M4 are in triode:

The source to gate voltage for M3 and M4 is
$ID_{3}=KP_{p}.W/L.[(V_{SG}-V_{thn}).V_{SD}- V_{SD}^{2}/2)]$
$20=40*10^{-6}.30/2.[(5-0-0.9). V_{SD}- V_{SD}^{2}/2)]$

solving the above quadratic equation we get $V_{SD}=8.19v$ and $0.00813v$. The former value is not a valid value as the source voltage applied is only 5V. So taking the latter value
$V_{D3}=V_{s3}-V_{SD3}=4.991V$
As the gate to source voltage of M3 and M4 are same and same I_{D} flows
$V_{SD3}= V_{SD4}$ thus $V_{D3} = V_{D4}=4.991V$

Now let us verify whether are assumptions are right or not

Consider M3
$V_{SG3}=5-0=5V$ and $V_{SD3}=0.00813V$
therefore $V_{SG3}>V_{thn}$ and $V_{SD3}<V_{SG3}-V_{thp}$ thus our assumption that M3 is triode is correct.
Consider M1
$V_{GS1}=2.4-1.44=1.06V$ and $V_{DS1}=4.967V$
therefore $V_{GS1}> V_{thn}$ and $V_{DS1}> V_{GS1}- V_{thn}$ thus our assumption is correct.
Similarly M2 and M4 are operating in saturation and triode regions respectively.

M3 and M4 can be modeled as resistors whose resistance is channel resistance as they are operating in triode
$$R_{CHM4}= R_{CHM3}=[KP_{p}\frac{W}{L}.[V_{SG4}-V_{thp}]]^{-1}=406.50 \text{ ohms.}$$

AC analysis
We start by writing loop equation
$1mv-v_{gs1}+v_{gs2}+1mv=0 => v_{gs1}-v_{gs2}=-2mv$

$$\frac{i_{d1}}{g_{m1}} - \frac{i_{d2}}{g_{m2}} = -2mv$$

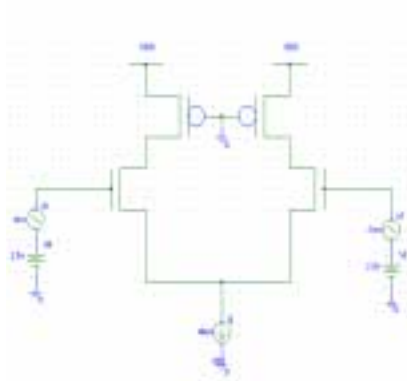since $i_{d1}=-i_{d2=}i_{d3}=-i_{d4}$ and $g_{m1}=g_{m2}$ $v_{gs1}=- v_{gs2}=1mv$
$i_{d1}= g_{m1.} v_{gs1}=150nA$
Ac drain voltages of M2 and M4= $- i_{d4}. R_{CHM4}=60.9uV$
AC drain voltage of M1 and M3=$- i_{d1.} R_{CHM1}=150nA. 406.5=60.9uV$
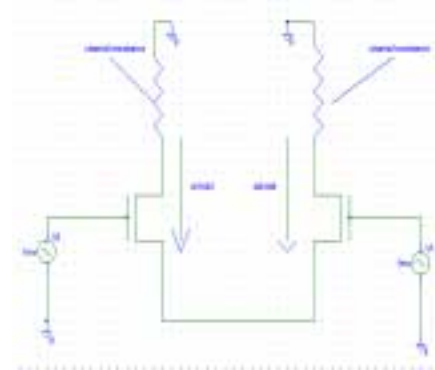$$i_{D1}=20u+0.15sin2\pi f$$
$$i_{D2}=20u-0.15sin2\pi f$$

DC analysis   AC analysis
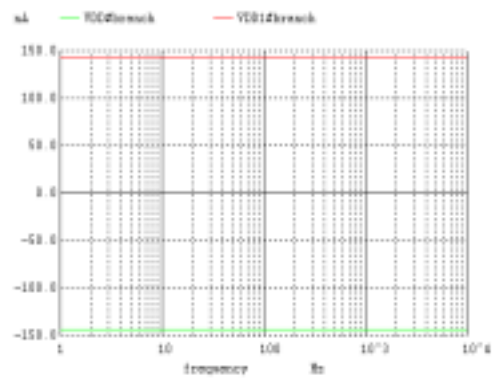

                                                         AC currents

Verification using Spice:
*** problem 9.14
.control
destroy all
run
** for the operating point analysis
*print all
* for the AC analysis
plot mag(vd13) mag(vs12) mag(vg1)
.endc
.option scale=1u
*.op
.ac dec 100 1 10k   From simulations $i_{d1}=-i_{d2}=143.86nA$

VDD	VDD	0	DC	5			
VG1	VG1	0	DC	2.5	AC	1m	SIN 2.5 1m 10k
VG2	VG2	0	Dc	2.5	AC	-1m	SIN 2.5 1m 10k
Ibias	VS12	0	DC	40u			
M1	VD13	VG1	VS12	0	NMOS L=2 W=10		
M2	VD24	VG2	VS12	0	NMOS L=2 W=10		
M3	VD13	0	VDD	VDD	PMOS L=2 W=30		
M4	VD24	0	VDD	VDD	PMOS L=2 W=30		

DC Operating Point

$vd13 = 4.989699e+00$

$vd24 = 4.989699e+00$

$vdd = 5.000000e+00$

$vdd\#branch = -4.00000e-05$

$vg1 = 2.500000e+00$

$vg1\#branch = 0.000000e+00$

$vg2 = 2.500000e+00$

$vg2\#branch = 0.000000e+00$

$vs12 = 1.171839e+00$

.

AC voltages

from simulations $mag(v_{d13})=74.2uV, V_{g1}=1mv$ The hand calculated values and simulations results
are almost close

9.15 To calculate the AC, DC voltages and currents in the circuit below:

To find the operating points of the circuit do the DC analysis. Hence short all the AC voltage sources.

DC Analysis:

The DC equivalent of the given problem is given below:

Assume both M1 and M2 are in saturation, we will verify our assumption shortly.
Since the sources of both M1 and M2 are tied together and gates are connected to 2.5V
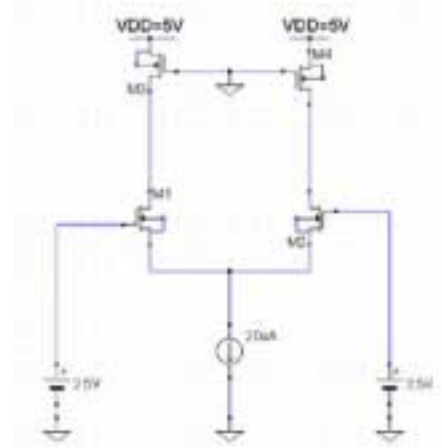
$$V_{GS1}=V_{GS2}$$

and since the circuit is symmetric $I_{D1}=I_{D2}=10uA$

$$V_{GS1} \text{ or } V_{GS2} = \sqrt{\frac{2IL}{KPnW}} + V_{thn}$$

$$= \sqrt{\frac{2.10.2}{120.10}} + 0.8 = 0.9825V$$

$\therefore$ It follows that $V_{S1} = V_{S2} = V_G - 0.9825$

$$2.5 - 0.9825 = 1.517V$$

DC equivalent circuit

Coming to M3 and M4, since both the gates are tied to ground and source is at VDD by intuition they might be in triode. We will verify this too shortly.

In triode:
$$I_D = KP_p.W/L. [(V_{SG}-V_{thp}).V_{SD3} - (V_{SD3})^2 /2)]$$

Since $I_D = 10 \mu A$ and other parameters are known except V_{SD3}, solve for V_{SD3}

$$10 = 40.\frac{30}{2}((5-0.9)Vsd - \frac{Vsd^2}{2})$$

Solving for V_{SD3} we get $V_{SD3} = 0.00406$ V or 8.195 V. The later value for V_{SD3} doesnot make any sense.

$$\therefore \quad V_{D3} = 5 - V_{SD3} = 4.995V$$

From the circuit it can be seen that $V_{D3} = V_{D4}$.

Now for M1:
$$V_{DS} = 4.995 - 1.517 = 3.478 \text{ V}$$
$$V_{GS} - V_{thn} = 0.9825 - 0.80 = 0.1825 \text{ V}$$

Since $V_{DS} > V_{GS} - V_{thn}$,our assumption that M1 is in saturation is correct.

Now for M3:

$$V_{SD} = 5 - 4.995 = 5mV$$
$$V_{SG} - V_{thp} = 5 - 0.90 = 4.1V$$

Since $V_{SD} < V_{SG} - V_{thp}$, our assumption that M3 is in triode is verified.

Similar argument follows for M2 and M4.

Since M3 and M4 are in triode they behave as a resistors whose resistance is given by:

$$R_{CHM4} = R_{CHM3} = V_{SD}/I_D = 0.00406/10uA = 406\Omega$$

The transconductance of M1 and M2 are given by:

$$g_{m1} = g_{m1} = KPn\frac{W}{L}(Vgs - Vthn)$$
$$= 120.10/2(0.9825-0.8) = 109.5 \ \mu A/V$$

Having calculated all the DC parameters lets check our calculations with simulations:

SPICE result = vd13 = vd24 = 4.994858e+00   Hand calculation gave us 4.995 V
SPICE result = vs12 = 1.239740e+00   Hand calculation gave us 1.517V

The discrepancy in vs12 is because of the fact that we did not take body effect into account.

Now coming to the AC analysis:

AC Analysis:

The AC equivalent circuit is shown:
By KVL:

$$1mV = v_{gs1} - v_{gs2} - 1mV$$

$$v_{gs1} - v_{gs2} = 2mV$$

and since $\dfrac{i_d}{g_m} = vgs$ it follows

$$\frac{i_{d1}}{g_{m1}} - \frac{i_{d2}}{g_{m2}} = 2mV$$

and we know that $i_{d1} = -i_{d2} = i_{d3} = -i_{d4}$ and $g_{m1} = g_{m2}$
Therefore it follows that $v_{gs1} = -v_{gs2} = 1mV$
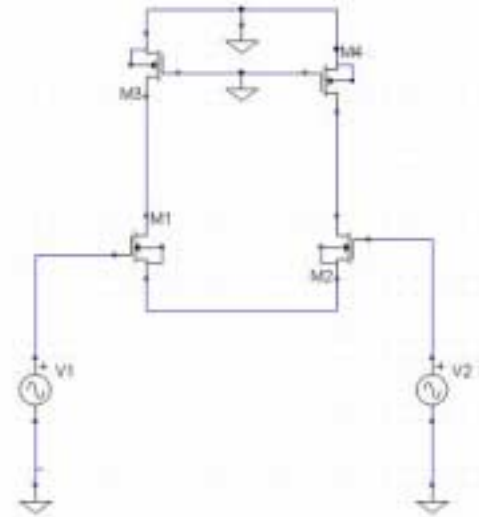
Calculating the AC drain current

AC equivalent circuit

$$i_{d1} = g_{m1} \cdot v_{gs1} = 109.5 \ \mu A/V * 1mV = 109.5nA$$

Therefore the total instantaneous current is given by

$$i_{D1} = 10u + 0.1095\sin 2\pi f$$
$$i_{D2} = 10u - 0.1095\sin 2\pi f$$

where "f" is the frequency of the AC source.

Now calculating the AC voltages:

AC drain voltage of M1 or M3 = $-i_{d1.}$ R_{CHM1} = 109.5nA X 406Ω = 0.044mV

AC drain voltage of M2 and M4= $i_{d4.}$ R_{CHM4} = 109.5nA X 406Ω = 0.044mV
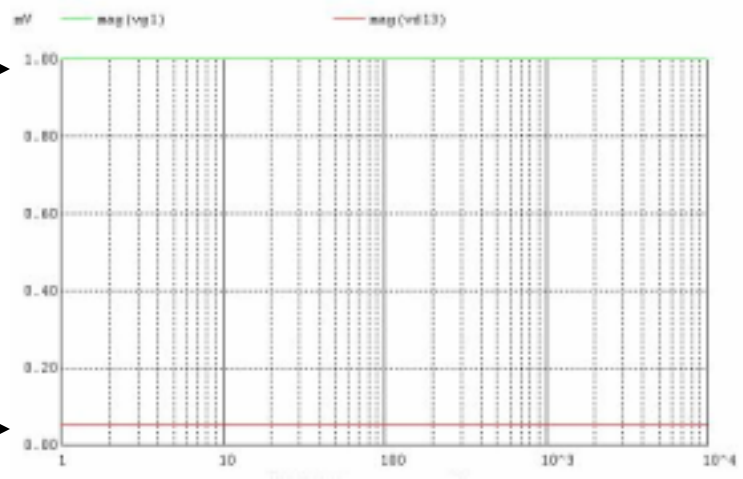
Lets check our hand calculations with simulated results:

Simulated drain voltage = 0.054mV   Hand calculated = 0.044mV.
Both the values are pretty close.

The SPICE net lists and plots are shown in below:

AC input voltage →

Drain voltages of
M1,M2,M3,M4 →

SPICE NETLIST:

.control
destroy all
run
** for the operating point analysis
*print all
*
** for the AC analysis
plot mag(vd13) mag(vg1)
.endc

.option scale=1u
*.op
.ac dec 100 1 10k

VDD	VDD	0	DC	5		
VG1	VG1	0	DC	2.5	AC 1m	SIN 2.5 1m 10k
VG2	VG2	0	DC	2.5	AC -1m	SIN 2.5 1m 10k
Ibias	VS12	0	DC	20u		

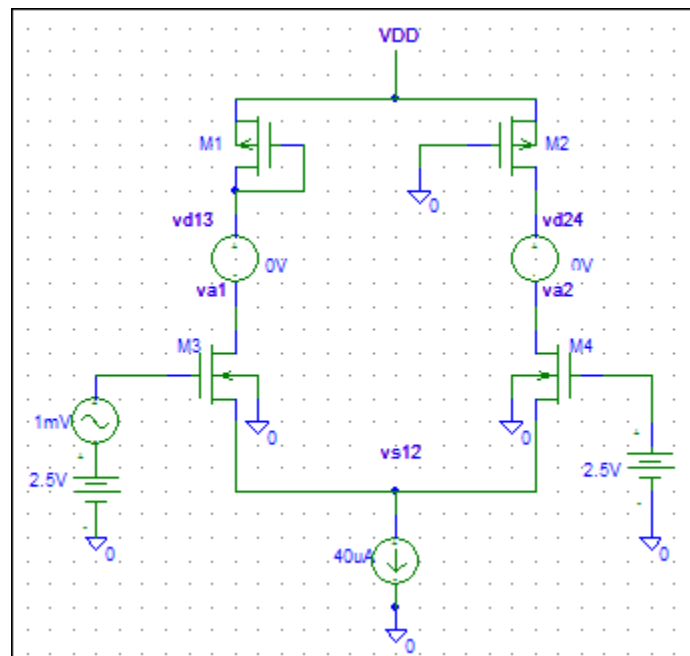| M1	VD13	VG1	VS12	0	NMOS L=2 W=10
M2	VD24	VG2	VS12	0	NMOS L=2 W=10
M3	VD13	0	VDD	VDD	PMOS L=2 W=30
M4	VD24	0	VDD	VDD	PMOS L=2 W=30

.end

The drain currents calculated in Ex. 9.5 are

$$i_{D1} = 20uA + 0.075\sin 2\Pi f$$

$$i_{D2} = 20uA - 0.075\sin 2\Pi f$$

To look at the drain currents in SPICE, zero volt DC sources are added and the currents through these added sources are plotted.

The schematic is shown below.

Spice Netlist

Prob 9.16
.control
destroy all
run

* for the AC analysis
* plot v1#branch v2#branch

**For transient analysis
**plot v1#branch
**plot v2#branch
.endc
.option scale=1u

*.ac dec 100 1 10k
**.tran 1u 300u

```
v1      vd13   va1   0v
v2      vd24   va2   0v
vdd     vdd    0     dc    5
vg1     vg1    0     dc    2.5    ac    1m    sin 2.5 1m 10k
vg2     vg2    0     dc    2.5
ibias   vs12   0     dc    40u

M1      va1    vg1   vs12  0      NMOS L=2 W=10
M2      va2    vg2   vs12  0      NMOS L=2 W=10
M3      vd13   vd13  vdd   vdd    PMOS  L=2 W=30
M4      vd24   0     vdd   vdd    PMOS  L=2 W=30
```

*Level 3 models
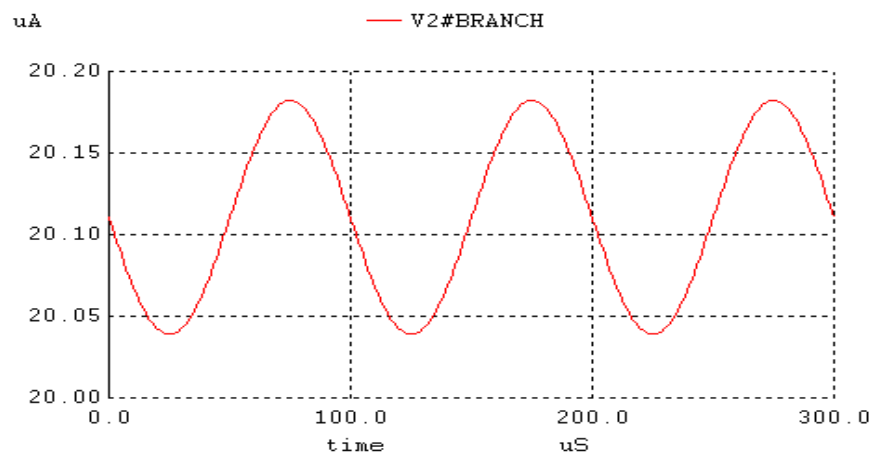.MODEL NMOS NMOS LEVEL = 3

.MODEL PMOS PMOS LEVEL = 3
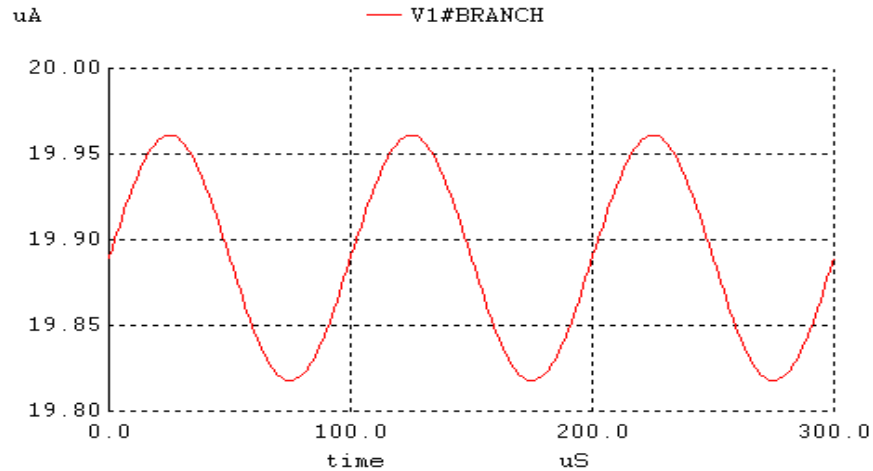--------------------------------
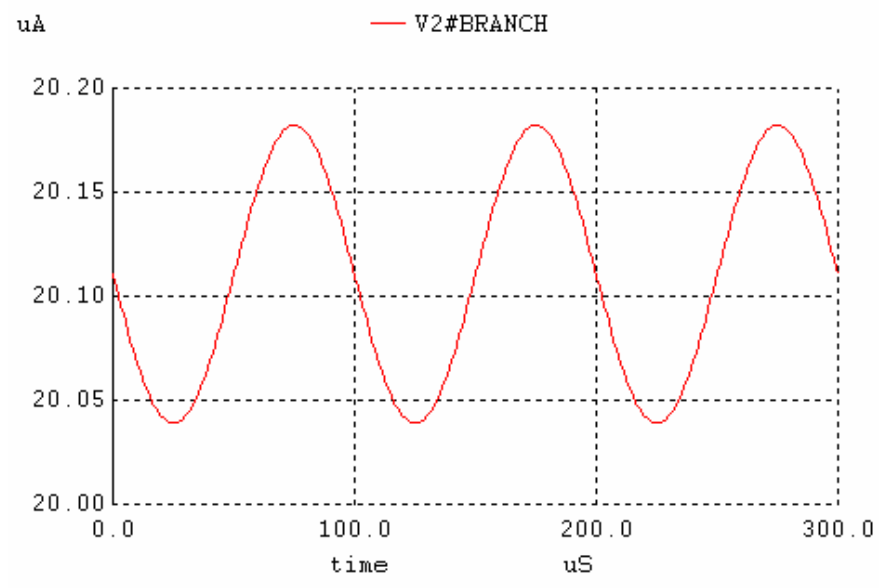
.end

AC Analysis

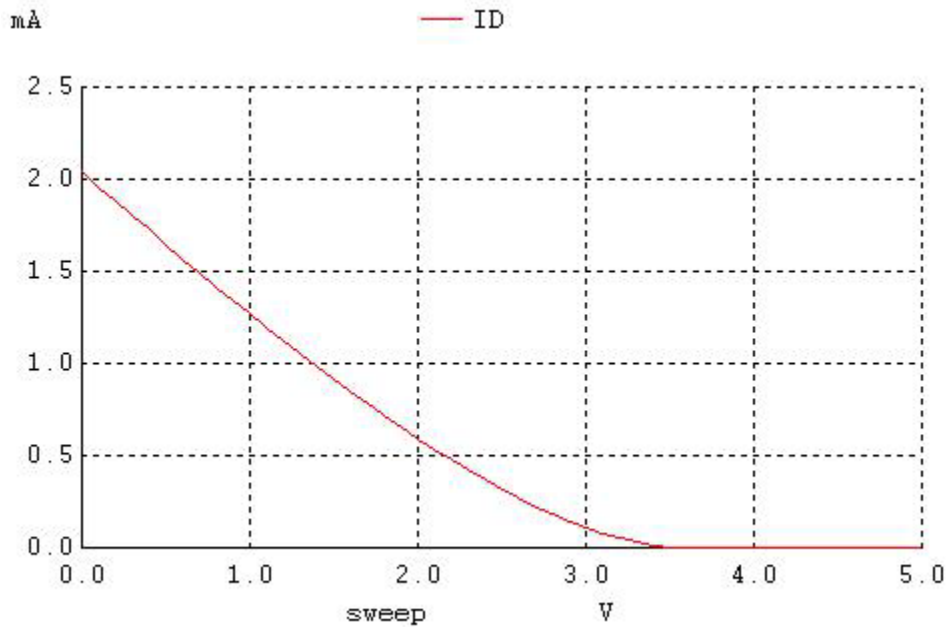$$V1\#branch = 72nA, \quad V2\#branch = -72nA$$

Transient Analysis

Problem 9.17

When the potential of the source of a MOSFET is increasing, a point is reached where the gate to source potential goes below the threshold voltage. The MOSFET then shuts off. That's the point where the graph cuts the x-axis. When the source voltage (or the source to bulk potential, since the body is grounded) is 0, the value of ID is where the graph cuts the y-axis.

SPICE Netlist:

*** PROBLEM 9.17 CMOS: Circuit Design, Layout, and Simulation ***

.control
destroy all
run
LET ID = -VMETER#branch
PLOT ID
.endc

.option scale=1u

.DC   VSB   0   5   100m

VDD   VDD   0   DC   5
VG   VG   0   DC   5
VSB   VSB   0   DC   5   AC   1m

M1   VD   VG   VSB   0   NMOS L=2 W=10

VMETER   VD   VDD   DC   0

```
.MODEL NMOS NMOS LEVEL  = 3
+ TOX   = 200E-10      NSUB  = 1E17        GAMMA  = 0.5
+ PHI   = 0.7         VTO   = 0.8        DELTA = 3.0
+ UO    = 650         ETA   = 3.0E-6      THETA = 0.1
+ KP    = 120E-6      VMAX  = 1E5         KAPPA = 0.3
+ RSH   = 0           NFS   = 1E12        TPG   = 1
+ XJ    = 500E-9      LD    = 100E-9
+ CGDO  = 200E-12     CGSO  = 200E-12      CGBO  = 1E-10
+ CJ    = 400E-6      PB    = 1           MJ    = 0.5
+ CJSW  = 300E-12     MJSW  = 0.5
*
.MODEL PMOS PMOS LEVEL  = 3
+ TOX   = 200E-10      NSUB  = 1E17        GAMMA  = 0.6
+ PHI   = 0.7         VTO   = -0.9        DELTA = 0.1
+ UO    = 250         ETA   = 0           THETA = 0.1
+ KP    = 40E-6       VMAX  = 5E4         KAPPA = 1
+ RSH   = 0           NFS   = 1E12        TPG   = -1
+ XJ    = 500E-9      LD    = 100E-9
+ CGDO  = 200E-12     CGSO  = 200E-12      CGBO  = 1E-10
+ CJ    = 400E-6      PB    = 1           MJ    = 0.5
+ CJSW  = 300E-12     MJSW  = 0.5

.end
```

Problem 9.18

For n-MOSFET W/L=100/20, p-MOSFET W/L=300/20

For a long channel n-MOSFET in saturation the equation for drain current is

$$I_D = \frac{KP_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{THP})^2$$

when W and L are both multiplied by 10 as seen in the equation the drain current does not change.

$$V_{SG} = \sqrt{\frac{2I_D}{KP_P} \cdot \frac{L}{W}} + V_{THP} = \sqrt{\frac{2.20}{40} \cdot \frac{20}{300}} + 0.9 = 1.158 \text{ V}$$

The V_{GS} (NMOS) & V_{SG} (PMOS) of the MOSFET's are 1.058 V and 1.158 V respectively they remain the same as in Ex. 9.5 as the drain current (roughly 20μ bias current) is almost the same. Both the MOSFET's have a $V_{DS.SAT}$ of 250mV

Figure shows the IV plots and the output resistance (the reciprocal of the derivative of the drain current) for the MOSFET's.

The output resistances (from the plots) of NMOS & PMOS are 500 MEG & 300 MEG respectively as against 5 MEG & 4 MEG in Ex.9.6.
As $\lambda \propto$ 1/L, $r_0 \propto L^2/V^2_{DS,SAT}$
Since L increases by 10 the output resistance increased by a factor of 100 and λ decreases.

The channel-length modulation parameter is calculated as follows:
$\lambda_{n} = $ 1/ $I_{DS,SAT}.r_0 =$ 1/ (20μ .500MEG) = .0001V^{-1}
$\lambda_{p} = $ 1/ $I_{DS,SAT}.r_0 =$ 1/ (20μ .300MEG) = .00016V^{-1}

Netlist
*** Problem 9.18
NMOS
.control
destroy all
run

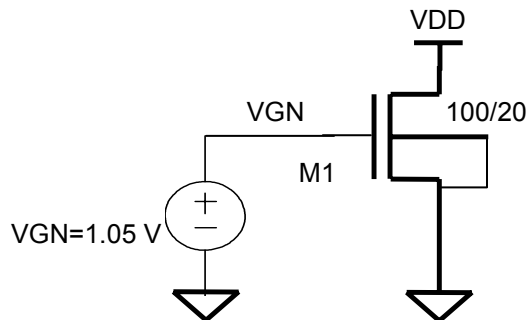let ID=-VDD#branch
plot ID

let ro=1/deriv(ID)
plot ro
.endc

.option scale=1u
.dc VDD 0 5 1m
VDD   VDD   0   DC   5
VGN   VGN   0   DC   1.05

M1   VDD   VGN   0   0   NMOS L=20 W=100

VDD

VGN   100/20

M1

VGN=1.05 V
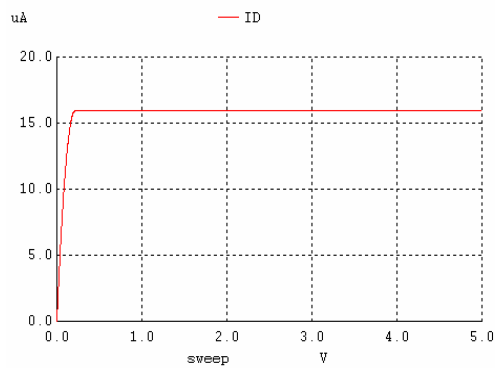
```
PMOS
.control
destroy all
run
let ID=-VDD#branch
plot ID
let ro=1/deriv(ID)
plot ro
.endc

.option scale=1u
.dc VDD 0 5 1m

VDD     VDD     0       DC      5
VGP     VDD     VGP     DC      1.15
M1      0       VGP     VDD     VDD     PMOS L=20 W=300
```
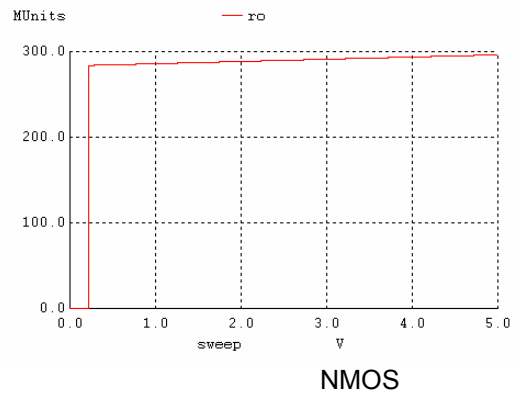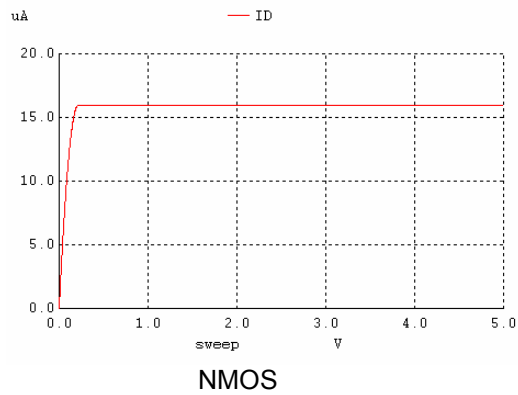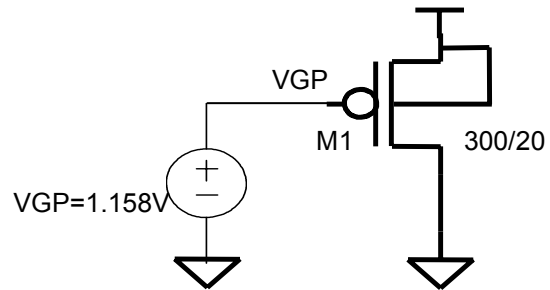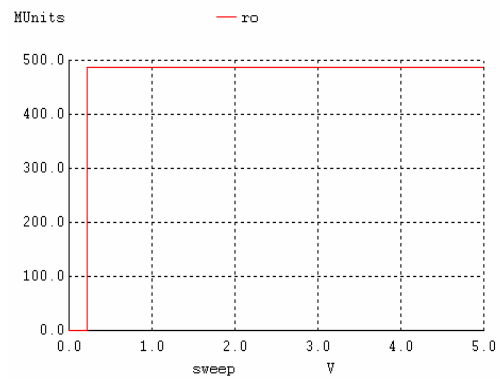
VGP

VGP=1.158V

M1   300/20

NMOS

NMOS

PMOS

PMOS

Problem 9.19

From the equation 9.36 we have,

$f_t = g_m / (2 \pi C_{gs})$ where $C_{gs} = (2/3) W L C_{ox}'$ and

$g_m = KP_n (W/L)(V_{gs} - V_{th})$ substituting we get

$f_t = [3 KP_n (V_{gs} - V_{th})] / [4 \pi L^2 C_{ox}']$ so

$f_{t1} = [3 KP_n (V_{gs} - V_{th})] / [4 \pi L_1^2 C_{ox}']$ and
$f_{t2} = [3 KP_n (V_{gs} - V_{th})] / [4 \pi L_2^2 C_{ox}']$

$f_{t1}/f_{t2} = (L_2 / L_1)^2$

For our case comparing 10/2 NMOS to 100/20 NMOS we get

$f_{t1}/f_{t2} = (20 / 2)^2 = 100$

$f_{t2} = f_{t1}/100$

From this relationship we can see that ft depends only on channel length. In other words ft decreases with channel length increase (quadratic dependence on channel length relationships).
To illustrate change, WinSpice simulations were performed and obtained following graphs:
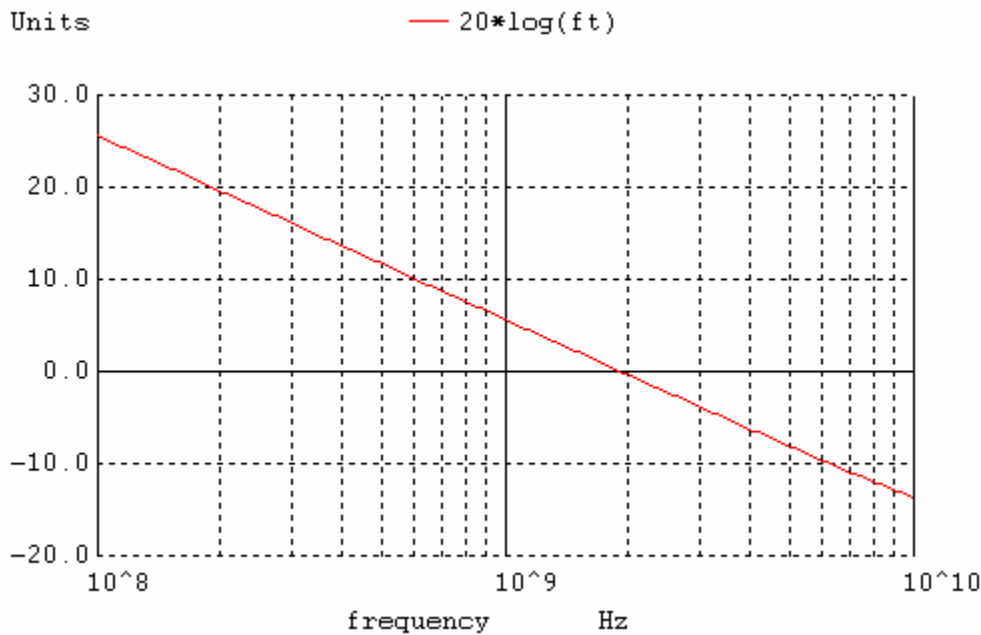

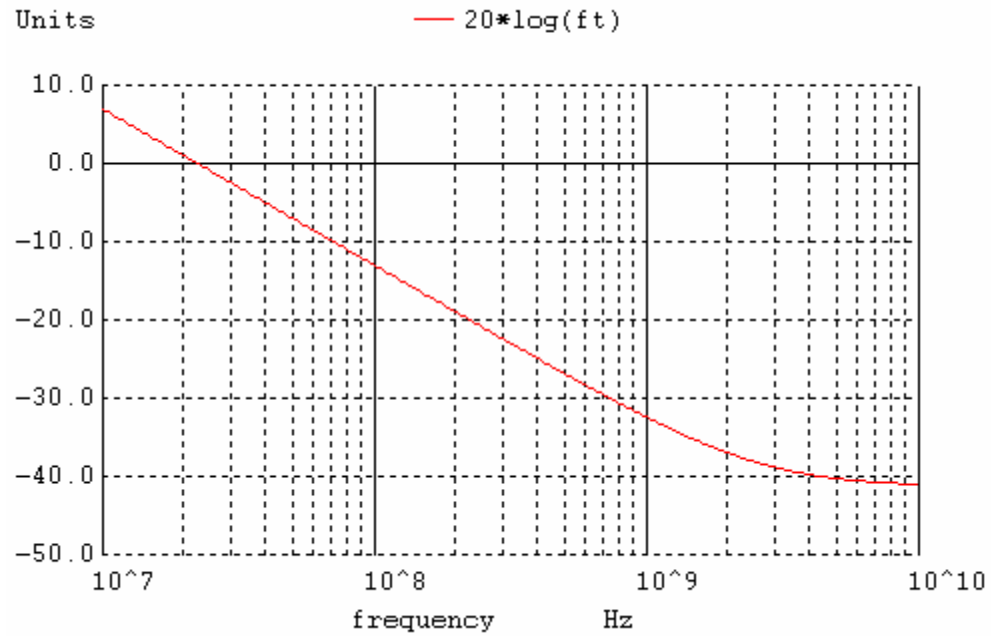Figure 1: Simulation f_{t1} Plot for 10/2 NMOS

Figure 2: Simulation ft_2 Plot for 100/20 NMOS

From figures 1 and 2 we can see that $ft_1 = 2 \times 10^9$ Hz (ft_1 intersect 0-axes) and $ft_2 = 2 \times 10^7$ Hz (ft_2 intersect 0-axes) approximately. So,

$ft_1/ft_2 = 100$ approximately

Problem 9.20

Yes, it is possible to have sub threshold operation when drain current is 100uA.Simply use a larger 'W/L' device .This scales currents in all regions (sub threshold, triode and saturation) to go up by a factor of 'W/L'.

Problem 9.21

This problem asks us to estimate the threshold voltage of a PMOS and a NMOS transistor which are fabricated using a short channel process. The dimensions of both MOSFETS are 50/5.

We will start with the NMOS. The threshold voltage may be estimated by examining two different plots. First, if we plot I_D versus V_{GS}, the threshold voltage may be estimated by linearly extrapolating back to the x-axis. As seen in figure 1, the extrapolation yields an approximate value of 280mV for V_{THN}.
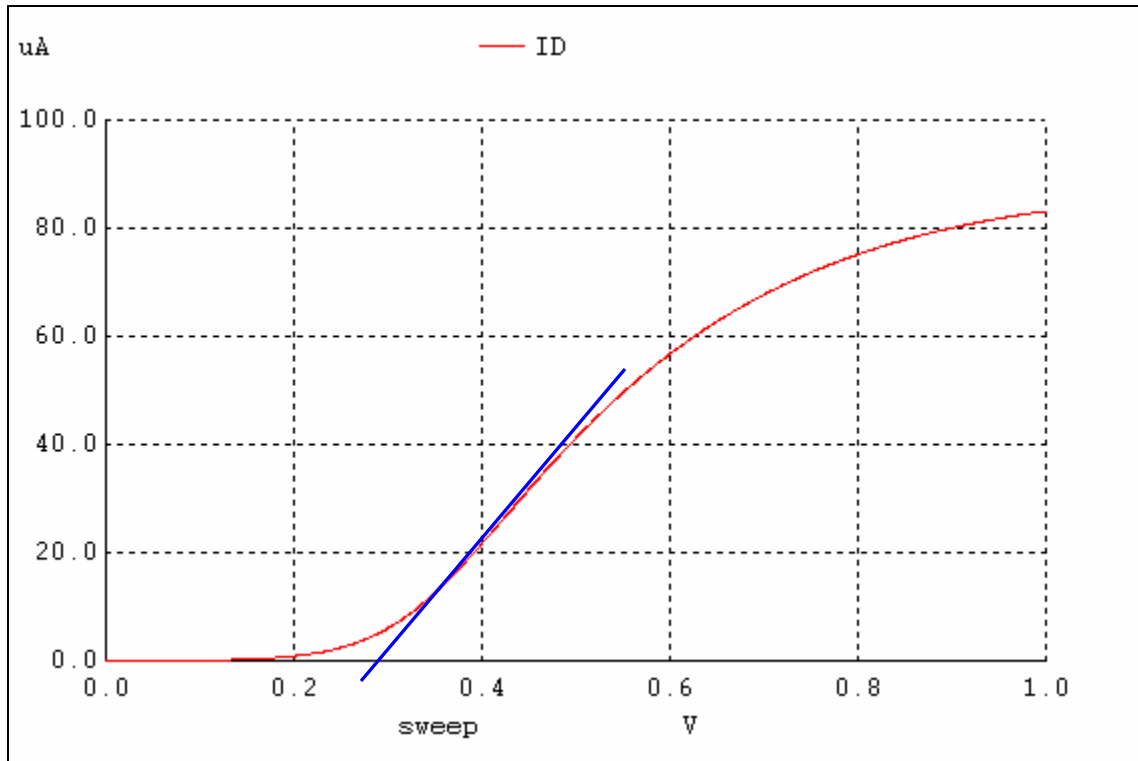

Figure 1: I_D verses V_{GS}, showing the Threshold Voltage at ~280mV

The second method of threshold estimation involves plotting the derivative of I_D versus V_{GS}. Once again, we will linearly extrapolate back to the x-axis to find the approximate value of V_{THN}. Figure 2 shows that the threshold voltage is approximately 210mV. This measurement is considered more accurate than the first. For more explanation, please see Figure 9.27 and the accompanying paragraph in chapter 9 of the text.

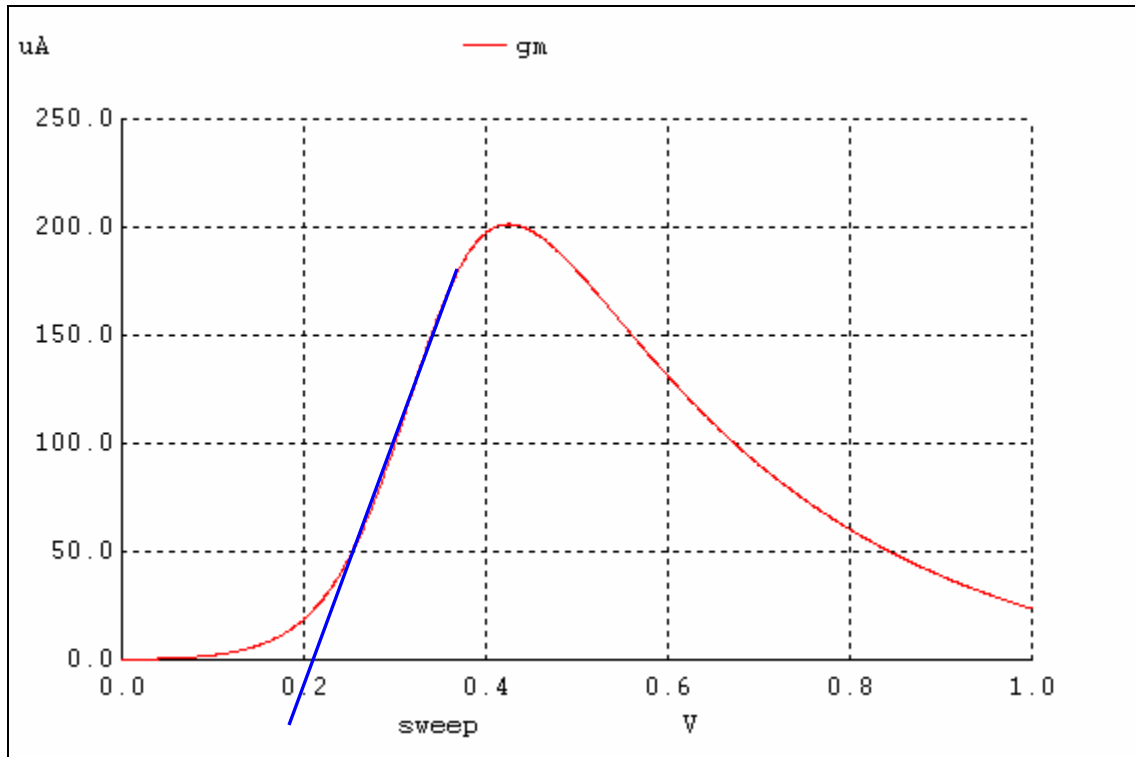The netlist used to generate these figures is shown in Figure 3.

Figure 2: The Derivative of I_D (gm) verses V_{GS}, showing the Threshold Voltage at ~210mV

```
*** Problem 9.21, from Figure 9.27 CMOS: Circuit Design, Layout, and Simulation ***

.control
destroy all
run
let ID=-VDS#branch
let gm=deriv(ID)
plot gm
plot ID
.endc

.option scale=50n
.DC    VGS   0        1         1m

VDS   VDS   0        DC       .1
VGS   VGS   0        DC       0

M1     VDS   VGS   0        0         NMOS L=5 W=50
```

Figure 3: Netlist used to generate Figures 1 & 2 (MOSFET models are omitted.)

The situation is the same for the PMOS. Figure 4 shows that VTHP is about 250mV. Figure 5 shows the VTHP is about 190mV. Finally the netlist used for the PMOS simulations is shown in figure 6.

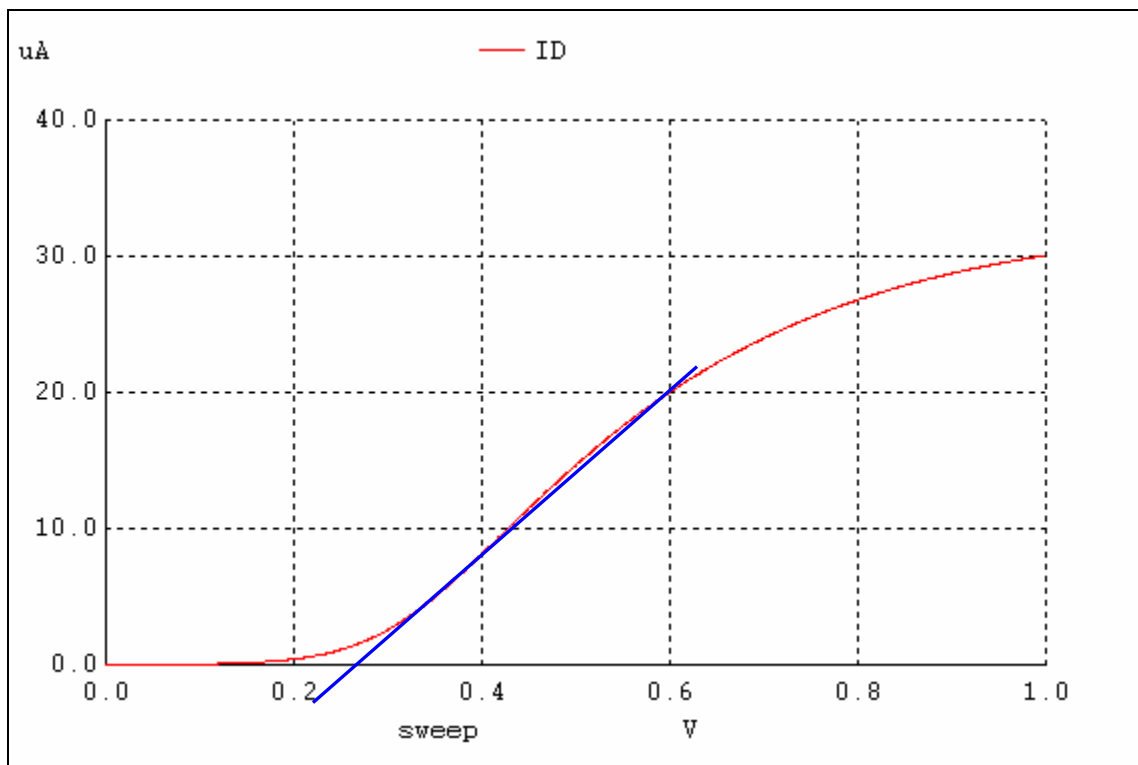**Figure 4: I$_D$ verses V$_{SG}$, showing the Threshold Voltage at 250mV**
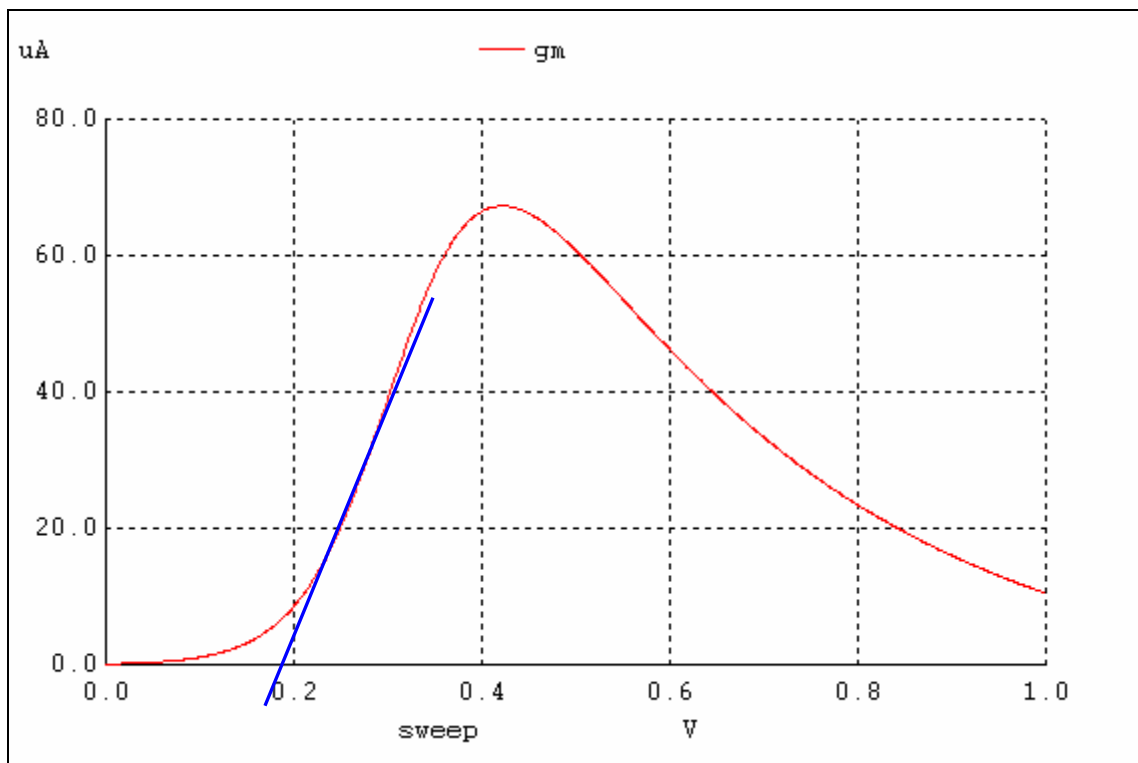
Figure 5: The Derivative of I_D (gm) verses V_{SG}, showing the Threshold Voltage at ~190mV

```
*** Problem 9.21, from Figure 9.27 (PMOS) CMOS: Circuit Design, Layout, and Simulation **

.control
destroy all
run
let ID=-VSD#branch
let gm=deriv(ID)
plot gm
plot ID
.endc

.option scale=50n
.DC    VSG   0        1        1m

VSD   0       VSD   DC     .1
VSG   0       VSG   DC     0

M1     VSD   VSG   0        0        PMOS L=5 W=50
```
Figure 6: Netlist used to generate Figures 4 & 5 (MOSFET models are omitted.)

Problem 9.22:-

Show the details leading to Eq. (9.43). Show, as an example, that the approximation is valid if $Q'_{bo}/C'_{ox} = 30mv$. (Remember: temperature is in Kelvin.)

Solution:-

From chapter 6, Eq.(6.17),

$$V_{THN} = -V_{ms} - 2V_{fp} + \frac{Q'_{bo} - Q'_{ss}}{C'_{ox}} \text{ , \textbf{where} } Q'_{ss} \text{ \textbf{is a constant.}}$$

$$Q'_{bo} = \sqrt{2qN_A\varepsilon_{si}/-2V_{fp}/} \text{ , } V_{fp} = -\frac{kT}{q}\ln\frac{N_A}{n_i} \text{ and } V_{ms} = \frac{kT}{q}\ln\frac{N_{D,poly}}{n_i} - V_{fp}$$

$$V_{THN} = -\frac{kT}{q}\ln\frac{N_{D,poly}}{n_i} + V_{fp} - 2V_{fp} + \frac{Q'_{bo} - Q'_{ss}}{C'_{ox}}$$

$$V_{THN} = -V_{fp} - \frac{kT}{q}\ln\frac{N_{D,poly}}{n_i} + \frac{Q'_{bo} - Q'_{ss}}{C'_{ox}}$$

$$V_{THN} = -\frac{kT}{q}\ln\frac{N_{D,poly}}{N_A} + \frac{\sqrt{4qN_A\varepsilon_{si}(kT/q)\ln(N_A/n_i)}}{C'_{ox}} - \frac{Q'_{ss}}{C'_{ox}}$$

By taking derivative on both sides with respect to temperature (T), we have,

$$\frac{\partial V_{THN}}{\partial T} = -\frac{k}{q}\ln\frac{N_{D,poly}}{N_A} + \frac{\sqrt{4qN_A\varepsilon_{si}(k/q)\ln(N_A/n_i)}}{2.\sqrt{T}.C'_{ox}}$$

$$\frac{\partial V_{THN}}{\partial T} = -\frac{k}{q}\ln\frac{N_{D,poly}}{N_A} + \frac{\sqrt{4qN_A\varepsilon_{si}(kT/q)\ln(N_A/n_i)}}{2.T.C'_{ox}}$$

$$\boxed{\frac{\partial V_{THN}}{\partial T} = -\frac{k}{q}\ln\frac{N_{D,poly}}{N_A} + \frac{Q'_{bo}}{2.T.C'_{ox}} \approx -\frac{k}{q}\ln\frac{N_{D,poly}}{N_A}}$$

$$N_{D,poly} = 10^{20}, N_A = 10^{15}, \frac{\partial V_T}{\partial T} = \frac{\partial}{\partial T}\left(\frac{kT}{q}\right) = \frac{k}{q} = 0.085mv/K .$$

Plugging in the numbers we get $\dfrac{\partial V_{THN}}{\partial T} = -\dfrac{k}{q}\ln\dfrac{10^{20}}{10^{15}} = -0.9786 \ mV/K$.

With the contributions from $\dfrac{Q'_{bo}}{C'_{ox}} = 30mv$ included at T=300K we get

$$\frac{\partial V_{THN}}{\partial T} = -\frac{k}{q}\ln\frac{N_{D,poly}}{N_A} + \frac{Q'_{bo}}{2.T.C'_{ox}} = -0.9786 + 0.05 = -0.9286 \ mV/K.$$

PROBLEM 9.23

(1) The NMOS is in saturation as a constant current is flowing through a gate- drain connected MOSFET.The expression for drain current for the short channel process is:

$$I_{DS} = \upsilon_{satn} * W * C_{ox}'*(V_{ovn} - V_{DSsat}) \dots..(1).$$

Substituting values for υ_{satn}, W, C_{ox}' and V_{DSsat} from table9.2.The values are at room temperature=27^0C

$10*10^{-6}$= $(110*10^9$ um/s)*(50um)*(25fF/um^2)*(V$_{GS}$ –0.28-0.05)

$\Rightarrow$V$_{GS}$=0.33V.   (@27^0C)

Since the source is at ground, the output voltage=0.33V

Simulated value of the output= 0.3535V.

From equation (1)

$$I_{ds} = \upsilon_{satn} * W * C_{ox}'*(V_{GS} - V_{thn} - V_{DSsat})$$

$$\Rightarrow \quad V_{GS} = \frac{I_{DS}}{\upsilon_{satn} * W * C_{ox}'} + V_{thn} + V_{DSsat}$$

Neglecting the change of υ_{satn} ,V_{DSsat} and oxide charge with temperature.

$$\Rightarrow \quad \frac{\partial V_{GS}}{\partial T} = \frac{\partial V_{thn}}{\partial T}$$

When temperature increases, threshold voltage decreases. $\frac{\partial V_{thn}}{\partial T} \approx -0.6mV / {}^0C \dots(2)$
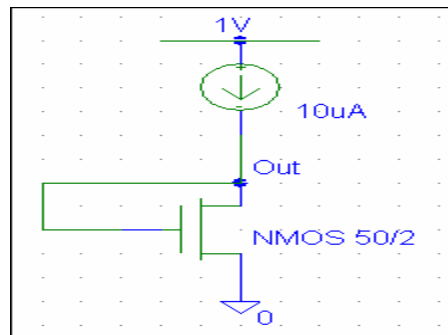
$$\Rightarrow \quad \frac{\partial V_{GS}}{\partial T} = \text{-0.6mV/}^0\text{C}$$

$$V_{GS} = V_{GS\,0} + \frac{\partial V_{GS}}{\partial T}(\text{T-T}_0) \text{ where } V_{GS} = 0.33\text{V (@room temp=}27^0\text{C}).$$

$$V_{GS} = 0.33 + (\text{-0.6mV/}^0\text{C})*(\text{T-27})\dots\dots\dots\dots\dots\dots\dots..(3)$$

The hand calculated and simulated values are shown below:

Temperature (^{0}C)	Output or Gate Voltage (V)	
	Simulations	Calculations
0	0.3701	0.3462
50	0.3398	0.3162
100	0.3115	0.2862
150	0.2843	0.2562

Circuit for problem 9.23

(2) The PMOS is also in saturation.The source is fixed@ 5V.The expression for drain current for drain current of PMOS is given by:

$$I_{SD} = \upsilon_{satp} * W * C_{ox}' * (V_{ovn} - V_{SDsat}) \dots\dots.\dots(4)$$

where $V_{ovn} = V_{SG} - V_{thp} = V_S - V_G - V_{thp}$ …………...(5).

Substituting the values for υ_{satn}, W, C_{ox}' and V_{DSsat} from table9.2.

$10*10^{-6} = (9*10^9 \text{um/s}) * (100 \text{um}) * (25 \text{fF/um}^2) * (1 - V_G - 0.28 - 0.05)$

$\Rightarrow V_G = 0.67V$.This is the output voltage of the PMOS circuit @T=27 ^{0}C.

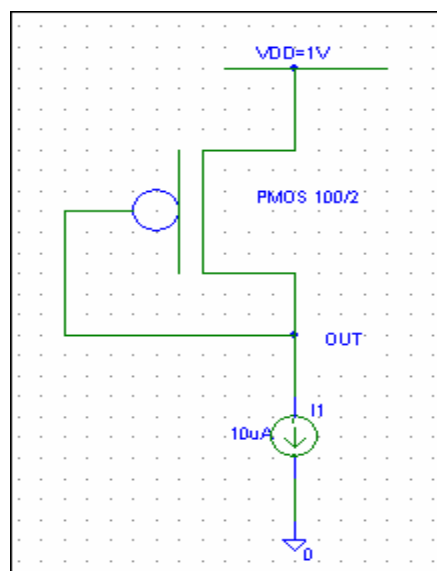Simulations result in an output voltage of 0.647V @T=27 ^{0}C.

Deriving the equation for the variation of V_{SG} with temperature for PMOS just like derived for NMOS results in the following equation:

$$V_{SG} \quad =0.33 + (-0.6 \text{mV}/^0\text{C}) * (T-27)\dots\dots\dots\dots..(6)$$

$$\Rightarrow V_{G=} V_S - [0.33 + (-0.6 \text{mV}/^0\text{C}) * (T-27)]\dots\dots\dots.. (7)$$

The hand calculated and simulated values are shown below:

Temperature (^{0}C)	Output or Gate Voltage (V)	
	Simulations	Calculations
0	0.6307	0.6538
50	0.6605	0.6838
100	0.6887	0.7138
150	0.7166	0.7438

Circuit for problem 9.23

NETLIST FOR THE SIMULATIONS:
```
*problem 9_23
*control statements
.options scale=50nm
. control
destroy all
set temp=0
run
print d
set temp=50
run
print d
set temp=100
run
print d
set temp=150
run
print d
.endc
*circuit netlist
*m1    d      d      s      s       pmos l=2 w=100
 m2    d      d      0      0       nmos l=2 w=50

*Ibias  d      0      DC     10u
 Ibiasn       vdd    d      DC     10u

*Vdd  s      0      DC     1
 Vddn        vdd    0      DC     1
 .op
```

9.24. Prove using simulation outputs that the GFT product is constant in the saturation region for different biasing conditions on a long channel process. Since GFT=gm*r0*fT, we will generate these three parameter for three different biasing using our 1u models. The three biasing currents will be set by forcing VGS to 1.5V, 2V, and 2.5V. The following file was used to simulate gm and ID with Winspice:

```
* ** Problem 9.24 Homework Finding GM using LEVEL3 models ***
.control
destroy all
run
let ID = abs(vdd#branch)
let GM = deriv(ID)
plot ID
plot GM
.endc

vdd  vdd  0  dc  5V
vg  vg  0  dc  1V
m1  vdd  vg  0  0  nmos  w=10  l=2

.DC vg 1.5V 2.5V 0.01V

.option scale=1u
** Include Model File Here ****
.end
```
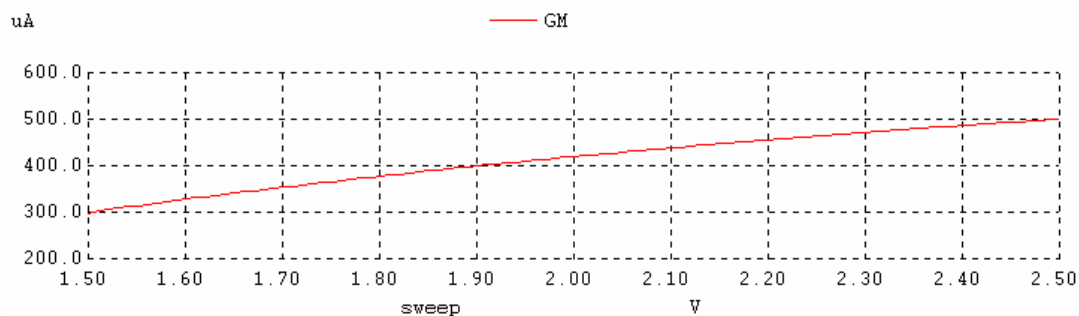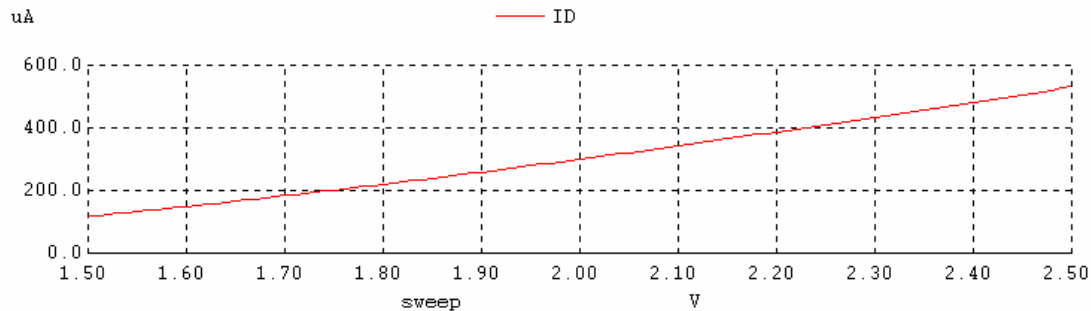
The plot for ID and gm are shown below:

Therefore: ID @ VGS=1.5V, 2V, 2.5V = 120uA, 300uA, and 530uA.
            gm @ VGS=1.5V, 2V, 2.5V = 300uA/V, 420uA/V, 500uA/V.

We will plot ID versus VDS at a constant VGS to calculate r0 (output resistance) in the saturation region. One over the slope of the line (1/derivative(ID with respect to VDS)) in the saturation region is equal to r0. The following file was used to calculate r0 for each bias condition and must be simulated three times with the different vg voltages:

* Problem 9.24 Homework Finding R0 using LEVEL3 models
.control
destroy all
run
let ID1 = abs(vdd#branch)
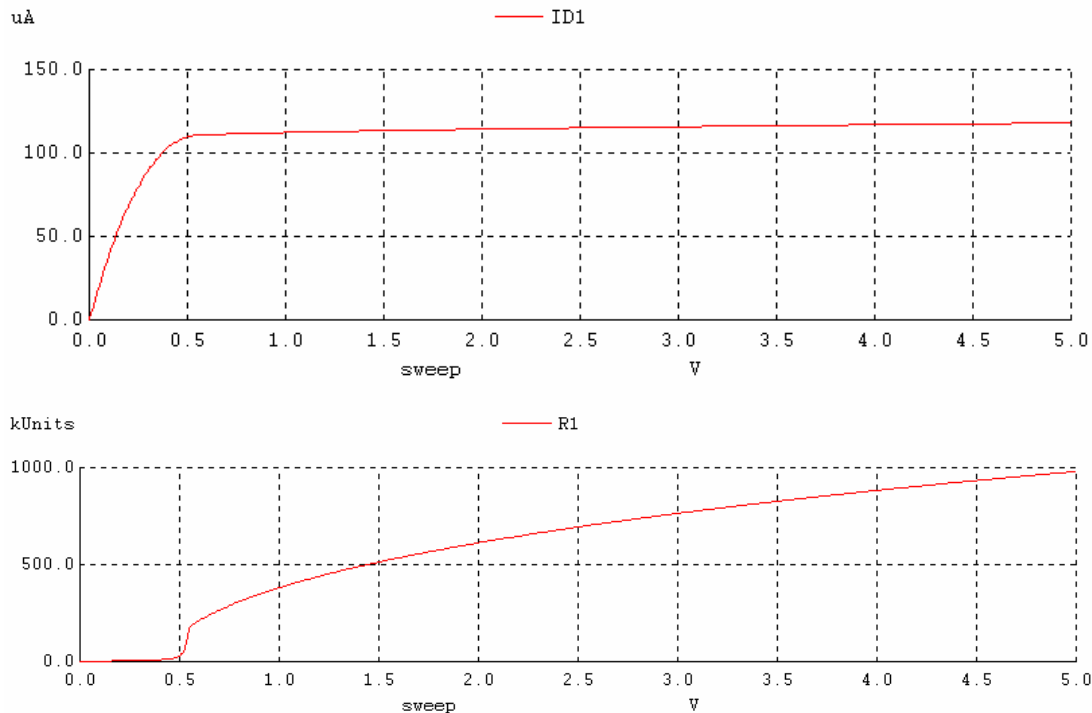let R1 = 1/deriv(ID1)
plot ID1
plot R1
.endc

vdd vdd 0 dc 3V
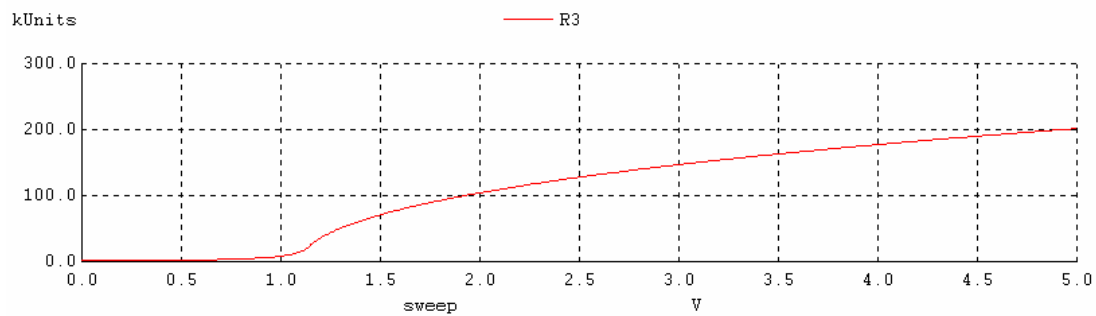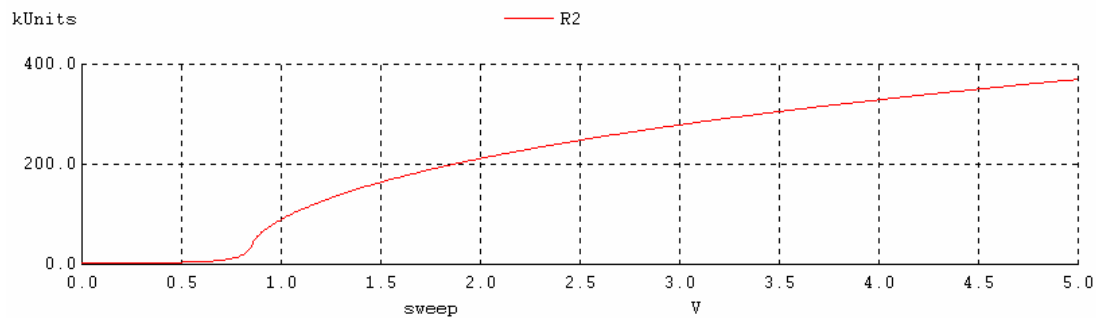vg vg 0 dc 1.5V
m1 vdd vg 0 0 nmos w=10 l=2

.DC vdd 0V 5V 0.01V

.options scale=1um

** Include Model File Here ****
.end

The plot for ID versus VDS at VGS=1.5V and r0 at VGS=1.5V, 2V, and 2.5V are shown below:

Therefore: r0 @ VDS=5V and VGS=1.5V, 2V, 2.5V = 980K, 370K, and 200K since R1 is r0 at VGS=1.5V, R2 is r0 at VGS=2V, and R3 is r0 at VGS=2.5V. IDSSAT at VGS=1.5V, 2V, 2.5V = 110uA, 280uA, and 500uA. Since VDSSAT = VGS – VTHN, VDSSAT=0.7V at VGS=1.5V, VDSSAT=1.2V at VGS=2V, and VDSSAT=1.7V at VGS=2.5V.

To calculate the GFT product, we need to find the fT at our three bias points. FT is found by running an AC analysis of a transistor in the saturation region with the AC signal applied to the gate terminal for the three VGS bias values. The value of fT is the frequency where |id| / |ig| = 0db. Plotting the logrithum of |id| / |ig| versus frequency and fT is the frequency where this quanity = 0. The following file was used to calculate fT for each bias condition and must be simulated three times with the different vg voltages:

```
* Problem 9.24 Homework Finding FT using LEVEL3 models
.control
destroy all
run
let FT1 = log(abs(vdd#branch) / abs(vg#branch))
plot FT1
.endc

vdd  vdd  0  dc  5V
vg  vg  0  dc  1.5V  ac  1mV
m1  vdd  vg  0  0  nmos  w=10  l=2

.AC lin 100 1G 5G

.options scale=1um

** Include Model File Here ****
.end
```
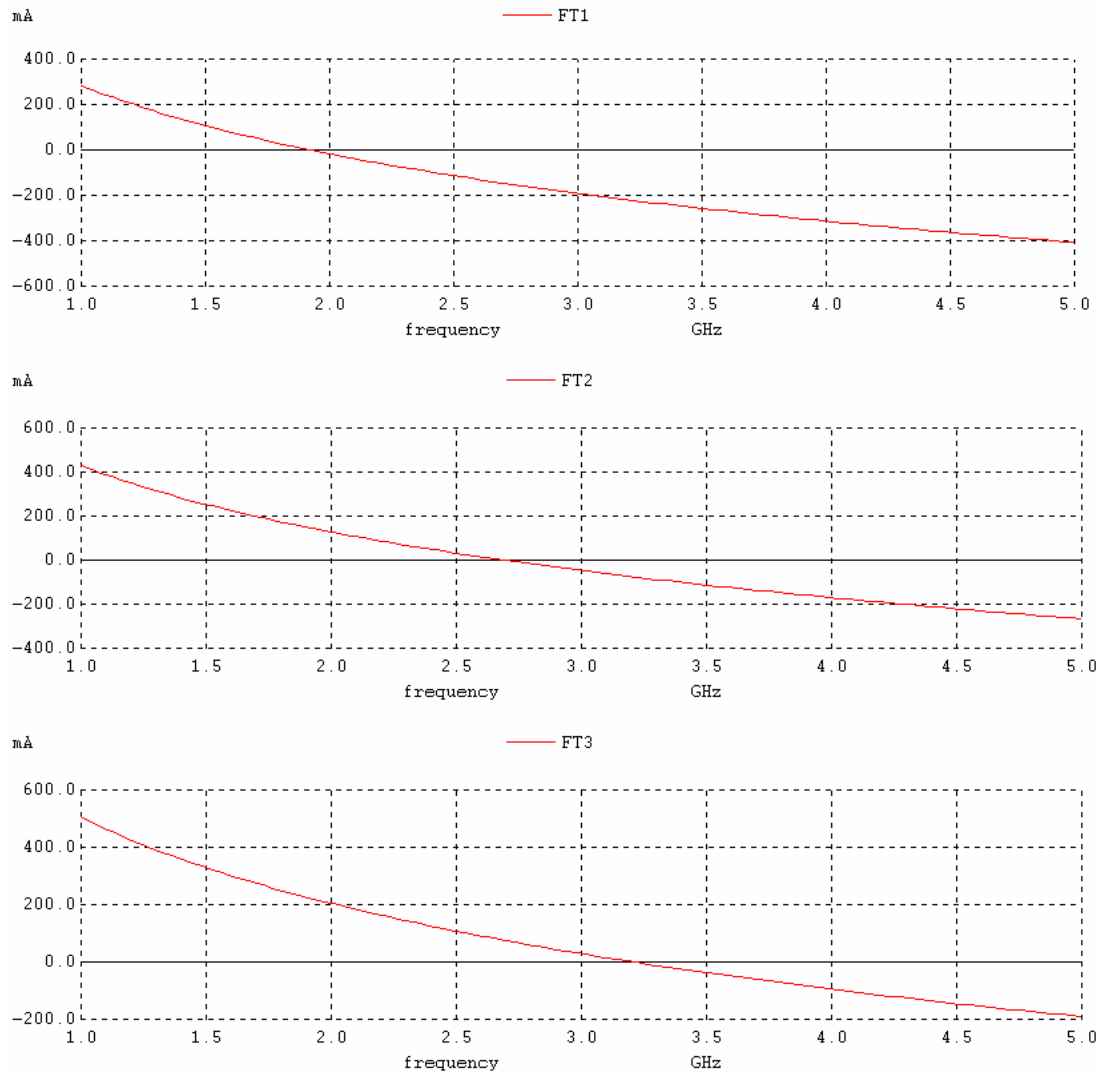
The plot for log(abs(id) / abs(ig)) versus frequency at VGS=1.5V, 2V, and 2.5V are shown below with fT being the value at 0db:

Therefore: fT @ VGS=1.5V, 2V, 2.5V = 1.9GHz, 2.7GHz, and 3.2GHz since FT1 is fT at VGS=1.5V, FT2 is fT at VGS=2V, and FT3 is fT at VGS=2.5V.

For VGS = 1.5V   =>   GFT = gm * r0 * fT = 300uA/V * 980K * 1.9GHz
    VDSSAT = 0.7V   GFT = 558.6GHz

For VGS = 2V   =>   GFT = gm * r0 * fT = 420uA/V * 370K * 2.7GHz
    VDSSAT = 1.2V   GFT = 419.6GHz

For VGS = 2.5V   =>   GFT = gm * r0 * fT = 500uA/V * 200K * 3.2GHz
    VDSSAT = 1.7V   GFT = 320GHz

Equation 9.59 is GFT = 3 * un / (2 * pi * L * L * lambda) where lambda = 1 / (r0 * IDSSAT). We are trying to show that GFT is approximately independent of biasing conditions. From VGS = 1.5V to 2.5V or over a 120uA to 530uA range (4.4X increase), GFT varied from 559GHz to 320GHz or decreased by 42%. Simulations showed that GFT decreases as the bias current is increased.

Name Vijayakumar Srinivasan
Problem 9.25
To calculate the ft of a short channel device and verify the same with
simulation.

The *ft* of a device is given by,
$$ft = (3Un*Vdssat)/(4Pi*(L^2)) = gm/(2*Pi*Cgs)$$
We know for a short channel device *gm= 150uA/V, Cgs= 4.17fF*
So, *ft=5.72GHz*
This is close to the theoretical value of 6GHz

Using simulation, with short channel models,
.control
destroy all

run
Let ft=mag(VDS#branch)/mag(VGS#branch)
plot 20*log(ft)
.endc

.option scale=50n
.ac dec 100 100M 10G

```
VDS     VDS    0       DC      1
VGS     VGS    0       DC      350m    AC 1m
M1      VDS    VGS     0       0       NMOS L=2 W=50
```
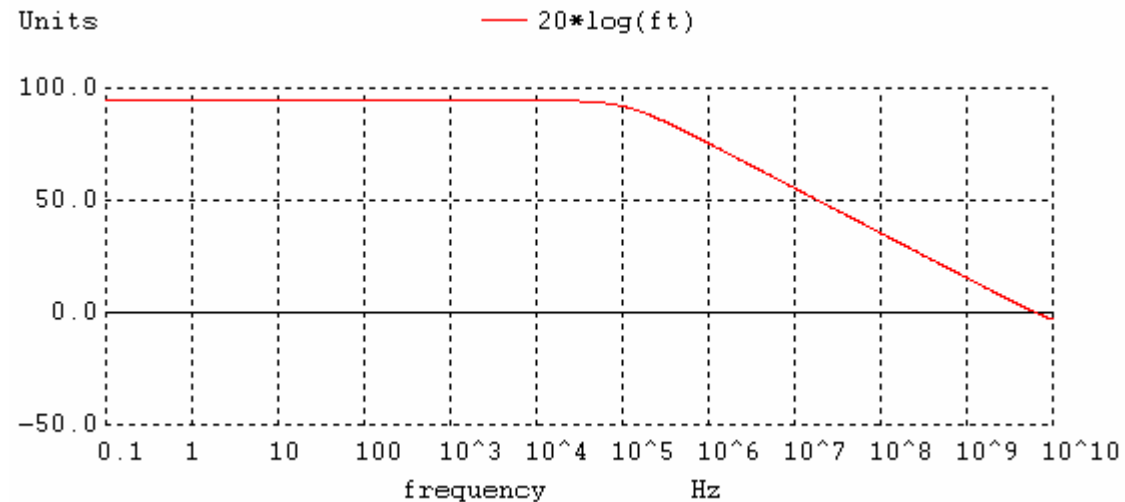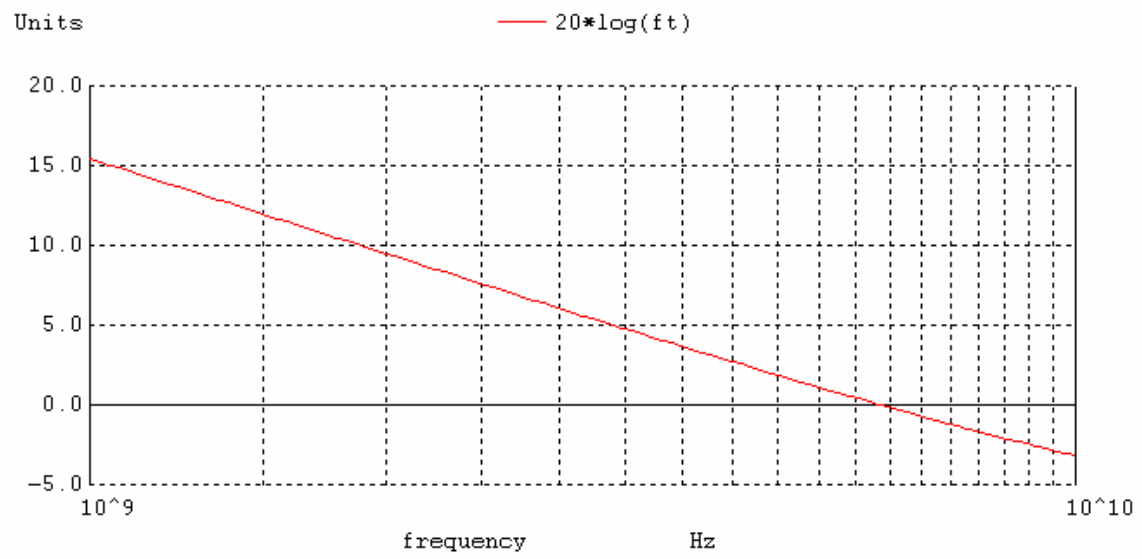
* BSIM4 models (model statements are not listed here)
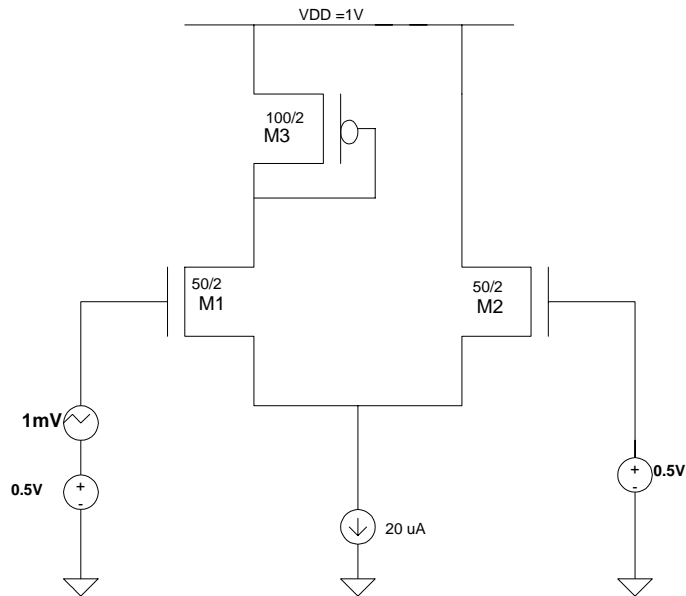.model   nmos   nmos   level = 14
.model   pmos   pmos   level = 14
.end

Using a 1GHz to 10GHz scale, we get a **ft close to 6.5GHz**

Problem 9.26

DC operating points:

The gates of both M1 and M2 are at 0.5v and the sources of M1 and M2 are tied together $V_{GS1}=V_{GS2}$ and ID1 =ID2=10uA

For short channel devices

$$V_{GS1} = V_{GS2} = \frac{I_D}{v_{sat}.C_{OX}'.W} + V_{THN} + V_{DSsat}$$

Substituting the values from the Table 9.2 for short channel devices we get

VGS1=VGS2=350mv

For PMOS M3 gate drain connected mosfet

$$V_{SG3} = \frac{I_D}{v_{sat}.C_{OX}'.W} + V_{THP} + V_{SDsat}$$

Substituting the values from the Table 9.2 for short channel devices we get

VSG3=350mv

Therefore Drain voltage of M1 is VD1=VG3=VD3= VDD-VSG3

VD1=650mv

Drain Voltage of M2 =VDD=1v

Ac Analysis:

The tranconductance of M1 and M2 is

$$g_{m1} = g_{m2} = v_{sat}.C_{OX}'.W$$
using table 9.2
$g_{m1}=g_{m2}=150uA/V$

We can replace Drain gate connected mosfet M3 with a resistor of $1/g_{m3}$
Where gm3 is calculated using table 9.2 as $g_{m3}=150uA/V$

Ac analysis of the circuit is

$$1mv= vgs1 - vgs2 = \frac{id1}{gm1} - \frac{id2}{gm2}$$

Here gm1=gm2 and id1=-id2

Therefore vgs1=-vgs2=0.5mv

The AC Drain currents are

id1=id3=gm1.vgs1=150uA/V . 0.5mV =75nA
Since id1=-id2, id2=-75nA
Therefore overall(AC+DC) drain currents are
i_{D1} = 10 + 0.075 SIN(2πf) uA
i_{D2} = 10 - 0.075 SIN(2πf) uA

AC drain voltages of M1 and M3 is

vd1=-id1. 1/gm3 =75n /150u = - 0.5mV

AC+DC drain voltages of M1 and M3 is

v_{D1} = 650 - 0.5 SIN(2πf) mv

For calculating AC drain voltage of M2
Output resistance of M2 is ro
Since M2 is in saturation
ro= $1/\lambda.I_D$
For short channel devices λ=0.6/V and I_D for M2 is 10uA
ro=167k ohms

AC drain voltages of M2
vd2=id2. ro =12.45mv

AC+DC drain voltages of M1 and M3 is

v_{D2} =1+0.01245 SIN(2πf) v

Since v_{D2} is 1+ac voltage there fore v_{D2} will stay at vdd since it can't go beyond vdd.

Simulations
*** Problem 9.26 CMOS: Circuit Design, Layout, and Simulation ***
.control
destroy all
run
** for the operating point analysis
*print all
*let vgs1=vg1-vs12
*let vgs2=vg2-vs12
*print vgs1 vgs2 vd13
let vd2=vdd
** for the AC analysis
*plot mag(vd13) mag(vdd)
** for the transient analysis
plot vd13
plot vd2
.endc
.option scale=50n
*.op
*.ac dec 100 1 10k
.tran 1u 300u

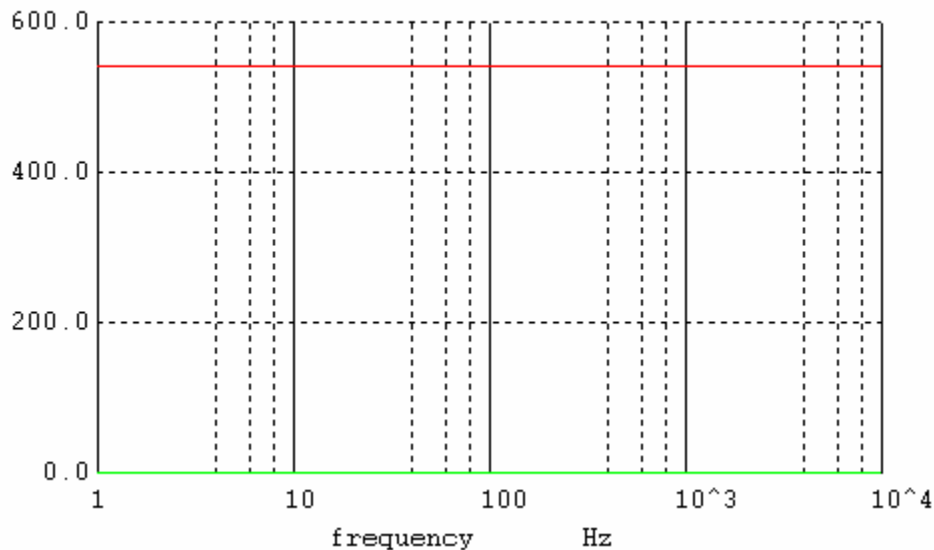| VDD | VDD | 0 | DC | 1 | | | |
VG1	VG1	0	DC	0.5	AC	1m	SIN 2.5 1m 10k
VG2	VG2	0	Dc	0.5			
Ibias	VS12	0	DC	20u			
M1	VD13	VG1	VS12	VS12	NMOS L=2 W=50		
M2	VDD	VG2	VS12	VS12	NMOS L=2 W=50		
M3	VD13	VD13	VDD	VDD	PMOS L=2 W=100		

DC Operating Point
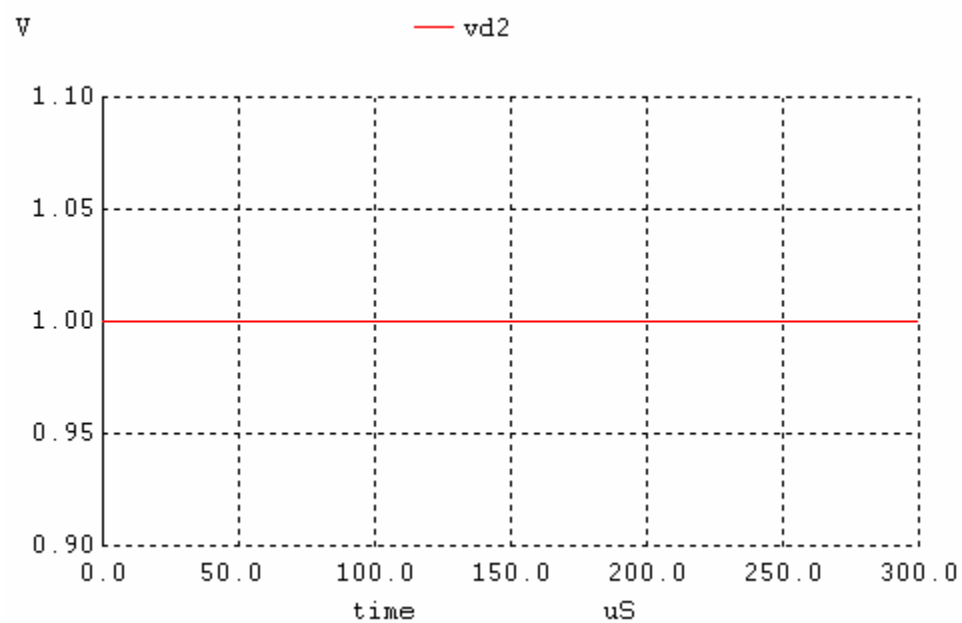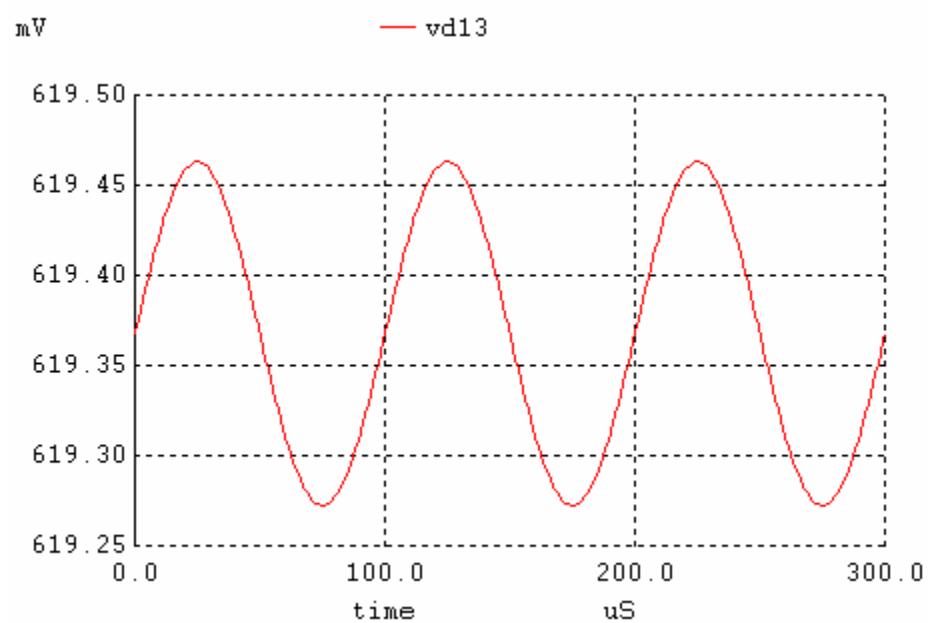vgs1 = 3.434905e-01
vgs2 = 3.434905e-01
vd13 = 6.525805e-01

Problem 9.27

The thermal noise of a MOSFET's drain current when operating in saturation is given by Equation (9.63).

$$I_R{}^2(f) = \frac{4\,KT}{\dfrac{3}{2} * \dfrac{1}{g_m}}$$

where the resistance is $\dfrac{3}{2} * \dfrac{1}{g_m}$

When the MOSFET is in DEEP TRIODE region, resistance is given by

$$R_{ch} = \frac{1}{g_m} \qquad \text{from equation (9.16)}$$

In between the deep triode and saturation regions, Thermal noise can be modeled with

$$\gamma \times \frac{1}{g_m}$$

where $1 < \gamma < 3/2$.

Problem 9.28

If we look at equation 9.66 we see that the total PSD of the mosfet drain noise current is proportional to the g_m

$$I_M{}^2 \propto g_m$$

So if we decrease g_m we can decrease $I_M{}^2$. but,

It will also decrease the signal to noise ratio (SNR). We would like to have as large of a signal to noise ratio as possible. Lets take a closer look.

Signal to Noise ratio = current through transistor/current noise

For the current through the transistor, let us take its square so we have;

. $i_{ds}{}^2 = gm^2 {*} v_{gs}{}^2$

so our signal to noise ratio becomes;

$$SNR = \frac{gm^2 \bullet v_{gs}{}^2}{\dfrac{KF \bullet I_D{}^{AF}}{f \bullet Cox^2 \bullet LW} + \dfrac{8kT}{3} \bullet gm}$$

If we then multiply the denominator by gm^2/gm^2 then our SNR becomes;

$$SNR = \frac{V_{gs}}{\dfrac{KF \bullet I_D{}^{AF}}{f \bullet C_{OX} \bullet LWgm^2} + \dfrac{8kT}{3 \bullet gm}}$$

Since the gm2 is proportional to I_D then the first term of the denominator wont change much as gm decreases. When we decrease gm the second term of the denominator will increase which will cause the SNR to decrease. For an amplifier we would like to have a large SNR and decreasing gm will decrease the SNR so although at first it appears to be a good way to decrease the noise, for an amplifier it negatively affects the SNR and is not a good idea.

9.29   Show how the thermal noise resistance of the channel seen in Eq. (9.63) is derived
for the MOSFET operating in the saturation region.

Equation (6.46) can be re-written without the area dependence as

$$Q'_I = \frac{2}{3} \cdot C'_{ox} \cdot (V_{GS} - V_{THN})$$

Plugging this into Eq. (6.27) and integrating

$$\int_0^{Rch} dR = \int_0^L \frac{1}{\mu_n \frac{2}{3} \cdot C'_{ox} \cdot (V_{GS} - V_{THN})} \cdot \frac{dy}{W}$$

Evaluating the integral gives

$$R_{ch} = \frac{1}{\frac{2}{3} \cdot \frac{W}{L} \mu_n C'_{ox} \cdot (V_{GS} - V_{THN})} = \frac{3}{2} \cdot \frac{1}{g_m}$$

which is the result seen in Eq. (9.63).