Kaijun Li

8.1 Show, using SPICE, how to adjust the phase and amplitude of the *I* and *Q* signals discussed in the beginning of the chapter to modulate the amplitude and phase of the resulting *I/Q* to construct a constellation diagram for 8-level rectangular *QAM*.

Solution:

Quadrature amplitude modulation (*QAM*) is basically trying to send two channels at the same bandwidth using single carrier frequency, so effectively the bandwidth that can be carried is being doubled. The constellation diagram for 8-level rectangular *QAM* is drawn in Figure 1, which means that there are two amplitude levels for *I* channel and no amplitude variation for *Q* channel.

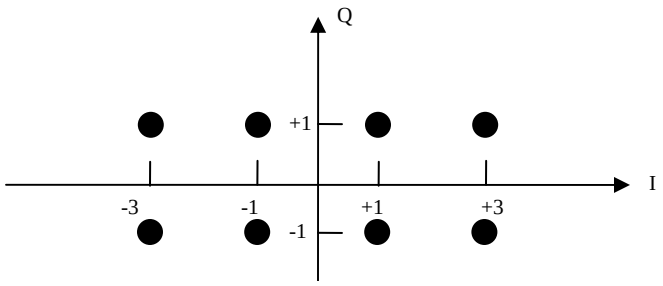


Figure 1. 8-level rectangular *QAM*

To show this in SPICE, we can first demonstrate how to the four dots on the upper plane where the Q channel has no phase shift. This is illustrated in Figure 2.

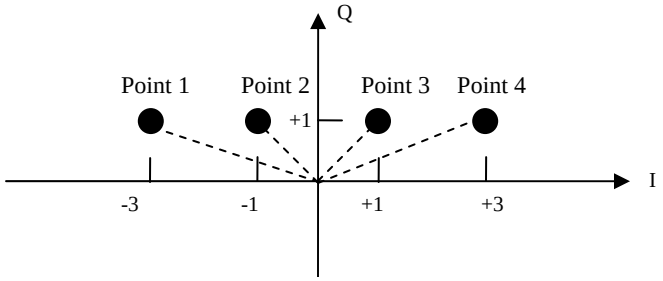


Figure 2. The modulation scheme for the first four points in the constellation diagram

In Figure 2, the amplitude and phase of Q channel signal are held constant, and the four points in Figure 2 are mapped to the amplitude and phase variations of *I* channel signals as follows:

Table 1. The amplitude and phase variations of *I* channel

	Point 1	Point 2	Point 3	Point 4
Amplitude	3	1	1	3
Phase	180˚	180˚	0˚	0˚

The SPICE simulation can be done and the schematic is shown in Figure 3.

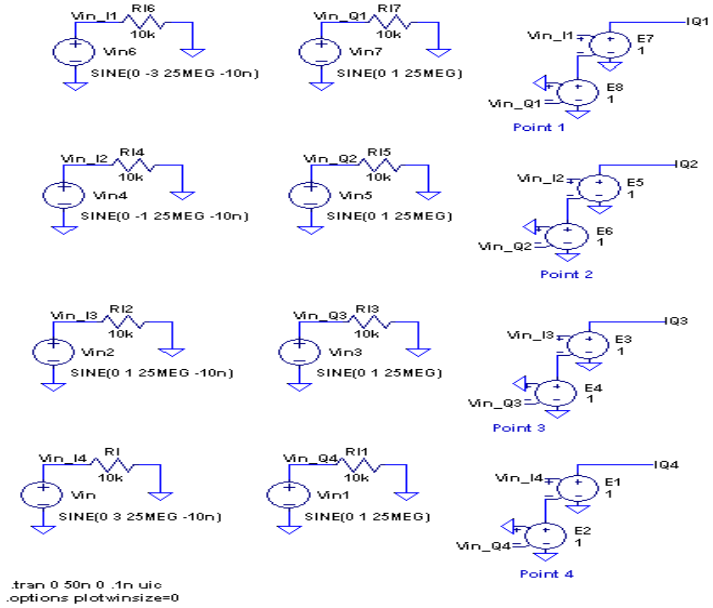


Figure 3. The schematic in SPICE for realization of the points in the upper half plane of the constellation diagram

The simulation results are shown Figure 4. The amplitude of point 1 in Figure 2 is supposed to be sqrt(3^2+1) or 3.16, and its phase is $\tan^{-1}$(1/(-3)) or 161.6˚. This is what we get in Figure 4.

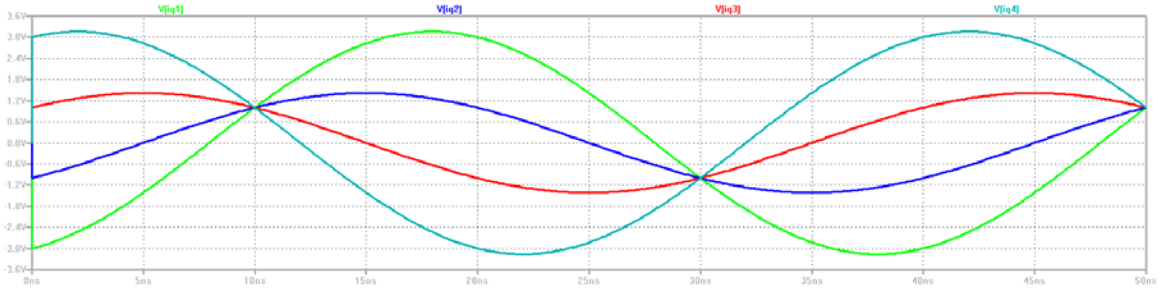


Figure 4. The four points in the upper plane of the constellation diagram realized in SPICE

Similarly, the other four points in the lower half plane of the constellation diagram can be realized. The schematic and the simulation results are seen in Figure 5 and Figure 6.

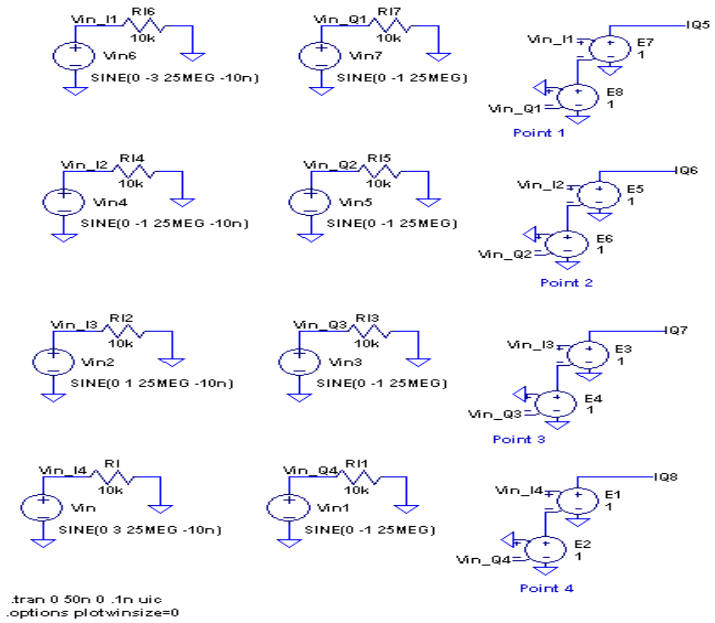


Figure 5. The schematic in SPICE for realization of the points in the lower half plane of the constellation diagram

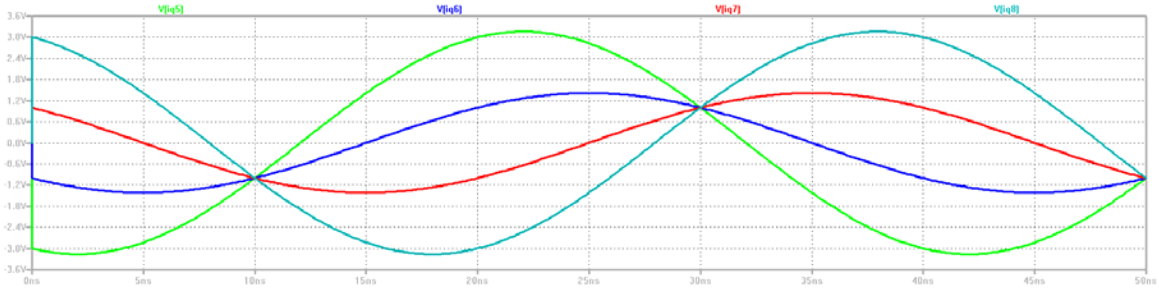


Figure 6. The four points in the lower half plane of the constellation diagram realized in SPICE

8.2) ***Suggest a topology for the bandpass passive-integrator NS modulator where the input and fed back signals are currents. Derive a transfer function for your design. Does your topology have the extra noise/distortion term seen in Eq. (8.12)? Why or why not? Simulate the operation of your design.***

Solution) We can use the bandpass modulator shown in Fig. 8.9, where a Low Noise Amplifier (LNA) is connected to a passive bandpass first order NS modulator. The figure is shown below in Fig. 1. The output of the LNA is a current $i_{in}= g_m v_{in}$, which is input to the NS modulator. The output of the modulator is a digital signal from the ADC, but it can be thought of as a current fedback i_{out}, to the resonator. Therefore the input and the fedback signals here are currents.

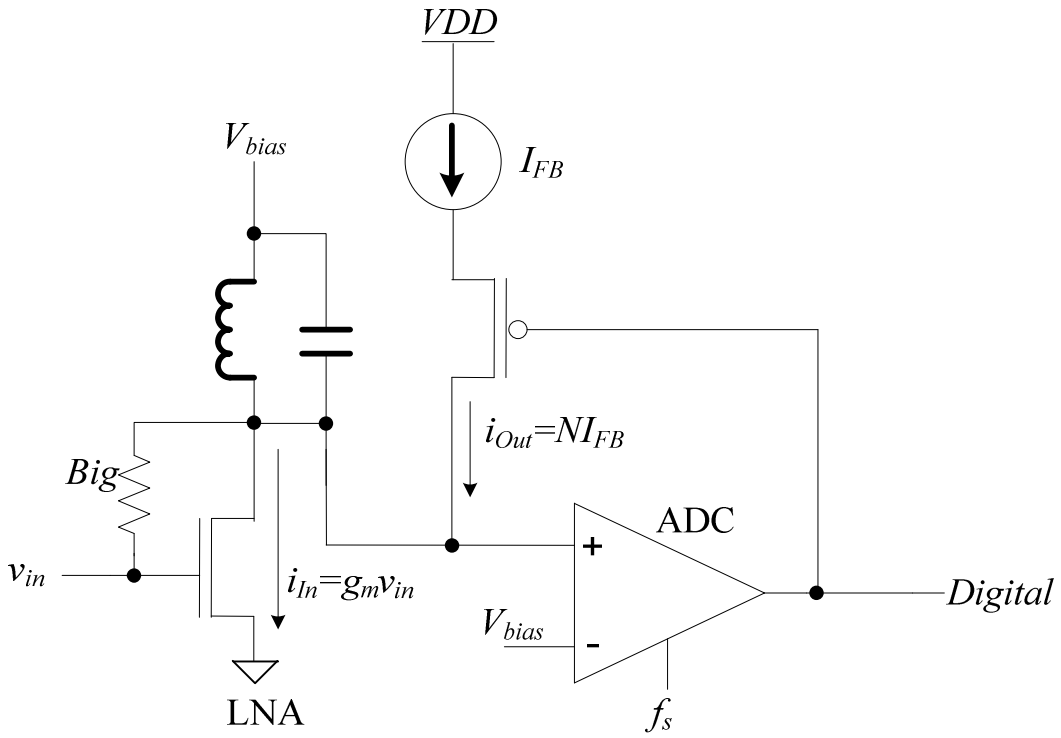


Figure 1: First order Bandpass NS Modulator

$$i_{in} = g_m v_{in} \quad \textbf{[1]}$$

The output current that is fedback to the resonator is equal to $N.I_{FB}$, where N is the number of times the output of the modulator goes low to keep the voltage on its positive input on an average equal to V_{bias}.

$$i_{Out} = N \cdot I_{FB} \quad \textbf{[2]}$$

Therefore on average the voltage on the positive input of the modulator is equal to

$$\left(i_{in} - i_{Out}\right) \cdot \left(sL // \left(1/sC\right)\right) = g_m v_{in} - N \cdot I_{FB} \quad \textbf{[3]}$$

$$\left(i_{in} - i_{Out}\right) \cdot \left(sL // \left(1/sC\right)\right) = \left(i_{in} - i_{Out}\right) \cdot \left(\frac{sL}{1+s^2LC}\right) \quad \textbf{[4]}$$

i_{Out} can be related to v_{Out} as $i_{Out} = v_{Out} . g_{m,Out,}$ where $g_{m,Out}$ is the effective transconductance relating the digital output voltage to the fedback current.

Therefore Eq. 4 can be written as,

$$\left(i_{in}-i_{Out}\right)\cdot\left(\frac{sL}{1+s^2LC}\right)=\left(g_m v_{in}-g_{m,Out}v_{Out}\right)\cdot\left(\frac{sL}{1+s^2LC}\right) \quad \textbf{[5]}$$

Since the ADC adds quantization noise $V_{Qe}(f)$, we can write the final output voltage Vout to be equal to,

$$v_{Out}=\left(g_m v_{in}-g_{m,Out}v_{Out}\right)\cdot\left(\frac{sL}{1+s^2LC}\right)+V_{Qe}(f) \quad \textbf{[6]}$$

$$v_{Out}\left(1+g_{m,Out}\left(\frac{sL}{1+s^2LC}\right)\right)=g_m v_{in}\cdot\left(\frac{sL}{1+s^2LC}\right)+V_{Qe}(f) \quad \textbf{[7]}$$

$$v_{Out}\left(\frac{1+s^2LC+sL\cdot g_{m,Out}}{1+s^2LC}\right)=g_m v_{in}\cdot\left(\frac{sL}{1+s^2LC}\right)+V_{Qe}(f) \quad \textbf{[8]}$$

$$v_{Out}=v_{in}\cdot\overbrace{\left(\frac{sL\cdot g_m}{s^2LC+sL\cdot g_{m,Out}+1}\right)}^{STF,BandPass}+V_{Qe}(f)\cdot\overbrace{\left(\frac{1+s^2LC}{s^2LC+sL\cdot g_{m,Out}+1}\right)}^{NTF,Bandreject} \quad \textbf{[9]}$$

Using this topology, as the comparator can on average hold its positive input node to a constant potential, we do not get the extra noise/distortion term seen in Eq. 8.12.

Let's use LTSpice to simulate the design; the input to the LNA is a 25MHz, 4V peak to peak sinusoidal signal with 2.5V DC offset. Since we need to be able to recover the input signal after eliminating the modulation nosie at the output, the center frequency for the bandpass should be at 25MHz. Therefore we can choose C=10pF and L=4.06uH, giving us a center frequency of $f_0=1/[2\pi\sqrt{(LC)}]=25MHz$.

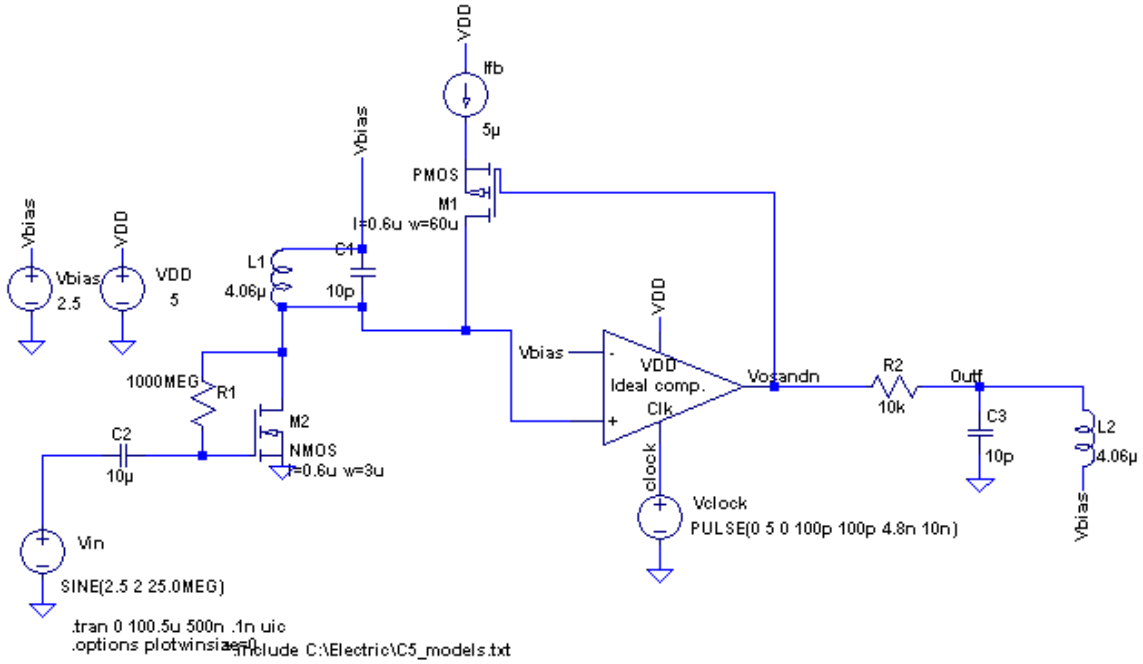


Figure 2: LTSpice Simulation of the Bandpass NS Modulator

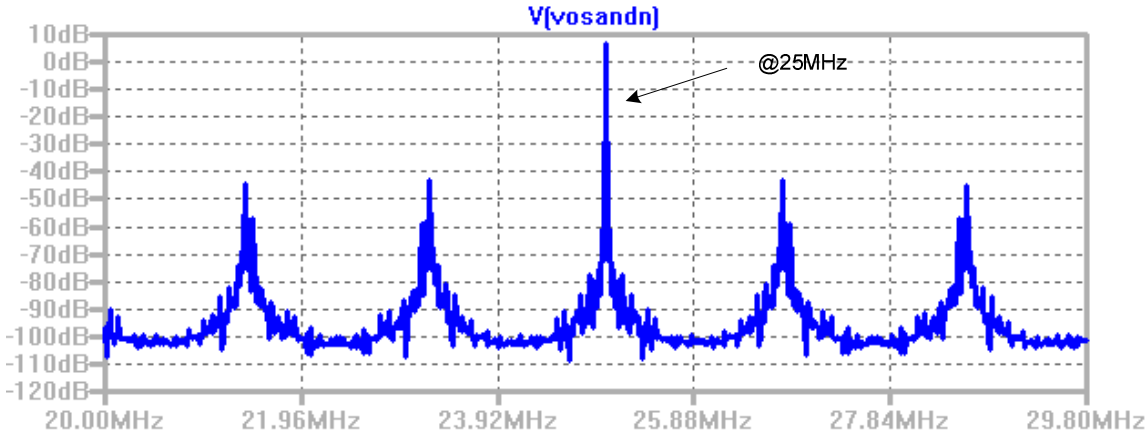


Figure 3: FFT of the output signal from the modulator

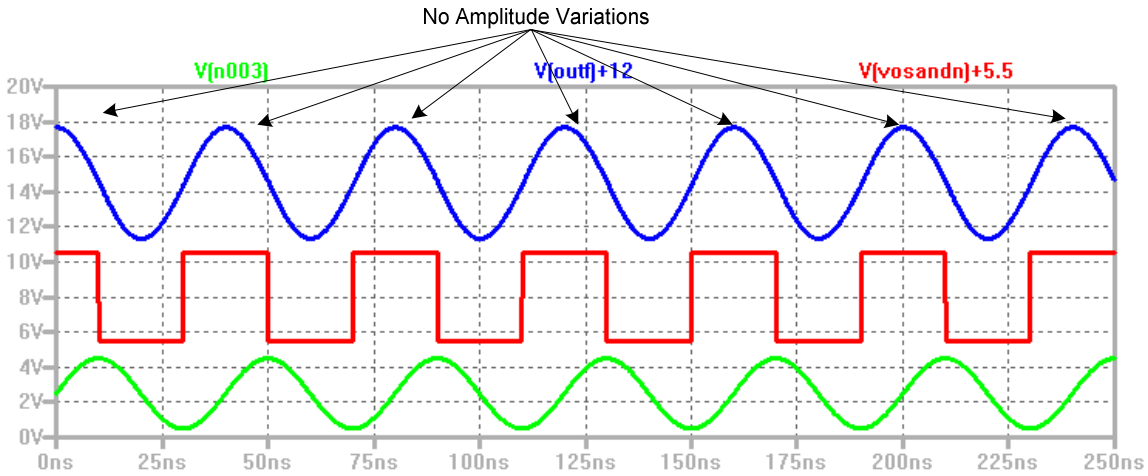


Figure 4: Time Domain simulation of the NS modulator

From Fig.4 we can see that the filtered output signal has no amplitude variations unlike the bandpass modulator shown in Fig. 8.2 of the textbook. This is due to the fact that the comparator on an average keeps the voltage on its positive input terminal constant.

Lincoln Bollschweiler

8.3 Show the detailed derivation of the transfer function for the modulator in Fig. 8.6.

Assume $V_{CM} = 0$ to simplify the derivation. Any DC bias or offset subtracts out. Also assume that v_{int} is the output of the integrator, input of quantizer (not the node drawn in Fig. 8.6).

Starting with the equations for the integrator:

$$\frac{v_{in}}{R} - \frac{v_o}{R} = \frac{-v_{\text{int}}}{sL \,||\, \frac{1}{sC}} \tag{1}$$

$$sL \,||\, \frac{1}{sC} = \frac{1}{\frac{1}{sL} + sC} = \frac{sL}{s^2LC + 1} \tag{2}$$

Plugging (2) into (1)

$$\frac{v_{in}}{R} - \frac{v_o}{R} = -v_{\text{int}} \left(\frac{s^2LC + 1}{sL} \right)$$

$$-v_{\text{int}} = \left(\frac{v_{in} - v_o}{R} \right) \cdot \left(\frac{sL}{s^2LC + 1} \right) \tag{3}$$

Moving on to equations for the quantizer:

$$v_o = -v_{\text{int}} + v_{Qe} \tag{4}$$

Plugging (3) into (4)

$$v_o = \left(\frac{v_{in} - v_o}{R} \right) \cdot \left(\frac{sL}{s^2LC + 1} \right) + v_{Qe}$$

$$v_o \left(\frac{s^2LRC + sL + R}{s^2LRC + R} \right) = v_{in} \left(\frac{sL}{s^2LRC + R} \right) + v_{Qe}$$

$$v_o = v_{in} \left(\frac{sL}{s^2LRC + R} \right) \cdot \left(\frac{s^2LRC + R}{s^2LRC + sL + R} \right) + v_{Qe} \left(\frac{s^2LRC + R}{s^2LRC + sL + R} \right)$$

$$v_o = v_{in} \left(\frac{sL}{s^2LRC + sL + R} \right) + v_{Qe} \left(\frac{s^2LRC + R}{s^2LRC + sL + R} \right) \tag{5}$$

Divide numerator and denominator by LRC to obtain

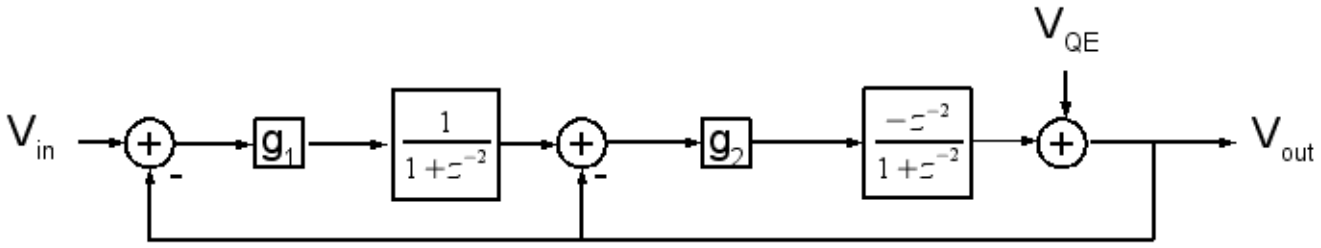
$$v_o = v_{in} \underbrace{\left(\frac{\frac{s}{RC}}{s^2 + \frac{s}{RC} + \frac{1}{LC}} \right)}_{\text{STF}(f)} + v_{Qe} \underbrace{\left(\frac{s^2 + \frac{1}{LC}}{s^2 + \frac{s}{RC} + \frac{1}{LC}} \right)}_{\text{NTF}(f)}. \tag{6}$$

■

Jason Durand

Problem 8.4 – Show the details of deriving the transfer function for the modulator in Fig 8.8.

The modulator in Fig 8.8 is a 'second order noise shaping' bandpass modulator, so it can only be implemented as a fourth order system. This is described best by the block diagram as seen below.



Note that the first integrator is non delaying, which just means that the half clock cycle delay is just seen as a delay on the input signal, and has no effect on the rest of the transfer function. If you follow the values at each node starting from the first summing node to the end, you get

$$\left[\frac{G_1(V_{in}-V_{out})}{1+z^{-2}}-V_{out}\right]\cdot\left(\frac{-G_2z^{-2}}{1+z^{-2}}\right)+V_{QE}=V_{out}\,.$$

Next, multiply both sides by $(1+z^{-2})$ and expand the terms.

$$\frac{-G_1G_2z^{-2}}{1+z^{-2}}\cdot V_{in}+\left(1+z^{-2}\right)\cdot V_{QE}=\frac{-G_1G_2z^{-2}}{1+z^{-2}}\cdot V_{out}-G_2z^{-2}\cdot V_{out}+\left(1+z^{-2}\right)\cdot V_{out}$$

Collect all V_{out} terms and multiply by $(1+z^{-2})$ again.

$$\left(\left(1+z^{-2}\right)^2-G_1G_2z^{-2}-G_2z^{-2}\left(1+z^{-2}\right)\right)\cdot V_{out}=-G_1G_2z^{-2}\cdot V_{in}+\left(1+z^{-2}\right)^2\cdot V_{QE}$$

Note that the block diagram represents the comparator as only adding noise to the system. While this is true, the comparator is the source of quantization error in the system, it also has a gain that complements the gain of each integration stage, making the overall gain of the system (ideally) one. This can be represented in the equations by setting the gains G_1 and G_2 equal to one, which greatly simplifies the transfer function.

$$\left(1+2z^{-2}+z^{-4}-z^{-2}-z^{-2}-z^{-4}\right)\cdot V_{out}=z^{-2}\cdot V_{in}+\left(1+z^{-2}\right)^{-2}\cdot V_{QE}$$

$$V_{out}=z^{-2}\cdot V_{in}+\left(1+z^{-2}\right)^{-2}\cdot V_{QE}$$

The output of the system is simply the delayed input, and the quantization noise gets second order shaping, about the frequency $f_s/4$.

Jake Baker

8.5 Derive the transfer function for the modulator seen in Fig. 8.9.

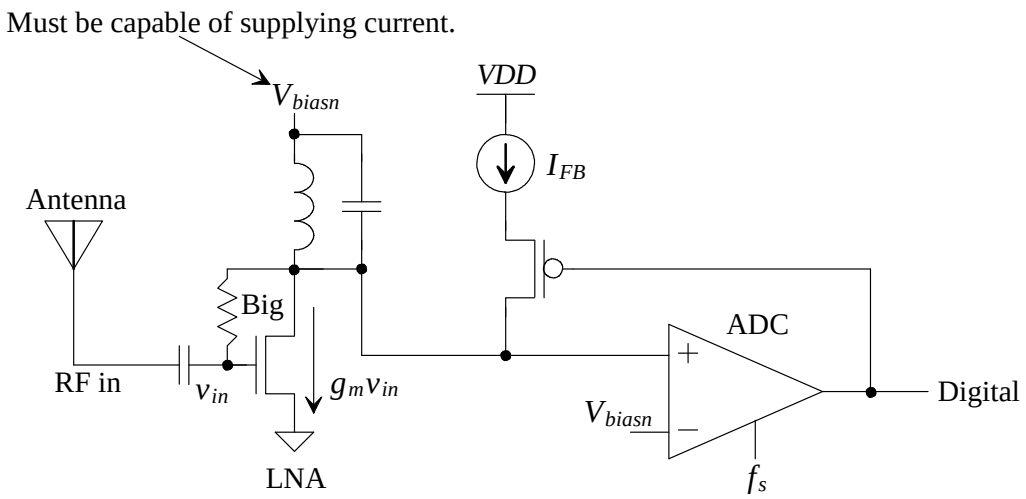
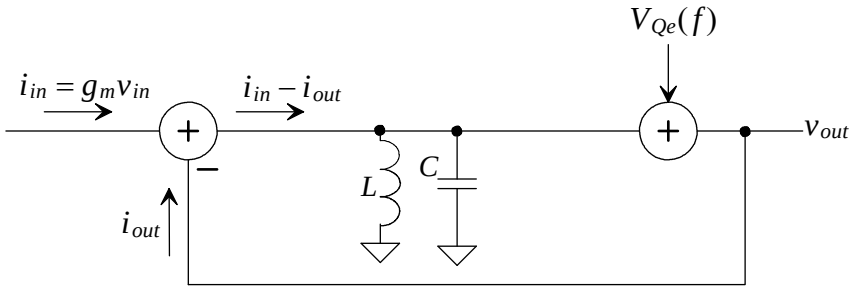


Figure 8.9 Design of a bandpass modulator for data conversion at RF.

The simplified representation of this schematic is seen below.



The voltage on the drain of the MOSFET can be written as

$$(i_{in} - i_{out}) \cdot \frac{sL}{1 + s^2 LC}$$

and knowing $i_{in} = g_m v_{in}$ and $i_{out} = g_{m,out} v_{out}$ (where $g_{m.out}$ is the effective transconductance relating the digital output voltage to the current I_F) we can write

$$v_{out} = V_{Qe}(f) + (g_m v_{in} - g_{m,out} v_{out}) \cdot \frac{sL}{1 + s^2 LC}$$

and

$$v_{out}\left(1 + \frac{g_{m,out} \cdot sL}{1 + s^2 LC}\right) = V_{Qe}(f) + \frac{sL g_m v_{in}}{1 + s^2 LC} = v_{out}\left(\frac{s^2 LC + g_{m,out} \cdot sL + 1}{1 + s^2 LC}\right)$$

so knowing that, on average, $i_{in} = i_{out}$ and thus $g_m = g_{m,out}$ we get

$$v_{out} = V_{Qe}(f) \cdot \underbrace{\frac{s^2 LC + 1}{s^2 LC + g_{m,out} \cdot sL + 1}}_{NTF\text{, Bandstop response, Fig. 8.3}} + v_{in} \cdot \underbrace{\frac{sL g_m}{s^2 LC + g_{m,out} \cdot sL + 1}}_{STF\text{, Bandpass response}}$$

8.6. Sketch the implementation of a modulator, based on the topology seen in Fig. 8.9, but using multi-bit quantizer and feedback DAC.

Sol. Before looking at the implementation of band pass modulator with an N-bit quantizer let us look at band pass modulator with a 1-bit quantizer (see Figure 8.9 in the book). The reference current (I_{FB}) is steered on to the drain of the input NMOS transistor, when the output of the ADC goes low. Current (i.e. I_{FB}) is steered on to the drain of the NMOS transistor at the input when the output of the ADC goes low. The same concept of feeding current based on the digital outputs of the ADC can be applied in the case of band pass modulator with N-bit quantizer.

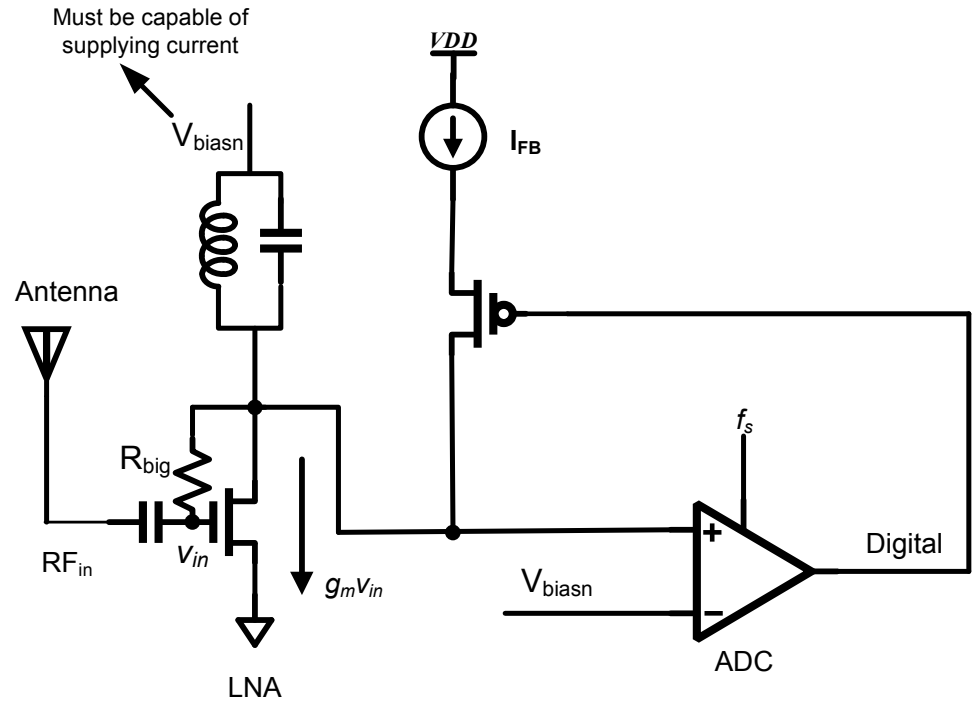


Figure 1. Band pass modulator for data conversion at RF (see Figure 8.9 in book)

If the 1-bit ADC in Fig 1 is replaced with an N-bit quantizer (or ADC), we need to steer weighted currents on to the drain of the NMOS based on the digital output values of the ADC. This can be realized by using a weighted current steering DAC as shown in Figure 2. The weighted current steering DAC is shown in Figure 2. The DAC outputs weighted currents when the individual digital inputs are zeroes, or else outputs zero currents. These output currents from the DAC are steered on to the drain of the NMOS transistor at input. A reference current I_{ref} is chosen such that it is much bigger than the input current $i_{in}=g_m v_{in}$. Then the equations for the output currents of the DAC are given below.

$$I_{0} = I_{in(0)} = \frac{2^0}{2^N} \cdot I_{ref} \text{ when } D_0=0 \text{ and } I_0 = 0 \text{ when } D_0 = 1 \qquad (1)$$

$$I_1 = I_{in(1)} = \frac{2^1}{2^N} \cdot I_{ref} \text{ when } D_1=0 \text{ and } I_1 = 0 \text{ when } D_1 = 1 \quad (2)$$

.....

$$I_{N-1} = I_{in(N-1)} = \frac{2^{N-1}}{2^N} \cdot I_{ref} \text{ when } D_0=0 \text{ and } I_{N-1} = 0 \text{ when } D_{N-1} = 1 \quad (3)$$

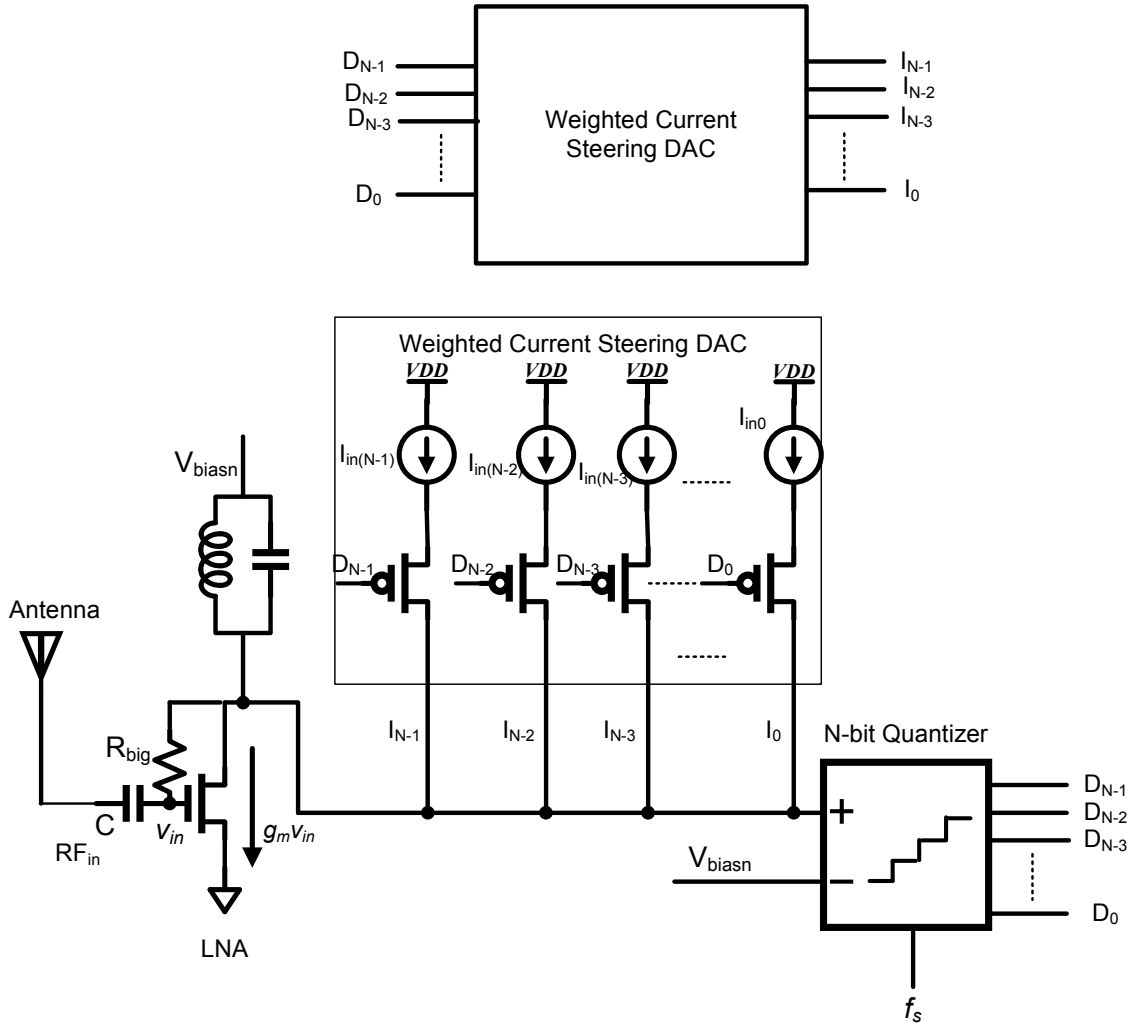


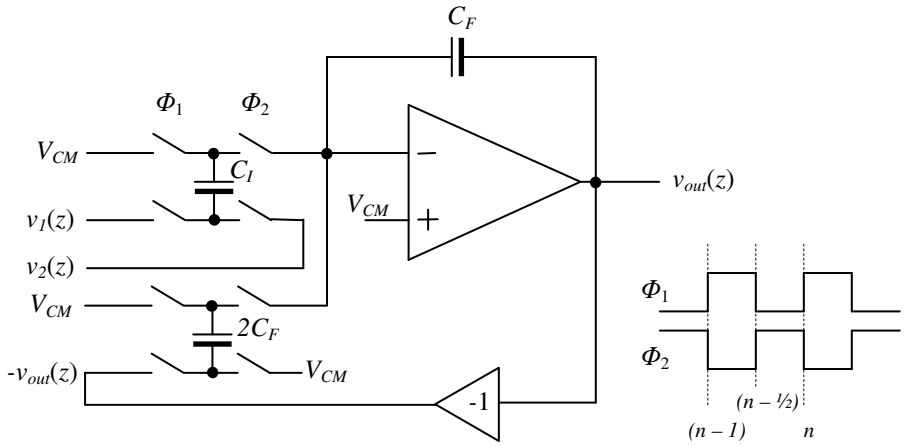
Figure 2. Band pass modulator for N-bit quantizer

Note: The total current supplied on to the drain of the input NMOS transistor when all the digital outputs of the N-bit quantizer are zero is given by $\frac{(2^N-1)}{2^N} \cdot I_{ref}$. For example in case of a 2-bit quantizer the maximum current steered on to the drain is $\frac{(2^2-1)}{2^N} \cdot I_{ref} = \frac{3}{4} \cdot I_{ref}$.

8.7 Show the details of how Eq. (8.18) is derived.

$$v_{out}(z) = \frac{v_1(z)\cdot z^{-1/2} - v_2(z)}{1+z^{-1}} \cdot \frac{C_I}{C_F}$$

Equation 8.18 is the transfer function for the $f_s/2$ resonator seen in F-1.



F-1 Implementing and $f_s/2$ resonator for use in a band-pass modulator

Charge conservation states that the charge flowing into a network is equal to the charge leaving the network. When viewing F-1 the charge is leaving through the feedback capacitor. We can characterize this charge over one clock cycle and say:

$$\left(v_{out}(z)[nT_s]C_F - V_{CM}\right) - \left(v_{out}(z)\left[(n-1)T_s\right]C_F - V_{CM}\right)$$

It is clear that the common mode voltage cancels out. We can also take this time domain equation into the z-domain by substituting $z = e^{j2\pi f \cdot T_s}$:

$$v_{out}(z)\left(1-z^{-1}\right)C_F$$

The above equation is the difference in charge (current) which flows to the output. To determine the charge that is flowing into the inverting terminal of the op-amp we have to realize that we defined the time when Φ_2 goes low as nT_s. From this definition we can see that the v_1 signal experiences ½ a clock cycle delay, v_2 experiences no delay, and the v_{out} signal must experience a full clock cycle delay.

Let's look at the contribution from v_1 and v_2:

$$Q_1 = \left(V_{CM} - v_1(z)\left[(n-1/2)T_s\right]\right)C_I$$

$$Q_1 = \left(V_{CM} - v_1(z)\, z^{-1/2}\right) C_I$$

$$Q_2 = \left(V_{CM} - v_2(z)\left[nT_s\right]\right) C_I$$

$$Q_2 = \left(V_{CM} - v_2(z)\right) C_I$$

$$Q_2 - Q_1 = Q_{out}$$

$$\left(V_{CM} - v_2(z)\right) C_I - \left(V_{CM} - v_1(z)\, z^{-1/2}\right) C_I = \left(v_1(z)\, z^{-1/2} - v_2(z)\right) C_I$$

The contribution from the v_{out} is:

$$-v_{out}\left[(n-1)T_s\right] 2C_F = -v_{out} z^{-1} 2C_F$$

Notice the V_{CM} terms are removed from this equation. We can use charge conservation to say:

$$\left(v_1(z)\, z^{-1/2} - v_2(z)\right) C_I - v_{out} z^{-1} 2C_F = v_{out}(z)\left(1 - z^{-1}\right) C_F$$

$$\left(v_1(z)\, z^{-1/2} - v_2(z)\right) C_I = v_{out}(z)\left(1 - z^{-1}\right) C_F + v_{out} z^{-1} 2C_F$$

$$\left(v_1(z)\, z^{-1/2} - v_2(z)\right) C_I = v_{out}(z)\left(1 + z^{-1}\right) C_F$$

$$\frac{v_1(z)\, z^{-1/2} - v_2(z)}{1 + z^{-1}} \cdot \frac{C_I}{C_F} = v_{out}(z)$$

Q 8.8 Derive the transfer function of the modulator seen in Fig. 8.12

Sol. Figure 1 shows the schematic of fig. 8.12 on page 294. In order to derive the transfer function charge transfer from input to output is analyzed. Output signal is clocked at ϕ_1 and op-amp is considered ideal.

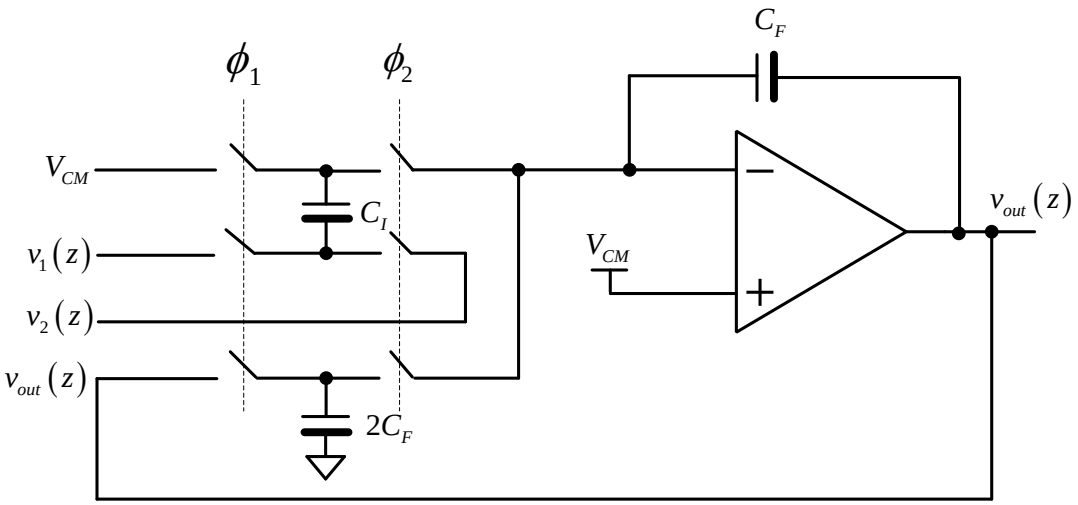


Figure 1 implementing a resonator for use in a bandpass modulator

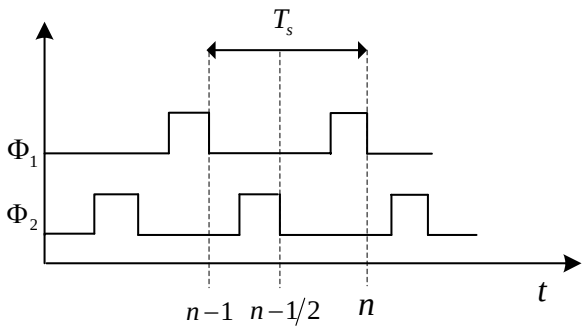


Figure 2 Timing diagram for the switched capacitor modulator clocks

At the instant $(n-1)T_s$ and $(n-1/2)T_s$ the circuit can be realized as seen in Fig. 3 and Fig. 4

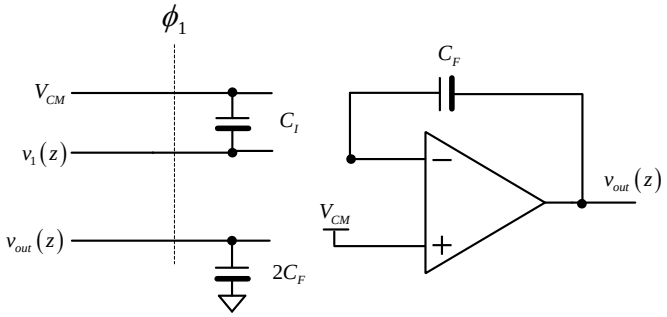


Figure 3 Circuit when ϕ_1 switch is closed

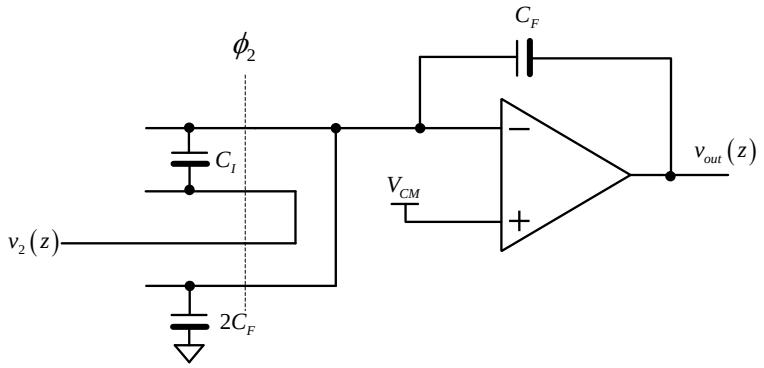


Figure 4 Circuit when ϕ_2 switch is closed

Initial charge in the circuit across different capacitors at time $(n-1)T_s$, at the falling edge of ϕ_1

$$Q_{iniC_I}: \quad C_I\left(V_{CM} - v_1\left[(n-1)T_S\right]\right)$$
$$Q_{iniC_F}: \quad C_F\left(v_{out}\left[(n-1)T_S\right] - V_{CM}\right)$$
$$Q_{ini2C_F}: \quad 2C_F\left(v_{out}\left[(n-1)T_S\right]\right)$$

Now looking at the output at instance $(n)T_s$ since it is clocked at ϕ_1 and charge across the other capacitors at $(n-1/2)T_s$

$$Q_{finC_I}: \quad C_I\left(V_{CM} - v_2\left[(n-1/2)T_S\right]\right)$$
$$Q_{finC_F}: \quad C_F\left(v_{out}\left[(n)T_S\right] - V_{CM}\right)$$
$$Q_{fin2C_F}: \quad 2C_F\left(V_{CM}\right)$$

As assumed that op-amp is ideal the change in charge across C_I and $2C_F$ is dumped across the feedback capacitor of the op-amp, thus by charge conservation

$$Q_{finC_F} - Q_{iniC_F} = \left(Q_{finC_I} - Q_{iniC_I}\right) + \left(Q_{fin2C_F} - Q_{ini2C_F}\right)$$

$$C_F\left(v_{out}\left[(n)T_S\right] - v_{out}\left[(n-1)T_S\right]\right) = C_I\left(v_1\left[(n-1)T_S\right] - v_2\left[(n-1/2)T_S\right]\right) + 2C_F\left(V_{CM} - v_{out}\left[(n-1)T_S\right]\right)$$

Putting the equation in terms of z^{-1} and assuming the constant term as zero because it is a reference DC voltage and rearranging the v_{out} together

$$C_F\left(v_{out} + v_{out}z^{-1}\right) = C_I\left(v_1z^{-1} - v_2z^{-1/2}\right)$$

$$v_{out} = \frac{C_I}{C_F}\frac{\left(v_1 z^{-1} - v_2 z^{-1/2}\right)}{1+z^{-1}}$$

Thus transfer function of circuit with respect to v_1 is $\frac{v_{out}}{v_1} = \frac{C_I}{C_F}\cdot\frac{z^{-1}}{1+z^{-1}}$ and with respect to v_2 is given as $\frac{v_{out}}{v_2} = \frac{C_I}{C_F}\cdot\frac{-z^{-1/2}}{1+z^{-1}}$

Solution by Geng Zheng

8.9 Using the modulator topology in Ex. 8.4, show that if we apply a 25 MHz input sinusoid to the modulator we can recover this input signal by passing the output digital data through a bandpass filter with a very small bandwidth (show that the input and output signal amplitudes are equal).

Solution:

For simplicity we can use the second-order bandpass filter, Fig. 1, with a transfer function

$$\frac{v_{out}}{v_{in}} = \frac{s\frac{1}{RC}}{s^2 + s\frac{1}{RC} + \frac{1}{LC}} \tag{1}$$

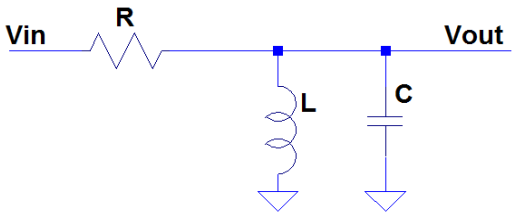


Figure 1 Second-order bandpass filter.

We need to pick the values for R, L, and C so

$$f_o = \frac{1}{2\pi\sqrt{LC}} = 25\,MHz \tag{2}$$

We also want the filter to have a very small bandwidth. Here we arbitrarily set the bandwidth, B to 410 kHz (the pass frequency range of the filter is $25\,MHz \pm 410\,kHz$). Then the required Q factor is

$$Q = \frac{f_o}{2B} = \frac{25\,MHz}{820\,kHz} = 30.5 \tag{3}$$

This filter has a very high Q! In practical implementation, a biquad active-RC, gm-C, or switched-capacitor implementation may be used. Setting $C = 10\ pF$ and using Eq. 2 we get $L = 4.05\,uH$.

Also knowing

$$Q = R\sqrt{\frac{C}{L}} \tag{4}$$

we can have $R = 20\,k\,\Omega$.

The frequency response of this bandpass filter is shown in Fig. 2.

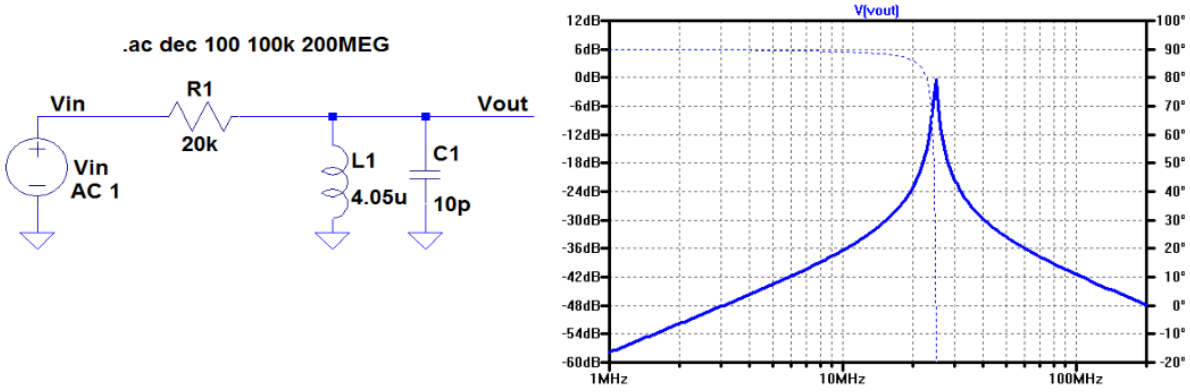


Figure 2 The frequency response of the high-Q bandpass filter.

Using this bandpass filter to filter the modulator output in Ex. 8.4 (with a 25 MHz input) results in the time domain filtered output shown in Fig. 3. There is only small difference between the amplitude of the input and the filtered output.

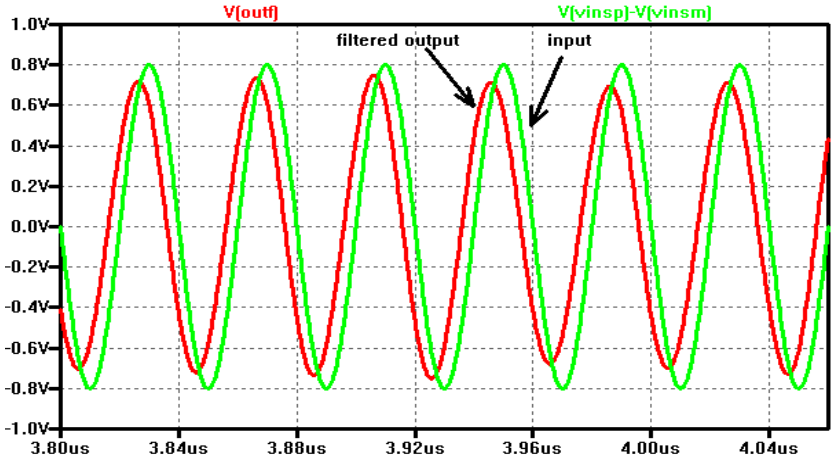


Figure 3 The input and the filtered output of Ex. 8.4.

Fig. 4 shows (a) the output spectral before filtering and (b) the filtered output spectral.

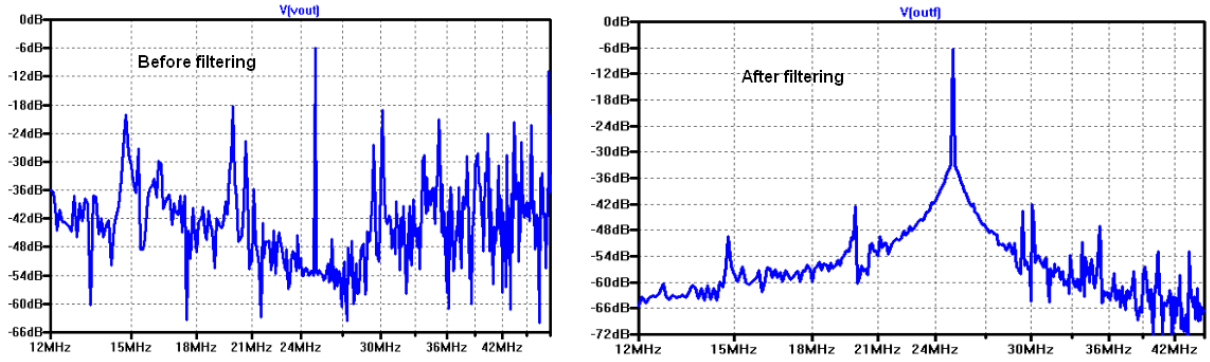


Figure 4 The output spectral of the modulator.

Q.8.10 Derive the transfer function of the topology seen in Fig. 8.17. Verify that the topology is unstable by determining the location of the topology's poles.

Sol. The block diagram of Fig. 8.17 is shown below

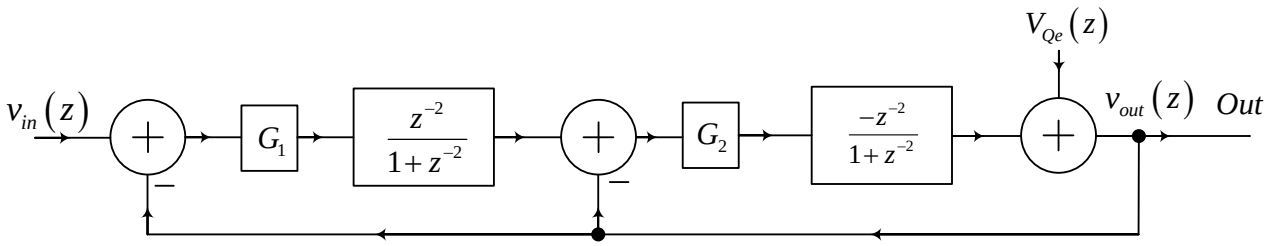


Figure 1 A fourth-order band pass modulator using two delaying resonators (unstable)

Looking at the block diagram, the output $v_{out}(z)$ is given as

$$\left(\left(\left(v_{in}(z)-v_{out}(z)\right)\cdot G_1\cdot\frac{z^{-2}}{1+z^{-2}}\right)-v_{out}(z)\right)\cdot G_2\cdot\frac{-z^{-2}}{1+z^{-2}}+V_{Qe}(z)=v_{out}(z)$$

$$\left(v_{in}(z)\cdot G_1\cdot\frac{z^{-2}}{1+z^{-2}}-v_{out}(z)\cdot G_1\cdot\frac{z^{-2}}{1+z^{-2}}-v_{out}(z)\right)\cdot G_2\cdot\frac{-z^{-2}}{1+z^{-2}}+V_{Qe}(z)=v_{out}(z)$$

$$\frac{-v_{in}(z)G_1G_2z^{-4}}{\left(1+z^{-2}\right)^2}+\frac{v_{out}(z)G_1G_2z^{-4}}{\left(1+z^{-2}\right)^2}+\frac{v_{out}(z)G_2z^{-2}}{1+z^{-2}}+V_{Qe}(z)=v_{out}(z)$$

Simplifying it further provides

$$v_{out}(z)=\frac{-v_{in}G_1G_2z^{-4}+V_{Qe}\cdot\left(1+z^{-2}\right)^2}{\left(1-G_1G_2-G_2\right)z^{-4}+(2-G_2)z^{-2}+1}$$

Analyzing the denominator of above equation to determine the poles of the system

$$\left(1-G_1G_2-G_2\right)z^{-4}+(2-G_2)z^{-2}+1=0$$

$$z^{-2}=\frac{-(2-G_2)\pm\sqrt{(2-G_2)^2-4\left(1-G_1G_2-G_2\right)}}{2\times\left(1-G_1G_2-G_2\right)}$$

The stability criteria condition on the forward gain of the second-order low pass modulator is $0\le G_F\le 1.333$. The forward gain of modulator shown in Fig. 1 is $G_F=G_1G_2$ (quantizer gain is not considered, one bit quantizer has undefined gain).As suggested in the text, assuming the forward gain of the fourth-order band pass modulator should follow the same criteria for

stability, the gain of modulator in Fig.1 is assumed as $G_F = 1$ (taking into the account that 1-bit quantizer adjusts its gain).

With $G_F = G_1 G_2 = 1$, setting $G_1 = G_2 = 1$ putting the values in equation below:

$$z^{-2} = \frac{-(2 - G_2) \pm \sqrt{(2 - G_2)^2 - 4\left(1 - G_1 G_2 - G_2\right)}}{2 \times \left(1 - G_1 G_2 - G_2\right)}$$

$$z^{-2} = \frac{-1 \pm \sqrt{5}}{-2}$$

The poles of system are at $z_{p1} = 1.27$, $z_{p2} = -1.27$, $z_{p3} = j0.787$, $z_{p4} = -j0.787$ looking at the values we can say that the system is unstable because the two poles are outside the unit circle. Also note that if we assume the value of either G_1 is less than 1 then G_2 will be greater than 1 and vice-versa, which will still result in poles outside the unit circle. Thus the modulator is inherently unstable because of excess delay in the system.

Q8.11 Using a bandpass modulator and digital demodulation (sketch the schematic of your design) show how to recover 10 KHz sine wave that is amplitude modulated with a carrier frequency of 1 MHz. Use SPICE to verify the operation of your design.

Sol. Figure 1 below shows the block diagram of bandpass modulator and digital demodulation scheme, input signal should be centered at $f_s/4$ for the resonator used in bandpass modulator. The given carrier frequency is 1 MHz thus effective sampling frequency will be 4 MHz for signal to be recovered from the bandpass modulator centered at $f_s/4$.

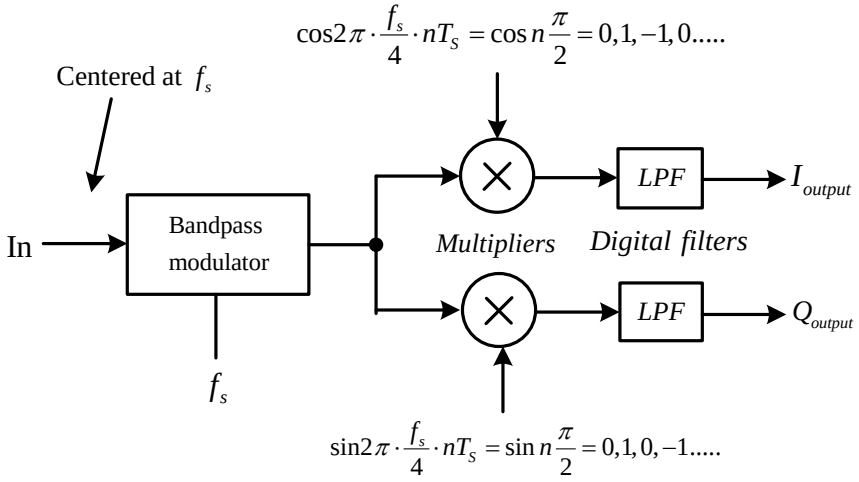


Figure 1 Block diagram for bandpass modulator with digital I/Q demodulation

For this solution we will be using 4th order bandpass modulator and additional circuit created with ideal component as supplied in addition with text material at CMOSedu.com. As discussed in the text the $f_s/4$ modulator is implemented using two $f_s/2$ in parallel or as *K*-path sampling system. This provides an easier way to implement two analog delays in feedback path in discrete time circuit.

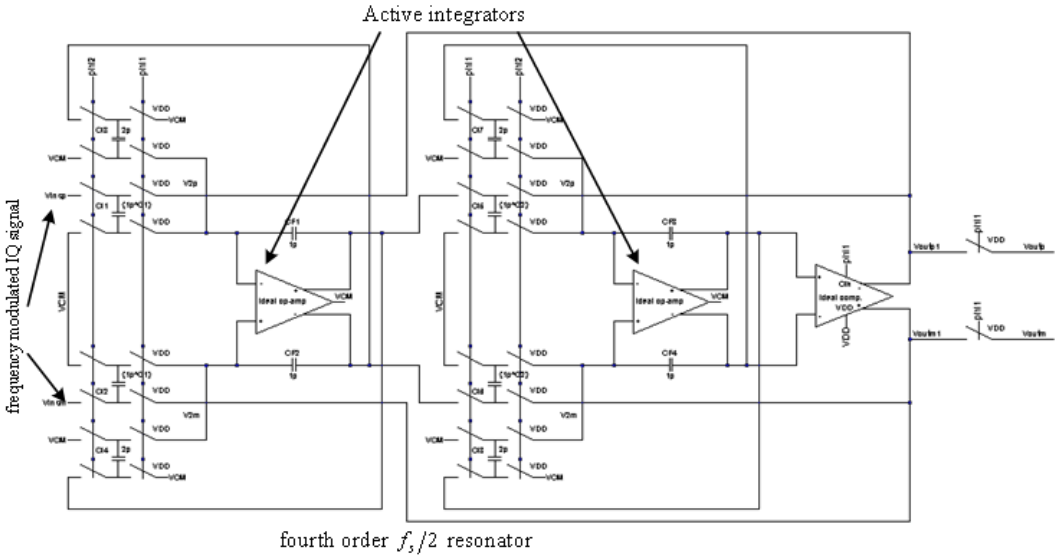


Figure 2 Fourth order $f_s/2$ resonator with QAM input signal

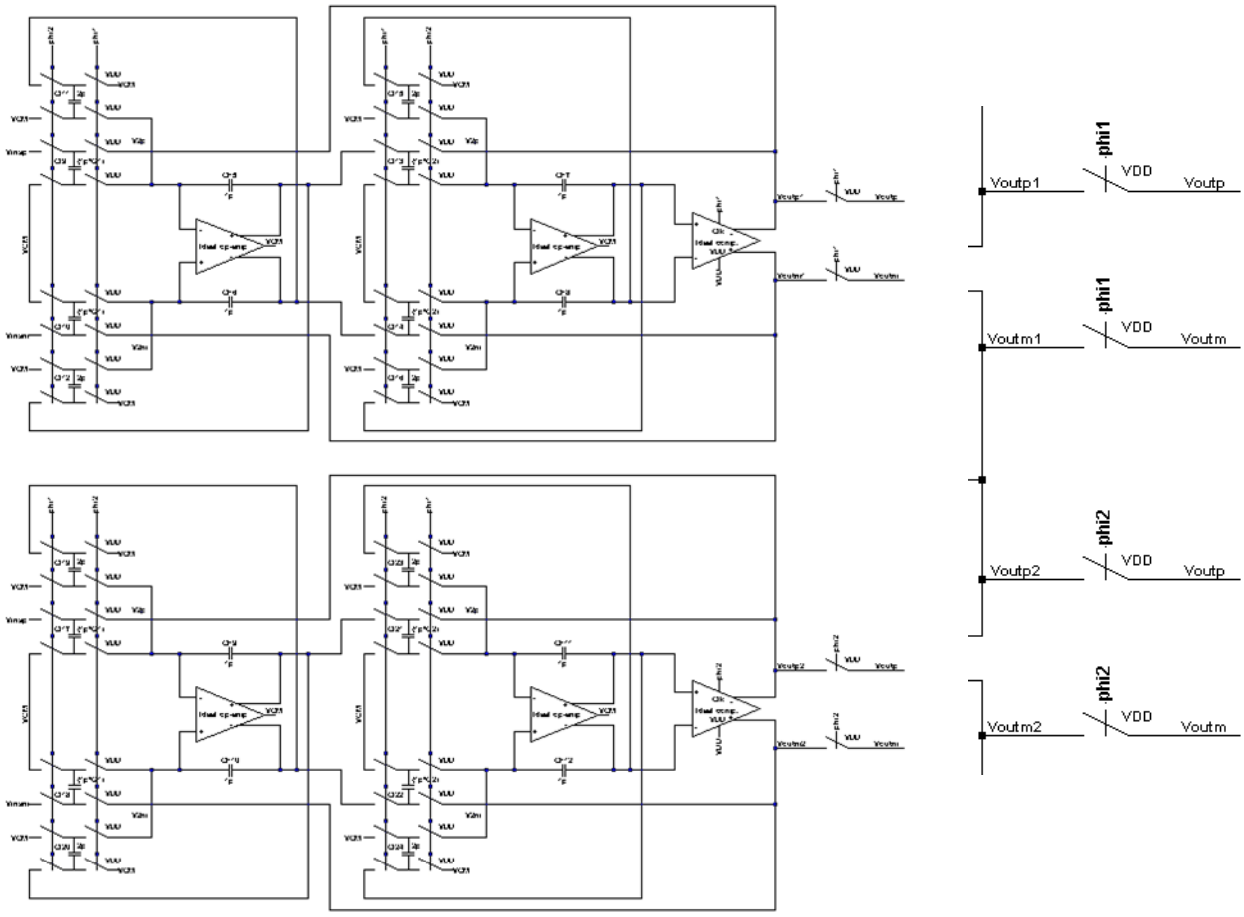


Figure 3 Two fourth order $f_s/2$ *modulator put in parallel and output clocked at different Clock phases with effective sampling at* f_s *and modulator behaving as* $f_s/4$

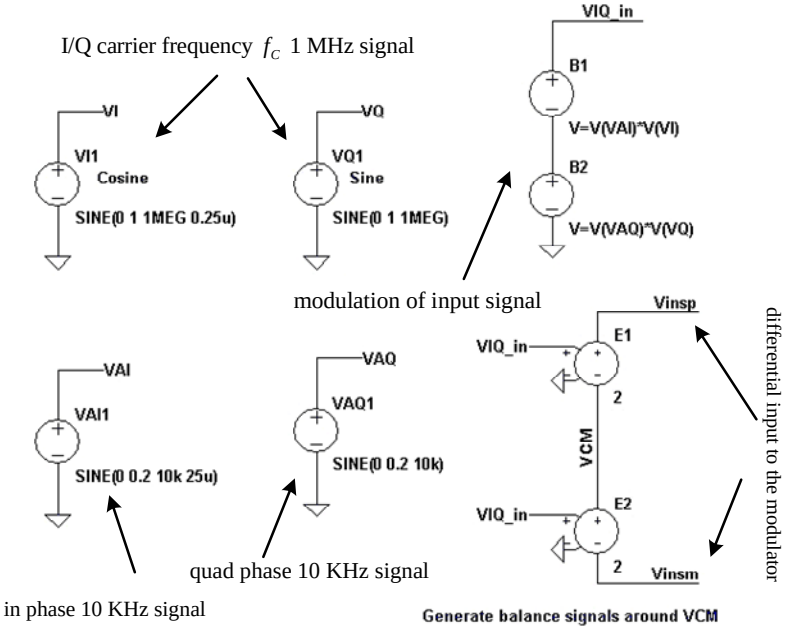


Figure 4 generating 1 KHz QAM signal at carrier freq. 1 MHz through ideal components and centering around V_{CM}

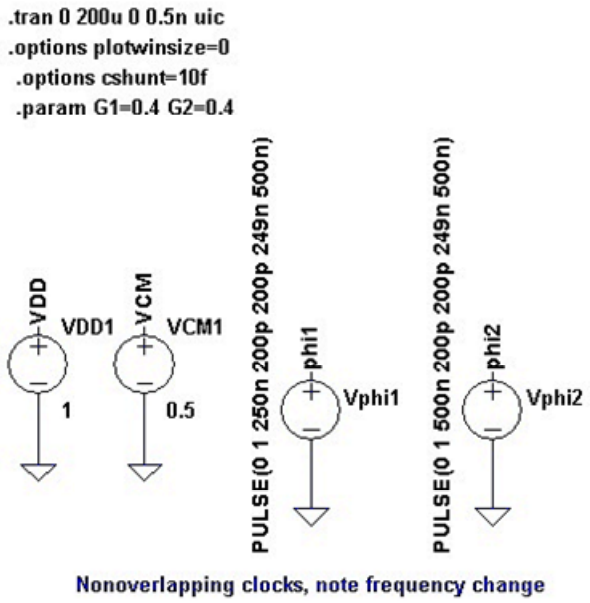


Figure 5 non overlapping clock frequencies of $f_s/2 = 2\ MHz$
Supply voltages and simulation time

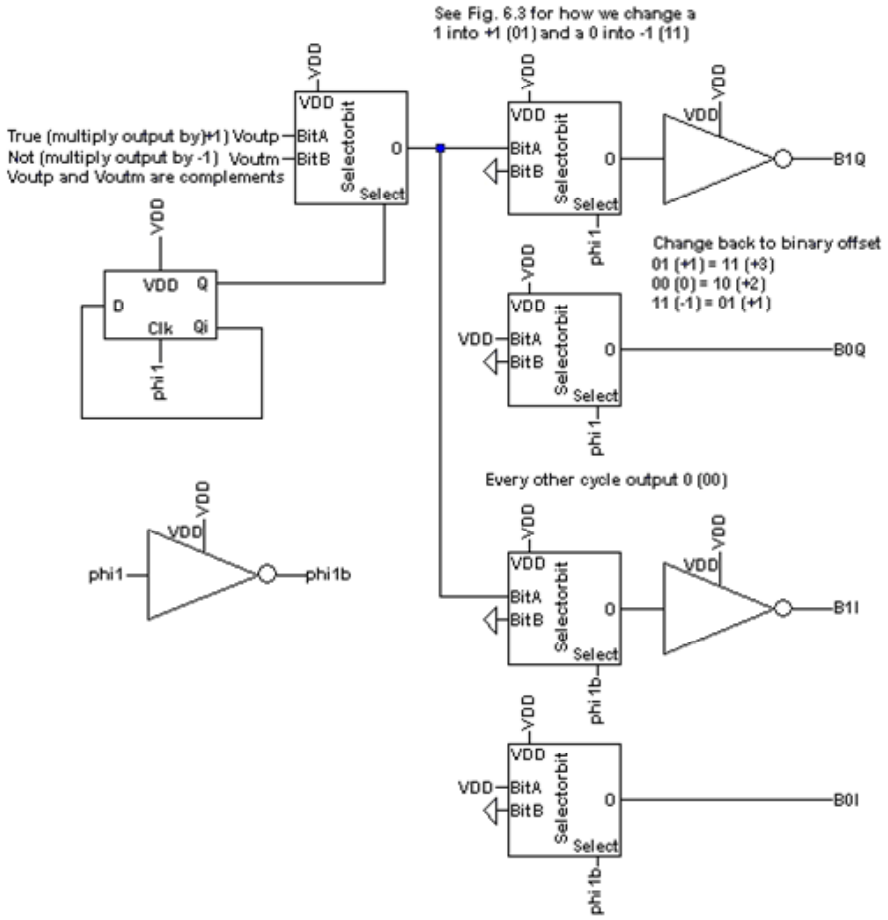


Figure 6 generating the and multiplying the modulator output with 1, 0,-1 for digital demodulation

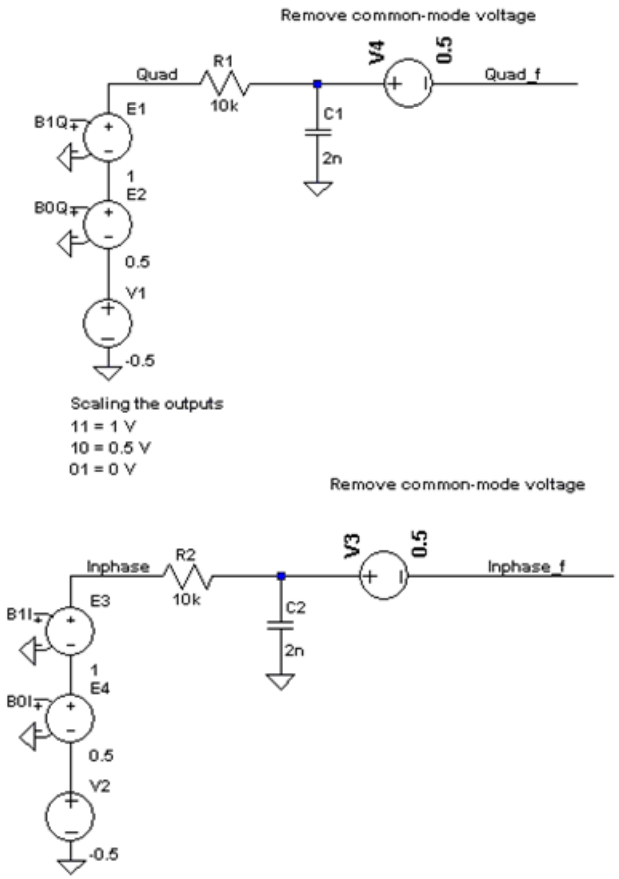


Figure 7 Digital I/Q demodulation, scaling the outputs and removing the common-mode voltage

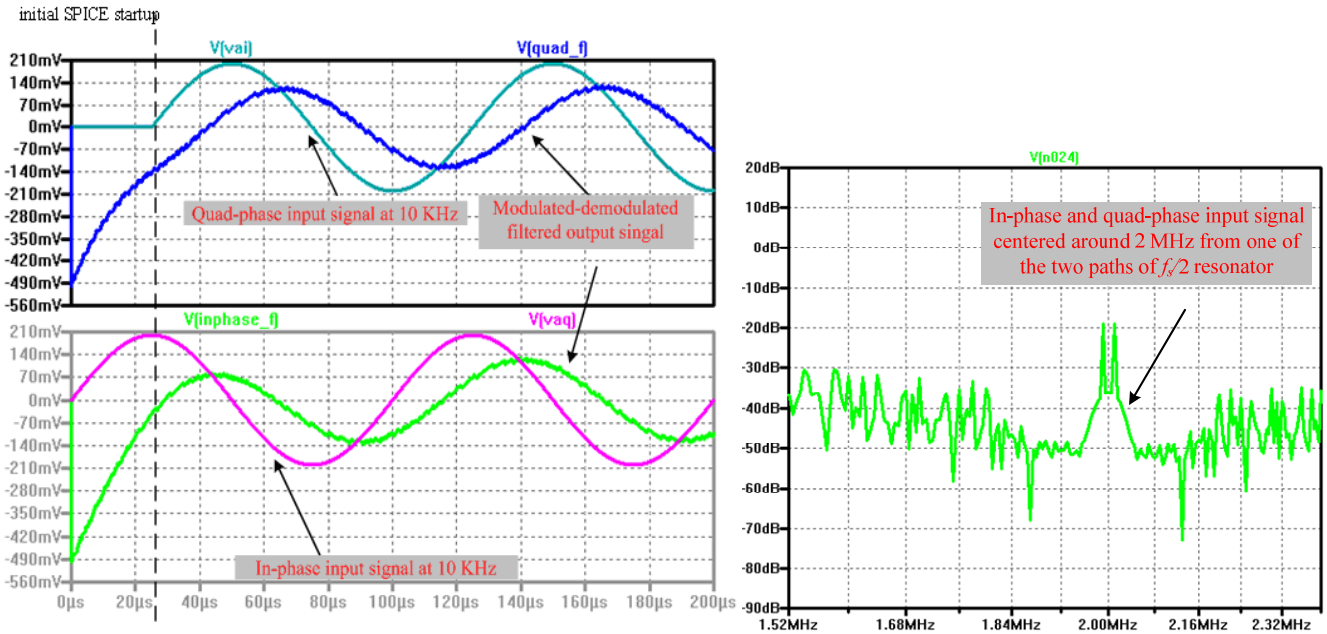


Figure 8 Simulation result for the working bandpass modulator; check CMOSedu.com LTspice examples for more

Note: In the solution a simple low pass filter is used it can be replaced with digital filter as seen in block diagram