Sakkarapani Balagopal

(P.29.1)A 3-bit, resistor-string DAC similar to the one shown in the fig. 29.2a was designed with a desired resistor of 500Ω. After fabrication, mismatch caused the actual value of the resistor to be R_1=500Ω, R_2=480Ω, R_3=470Ω, R_4=520Ω, R_5=510Ω, R_6=490Ω, R_7=530Ω, R_8=500Ω. Determine the maximum INL and DNL for the DAC assuming V_{ref}=5V.

The equivalent value of R is given by equation-29.1-1.

$$R_{Equivalent} = \sum_{i=1}^{8} R_i \tag{29.1-1}$$

$$R_{Equivalent} = 4000\Omega$$

The current flowing through the resistor string is given by equation-29.1-2.

$$I_{R\_String} = \frac{V_{ref}}{R_{Equivalent}} \tag{29.1-2}$$

$$\boxed{I_{R\_String} = \frac{5V}{4000\Omega} = 1.25mA}$$

Table 29.1-1 clearly shows the INL and DNL calculation for the given problem.

Table 29.1-1 – INL and DNL calculation of 3-bit DAC

Digital input	Node Voltages	V_{Act}(V)	V_{Ideal}(V)	Step height(V)		DNL(V)= S_{Act}-S_{Ideal}	INL(V)= V_{Act}-V_{Ideal}
				S_{Act}(V)	S_{Ideal}(V)		
0000_000	V_0	0	0	0	0	0	0
0000_001	V_1	0.625	0.625	0.625	0.625	0	0
0000_010	V_2	1.225	1.25	0.6	0.625	-0.025	-0.025
0000_100	V_3	1.8125	1.875	0.5875	0.625	-0.0375	-0.0625
0001_000	V_4	2.4625	2.5	0.65	0.625	0.025	-0.0375
0010_000	V_5	3.1	3.125	0.6375	0.625	0.0125	-0.025
0100_000	V_6	3.7125	3.75	0.6125	0.625	-0.0125	-0.0375
1000_000	V_7	4.375	4.375	0.6625	0.625	0.0375	0

From Table 29.1-1,

$$\boxed{|DNL_{MAX}| = 0.0375V = 0.06LSB}$$

$$\boxed{|INL_{MAX}| = 0.0625V = 0.1LSB}$$

29.2 An 8-bit resistor string DAC similar to the one shown in Fig. 29.2b was fabricated with a nominal resistance value of 1 kΩ. If the process was able to provide matching of resistors to within 1%, find the effective resolution of the converter. What is the maximum INL and DNL of the converter? Assume that $V_{REF} = 5V$.

$$1 \text{ LSB} = \frac{V_{REF}}{2^N} = \frac{5V}{2^8} \approx 19.53 \text{ mV}$$

From Eq (29.10),

$$|INL|_{max} = \frac{1}{2} LSB * 2^N * \left|\frac{\Delta R_k}{R}\right|_{\max}$$

$$|INL|_{max} = \frac{1}{2} LSB * 2^8 * 0.01$$

$$|INL|_{max} = 1.28\, LSB \approx 25 \text{ mV}$$

From Eq (29.13),

$$|DNL|_{max} = \frac{V_{REF}}{2^N} * \left|\frac{\Delta R_k}{R}\right|_{\max} = 1 \text{ LSB} * 0.01$$

$$|DNL|_{max} = 0.01 \text{ LSB} \approx 0.1953 \text{ mV}$$

The INL is the limiting factor for the resolution of a resistor-string DAC. To determine the effective resolution of the DAC in this problem, we again use Eq (29.10) and the fact that the INL must be < 0.5 *LSB*.

$$|INL|_{max} = \frac{1}{2} LSB * 2^N * \left|\frac{\Delta R_k}{R}\right|_{\max}$$

$$\frac{1}{2} LSB = \frac{1}{2} LSB * 2^N * \left|\frac{\Delta R_k}{R}\right|_{\max}$$

$$1 = 2^N * 0.01$$

$$2^N = 100$$

$$N = \frac{\log(100)}{\log(2)} \approx 6.64 \text{ bits}$$

So, a resistor-string DAC with 1% matching will have a resolution of 6 bits. Another way to determine this for the 8-bit DAC in this problem is to say the effective resolution is equal to the number of bits minus the ceiling of $|INL|_{max}$.

Effective resolution = 8 bits – 2 bits = 6 bits

29.3 *Compare the digital input codes necessary to generate all eight output values for a 3-bit resistor string DAC similar to those shown in Fig. 29.2a and b. Design a digital circuit that will allow a 3-bit binary digital input code to be used for the DAC in Fig. 29.2a. Discuss the advantages and disadvantages of both architectures.*

A 3-bit resistor string DAC requires 2^N resistors, Figure 29.2 shows a simple resistor-string DAC and a binary switch resistor-string DAC.

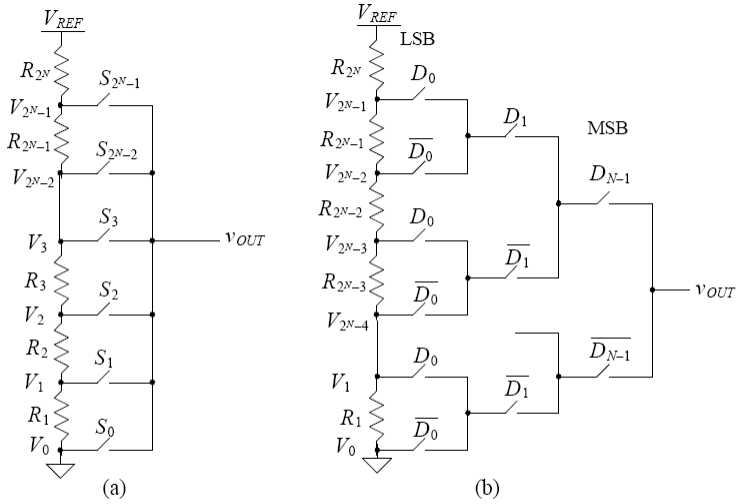


Figure 29.2 (a) A simple resistor string DAC and (b) use of a binary switch array to lower the output capacitance.

The DAC in Figure 29.2 (a) is termed a simple resistor string DAC because it is a relatively simple structure consisting of 2^N resistors and 2^N switches. If we want V_0 as the output we simply make S_0 high and ground all of the other voltages. If we want V_1 as the output we make S_1 high and ground all of the other voltages. The corresponding voltage on V_1 can be determined by realizing that it is simply a resistor divider:

$$V_1 = V_{REF} \cdot \frac{1 \cdot R}{(N-1) \cdot R + 1 \cdot R} = V_{REF} \cdot \frac{1}{8}$$

And similarly:

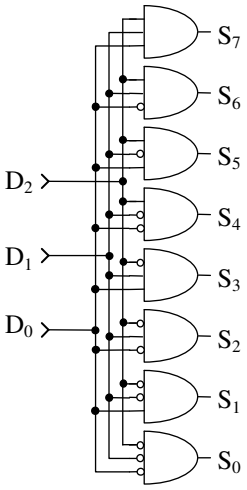
$$V_4 = V_{REF} \cdot \frac{4 \cdot R}{(N-4) \cdot R + 4 \cdot R} = V_{REF} \cdot \frac{4}{8}$$

Using this information we can create table 1 with the digital input codes necessary to generate all eight output values for the resistor string DACs seen in Figure 29.2.

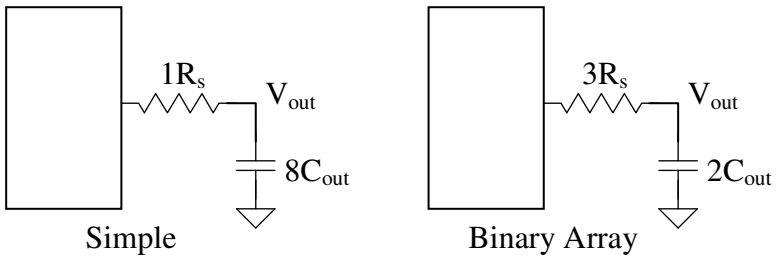
Table 1: Digital input code and corresponding output voltage for the DACs in Figure 29.2.

S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0		D_2	D_1	D_0	V_{OUT}
0	0	0	0	0	0	0	1		0	0	0	0.000
0	0	0	0	0	0	1	0		0	0	1	0.625
0	0	0	0	0	1	0	0		0	1	0	1.250
0	0	0	0	1	0	0	0		0	1	1	1.875
0	0	0	1	0	0	0	0		1	0	0	2.500
0	0	1	0	0	0	0	0		1	0	1	3.125
0	1	0	0	0	0	0	0		1	1	0	3.750
1	0	0	0	0	0	0	0		1	1	1	4.375

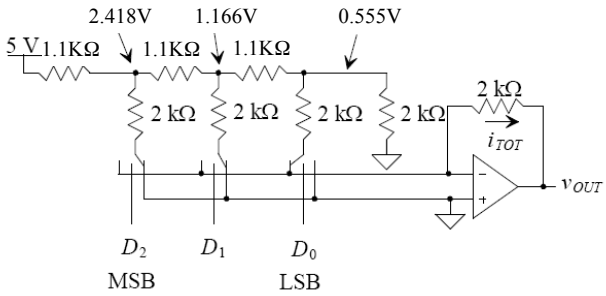
In order to create a circuit that generates the digital codes of table 1 using the digital input codes of table 2 we can use three input AND gates. Figure 1 shows the circuit used to create the input code for the DAC in Figure 29.2 (a).

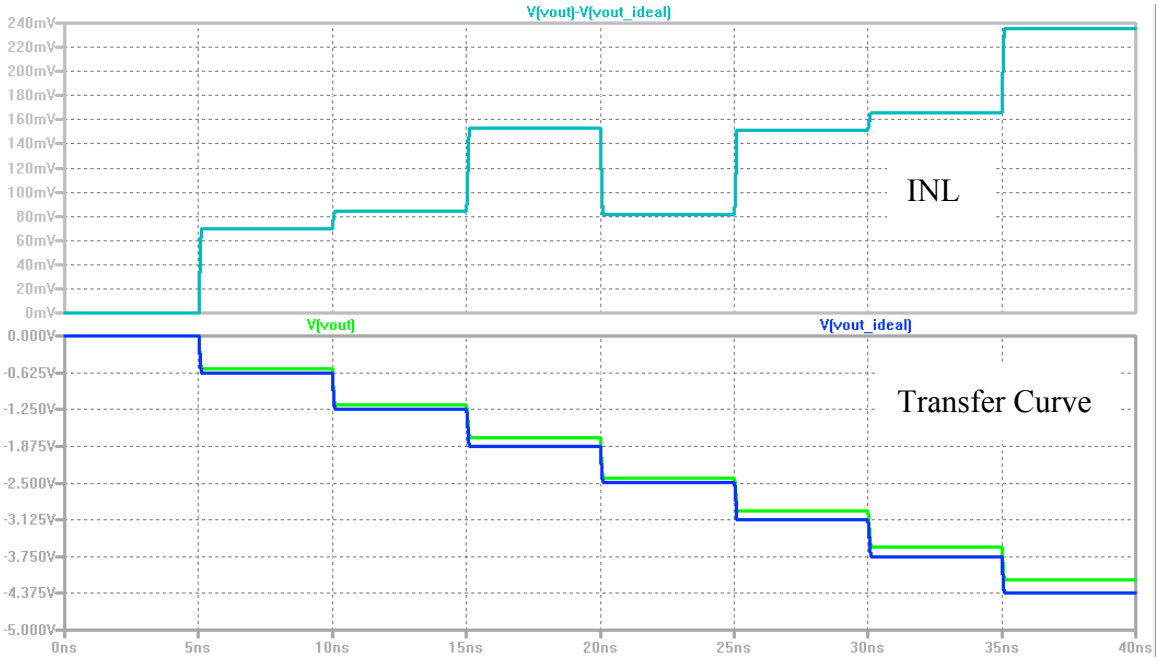


The advantages and disadvantages of the two resistor string DAC structures in figure 29.2, relative to each other, are based on the output capacitance and the switch resistance. While the simple resistor string DAC provides significantly large output capacitance due to the 2^N depletion capacitances it only has one switch resistance connected to the output. The binary switch array has much less capacitance attached to the output but also has the disadvantage of having more switch resistance connected to the output. In case of a 3-bit DAC, with both structures using the same switches we can estimate the load as:



29.4 Plot the transfer curve of a 3-bit R-2R DAC if all Rs = 1.1 kΩ and 2Rs = 2 kΩ. What is the maximum INL and DNL for the converter? Assume all of the switches to be ideal and V_{REF} = 5V.





DIN	Ideal Vout (V)	Vout (V)	DNL (LSB)	INL (LSB)
000	0	0		0
001	-0.625	-0.555	-0.112	0.112
010	-1.25	-1.165	-0.024	0.134
011	-1.875	-1.72	-0.112	0.245
100	-2.5	-2.416	0.114	0.131
101	-3.125	-2.971	-0.112	0.242
110	-3.75	-3.581	-0.024	0.266
111	-4.375	-4.136	-0.112	0.376

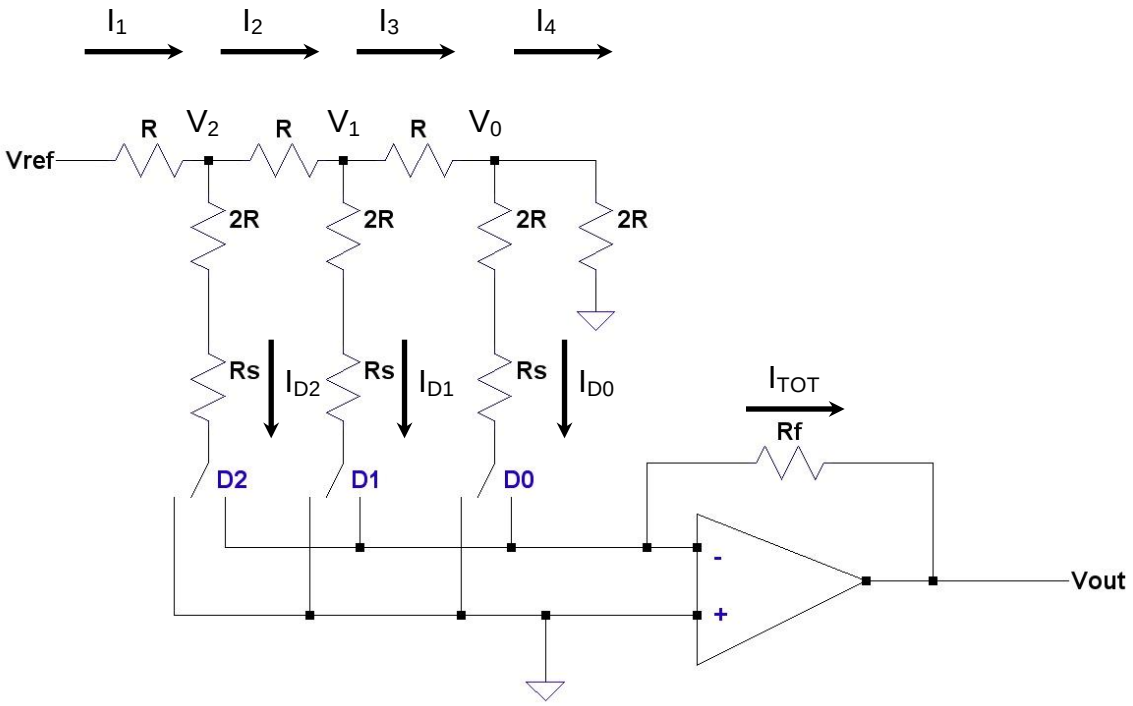
$DNL_{max} = DNL_{100} = 0.114$ LSB
$INL_{max} = INL_{111} = 0.376$ LSB

Justin Wood

29.5 Suppose that a 3-bit R-2R DAC contained resistors that were perfectly matched and that R=1kΩ and V_{REF}=5V. Determine the maximum switch resistance that can be tolerated for which the converter will still have 3-bit resolution. What are the values of INL and DNL?

For the converter to have 3-bit resolution, the INL and DNL must be within +/- 0.5 LSB. With a 3-bit DAC and V_{REF}=5, INL and DNL must be +/- 0.3125 V.

First, we need to derive the equations for the R-2R DAC. The general R-2R schematic is:



From the schematic above:

$$V_{OUT} = -I_{TOT} \cdot R_F$$

$$I_{TOT} = I_{D0} + I_{D1} + I_{D2}$$

$$I_{D0} = \frac{V_0}{2R + R_s}, I_{D1} = \frac{V_1}{2R + R_s}, I_{D2} = \frac{V_2}{2R + R_s}$$

$$I_1 = \frac{V_{REF} - V_2}{R}, I_2 = \frac{V_2 - V_1}{R}, I_3 = \frac{V_1 - V_0}{R}, I_4 = \frac{V_0}{2R}$$

Using KCL at each node (V_2, V_1, V_0) and substituting:

$$V_0 = \frac{V_{REF}}{\left(2+\frac{1}{2+\frac{R_s}{R}}\right)\cdot\left(\left(\left[2+\frac{1}{2+\frac{R_s}{R}}\right]\cdot\left[1.5+\frac{1}{2+\frac{R_s}{R}}\right]-1\right)-1.5+\frac{1}{2+\frac{R_s}{R}}\right.}$$

$$V_1 = \left(1.5+\frac{1}{2+\frac{R_s}{R}}\right)V_0$$

$$V_2 = \left(2+\frac{1}{2+\frac{R_s}{R}}\right)V_1 - V_0$$

DNL and INL in terms of our output current are as follows:

$$DNL(k) = \left(\left(-I_{TOT,Actual\ (k)} + I_{TOT,Actual\ (k-1)}\right) - \left(-I_{TOT,Ideal\ (k)} + I_{TOT,Ideal\ (k-1)}\right)\right)\cdot R_f\ (V)$$

$$INL(k) = \left(-I_{TOT,Actual\ (k)} + I_{TOT,Ideal\ (k)}\right)\cdot R_f\ (V)$$

Using the equations that we defined above, we can increase R_S and recalculate DNL or INL is greater than 0.3125V. R_s was found to be 307Ω using excel.

Below is a sample calculation of INL1 and DNL1 @ R_s=307Ω

$$INL1 = \left(-I_{TOT,Actual\ 001} + I_{TOT,Ideal\ 001}\right)\cdot R_f\ (V)$$

$$INL1 = \left[-\left(I_{D0,ACTUAL} + I_{D1,ACTUAL} + I_{D2,ACTUAL}\right) + \left(I_{D0,Ideal} + I_{D1,Ideal} + I_{D2,Ideal}\right)\right]\cdot R_f\ (V)$$

$$INL1 = \left[-\left(\frac{V_{o,actual}}{2R+R_s} + 0 + 0\right) + \left(\frac{V_{o,ideal}}{2R} + 0 + 0\right)\right]\cdot 2R = 0.01298\ (V)$$

$$INL1 = 0.01298\ (V)\cdot\frac{2^3(LSBs)}{5(V)} = 0.02077(LSBs)$$

$$DNL1 = \left(\left(-I_{TOT,Actual\ 1} + I_{TOT,Ideal\ 1}\right) - \left(-I_{TOT,Actual\ 0} + I_{TOT,Ideal\ 0}\right)\right)\cdot R_f\ (V)$$

$$DNL1 = \left[\left(-\left(\frac{V_{o,actual}}{2R+R_s} + 0 + 0\right) + \left(\frac{V_{o,ideal}}{2R} + 0 + 0\right)\right) - 0 + 0\right)\cdot 2R = 0.01298\ (V)$$

$$DNL1 = 0.01298\ (V)\cdot\frac{2^3(LSBs)}{5(V)} = 0.02077(LSBs)$$

The rest of the calculations are shown below:

VREF	5
R	1000
Rs	307
V0,actual	0.705961
V1,actual	1.364949
V2,actual	2.615593
V0,ideal	0.625
V1,ideal	1.25
V2,ideal	2.5

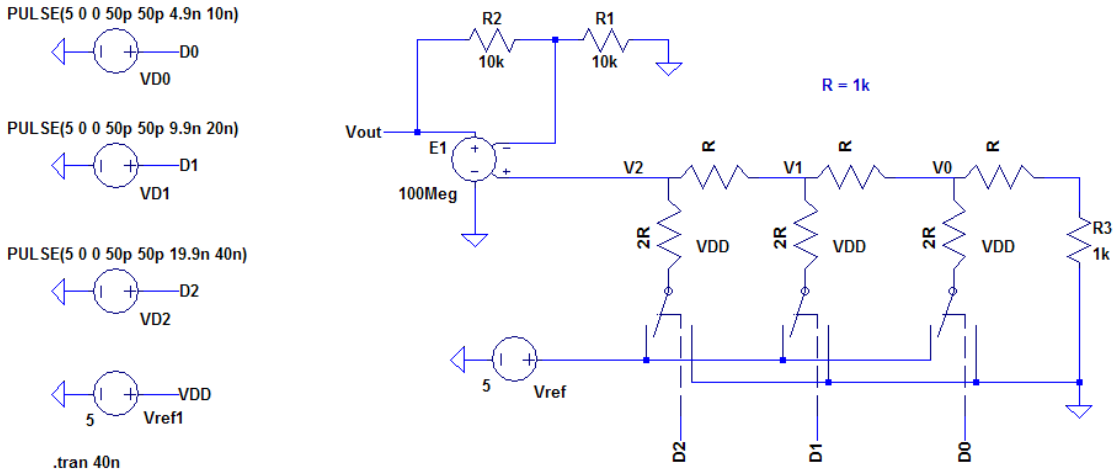
D2	D1	D0	I(TOT,ideal)	I(TOT,actual)
0	0	0	0	0
0	0	1	0.0003125	0.000306008
0	1	0	0.000625	0.000591655
0	1	1	0.0009375	0.000897663
1	0	0	0.00125	0.001133764
1	0	1	0.0015625	0.001439772
1	1	0	0.001875	0.001725419
1	1	1	0.0021875	0.002031427

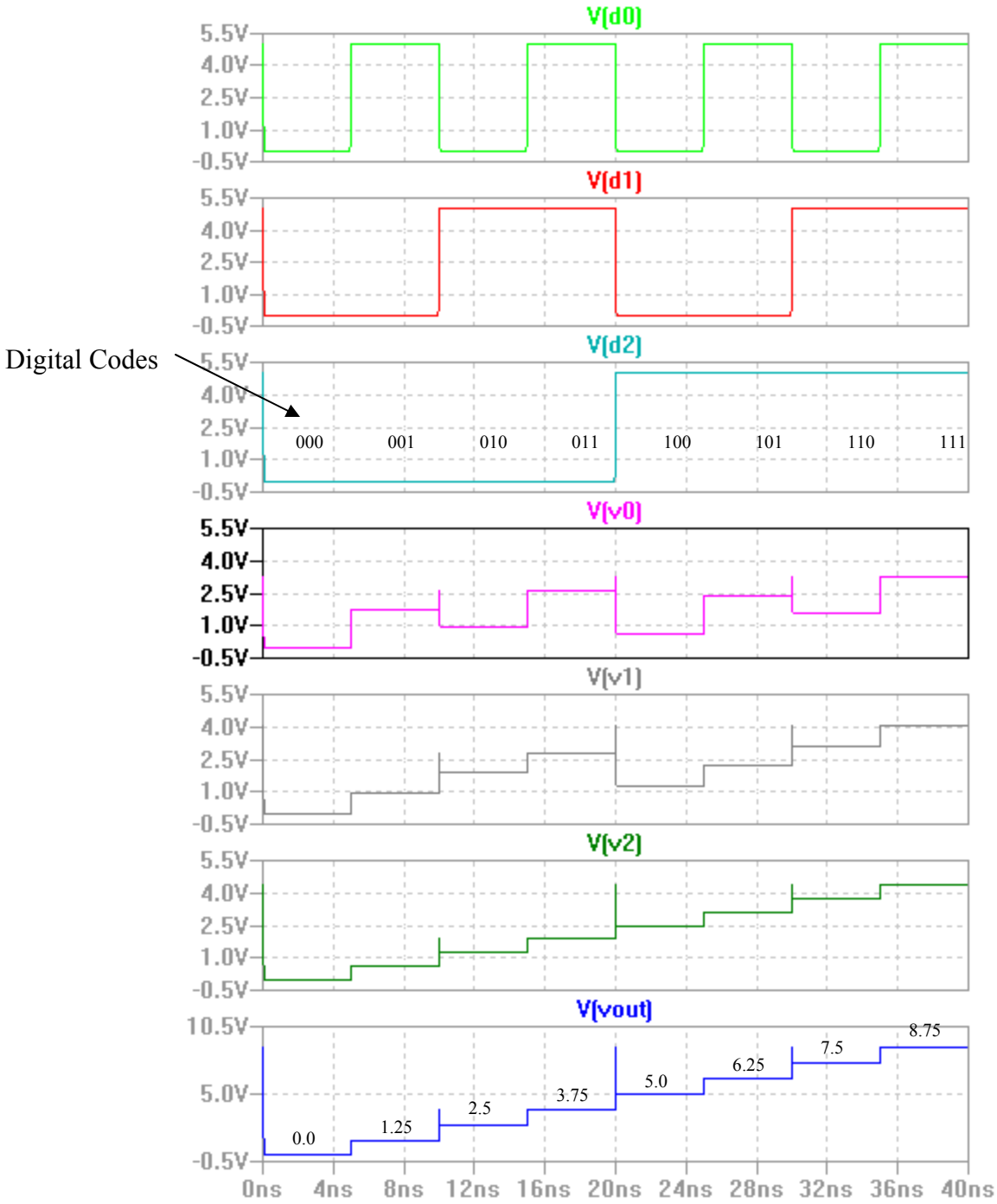
	(V)	(LSBs)
INL0	0	0
INL1	0.012984	0.020774
INL2	0.066689	0.106703
INL3	0.079673	0.127477
INL4	0.232473	0.371956
INL5	0.245457	0.392731
INL6	0.299162	0.478659
INL7	0.312146	0.499433
DNL1	0.012984	0.020774
DNL2	0.053705	0.085929
DNL3	0.012984	0.020774
DNL4	0.1528	0.244479
DNL5	0.012984	0.020774
DNL6	0.053705	0.085929
DNL7	0.012984	0.020774

Lincoln Bollschweiler

29.6 The circuit illustrated in Fig. 29.5 is known as a current-mode R-2R DAC, since the output voltage is defined by the current through R_F. Shown in Fig. 29.52 is an N-bit voltage-mode R-2R DAC. Design a 3-bit voltage mode DAC and determine the output voltage for each of the eight input codes. Label each node voltage for each input. Assume that $R = 1k\Omega$ and that $R_2 = R_1 = 10k\Omega$ and $V_{REF} = 5V$.

The following LTSpice circuit schematic shows the 3-bit DAC. The output voltages see a gain of 2 and therefore show a range which exceeds the rails of a 5V process amplifier. As an ideal amplifier is used, the output range, shown on the following page, ranges 0V to 8.8V. Output voltages are labeled on the simulation output for V_{OUT}.




V(d0)
5.5V
4.0V
2.5V
1.0V
-0.5V
V(d1)
5.5V
4.0V
2.5V
1.0V
-0.5V
Digital Codes
V(d2)
5.5V
4.0V
2.5V
1.0V
-0.5V
000
001
010
011
100
101
110
111
V(v0)
5.5V
4.0V
2.5V
1.0V
-0.5V
V(v1)
5.5V
4.0V
2.5V
1.0V
-0.5V
V(v2)
5.5V
4.0V
2.5V
1.0V
-0.5V
V(vout)
10.5V
5.0V
-0.5V
0.0
1.25
2.5
3.75
5.0
6.25
7.5
8.75
0ns
4ns
8ns
12ns
16ns
20ns
24ns
28ns
32ns
36ns
40ns

Sakkarapani Balagopal

(P29.7) Design a 3-bit, current-steering DAC using the generic current-steering DAC shown in figure 29.9. Assume that each current source, I, is 5μA, and find the total output current for each input code.

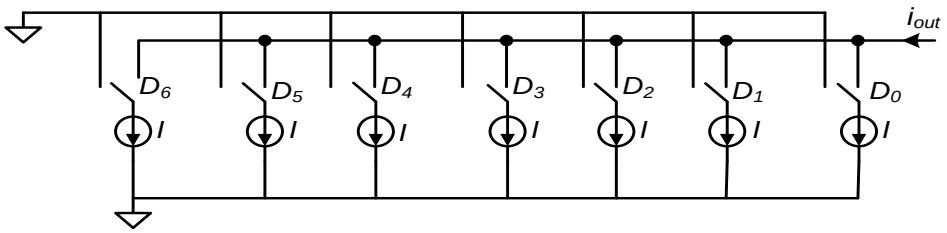


Figure 29.9-1 - A generic current-steering DAC.

The simple 3-bit current steering DAC is shown in the figure 29.9-1. For a 3-bit DAC, seven equal value current sources of value I=5μA will be needed. Depend on the binary control signals from D_0 to D_6, the current sources are either connected to i_{out} or ground. The resulting currents are shown in the table 29.7-1.

Table 29.7-1 - Output current generated from 3-bit DAC

Digital Input Code	D_0	D_1	D_2	D_3	D_4	D_5	D_6	i_{out}
000	0	0	0	0	0	0	0	0
001	1	0	0	0	0	0	0	5μA
010	1	1	0	0	0	0	0	10μA
011	1	1	1	0	0	0	0	15μA
100	1	1	1	1	0	0	0	20μA
101	1	1	1	1	1	0	0	25μA
110	1	1	1	1	1	1	0	30μA
111	1	1	1	1	1	1	1	35μA

29.8 A certain process is able to fabricate matched current sources to within 0.05%. Determine the maximum resolution that a current-steering (non-binary-weighted) DAC can attain using this process.

From Eq (29.21),

$$\left|\Delta I\right|_{\max,INL} = \frac{I}{2^N}$$

From Eq (29.26),

$$\left|\Delta I\right|_{\max,DNL} = \frac{I}{2}$$

The terms $\left|\Delta I\right|_{\max,INL}$ and $\left|\Delta I\right|_{\max,DNL}$ represent the maximum current source mismatch error that will keep the INL and DNL, respectively, less than 0.5 LSB. Clearly the INL is the limiting factor in a non-binary-weighted current-steering DAC.

If the current sources are matched within 0.05%, then $\left|\Delta I\right|_{\max} = 0.05\% * I$.

$$\left|\Delta I\right|_{\max,INL} = \frac{I}{2^N}$$

$$0.05\% * I = \frac{I}{2^N}$$

$$2^N = \frac{1}{0.0005}$$

$$N = \frac{\log(\frac{1}{0.0005})}{\log(2)} \approx 10.97$$

The maximum resolution is then 10 bits.

29.9 *Design an 8-bit current-steering DAC using binary-weighted current sources. Assume that the smallest current source will have a value of 1 μA. What is the range of values that the current source corresponding to the MSB can have while maintaining an INL of ½ LSB? Repeat for a DNL less than or equal to ½ LSB.*

Figure 29.10 gives a generic view of a binary-weighted current-steering DAC.

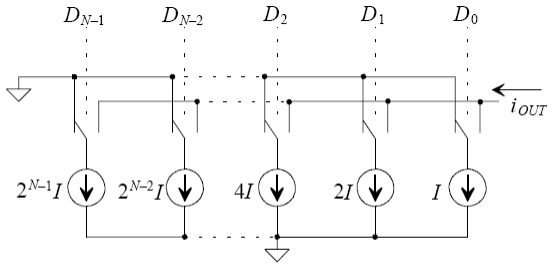


Figure 29.10 A current steering DAC using binary-weighted current sources.

An 8-bit current-steering DAC using binary-weighted current sources will have N current sources. Figure 1 shows the binary-weighted current sources used in an 8-bit DAC.

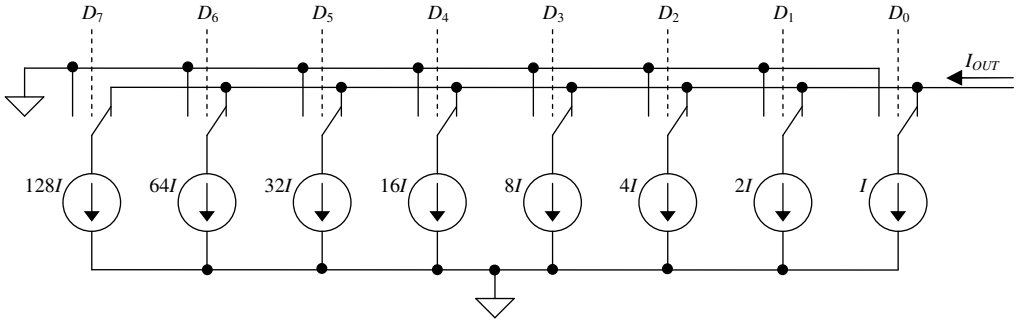


Figure 1 Block diagram of an 8-bit binary-weighted current-steering DAC.

Analyzing the integral nonlinearity of the binary weighted current steering DAC is accomplished by realizing that the sum of current error sums to zero and that one half of the current sources contain the maximum INL error. In this case, the MSB current will contain the maximum error.

$$I_{MSB,actual} = 2^{N-1}\left(I + \Delta I\right)$$

Subtracting the ideal current from the actual current gives the value of the maximum INL:

$$INL_{MAX} = I_{MSB,actual} - I_{MSB,ideal} = 2^{N-1}\left(I + \Delta I\right) - 2^{N-1}\left(I\right) = 2^{N-1}\Delta I$$

Realize that the LSB of the current steering DAC is simply *I*, and we can equate the maximum INL to ½ LSB:

$$INL_{MAX} = \tfrac{1}{2}\,LSB$$

$$2^{N-1}\Delta I = \tfrac{1}{2} I$$

$$\Delta I = \frac{I}{2^N} = \frac{1\mu A}{2^8} \approx 4nA$$

In order to design a binary weighted current source with an INL less than ½ LSB, the range of the MSB must be:

$$I_{MSB,ideal} - \Delta I \le I_{MSB,actual} \le I_{MSB,ideal} - \Delta I$$

$$127.996\mu A \le I_{MSB,actual} \le 128.004\mu A$$

For the determination of the DNL we have to realize that the worst case occurs at the transition from 01111111 to 10000000. We also assume that the errors all sum to zero. As an example, consider a 3-bit binary weighted DAC with the lower two current sources containing negative error and the MSB containing positive error. To determine the maximum DNL we simply subtract the currents to determine the "step height":

$$DNL_{MAX} = 2^2\left(I + \Delta I\right) - 2^1\left(I - \Delta I\right) - 2^0\left(I - \Delta I\right) - I$$

$$DNL_{MAX} = 4I + 4\Delta I - 3I + 3\Delta I - I = 7\Delta I$$

Restating equation 29.28, shows that this approach is correct:

$$DNL_{MAX} = \left[2^{N-1}\cdot\left(I + \Delta I\right) - \sum_{k=1}^{N-1} 2^{k-1}\cdot\left(I - \Delta I\right)\right] - I$$

Which results in $DNL_{MAX} = \left(2^N - 1\right)\cdot\Delta I$, if we wish to keep the DNL equal to less than ½ LSB we simply equate the two and solve for the maximum error, remembering that an LSB is equal to *I*:

$$\left(2^N - 1\right)\cdot\Delta I = \tfrac{1}{2} I$$

$$\Delta I = \frac{I}{2\left(2^N - 1\right)} = \frac{1\mu A}{2\cdot 255} \approx 2nA$$

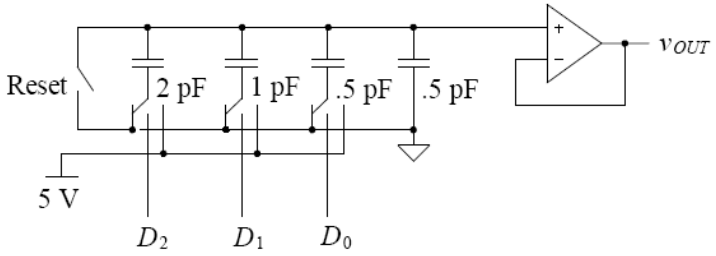
For the DNL to be less than or equal to ½ LSB the MSB current source must have the range of:

$$127.998\mu A \le I_{MSB,actual} \le 128.002\mu A$$

Comparing the two results we can see that the DNL requirement is more stringent.

Adam Johnson

29.10 Prove that the 3-bit charge-scaling DAC used in Ex. 29.6 has the same output voltage increments as the R-2R DAC in Ex. 3 for V_{REF} = 5 V and C = 0.5 pF.



From Eq. (29.33), $V_{OUT} = (D_0*2^{-3} + D_1*2^{-2} + D_2*2^{-1})*V_{REF}$

For DIN = 000, $V_{OUT} = (0*2^{-3} + 0*2^{-2} + 0*2^{-1})*5V = 0V$

For DIN = 001, $V_{OUT} = (1*2^{-3} + 0*2^{-2} + 0*2^{-1})*5V = 0.625V$

For DIN = 010, $V_{OUT} = (0*2^{-3} + 1*2^{-2} + 0*2^{-1})*5V = 1.25V$

For DIN = 011, $V_{OUT} = (1*2^{-3} + 1*2^{-2} + 0*2^{-1})*5V = 1.875V$

For DIN = 100, $V_{OUT} = (0*2^{-3} + 0*2^{-2} + 1*2^{-1})*5V = 2.5V$

For DIN = 101, $V_{OUT} = (1*2^{-3} + 0*2^{-2} + 1*2^{-1})*5V = 3.125V$

For DIN = 110, $V_{OUT} = (0*2^{-3} + 1*2^{-2} + 1*2^{-1})*5V = 3.75V$

For DIN = 111, $V_{OUT} = (1*2^{-3} + 1*2^{-2} + 1*2^{-1})*5V = 4.375V$

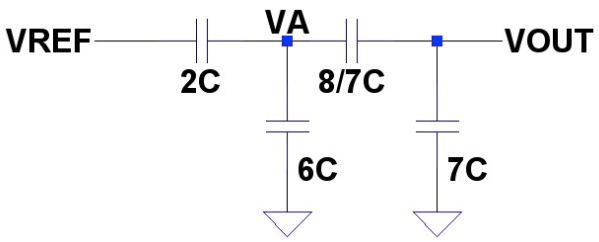
DIN	Ex. (29.3)	Ex. (29.6)
000	0	0
001	-0.625	0.625
010	-1.25	1.25
011	-1.875	1.875
100	-2.5	2.5
101	-3.125	3.125
110	-3.75	3.75
111	-4.375	4.375

The voltage increments (V_{LSB}) of both DACs are the same in magnitude at 0.625V, but opposite in sign.

Justin Wood

29.11 Determine the output of the 6-bit, charge-scaling DAC used in Ex. 29.7 for each of the following inputs: D = 000010, 000100, 001000, and 010000.

With D=000010, the equivalent circuit would be:



We first calculate V_A as follows:

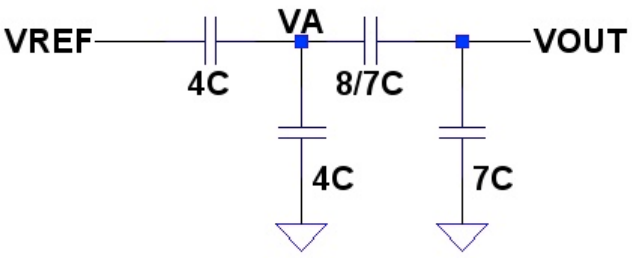
$$V_A = \frac{2C}{6C + \left(\frac{8}{7}C \text{ series } 7C\right) + 2C} V_{REF} = \frac{2}{6 + \left(\frac{\frac{8}{7}\cdot 7}{\frac{8}{7}+7}\right) + 2} V_{REF} = \frac{2}{8 + \frac{56}{57}} V_{REF}$$

V_{OUT} is then calculated as follows:

$$V_{OUT} = \left(\frac{\frac{8}{7}}{\frac{8}{7}+7}\right) V_A$$

$$V_{OUT} = \left(\frac{\frac{8}{7}}{\frac{8}{7}+7}\right)\left(\frac{2}{8+\frac{56}{57}}\right) V_{REF} = \frac{1}{32} V_{REF}$$

With D=000100, the equivalent circuit would be:



We first calculate V_A just like the previous code:

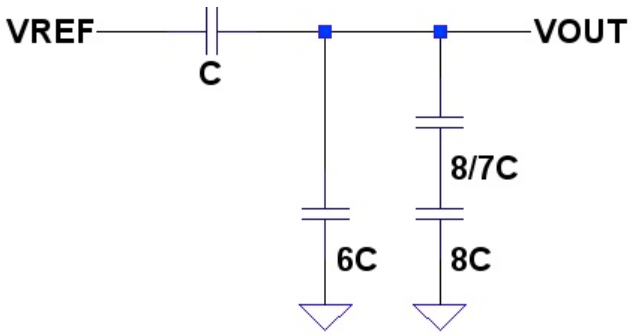
$$V_A = \frac{4C}{4C + \left(\frac{8}{7}C \text{ series } 7C\right) + 4C} V_{REF} = \frac{4}{\left(\frac{\frac{8}{7}\cdot 7}{\frac{8}{7}+7}\right) + 8} V_{REF} = \frac{4}{8 + \frac{56}{57}} V_{REF}$$

V_{OUT} is then calculated as follows:

$$V_{OUT} = \left(\frac{\frac{8}{7}}{\frac{8}{7}+7}\right) V_A$$

$$V_{OUT} = \left(\frac{\frac{8}{7}}{\frac{8}{7}+7}\right)\left(\frac{4}{8+\frac{56}{57}}\right) V_{REF} = \frac{1}{16} V_{REF}$$

With D=001000, the equivalent circuit would be:

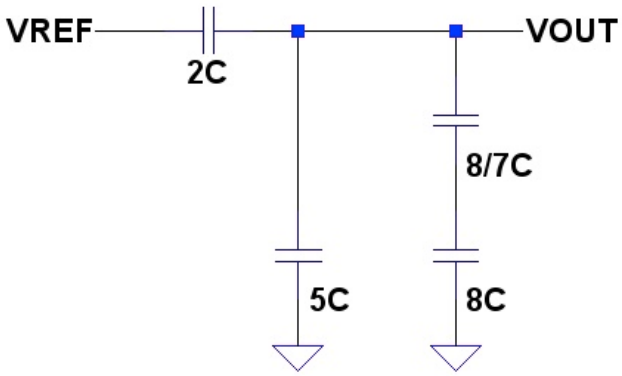


V_{OUT} is calculated as follows:

$$V_{OUT} = \left(\frac{1C}{6C + \left(\frac{8}{7}C \ series \ 8C \right) + 1C} \right) V_{REF}$$

$$V_{OUT} = \frac{1}{\left(\frac{\frac{8}{7} \cdot 8}{\frac{8}{7} + 8} \right) + 7} V_{REF} = \frac{1}{8} V_{REF}$$

With D=010000, the equivalent circuit would be:



V_{OUT} is calculated as follows:

$$V_{OUT} = \left(\frac{2C}{5C + \left(\frac{8}{7}C \ series \ 8C \right) + 2C} \right) V_{REF}$$

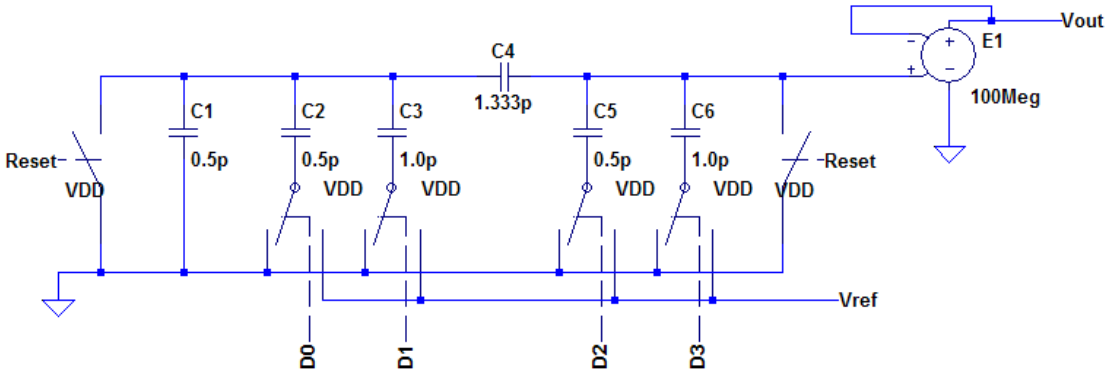
$$V_{OUT} = \frac{2}{\left(\frac{\frac{8}{7} \cdot 8}{\frac{8}{7} + 8} \right) + 7} V_{REF} = \frac{1}{4} V_{REF}$$

Lincoln Bollschweiler

29.12 Design a 4-bit, charge-scaling DAC using a split array. Assume that V_{REF} = 5V and that C = 0.5pF. Draw the equivalent circuit for each of the following input words and determine the value of the output voltage: D = 0001, 0010, 0100, 1000. Assume the capacitor associated with the MSB had a mismatch of 4 percent, calculate the INL and DNL.

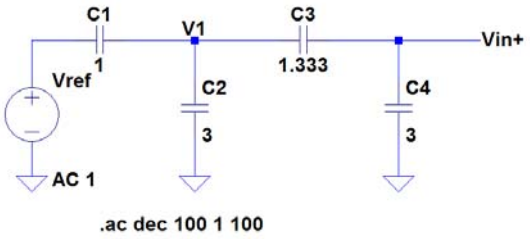
We find the value of the attenuation capacitor, using (29.35) to be (4/3)C = 1.333pF.

The complete circuit is shown as follows:

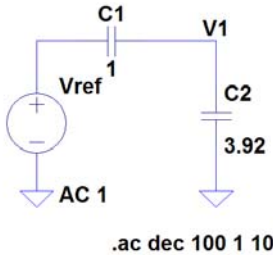


In all simplifications shown, the capacitor values will be normalized to C=1

a. The equivalent circuit for input code 0001 is as follows:

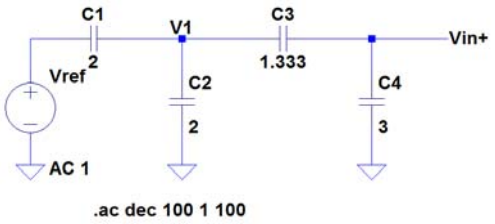


C3 in series with C4 reduces to 12/13. That in parallel with C2 is 3+12/13. That circuit is as follows:



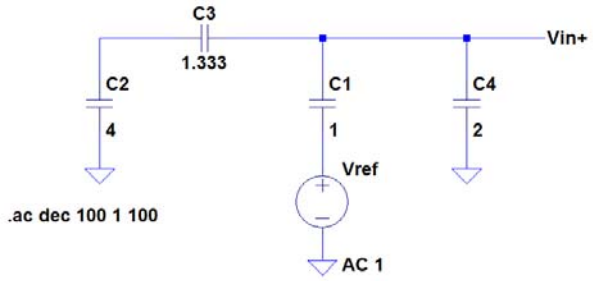
We can easily solve for V1 now by capacitive divider. V1 = 0.203Vref. We can use V1 in a capacitive divider with C3 and C4 to get Vin+. **Vin+ = 0.0625Vref = Vref/16. Vout = Vin+** due to voltage follower.

b. The equivalent circuit for input code 0010 is as follows:

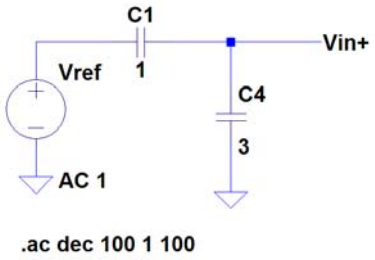


By similar analysis technique we can find that V1 = 0.406Vref. **Vout = 0.125Vref = Vref/8.**

c. The equivalent circuit for input code 0100 is as follows:

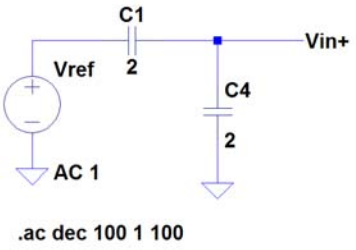


which further reduces to:



It can be readily seen by capacitive voltage divider that **Vout = Vin+ = Vref/4.**

d. The equivalent circuit for input code 1000 is as follows:



It can be readily seen that **Vout = Vin+ = Vref/2.**

To find INL we can start by realizing that 4% matching on the MSB capacitor is the same as having the MSB cap being off by +2% while all the others are off by -2%. Overall we have 2% mismatch. We can use the R2-R DAC equations from chapter 30 to find INL and DNL.

Using (30.13) and % mismatch = 2 we find: $DNL = 5\left|0.02 - \frac{1}{2^4}\right| = 0.213V = 0.68LSB.$

Using (30.16) we find:. $INL = \frac{5}{2} \cdot \frac{2}{100+2} = 0.049V = 0.157LSB.$

(P.29.13)For the cyclic converter shown in the figure 29.17, determine the gain error for a 3-bit conversion if the feedback amplifier had a gain of 0.45V/V. Assume that V_{ref}=5V.

The output voltage at the end of nth cycle of the conversion with feedback amplifier gain of 0.5V/V is given in equation 29.13-1.

$$V_{Out}(n) = \left(D_{n-1}.V_{ref} + \frac{1}{2}V_A(n-1) \right)\frac{1}{2} \tag{29.13-1}$$

Table 29.13-1 summarizes the resultant output voltage for different inputs. Results are plotted in the figure 29.13-1.

Table-29.13-1 - Output voltage of 3-bit DAC with different feedback amplifier gain

Input	D_0	D_1	D_2	$V_{out,actual}$(V) for a gain of 0.5V/V	$V_{out,actual}$(V) for a gain of 0.45V/V
0	0	0	0	0	0
1	0	0	1	0.625	0.4556525
2	0	1	0	1.25	1.0125
3	0	1	1	1.875	1.468125
4	1	0	0	2.5	2.25
5	1	0	1	3.125	2.705625
6	1	1	0	3.75	3.2625
7	1	1	1	4.375	3.718125

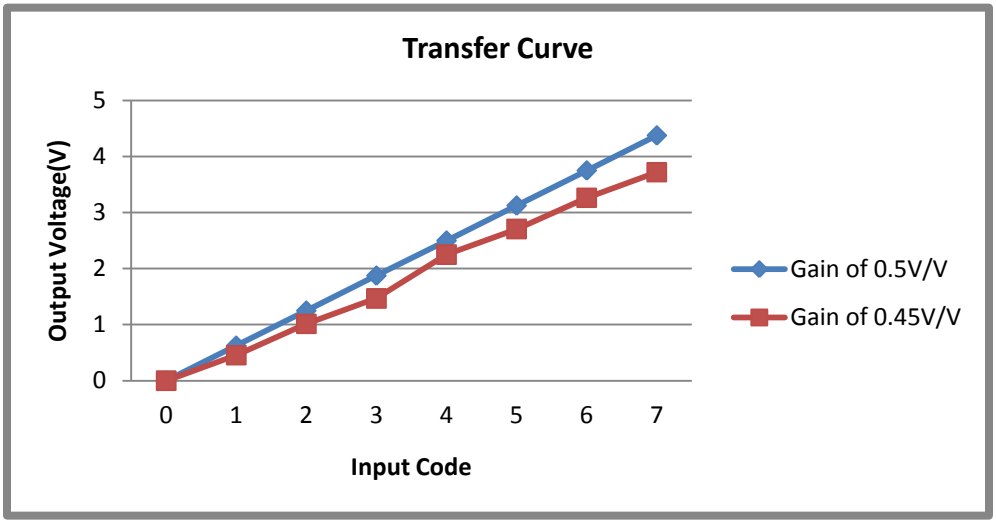


Figure 29.13-1 Transfer curve for 3-bit DAC for different feedback amplifier gain

From page no.945 of the textbook, the gain error can be written as

$$Gain\_Error = Ideal\_Slope_{Blue} - Actual\_Slope_{Red}$$

$$Gain\_Error = \left(\frac{y_2 - y_1}{x_2 - x_1}\right)_{Blue} - \left(\frac{y_2 - y_1}{x_2 - x_1}\right)_{Red}$$

$$Gain\_Error = \left(\frac{\frac{7}{8}V_{REF} - 0}{111 - 000}\right)_{Blue} - \left(\frac{3.718125 - 0}{111 - 000}\right)_{Red}$$

The x and y axis in figure 29.15-1 are in different units. So, convert the denominator on above equation into same unit or volts.

$$Gain\_Error = \left(\frac{\frac{7}{8}V_{REF} - 0}{\frac{7}{8}V_{REF} - 0}\right)_{Blue} - \left(\frac{3.718125 - 0}{\frac{7}{8}V_{REF} - 0}\right)_{Red}$$

$$Gain\_Error = 1 - \left(\frac{3.718125}{\frac{7}{8}.5}\right)_{Red} = 1 - 0.85$$

$$\boxed{Gain\_Error = 0.15\frac{V}{V}}$$

29.14 Repeat Problem 29.13 assuming that the output of the summer was always 0.2V greater than the ideal and that the amplifier in the feedback path had a perfect gain of 0.5 V/V.

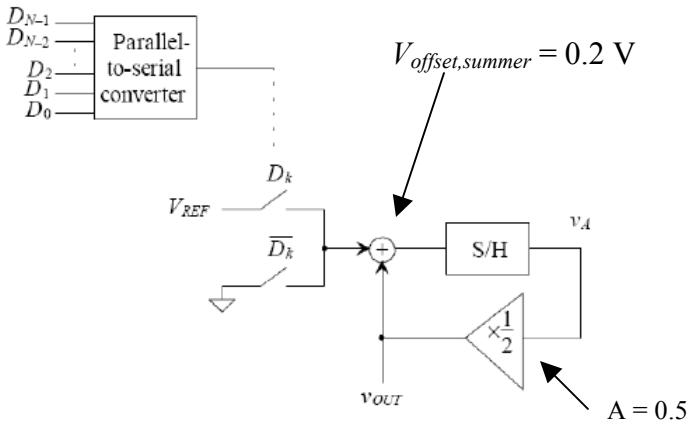


Figure 29.17 A cyclic digital-to-analog converter.

The output voltage at the end of the n[th] cycle can be expressed as:

$$V_{out}(n) = \left(D_{n-1} \cdot V_{REF} + A \cdot V_A(n-1) + V_{offset,summer}\right) \cdot A$$

And $V_A(n)$ can be expressed as:

$$V_A(n) = D_{n-1} \cdot V_{REF} + A \cdot V_A(n-1) + V_{offset,summer}$$

We can then write $V_{out}(n)$ as:

$$V_{out}(n) = \left(D_{n-1} \cdot V_{REF} + A \cdot \left(D_{n-2} \cdot V_{REF} + A \cdot V_A(n-2) + V_{offset,summer}\right) + V_{offset,summer}\right) \cdot A$$

$$V_{out}(n) = A \cdot D_{n-1} \cdot V_{REF} + A^2 \cdot D_{n-2} \cdot V_{REF} + A^3 \cdot V_A(n-2) + A^2 \cdot V_{offset,summer} + A \cdot V_{offset,summer}$$

$$V_{out}(n) = \underbrace{V_{REF} \cdot \sum_{k=0}^{n-1} A^{n-k} \cdot D_k}_{Vout,ideal(n)} + V_{offset,summer} \cdot \sum_{k=0}^{n-1} A^{n-k}$$

For an N-bit DAC, we sample the output voltage on the N[th] cycle. We are using a 3-bit DAC in this problem, so the output voltage is:

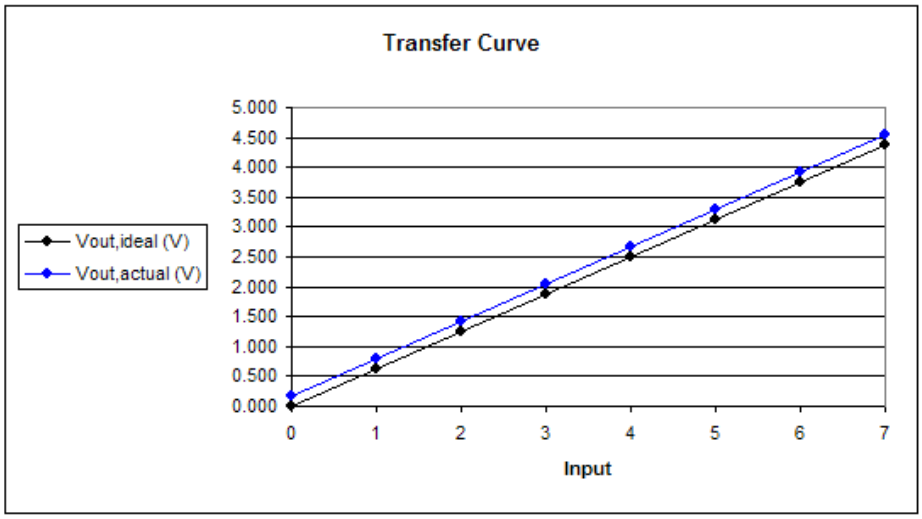
$$V_{out} = V_{out}(n=3) = V_{REF} \cdot \left(A^3 \cdot D_0 + A^2 \cdot D_1 + A \cdot D_2\right) + V_{offset,summer} \cdot \left(A^3 + A^2 + A\right)$$

$$V_{out} = 5V \cdot \left(0.5^3 \cdot D_0 + 0.5^2 \cdot D_1 + 0.5 \cdot D_2\right) + 0.2V \cdot \left(0.5^3 + 0.5^2 + 0.5\right)$$

$$V_{out} = \underbrace{5V \cdot \left(0.5^3 \cdot D_0 + 0.5^2 \cdot D_1 + 0.5 \cdot D_2\right)}_{Vout,ideal} + 0.175V$$

The output values and transfer curve are shown below.

Input	D2	D1	D0	Vout,ideal (V)	Vout,actual (V)
0	0	0	0	0.000	0.175
1	0	0	1	0.625	0.800
2	0	1	0	1.250	1.425
3	0	1	1	1.875	2.050
4	1	0	0	2.500	2.675
5	1	0	1	3.125	3.300
6	1	1	0	3.750	3.925
7	1	1	1	4.375	4.550



Gain error = slope of $V_{out,ideal}$ *– slope of* $V_{out,actual}$

It is clear from the plot that the slopes of both lines are equal. There is only an offset error equal of 175 mV. After removing the offset error, we would report:

Offset error = 175 mV
Gain error = 0
$|INL|_{max} = 0$
$|DNL|_{max} = 0$

29.15 *Repeat Problem 29.13 assuming that the output of the summer was always 0.2 V greater than the ideal and that the amplifier in the feedback path had a gain of 0.45 V/V.*

29.13 *For the cyclic converter shown in Fig. 29.17, determine the gain error for a 3-bit conversion if the feedback amplifier had a gain of 0.45 V/V. Assume that V_{REF} = 5 V.*

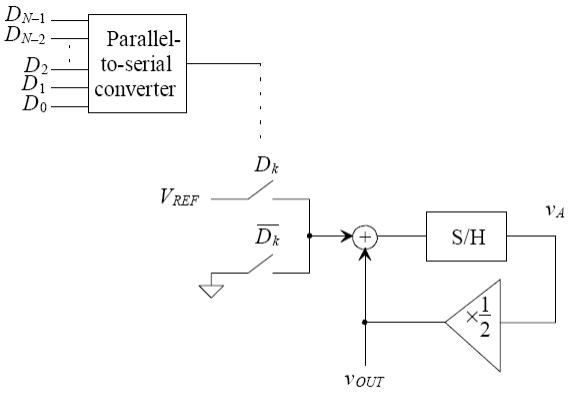


Figure 29.17 A cyclic digital-to-analog converter.

The gain error of a DAC is difference in the slope of the best fit line to the ideal transfer curve of the DAC. Consider figure 28.17:

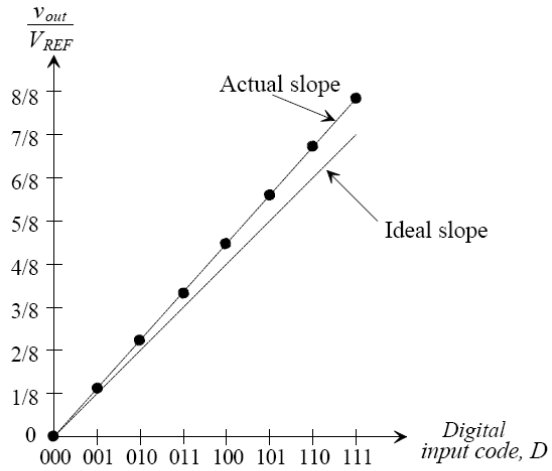


Figure 28.17 Illustration of gain error for a 3-bit DAC.

A plot of the transfer curve of our 3-bit DAC versus the ideal 3-bit DAC will give us our gain error. Realizing that the summation block has an offset of 0.2 V and the amplifier has a gain of 0.45 V/V we can build an output table for our 3-bit DAC. An example of the output table is shown below for a digital input of 110.

Table 1 Output from the 3-bit cyclic DAC used in Problem 29.15

Cycle Number, n	D_{n-1}	$v_{A(n-1)}[n-1]$	$v_{out}[n]$
1	0	0	$0.45\cdot(0+0+0.2)=0.090V$
2	0	0.090	$0.45\cdot(0+0.09+0.2)=0.131V$
3	0	0.131	$0.45\cdot(0+0.131+0.2)=0.149V$
1	1	0	$0.45\cdot(5+0+0.2)=2.34V$
2	1	0.090	$0.45\cdot(5+2.34+0.2)=3.393V$
3	1	2.381	$0.45\cdot(5+3.393+0.2)=3.867V$

Using the approach seen in Table 1 we are able to plot a transfer curve for each of the eight digital input codes and compare them to the ideal.

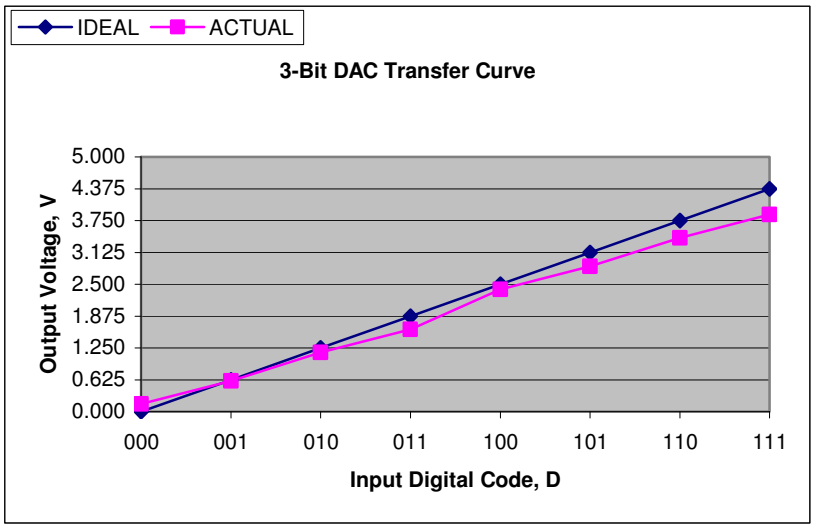
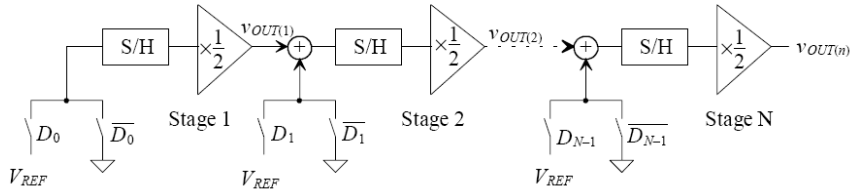


Figure 1 Transfer curve of the 3-bit cyclic DAC of problem 29.15.

The gain error can be determined by finding the slopes of both lines. Here we simply subtract the initial and final values.

$$Gain\ Error = 1-\frac{3.718/0.625}{7} = 0.15\ ^{LSB}/_{LSB}$$

29.16 Design a 3-bit pipeline DAC using V_{REF} = 5 V. (a) Determine the maximum and minimum gain values for the first-stage amplifier for the DAC to have less than ±½ LSBs of DNL assuming that the rest of the circuit is ideal. (b) Repeat for the second-stage amplifier. (c) Repeat for the last stage amplifier.



From Eq. (29.40) we can see that

$$V_{OUT} = (D_0*A_0*A_1*A_2 + D_1*A_1*A_2 + D_2*A_2)*V_{REF}$$

Where A_n is the gain of the amplifier of stage *n*, and $A_0 = A_1 = A_2 = ½$ for the ideal case.

$$V_{LSB,Ideal} = A_0*A_1*A_2*V_{REF} = ½*½*½*5V = 0.625V$$
$$½\ V_{LSB} = 0.3125V$$

(a) For the first-stage amplifier DNL error, we can look at the 000 to 001 transition

$$A_{0,MIN}*½*½*5V = 0.625V - 0.3125V$$
$$A_{0,MIN} = 0.25$$

$$A_{0,MAX}*½*½*5V = 0.625V + 0.3125V$$
$$A_{0,MAX} = 0.75$$

(b) In similar fashion, the second-stage amplifier DNL error can be seen with a 011 to 100 transition

$$V_{OUT,100} - V_{OUT,011} = ½*5V - (½*A_{1,MIN}*½ + ½*A_{1,MIN})*5V = 0.625V + 0.3125V$$
$$A_{1,MIN} = 0.42$$

$$V_{OUT,100} - V_{OUT,011} = ½*5V - (½*A_{1,MAX}*½ + ½*A_{1,MAX})*5V = 0.625V - 0.3125V$$
$$A_{1,MAX} = 0.58$$

(c) The last-stage amplifier DNL can be seen with the same 011 to 100 transition

$$V_{OUT,100} - V_{OUT,011} = A_{2,MIN}*5V - (½*½*½ + ½*½)*5V = 0.625V - 0.3125V$$
$$A_{2,MIN} = 0.44$$

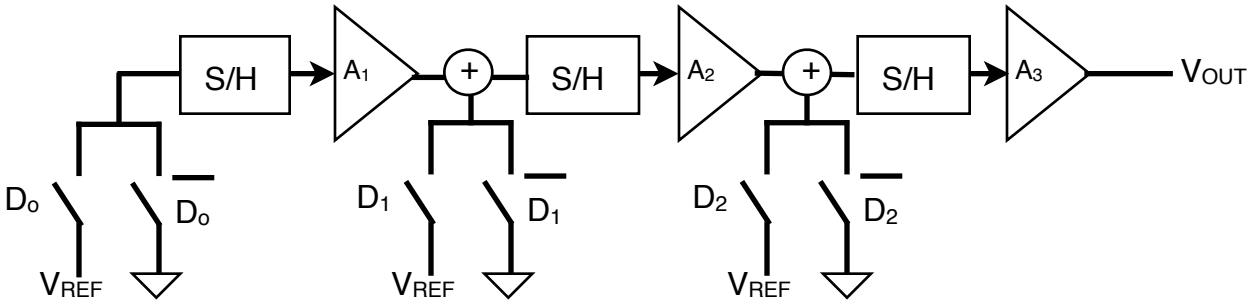
$$V_{OUT,100} - V_{OUT,011} = A_{2,MAX}*5V - (½*½*½ + ½*½)*5V = 0.625V + 0.3125V$$
$$A_{2,MAX} = 0.56$$

Justin Wood

29.17 Using the same DAC designed in Problem 29.16:

(a) determine the overall error (offset, DNL, and INL) for the DAC if the S/H amplifier in the first stage produces an offset at its output of 0.25V. Assume that all the remaining components are ideal.

The 3-bit pipeline DAC schematic is below.



With the offset applied to the first S/H, the output voltage from each stage would be calculated as follows:

$$V_{OUT1} = (D_0 \cdot V_{REF} + V_{OFFSET}) \cdot A_1$$
$$V_{OUT2} = (D_1 \cdot V_{REF} + V_{OUT1})A_2 = (D_1 \cdot V_{REF} + (D_0 \cdot V_{REF} + V_{OFFSET}) \cdot A_1)A_2$$
$$V_{OUT3} = (D_2 \cdot V_{REF} + V_{OUT2})A_3 = (D_2 \cdot V_{REF} + (D_1 \cdot V_{REF} + (D_0 \cdot V_{REF} + V_{OFFSET}) \cdot A_1)A_2)A_3$$
$$A_1 = A_2 = A_3$$
$$\therefore V_{OUT3} = V_{REF}(D_2A + D_1A^2 + D_0A^3) + V_{OFFSET}A^3$$

For V_{OFFSET} of 0.25V and A = 0.5, the offset would be: $0.25 \cdot (0.5)^3 = 0.03125V$

In terms of LSBs, the offset is: $0.03125V \cdot \frac{2^3 LSBs}{5V} = 0.05 LSBs$

For the pipeline DAC, an offset doesn't contribute to DNL because it will offset all outputs by the same amount so the step change will remain unchanged. Depending on how INL is specified, the offset could negatively impact INL. Typically, offset is removed when determining INL (ie. using the best-fit method). Therefore, INL and DNL = 0 assuming all other elements are ideal.

(b) Repeat for the second-stage S/H.

With the offset applied to the second S/H, the output voltage from each stage would be calculated as follows:

$$V_{OUT1} = (D_0 \cdot V_{REF}) \cdot A_1$$
$$V_{OUT2} = (D_1 \cdot V_{REF} + V_{OUT1} + V_{OFFSET})A_2 = (D_1 \cdot V_{REF} + (D_0 \cdot V_{REF}) \cdot A_1 + V_{OFFSET})A_2$$
$$V_{OUT3} = (D_2 \cdot V_{REF} + V_{OUT2})A_3 = (D_2 \cdot V_{REF} + (D_1 \cdot V_{REF} + (D_0 \cdot V_{REF}) \cdot A_1 + V_{OFFSET})A_2)A_3$$
$$A_1 = A_2 = A_3$$
$$\therefore V_{OUT3} = V_{REF}(D_2A + D_1A^2 + D_0A^3) + V_{OFFSET}A^2$$

For V_{OFFSET} of 0.25V and A = 0.5, the offset would be: $0.25 \cdot (0.5)^2 = 0.0625V$

In terms of LSBs, the offset is: $0.0625V \cdot \frac{2^3 LSBs}{5V} = 0.1LSBs$

Again DNL/INL are 0.

(c) Repeat for the last-stage S/H.

With the offset applied to the first S/H, the output voltage from each stage would be calculated as follows:

$$V_{OUT1} = (D_0 \cdot V_{REF}) \cdot A_1$$
$$V_{OUT2} = (D_1 \cdot V_{REF} + V_{OUT1})A_2 = (D_1 \cdot V_{REF} + (D_0 \cdot V_{REF}) \cdot A_1)A_2$$
$$V_{OUT3} = (D_2 \cdot V_{REF} + V_{OUT2} + V_{OFFSET})A_3 = (D_2 \cdot V_{REF} + (D_1 \cdot V_{REF} + (D_0 \cdot V_{REF}) \cdot A_1)A_2 + V_{OFFSET})A_3$$
$$A_1 = A_2 = A_3$$
$$\therefore V_{OUT3} = V_{REF}(D_2A + D_1A^2 + D_0A^3) + V_{OFFSET}A$$

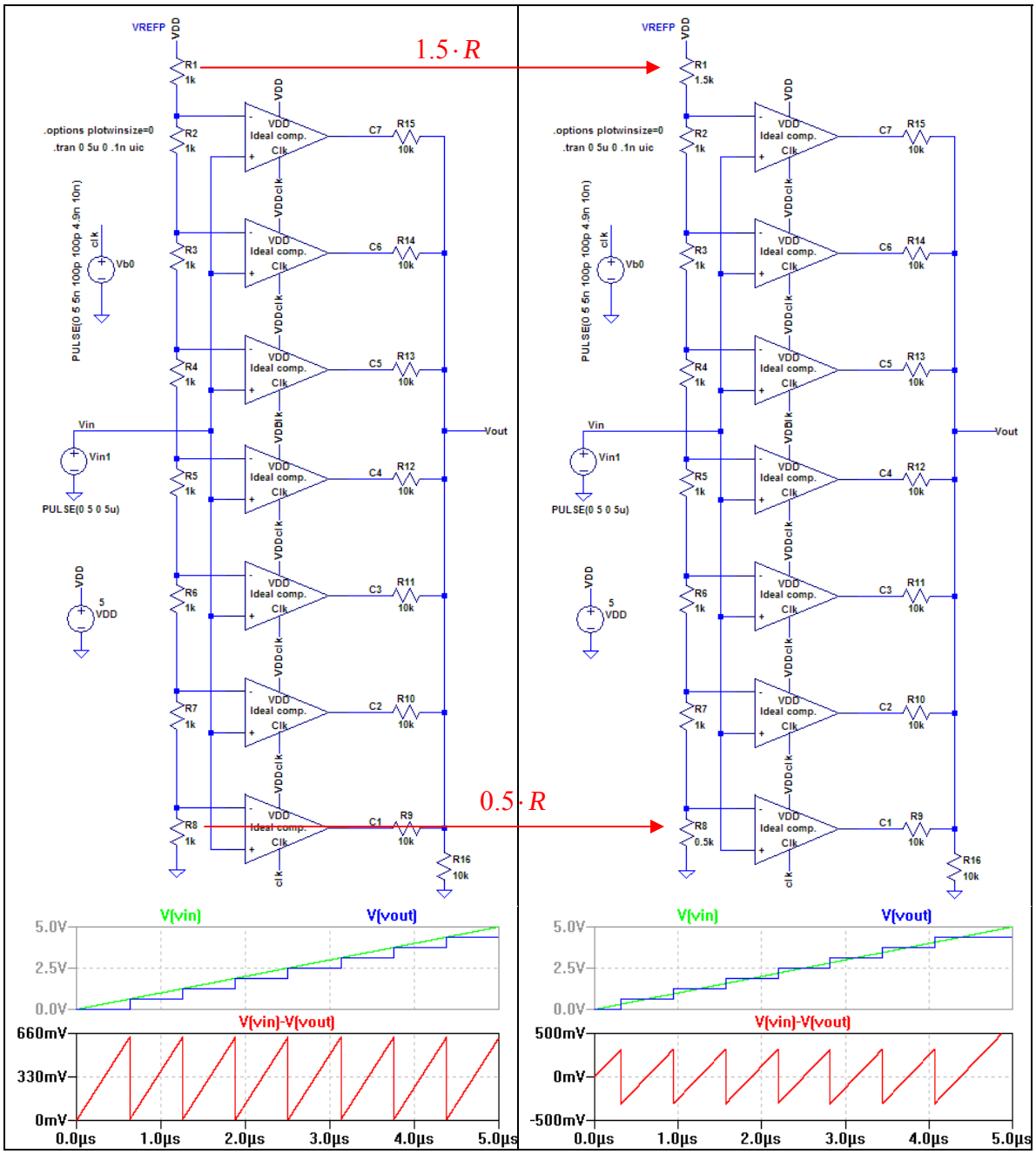
For V_{OFFSET} of 0.25V and A = 0.5, the offset would be: $0.25 \cdot (0.5) = 0.125V$

In terms of LSBs, the offset is: $0.125V \cdot \frac{2^3 LSBs}{5V} = 0.2LSBs$

Again DNL/INL are 0.

Lincoln Bollschweiler

29.18 Design a 3-bit Flash ADC with its quantization error centered about zero LSBs. Determine the worst-case DNL and INL if resistor matching is known to be 5%. Assume that V_{REF} = 5V.



From (29.48), and assuming $V_{OS} = 0$, $INL = \frac{5}{2} \cdot 0.05 = 0.125V$ or 0.2LSBs.

From (29.52), also assuming $V_{OS} = 0$, $DNL = \frac{5}{2^3} \cdot 0.05 = 0.031V$ or 0.05LSBs.

(P.29.19)Using the ADC designed in problem 29.18, determine the maximum offset that can be tolerated if all of the comparator have the same magnitude of offset, but with different polarities, to attain a DNL of less than or equal to±0.5LSB.

The Maximum DNL will occur, assuming ΔR_i is at its maximum, V_{osi} is at its maximum positive value is given in equation 29.19-1.

$$\left|DNL\right|_{Max} = \frac{V_{ref}}{2^N}.\left|\frac{\Delta R_i}{R}\right|_{Max} + 2\left|V_{os}\right|_{Max} \tag{29.19-1}$$

For the given maximum DNL of ±0.5LSB and 5% resistor mismatch from previous problem, the calculated offset voltage is

$$\frac{5}{2^{N+1}} \le \frac{5}{2^N}.0.05 + 2\left|V_{os}\right|_{Max}$$

$$\left|V_{os}\right|_{Max} \le \frac{\frac{5}{2^{N+1}} - \frac{5}{2^N}.0.05}{2}$$

$$\boxed{\left|V_{os}\right|_{Max} \le 140mV}$$

Chris Gagliano

29.20 A 4-bit Flash ADC converter has a resistor string with mismatch as shown in Table 29.1. Determine the DNL and INL of the converter. How many bits of resolution does this converter possess? V_{REF} = 5 V.

For a 4-bit ADC with V_{REF} = 5 V,

$$1\ \text{LSB} = \frac{5V}{2^4} = 0.3125\ \text{V}$$

The INL and DNL values are calculated in the table below. Note that the column labeled $V_{in,nulled\text{-}offset\text{-}gain}$, is used for the INL and DNL calculations since it contains the values with the static offset and gain errors nullified.

The offset error is calculated as follows:

$$V_{offset} = V_{in,actual}(D{=}1) - V_{in,ideal}(D{=}1) = 0.3172\ \text{V} - 0.3125\ \text{V} = 0.0047\ \text{V}$$

The gain error is calculated as follows (using the $V_{in,no\text{-}offset}$ values):

$$\text{Gain error} = 1 - \frac{\frac{4.6813V}{0.3125\,V/LSB}}{15\ \ LSB} \approx 0.0013\ \ LSB/LSB$$

The $V_{in,nulled\text{-}offset\text{-}gain}$ values in the table are then calculated by the following equation:

$$V_{in,nulled\text{-}offset\text{-}gain}(n) = V_{in,no\text{-}offset}(n) + n * 1\ LSB * Gain\ error$$

$$V_{in,nulled\text{-}offset\text{-}gain}(n) = V_{in,no\text{-}offset}(n) + n * 0.3125\ \text{V} * 0.0013$$

The resolution of the ADC is calculated using the maximum INL value from the table and knowing that it cannot be more than half an LSB.

$$\left|INL\right|_{\max} = 15.03mV \le \frac{1}{2}\cdot\frac{V_{REF}}{2^N}$$

$$2^N = \frac{5V}{2\cdot 0.01503V} \approx 166.33$$

$$N = \frac{\log(166.33)}{\log(2)} \approx 7.38$$

The resolution of the ADC is 7 bits.

Resistor	Mismtach (%)
1	2
2	1.5
3	0
4	-1
5	-0.5
6	1
7	1.5
8	2
9	2.5
10	1
11	-0.5
12	-1.5
13	-2
14	0
15	1
16	1

Table 29.1

R	ΔR
1.02	0.020
1.015	0.015
1	0.000
0.99	-0.010
0.995	-0.005
1.01	0.010
1.015	0.015
1.02	0.020
1.025	0.025
1.01	0.010
0.995	-0.005
0.985	-0.015
0.98	-0.020
1	0.000
1.01	0.010
1.01	0.010

0.08 sum

Output Code, D	Vin,ideal (V)	Vin,actual (V)	Vin,no offset (V)	Vin,nulled-offset-gain (V)	INL (mV)	DNL (mV)
0	0.0000	0.0000	0.0000	0.0000	0.00	-
1	0.3125	0.3172	0.3125	0.3129	0.41	0.41
2	0.6250	0.6328	0.6281	0.6289	3.94	3.52
3	0.9375	0.9437	0.9391	0.9403	2.80	-1.14
4	1.2500	1.2516	1.2469	1.2485	-1.45	-4.25
5	1.5625	1.5609	1.5563	1.5584	-4.15	-2.69
6	1.8750	1.8750	1.8703	1.8728	-2.18	1.97
7	2.1875	2.1906	2.1859	2.1888	1.35	3.52
8	2.5000	2.5078	2.5031	2.5064	6.43	5.08
9	2.8125	2.8265	2.8218	2.8256	13.06	6.63
10	3.1250	3.1405	3.1359	3.1400	15.03	1.97
11	3.4375	3.4499	3.4453	3.4498	12.33	-2.69
12	3.7500	3.7562	3.7516	3.7565	6.53	-5.80
13	4.0625	4.0609	4.0563	4.0617	-0.83	-7.36
14	4.3750	4.3719	4.3672	4.3730	-1.97	-1.14
15	4.6875	4.6859	4.6813	4.6875	0.00	1.97

Voffset = 0.0047 Gain error = 0.0013267

29.21 *Determine the open-loop gain required for the residue amplifier of a two-step ADC necessary to keep the converter to within ½ LSB of accuracy with resolutions of (a) 4 bits, (b) 8 bits, and (c) 10 bits.*

Consider the block diagram of a two-step Flash ADC as seen in Figure 29.26.

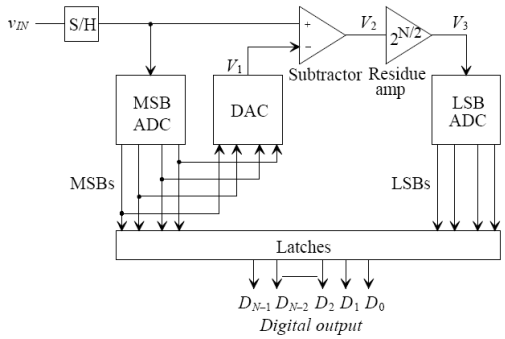


Figure 29.26 Block diagram of a two-step Flash ADC.

An advantage of the two-step Flash ADC is that each Flash ADC is only $2^{N/2}$ bits accurate. If the residue amplifier wants to be accurate to within ½ LSB we can state:

$$Accuracy = \frac{\frac{1}{2}LSB}{V_{REF}} = \frac{\frac{1}{2}\cdot V_{REF}/2^N}{V_{REF}} = \frac{1}{2^{N+1}}$$

Figure 29.26 shows that the residue amplifier has gain equal to $2^{N/2}$, we can write the open loop gain in terms of the closed loop gain:

$$A_{CL} = \frac{A_{OL}}{1 - A_{OL}\beta}$$

As A_{OL} increases the closed loop gain approaches 1/β. If we want the amplifier to have an accuracy of ½ LSB we can write the closed loop gain as:

$$A_{CL} = \frac{A_{OL}}{1 - A_{OL}\beta} = \frac{1}{\beta} - \Delta A$$

Where ΔA is the accuracy. Solving for the open loop gain gives us:

$$A_{OL} \approx \frac{2^{N+1}}{\beta} = 2^{N+1}\cdot 2^{N/2}$$

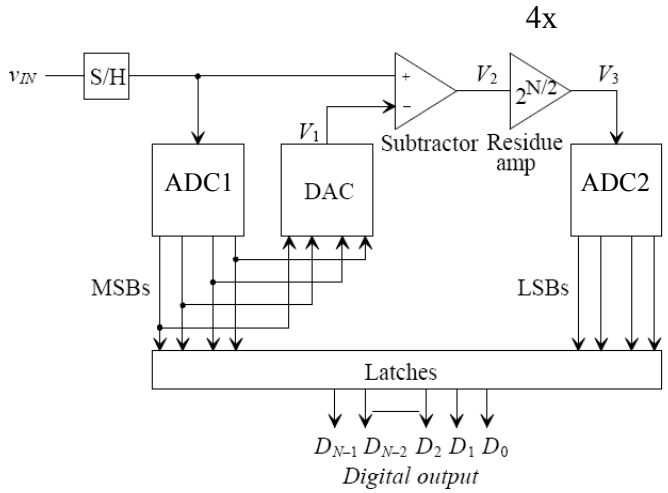
Using the equation above, we can state that the requirements of the open loop gain for each number of bits:

4 bits $\rightarrow 2^7 = 128$

8 bits $\rightarrow 2^{13} = 8192$

10 bits $\rightarrow 2^{16} = 65536$

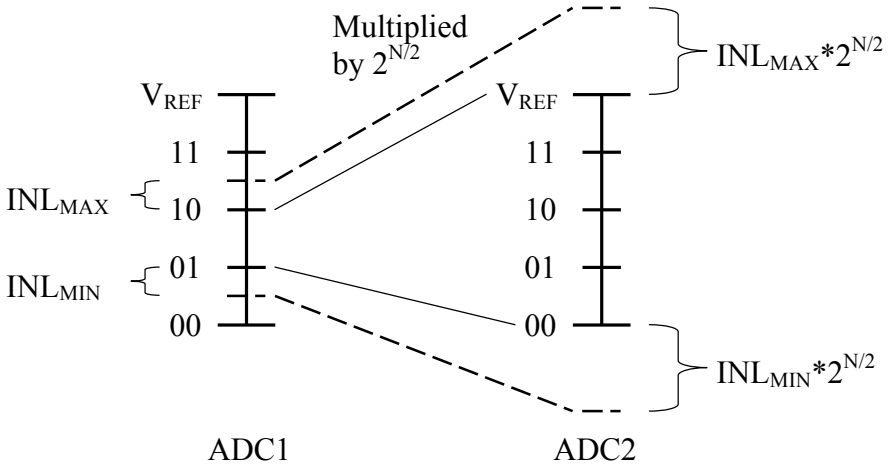
29.22 Assume that a 4-bit, two-step Flash ADC uses two separate Flash converters for the MSB and LSB ADCs. Assuming that all other components are ideal, show that the first Flash converter needs to be more accurate than the second converter. Assume that V_{REF} = 5 V.



In the ideal case, the V_2 must be between 0 and V_{REF}. If we include INL, the V_2 value can be between $-INL_{MIN,ADC1}$ and $V_{REF} + INL_{MAX,ADC1}$.

Since $V_3 = V_2 * 2^{N/2}$, and this is a 4-bit ADC, we can see that the range on V_3 will be between $-(INL_{MIN,ADC1})*4$ and $V_{REF} + (INL_{MAX,ADC1})*4$. So essentially, any error from the first ADC conversion is multiplied along with the residual voltage by the residue amplifier.

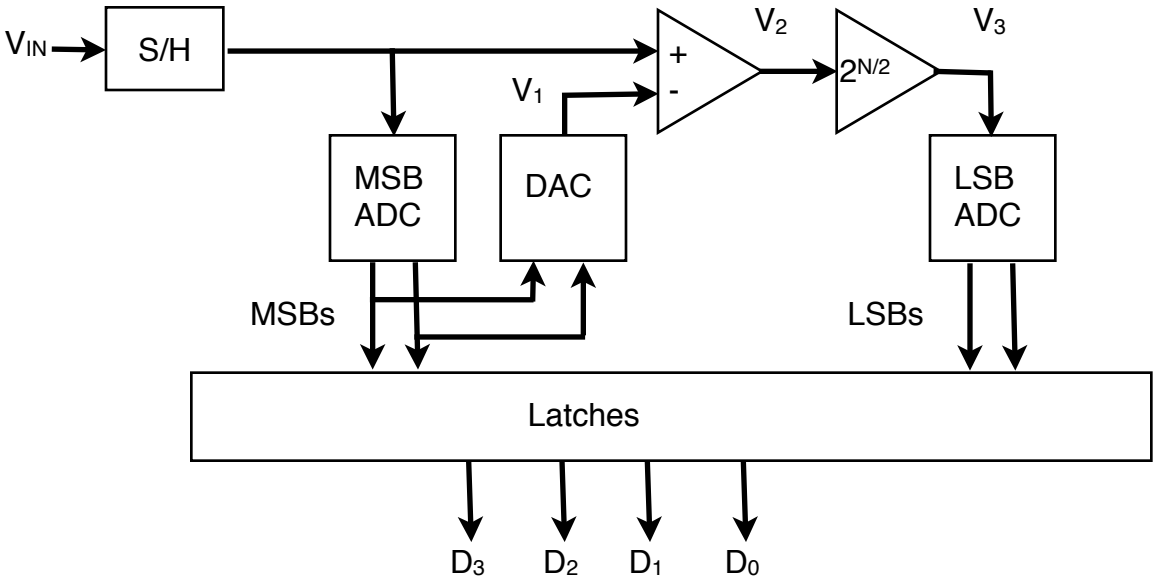
For this 4-bit ADC, if the INL/DNL needs to be < ½ LSB overall, then for the first ADC, the INL/DNL needs to be < $^1/_8$ LSB, and the second ADC can be < ½ LSB.



29.23 Repeat Ex. 29.12 for V_{IN} = 3, 5, 7.5, 14.75 V.

Example 29.12
Assume that the two-step ADC shown in Fig. 29.26 has four bits of resolution. Make a table listing the MSBs, V_1, V_2, V_3, and the LSBs for V_{IN} = 3, 5, 7.5, 14.75 V assuming that V_{REF} = 16V.

With 4-bit resolution, Figure 29.26 would be as follows:



The MSB and LSB ADCs in the picture are both 2-bit ADCs and their LSBs are equal to 4V $\left(\frac{16V}{2^2} = 4V\right)$. First, lets calculate the output for V_{IN}=3V. Starting with the MSB ADC, D_3D_2 would be 00 until $V_{IN} > 4V$ (LSB). V_1 would then be 0, V_2 would be 3V. N=4 and $V_3 = 3*(2^2)$ or 12V. The output of the LSB ADC would then be 11. Final output code is 0011. Output code for V_{IN} are similarly calculated as shown in the table.

V_{IN}	D_3D_2(MSBs)	V_1	V_2	V_3	D_1D_0(LSBs)
3	00	0	3	12	11
5	01	4	1	4	01
7.5	01	4	3.5	14	11
14.75	11	12	2.75	11	10

Lincoln Bollschweiler

29.24 Repeat Ex. 29.13 for V_{IN} = 1, 3, 6, 7 V and V_{REF} = 8V.

> *Example 29.13 – Assume that the pipeline converter shown in Fig. 29.30 is a 3-bit converter. Analyze the conversion process by making a table of the following variables: D_2, D_1, D_0, V_3, and V_2 for V_{IN} = 2, 3, and 4.5 V. Assume that V_{REF} = 5V, V_3 is the residue voltage out of the first stage, V_2 is the residue from the second.*

With a V_{REF} of 8V, all comparators will give an output of 1 for vin_p of 4V or greater; output of 0 otherwise.

v_{IN} (V)	V_3 (V)	V_2 (V)	Digital Out ($D_2D_1D_0$)
1.0	2	4	001
3.0	6	4	011
6.0	4	0	110
7.0	6	4	111

As is expected, since the reference voltage is 8 and the LSB = $8/2^2$ = 1V, the digital code is simply the input (decimal) converted to 3-bit binary.

(P.29.25)Assume that 8-bit pipeline ADC was fabricated and that all the amplifiers had a gain of 2.1V/V instead of 2V/V. If V_{IN}=3V and V_{REF}=5V, what would be the resulting digital output if the remaining components were considered to be ideal? What are the DNL and INL for this converter?

8-bit Pipelined ADC requires 8-steps to convert the given analog signal into 8-bit digital codes. The positive input of the comparator to the next stage is given by equation 29.25-1.Table 29.25-1 shows the conversion of the analog signal into digital codes in 8 steps.

$$V_{IN}(n+1) = \left(V_{IN}(n) - \frac{V_{REF}.C_{OUT}(n)}{2} \right).Gain \tag{29.25.1}$$

Table 29.25-1 8-bit Pipelined ADC conversion for V_{IN} = 3V, V_{REF} = 5V

STEP(n)	Comparator's Positive Input $V_{IN}(n)$	Comparator's Negative Input($V_{REF}/2$)	Comparator Output($C_{OUT}(n)$)
1	3	2.5	1
2	1.05	2.5	0
3	2.205	2.5	0
4	4.6305	2.5	1
5	4.47405	2.5	1
6	4.145505	2.5	1
7	3.4555605	2.5	1
8	2.00667705	2.5	0

8-bit Pipelined ADC output = 1 0 0 1 1 1 1 0

We can write the input analog voltage in terms of digital codes with a gain of the amplifier of 2.1 V/V for N-bit Pipelined ADC as

$$V_{IN,N} = \frac{1}{2}D_{N-1}.V_{REF} + \frac{1}{2}D_{N-2}.\frac{V_{REF}}{Gain} + ...+ \frac{1}{2}D_1.\frac{V_{REF}}{Gain^{N-2}} + \frac{1}{2}D_0.\frac{V_{REF}}{Gain^{N-1}} \tag{29.25-2}$$

Using the above equation, DNL and INL of 8-bit pipelined ADC is plotted in figure 29.25-1 and 2 respectively. Calculation of INL and DNL of the converter is shown in Table 29.25-2 for digital outputs ranging from 0 to 6.

Table 29.25-2 8-bit Pipelined ADC INL and DNL Calculation

Possible Digital O/P (n)	D0	D1	D2	D3	D4	D5	D6	D7	Corresponding Analog Input(X_n) Calculation Using Equation 29.25-2	X_n in LSB (Y_n)	Y_n Shifted by 0.5LSB (Z_n)	Ideal Analog Input in LSB (I_n)	DNL(n) = (Z_{n+1}-Z_n) - 1LSB	INL(n) =Z_n- I_n
0	0	0	0	0	0	0	0	0	0	0	0.5	0.5	-	0
1	1	0	0	0	0	0	0	0	0.013880495	0.71069	1.21069	1.5	-0.28931	-0.28930
2	0	1	0	0	0	0	0	0	0.029149039	1.49245	1.99245	2.5	-0.218241	-0.50755
3	1	1	0	0	0	0	0	0	0.043029534	2.20314	2.70314	3.5	-0.28931	-0.79685
4	0	0	1	0	0	0	0	0	0.061212982	3.134145	3.634145	4.5	-0.068996	-0.86585
5	1	0	1	0	0	0	0	0	0.075093476	3.844835	4.344835	5.5	-0.28931	-1.15516
6	0	1	1	0	0	0	0	0	0.090362021	4.626595	5.126595	6.5	-0.218241	-1.37340

DNL of the 8-bit Pipelined ADC:

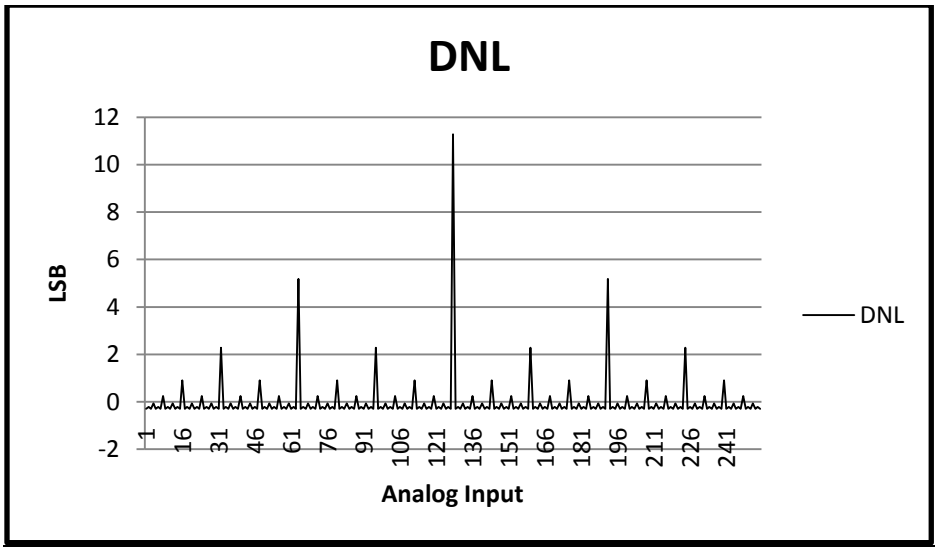


Figure – 29.25-1 DNL of the 8-bit Pipelined ADC

INL of the 8-bit Pipelined ADC:

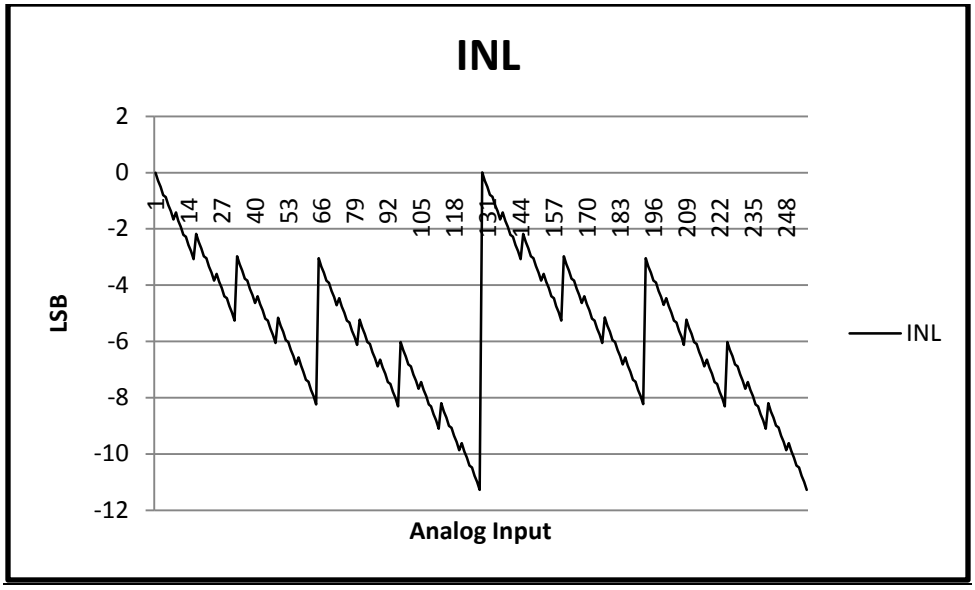
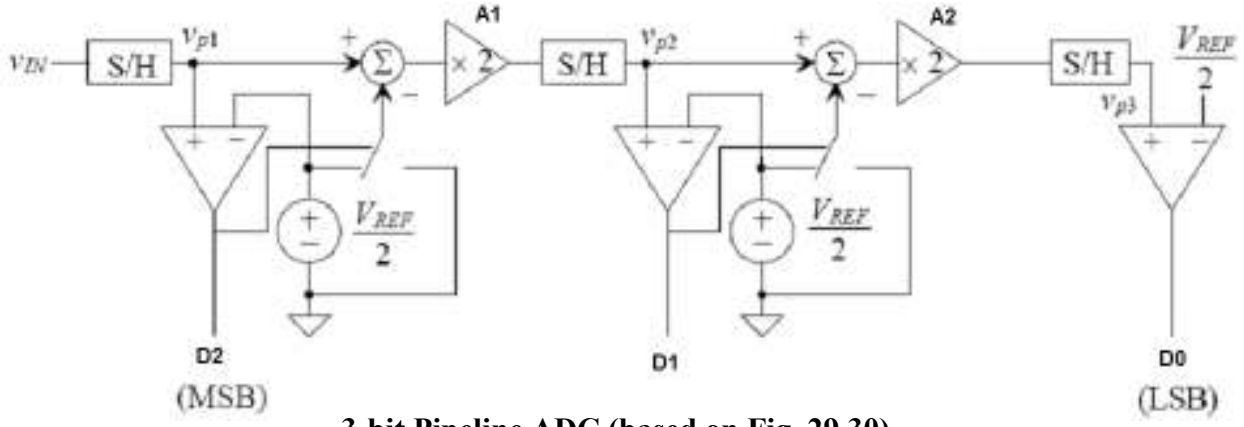


Figure – 29.25-2 INL of the 8-bit Pipelined ADC

From the figure 29.25-1, 2 the maximum and minimum INL and DNL are given as

	DNL	INL
Maximum	11.28259	0.001638
Minimum	-0.28931	-11.281

29.26 Show that the first-stage accuracy is the most critical for a 3-bit, 1-bit per stage pipeline ADC by generating a transfer curve and determining DNL and INL for the ADC for three cases: (1) The gain of the first-stage residue amplifier set equal to 2.2 V/V, (2) the second-stage residue amplifier set equal to 2.2 V/V. For each case, assume that the remaining components are ideal. Assume that V_{REF} = 5V.



3-bit Pipeline ADC (based on Fig. 29.30)

D_2 will transition high when $V_{p1} = \frac{1}{2} \cdot V_{REF}$ and since $V_{p1} = V_{IN}$ we can write the input voltage at which D_2 transitions high as:

$$V_{IN,1} = \frac{1}{2} \cdot V_{REF}$$

D_1 will transition high when $V_{p2} = \frac{1}{2} \cdot V_{REF}$ and we can write V_{p2} as:

$$V_{p2} = \left[V_{p1} - \frac{1}{2} \cdot V_{REF} \cdot D_2 \right] \cdot A_1$$

We can then solve for the input voltage at which D_1 transitions high, keeping in mind that $V_{p1} = V_{IN}$:

$$\frac{1}{2} \cdot V_{REF} = \left[V_{IN,2} - \frac{1}{2} \cdot V_{REF} \cdot D_2 \right] \cdot A_1$$

$$V_{IN,2} = \frac{1}{2 \cdot A_1} \cdot V_{REF} + \frac{1}{2} \cdot V_{REF} \cdot D_2$$

D_0 will transition high when $V_{p3} = \frac{1}{2} \cdot V_{REF}$ and we can write V_{p3} as:

$$V_{p3} = \left[V_{p2} - \frac{1}{2} \cdot V_{REF} \cdot D_1 \right] \cdot A_2 = \left[\underbrace{\left(V_{p1} - \frac{1}{2} \cdot V_{REF} \cdot D_2 \right) \cdot A_1}_{Vp2} - \frac{1}{2} \cdot V_{REF} \cdot D_1 \right] \cdot A_2$$

We can then solve for the input voltage at which D_0 transitions high, again keeping in mind that $V_{p1} = V_{IN}$:

$$\frac{1}{2} \cdot V_{REF} = \left[\left(V_{IN,3} - \frac{1}{2} \cdot V_{REF} \cdot D_2 \right) \cdot A_1 - \frac{1}{2} \cdot V_{REF} \cdot D_1 \right] \cdot A_2$$

$$V_{IN,3} = \frac{1}{2 \cdot A_1 \cdot A_2} \cdot V_{REF} + \frac{1}{2 \cdot A_1} \cdot V_{REF} \cdot D_1 + \frac{1}{2} \cdot V_{REF} \cdot D_2$$

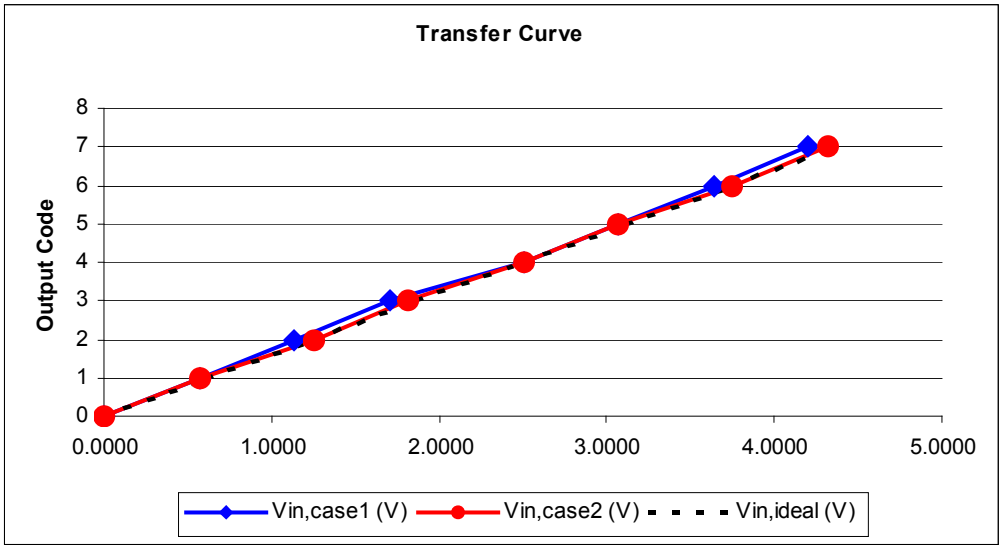
So, for a given output code, we can write a corresponding expression for V_{IN} and use it to generate a table of values for the two cases presented in the problem statement. We can then calculate the INL and DNL values for both cases to see how they compare.

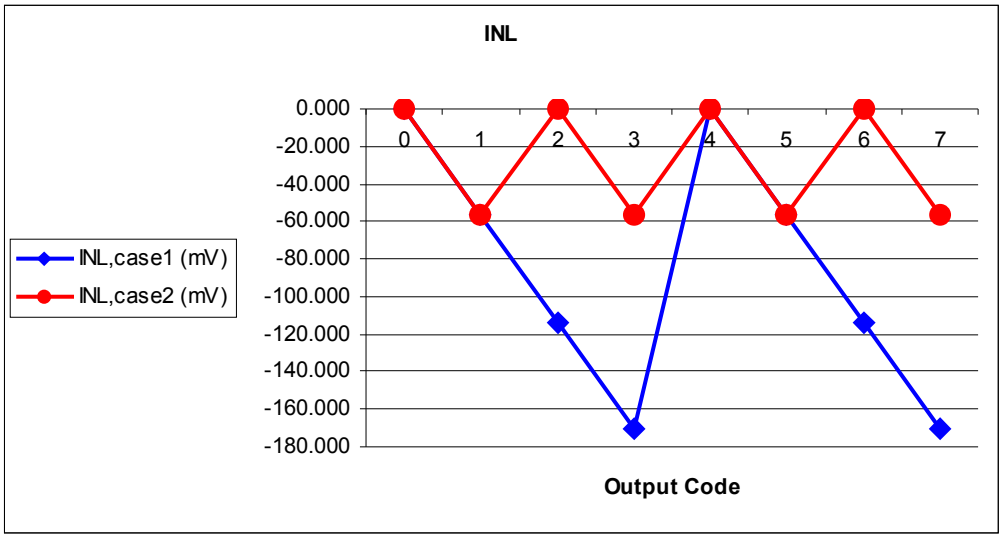
The output code values and corresponding input voltages for both cases are shown below. The transfer curve shows that the second case ($A_1 = 2.0$, $A_2 = 2.2$) is more optimal (closer to ideal curve) than the first case ($A_1 = 2.2$, $A_2 = 2.0$). The INL and DNL values are also better for the second case when compared to the first case. We can then conclude that the first stage accuracy is the most critical.

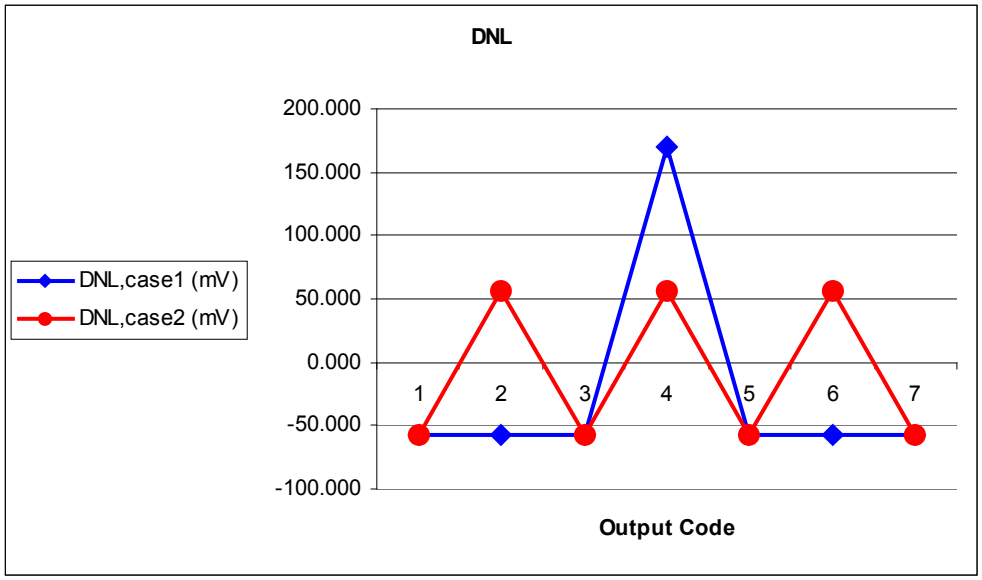
$$V_{IN} = \frac{1}{2 \cdot A_1 \cdot A_2} \cdot V_{REF} \cdot D_0 + \frac{1}{2 \cdot A_1} \cdot V_{REF} \cdot D_1 + \frac{1}{2} \cdot V_{REF} \cdot D_2 + Residue$$

	Case 1	Case 2
Vref	5.0	5.0
A1	2.2	2.0
A2	2.0	2.2

Output Code	D2	D1	D0	Vin,ideal (V)	Vin,case1 (V)	Vin,case2 (V)	INL,case1 (mV)	INL,case2 (mV)	DNL,case1 (mV)	DNL,case2 (mV)
0	0	0	0	0.0000	0.0000	0.0000	0.000	0.000	-	-
1	0	0	1	0.6250	0.5682	0.5682	-56.818	-56.818	-56.818	-56.818
2	0	1	0	1.2500	1.1364	1.2500	-113.636	0.000	-56.818	56.818
3	0	1	1	1.8750	1.7045	1.8182	-170.455	-56.818	-56.818	-56.818
4	1	0	0	2.5000	2.5000	2.5000	0.000	0.000	170.455	56.818
5	1	0	1	3.1250	3.0682	3.0682	-56.818	-56.818	-56.818	-56.818
6	1	1	0	3.7500	3.6364	3.7500	-113.636	0.000	-56.818	56.818
7	1	1	1	4.3750	4.2045	4.3182	-170.455	-56.818	-56.818	-56.818


Transfer Curve
Output Code
8
7
6
5
4
3
2
1
0
0.0000
1.0000
2.0000
3.0000
4.0000
5.0000
Vin,case1 (V)
Vin,case2 (V)
Vin,ideal (V)


INL
INL,case1 (mV)
INL,case2 (mV)
0.000
-20.000
-40.000
-60.000
-80.000
-100.000
-120.000
-140.000
-160.000
-180.000
0
1
2
3
4
5
6
7
Output Code


DNL
DNL,case1 (mV)
DNL,case2 (mV)
200.000
150.000
100.000
50.000
0.000
-50.000
-100.000
1
2
3
4
5
6
7
Output Code

29.27 *An 8-bit single-slope ADC with a 5V reference is used to convert a slow-moving analog signal. What is the maximum conversion time assuming that the clock frequency is 1 MHz? What is the maximum frequency of the analog signal? What is the maximum value of the analog signal which can be converted?*

Figure 29.32 depicts a block diagram of a single-slope integrating ADC.

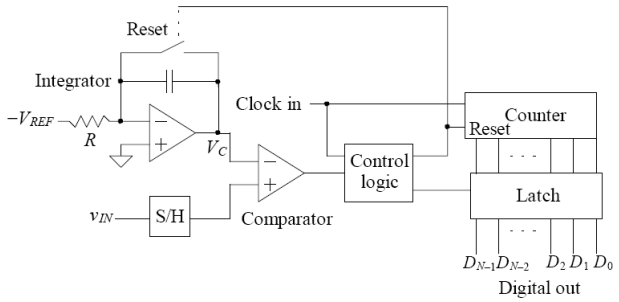


Figure 29.32 Block diagram of a single-slope ADC.

As discussed in section 29.2.4 the single-slope integrating ADC operates by placing a negative (with respect to the input) voltage on the inverting side of the comparator and the sampled input on the other input of the comparator. The counter is used to count how many clock cycles it takes to integrate the reference current before the V_C voltage exceeds the sampled input voltage. When the comparator switches states the count value is latched and the integrator is reset. Figure 29.33 shows one conversion cycle.

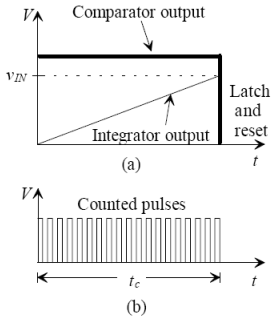


Figure 29.33 Single-slope ADC timing diagrams for (a) the comparator inputs and outputs and (b) the resulting counted pulses.

The digital output code will count from 00000000 (0) to 11111111 (255). The minimum code refers to the minimum voltage and the maximum count refers to the maximum input voltage which is equal to V_{REF} – 1 LSB. Using equation 29.79 we can say:

$$t_c = \frac{v_{in}}{V_{REF}} \cdot 2^N \cdot T_{CLK}$$

$$t_c = \frac{V_{REF}\left(1 - \frac{1}{2^N}\right)}{V_{REF}} \cdot 2^N \cdot \frac{1}{f_{CK}} = \frac{2^N - 1}{f_{CK}} = \frac{255}{1MHz} = 255\mu s$$

The equation above shows that the full sampling time of the ADC is 255 µs. Using Nyquist's Criteria we can say that the sampling frequency must be equal to twice the input frequency, therefore we can say:

$$\frac{1}{255\mu s} > 2f_{in}$$

$$f_{in} \approx 2kHz$$

The maximum value of the input signal is simply equal to V_{REF} – 1 LSB or ~4.98 V, while the minimum voltage is 0 V.

29.28 An 8-bit single-slope ADC with a 5V reference uses a clock frequency of 1MHz. Assuming that all of the other components are ideal, what is the limitation on the value of RC? What is the tolerance of the clock frequency which will ensure less than 0.5 LSB of INL?

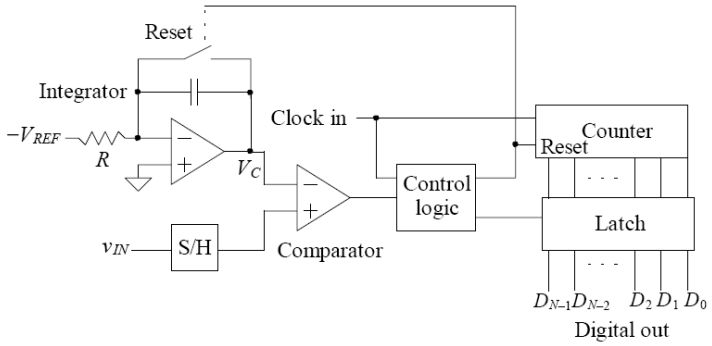


Figure 29.32 Block diagram of a single-slope ADC.

We want the V_C node to fully charge within a single clock cycle. From Eq. (29.81), we can find the value of RC for a full-scale analog voltage of 5V, assuming that max input voltage is equal to the reference voltage.

$$RC = \frac{VREF \cdot t_c}{V_C} = \frac{5V}{5V \cdot f_c} = 1us$$

$$RC \le 1us$$

To find the clock frequency of the clock jitter, we start with finding that 0.5 LSB is 0.5 * 5V / 2^8, or 9.77mV. Using Eq. (29.81) again we can find the Δt that is equivalent to this error.

$$\Delta t = \frac{RC \cdot \Delta V_C}{VREF} = \frac{1us \cdot 9.77mV}{5V} = 1.95ns$$

So the clock period must be 1us +/- 1.95ns, or $1.00195MHz \le f_{CLK} \le .99805MHz$.

Justin Wood

29.29 An 8-bit dual slope ADC with a 5V reference is used to convert the same analog signal in Problem 29.27. What is the maximum conversion time assuming that the clock frequency is 1 Mhz? What is the minimum conversion time that can be attained? If the analog signal is 2.5V, what will be the total conversion time?

The analog signal from 29.27 was defined as a slow-moving signal. Therefore, the discussion on pages 998 -1002 is valid (ie. $f_{CLK} >> f_{IN}$). Since we are dealing with a dual-slope topology, the total conversion time is the sum of the charging time (T_1) and the discharging time (T_2).

T_1 is fixed and always takes $2^N * t_{CLK}$ before the counter overflows. For our 8-bit ADC with 1Mhz clock frequency, T_1 is equal to 256µs. The discharge time can then be calculated from equation 29.86 shown below:

$$|v_{in}| \cdot T_1 = V_{REF} \cdot T_2$$

The maximum conversion time occurs when v_{in} equals $-V_{REF}$. The discharge time, T_2, is then equal to the charging time, T_1. The conversion time is then $2T_1$ or 512µs.

The minimum conversion time is achieved when v_{in} is equal to 0. The conversion time is then just T_1 or 256µs (T_2=0).

If the analog signal is 2.5V, the conversion time is (knowing T_1=256µs):

$$|v_{in}| \cdot T_1 = V_{REF} \cdot T_2$$
$$|2.5| \cdot 256\mu s = 5 \cdot T_2$$
$$T_2 = 128\mu s$$
$$T_{TOTAL} = T_1 + T_2 = 384\mu s$$

Lincoln Bollschweiler

29.30 Discuss the advantages and disadvantages of using a dual-slope versus a single-slope ADC architecture.

One of the more obvious disadvantages to the dual slope is the fact that the required charging period adds time to the conversion over the single-slope. For a full scale signal this can mean twice the time (2^N clocks up, 2^N clocks down) . Another disadvantage is the use of additional circuit components which mean a larger layout area required.

An advantage of the dual-slope converter is the fact that the same integrator and clock are used to produce both slopes. This means that any non-idealities inherent to the converter will be added to each conversion (slope) equally and, ideally, cancel out. This makes for a much more accurate converter than the single-slope, making design specifications less stringent (lower-power, smaller devices, etc).

(P.29.31)Repeat Ex. 29.15 for a 4-bit successive approximation ADC using V_{REF}=5V for V_{IN}=1, 3 and full-scale.

Let D^B_3, D^B_2, D^B_1 and D^B_0 are the initial outputs of SAR before the comparator makes its decision. B_3, B_2, B_1 and B_0 are the inputs of SAR. D_3, D_2, D_1 and D_0 are the final output of the SAR ADC after comparator decision. V_{OUT} is the output of 4-bit DAC and C_{OUT} is the output of comparator.

When V_{REF} = 5V, V_{IN} = 1V,

STEP	B_3	B_2	B_1	B_0	D^B_3	D^B_2	D^B_1	D^B_0	V_{OUT}(V)	C_{OUT}	D_3	D_2	D_1	D_0
1	1	0	0	0	1	0	0	0	2.5	1	0	0	0	0
2	0	1	0	0	0	1	0	0	1.25	1	0	0	0	0
3	0	0	1	0	0	0	1	0	0.625	0	0	0	1	0
4	0	0	0	1	0	0	1	1	0.9375	0	0	0	1	1

4-bit ADC output = 0 0 1 1

When V_{REF} = 5V, V_{IN} = 3V,

STEP	B_3	B_2	B_1	B_0	D^B_3	D^B_2	D^B_1	D^B_0	V_{OUT}(V)	C_{OUT}	D_3	D_2	D_1	D_0
1	1	0	0	0	1	0	0	0	2.5	0	1	0	0	0
2	0	1	0	0	1	1	0	0	3.75	1	1	0	0	0
3	0	0	1	0	1	0	1	0	3.125	1	1	0	0	0
4	0	0	0	1	1	0	0	1	2.8125	0	1	0	0	1

4-bit ADC output = 1 0 0 1

When V_{REF} = 5V, V_{IN} = 5V,

STEP	B_3	B_2	B_1	B_0	D^B_3	D^B_2	D^B_1	D^B_0	V_{OUT}(V)	C_{OUT}	D_3	D_2	D_1	D_0
1	1	0	0	0	1	0	0	0	2.5	0	1	0	0	0
2	0	1	0	0	1	1	0	0	3.75	0	1	1	0	0
3	0	0	1	0	1	1	1	0	4.375	0	1	1	1	0
4	0	0	0	1	1	1	1	1	4.6875	0	1	1	1	1

4-bit ADC output = 1 1 1 1

29.32 Assume that v_{in} = 2.49 V for the ADC used in Problem 29.31 and that the comparator, because of its offset, makes the wrong decision for the MSB conversion. What will be the final digital output? Repeat for v_{in} = 0.3025 V, assuming that the comparator makes the wrong decision on the LSB.

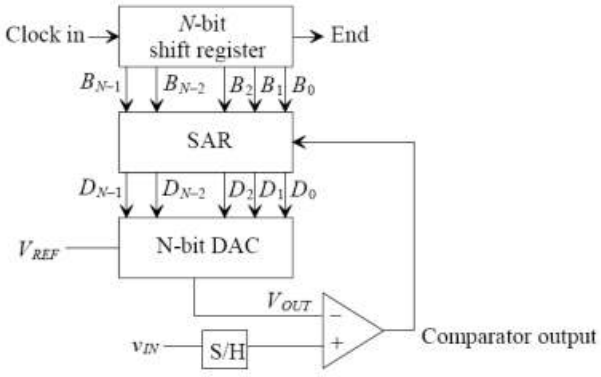


Figure 29.36 Block diagram of the successive approximation ADC.

As in Example 29.15, we designate D_3'D_2'D_1'D_0' as the initial output of the SAR before the comparator makes its decision. The final value is designated as $D_3D_2D_1D_0$.

For the case where V_{IN} = 2.49 V, let's first look at the ideal case where the comparator does not make any wrong decisions and then look at the case where the comparator makes the wrong decision on the MSB.

Comparator makes all correct decisions

Step	Vin (V)	B3	B2	B1	B0	D3'	D2'	D1'	D0'	Vout (V)	Comp Out	D3	D2	D1	D0
T1	2.49	1	0	0	0	1	0	0	0	2.5000	1	0	0	0	0
T2	2.49	0	1	0	0	0	1	0	0	1.2500	0	0	1	0	0
T3	2.49	0	0	1	0	0	1	1	0	1.8750	0	0	1	1	0
T4	2.49	0	0	0	1	0	1	1	1	2.1875	0	0	1	1	1

Comparator makes wrong decision on MSB

Step	Vin (V)	B3	B2	B1	B0	D3'	D2'	D1'	D0'	Vout (V)	Comp Out	D3	D2	D1	D0
T1	2.49	1	0	0	0	1	0	0	0	2.5000	0 (mistake)	1	0	0	0
T2	2.49	0	1	0	0	1	1	0	0	3.7500	1	1	0	0	0
T3	2.49	0	0	1	0	1	0	1	0	3.1250	1	1	0	0	0
T4	2.49	0	0	0	1	1	0	0	1	2.8125	1	1	0	0	0

We can see that the final output is 1000 when the comparator makes the wrong decision on the MSB whereas the final output should be 0111.

Next, let's consider the case where V_{IN} = 0.3025 V and look at the results when the comparator does not make any wrong decisions compared to when the comparator makes a wrong decision on the LSB.

Comparator makes all correct decisions

Step	Vin (V)	B3	B2	B1	B0	D3'	D2'	D1'	D0'	Vout (V)	Comp Out	D3	D2	D1	D0
T1	0.3025	1	0	0	0	1	0	0	0	2.5000	1	0	0	0	0
T2	0.3025	0	1	0	0	0	1	0	0	1.2500	1	0	0	0	0
T3	0.3025	0	0	1	0	0	0	1	0	0.6250	1	0	0	0	0
T4	0.3025	0	0	0	1	0	0	0	1	0.3125	1	0	0	0	0

Comparator makes wrong decision on LSB

Step	Vin (V)	B3	B2	B1	B0	D3'	D2'	D1'	D0'	Vout (V)	Comp Out	D3	D2	D1	D0
T1	0.3025	1	0	0	0	1	0	0	0	2.5000	1	0	0	0	0
T2	0.3025	0	1	0	0	0	1	0	0	1.2500	1	0	0	0	0
T3	0.3025	0	0	1	0	0	0	1	0	0.6250	1	0	0	0	0
T4	0.3025	0	0	0	1	0	0	0	1	0.3125	0 (mistake)	0	0	0	1

The final output is 0001 when the comparator makes the wrong decision on the LSB whereas the final output should be 0000 because the input voltage is less than 1 LSB.

29.33 *Design a 3-bit, charge-redistribution ADC similar to that shown in Fig. 29.39 and determine the voltage on the top plate of the capacitor array throughout the conversion process for v_{IN} = 2, 3, and 4 V, assuming that V_{REF} = 5 V. Assume that all components are ideal. Draw the equivalent circuit for each bit decision.*

Figure 29.39 is shown below:

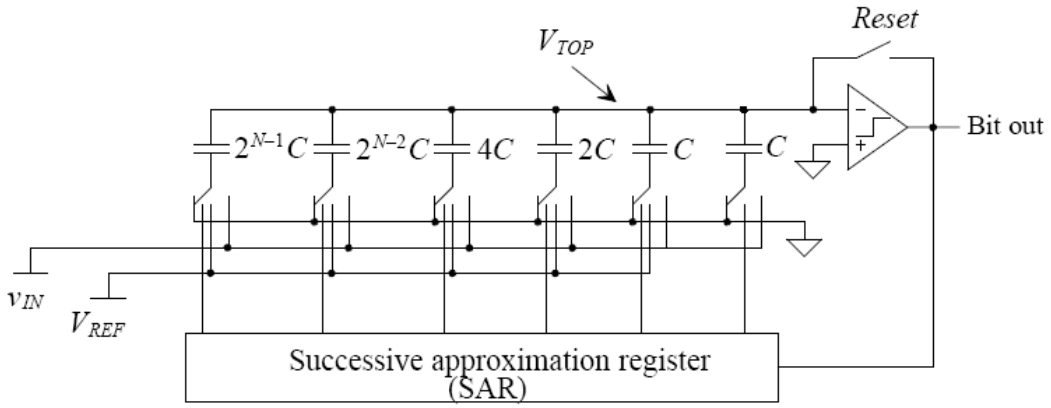
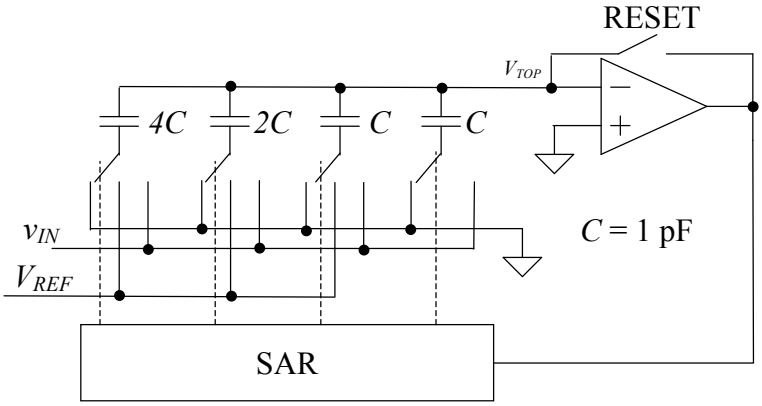


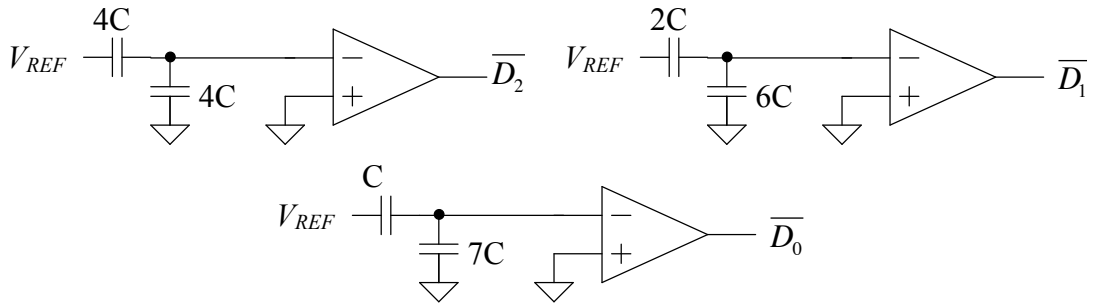
Figure 29.39 A charge redistribution ADC using a binary-weighted capacitor array DAC.

Using Figure 29.39 it is possible to design a 3-bit charge redistribution ADC, the completed design is seen in the figure below.



***F*1** – 3-*bit charge redistribution ADC*

In order to draw an equivalent circuit for each bit we simply connect each capacitor to V_{REF} while grounding all of the other capacitors. The final 1 pF capacitor remains connected to ground for each bit.



You have to notice that when the conversion begins the MSB capacitor is connected to V_{REF} and a voltage of $V_{REF}/2$ (or 2.5 V) is added to V_{TOP}. For a 2 V input this leaves a positive 0.5 V on V_{TOP}, if the capacitance is not reset to v_{IN} the comparator output will remain in a low state. Due to this, the control logic will need to save the state of each bit (connected to V_{REF} if the comparator output stays high, or connect to *GND* if the comparator output goes low), reset the top voltage, and continue the conversion process with the next bit. In an attempt to understand this the tables below show the conversion process for an input voltage of 2 V, 3 V, and 4 V.

For 2 V input:

Step	*$D_2D_1D_0$*	*V_{TOP} (V)*	*Comparator Out*
---	*---*	*- 2*	*---*
1	*100*	*- 2 + 2.5 = 0.5*	*Low (reset)*
2	*010*	*-2 + 1.25 = -0.75*	*High (save)*
3	*011*	*-2 + 1.25 + 0.625 = -0.125*	*High (save)*

Output code = 011

For 3 V input:

Step	*$D_2D_1D_0$*	*V_{TOP} (V)*	*Comparator Out*
---	*---*	*- 3*	*---*
1	*100*	*- 3 + 2.5 = -0.5*	*High (save)*
2	*110*	*-3 + 2.5 + 1.25 = 0.75*	*Low (reset)*
3	*101*	*-3 + 2.5 + 0.625 = 0.125*	*Low (reset)*

Output code = 100

For 4 V input:

Step	*$D_2D_1D_0$*	*V_{TOP} (V)*	*Comparator Out*
---	*---*	*- 4*	*---*
1	*100*	*- 4 + 2.5 = -1.5*	*High (save)*
2	*110*	*-4 + 2.5 + 1.25 = -0.25*	*High (save)*
3	*111*	*-4 + 2.5 +1.25 + 0.625 = 0.375*	*Low (reset)*

Output code = 110

29.34 Determine the maximum INL and maximum DNL of the ADC designed in Problem 29.33 assuming that the capacitor array matching is 1%. Assume that the remaining components are ideal and that the unit capacitance, C, is 1pF.

Problem 29.33 is a 3-bit charge distribution ADC like Figure 29.39

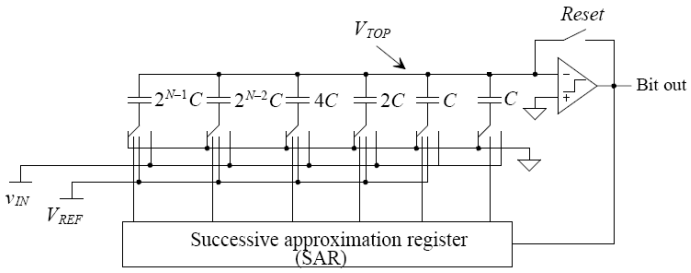


Figure 29.39 A charge redistribution ADC using a binary-weighted capacitor array DAC.

From Eq. (29.91) we get the INL for $\frac{\Delta C}{C} = 1\%$:

$$|INL|_{\max} = \frac{V_{REF}}{2} \cdot \frac{\Delta C}{C} = 25mV = 0.04LSB$$

From Eq. (29.93) we get the DNL:

$$DNL_{\max} = \frac{(2^N - 1) \cdot V_{REF}}{2^N} \cdot \frac{|\Delta C|}{C} = 43.75mV = 0.07LSB$$

Justin Wood

29.35 Show that the charge redistribution ADC used in Problems 29.32 and 29.33 is immune to comparator offset by assuming an initial offset voltage of 0.3 and determining the conversion for V_{IN}=2V.

With V_{OS} = 0.3V and V_{IN} = 2V, the conversion process for the charge redistribution ADC would be as follows (using equations 29.88, 29.89, and 29.90):

Step	*D2D1D0*	*VTOP(V)*	*Comparator Output*
--	--	-2V	--
1	000	-2 + Vref/2 +0.3 = 0.8	0
2	010	-2 + Vref/4 + 0.3 = -0.45V	1
3	011	-2 + Vref/4 + Vref/8 + 0.3 = 0.175V	1

The key takeaway here is that with a 0.3V comparator offset, the comparator output changes at $V_{top} > 0.3V$ instead of GND. Therefore, even though in step 3 V_{TOP} is positive, the comparator output remains high because it is not > 0.3V. You can see that the comparator output is the same as shown in 29.33 where no offset was present.

29.36 Discuss the differences between Nyquist rate ADC's and oversampling ADCs.

Nyquist rate ADCs, as the name implies, sample the analog input signal at 2X the input bandwidth. Oversampling ADCs sample the input at a rate much faster than the Nyquist rate. The higher sampling frequency of the oversampling ADCs results in some distinct advantages over the Nyquist rate ADCs.

In general, the oversampling ADCs end up providing a simplified implementation. Figure 29.41 (page 1008) shown below shows the block diagram for the two ADCs.

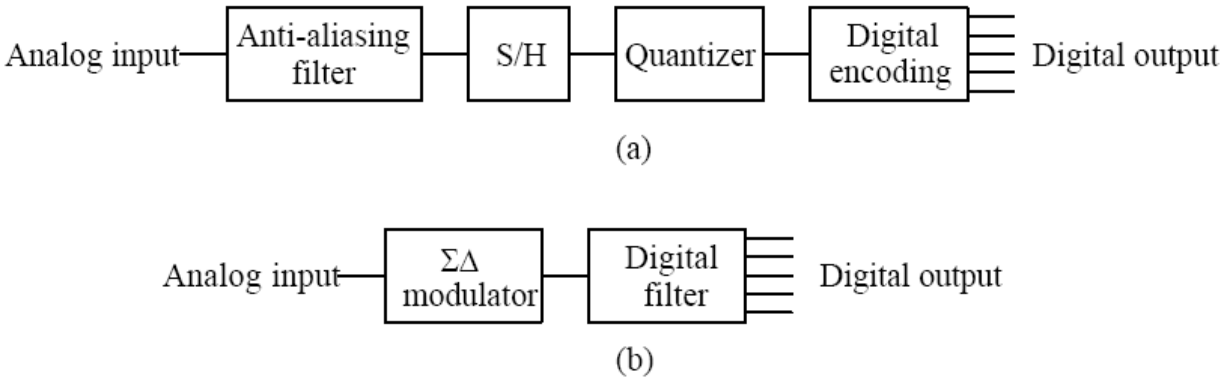


Figure 29.41 Typical block diagram for (a) Nyquist rate converters and (b) oversampling ADCs.

As can be seen in the figure, the oversampling ADC doesn't need a dedicated S/H or quantizer. The modulator takes care of the quantizing and the implementation usually includes switched-capacitor circuits, which eliminates the need for a S/H.

The oversampling ADC requires more sampling time and has a lower throughput than the Nyquist rate ADC. Because the sampling rate is much greater than the input bandwidth, the frequency spectra are spaced much farther apart and there is little or no aliasing. This results in a much simpler anti-aliasing filter if one is needed at all.

The one drawback of the oversampling ADC is the throughput. The oversampling ADC requires more sampling time have a lower throughput than the Nyquist rate ADCs.

Additional discussion is available in section 29.2.6.

29.37 Write a simple computer program or use a math program to perform the analysis shown in Ex. 29.16. Run the program for k = 200 clock cycles and show that the average value of $v_q(kT)$ converges to the correct answer. How many clock cycles will it take to obtain an average value if $v_q(kT)$ stays within 8-bit accuracy of the ideal value of 0.4V? 12-bit accuracy? 16-bit accuracy?

Ex. 29.16: Using a general first order ΣΔ modulator, assume that the input to the modulator $v_x(kT)$ is a positive DC voltage of 0.4 V. Show the values of each variable around the ΣΔ modulator loop and prove that the overall average output of the DAC approaches 0.4V after 10 cycles. Assume that the DAC output is at +/- 1 V, and that the integrator output has a unity gain with an initial output voltage of 0.1 V, and that the comparator output is either +/-1 V.

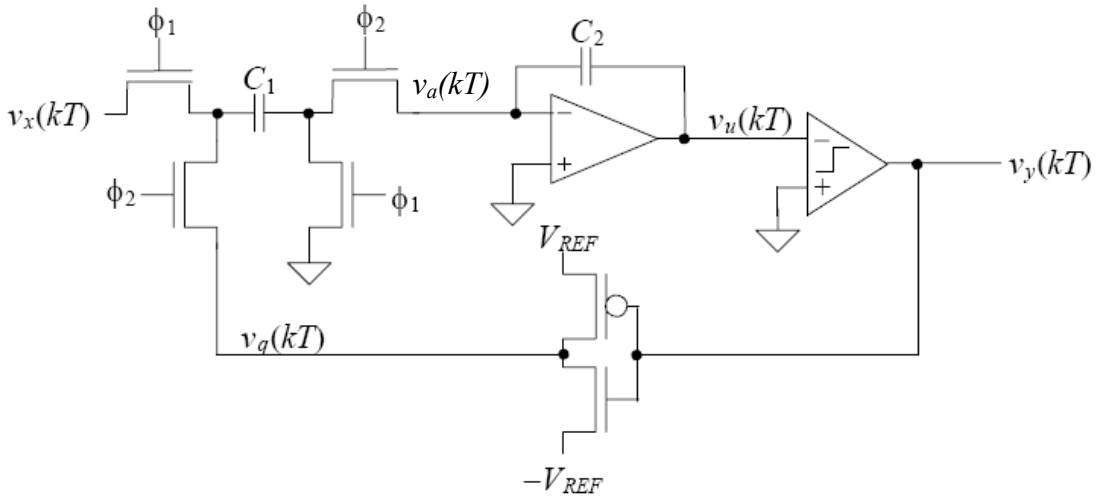


Figure 29.47 Implementation of a first-order sigma-delta modulator using a switched capacitor integrator.

Perl code:

```
#!/usr/bin/perl

# User changable parameters
$vref = 1.0;
$loops = 200;
$vx = 0.4; # DC input value

# Variables of interest
$k = 0; # iterator
$va = 0; # integrator input
$vu = 0; # integrator output
$va_last = 0; # previous integrator input
$vu_last = 0.1; # previous integrator output
$vq = 0; # feedback/output
$vq_sum = 0; # feedback/output sum

printf("k\t va\t vu\t vq\t Qe\tvq(avg)\tQe(avg)\n");
for ($k=0; $k<=$loops; $k++) {
        $vu = $vu_last + $va_last;
        if ($vu <= 0) {
                $vq = - $vref;
        } else {
                $vq = $vref;
        }
        $va = $vx - $vq;
        $vq_sum = $vq_sum + $vq;
        printf("%03d\t%6.2f\t%6.2f\t%6.2f\t%6.2f\t%7.3f\t%9.6f\n",
                $k, $va, $vu, $vq, $vq - $vu, $vq_sum/($k+1), ($vq_sum/($k+1))-$vx);
        $va_last = $va;
        $vu_last = $vu;

}
```

200 Loops:

k	va	vu	vq	Qe	vq(avg)	Qe(avg)
000	-0.60	0.10	1.00	0.90	1.000	0.600000
001	1.40	-0.50	-1.00	-0.50	0.000	-0.400000
002	-0.60	0.90	1.00	0.10	0.333	-0.066667
003	-0.60	0.30	1.00	0.70	0.500	0.100000
004	1.40	-0.30	-1.00	-0.70	0.200	-0.200000
005	-0.60	1.10	1.00	-0.10	0.333	-0.066667
006	-0.60	0.50	1.00	0.50	0.429	0.028571
007	1.40	-0.10	-1.00	-0.90	0.250	-0.150000
008	-0.60	1.30	1.00	-0.30	0.333	-0.066667
009	-0.60	0.70	1.00	0.30	0.400	0.000000
010	-0.60	0.10	1.00	0.90	0.455	0.054545
011	1.40	-0.50	-1.00	-0.50	0.333	-0.066667
012	-0.60	0.90	1.00	0.10	0.385	-0.015385
013	-0.60	0.30	1.00	0.70	0.429	0.028571
014	1.40	-0.30	-1.00	-0.70	0.333	-0.066667
015	-0.60	1.10	1.00	-0.10	0.375	-0.025000
.						
.						
185	-0.60	1.10	1.00	-0.10	0.398	-0.002151
186	-0.60	0.50	1.00	0.50	0.401	0.001070
187	1.40	-0.10	-1.00	-0.90	0.394	-0.006383
188	-0.60	1.30	1.00	-0.30	0.397	-0.003175
189	-0.60	0.70	1.00	0.30	0.400	0.000000
190	-0.60	0.10	1.00	0.90	0.403	0.003141
191	1.40	-0.50	-1.00	-0.50	0.396	-0.004167
192	-0.60	0.90	1.00	0.10	0.399	-0.001036
193	-0.60	0.30	1.00	0.70	0.402	0.002062
194	1.40	-0.30	-1.00	-0.70	0.395	-0.005128
195	-0.60	1.10	1.00	-0.10	0.398	-0.002041
196	-0.60	0.50	1.00	0.50	0.401	0.001015
197	1.40	-0.10	-1.00	-0.90	0.394	-0.006061
198	-0.60	1.30	1.00	-0.30	0.397	-0.003015
199	-0.60	0.70	1.00	0.30	0.400	0.000000
200	-0.60	0.10	1.00	0.90	0.403	0.002985

8-bit accuracy would require Qe(avg) < 1/2LSB or $0.5*V_{REF}/2^8$, or Qe(avg) < 1.95mV. by modifying the code above to only print out errors greater than this threshold, we can see that this requires >300 cycles.

(Ran 1000 times)

k	va	vu	vq	Qe	vq(avg)	Qe(avg)
200	-0.60	0.10	1.00	0.90	0.403	0.002985
203	-0.60	0.30	1.00	0.70	0.402	0.001961
210	-0.60	0.10	1.00	0.90	0.403	0.002844
220	-0.60	0.10	1.00	0.90	0.403	0.002715
230	-0.60	0.10	1.00	0.90	0.403	0.002597
240	-0.60	0.10	1.00	0.90	0.402	0.002490
250	-0.60	0.10	1.00	0.90	0.402	0.002390
260	-0.60	0.10	1.00	0.90	0.402	0.002299
270	-0.60	0.10	1.00	0.90	0.402	0.002214
280	-0.60	0.10	1.00	0.90	0.402	0.002135
290	-0.60	0.10	1.00	0.90	0.402	0.002062
300	-0.60	0.10	1.00	0.90	0.402	0.001993

12-bit accuracy would require Qe(avg) < 122uV, which requires >4910 cycles.

(Ran 10000 times)

k	va	vu	vq	Qe	vq(avg)	Qe(avg)
4770	-0.60	0.10	1.00	0.90	0.400	0.000126
4780	-0.60	0.10	1.00	0.90	0.400	0.000125
4790	-0.60	0.10	1.00	0.90	0.400	0.000125
4800	-0.60	0.10	1.00	0.90	0.400	0.000125
4810	-0.60	0.10	1.00	0.90	0.400	0.000125
4820	-0.60	0.10	1.00	0.90	0.400	0.000124
4830	-0.60	0.10	1.00	0.90	0.400	0.000124
4840	-0.60	0.10	1.00	0.90	0.400	0.000124
4850	-0.60	0.10	1.00	0.90	0.400	0.000124
4860	-0.60	0.10	1.00	0.90	0.400	0.000123
4870	-0.60	0.10	1.00	0.90	0.400	0.000123
4880	-0.60	0.10	1.00	0.90	0.400	0.000123
4890	-0.60	0.10	1.00	0.90	0.400	0.000123
4900	-0.60	0.10	1.00	0.90	0.400	0.000122
4910	-0.60	0.10	1.00	0.90	0.400	0.000122

16-bit accuracy would require Qe(avg) < 7.63uV, which requires >78630 cycles.

(Ran 100000 times)

k	va	vu	vq	Qe	vq(avg)	Qe(avg)
78530	-0.60	0.10	1.00	0.90	0.400	0.000007640
78540	-0.60	0.10	1.00	0.90	0.400	0.000007639
78550	-0.60	0.10	1.00	0.90	0.400	0.000007638
78560	-0.60	0.10	1.00	0.90	0.400	0.000007637
78570	-0.60	0.10	1.00	0.90	0.400	0.000007636
78580	-0.60	0.10	1.00	0.90	0.400	0.000007635
78590	-0.60	0.10	1.00	0.90	0.400	0.000007634
78600	-0.60	0.10	1.00	0.90	0.400	0.000007633
78610	-0.60	0.10	1.00	0.90	0.400	0.000007633
78620	-0.60	0.10	1.00	0.90	0.400	0.000007632
78630	-0.60	0.10	1.00	0.90	0.400	0.000007631

29.38 *Prove that the output of the second-order* $\Sigma\Delta$ *modulator shown in Fig. 29.49 is,*

$$y(kT) = x(kT - T) + Q_e(kT) - 2Q_e(kT - T) + Q_e(kT - 2T)$$

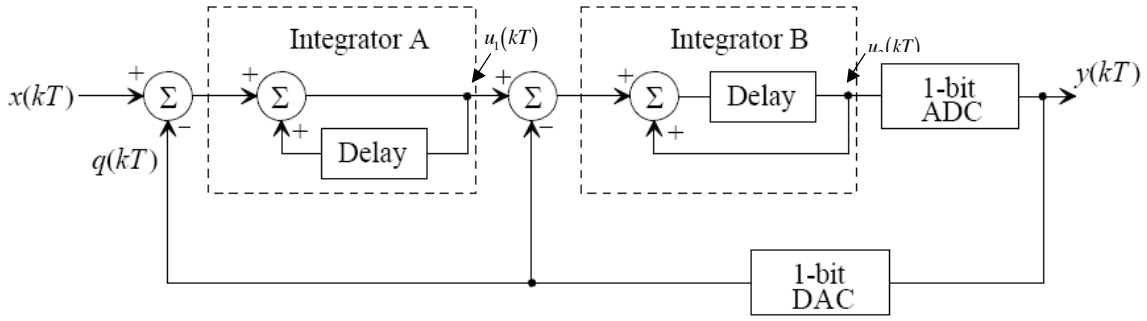


Figure 29.49 A second-order, sigma-delta modulator.

In order to prove that the above equation is that of the second-order sigma delta modulator we first start by determining the intermediate voltages shown above:

$$u_1(kT) = x(kT) - y(kT) + u_1(kT - T)$$

$$u_2(kT) = u_1(kT - T) - y(kT - T) + u_2(kT - T)$$

The equations above have taken $q(kT) = y(kT)$ for an ideal 1-bit DAC. We can plug $u_1(kT)$ into $u_2(kT)$ and get:

$$u_2(kT) = x(kT - T) - y(kT - T) + u_1(kT - 2T) - \underbrace{y(kT - T) + u_2(kT - T)}_{Q_e(kT - T)}$$

The quantization noise of the ADC can be written as:

$$Q_e(kT) = y(kT) - u_2(kT)$$

We can use the quantization noise equation above in two places. First we can rewrite $u_2(kT)$ with the quantization noise, and then we can plug $u_2(kT)$ into the quantization noise equation to solve for $y(kT)$.

$$u_2(kT) = x(kT - T) - y(kT - T) + u_1(kT - 2T) - Q_e(kT - T)$$

$$y(kT) = Q_e(kT) + u_2(kT)$$

$$y(kT) = Q_e(kT) + x(kT - T) - y(kT - T) + u_1(kT - 2T) - Q_e(kT - T)$$

The $u_1(kT - 2T)$ term is the only term that will not be in our final equation. In order to change this term we can use the $u_2(kT)$ equation:

$$u_2(kT) = u_1(kT - T) - y(kT - T) + u_2(kT - T)$$

Solving for $u_1(kT - T)$:

$$u_1(kT - T) = u_2(kT) + y(kT - T) - u_2(kT - T)$$

Advancing time by one clock cycle gives:

$$u_1(kT - 2T) = u_2(kT - T) + y(kT - 2T) - u_2(kT - 2T)$$

Plugging this into our $y(kT)$ equation gives:

$$y(kT) = Q_e(kT) + x(kT - T) - y(kT - T) + u_2(kT - T) + y(kT - 2T) - u_2(kT - 2T) - Q_e(kT - T)$$

Rearranging:

$$y(kT) = x(kT - T) + Q_e(kT) - \overbrace{y(kT - T) + u_2(kT - T)}^{Q_e(kT - T)} - Q_e(kT - T) + \overbrace{y(kT - 2T) - u_2(kT - 2T)}^{Q_e(kT - 2T)}$$

Using the quantization equation gives:

$$y(kT) = x(kT - T) + Q_e(kT) - 2Q_e(kT - T) + Q_e(kT + 2T)$$

29.39 Assume that a first order ΣΔ ADC used on a satellite in a low earth orbit experiences radiation in which an energetic particle causes a noise spike resulting in the comparator making the wrong decision on the 10^{th} clock period. Using the program written in Problem 29.37, determine the number of clock cycles required before the average value of $v_q(kT)$ is within 12-bit accuracy of the ideal value of 0.4 V. How many extra clock cycles were required for this case versus the ideal conversion used in Prob. 37?

For this problem, I wrote a Perl script to perform the analysis shown in Ex. 29.16. The script was used to solve problem 29.37 (referenced by this problem) as well so the comparison can be made between the ideal case (problem 29.37) and the case in this problem where the comparator makes the wrong decision on the 10^{th} clock period. To determine if the average value of $V_q(kT)$ stays within the chosen accuracy, I check that all of the values within a certain window size be within the chosen accuracy. I somewhat arbitrarily selected a window size of 5 values.

The results are summarized below and the Perl code follows. In short, the wrong decision on cycle 10 in this problem does not affect the point at which the average value of $V_q(kT)$ stays within the chosen accuracy for the chosen window size of 5. However, we can see that the clock cycle at which the average value of $V_q(kT)$ initially becomes exactly equal to the ideal value of 0.4 V changes from clock cycle 10 in the ideal case to clock cycle 20.

Running until Avg Vq(kT) is 12-bit accurate (between 0.3997558594 and 0.4002441406) for 5 cycles

k	Vq(kT)	Vu(kT)	Vq(kT)	Qe(kT)	Avg Vq(kT)
0	-0.600	0.100	1.000	0.900	1.0000000000
1	1.400	-0.500	-1.000	-0.500	0.0000000000
2	-0.600	0.900	1.000	0.100	0.3333333333
3	-0.600	0.300	1.000	0.700	0.5000000000
4	1.400	-0.300	-1.000	-0.700	0.2000000000
5	-0.600	1.100	1.000	-0.100	0.3333333333
6	-0.600	0.500	1.000	0.500	0.4285714286
7	1.400	-0.100	-1.000	-0.900	0.2500000000
8	-0.600	1.300	1.000	-0.300	0.3333333333
9	1.400	0.700	**-1.000**	-1.700	0.2000000000
10	-0.600	2.100	1.000	-1.100	0.2727272727
11	-0.600	1.500	1.000	-0.500	0.3333333333
12	-0.600	0.900	1.000	0.100	0.3846153846
13	-0.600	0.300	1.000	0.700	0.4285714286
14	1.400	-0.300	-1.000	-0.700	0.3333333333
15	-0.600	1.100	1.000	-0.100	0.3750000000
16	-0.600	0.500	1.000	0.500	0.4117647059
17	1.400	-0.100	-1.000	-0.900	0.3333333333
18	-0.600	1.300	1.000	-0.300	0.3684210526
19	-0.600	0.700	1.000	0.300	**0.4000000000**

P29.39: Comparator makes wrong decision on cycle 10

Initially converges to 0.4 V at cycle 20.

Running until Avg Vq(kT) is 12-bit accurate (between 0.3997558594 and 0.4002441406) for 5 cycles

k	Vq(kT)	Vu(kT)	Vq(kT)	Qe(kT)	Avg Vq(kT)
0	-0.600	0.100	1.000	0.900	1.0000000000
1	1.400	-0.500	-1.000	-0.500	0.0000000000
2	-0.600	0.900	1.000	0.100	0.3333333333
3	-0.600	0.300	1.000	0.700	0.5000000000
4	1.400	-0.300	-1.000	-0.700	0.2000000000
5	-0.600	1.100	1.000	-0.100	0.3333333333
6	-0.600	0.500	1.000	0.500	0.4285714286
7	1.400	-0.100	-1.000	-0.900	0.2500000000
8	-0.600	1.300	1.000	-0.300	0.3333333333
9	-0.600	0.700	1.000	0.300	**0.4000000000**

Ideal Case (P29.37)

Initially converges to 0.4 V at cycle 10

Overall, the comparator making a wrong decision on cycle 10 does not affect when the average value of $V_q(kT)$ finally reaches and stays within the 8-, 12-, or 16-bit accuracy as shown in the table below.

	Accuracy		
	8-bit	12-bit	16-bit
Lower Limit (V)	0.3960937500	0.3997558594	0.3999847412
Upper Limit (V)	0.4039062500	0.4002441406	0.4000152588
# Clocks required to reach and stay within limits for 5 cycles			
P29.37 (Ideal)	213	3283	52433
P29.39	213	3283	52433

Vref = 1V, Vin = 0.4V DC

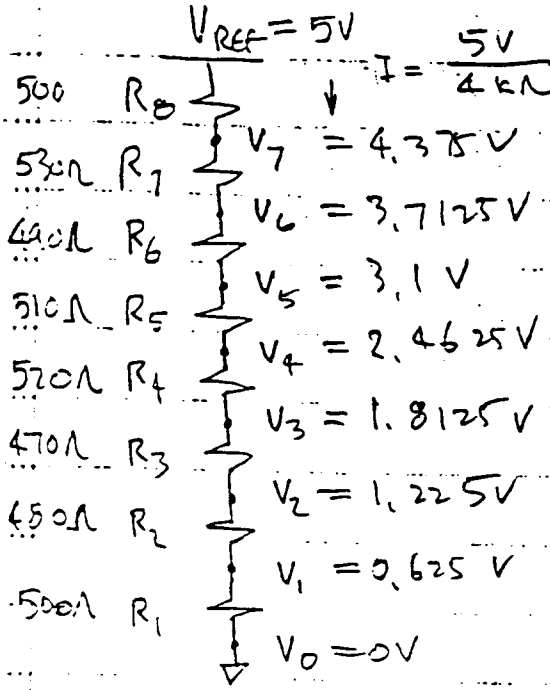
Perl Code:

```
# P29.39 - N-bit accurate w/ error on 10th cycle

# Get input argument
if(exists($ARGV[0])) {
   $N = $ARGV[0];    # Number of bits of accuracy
}
else {
   die "ERROR: Must supply input argument (N). For example: $0 8\n";
}

$output_file = sprintf("P29.39_%d_bit_sim_output.txt", $N);

$Vref = 1.0; # Vref
$Vx = 0.4;   # Input voltage is DC 0.4V

$max_delta = $Vref / (2 ** $N);   # Vref/(2^N) = 1 LSB
$window = 5;                      # Number of cycles for which the Average Vq stays within Vx +/-
max_delta

@Va = ();
@Vu = ();
@Vq = ();
@Qe = ();
@Avg_Vq = ();

$Vu[0] = 0.1; # Initial condition. Integrator output = 0.1V.

$sum = 0;
$k = 0;
$converged = 0;
while(!$converged)
{
   if($k > 0) {
      $Vu[$k] = $Vu[$k-1] + $Va[$k-1]; # Eq (29.102)
   }
   if($Vu[$k] > 0) {
      $Vq[$k] = $Vref;
   }
   else {
      $Vq[$k] = -$Vref;
   }

   # Problem 29.39: The comparator makes a wrong decision on the 10th cycle
   if($k == 9) {
      $Vq[$k] = -$Vq[$k];  # Invert the decision made on the 10th clock cycle
   }

   $Va[$k] = $Vx - $Vq[$k];      # Eq (29.103)
```

```
   $Qe[$k] = $Vq[$k] - $Vu[$k];  # Eq (29.104)

   # Calculate Average Vq
   $sum += $Vq[$k];
   $Avg_Vq[$k] = $sum / ($k+1);

   # Check to see if we have converged to Vx +/- max_delta for the given window size
   if(($k+1) >= $window) {
      $converged = 1; # Start off optimistic
      for($i=0; $i < $window; $i++) {
         if(($Avg_Vq[$k-$i] < ($Vx - $max_delta)) || ($Avg_Vq[$k-$i] > ($Vx + $max_delta))) {
            $converged = 0; # Avg Vq is outside of Vx +/- max_delta, so keep going
         }
      }
   }

   $k++;
}

$num_clocks = $k;

# Print results (to screen and output file)
open(OUTPUT, ">$output_file");
printf(       "Running until Avg Vq(kT) is %d-bit accurate (between %.10f and %.10f) for %d
cycles\n", $N, ($Vx - $max_delta), ($Vx + $max_delta), $window);
printf(OUTPUT "Running until Avg Vq(kT) is %d-bit accurate (between %.10f and %.10f) for %d
cycles\n", $N, ($Vx - $max_delta), ($Vx + $max_delta), $window);
printf(       "%4s %10s %10s %10s %10s %15s\n", "k", "Vq(kT)", "Vu(kT)", "Vq(kT)", "Qe(kT)", "Avg
Vq(kT)");
printf(OUTPUT "%4s %10s %10s %10s %10s %15s\n", "k", "Vq(kT)", "Vu(kT)", "Vq(kT)", "Qe(kT)", "Avg
Vq(kT)");
for($k=0; $k < $num_clocks; $k++)
{
   printf(       "%4d %10.3f %10.3f %10.3f %10.3f %15.10f\n", $k, $Va[$k], $Vu[$k], $Vq[$k],
$Qe[$k], $Avg_Vq[$k]);
   printf(OUTPUT "%4d %10.3f %10.3f %10.3f %10.3f %15.10f\n", $k, $Va[$k], $Vu[$k], $Vq[$k],
$Qe[$k], $Avg_Vq[$k]);
}
close(OUTPUT);

exit;
```

Chapter 29

29.1



Digital Input	Step Height (V) Actual	Step Height (V) Ideal	DNL(V) (LSB)		Voltage Output (V) Actual	Voltage Output (V) Ideal	INL(V)
000					0	0	0
001	0.625	0.625	0	0	0.625	0.625	0
010	0.595	"	-0.03	-0.040	1.225	1.25	-0.025
011	0.5925	"	-0.0325	-0.052	1.8125	1.875	-0.0625
100	0.65	"	0.025	0.04	2.4625	2.5	-0.0375
101	0.6375	"	0.0125	0.02	3.1	3.125	-0.025
110	0.6125	"	-0.0125	-0.02	3.7125	3.75	-0.0375
111	0.6625	"	0.0375	0.06	4.375	4.375	0

$$|DNL|_{MAX} = \boxed{0.0375\,V = 0.06\,LSB}$$

$$|INL|_{max} = \boxed{0.0625\,V = 0.1\,LSB}$$

29.2

$$|DNL|_{max} = \left| \frac{V_{REF}}{2^N} \cdot \left(\frac{\Delta R}{R}\right)_{max} \right| \quad (V)$$

$$= \left| \left(\frac{\Delta R}{R}\right)_{max} \right| \quad (LSB)$$

$$= \boxed{0.01\ LSB}$$

$$|INL|_{max} = \left| \frac{V_{REF}}{2^N} \cdot 2^{N-1} \left(\frac{\Delta R}{R}\right)_{max} \right| \quad (V)$$

$$= \left| 2^{N-1} \left(\frac{\Delta R}{R}\right)_{max} \right| \quad LSB$$

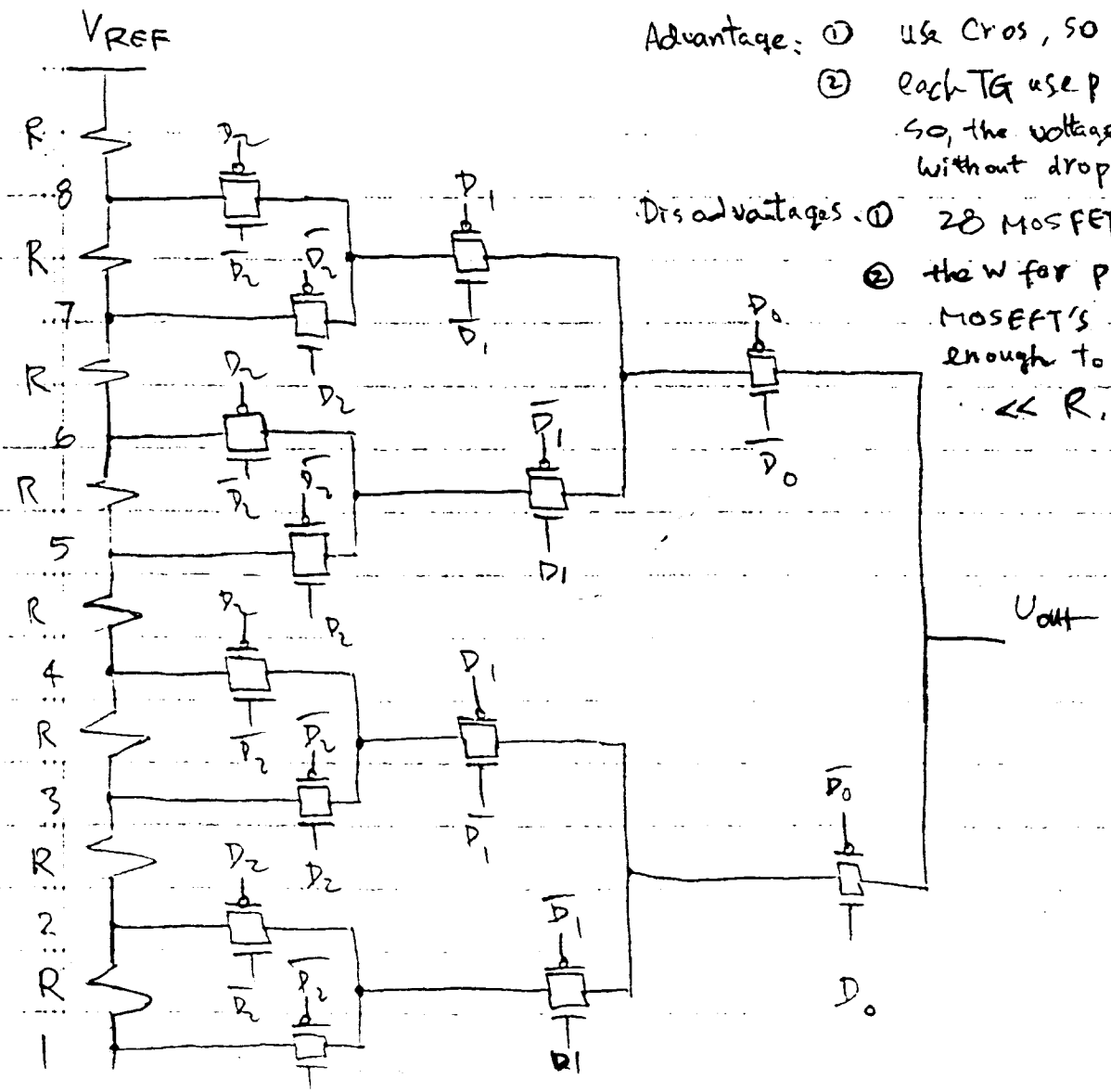
$$= \boxed{1.28\ LSB}$$

The effective resolution is $\boxed{8 - 2 = 6}$

29.3

Digital Input Code

	Resistor String DAC Figure 29.2(a)								Resistor String DAC Figure 29.2(b)		
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_2	D_1	D_0
0								1	0	0	0
1							1		0	0	1
2						1			0	1	0
3					1				0	1	1
4				1					1	0	0
5			1						1	0	1
6		1							1	1	0
7	1								1	1	1



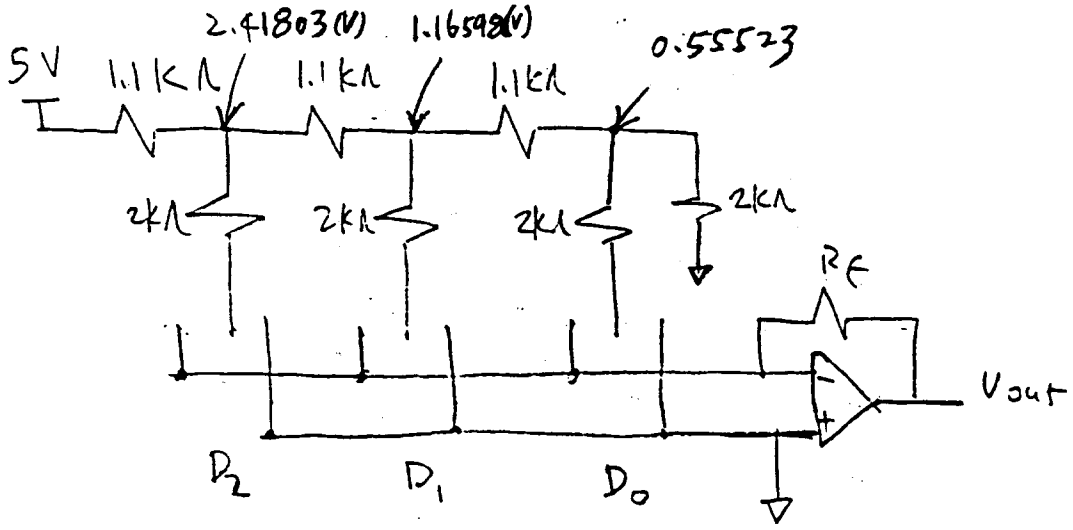
Advantage: ① use Cmos, so easy to fabricate

② each TG use p & n channel types so, the voltage can transfer without dropping

Disadvantages: ① 28 MOSFET's are used

② the W for p & n channel MOSFET's should be big enough to let the TG Resi $\ll R$.

29.4

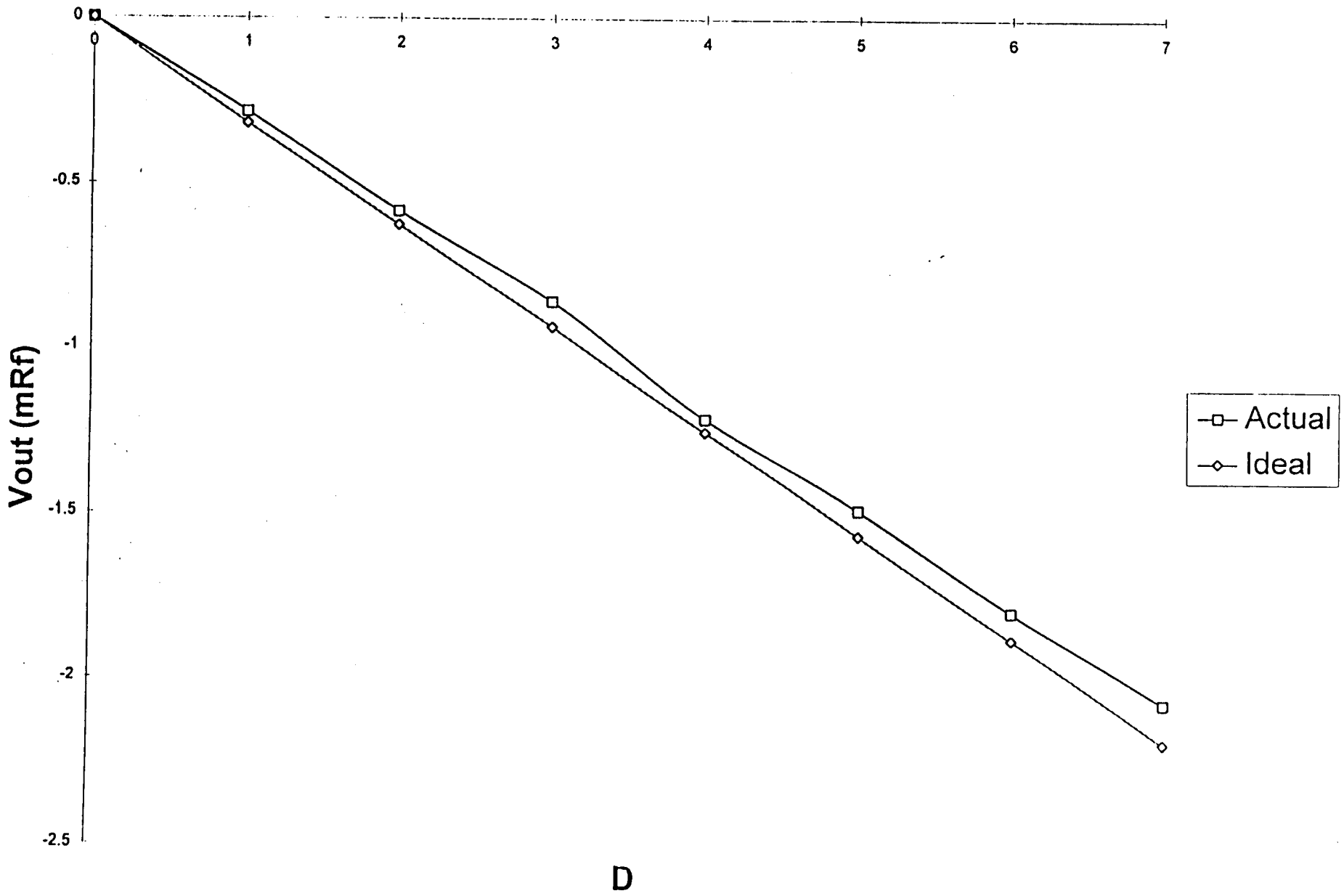


$$V_{out} = -I_{TOT} \cdot R_F$$

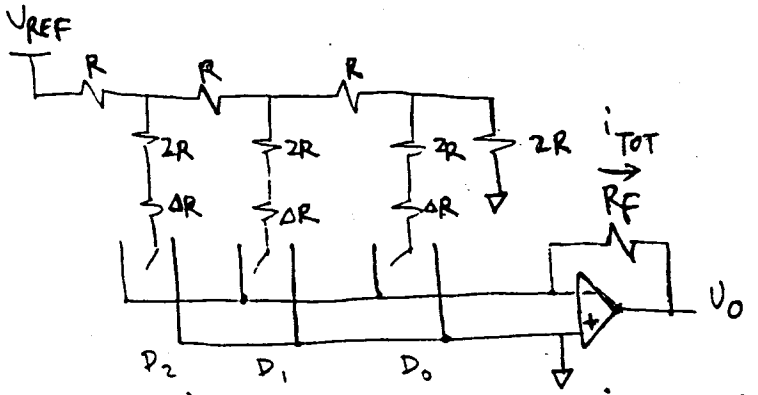
Digital Input D_2 D_1 D_0	Voltage Output (V) Actual	Ideal	INL (LSB)	Step Height (V) Actual	Ideal	DN
0 0 0	0	0	0			
0 0 1	$-0.2776\,m R_F$	$-0.3125\,m R_F$	-0.11	$-0.2776\,m R_F$	$-0.3125\,m R_F$	-0.11
0 1 0	$-0.5830\,m R_F$	$-0.625\,m R_F$	-0.13	$-0.3054\,m R_F$	"	-0.0
0 1 1	$-0.8608\,m R_F$	$-0.9375\,m R_F$	-0.25	$-0.2778\,m R_F$	"	-0.11
1 0 0	$-1.2090\,m R_F$	$-1.25\,m R_F$	-0.13	$-0.3482\,m R_F$	"	0.11
1 0 1	$-1.4866\,m R_F$	$-1.5625\,m R_F$	-0.24	$-0.2776\,m R_F$	"	-0.11
1 1 0	$-1.7920\,m R_F$	$-1.875\,m R_F$	-0.27	$-0.3054\,m R_F$	"	-0.0
1 1 1	$-2.0696\,m R_F$	$-2.1875\,m R_F$	-0.38	$-0.2776\,m R_F$	"	-0.11

$$\frac{\text{Actual} - \text{Ideal}}{-0.3125\,m R_F} \uparrow -0.625\,\frac{R_F}{2K}$$

$$\frac{\text{Actual} - \text{Ideal}}{-0.3125\,m R_F}$$

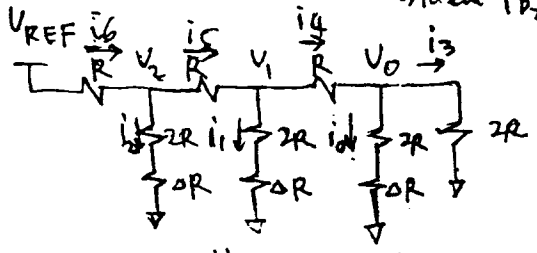

0
0
1
2
3
4
5
6
7
-0.5
-1
-1.5
-2
-2.5
Vout (mRf)
Actual
Ideal
D

Prob.29.5



$$INL = \frac{V_{0,actual} - V_{0,ideal}}{V_{0,ideal}\big|_{D_2D_1D_0=001}} = \frac{(-i_{TOT,actual}) - (-i_{TOT,ideal})}{-i_{TOT,ideal}\big|_{D_2D_1D_0=001}} \quad (LSB)$$

$$DNL = \frac{(V_{0,actual_k} - V_{0,actual_{k-1}}) - (V_{0,ideal_k} - V_{0,ideal_{k-1}})}{V_{0,ideal}\big|_{D_2D_1D_0=001}} = \frac{(-i_{TOT,actual_k} + i_{TOT,actual_{k-1}}) - i_{TOT,ideal}\big|_{D_2D_1D_0=001}}{-i_{TOT,ideal}\big|_{D_2D_1D_0=001}} \quad (LSB)$$



$$i_6 = i_2 + i_5 : \quad \frac{V_{REF} - V_2}{R} = \frac{V_2 - V_1}{R} + \frac{V_2}{2R+\Delta R} \rightarrow \left(2 + \frac{1}{2+\Delta R/R}\right) V_2 = V_1 + V_{REF} \quad (1)$$

$$i_5 = i_1 + i_4 : \quad \frac{V_2 - V_1}{R} = \frac{V_1 - V_0}{R} + \frac{V_1}{2R+\Delta R} \rightarrow \left(2 + \frac{1}{2+\Delta R/R}\right) V_1 = V_0 + V_2 \quad (2)$$

$$i_4 = i_0 + i_3 : \quad \frac{V_1 - V_0}{R} = \frac{V_0}{2R} + \frac{V_0}{2R+\Delta R} \rightarrow \left(1.5 + \frac{1}{2+\Delta R/R}\right) V_0 = V_1 \quad (3)$$

With MathCAD, increase ΔR to make INL or DNL ≐ 0.5 LSB. get.

when $\Delta R = 305\,\Omega$ $\quad |INL|_{max} = |INL_7| = 0.496$ LSB.
$|DNL|_{max} = |DNL_4| = 0.243$ LSB

So, $\boxed{\Delta R \doteq 300\,\Omega}$ is the upper limit to keep the DAC have 3 bit resolution

Vref := 5 DR := .305 R := 1

$$DRR := \frac{DR}{R}$$

$$alfa := 1.5 + \frac{1}{2 + DRR}$$

$$V0 := \frac{Vref}{((0.5 + alfa)\cdot((0.5 + alfa)\cdot alfa - 1) - alfa)} \qquad V0 = 0.705$$

$$V1 := alfa \cdot V0 \qquad V1 = 1.364$$

$D2 := 0 \quad D1 := 0 \quad D0 := 0$

$$iTAC0 := D0 \cdot \frac{V0}{2 \cdot R + DR} + D1 \cdot \frac{V1}{2 \cdot R + DR} + D2 \cdot \frac{V2}{2 \cdot R + DR} \qquad iTAC0 = 0$$

$iTID0 := 0$

$D2 := 0 \quad D1 := 0 \quad D0 := 1$

$$iTAC1 := D0 \cdot \frac{V0}{2 \cdot R + DR} + D1 \cdot \frac{V1}{2 \cdot R + DR} + D2 \cdot \frac{V2}{2 \cdot R + DR} \qquad iTAC1 = 0.306$$

$iTID1 := .3125 \quad iLSB := iTID1$

$D2 := 0 \quad D1 := 1 \quad D0 := 0$

$$iTAC2 := D0 \cdot \frac{V0}{2 \cdot R + DR} + D1 \cdot \frac{V1}{2 \cdot R + DR} + D2 \cdot \frac{V2}{2 \cdot R + DR} \qquad iTAC2 = 0.592$$

$iTID2 := .625$

$D2 := 0 \quad D1 := 1 \quad D0 := 1$

$$iTAC3 := D0 \cdot \frac{V0}{2 \cdot R + DR} + D1 \cdot \frac{V1}{2 \cdot R + DR} + D2 \cdot \frac{V2}{2 \cdot R + DR} \qquad iTAC3 = 0.898$$

$iTID3 := .9375$

$D2 := 1 \quad D1 := 0 \quad D0 := 0$

$$iTAC4 := D0 \cdot \frac{V0}{2 \cdot R + DR} + D1 \cdot \frac{V1}{2 \cdot R + DR} + D2 \cdot \frac{V2}{2 \cdot R + DR} \qquad iTAC4 = 1.134$$

$iTID4 := 1.25$

$D2 := 1 \quad D1 := 0 \quad D0 := 1$

$$iTAC5 := D0 \cdot \frac{V0}{2 \cdot R + DR} + D1 \cdot \frac{V1}{2 \cdot R + DR} + D2 \cdot \frac{V2}{2 \cdot R + DR} \qquad iTAC5 = 1.441$$

$iTID5 := 1.5625$

$D2 := 1 \quad D1 := 1 \quad D0 := 0$

$$iTAC6 := D0 \cdot \frac{V0}{2 \cdot R + DR} + D1 \cdot \frac{V1}{2 \cdot R + DR} + D2 \cdot \frac{V2}{2 \cdot R + DR} \qquad iTAC6 = 1.726$$

$iTID6 := 1.875$

$D2 := 1 \quad D1 := 1 \quad D0 := 1$

$$iTAC7 := D0 \cdot \frac{V0}{2 \cdot R + DR} + D1 \cdot \frac{V1}{2 \cdot R + DR} + D2 \cdot \frac{V2}{2 \cdot R + DR} \qquad iTAC7 = 2.032$$

INL and DNL

$$INL0 := \frac{iTAC0 - iTID0}{iLSB} \qquad INL0 = 0$$

$$INL1 := \frac{iTAC1 - iTID1}{iLSB} \qquad INL1 = -0.021$$

$$INL2 := \frac{iTAC2 - iTID2}{iLSB} \qquad INL2 = -0.106$$

$$INL3 := \frac{iTAC3 - iTID3}{iLSB} \qquad INL3 = -0.127$$

(LSB)

$$INL4 := \frac{iTAC4 - iTID4}{iLSB} \qquad INL4 = -0.37$$

$$INL5 := \frac{iTAC5 - iTID5}{iLSB} \qquad INL5 = -0.39$$

$$INL6 := \frac{iTAC6 - iTID6}{iLSB} \qquad INL6 = -0.476$$

$$INL7 := \frac{iTAC7 - iTID7}{iLSB} \qquad INL7 = -0.496$$

$$DNL1 := \frac{iTAC1 - iTAC0 - iLSB}{iLSB} \qquad DNL1 = -0.021$$

$$DNL2 := \frac{iTAC2 - iTAC1 - iLSB}{iLSB} \qquad DNL2 = -0.085$$

$$DNL3 := \frac{iTAC3 - iTAC2 - iLSB}{iLSB} \qquad DNL3 = -0.021$$

$$DNL4 := \frac{iTAC4 - iTAC3 - iLSB}{iLSB} \qquad DNL4 = -0.243$$

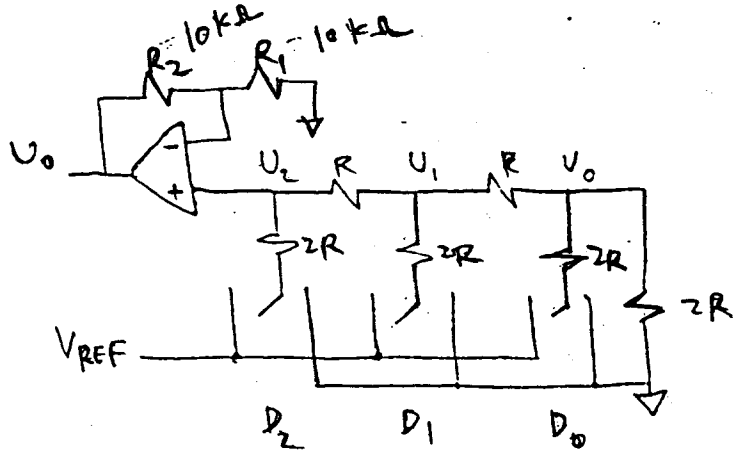
(LSB)

$$DNL5 := \frac{iTAC5 - iTAC4 - iLSB}{iLSB} \qquad DNL5 = -0.021$$

$$DNL6 := \frac{iTAC6 - iTAC5 - iLSB}{iLSB} \qquad DNL6 = -0.085$$

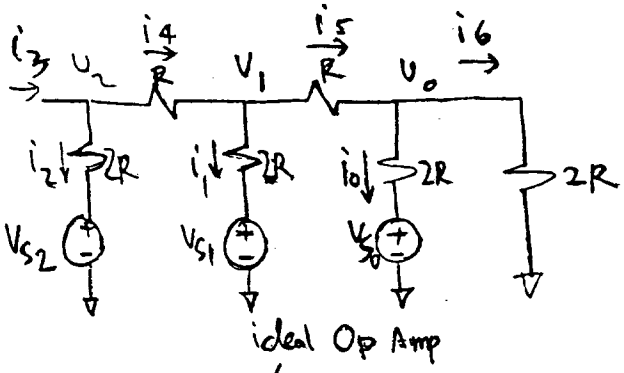
$$DNL7 := \frac{iTAC7 - iTAC6 - iLSB}{iLSB} \qquad DNL7 = -0.021$$

29.6



R=1kΩ

$$U_0 = \left(1 + \frac{R_2}{R_1}\right) U_2 = R U_2$$



$$i_3 = i_2 + i_4 : \quad 0 = \frac{U_2 - U_1}{R} + \frac{U_2 - U_{S2}}{2R} \rightarrow 1.5\,U_2 = U_1 + 0.5\,U_{S2}$$

$$i_4 = i_1 + i_5 : \quad \frac{U_2 - U_1}{R} = \frac{U_1 - U_0}{R} + \frac{U_1 - U_{S1}}{2R} \rightarrow U_2 = 2.5\,U_1 - U_0 - 0.5$$

$$i_5 = i_0 + i_6 : \quad \frac{U_1 - U_0}{R} = \frac{U_0}{2R} + \frac{U_0 - U_{S0}}{2R} \rightarrow U_1 = 2U_0 - 0.5\,U_{S0}$$

$$\Rightarrow \begin{cases} U_0 = \frac{1}{4}(0.5\,U_{S2} + 0.75\,U_{S1} + 1.375\,U_{S0}) \\ U_1 = 2U_0 - 0.5\,U_{S0} \\ U_2 = 2.5\,U_1 - U_0 - 0.5\,U_{S1} \end{cases}$$

$D_2D_1D_0$	U_{S2}	U_{S1}	U_{S0} (V)	U_0	U_1	U_2 (V)	$U_{out} = 2U_2$ (V)
000	0	0	0	0	0	0	0
001	0	0	5	1.719	0.938	0.625	1.25
010	0	5	0	0.938	1.875	1.25	2.5
011	0	5	5	2.656	2.813	1.85 5	3.75
100	5	0	0	0.625	1.25	2.5	5
101	5	0	5	2.342	2.188	3.125	6.25
110	5	5	0	1.563	3.125	3.75	7.5

Prob.29.6

D=000

$VS2 := 0 \quad VS1 := 0 \quad VS0 := 0$

$V0 := \frac{1}{4}\cdot(0.5\cdot VS2 + 0.75\cdot VS1 + 1.375\cdot VS0)$ $V0 = 0$

$V1 := 2\cdot V0 - 0.5\cdot VS0$ $V1 = 0$

$V2 := 2.5\cdot V1 - V0 - .5\cdot VS1$ $V2 = 0$

D=001

$VS2 := 0 \quad VS1 := 0 \quad VS0 := 5$

$V0 := \frac{1}{4}\cdot(0.5\cdot VS2 + 0.75\cdot VS1 + 1.375\cdot VS0)$ $V0 = 1.719$

$V1 := 2\cdot V0 - 0.5\cdot VS0$ $V1 = 0.938$

$V2 := 2.5\cdot V1 - V0 - .5\cdot VS1$ $V2 = 0.625$

D=010

$VS2 := 0 \quad VS1 := 5 \quad VS0 := 0$

$V0 := \frac{1}{4}\cdot(0.5\cdot VS2 + 0.75\cdot VS1 + 1.375\cdot VS0)$ $V0 = 0.938$

$V1 := 2\cdot V0 - 0.5\cdot VS0$ $V1 = 1.875$

$V2 := 2.5\cdot V1 - V0 - .5\cdot VS1$ $V2 = 1.25$

D=011

$VS2 := 0 \quad VS1 := 5 \quad VS0 := 5$

$V0 := \frac{1}{4}\cdot(0.5\cdot VS2 + 0.75\cdot VS1 + 1.375\cdot VS0)$ $V0 = 2.656$

$V1 := 2\cdot V0 - 0.5\cdot VS0$ $V1 = 2.813$

$V2 := 2.5\cdot V1 - V0 - .5\cdot VS1$ $V2 = 1.875$

D=100

$VS2 := 5 \quad VS1 := 0 \quad VS0 := 0$

$V0 := \frac{1}{4}\cdot(0.5\cdot VS2 + 0.75\cdot VS1 + 1.375\cdot VS0)$ $V0 = 0.625$

$V1 := 2\cdot V0 - 0.5\cdot VS0$ $V1 = 1.25$

D=101

VS2 := 5 VS1 := 0 VS0 := 5

$V0 := \frac{1}{4} \cdot (0.5 \cdot VS2 + 0.75 \cdot VS1 + 1.375 \cdot VS0)$ V0 = 2.344

V1 := 2·V0 – 0.5·VS0 V1 = 2.188

V2 := 2.5·V1 – V0 – .5·VS1 V2 = 3.125

D=110

VS2 := 5 VS1 := 5 VS0 := 0

$V0 := \frac{1}{4} \cdot (0.5 \cdot VS2 + 0.75 \cdot VS1 + 1.375 \cdot VS0)$ V0 = 1.563

V1 := 2·V0 – 0.5·VS0 V1 = 3.125

V2 := 2.5·V1 – V0 – .5·VS1 V2 = 3.75

D=111

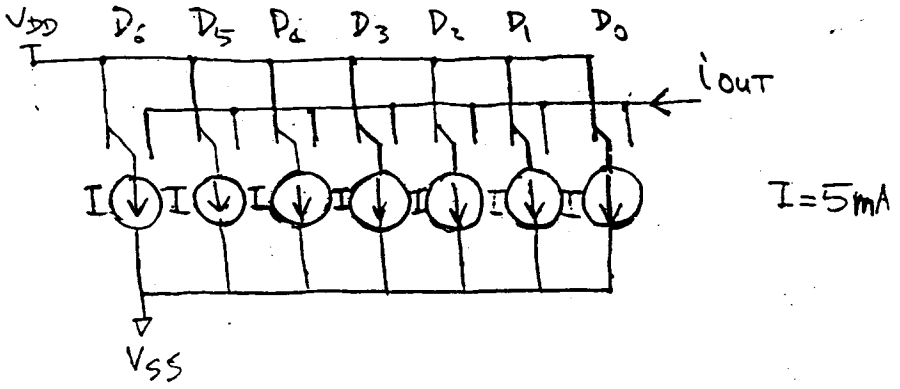
VS2 := 5 VS1 := 5 VS0 := 5

$V0 := \frac{1}{4} \cdot (0.5 \cdot VS2 + 0.75 \cdot VS1 + 1.375 \cdot VS0)$ V0 = 3.281

V1 := 2·V0 – 0.5·VS0 V1 = 4.063

V2 := 2.5·V1 – V0 – .5·VS1 V2 = 4.375

29.7



	D_6	D_5	D_4	D_3	D_2	D_1	D_0	i_{out}
000	0	0	0	0	0	0	0	0
001	0	0	0	0	0	0	1	I
010	0	0	0	0	0	1	1	2I
011	0	0	0	0	1	1	1	3I
100	0	0	0	1	1	1	1	4I
101	0	0	1	1	1	1	1	5I
110	0	1	1	1	1	1	1	6I
111	1	1	1	1	1	1	1	7I

29.8 For nonbinary weight_current steering DAC

$$|DNL|_{max} = |\Delta I_{max}|(A) = |\Delta I_{max}|/I = 0.05\%(LSB) \text{ in our case}$$

$$|INL|_{max} = 2^{N-1}|\Delta I|_{max}(A) = 2^{N-1}|\Delta I|_{max}/I = 2^{N-1}\cdot 0.05\% \text{ (LS}$$

in our case

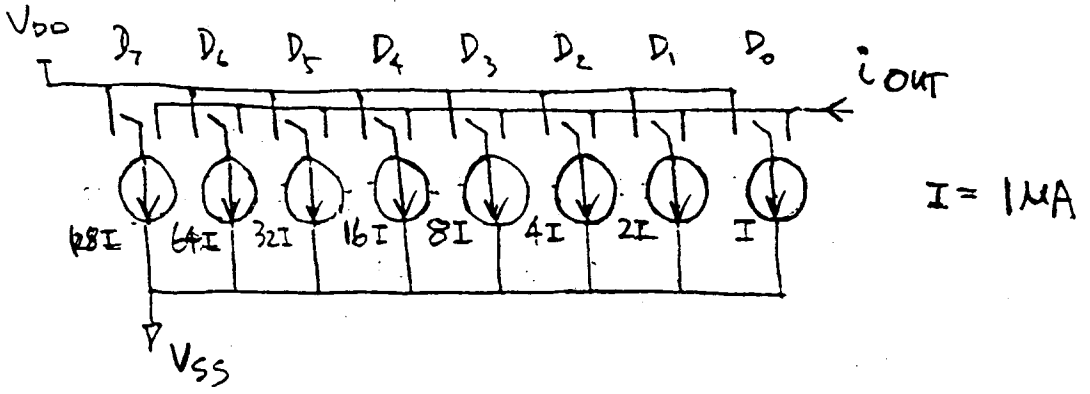
$$N = \frac{\lg |INL|_{max} - \lg(0.05\%)}{\lg 2} + 1$$

Let $|INL|_{max} = 0.5$ LSB

$$N = \frac{\lg(0.5) - \lg(0.05\%)}{\lg 2} + 1 = 10.97$$

the maximum resolution the DAC can attain using the process is 10 bit

29.9



$I = 1\,MA$

The range of values that the current source corresponding to the MS can have :

① $|INL|_{max} \le \frac{1}{2} LSB$

$$|\Delta I|_{max,\,INL} = \frac{|INL|_{max}}{2^{8-1}} = \frac{0.5}{2^7} = 3.906 \times 10^{-3}$$

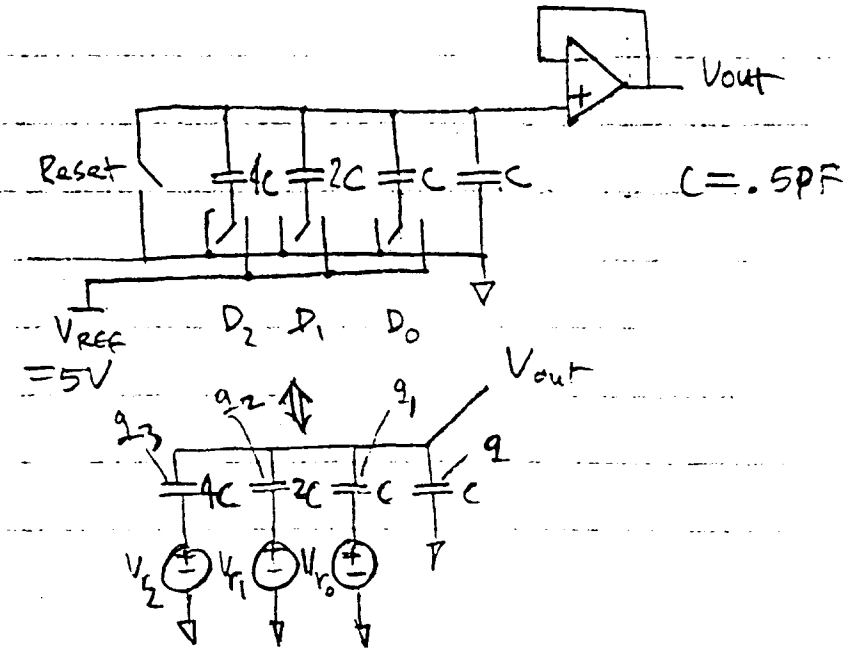
$$I_{MSB} = 128 \pm 128 \cdot |\Delta I|_{max,\,INL} = \boxed{128 \pm 0.5\ mA} \quad (= 3.906\,(mA))$$

② $|DNL|_{max} \le \frac{1}{2} LSB$

$$|\Delta I|_{max,\,DNL} = \frac{|DNL|_{max}}{2^{8}-1} = \frac{0.5}{2^8-1} = 1.961 \times 10^{-3}\ LSB \quad (= 1.961\,(mA))$$

$$I_{MSB} = 128 \pm 128\,|\Delta I|_{max,\,DNL} = \boxed{128 \pm 0.25\ mA}$$

29.10



C = .5PF

$$q_0 + q_1 + q_2 + q = 0$$

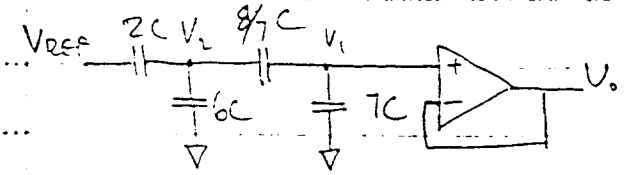
$$(1+2+4+1)\,V_{out} = V_{r0} + 2V_{r1} + 4V_{r2}$$

$$\boxed{V_{out} = \frac{1}{8}V_{r0} + \frac{1}{4}V_{r1} - \frac{1}{2}V_{r2}}$$

$D_2D_1D_0$	V_{r2}(V)	V_{r1}(V)	V_{r0}(V)	V_{out}(V)
0 0 0	0	0	0	0
0 0 1	0	0	5	0.625
0 1 0	0	5	0	1.250
0 1 1	0	5	5	1.875
1 0 0	5	0	0	2.500
1 0 1	5	0	5	3.125
1 1 0	5	5	0	3.750
1 1 1	5	5	5	4.375

29.11 $D = 000010$

equivalent CKT:

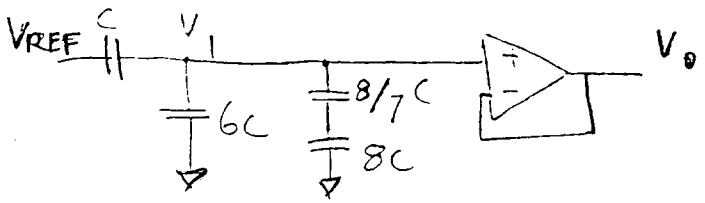


$$V_2 = \frac{2}{\left(6 + \frac{8/7 \cdot 7}{8/7 + 7}\right) + 2} V_{REF} = \frac{2}{8 + 56/57}$$

$$V_o = V_1 = \frac{8/7}{8/7 + 7} \cdot V_2 = \frac{8}{57} \cdot \frac{2}{8 + 56/57} V_{REF} = \boxed{\frac{V_{REF}}{32}}$$

$D = 001000$

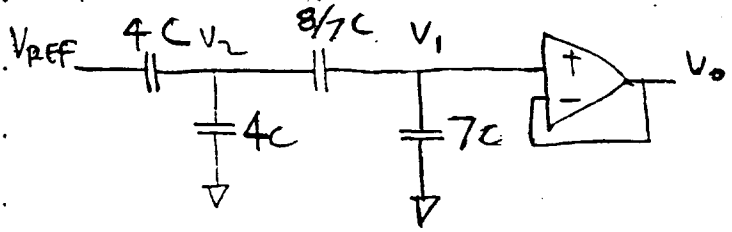
equivalent CKT



$$V_o = V_1 = \frac{1}{\frac{8/7 \cdot 8}{8/7 + 8} + 6 + 1} = \boxed{\frac{V_{REF}}{8}}$$

D = 000100

equivalent CKT

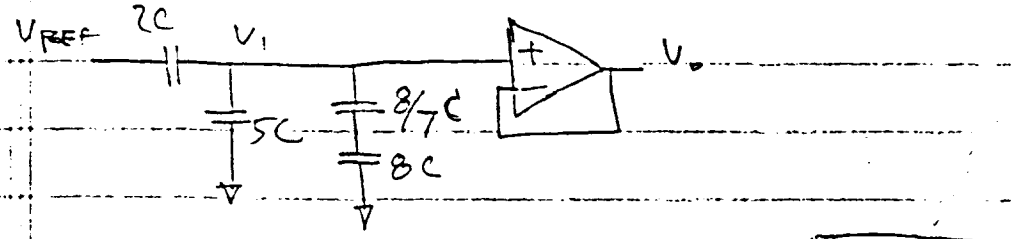


$$V_2 = \frac{4}{\left(\frac{8/7 \cdot 7}{8/7 + 7} + 4\right) + 4} V_{REF} = \frac{4}{8 + 56/57} V_{REF}$$

$$V_o = V_1 = \frac{8/7}{8/7 + 7} \cdot V_2 = \frac{8}{57} \cdot \frac{4}{8 + 56/57} V_{REF} = \boxed{\frac{V_{REF}}{16}}$$

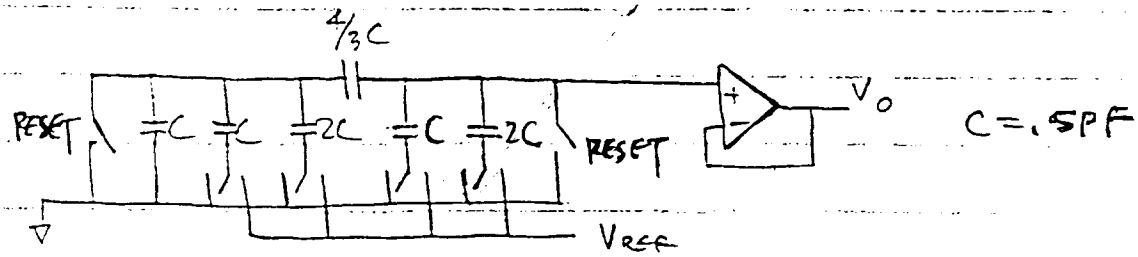
D = 0100000

equivalent CKT



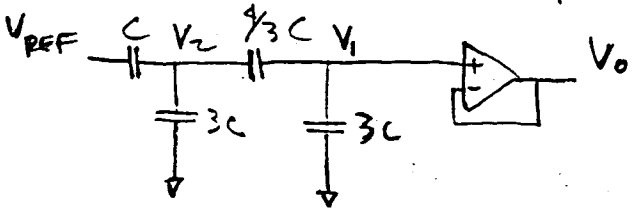
$$V_o = V_1 = \frac{2}{5 + \frac{8/7 \cdot 8}{8/7 + 8} + 2} V_{REF} = \boxed{\frac{1}{4} V_{REF}}$$

29.12



C = .5PF

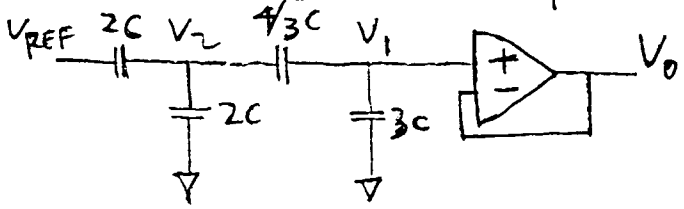
D = 0001 equivalent ckt



$$V_2 = \frac{1}{\left(\frac{4/3 \cdot 3}{4/3+3} + 3\right)+1} V_{REF} = \frac{1}{4+12/13} V_{REF}$$

$$V_o = V_1 = \frac{4/3}{4/3+3} \cdot V_2 = \frac{4/3}{4/3+3} \cdot \frac{1}{4+12/13} V_{REF} = \frac{5}{16} = \boxed{0.3125}$$

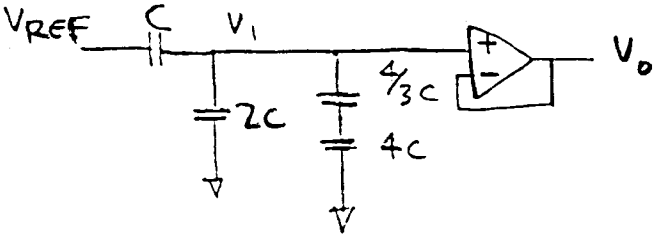
D = 0010 equivalent ckt



$$V_2 = \frac{2}{\left(\frac{4/3 \cdot 3}{4/3+3} + 2\right)+2} V_{REF} = \frac{2}{4+12/13} V_{REF}$$

$$V_o = V_1 = \frac{4/3}{4/3+3} \cdot \frac{2}{4+12/13} V_{REF} = \frac{5}{8} = \boxed{0.625\,V}$$

D = 0100 equivalent ckt



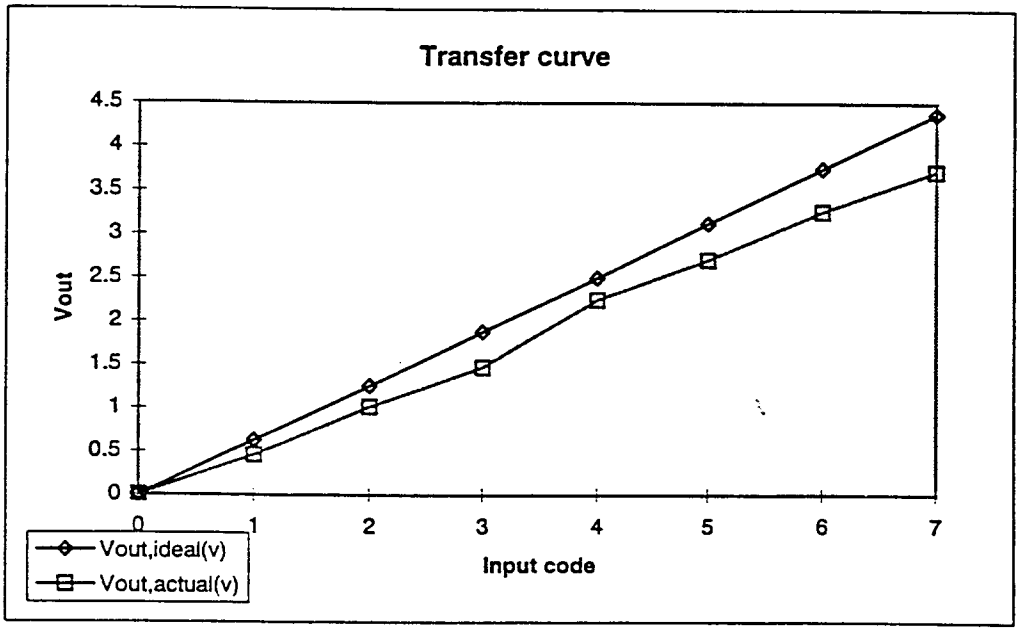
$$V_o = V_1 = \frac{1}{\left(\frac{4/3 \cdot 4}{4/3+4} + 3\right)+1} V_{REF} = \frac{5}{4} = \boxed{1.25\,V}$$

D = 1000 equivalent ckt

V_{REF} 2C V_1

29.13.

Input	D2	D1	D0	Vout,ideal(v)	Vout,actual(v)	Vout,nogain(v)	INL(v)	INL(LSBs)	DNL(v)	DNL(LSBs)
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0.625	0.455625	0.536119516	-0.08888	-0.142209	-0.08888	-0.1422088
2	0	1	0	1.25	1.0125	1.191376702	-0.058623	-0.093797	0.030257	0.0484115
3	0	1	1	1.875	1.468125	1.727496218	-0.147504	-0.236006	-0.08888	-0.1422088
4	1	0	0	2.5	2.25	2.647503782	0.147504	0.2360061	0.295008	0.4720121
5	1	0	1	3.125	2.705625	3.183623298	0.058623	0.0937973	-0.08888	-0.1422088
6	1	1	0	3.75	3.2625	3.838880484	0.08888	0.1422088	0.030257	0.0484115
7	1	1	1	4.375	3.718125	4.375	8.88E-16	1.421E-15	-0.08888	-0.1422088
					MAXIMUM		0.147504	0.2360061	~~0.08888~~	~~0.1422088~~



$V_{out,actual} = V_{REF} \sum_{K=0}^{N} A^{N-K} \cdot D_K = V_{REF}\left[A \cdot D_2 + A^2 \cdot D_1 + A^1 \cdot D_0\right]$ $A = 0.45$

offset = 0

Gain error = Gain,ideal − Gain,actual

$= 1 - \frac{3.71875/0.625}{7} \doteq 1 - 0.85 = 0.15$ LSB/LSB

After removing offset, gain error

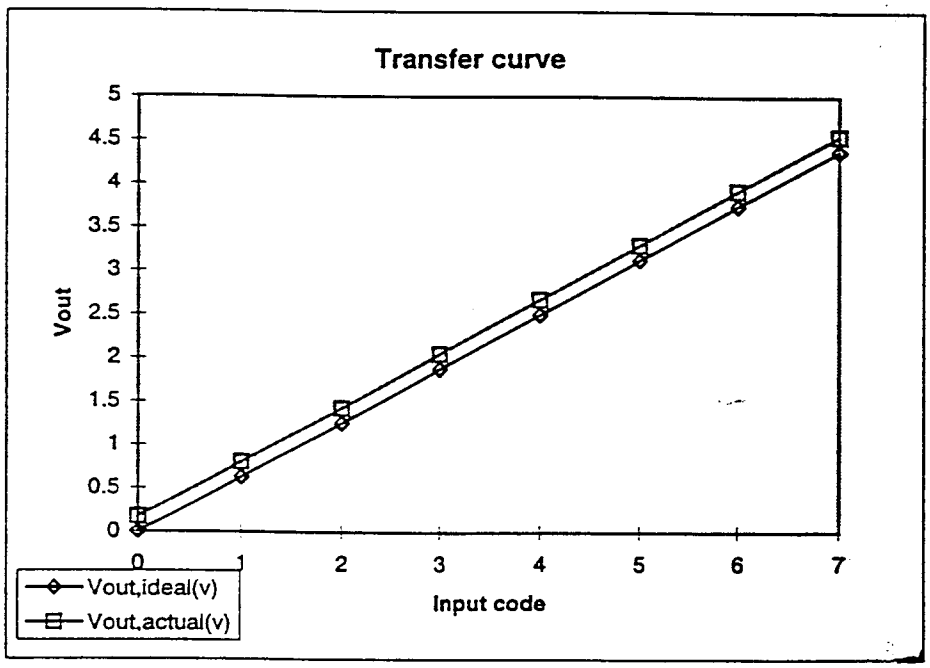
$|INL|_{max} = 0.236$ LSBs $= 0.1475$ V

$|DNL|_{max} = 0.472$ LSBs $= 0.295$ V.

29.14

Input	D2	D1	D0	Vout,ideal(v)	Vout,actual(v)	Vout,nooff(v)	INL(v)	INL(LSBs)	DNL(v)	DNL(LSBs)
0	0	0	0	0	0.175	0	0	0	0	0
1	0	0	1	0.625	0.8	0.625	0	0	0	0
2	0	1	0	1.25	1.425	1.25	0	0	0	0
3	0	1	1	1.875	2.05	1.875	0	0	0	0
4	1	0	0	2.5	2.675	2.5	0	0	0	0
5	1	0	1	3.125	3.3	3.125	0	0	0	0
6	1	1	0	3.75	3.925	3.75	0	0	0	0
7	1	1	1	4.375	4.55	4.375	0	0	0	0
					MAXIMUM		0	0	0	0

Offset=0.175v



Assume: $V_{off} = 0.2V$

$A = 0.5$

$V_{off} = 0.2V$

$$V_{out} = V_{ref} \sum_{K=0}^{N-1} A^{N-K} \cdot D_K + \sum_{K=0}^{N-1} A^{N-K} \cdot V_{off}$$

$$= V_{REF} \left[A \cdot D_2 + A^2 \cdot D_1 + A^3 D_0\right] + V_{off} \left[A + A^2 + A^3\right]$$

$$= V_{out,ideal} + 0.175V$$

offset $= 0.175V$

gain error $= 0$

After removing offset, gain error.

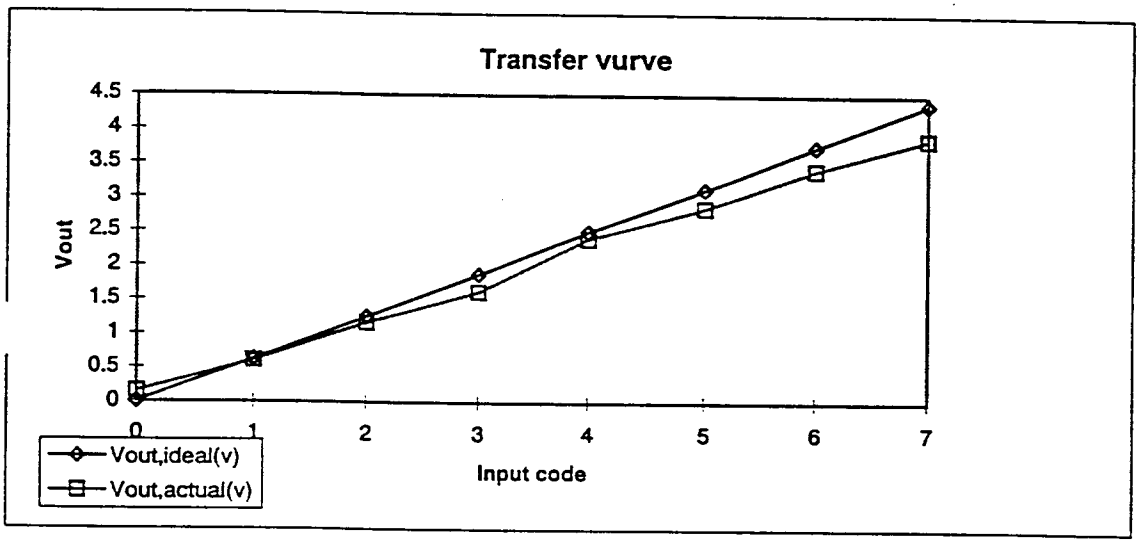
$|INL|_{max} = 0$

$|DNL|_{max} = 0$

29.15

Input	D2	D1	D0	Vout,ideal(v)	Vout,actual(v)	Vout,nooff(v)	Vout,nogain(v)	INL(v)	INL(LSBs)	DNL(v)	DNL(LSBs)
0	0	0	0	0	0.148725	0	0	0	0	0	0
1	0	0	1	0.625	0.60435	0.455625	0.536119516	-0.08888	-0.14221	-0.08888	-0.14221
2	0	1	0	1.25	1.161225	1.0125	1.191376702	-0.05862	-0.0938	0.030257	0.048411
3	0	1	1	1.875	1.61685	1.468125	1.727496218	-0.1475	-0.23601	-0.08888	-0.14221
4	1	0	0	2.5	2.398725	2.25	2.647503782	0.147504	0.236006	0.295008	0.472012
5	1	0	1	3.125	2.85435	2.705625	3.183623298	0.058623	0.093797	-0.08888	-0.14221
6	1	1	0	3.75	3.411225	3.2625	3.838880484	0.08888	0.142209	0.030257	0.048411
7	1	1	1	4.375	3.86685	3.718125	4.375	0	0	-0.08888	-0.14221
					MAXIMUM			0.147504	0.236006	~~0.08888~~ 0.295008	~~0.142209~~ 0.472012

Offset=0.175v



$V_{out} = V_{ref}[A \cdot D_2 + A^2 \cdot D_1 + A^3 \cdot D_0] + V_{off}[A + A^2 + A^3]$

$A = 0.45$

$V_{off} = 0.2V$

offset = 0.148725 V = 0.23796 LSBs

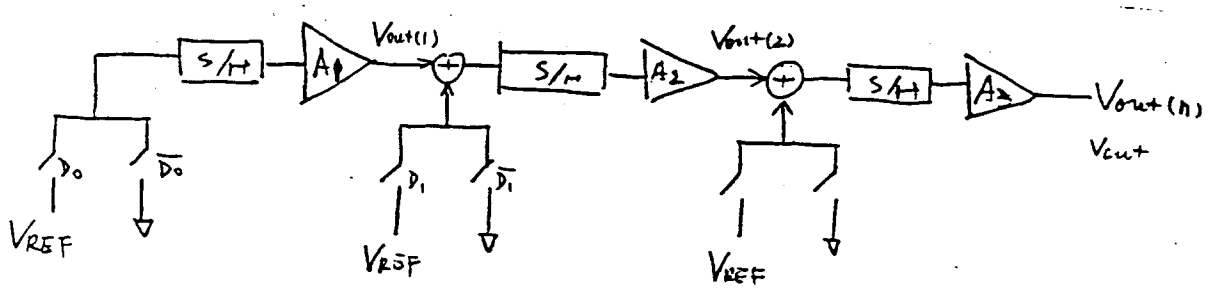
gain error $= 1 - \frac{3.718125/0.625}{7} = 1 - 0.85 = .15$ LSB/LSB

after removing offset, gain error

$|INL|_{max} = 0.1475\ V = 0.236$ LSBs

$|DNL|_{max} = 0.295\ V = 0.472$ LSBs

29.16.



$A_{ideal} = 1/2$, $V_{REF} = 5V$

a) $A_2 = A_3 = A_{ideal} = 1/2 = A$.

$V_{out(1)} = D_0 \cdot V_{REF} \cdot A_1$

$V_{out(2)} = (D_1 \cdot V_{REF} + D_0 V_{REF} \cdot A_1) A_2$

$V_{out(3)} = (D_2 V_{REF} + (D_1 \cdot V_{REF} + D_0 V_{REF} A_1) A_2) A_3$

$= V_{REF}(D_0 \cdot A_1 A_2 A_3 + D_1 \cdot A_2 \cdot A_3 + D_2 \cdot A_3)$

In this case, $V_{out,actual} = V_{REF}(D_2 \cdot \frac{1}{2} + D_1 \cdot \frac{1}{4} + D_0 \cdot \frac{A_1}{4})$

Input	V_{out}, actual	DNL (no offset)
000	0	0
001	$V_{REF}(\frac{A_1}{4})$	$\chi \cdot V_{REF}(\frac{A_1}{4}) - \frac{V_{REF}}{8}$
010	$V_{REF}(\frac{1}{4})$	$\chi \cdot V_{REF}(\frac{1-A_1}{4}) - \frac{V_{REF}}{8}$
011	$V_{REF}(\frac{1}{4} + \frac{A_1}{4})$	$\chi \cdot V_{REF}(\frac{A_1}{4}) - \frac{V_{REF}}{8}$
100	$V_{REF}(\frac{1}{2})$	$\chi \cdot V_{REF}(\frac{1-A_1}{4}) - \frac{V_{REF}}{8}$
101	$V_{REF}(\frac{1}{2} + \frac{A_1}{4})$	$\chi \cdot V_{REF}(\frac{A_1}{4}) - \frac{V_{REF}}{8}$
110	$V_{REF}(\frac{1}{2} + \frac{1}{4})$	$\chi \cdot V_{REF}(\frac{1-A_1}{4}) - \frac{V_{REF}}{8}$
111	$V_{REF}(\frac{1}{2} + \frac{1}{4} + \frac{A_1}{4})$	$\chi \cdot V_{REF}(\frac{A_1}{4}) - \frac{V_{REF}}{8}$

offset = 0

gain error factor = χ

$\chi = \frac{\frac{7}{8} V_{ref}}{V_{ref}(\frac{1}{2} + \frac{1}{4} + \frac{A_1}{4})} = \frac{7}{2(3+A_1)}$

Set $|DNL| \le \frac{1}{2} LSB_s = \frac{1}{2} \cdot \frac{V_{REF}}{8} = \frac{1}{16} V_{REF}$

$\left| \frac{7}{2(3+A_1)} \frac{A_1}{4} - \frac{1}{8} \right| \le \frac{1}{16} \Rightarrow \frac{3}{13} \le A_1 \le \frac{9}{11}$

$\left| \frac{7}{2(3+A_1)} \frac{1-A_1}{4} - \frac{1}{8} \right| \le \frac{1}{16} \Rightarrow \frac{5}{17} \le A_1 \le \frac{11}{15}$

$\Rightarrow \frac{5}{17} \le A_1 \le \frac{11}{15}$

$0.294 \le A \le 0.733$

In order to let the DAC have $\le \pm \frac{1}{2}$ LSBs of DNL, the gain of first st should be :

$\boxed{0.294 < A < 0.733}$

b) $V_{out,actual} = V_{REF}\left(D_2\cdot\frac{1}{2} + D_1\cdot\frac{A_2}{2} + D_0\cdot\frac{A_2}{4}\right)$

Input	V_{out} actual	DNL
0 0 0	0	0
0 0 1	$V_{REF}\left(\frac{A_2}{4}\right)$	$\chi\cdot V_{REF}\left(\frac{A_2}{4}\right)-\frac{1}{8}V_{ref}$
0 1 0	$V_{REF}\left(\frac{A_2}{2}\right)$	$\chi\cdot V_{REF}\left(\frac{A_2}{4}\right)-\frac{1}{8}V_{ref}$
0 1 1	$V_{REF}\left(\frac{3A_2}{4}\right)$	$\chi\cdot V_{REF}\left(\frac{A_2}{4}\right)-\frac{1}{8}V_{ref}$
1 0 0	$V_{REF}\left(\frac{1}{2}\right)$	$\chi\cdot V_{REF}\left(\frac{1}{2}-\frac{3A_2}{4}\right)-\frac{1}{8}V_{ref}$
1 0 1	$V_{REF}\left(\frac{1}{2}+\frac{A_2}{4}\right)$	$\chi\cdot V_{REF}\left(\frac{A_2}{4}\right)-\frac{1}{8}V_{ref}$
1 1 0	$V_{REF}\left(\frac{1}{2}+\frac{A_2}{2}\right)$	$\chi\cdot V_{REF}\left(\frac{A_2}{4}\right)-\frac{1}{8}V_{ref}$
1 1 1	$V_{REF}\left(\frac{1}{2}+\frac{3A_2}{4}\right)$	$\chi\cdot V_{REF}\left(\frac{A_2}{4}\right)-\frac{1}{8}V_{ref}$

offset = 0

gain error factor χ

$\chi = \frac{\frac{7}{8}V_{ref}}{V_{ref}\left(\frac{1}{2}+\frac{3}{4}A_2\right)} = \frac{7}{2(2+3A_2)}$

Set $|DNL| \le \frac{1}{16}V_{REF}$

$\left|\frac{7}{2(2+3A_2)}\left(\frac{A_2}{4}\right)-\frac{1}{8}\right| \le \frac{1}{16} \Rightarrow \frac{2}{11} \le A_2 \le \frac{6}{5}$

$\left|\frac{7}{2(2+3A_2)}\left(\frac{1}{2}-\frac{3A_2}{4}\right)-\frac{1}{8}\right| \le \frac{1}{16} \Rightarrow \frac{22}{51} \le A_2 \le \frac{26}{45}$

$\Rightarrow \frac{22}{51} \le A_2 \le \frac{26}{45}$

$\boxed{0.4314 \le A_2 \le 0.5778}$

c) $V_{out,actual} = V_{REF}\left(D_2\cdot A_3 + D_1\cdot\frac{A_3}{2} + D_0\cdot\frac{A_3}{4}\right)$

Input	$V_{out,actual}$	DNL
0 0 0	0	0
0 0 1	$V_{REF}\left(\frac{A_3}{4}\right)$	$\chi\cdot V_{REF}\left(\frac{A_3}{4}\right)-\frac{1}{8}V_{ref}$
0 1 0	$V_{REF}\left(\frac{A_3}{2}\right)$	$\chi\cdot V_{REF}\left(\frac{A_3}{4}\right)-\frac{1}{8}V_{ref}$
0 1 1	$V_{REF}\left(\frac{3A_3}{4}\right)$	$\chi\cdot V_{REF}\left(\frac{A_3}{4}\right)-\frac{1}{8}V_{ref}$
1 0 0	$V_{REF}\left(A_3\right)$	$\chi\cdot V_{REF}\left(\frac{3A_3}{4}\right)-\frac{1}{8}V_{ref}$
1 0 1	$V_{REF}\left(\frac{5A_3}{4}\right)$	$\chi\cdot V_{REF}\left(\frac{1}{4}A_3\right)-\frac{1}{8}V_{ref}$
1 1 0	$V_{REF}\left(\frac{6A_3}{4}\right)$	$\chi\cdot V_{REF}\left(\frac{A_3}{2}\right)-\frac{1}{8}V_{ref}$
1 1 1	$V_{REF}\left(\frac{7}{4}A_3\right)$	$\chi\cdot V_{REF}\left(\frac{A_3}{4}\right)-\frac{1}{8}V_{ref}$

offset = 0

gain error factor χ

$\chi = \frac{\frac{7}{8}V_{ref}}{V_{ref}\left(\frac{7}{8}A_3\right)} = \frac{1}{2A_3}$

Set $|DNL| \le \frac{1}{16}V_{REF}$

$\left|\frac{1}{2A_3}\cdot\frac{A_3}{4}-\frac{1}{8}\right| = |0| \le \frac{1}{16}V_{ref}$

In this case, $\boxed{\text{no restriction for } A_3}$ but there will be gain error

$V_{off} = 0.25$ $\quad A_1 = A_2 = A_3 = A = \frac{1}{2}$

29.17 a) $V_{out1} = (D_0 \cdot V_{REF} + V_{off}) A_1$

$V_{out2} = (D_1 \cdot V_{REF} + (D_0 \cdot V_{REF} + V_{off}) \cdot A_1) A_2$

$V_{out3} = (D_2 \cdot V_{REF} + (D_1 V_{REF} + (D_0 \cdot V_{REF} + V_{off}) A_1) A_2) A_3$

$= V_{REF}(D_2 \cdot A_3 + D_1 \cdot A_2 A_3 - D_0 \cdot A_1 A_2 A_3) + V_{off} \cdot A_1 A_2 A_3$

$= V_{REF} \cdot (D_2 A + D_1 A^2 + D_0 A^3) + 0.03125V = V_{i,ideal} + 0.5125V$

offset $= 0.03125\,V = 0.05$ LSBs

After removing offset. $V_{out,\,no\,offset} = V_{i,ideal}$

$|INL|_{max} = 0$

$|DNL|_{max} = 0$

b) $V_{out} = V_{REF} \cdot (D_2 \cdot A + D_1 \cdot A^2 + D_0 A^3) + V_{off} \cdot A_2 \cdot A_3$

$= V_{i,ideal} + 0.0625V$

offset $= 0.0625\,V = 0.1$ LSBs

$|INL|_{max} = 0$, $\quad |DNL|_{max} = 0$

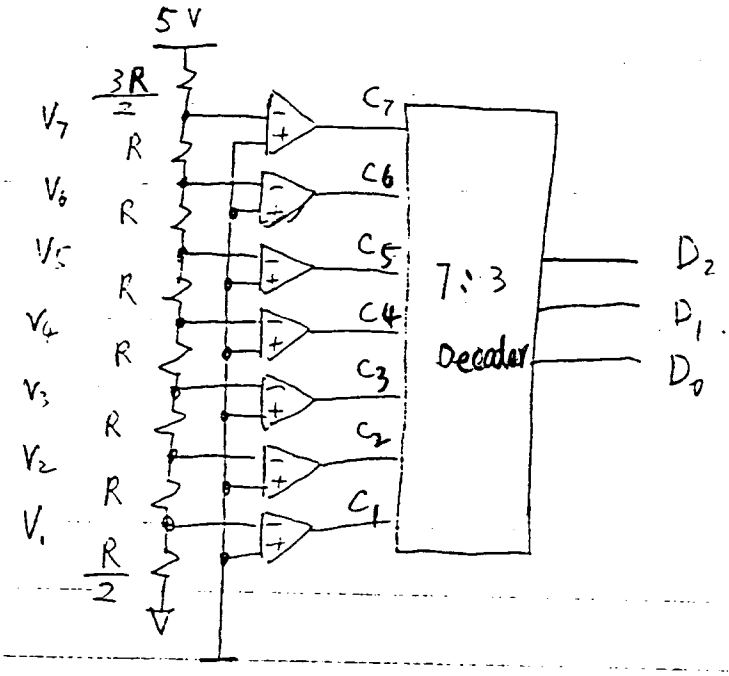
c) $V_{out} = V_{REF}(D_2 \cdot A + D_1 \cdot A^2 + D_0 A^3) + V_{off} \cdot A_3$

$= V_{i,ideal} + 0.125\,V$

offset $= 0.125\,V = 0.2$ LSBs

$|INL|_{max} = 0$ $\quad |DNL|_{max} = 0$

29.18 3-bit flash ADC



V_{in}	$C_7C_6C_5C_4C_3C_2C_1$	$D_2D_1D_0$
$0 \le V_{in} < 0.3125$	0000000	000
$0.3125 \le V_{in} < 0.9375$	0000001	001
$0.9375 \le V_{in} < 1.5625$	0000011	010
$1.5625 \le V_{in} < 2.1875$	0000111	011
$2.1875 \le V_{in} < 2.8125$	0001111	100
$2.8125 \le V_{in} < 3.4375$	0011111	101
$3.4375 \le V_{in} < 4.0625$	0111111	110
$4.0625 \le V_{in}$	1111111	111

$$|DNL|_{max} = \frac{5V}{8} \times 0.05 = 31.25\,mV = 0.05\,LSB$$

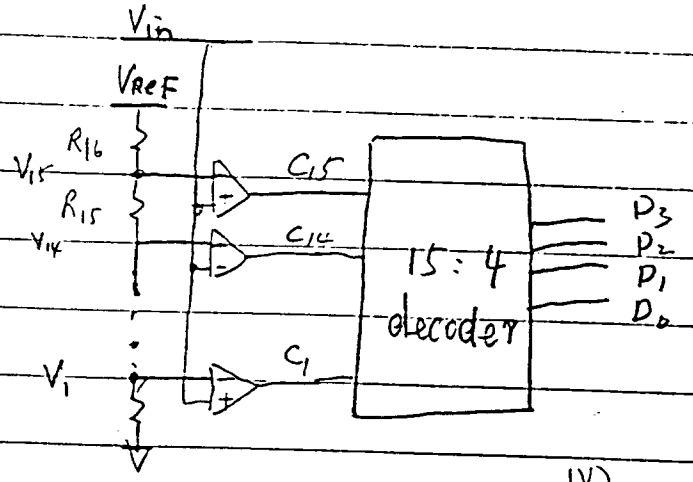
$$|INL|_{max} = \frac{5}{2} \times 0.05 = 125\,mV = 4.2\,LSB$$

29.19 $1LSB = \frac{5}{8} V = 625\,mV$

$$|DNL|_{max} = \frac{V_{REF}}{2^N}\left|\frac{\Delta R}{R}\right|_{max} + 2|V_{os}|_{max} \le \frac{625\,mV}{2}$$

$$\therefore |V_{os}|_{max} \le \left(\frac{625\,mV}{2} - 31.25\,mV\right)/2 = \boxed{140.625\,mV}$$

29.20 $\sum_{i=1}^{16}\left(\frac{\Delta R}{R}\right)_i = (2+1.5+0-1-0.5+1+1.5+3+2.5+1-0.5-1.5-2+0+1+1)\% = 8\% \neq 0.$



n	R	V_n (V)	$V_{n,ideal}$ (V)	$V_{n,no-of}$ (V)	$V_{n,measured}$ (V)	INL (mV)	DNL (mV)
1	1.02	0.317	0.3125	0.3125	0.31290	0.4	0.4
2	1.015	0.633	0.6250	0.6285	0.6293	4.3	3.9
3	1	0.944	0.9375	0.9395	0.9407	3.2	-1.1
4	0.99	1.252	1.2500	1.2475	1.2491	0.9	-4.1
5	0.995	1.561	1.5625	1.5565	1.5585	-4.0	-3.1
6	1.01	1.875	1.8750	1.8705	1.8729	-2.1	-1.9
7	1.015	2.191	2.1875	2.1865	2.1893	-1.8	-2.5
8	1.02	2.508	2.5000	2.5035	2.5067	-6.7	4.9
9	1.025	2.826	2.8125	2.8215	2.8251	12.6	4.9
10	1.01	3.141	3.1250	3.1365	3.1405	15.5	2.9
11	0.995	3.450	3.4375	3.4455	3.4499	12.4	-3.1
12	0.985	3.756	3.7500	3.7515	3.7563	6.3	-6.1
13	0.98	4.061	4.0625	4.0565	4.0617	-0.8	-7.1
14	1.	4.372	4.3725	4.3675	4.3731	-0.6	-1.1
15	1.01	4.686	4.6825	4.6815	4.6875	0	1.0

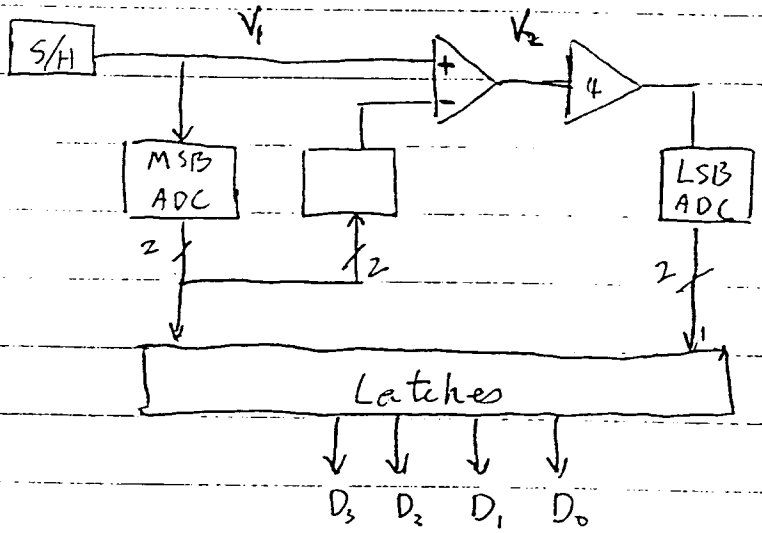
$$|INL|_{max} = 15.5\,mV \leq \frac{5}{2^{N+1}}$$

$$N = \log_2\left(\frac{5}{15.5\times10^{-3}}\right) - 1 = 7.333 \approx 7$$

This converter possesses 7-bit resolution

29.21

$$A_{CL} \cong \frac{1}{\beta} = 2^{N/2} \qquad |A_{OL}| \geq \frac{2^{N+1}}{\beta} = 2^{\frac{3N}{2}+1}$$



$$|A_{OL}| = \frac{1}{\beta}(2^{N+1}+1) \geq \frac{2^{N+1}}{\beta}$$

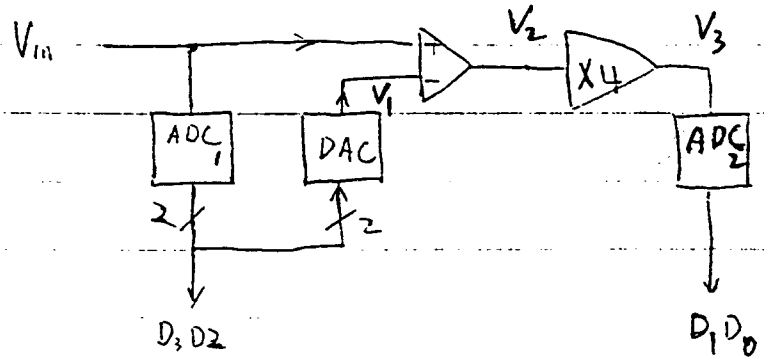
(a) For $N=4$ $\quad |A_{OL}| \geq 2^7 = 128$

(b) For $N=8$ $\quad |A_{OL}| \geq 2^{13} = 8192$

(c) For $N=10$ $\quad |A_{OL}| \geq 2^{16} = 65536$

29.22

4-bit, two-step flash ADC



IF ADC_2 has an accuracy of $\frac{1}{2^{N_2}}$

$$\Delta V_3 = \frac{V_{REF}}{2^{N_2+1}} \qquad \Delta V_2 = \frac{\Delta V_3}{4} = \frac{V_{REF}}{2^{N_2+3}}$$

Assume ADC1 is ideal, then

$$\Delta V_{in} = -\Delta V_2 = \frac{V_{REF}}{2^{N_2+3}} \leq \frac{V_{REF}}{2^{4+1}} \Rightarrow N_2 \geq 2$$

So ADC_2 has 2-bit accuracy at least.

If ADC_1 has an accuracy of $\frac{1}{2^{N_1}}$

$$\Delta V_{in} = \Delta V_1 = \frac{V_{REF}}{2^{N_1+1}} = \Delta V_2 \Rightarrow \Delta V_3 = \frac{4\,V_{REF}}{2^{N_1+1}} \leq \frac{V_{REF}}{2^{2+1}}$$

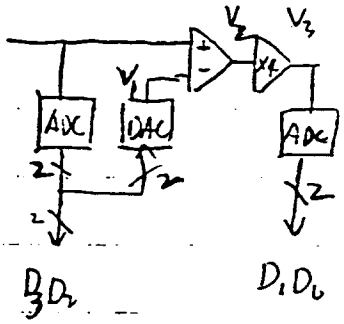
$$\Rightarrow N_1 = 4.$$

So ADC_1 has 4-bit accuracy at least.

∴ The first flash converter needs to be more accurate than the second one

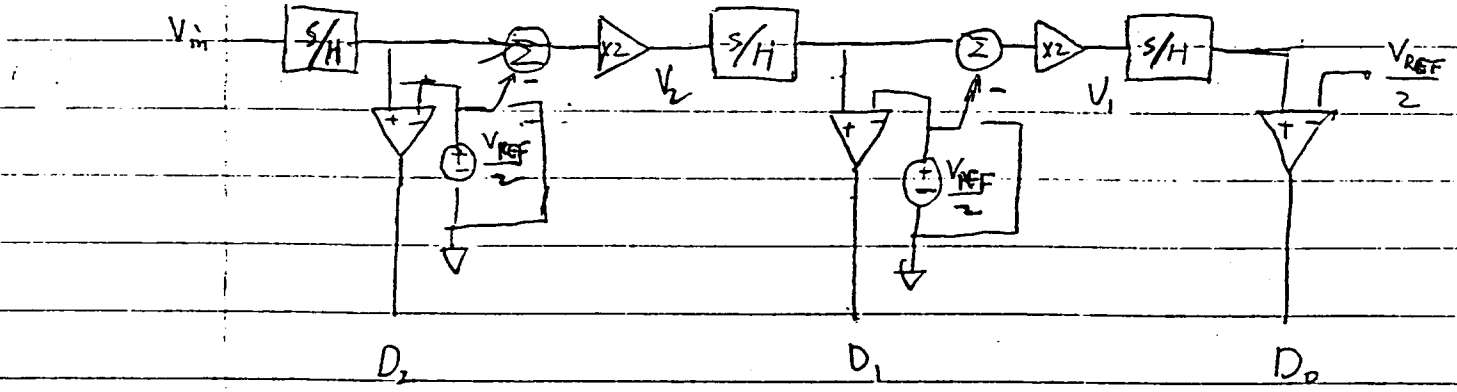
29.23. $V_{in} = 3, 5, 7.5, 14.75\,V$.

V_{in}	V_1	V_2	V_3	$D_3D_2D_1D_0$
3	0	3	12	0011
5	4	1	4	0101
7.5	4	3.5	14	0111
14.75	12	2.75	11	1110



29.24

$V_{REF} = 8V$



V_{in}	V_2	V_1	D_2	D_1	D_0
1	2	4	0	0	1
4	0	0	1	0	0
6	4	0	1	1	0
7	6	4	1	1	1

29.25 For 8 bits, it is best to write a program that generates the transfer curve, for increasing values of v_{IN}. INL & DNL can be determined from the resulting data.

2926 Use eqs. 29.61, 29.62 & 29.63 to calculate the values of v_{IN} that cause the digital output to change.

For a 3 bit pipeline, there are only two residue amplifiers.

When the 1st residue amp. has a gain of 2.2 the new switch points occur at:

$V_{IN,1} = 2.5V$

$$V_{p2?} = 2.5V = \left[V_{IN} - \tfrac{1}{2} D_{N-1} \cdot V_{REF}\right] 2.2$$

(2.2: gain of 1st residue amp.)

or $V_{IN} = \frac{2.5}{2.2} + \frac{1}{2} D_{N-1} \cdot V_{REF}$ where $D_{N-1} = D_2$ (MSB) & can be either 0 or 1.

$\therefore$ D_1 switches when

$V_{IN} = 1.136\,V,\ 3.636$

since $V_{p3} = 2.5 = \left[\left[V_{IN} - \tfrac{1}{2} \cdot D_2 \cdot V_{REF}\right] A_2 - \left[\tfrac{1}{2} \cdot D_1 \cdot V_{REF}\right]\right] A_1$

(A_2: gain of 1st residue amp; A_1: gain of the 2nd residue amp.)

$\therefore$ D_0 switches when

$$V_{IN} = \frac{\frac{2.5}{2} + 2.5 D_1}{2.2} + 2.5 D_2$$

for $D_2 D_1$ 4 combinations

or $V_{IN} = 0.5682,\ 3.068,\ 1.7045,\ 4.2045$

29.26 con't.

∴ when A_2 (the 1st residue amp) has a gain of 2.2, V_{IN} switches at:

A_2=2.2		Ideal	DNL (V)	INL (V)
0	000	0		
0.5682	001	0.625	-0.0568	-0.0568
1.136	010	1.25	-0.0572	-0.114
1.7045	011	1.875	-0.0565	-0.1705
2.5	100	2.5	0	0
3.068	101	3.125	-0.057	-0.057
3.6364	110	3.75	-0.0566	-0.1136
4.2045	111	4.375	-0.0569	-0.1705

INL + DNL can be calculated by comparing the new switching pts to the ideal case, as see above.

Now perform same analysis using $A_1 = 2.2$, while $A_2 = 2.0$. This yields,

$$V_{IN} = \frac{\frac{2.5}{2.2} + 2.5 D_1}{2.0} + 2.5 D_2 \quad \text{or}$$

$$V_{IN} = 0.5682,\ 1.818,\ 3.0682,\ 4.3182$$

Note that since the 1st residue is now ideal (gain of 2), all the other switching points are ideal (eq. 29.63, 29.61)

A_1=2.2 yields the following switch points,

V_{IN}	DNL	INL
0	-	0
0.5682	-0.0568	-0.0568
1.25	0.0568	0
1.818	-0.057	-0.057
2.5	0.057	0
3.0682	-0.0568	-0.0568
3.75	0.0568	0
4.3182	-0.0568	-0.0568

Compare these values to the previous case shows both DNL + INL are improved!

29.27

$t_{c(max)} \Rightarrow$ occurs when $N_{IN} = V_{FS}$

$\therefore$ eqs. (29.8) and (29.79)

$$\therefore t_c = \frac{V_{FS}}{V_{REF}} \cdot 2^N \cdot T_{CLK}$$

$$= \frac{2^N - 1}{2^N} \cdot \frac{V_{REF}}{V_{REF}} \cdot 2^N \cdot T_{CLK}$$

$$= (255)(1\mu S) = 255\mu S.$$

eq. (29.80) $$F_{max} = \frac{f_{sample}}{2} = \frac{V_{REF}}{V_{FS} \cdot 2^{N+1}} \cdot 1MHz = \frac{1MHz}{510} = \underline{1.96\ kHz}\ !$$

$$V_{Max} = V_{FS} = \frac{255}{256} \cdot V_{REF} = \underline{4.98\ V.}$$

29.28

eq. (29.81) $\Rightarrow$ $V_C = \frac{V_{REF} \cdot t_c}{RC}$

since the conversion time, t_c, is dependent on the value of V_{IN}, for the worst case of $V_{IN} = V_{FS} = V_C$

$$V_{C(ideal)} = \frac{V_{REF} \cdot (2^N - 1) T_{CLK}}{RC} = \frac{2^N - 1}{2^N} V_{REF}$$

$\therefore$ The RC time constant must be:

$$RC = 2^N T_{CLK} = \underline{256\mu S}$$

Tolerance on clock (Assume $V_{IN} = 2.5\ V$ worst-case)

$V_{C,ideal} = 2.5\ V$

for ½ LSB INL, $V_{C,actual} - 2.5 = \frac{5}{2^9} = \pm 9.765\ mV$

or $V_{C,actual} = 2.5 \pm 9.765\ mV$ & $f_{CLK} = \frac{2^N \cdot 2.5}{V_{C,actual} \cdot RC}$ (29.82)

$+ \quad 996.11\ kHz \leq f_{CLK} \leq 1.0389\ MHz$

29.29 Max Conversion time:

1st integration takes 2^N clock cycles

2nd integration takes $2^N - 1$ maximum clock cycles. (when $V_{IN} = V_{FS}$)

∴ Max conversion time is,

$$t_{c(max)} = (2^N + 2^N - 1)\,1\mu s \text{ or } 511\ \mu s$$

Minimum conversion time still requires the 1st integration of 2^N clock cycles

If $V_{IN} = 0$, then $t_{c(min)} = 256\ \mu s$

For $V_{IN} = 2.5$ V,

$$t_c = 2^N + \frac{1}{2}(2^N) = 256 + 128 = 384\ \mu s$$

($\frac{V_{IN}}{V_{REF}}$; 1st int.; 2nd)

29.30

Advantages: Dual slope removes nonidealities of R, C, & F_{CLK} so is the more accurate of two converters

Disadvantage: The first integration can be considered as a calibration phase which requires a hefty 2^N clock cycle overhead for each conversion.

29.31

$V_{REF} = 5\,V$, $V_{IN} = 1\,V$

Step	$B_3B_2B_1B_0$	$D_3'D_2'D_1'D_0'$	V_{OUT}	Comp_Out	$D_3D_2D_1D_0$
1	1000	1000	$\frac{1}{2}V_{REF} = 2.5V$	1	0000
2	0100	0100	$\frac{1}{4}V_{REF} = 1.25V$	1	0000
3	0010	0010	$\frac{1}{8}V_{REF} = 0.625V$	0	0010
4	0001	0011	$\frac{3}{16}V_{REF} = 0.9375V$	0	0011

$V_{IN} = 3\,V$

Step	$B_3B_2B_1B_0$	$D_3'D_2'D_1'D_0'$	V_{OUT}	Comp_Out	$D_3D_2D_1D_0$
1	1000	1000	2.5 V	0	1000
2	0100	1100	3.75 V	1	1000
3	0010	1010	3.125 V	1	1000
4	0001	1001	2.8125 V	0	1001

$V_{IN} = V_{FS} = 4.6875$

Step	$B_3B_2B_1B_0$	$D_3'D_2'D_1'D_0'$	V_{OUT}	Comp_Out	$D_3D_2D_1D_0$
1	1000	1000	2.5 V	0	1000
2	0100	1100	3.75 V	0	1100
3	0010	1110	4.375 V	0	1110
4	0011	1111	4.6875	0	1111

29.32 Refer to Fig. 29.36 This problem refers to the 4bit ADC used in P29.31

$V_{IN} = 2.49$

Because of offset, Comp_out = 0 (wrong decision)

step	$D_3'D_2'D_1'D_0'$	V_{OUT}	Comp_OUT	$D_3D_2D_1D_0$
1	1000	2.5V	0	1000
2	1100	3.75V	1	1000
3	1010	3.125	1	1000
4	1001	2.8125	1	1000

The answer should be 0111

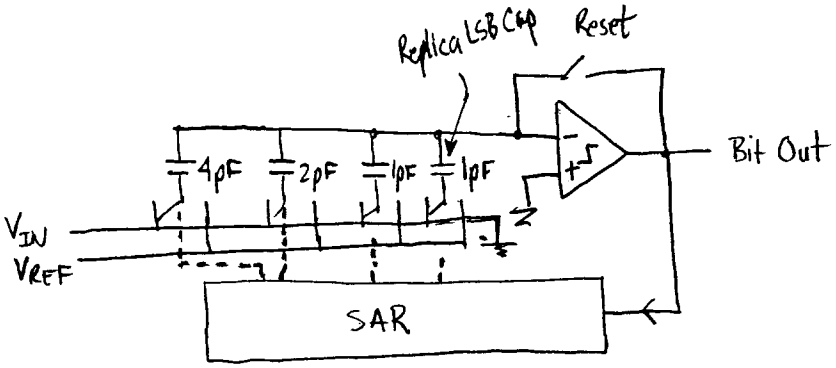
$V_{IN} = 0.3025$

Step	$D_3'D_2'D_1'D_0'$	V_{OUT}	Comp_OUT	$D_3D_2D_1D_0$
1	1000	2.5	1	0000
2	0100	1.25	1	0000
3	0010	0.625	1	0000
4	0001	0.3125	0	0001

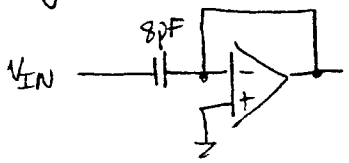
The answer should be 0000 since

$V_{IN} < 1$ LSB!

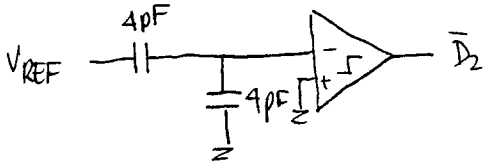
29.33



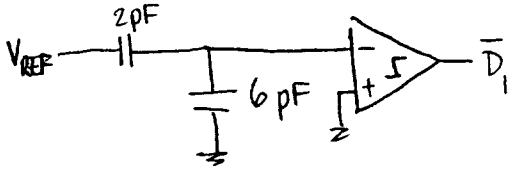
Sampling



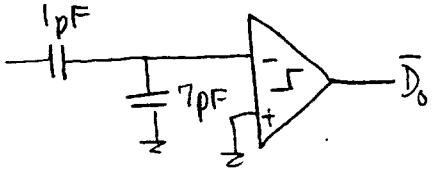
MSB (D_2 Comparison)



D_1 Comparison ($D_2 = 0$)



D_0 Comparison ($D_2 + D_1 = 0$)



Note that after sampling, the bottom plate of the replica LSB capacitor always stays on ground.

For $V_{IN} = 2$ V,

Step	$D_2 D_1 D_0$	V_{TOP}
1	0 0 0	-2 V
2	0 1 0	$-2\text{ V} + \frac{V_{REF}}{4} = -0.75$ V
3	0 1 1	$-2\text{V} + \frac{V_{REF}}{4} + \frac{V_{REF}}{8} = -0.125$V

See eq. (29.89)

29.33 (Con't)

For $V_{IN} = 3V$

Step	D_2 D_1 D_0	V_{TOP}
1	1 0 0	$-3 + \frac{V_{REF}}{2} = -0.5$
2	1 0 0	$-0.5V$
3	1 0 0	$-0.5V$

For $V_{IN} = 4V$

Step	$D_2 D_1 D_0$	V_{TOP}
1	1 0 0	$-3 + \frac{V_{REF}}{2} = -0.5$
2	1 1 0	$-3 + \frac{V_{REF}}{2} + \frac{V_{REF}}{4} = -0.25V$
3	1 1 0	$-0.25V$

Note that once V_{TOP} is within ± 1 LSB, that the converted digital output doesn't change.

29.34

eq. (29.91) $|INL|_{max} = 4 \cdot (0.01) = \underline{0.04}$

eq. (29.93) $DNL_{max} = (7)(0.01) = \underline{0.07}$

Note that the INL & DNL are independent of the absolute size of the capacitor.

29.35

See problem 29.33

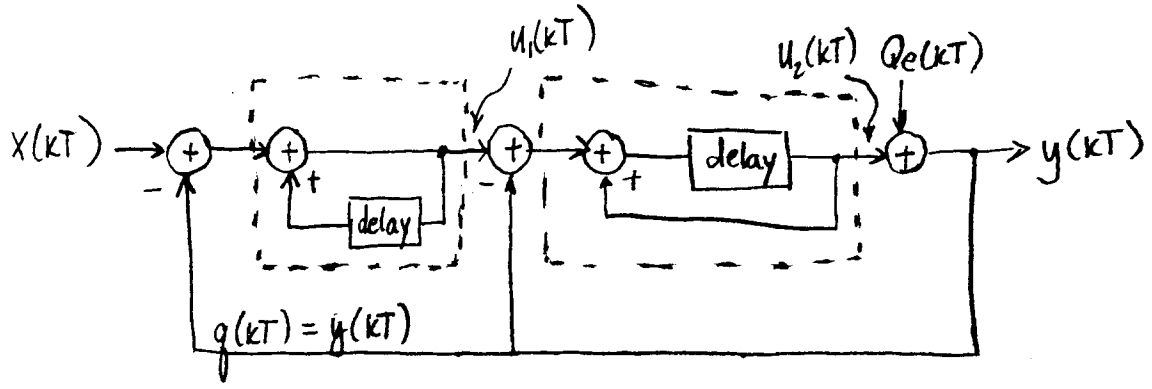
If $V_{OS} = 0.3$ Then, for $V_{IN} = 2.0V$

Step	D_2 D_1 D_0	V_{TOP}
1	0 0 0	$-2 + 0.3 = -1.7V$
2	0 1 0	$-2 + \frac{V_{REF}}{4} + 0.3 = -0.45$
3	0 1 1	$-2 + \frac{V_{REF}}{4} + \frac{V_{REF}}{8} + 0.3 = 0.175$

Even though V_{TOP} is now positive, because of the comparator's offset, the output stays the same. The comparator doesn't switch states until the plus input is 0.3V above ground.

29.36 See sec. 29.2.6

Problem 29.38



1.) $u_2(kT) = u_1(kT-T) - y(kT-T) + u_2(kT-T)$

2.) $u_1(kT) = x(kT) - y(kT) + u_1(kT-T)$

$-Q_e(kT-T)$

3) = 2) → 1.) $u_2(kT) = x(kT-T) - y(kT-T) + u_1(kT-2T) - y(kT-T) + u_2(kT-T)$

4.) $y(kT) = Q_e(kT) + u_2(kT)$

plugging 3) → 4.) $= x(kT-T) - y(kT-T) + u_1(kT-2T) + Q_e(kT) - Q_e(kT-T)$

from 1), we know

$$u_1(kT-2T) = u_2(kT-T) + y(kT-2T) - u_2(kT-2T)$$

4 4.) becames,

$-Q_e(kT-T)$ $\qquad$ $Q_e(kT-2T)$

$$y(kT) = x(kT-T) - y(kT-T) + u_2(kT-T) + y(kT-2T) - u_2(kT-2T) + Q_e(kT) - Q_e(kT-T)$$

$$\therefore y(kT) = x(kT-T) + Q_e(kT) - 2Q_e(kT-T) + Q_e(kT-2T)$$