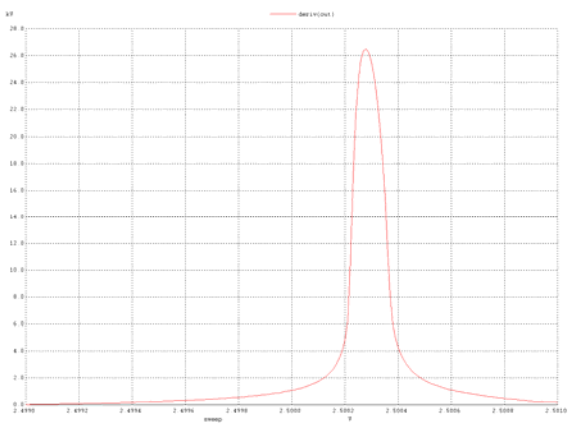
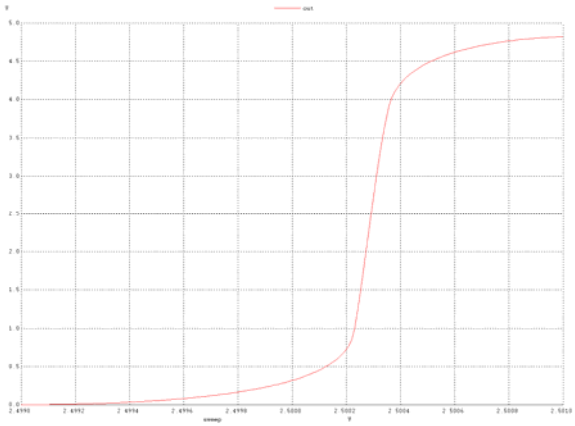
Problem 27.1

Using long channel CMOS process, compare the performance (using simulations) of the comparator in Fig. 27.8 with the comparator in Fig. 27.9. Your comparison should include: DC gain, systematic offset, delay, sensitivity, and power consumption.

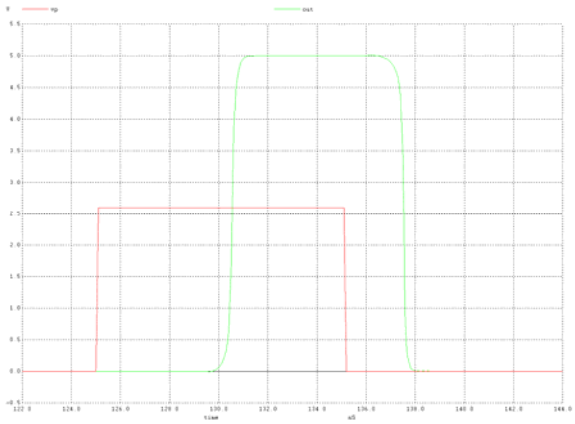
Lets begin by simulating the comparator in Fig. 27.8 and examine its performance.



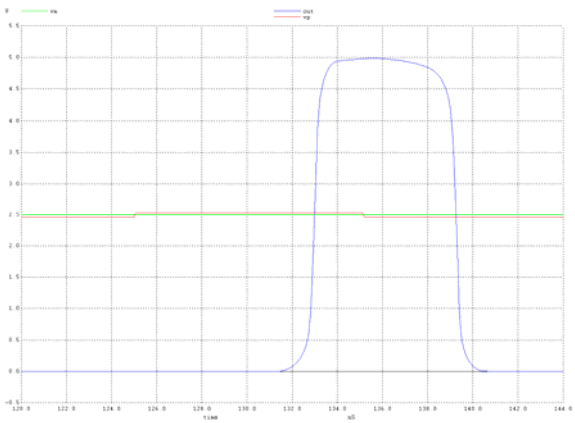
Gain = 26500 V/V



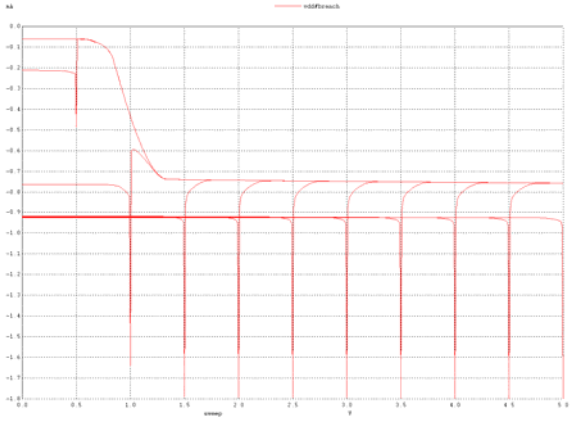
Offset = 300uV



Delay = 5.5nS

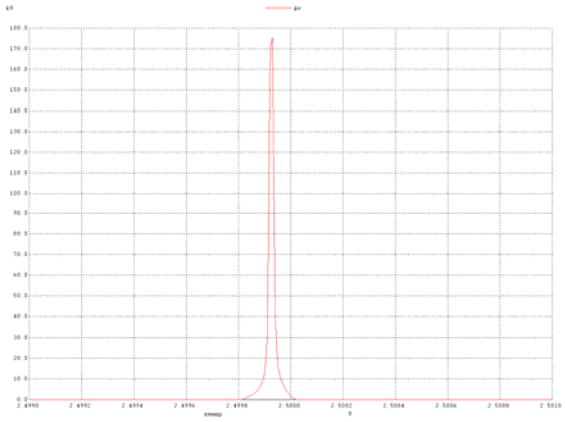


Sensitivity = 40mV

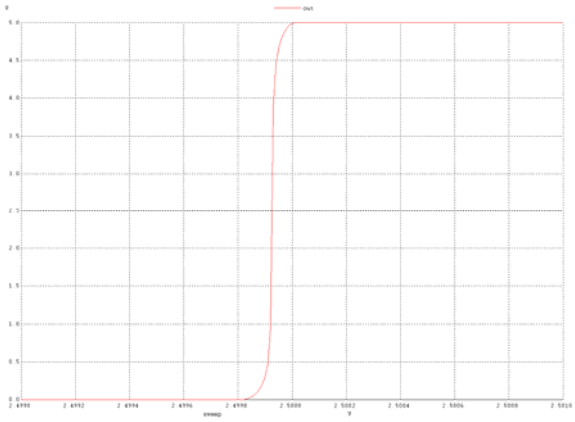


power consumption

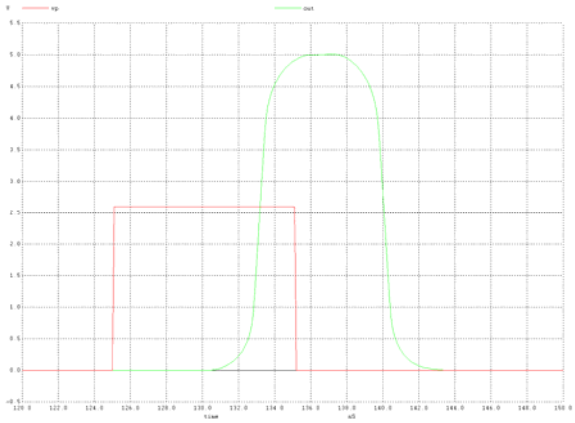
Let’s now revisit the performance of the comparator seen in Fig. 27.9 and compare the performance of the two comparators.



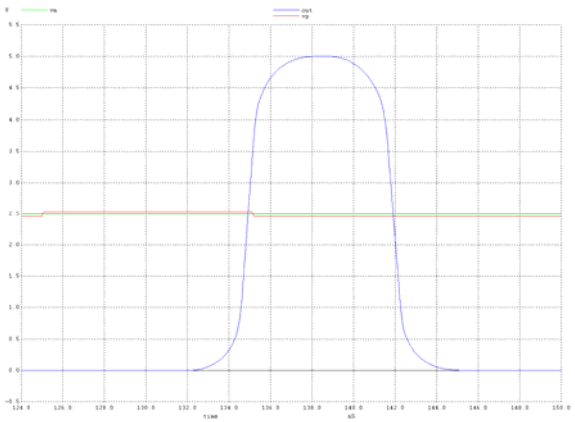
Gain = 175000 V/V



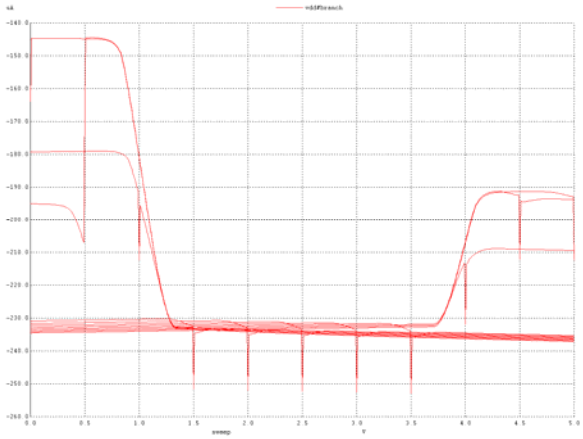
Offset = 75uV



Delay = 8nS



Sensitivity = 40mV



power consumption

The gain is less for the comparator in Fig 27.8 (26.5 kV/V vs. 150 kV/V)
The offset is greater for the comparator in Fig 27.8 (300uV vs. 75 uV)

The Delay is less for the comparator in Fig 27.8 (5.5nS vs. 8.nS)
The sensitivity is roughly the same
The power consumption is greater in the comparator in Fig 27.8, as can be seen by the larger amount of current flowing through it as compared to the comparator in Fig27.9
The comparator in Fig. 27.8 is less complex and has a smaller layout area.

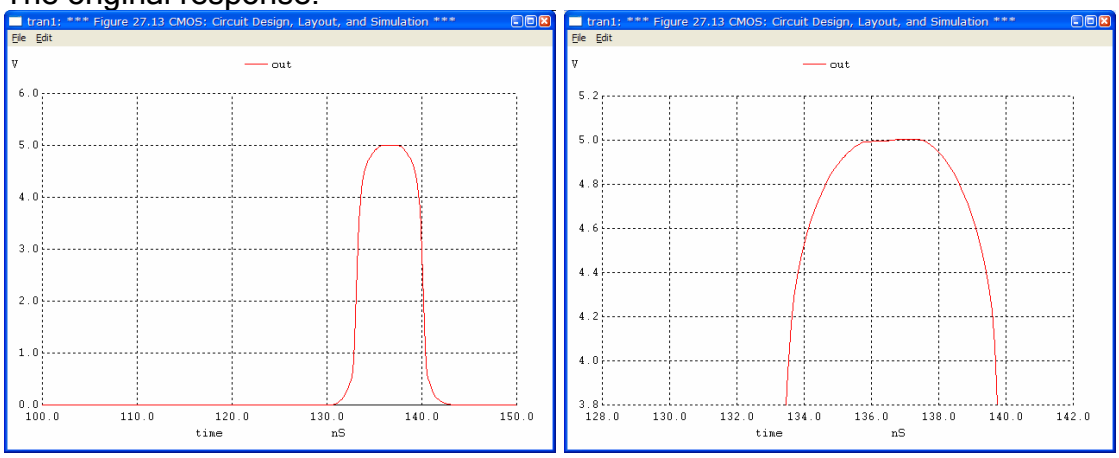
The net list for the comparator in Fig. 27.8 is as follows.

```
Problem 27.1
.control
destroy all
run
.endc
.option scale=1u
*.dc vp     0     5     10m   vm    0     5     500m
*.dc vp     2.499 2.501 10u
.tran 100p 150n

VDD   VDD   0     DC    5
Vp    vp    0     DC    2.5 PULSE 2.46 2.54 125n 0 0 10n
vm    vm    0     DC    2.5
X1    vbiasn      vbiasp      vdd   bias
M1    n1    vp    vss   0     NMOS L=1 W=10
M2    n2    vm    vss   0     NMOS L=1 W=10
Ma    vss   vbiasn      0     0     NMOS L=2 W=20
M31   n1    n1    vdd   vdd   PMOS L=1 W=20
M41   n2    n2    vdd   vdd   PMOS L=1 W=20
M3    vop   n1    vdd   vdd   PMOS L=1 W=20
M4    vom   n2    vdd   vdd   PMOS L=1 W=20
M5    vop   vop   vc    0     NMOS L=1 W=10
M6    vop   vom   vc    0     NMOS L=1 W=10
M7    vom   vop   vc    0     NMOS L=1 W=10
M8    vom   vom   vc    0     NMOS L=1 W=10
Mb    vc    vc    0     0     NMOS L=10 W=10
M9L   n4    vom   n3    0     NMOS L=1 W=10
M9R   vdo   vop   n3    0     NMOS L=1 W=10
M10L  n4    n4    vdd   vdd   PMOS L=1 W=20
M10R  vdo   n4    vdd   vdd   PMOS L=1 W=20
Mc    n3    n4    0     0     NMOS L=1 W=10
MIN   out   vdo   0     0     NMOS L=1 W=10
MIP   out   vdo   vdd   vdd   PMOS L=1 W=20

.subckt bias      vbiasn      vbiasp      VDD
M1    Vbiasn      Vbiasn      0     0     NMOS L=2 W=10
M2    Vbiasp      Vbiasn      Vr    0     NMOS L=2 W=40
M3    Vbiasn      Vbiasp      VDD   VDD   PMOS L=2 W=30
M4    Vbiasp      Vbiasp      VDD   VDD   PMOS L=2 W=30
Rbias Vr    0     6.5k
MSU1  Vsur  Vbiasn      0     0     NMOS L=2   W=10
MSU2  Vsur  Vsur  VDD   VDD   PMOS L=100 W=10
MSU3  Vbiasp      Vsur  Vbiasn      0     NMOS L=1   W=10
.ends
.include .\1um_models.txt
.end
```

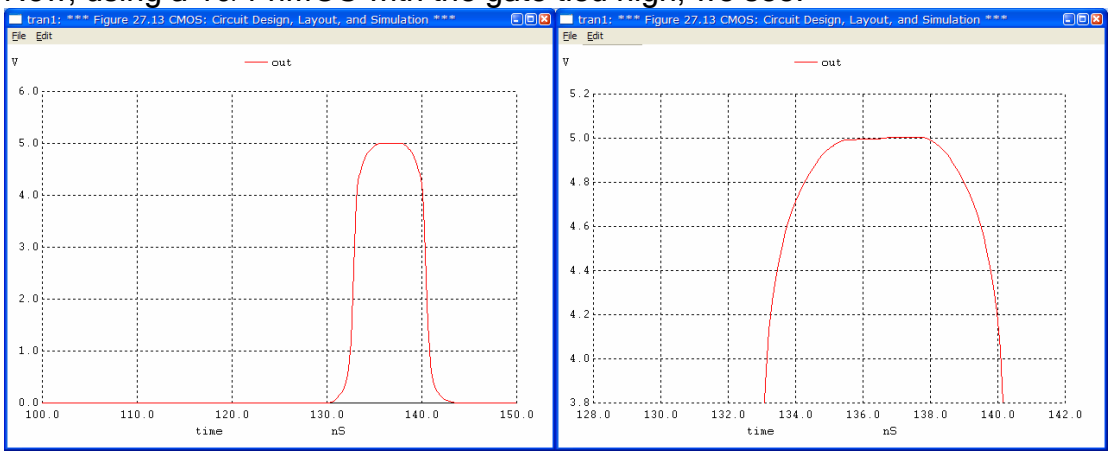
Problem 27.2

Show, using simulations, how the addition of a balancing resistor in Fig. 27.14 can be used to improve the response seen in Fig. 27.13.

The original response:



Now, using a 10/1 nMOS with the gate tied high, we see:



As can be seen from the right-hand plots, the step response is marginally wider, providing more energy in the output pulse.

Problem 27.3

Simulate the operation of the comparator in Fig 27.15 in the short channel CMOS process. Determine the comparators sensitivity and kickback noise.

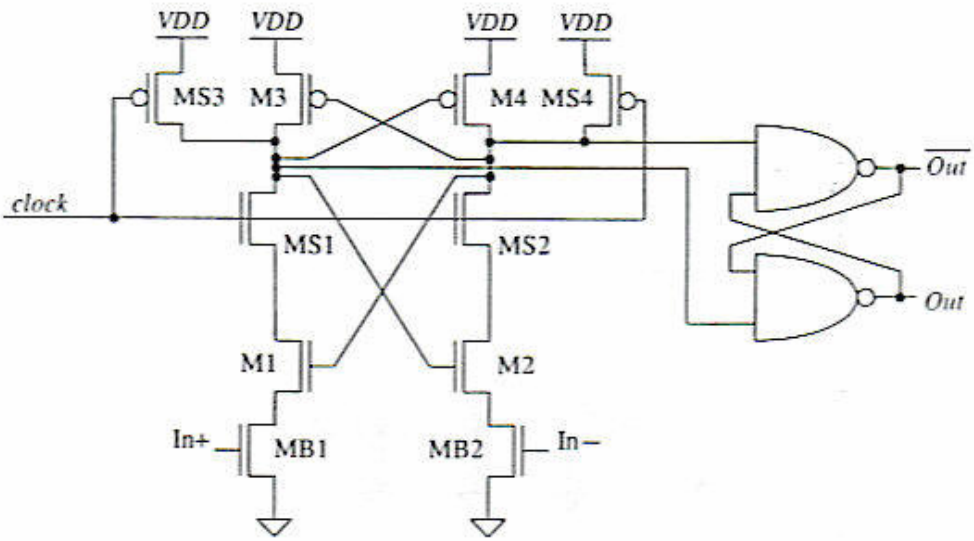
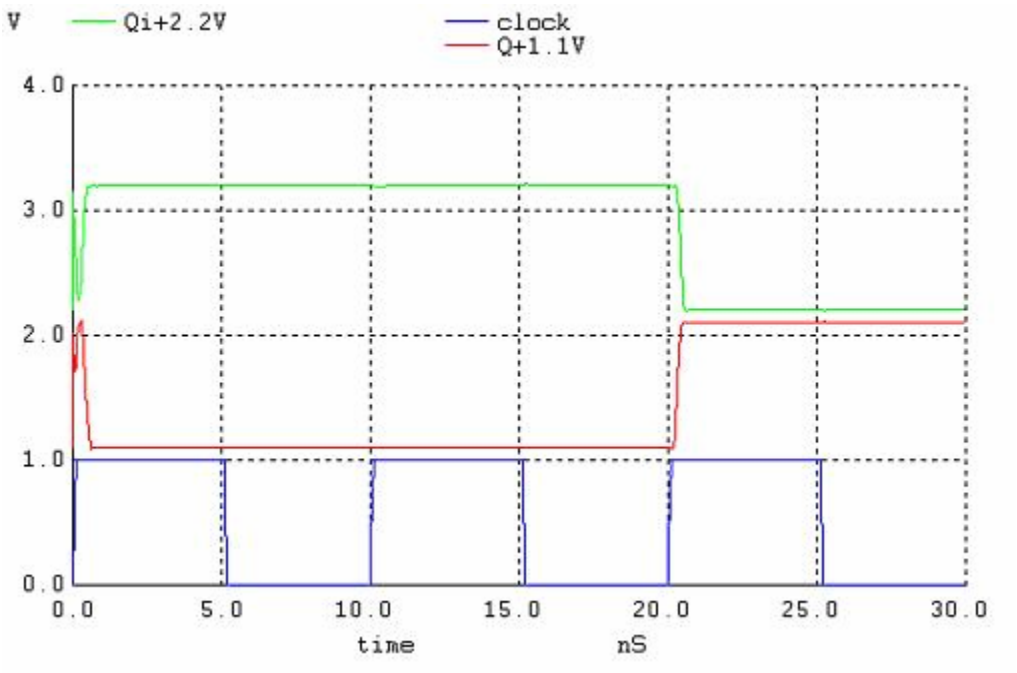


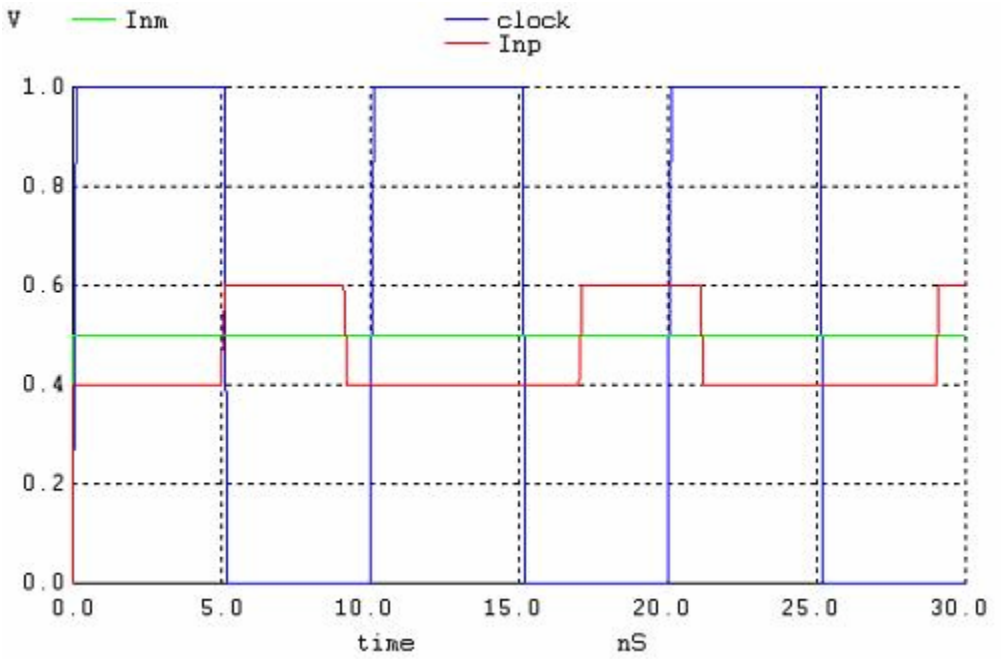
Figure 27.15 A clocked comparator based on Figs. 16.32 and 16.35.

The next two graphs show the general operation of the comparator. You can see from Fig 27.15 that when clock is low, the outputs of the diff amp are pulled to VDD. This causes the outputs to hold the desired value and also charges the output nodes to a known value before the sense. Transistors M1 and M2 fully turn on also when clock goes low causing all nodes to be at a known state unless the inputs are less than the threshold voltage.

Outputs Versus Clock

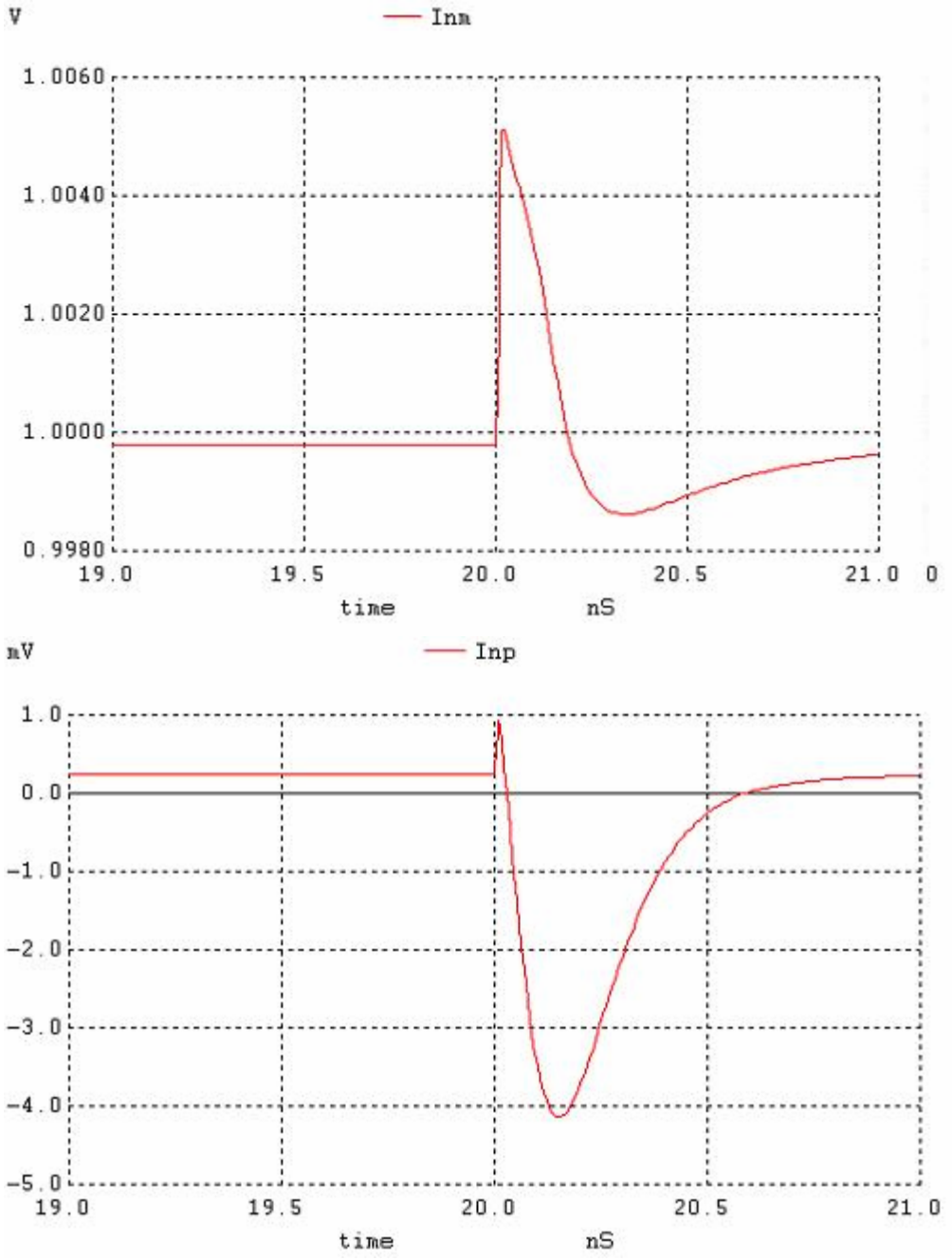


Inputs Versus Clock



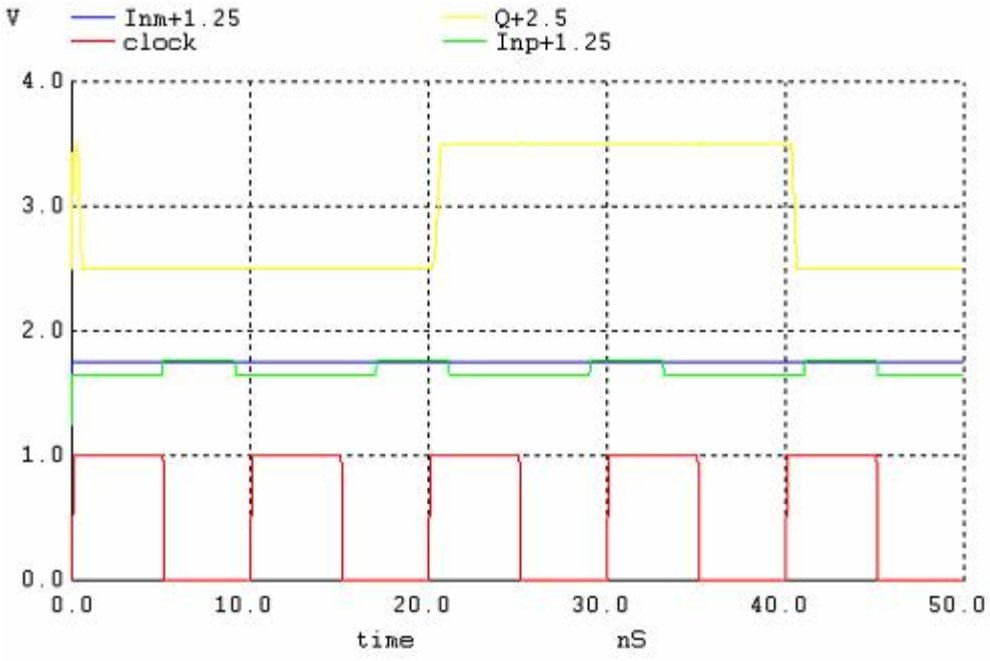
Kickback Noise:

In order to simulate the kickback noise non-ideal sources must be used. The next two graphs were generated using long L inverters to drive the comparator inputs. An example of this technique can be found on page 16-17 Fig 16.28. The kick back noise is around 5mV.



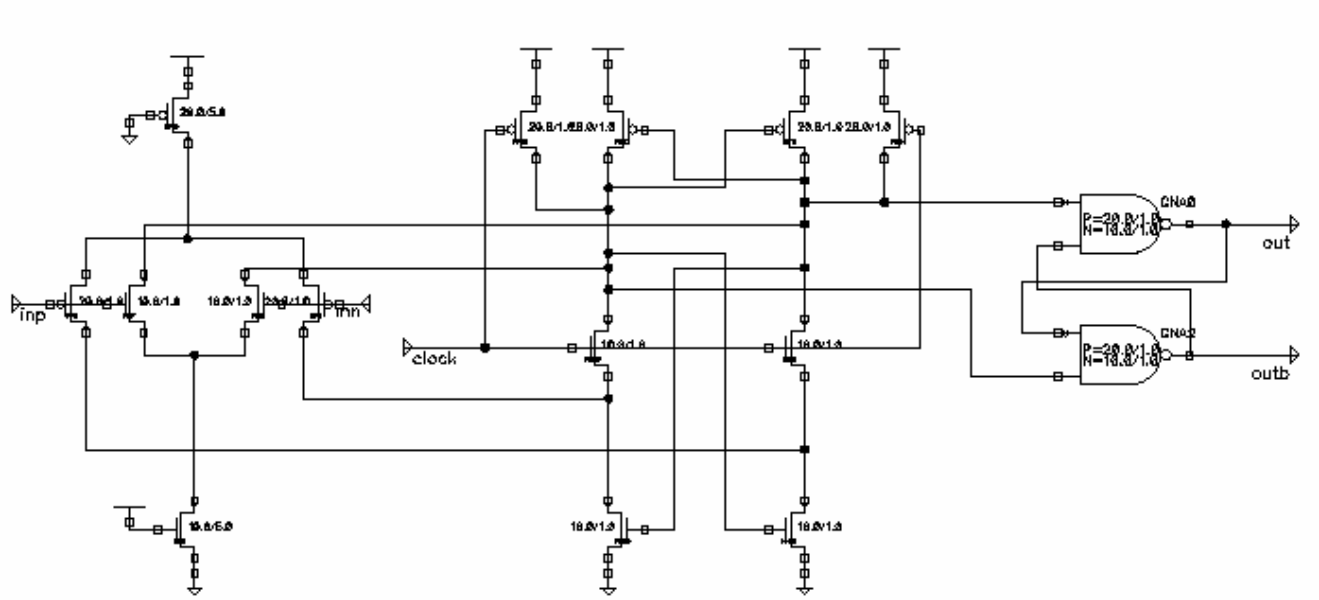
Sensitivity:

Shown is the smallest signal I was able to resolve using the worse case transition. It is around 8mV. I am using a voltage source for my inputs so they are ideal. The capacitances that you are going to need to charge in the Flip Flop are the reason for the sense limitation in this example.

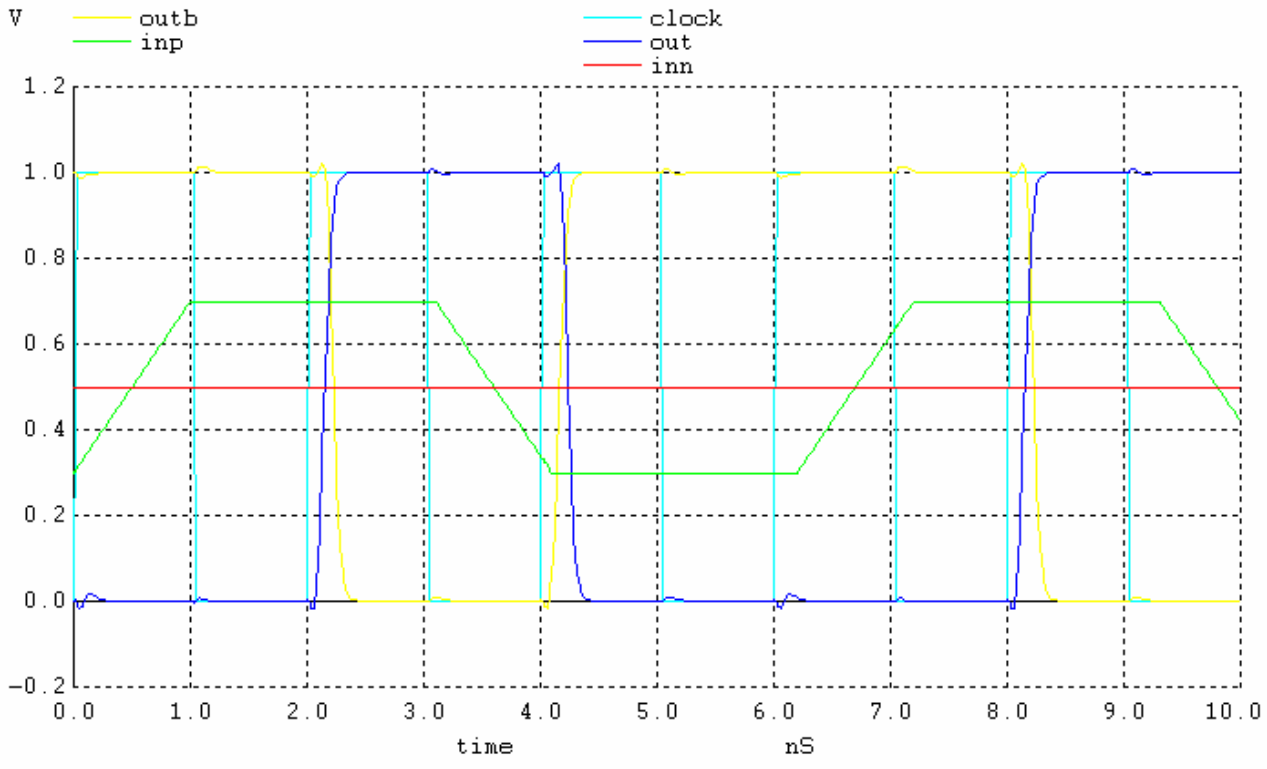

V
Inm+1.25
clock
Q+2.5
Inp+1.25
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
time
nS

EE597 HW 27.4 5

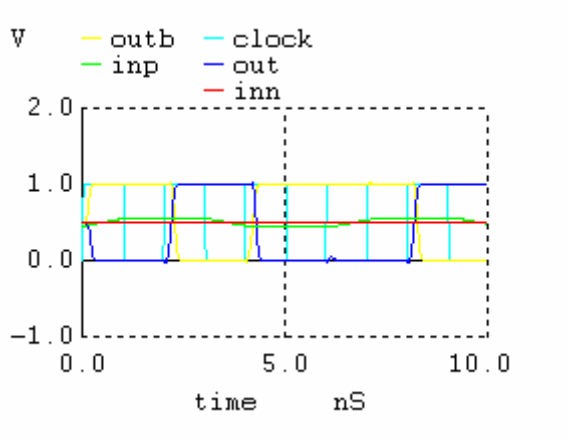
27.4 Repeat the problem of 27.3 for the comparator in Fig 27.16. Show that the input common mode range of the comparator in Fig 27.16 extends beyond the power supply rails.



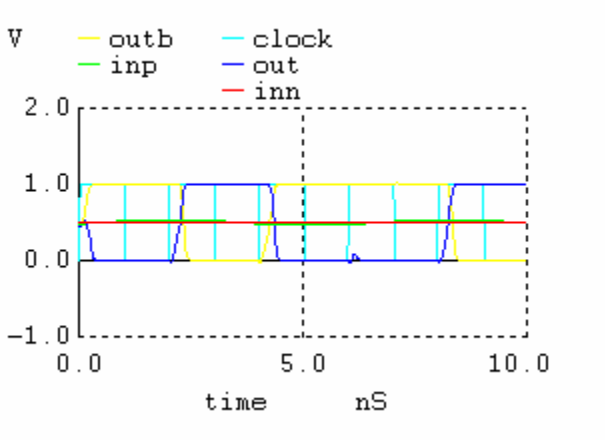
Simulation result:



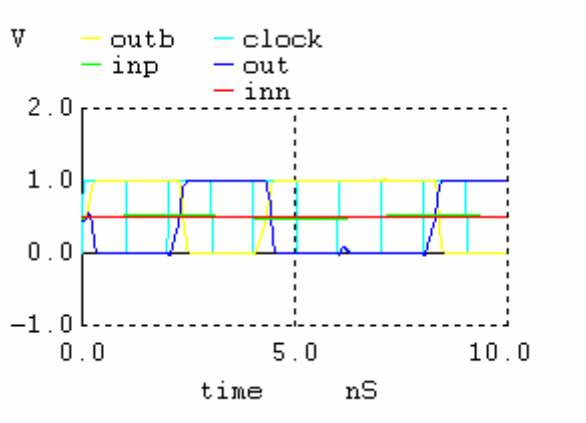
Sensitivity Analysis:



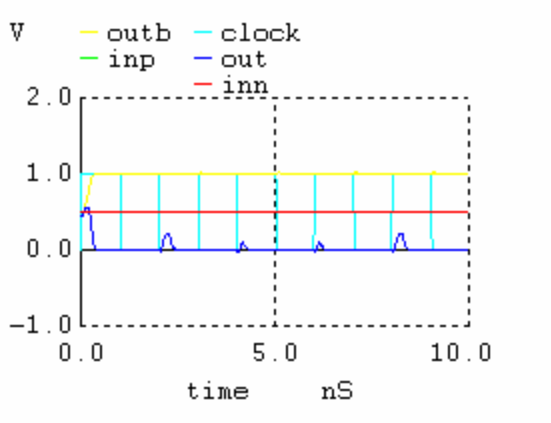
Input is +/-50mV



Input is +/-20mV



Input is +/-15mV

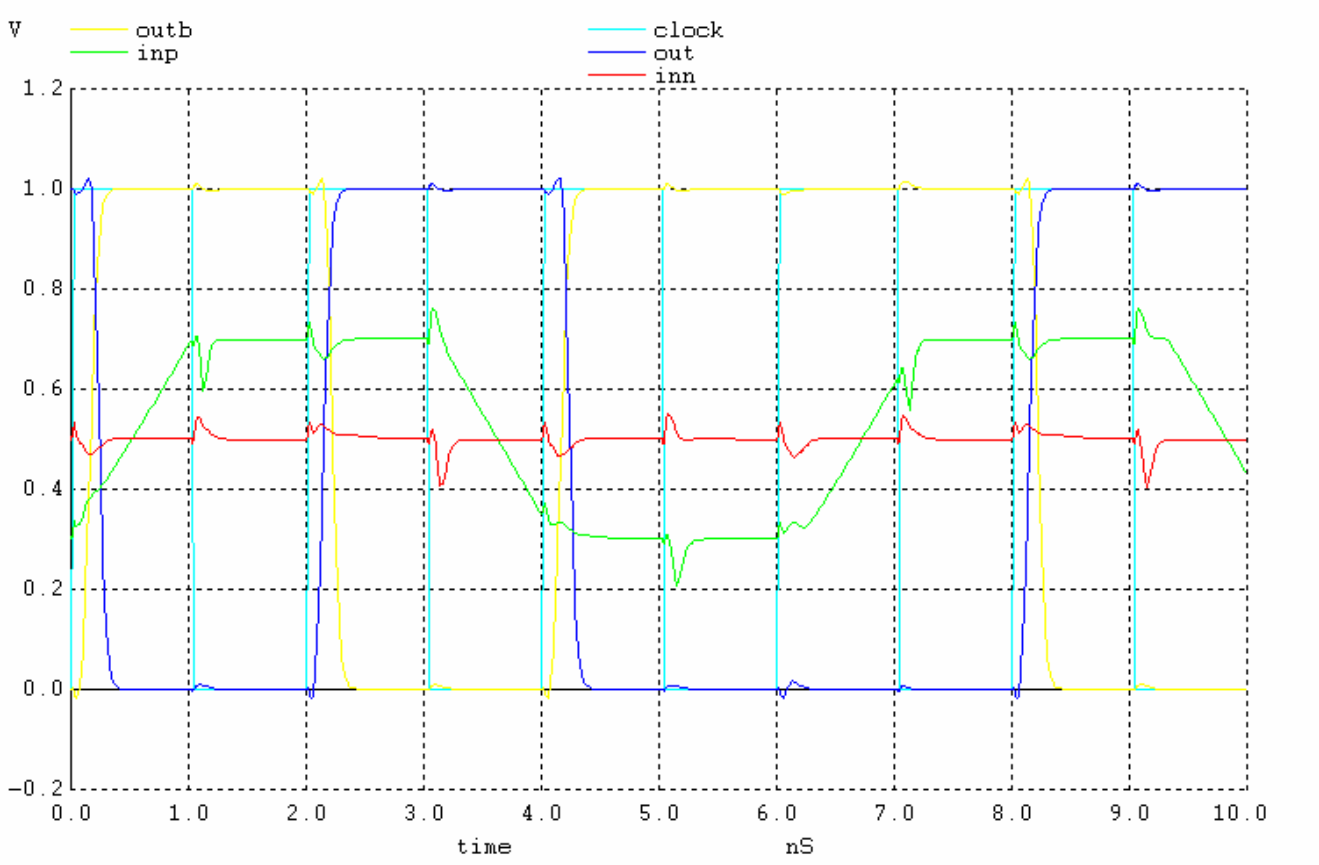


Input is +/-10mV

Sensitivity is about 15mV for this circuit.

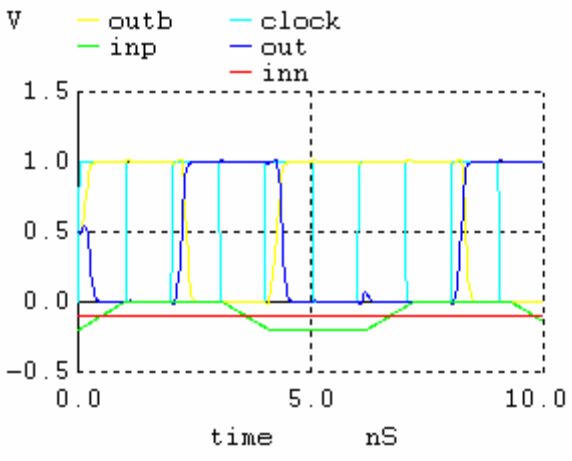
Kickback noise Analysis:

Add 10K ohm resistor at the both inputs.

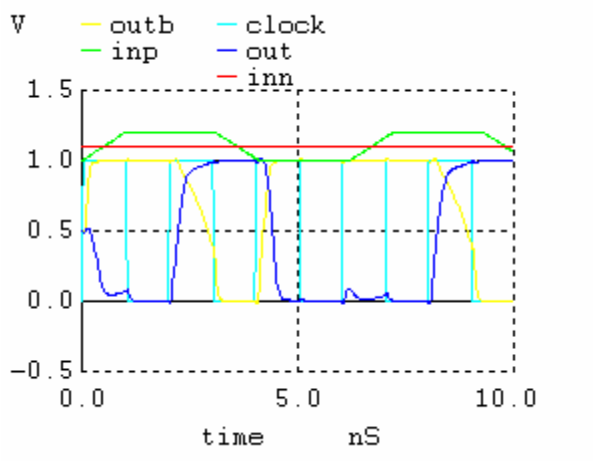


We have kickback noise for about 100mV.

Simulation results as the input common mode voltage extend to over power rails.



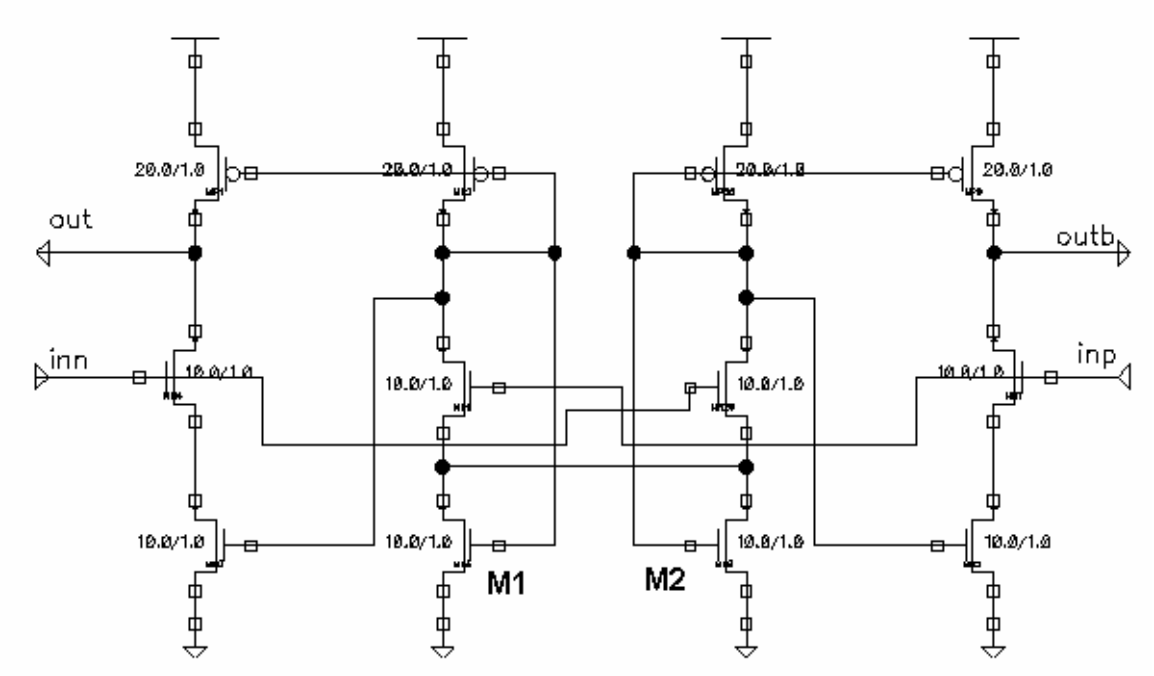
Input common mode = -0.1V



Input common mode = 1.1V

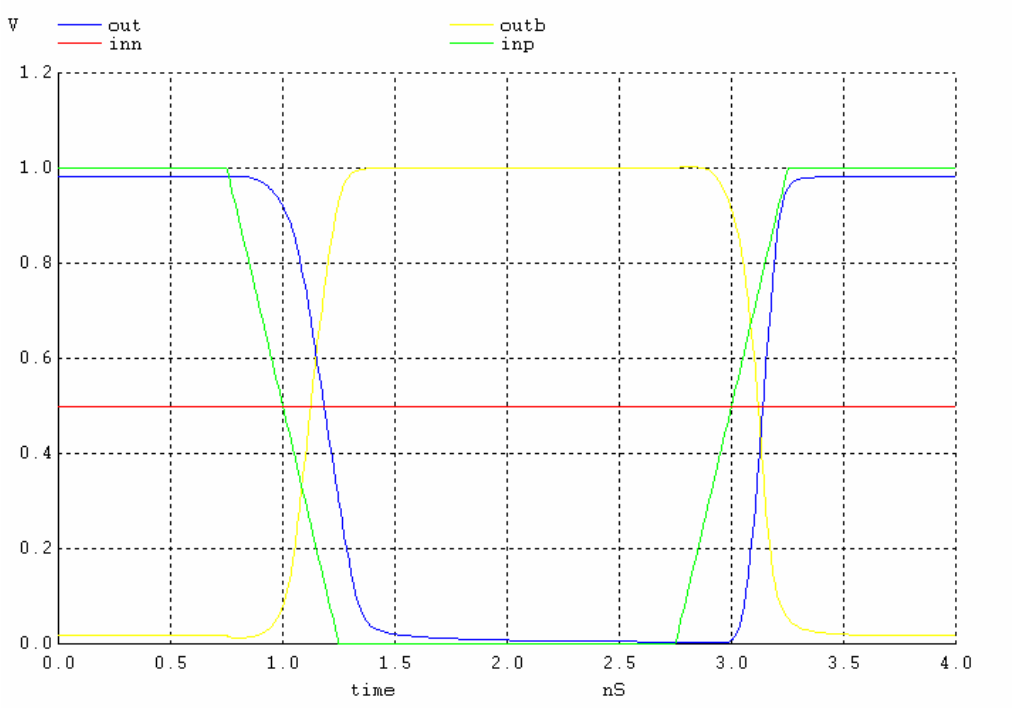
27.5 Simulate the operation of the input buffer in Fig 27.17 in the short channel CMOS process. How sensitive is the buffer to the input slew-rate? How symmetrical are the output rise and fall-times? Suggest, and verify with simulation, a method to reduce the power consumed by the input buffer.

Circuit diagram:



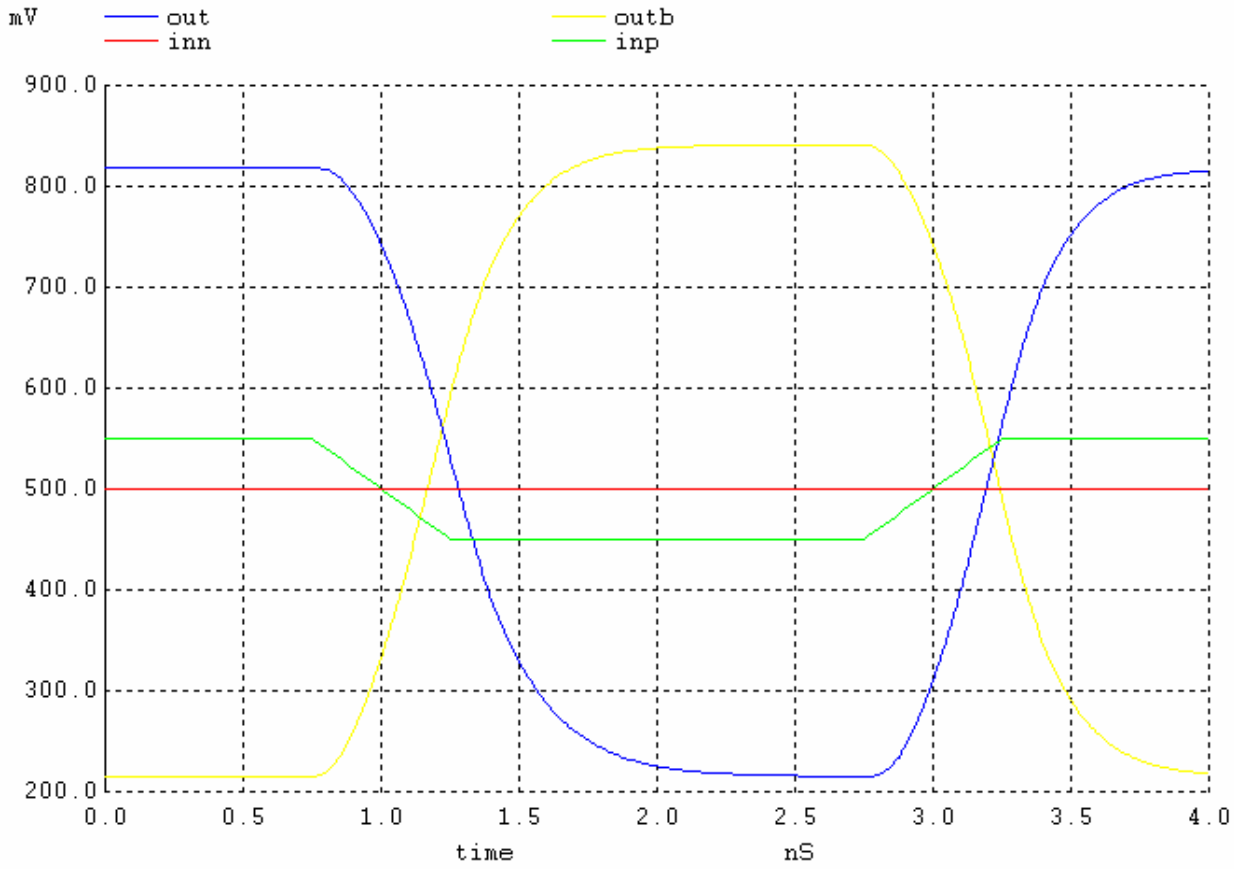
- All the NMOS size= 10/1. All the PMOS size = 20/1

Simulation result with input slew rate =2 V/ns. Input low =0V, input high =1V



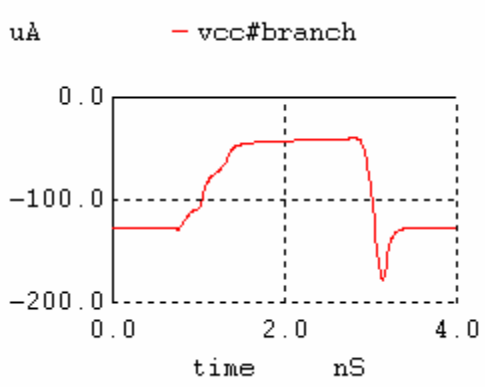
The delay time of the inp is rising =140 ps while the inp is falling =200 ps. (assume the OUT node reaches VCC/2) Almost Symmetrical.

Simulation result with input slew rate =0.5 V/ns. Input low =4.5V, input high =5.5V

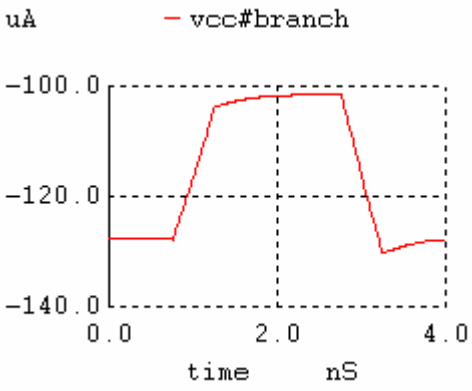


The delay time of the inp is rising =200 ps while the inp is falling =280 ps. At the same time, the output swing is reduced.

Method to reduce the current:
Change the M1 and M2 size from 10/1 to 10/4.

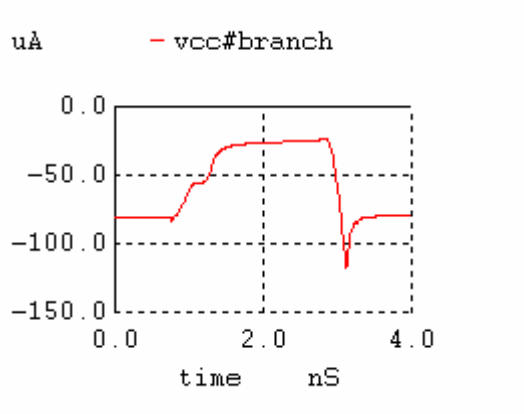


Current of the original circuit (Wide input swing)

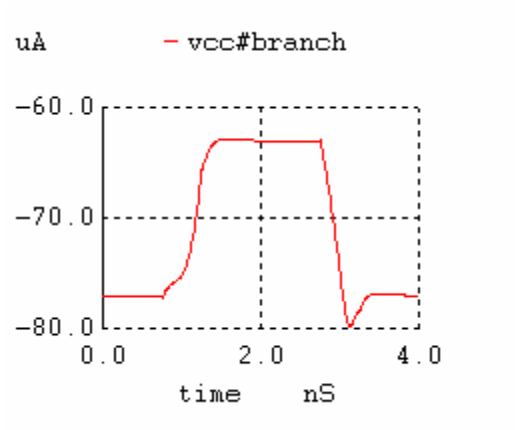


Current of the original circuit (Tight input swing)

New circuit reduces the current about 30% - 40% .

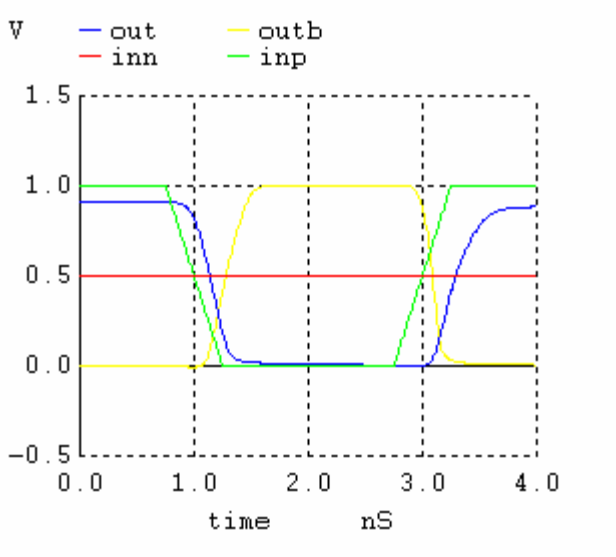


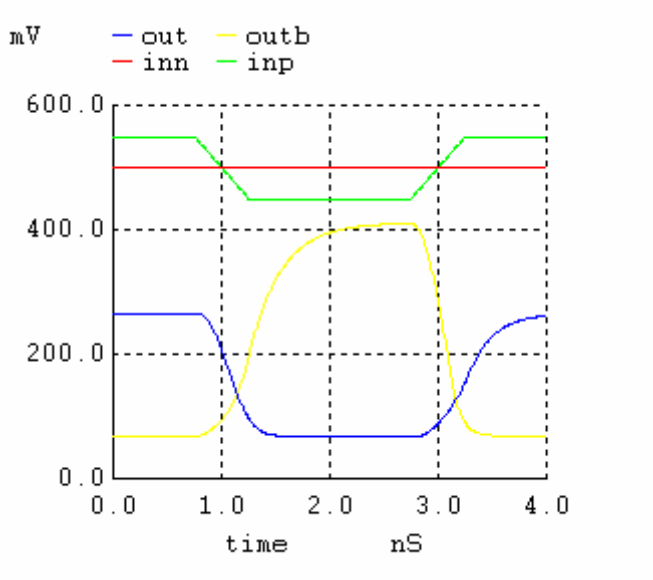
Current of the new circuit (Wide input swing)



Current of the new circuit (Tight input swing)

However, the output swing become worse with reduced current.





Output of the new circuit (Wide input swing)

Output of the new circuit (Tight input swing)

Problem 27.6

Design a lower power clocked comparator for use with a Flash ADC (discussed in Ch. 29). Using the short channel CMOS process and a clocking frequency of 250 MHz, estimate the power dissipated by 256 of these comparators.

The Flash ADC will require that I have a wide input swing. I could develop different comparators based on the different reference values I need but I am just going to show a comparator that will work in general for all references. My design is going to be based on the comparator in Figure 27.16.

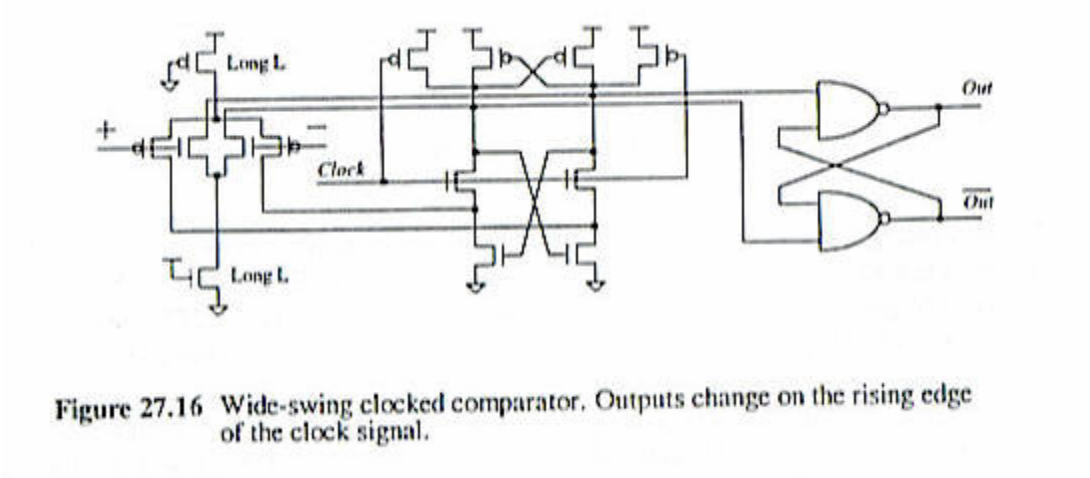
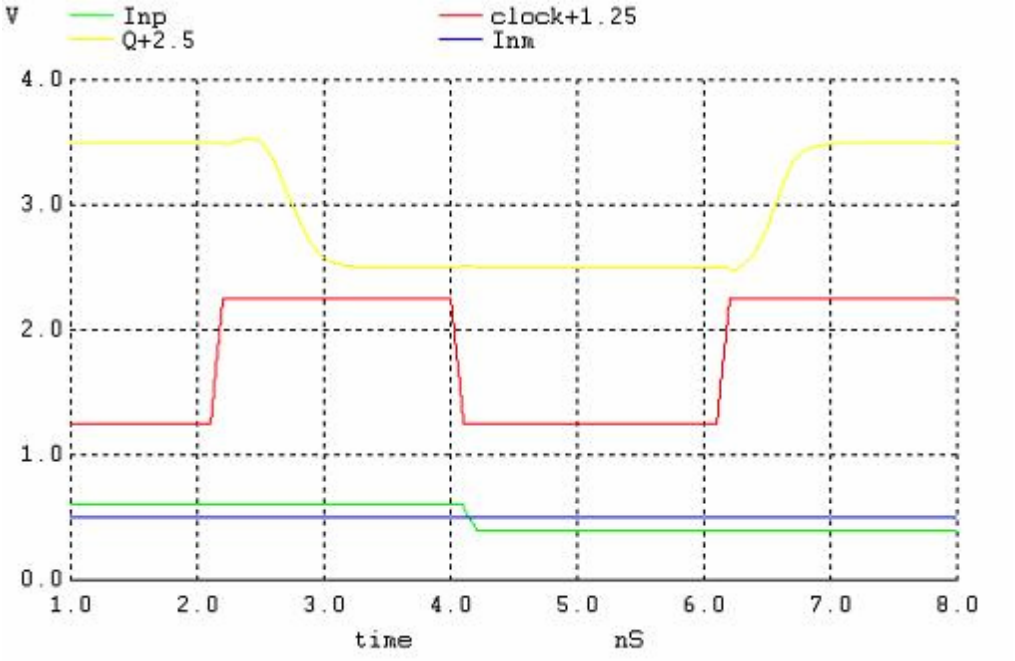
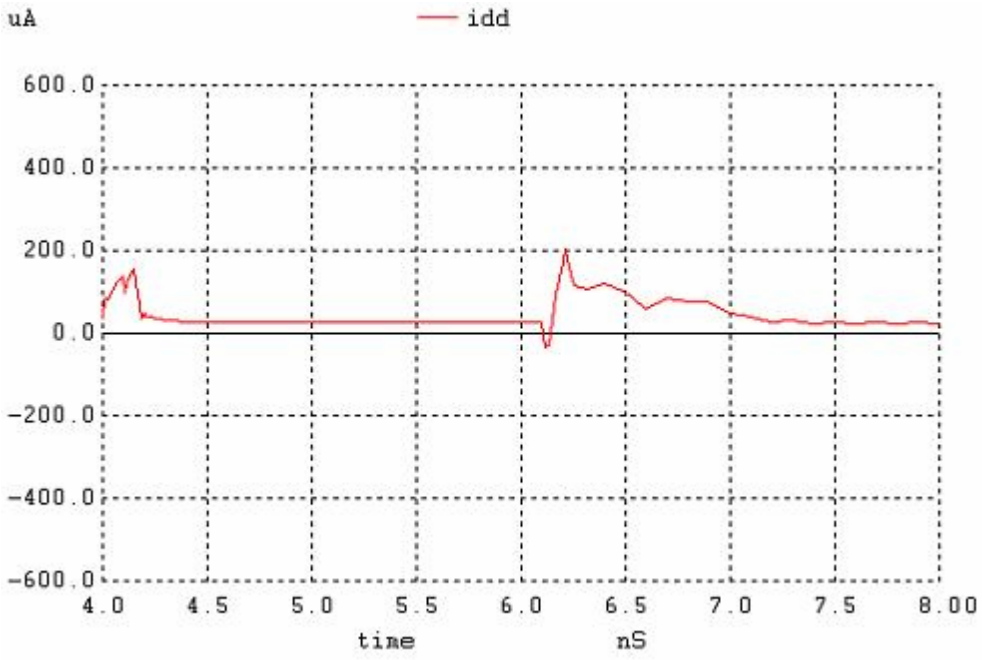


Figure 27.16 Wide-swing clocked comparator. Outputs change on the rising edge of the clock signal.

Shown in the next graph is just the basic operation of the wide swing comparator of Figure 27.16.



To get a 250MHz clock cycle you need to use a period of 4ns. The next graph shows the current consumption. At 4ns clock goes high and the output drives to the desired value. At 6ns the clock goes low and conditions all the nodes to known states. The amount of current that is still being drawn is due to the Long L devices. The real benefit of this design is the low current pull when the data is not being sensed. The average current usage of this device turns out to be around 100.0 uA.



Power for 256 Comparators:

256 * 100 uA = 25.6 mA

Spice:

*** Problem 27.6 *****

```
.control
destroy all
run
let idd = -vdd#branch
plot idd
plot clock+1.25 Inp Inm Q+2.5
print mean(idd)
.endc


.option scale=50n

.tran 100p 50n 0 100p UIC

VDD     VDD     0       DC      1
Vinp    Inp     0       DC      0       PULSE .4 .6 0n 0 0 4n 8n
Vinm    Inm     0       DC      .5
Vclock  clock   0       DC      0       PULSE 1  0 0 0 0 2n 4n

M1      d1      Outp    0       0       NMOS L=1 W=10
```

```
M2      d2      Outm    0       0       NMOS L=1 W=10
M3      Outm    Outp    VDD     VDD     PMOS L=1 W=20
M4      Outp    Outm    VDD     VDD     PMOS L=1 W=20

MS1     Outm    clock   d1      0       NMOS L=1 W=10
MS2     Outp    clock   d2      0       NMOS L=1 W=10
MS3     Outm    clock   VDD     VDD     PMOS L=1 W=20
MS4     Outp    clock   VDD     VDD     PMOS L=1 W=20
```

*** diff amp portion ***

```
MB1     Outp    Inp     n1      0       NMOS L=1 W=10
MB2     Outm    Inm     n1      0       NMOS L=1 W=10
MB3     d1      Inp     n2      VDD     PMOS L=1 W=20
MB4     d2      Inm     n2      VDD     PMOS L=1 W=20

** Long L's ***

MLP     n2      0       VDD     VDD     PMOS L=10 W=20
MLN     n1      VDD     0       0       NMOS L=10 W=10

X1      Outp    Q       Qi      VDD     Nand
X2      Qi      Outm    Q       VDD     Nand

.subckt Nand A B ANANDB VDD
M1      ANANDB A        d2      0       NMOS L=2 W=10
M2      d2      B       0       0       NMOS L=2 W=10
M3      ANANDB A        VDD     VDD     PMOS L=2 W=20
M4      ANANDB B        VDD     VDD     PMOS L=2 W=20
.ends


* 50nm BSIM4 models
*
* Don't forget the .options scale=50nm if using an Lmin of 1
* 1<Ldrawn<200   10<Wdrawn<10000 Vdd=1V
* Change to level=54 when using HSPICE
```