9.1) ***What is a time-interleaved data converter? Why is a time-interleaved converter different from the K-Delta-1-Sigma converter seen in Fig. 9.4? Sketch the implementation of a time-interleaved data converter implemented with Delta-Sigma modulators. Also sketch the clock signals used in the topology.***

Solution)

Time-interleaved, poly-phase or multi-rate signal processing data converters employ multiple data-converters connected in parallel clocked at different clock phases. Let's look at a single path noise-shaping modulator and its noise transfer functions first and we will build up to a K-path time-interleaved data converter.

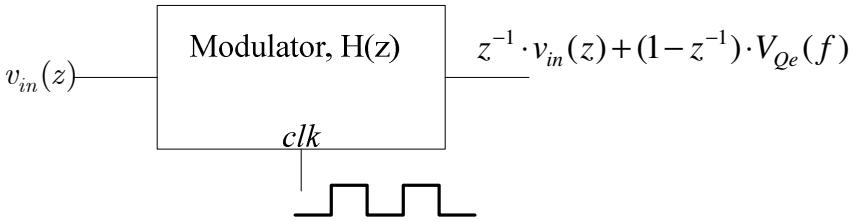


Figure 1: Single Path NS Modulator

A Single path NS modulator is clocked at a sampling frequency of say f_s=100MHz. The NS modulator when implemented using switched-capacitors has an input/output relationship given by,

$$v_{out}(z) = z^{-1} \cdot v_{in}(z) + (1 - z^{-1}) \cdot V_{Qe}(f)$$

The STF is just a one clock cycle delay, while the NTF shows that the quantization noise is differentiated. The magnitude response of the noise is just a response of a first order digital differentiator, as seen in Fig.2.

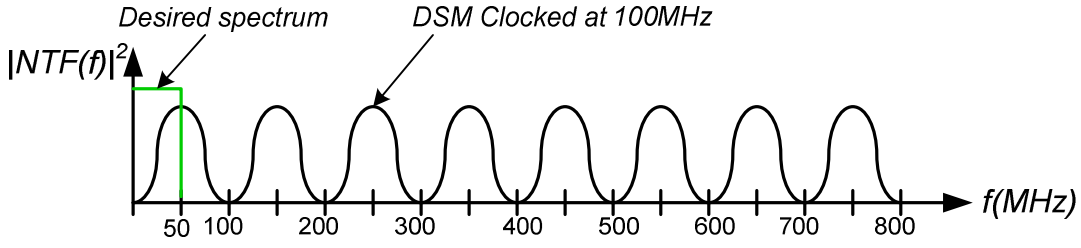


Figure 2: NTF of the NS Modulator from Fig.1 clocked at 100MHz

The spectral content repeats itself at every f_s, as it is a discrete-time system and its frequency response repeats with the sampling frequency.

Fig.3 shows the quantization noise power spectral density, where all the quantization noise is assumed to fall in the frequency spectrum of interest.

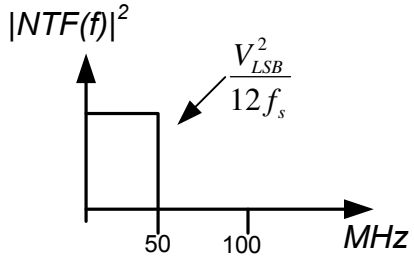


Figure 3: Quantization Noise Power Spectral Density (PSD)

Next, let's move to a 8-path time-interleaved NS data converter. Eight of the single path NS modulators shown in Fig.1 are used in parallel, where each modulator is clocked at f_s but with clocks that are shifted in time. The resulting topology is seen in Fig.4.The equivalent circuit of the topology shown below, is effectively clocked at a high clock frequency of $K_{path}.f_s$.

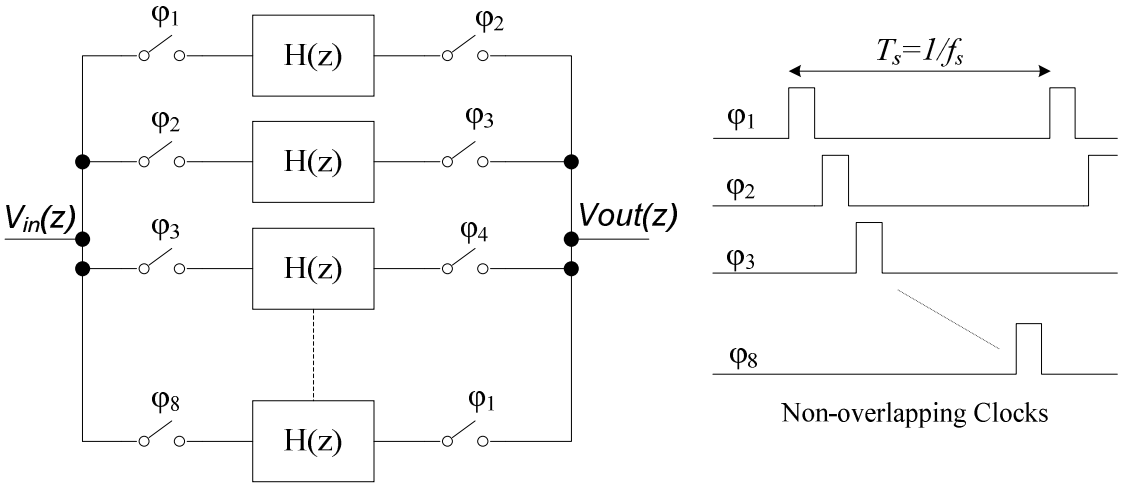


Figure 4: 8-path Time Interleaved Topology, also shown are the clock signals used to clock the various paths

The NTF of this equivalent circuit is given by,

$$H(z^{K_{path}}) = z^{-K_{path}} \cdot v_{in}(z) + \underbrace{(1 - z^{-K_{path}})}_{NTF} \cdot V_{Qe}(f)$$

The power spectral density of the quantization noise is now spread out to higher frequencies as the effective sampling frequency is increased, which also leads to a lowering of quantization noise in the frequency of interest, as shown below. Hence we get an improvement in the SNR using the K-path time interleaved data converters.

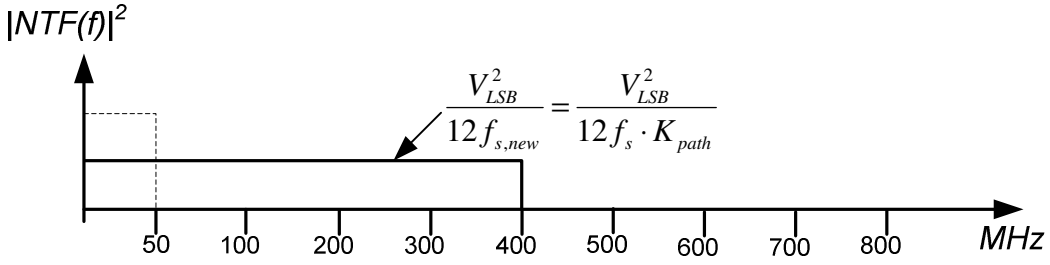


Figure 5: Quantization noise, PSD for the 8-path time-interleaved data converter

As we are using 8-paths, the NTF can be written as, $1 - z^{-8} = 1 - \frac{1}{z^8} = \frac{z^8 - 1}{z^8}$, resulting in a pole-zero plotted in Fig. 6.

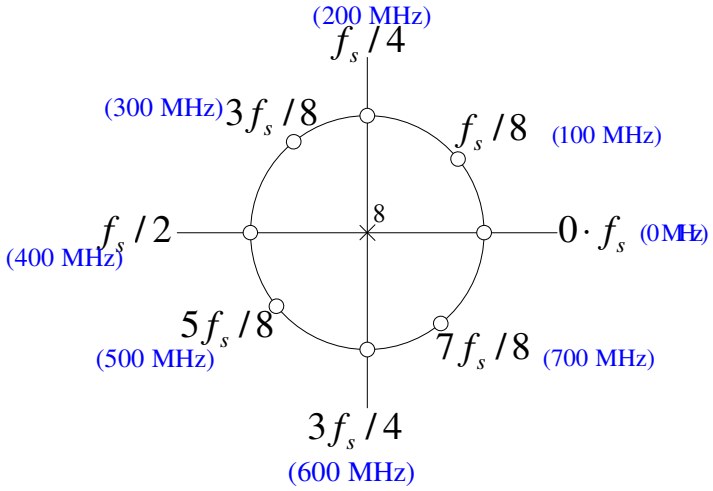


Figure 6: Pole-Zero plot of the NTF for the 8-path Time Interleaved Topology

The modulation noise still repeats itself at the original sampling frequency of 100 MHz as the each path is still being clocked at f_s. And as the power spectral density of the quantization noise is spread out over a larger frequency range, the peak amplitude of the NTF is reduced as shown in the figure below.

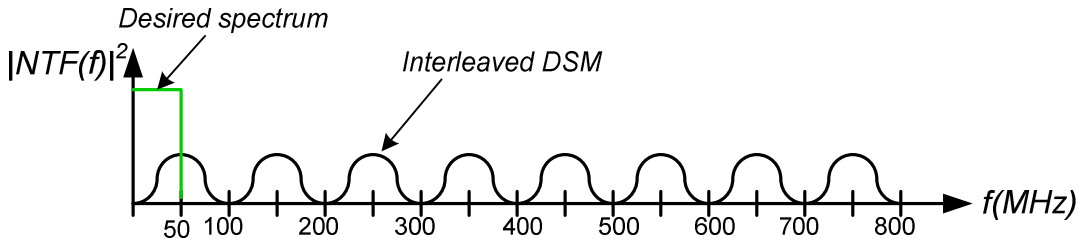


Figure 7: Modulation Noise of the 8-path topology

Therefore, this topology reduces the modulation noise added to our signal in the bandwidth of interest, from DC to 50MHz as shown in Fig.7.We will clearly get an improvement in the SNR using the time-interleaved topology by comparing Fig.2 and Fig. 7.

Now, let's look at the K-delta 1-sigma topology. Here, a single integrator is used to perform the delta from the *K* paths. The high speed sampling is achieved from using the *K*-feedback paths or K-Deltas. Since a single integrator is used, the quantization noise is pushed to high frequencies. The implementation of the K-Delta 1-Sigma is shown in Fig. 8.

In this topology, the modulator is effectively clocked at $K.f_s$ and therefore the noise is pushed out the high frequencies as shown in Fig.9, where the noise peaks at $K.f_s/2$. As this system is still a discrete time topology, the spectrum repeats itself at every $K.f_s$.

Therefore, it should be clear that using the K-delta 1-sigma the noise is removed from the frequency of interest and will result in a SNR improvement greater than the time-interleaved topologies. The noise spectrum comparison of the K-delta 1-sigma and the K-path time-interleaved data converter are shown in Fig. 10.

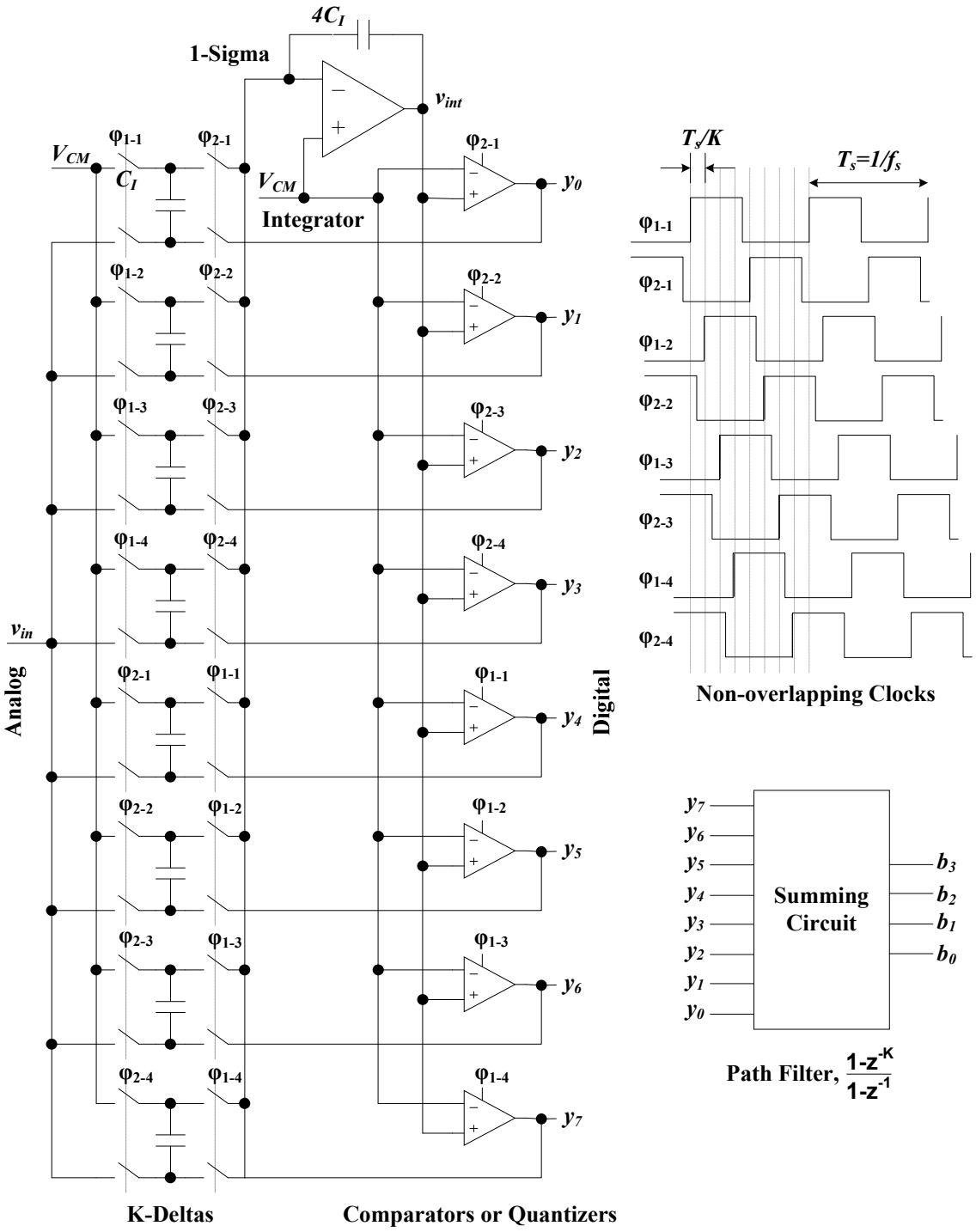


Figure 8: Topology for K-Delta 1-Sigma Data Converter with clock signals

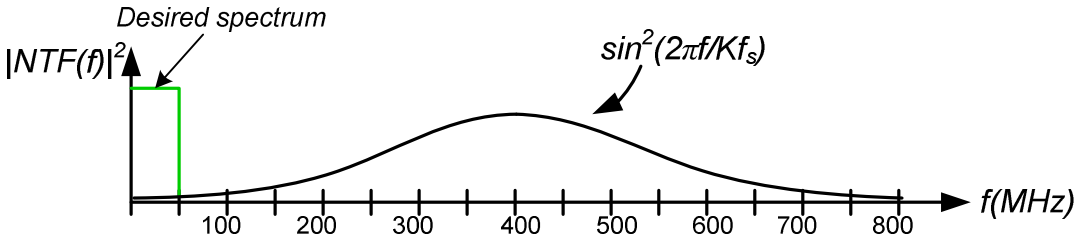


Figure 9: Modulation noise spread for the 8-Delta 1-Sigma Topology

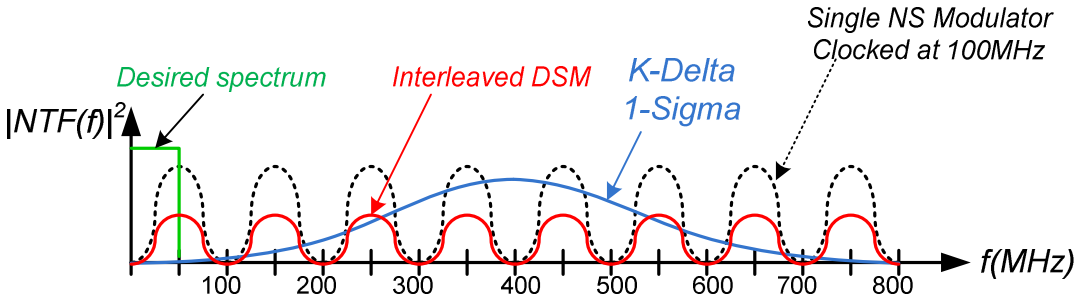


Figure 10: Modulation noise shaping comparisions

The K-Delta 1-Sigma topology leads to better removal of noise from the frequency of interest. The K-path time-interleaved topology reduces the noise amplitude from the frequency of interest, but does not eliminate the noise as effectively as the K-Delta 1-Sigma topology.

Lincoln Bollschweiler

9.2) Using the modulator from example 9.2 show that capacitor matching isn't important in the K-Delta-1-Sigma topology.

In order to modify the circuit that was found on CMOSedu.com (Fig9.4 no path filter v1 MSD) for the circuit discussed in example 9.2 four steps were taken: 1 – drop down into the switched capacitor cell and remove the capacitor; 2- add pins to the schematic and to the symbol where the capacitor connected to; 3- go to the top level schematic and replace the old symbols with the new one; 4 – place capacitors of various sizes (within 1%) on the switches. 1% was chosen because "capacitor matching should easily be better than 1% so the worst-case mismatch is a capacitor with a value of 99 fF or 101 fF"[1]. The actual values chosen were 100.0f, 100.6f, 100.2f, 99.8f, 99.8f, 99.7f, 100.0f, and 99.9f, which average to 100.0fF.

The updated symbol and schematic are shown in Figs. 1 and 2. The new version of the top level schematic is seen in Fig. 3.

The spice simulations show no appreciable difference. These can be seen in Figs. 4 and 5. Running through the MATLAB analysis (also found on CMOSedu.com) we find, for the ***original version: BW = 6.25 MHz; SNR = 58.8dB; and Neff = 9.47 bits***. For the ***modified version with capacitor mismatches: BW = 6.25 MHz; SNR = 56.6 dB; and Neff = 9.1 bits***. This is very close to the ideal situation. The reason these mismatched capacitances have little affect on the performance is due to the averaging effect of the K-paths. "The variance of the capacitor mismatch is divided by Kpath" [1].

Trying to push the envelope, another simulation was run with a slightly wider swing on the capacitor mismatch vales. This time the following values were used: 100.0f, 101.0f, 100.2f, 99.8f, 99.5f, 99.0f, 100.0f, and 100.5f, with the following results: ***BW = 6.25 MHz; SNR = 56.1; and Neff = 9.0 bits.*** Again, just a few dB less for the SNR than the ideal case. The more paths that are used, the more chance for capacitor mismatch, but at the same time, the more averaging of these mismatches.

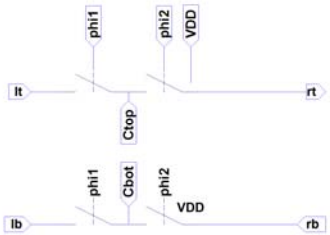


Figure 1. Updated version of SC input 1(sch.)

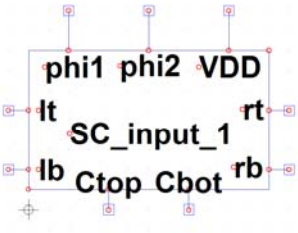


Figure 2. Updated version of SC input 1(sym.)

[1] Jake Baker, personal email to author, 2009.

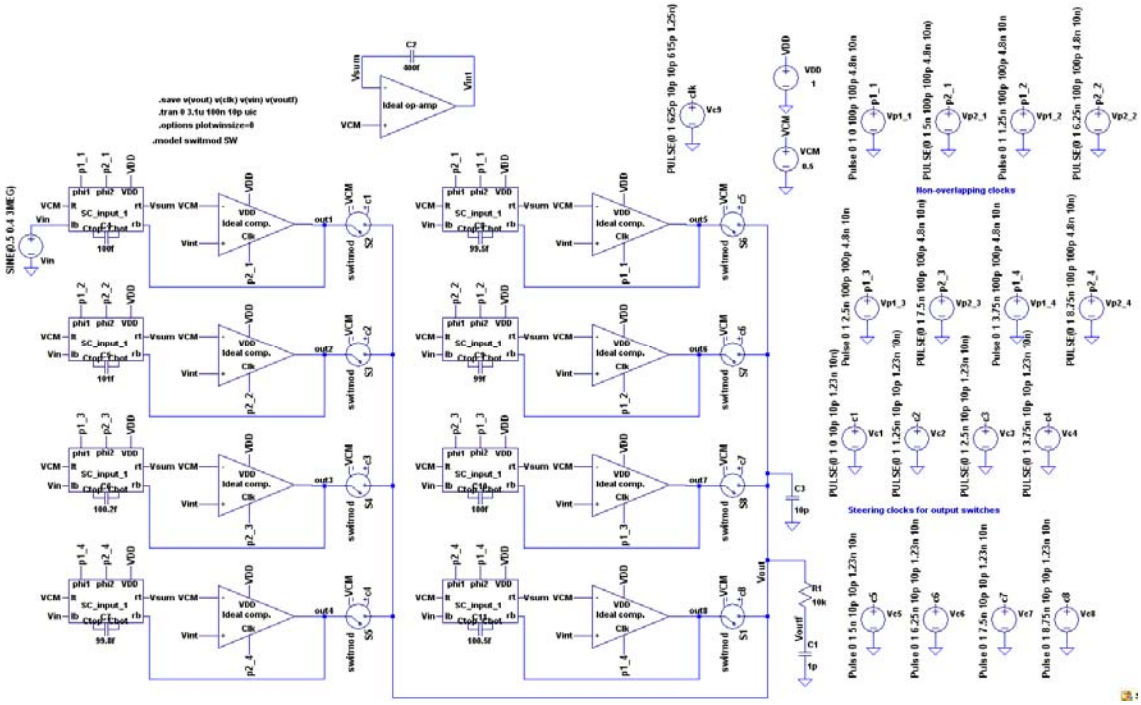


Figure 3. Copy of Fig9.4 no path filter v1 MSD circuit from CMOSedu.com, updated with capacitors ranging in value from 99.7fF to 100.6fF for test 1 and 99fF to 101fF for test 2.

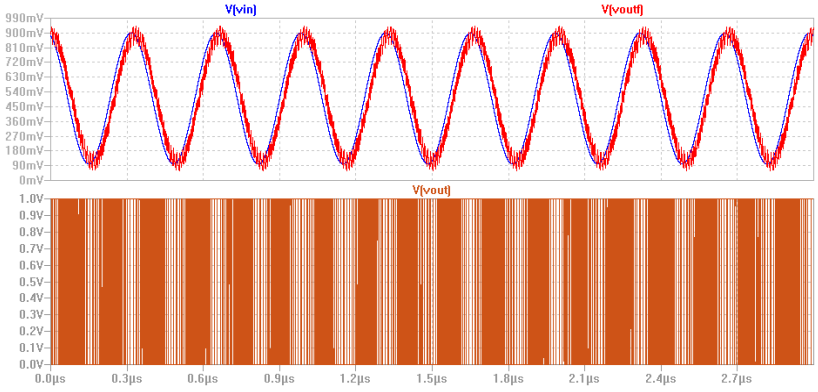


Figure 4. SPICE sim for ideal, unaltered version.

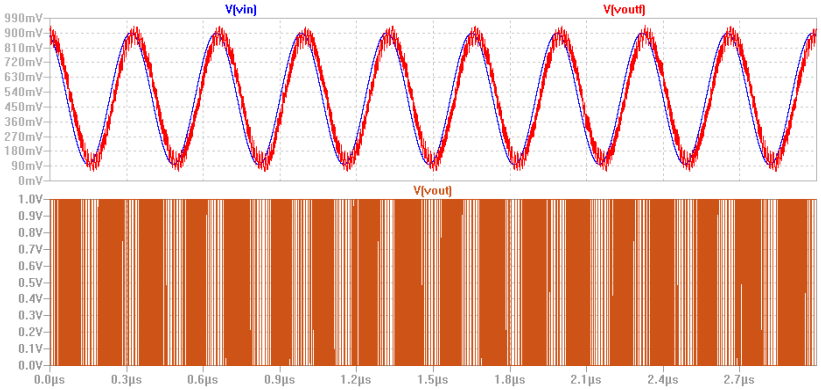
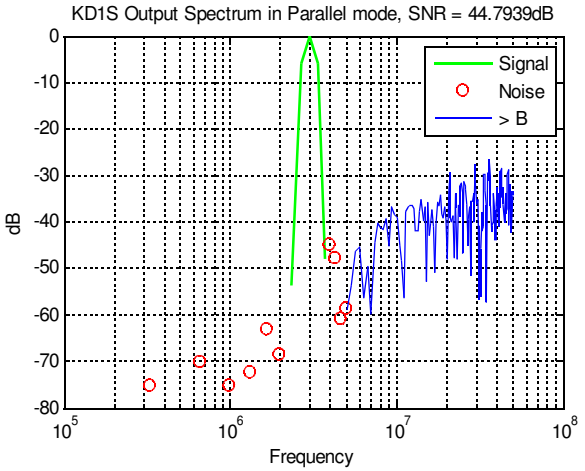


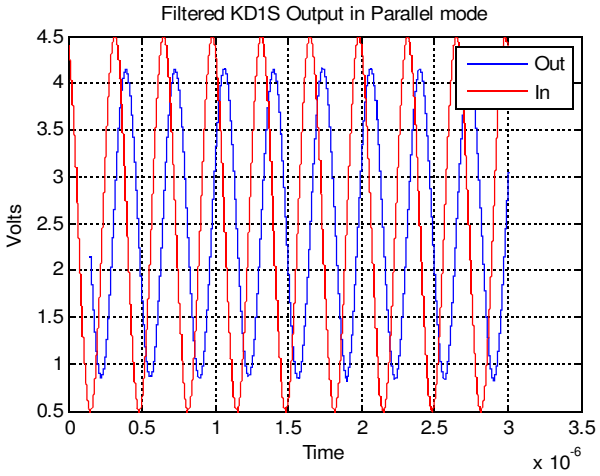
Figure 5. SPICE sim for mismatched capacitors version.

Jason Durand

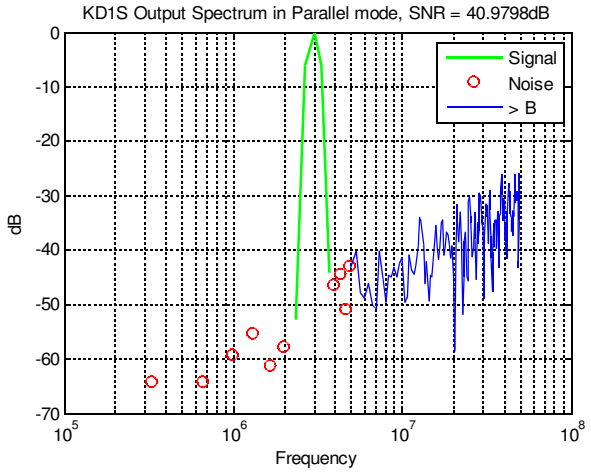
Problem 9.3 – Using the modulator from example 9.1, show that the open loop gain of the amplifier used in the integrator isn't critical.

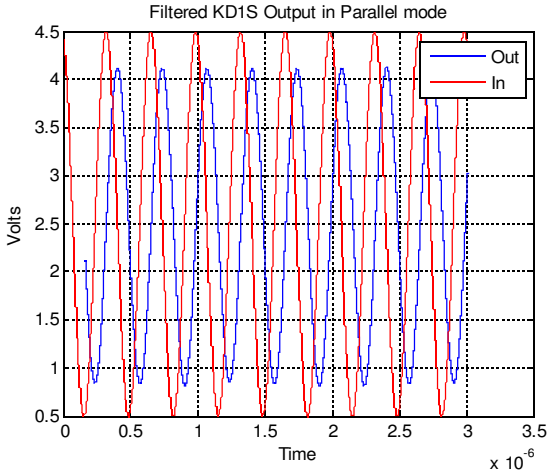
Fig 9.4 in CMOS, Mixed Signal Circuit Design is made of near-ideal components, with the amplifier having an open-loop gain of one million. With the near ideal components and an input frequency of 3MHz, (nearly the signal bandwidth), the output signal and spectrum are pictured below.





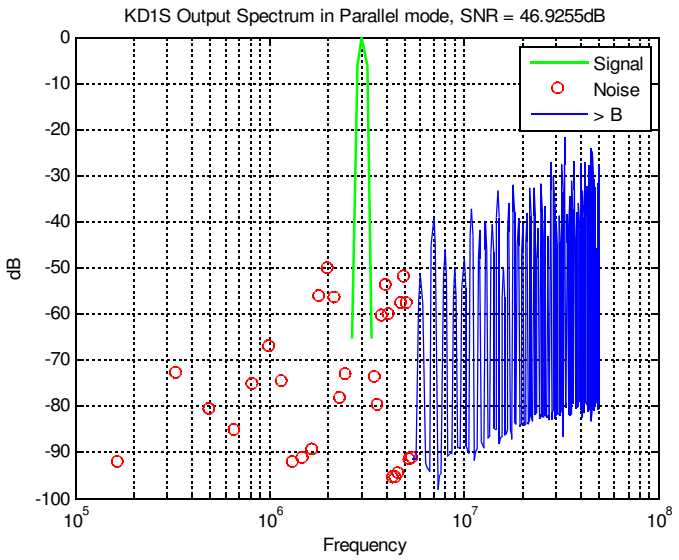
Using the decimation filter that simply adds all the outputs together every $1/f_s$ and ideal components, the SNR is 44.8dB, or 7.15 effective bits. Now, lets try it with a integrator that has significantly less gain.





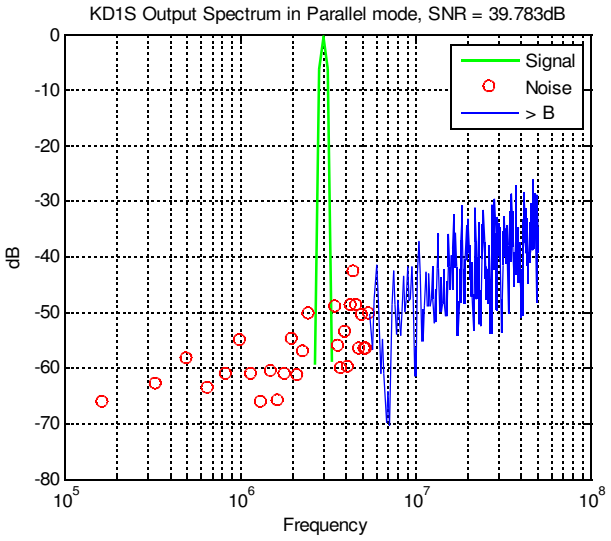
The spectrum and output above is the same modulator and filter as before, except the open loop gain of the integration opamp is 100. This is quite low, and while it had an effect of the SNR, the difference in complexity between an opamp with a gain of 100 and a gain of 1,000,000 is much bigger. The output SNR is now 41.0dB, or 6.51 effective bits. To try once more, lets reduce the open loop gain of the integrator down to 10. Simulations follow:

Spectrum with $A_{OL} = 10$

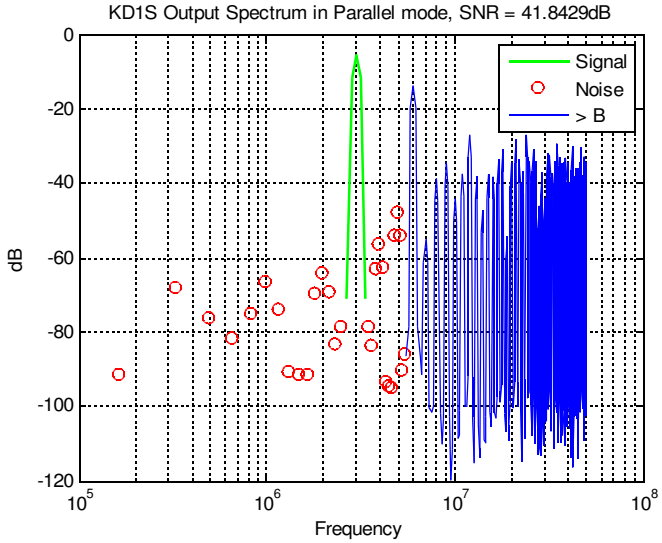


The SNR of this simulation is even higher than the original, but that might have to do with simulation accuracy, or the use of ideal components in the other parts of the simulation (eg. the comparators are also ideal). Whatever the cause, it shows that the open loop gain of the op-amp is not critical to the operation of the circuit.

Spectrum with $A_{OL} = 5$



Spectrum with $A_{OL} = 1$



Reducing the opamp gain too much will attenuate the signal, as seen in the final spectrum with $A_{OL} = 1$, but the modulator still continues to function.

Q 9.4 Show the details of (derive from the time-domain outputs of the *K*-Delta-1-Sigma modulator) how the path filter seen in Fig. 9.4 has a *z*-domain transfer function of

$$\frac{1-z^{-8}}{1-z^{-1}}$$

Explain how this filter performs a moving–average filtering of the modulator's outputs. Does this filter decimate the *K*-Delta-1-Sigma outputs? Why or why not?

Sol. Figure 1 below shows Fig. 9.4 (page 304 MSD text book), solution is discussed looking at the figures below

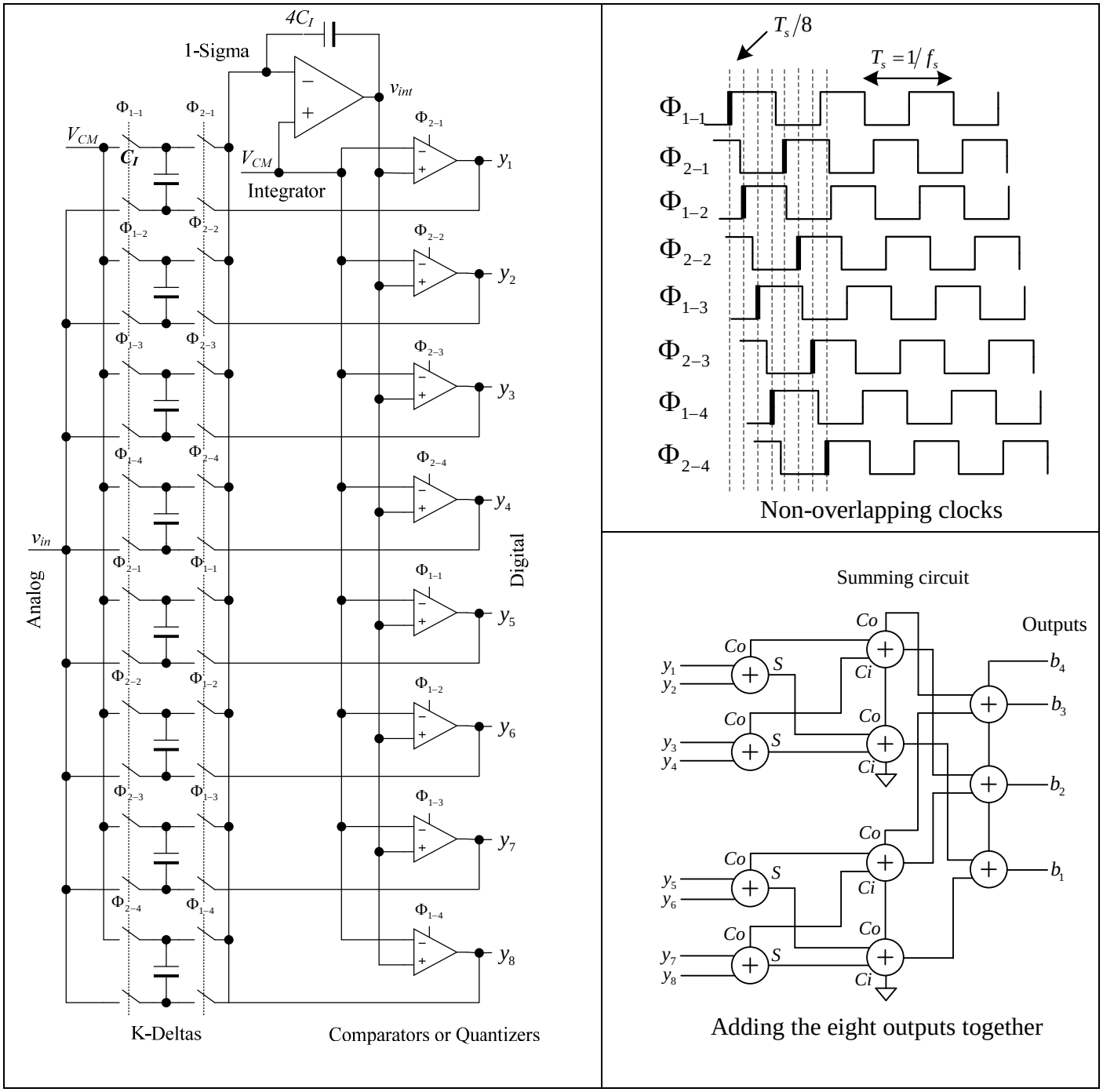


Figure 1 K-Delta-1-Sigma ADC, non-overlapping clocks and the block diagram of summing circuit as path filter

When discussing the path filter it is assumed that the summing block is a high speed digital circuit which can perform logic functions practically at the rate greater than $K \cdot f_s$ where K=8 in this problem. The summing of K-Delta-1-Sigma modulator outputs can be written as:

$$y_{sum} = y_1 + y_2 + y_3 + y_4 + y_5 + y_6 + y_7 + y_8$$

where y_{sum} is the output of summer. Looking at the figure of non-overlapping clocks, the total value y_{sum} is the sum of modulator outputs arriving at different instants of time with $T_s/8$ time between any two output samples. If the first output arrives at the rising edge of the clock Φ_{1-1} through clocked comparator then writing the sum for the outputs of modulators arriving at consecutive clock cycles $\Phi_{1-2}, \Phi_{1-3}, \Phi_{1-4}, \Phi_{2-1}, \Phi_{2-2}, \Phi_{2-3}, \Phi_{2-4}$ as :

$$\begin{aligned} y_{sum}\left[nT_{s,new}\right] = {} & y_5\left[nT_{s,new}\right] + y_6\left[(n-1)T_{s,new}\right] + y_7\left[(n-2)T_{s,new}\right] + y_8\left[(n-3)T_{s,new}\right] + \\ & y_1\left[(n-4)T_{s,new}\right] + y_2\left[(n-5)T_{s,new}\right] + y_3\left[(n-6)T_{s,new}\right] + y_4\left[(n-7)T_{s,new}\right] \end{aligned}$$

Since the magnitude of the samples are same and $T_{s,new} = T_S/8$, y_{sum} can be written in terms of unit delay z^{-1} where once again $z = e^{2\pi f/f_{s,new}}$ and $f_{s,new} = K_{path} \cdot f_s = 8 \cdot f_s$

$$y_{sum} = y \cdot 1 + y \cdot z^{-1} + y \cdot z^{-2} + y \cdot z^{-3} + y \cdot z^{-4} + y \cdot z^{-5} + y \cdot z^{-6} + y \cdot z^{-7}$$

$$\frac{y_{sum}}{y} = H(z) = 1 + z^{-1} + z^{-2} + z^{-3} + z^{-4} + z^{-5} + z^{-6} + z^{-7}$$

Where $H(z)$ simplifies to $H(z) = \dfrac{1 - z^{-8}}{1 - z^{-1}}$, which is equivalent to the output of moving average filter or Low pass Sinc filter which is realized as in Fig.2 and have spectrum shown in Fig. 3

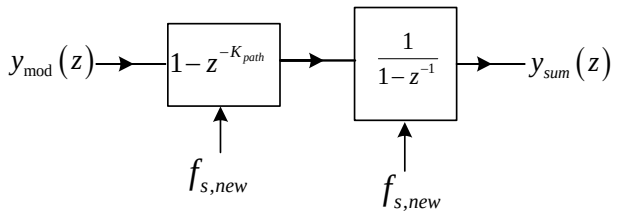


Figure 2 Low pass Sinc filter realized with comb filter and non-delaying integrator ; **aka** *moving average filter*

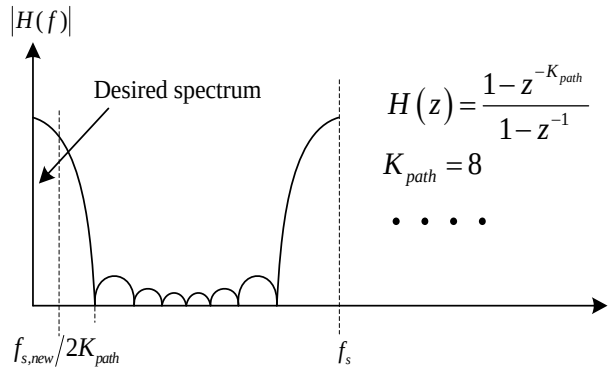


Figure 3 Frequency response of filter

As stated earlier the summing block of the path filter is assumed to perform at faster rate and also the modulator output is being averaged (summed) at effective frequency of $K \cdot f_s$. It can be assumed that the output of summing block is being strobed at the same frequency; $K \cdot f_s$ hence there is **no decimation** at the output of summer. The statement can be argued by comparing it with moving average filter output discussed above.

Solution by Geng Zheng

9.5 Sketch the decimate by $K/4$ topology similar to the topologies seen in Fig. 9.7. Ensure the proper clock signals are used in your sketch.

Solution:

In Ex. 9.2 the clock signal f_s is 100 MHz. The effective sampling frequency is $K_{path} \cdot f_s$ or 800 MHz. Decimating by $K/4$ (or 8/4 =2) results in a final clock frequency of 400 MHz. The decimate by $K/4$ topology and simulation are shown in Fig. 1.

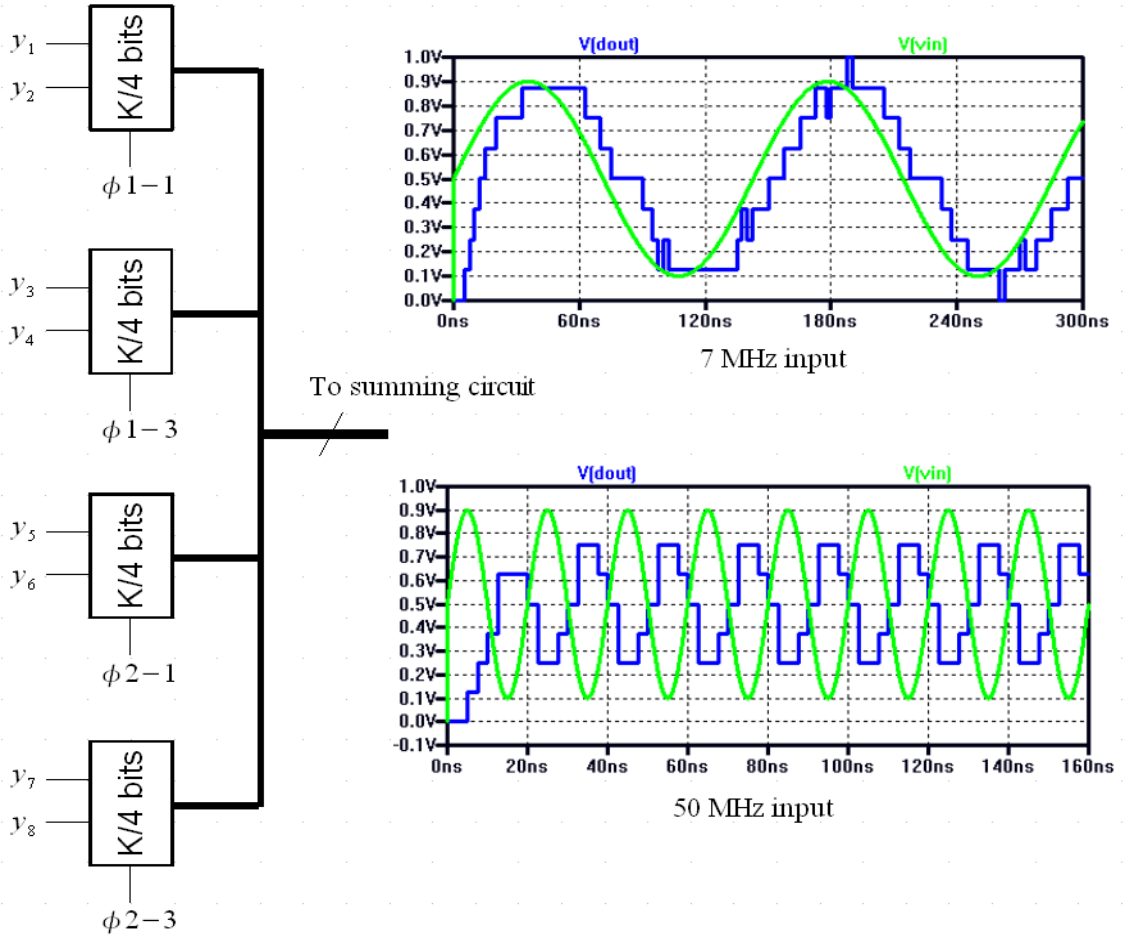
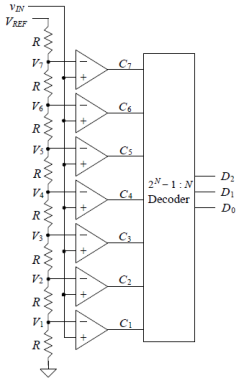


Figure 1 Decimate by K/4 topology.

QAWI HARVARD – ECE615 CMOS Mixed Signal Design

9.6 Explain, in your own words, why oversampling (averaging the output) using a 3-bit Flash converter (eight comparators), won't result in as significant improvement in SNR as the K-Delta-1-Sigma topology.

A 3-bit Flash ADC can be seen in F-1.

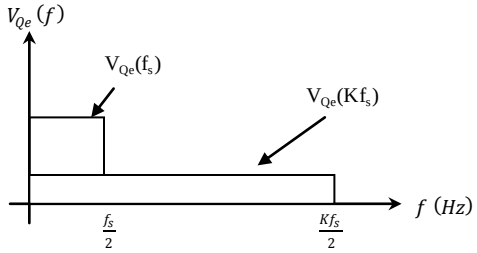


F-1 Schematic of a 3-bit Flash ADC

When oversampling a three bit Flash ADC the voltage spectral density of quantization noise can be estimated as:

$$V_{Qe}(f) = \frac{V_{LSB}}{\sqrt{12 \cdot Kf_s}} \left(V/\sqrt{Hz}\right)$$

The frequency response of the Flash ADC's quantization noise is spread out over the higher clock frequency without being shaped to higher frequencies. F-2 depicts the Flash ADC quantization noise being spread out over higher frequencies.



F-2 Showing the Flash ADC's quantization noise being spread out with oversampling

The K-Delta-1-Sigma (KD1S) topology allows for true noise shaping at the higher clock frequency. The KD1S topology also benefits from the reduced quantization noise due to an increased sampling rate, but also modulates the noise within the conversion band to a higher frequency.

The modulation noise spectral density can be viewed in F-3.

9.7. What is the frequency response (an equation) of the filter seen in Fig 9.10?

Sol. Let us see the frequency response of the cascaded filter shown in Figure 1.
We can see that the final transfer function $H_{eff}(z)$ in z-domain is a multiplication of the transfer functions of the individual filters in the cascaded filter.

$$H_{eff}(z)=\left(\frac{1-z^{-8}}{1-z^{-1}}\right)\bullet\left(\frac{1-z^{-8}}{1-z^{-1}}\right)$$

$$H_{eff}(z)=\left(\frac{1-z^{-8}}{1-z^{-1}}\right)\bullet\left(\frac{1-z^{-8}}{1-z^{-1}}\right)$$

Since $z = e^{j2\pi f/fs}$

$$H_{eff}(f)=\left(\frac{1-e^{-\frac{j8\cdot 2\pi f}{fs}}}{1-e^{-\frac{j2\pi f}{fs}}}\right)\bullet\left(\frac{1-e^{-\frac{j8\cdot 2\pi f}{fs}}}{1-e^{-\frac{j2\pi f}{fs}}}\right)$$

If we let $\theta = 2\pi f/fs$ then

$$H_{eff}(f)=\left(\frac{1-e^{-8j\theta}}{1-e^{-j\theta}}\right)\bullet\left(\frac{1-e^{-8j\theta}}{1-e^{-j\theta}}\right)$$

$$H_{eff}(f)=\left(\frac{1-\cos 8\theta-j\sin 8\theta}{1-\cos\theta-j\sin\theta}\right)\bullet\left(\frac{1-\cos 8\theta-j\sin 8\theta}{1-\cos\theta-j\sin\theta}\right)$$

$$H_{eff}(f)=H_1(f)\bullet H_1(f) \quad \textbf{[1]}$$

In order to find the frequency response of $H_{eff}(f)$, let us see the magnitude and phase response of $H_1(f)$.

$$H_1(f)=\left(\frac{1-\cos 8\theta-j\sin 8\theta}{1-\cos\theta-j\sin\theta}\right)$$

$$H_1(f)=\left[\frac{2\sin^2 4\theta-j2\sin 4\theta\cos 4\theta}{2\sin^2\frac{\theta}{2}-j2\sin\frac{\theta}{2}\cos\frac{\theta}{2}}\right]$$

$$H_1(f)=\left[\frac{2\sin^2 4\cdot\frac{2\pi f}{fs}-j2\sin 4\cdot\frac{2\pi f}{fs}\cos 4\cdot\frac{2\pi f}{fs}}{2\sin^2\frac{2\pi f}{2fs}-j2\sin\frac{2\pi f}{2fs}\cos\frac{2\pi f}{2fs}}\right]$$

$$H_1(f) = \left[\frac{2\sin^2 4\cdot\frac{2\pi f}{fs} - j2\sin 4\cdot\frac{2\pi f}{fs}\cos 4\cdot\frac{2\pi f}{fs}}{2\sin^2\frac{2\pi f}{2fs} - j2\sin\frac{2\pi f}{2fs}\cos\frac{2\pi f}{2fs}} \right]$$

$$H_1(f) = \left[\frac{2\sin 4\cdot\frac{2\pi f}{fs}\left(\sin 4\cdot\frac{2\pi f}{fs} - j\cos 4\cdot\frac{2\pi f}{fs}\right)}{2\sin\frac{2\pi f}{2fs}\left(\sin\frac{2\pi f}{2fs} - j\cos\frac{2\pi f}{2fs}\right)} \right]$$

$$H_1(f) = \left[\frac{\sin 4\cdot\frac{2\pi f}{fs}\left(\cos\left(\frac{\pi}{2} + 4\cdot\frac{2\pi f}{fs}\right) + j\sin\left(\frac{\pi}{2} + 4\cdot\frac{2\pi f}{fs}\right)\right)}{\sin\frac{2\pi f}{2fs}\left(\cos\left(\frac{\pi}{2} + \frac{2\pi f}{2fs}\right) + j\sin\left(\frac{\pi}{2} + \frac{2\pi f}{2fs}\right)\right)} \right]$$

$$H_1(f) = \left[\frac{\sin 4\cdot\frac{2\pi f}{fs}}{\sin\frac{2\pi f}{2fs}} \right] \left(\angle 4\cdot\frac{2\pi f}{fs} - \angle\frac{2\pi f}{2fs} \right)$$

$$H_1(f) = \left[\frac{\sin\frac{8\pi f}{fs}}{\sin\frac{\pi f}{fs}} \right] \left(\angle\frac{7\pi f}{fs} \right)$$

From equation **[1]** magnitude response of the individual frequency responses is multiplied to get the effective system frequency response. The individual phase responses are added to get the final phase response.

$$H_{eff}(f) = \left[\frac{\sin\frac{8\pi f}{fs}}{\sin\frac{\pi f}{fs}} \right]^2 \left(\angle\frac{14\pi f}{fs} \right) \quad \textbf{[2]}$$

The effective magnitude response of the system has zeroes at multiples of fs/8.

The individual filters of the cascaded filter i.e. $H_1(f)$ and $H_2(f)$ as shown in Figure 1 have a frequency response as shown in Figure 2.

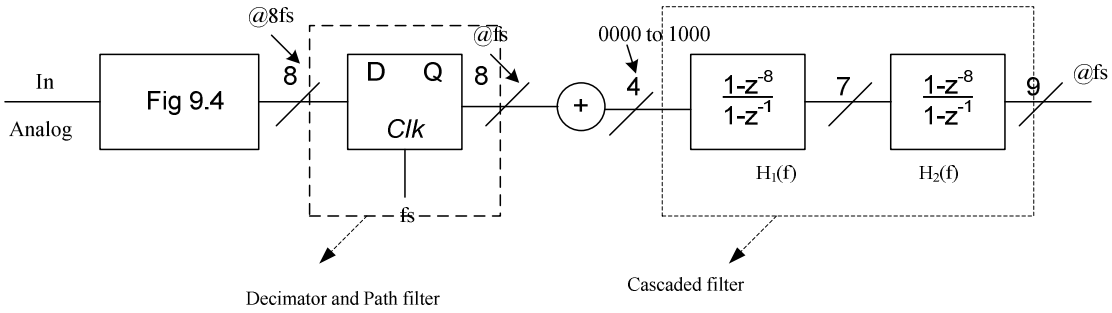


Figure 1. Decimating and filtering the output of a the K-path (K=8) modulator

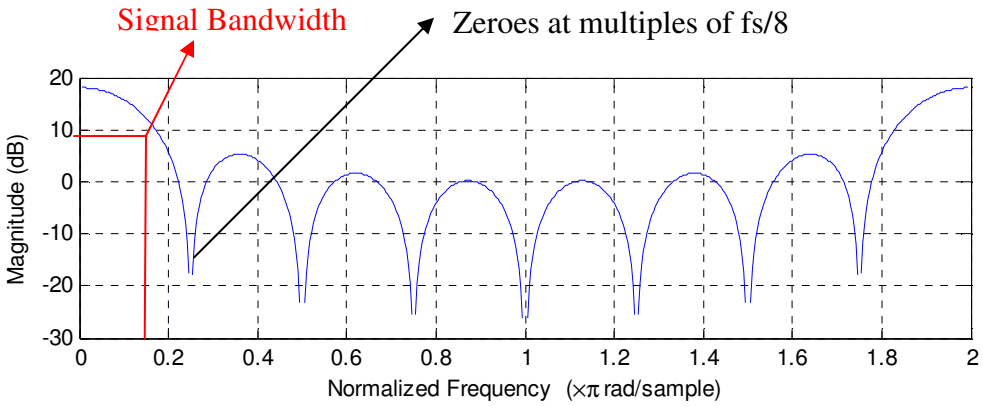


Figure 2. The frequency response of H_1 (f) or H_2(f) in Figure 1

From Figure 2 We can see that magnitude of H_1 (f) or H_2 (f) has zeroes at multiples of fs/8.

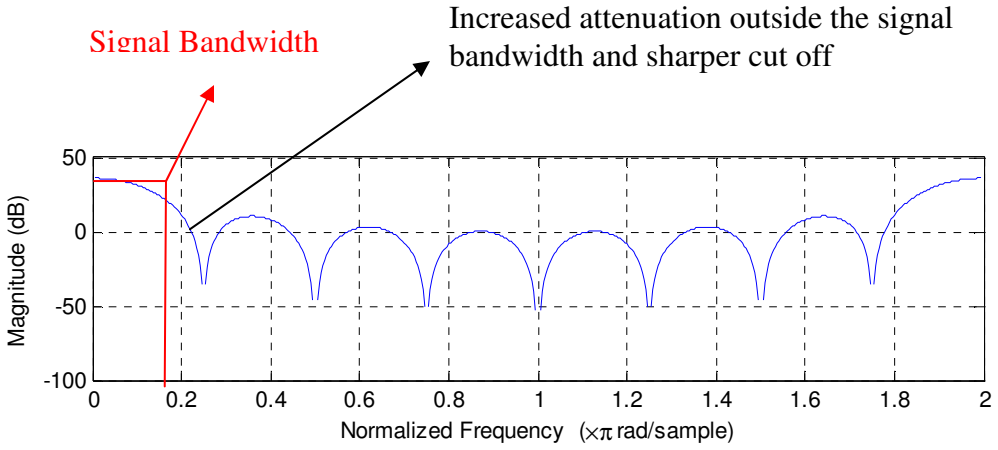


Figure 3. The frequency response of H_{eff} (f)

The cascaded filter in the Figure 3 results in a sharper cut off frequency and increased attenuation in the frequency bands adjacent to the signal bandwidth.

9.8. What is the frequency response (an equation) of the filter seen in Fig 9.12?
Sol. Let us see the frequency response of the filter shown in Figure 1. The transfer function of the filter is derived assuming $f_{snew} = 8fs$. Since

$$z = e^{j2\pi f/fsnew}$$

The output at Section 1 of filter in Figure 1 is given by $1+z^{-1}$. The output at Section 2 is given by $1+z^{-2}$ as sampling frequency is decreased by 2. Similarly the output at Section 1 is given by $1+z^{-4}$. The output at Section 4 is given by $1+z^{-8}$.

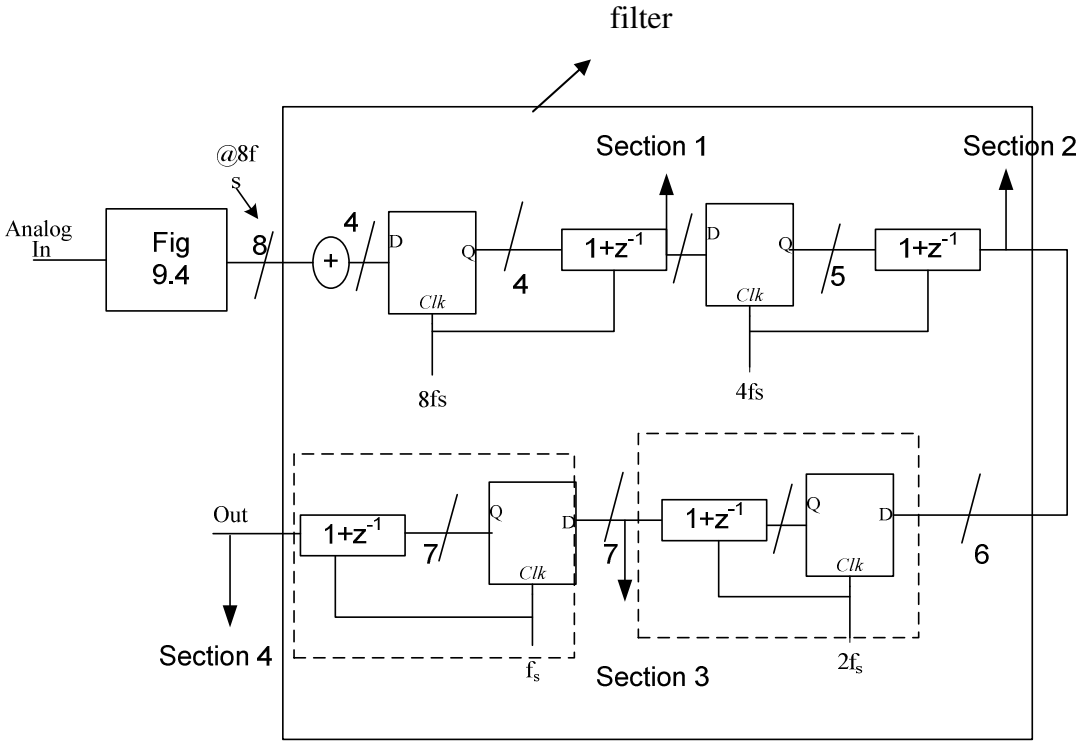


Figure 1. Decimating through filter (Fig 9.12 in book)

Hence the overall transfer function in the z-domain is given by

$$H(z) = \left(1+z^{-1}\right)\left(1+z^{-2}\right)\left(1+z^{-4}\right)\left(1+z^{-8}\right)$$

$$H(z) = \left(\frac{1-z^{-16}}{1-z^{-1}}\right) \qquad \text{Since} \quad z = e^{\frac{j2\pi f}{fsnew}} = e^{\frac{j2\pi f}{8fs}}$$

The frequency response is given by

$$H(f) = \left(\frac{1-e^{-j\frac{16\cdot 2\pi}{8}\cdot\frac{f}{fs}}}{1-e^{-\frac{j\cdot 2\pi}{8}\cdot\frac{f}{fs}}}\right) = \left(\frac{1-e^{-j4\pi\cdot\frac{f}{fs}}}{1-e^{-\frac{j\pi}{4}\cdot\frac{f}{fs}}}\right)$$

Let $\theta = \frac{\pi}{2} \cdot \frac{f}{fs}$

$$H(f) = \left(\frac{1 - e^{-j8\theta}}{1 - e^{-j\frac{\theta}{2}}} \right)$$

$$H(f) = \left(\frac{1 - \cos 8\theta - j\sin 8\theta}{1 - \cos\frac{\theta}{2} - j\sin\frac{\theta}{2}} \right)$$

$$H(f) = \frac{2\sin^2 4\theta - j2\sin 4\theta\cos 4\theta}{2\sin^2\frac{\theta}{4} - j2\sin\frac{\theta}{4}\cos\frac{\theta}{4}}$$

$$H(f) = \frac{2\sin 4\theta(\sin 4\theta - j\cos 4\theta)}{2\sin\frac{\theta}{4}(\sin\frac{\theta}{4} - j\cos\frac{\theta}{4})}$$

$$H(f) = \frac{2\sin 4\theta\left(\cos\left(\frac{\pi}{2} + 4\theta\right) - j\sin\left(\frac{\pi}{2} + 4\theta\right)\right)}{2\sin\frac{\theta}{4}\left(\cos\left(\frac{\pi}{2} + \frac{\theta}{4}\right) - j\sin\left(\frac{\pi}{2} + \frac{\theta}{4}\right)\right)}$$

$$H(f) = \frac{2\sin 4\theta}{2\sin\frac{\theta}{4}}\left[\angle 4\theta - \angle\frac{\theta}{4}\right]$$

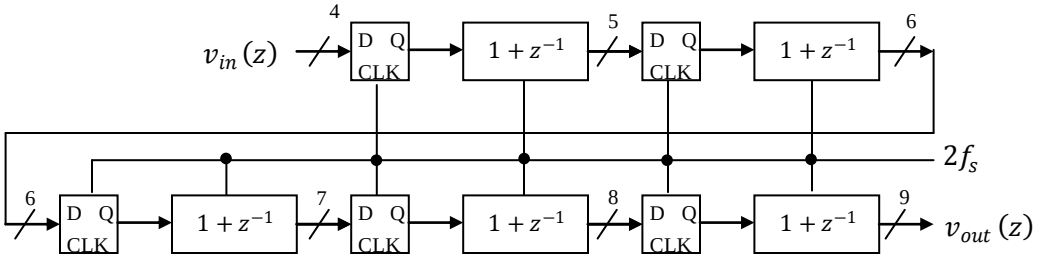
$$H(f) = \frac{\sin 4\theta}{\sin\frac{\theta}{4}}\left[\angle 15\frac{\theta}{4}\right]$$

Substituting $\theta = \frac{\pi}{2} \cdot \frac{f}{fs}$

We get magnitude response as $|H(f)| = \frac{\sin\left(\frac{2\pi f}{f_s}\right)}{\sin\left(\frac{\pi f}{8f_s}\right)}$ **[1]**

Phase response as $\angle H(f) = \frac{15\pi f}{8f_s}$ **[2]**

9.9 What is the frequency (an equation) of the filter seen in Fig. 9.14?



F-1 Filter used in Figure 9.14

Figure 9.14 uses the cascade of comb filters clocked at $2f_s$. Before determining the transfer function of the cascade comb filter above let's review the comb filter.

$$|1+z^{-1}| = \left|1+e^{-j2\pi\frac{f}{f_s}}\right| = \left|1+\cos\left(-2\pi\frac{f}{f_s}\right)+j\sin\left(-2\pi\frac{f}{f_s}\right)\right|$$

$$= \left|1+\cos\left(-2\pi\frac{f}{f_s}\right)+j\sin\left(-2\pi\frac{f}{f_s}\right)\right| = \left|\sqrt{\left(1+\cos\left(-2\pi\frac{f}{f_s}\right)\right)^2+\left(\sin\left(-2\pi\frac{f}{f_s}\right)\right)^2}\right|$$

$$= \left|\sqrt{2\left(1+\cos\left(2\pi\frac{f}{f_s}\right)\right)}\right| = 2\left|\cos\left(\pi\frac{f}{f_s}\right)\right|$$

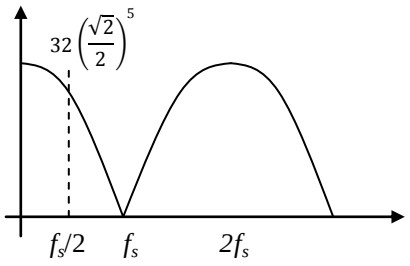
So for the cascade structure seen in F-1 we can state that the transfer function is:

$$H(z) = \frac{v_{out}}{v_{in}} = (1+z^{-1})^5$$

This is simply the transfer function of a cascaded comb filter with sampling frequency equal to $2f_s$. The magnitude of this transfer function is:

$$|H(f)| = \left|\frac{v_{out}}{v_{in}}\right| = 32\left|cos\left(\pi\frac{f}{2f_s}\right)\right|^5$$

Figure 9.14 also provides the magnitude plot of this comb filter:



F-2 Magnitude response of a cascade filter

Kaijun Li
9.10 What is the frequency response (an equation) of the filter seen in Fig. 9.16?

Solution:
The filter seen in Fig. 9.10 is essentially cascading five stage of averager. The filter's transfer function can be found as

$$H(z) = \left(1 + z^{-1}\right)^5$$

The frequency response can be roughly depicted as seen in Figure 1.

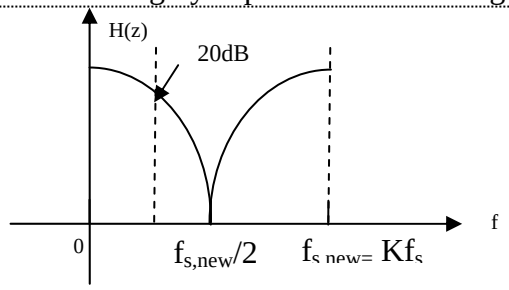


Figure 1. The frequency response of the filter seen in Fig. 9.16

In Figure 1, it is noted that the filter won't do a good job in removing the quantization noise, and this can be verified in the SPICE simulation as discussed below.

The SPICE simulation time for Fig. 9.16 (can be downloaded from CMOSedu.com) can be changed to 4us and input signal frequency is changed to be 4MHz to avoid the noise leakage when performing the FFT plot. The time-domain result is shown in Figure 2.

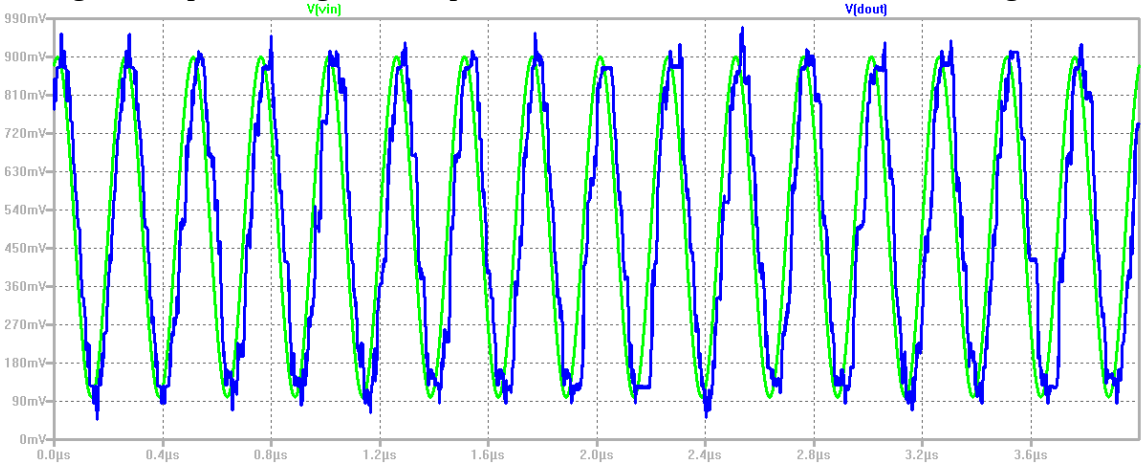


Figure 2. The time-domain results for the filter seen in Fig. 9.16

The FFT plots are shown in Figure 3 and Figure 4.

Figure 3. The FFT plot for the filtered output data (log frequency)

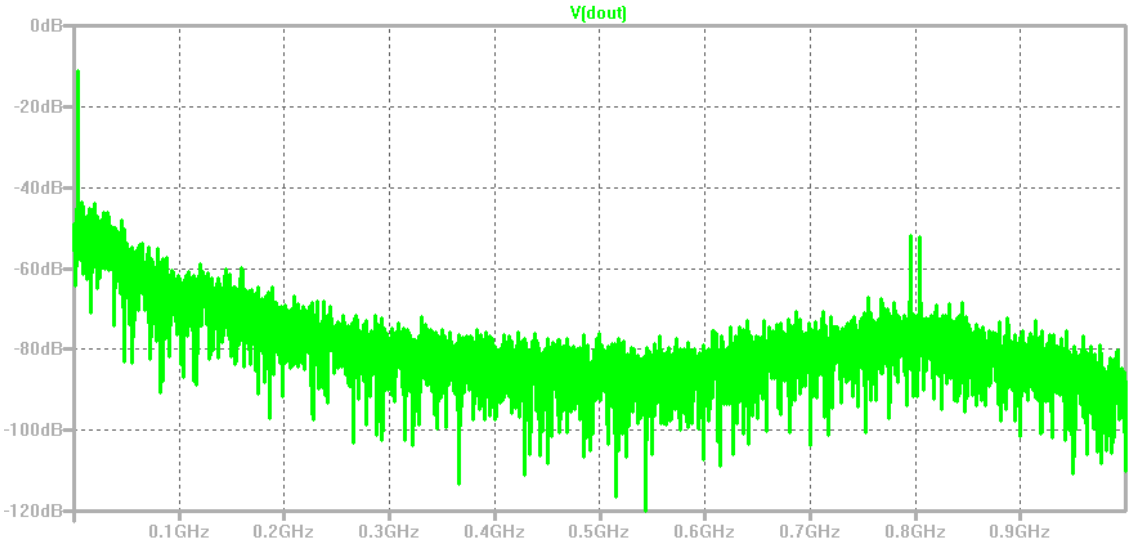


Figure 4. The The FFT plot for the filtered output data (linear frequency)

As seen in these figures, the quantization at the lower frequency (less than nyquist frequency 400MHz) is attenuated. However, the quantization noise is not greatly removed effectively to get good resolution or high signal-to-noise ratio.

Kaijun Li

9.11 Show how the switches on the inputs and outputs of the 8 modulators in parallel seen in Fig. 9.20 can be described using the unit matrix and delays or

$$\begin{bmatrix} 1\,0\,0\,0\,0\,0\,0\,0 \\ 0\,1\,0\,0\,0\,0\,0\,0 \\ 0\,0\,1\,0\,0\,0\,0\,0 \\ 0\,0\,0\,1\,0\,0\,0\,0 \\ 0\,0\,0\,0\,1\,0\,0\,0 \\ 0\,0\,0\,0\,0\,1\,0\,0 \\ 0\,0\,0\,0\,0\,0\,1\,0 \\ 0\,0\,0\,0\,0\,0\,0\,1 \end{bmatrix} \cdot \begin{bmatrix} z^{-0} \\ z^{-1/8} \\ z^{-2/8} \\ z^{-3/8} \\ z^{-4/8} \\ z^{-5/8} \\ z^{-6/8} \\ z^{-7/8} \end{bmatrix}$$

Where $z = e^{j2\pi f \cdot T_S}$. Using these relationships show how to relate the inputs of the *K* paths in parallel, Fig. 9.20, to the transfer function and the resulting topology's outputs.

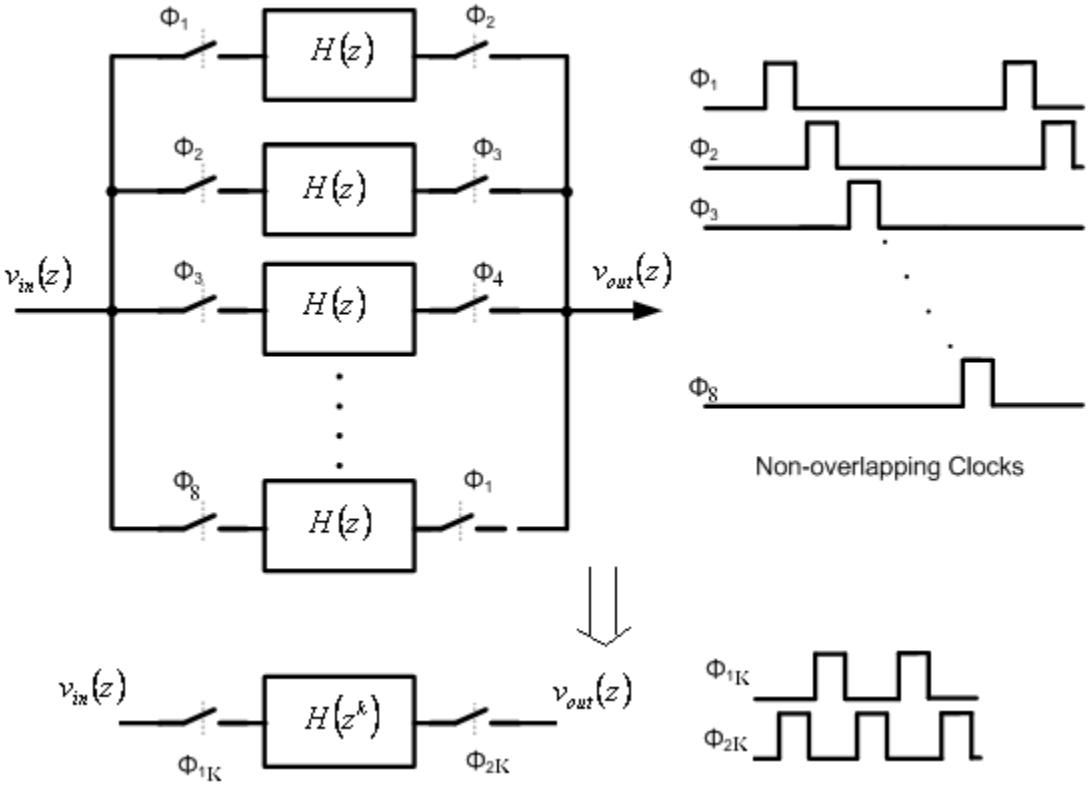


Figure 9.20. Eight modulators in parallel (a time-interleaved topology)

Solution:

The way to better to understand the parallel structure properly is to introduce the concept of poly-phase decomposition.

The basic concept for poly-phase decomposition is so called multi-rate signal processing or effectively changing the sampling rate among these parallel channels. The block diagram for a poly-phase decomposition system is shown in Figure 1.

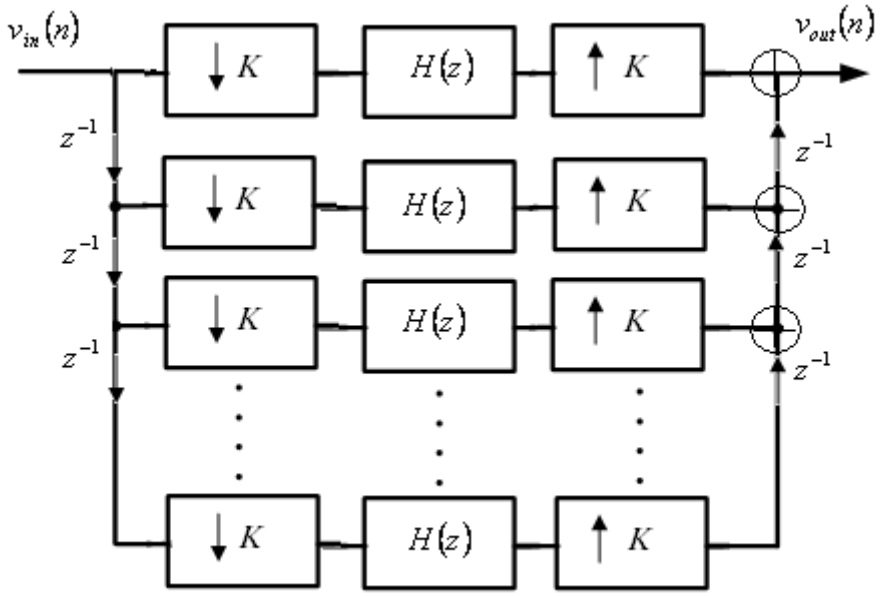


Figure 1. Block diagram for a poly-phase decomposition system

In Figure 1, the input signal is experiencing down-sampling when it is passed through each single path. Also it is noticed that the input signal's delay version is fed into each path, and the delay is at the fast clock frequency which are the clock signals Φ_{1K} and Φ_{2K} seen in Fig. 9.20.

The equivalent block diagram for Figure 1 is shown in Figure 2 where the transfer function $H(z)$ for single path is replaced with $H(z^K)$. That is because each individual path is running at a slower rate, and here $z = e^{j2\pi f \cdot T_{S,new}}$ or $e^{j2\pi f \cdot T_S / K}$.

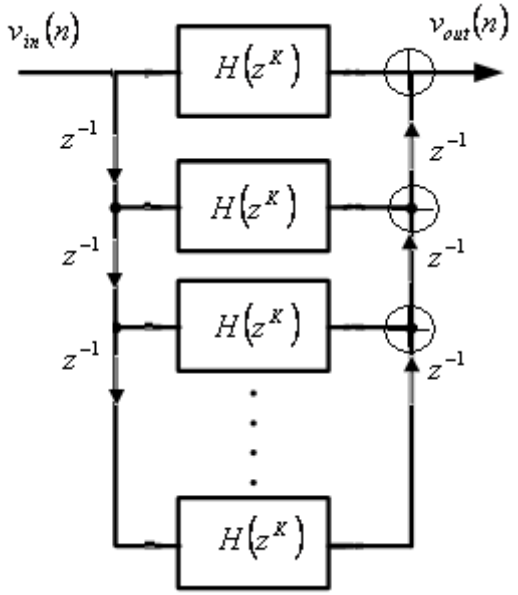


Figure 2. The simplified block diagram for poly-phase system

Finally, it comes down to the block diagram seen in the bottom part of Fig. 9.20 or redrawn in Figure 3.

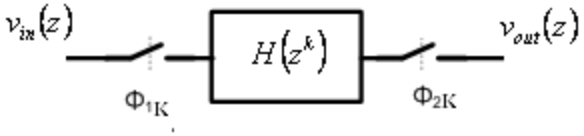


Figure 4. The equivalent diagram for the time-interleaved topology

So the resulting system transfer function is $H(z^K)$ instead of $H(z)$, and that is the key point discussed here. For the noise shaping data conversion, the output can be expressed as:

$$V_{out}(z^K) = V_{in}(z)z^{-K} + (1 - z^{-K})V_{Qe}(z)$$

And the noise-shaping effect for the time-interleaved modulator is seen in Figure 5.

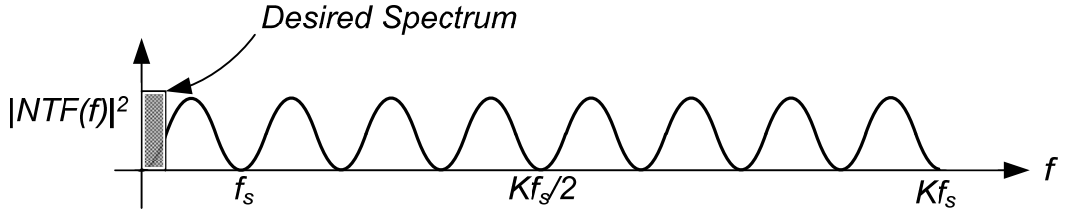


Figure 5. Noise Shaping for the K-path time-interleaved topology

As discussed above, the time-interleaved topology won't be able to increase the SNR dramatically since it doesn't shape the quantization noise to $Kf_s/2$ but instead it lowers the quantization noise floor by spreading the noise over a wider spectrum.

Solution by Geng Zheng

9.12 The effective frequency of the K-Delta-1-Sigma ADC discuss in Sec. 9.2 is roughly 1.6 GHz. Can any component of the ADC operate at, or be clocked at, 1.6 GHz. Verify your answers using SPICE and the 500 nm, 5V, CMOS models used to generate these figures. What is the most critical component then, from a timing perspective, (the DFF used to capture the eight bits coming out of the modulators) and what is critical in that component (the DFF's setup and hold times): What happens if an error is made in the most critical component? (The wrong count is captured. For example, we would capture 6 logic 1s but actually capture 5 or 7 logic 1s. Since we have a significant amount of averaging in the digital filter the effects should be small. If an equal number of positive and negative error are made the errors average to zero and don't affect the converter's performance.)

Solution:

If the ADC is operate at 1.6 GHz (the effective sampling frequency is then 8×1.6 GHz), only the switched-capacitor input and the DFF can work properly. The time constant of the switched-capacitor input is 50 ps so the capacitor can be fully charged (Fig. 1) even when the circuit is operated at 1.6 GHz. Fig. 2 shows that the opamp cannot fully charge the output load if we clock the circuit at 1.6 GHz. Fig. 3 shows that the clocked comparator doesn't function correctly if it is clocked at 1.6 GHz. Fig. 4 shows the operation of the DFF clocked at 1.6 GHz.

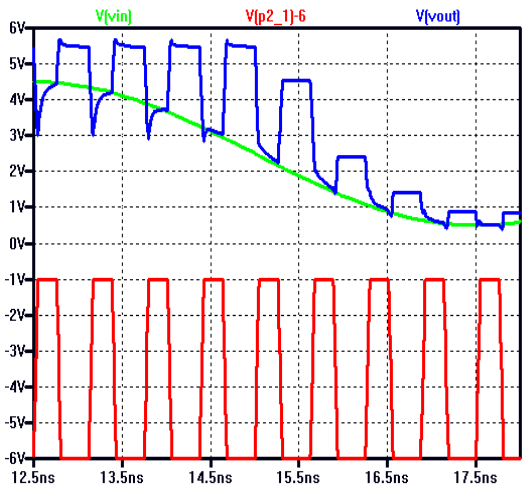


Figure 1 The switched-capacitor input clocked 1.6 GHz.

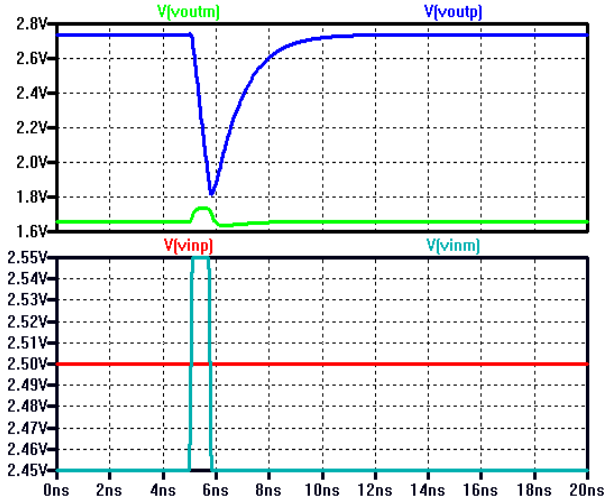


Figure 2 The operation of the amplifier when the circuit is clocked at 1.6 GHz.

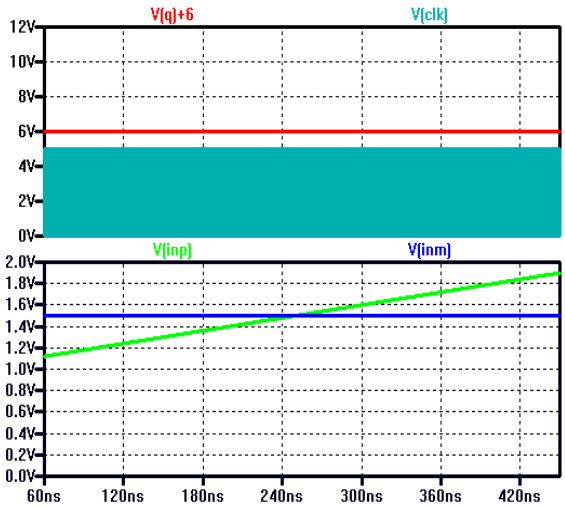


Figure 1 The operation of the clocked comparator clocked at 1.6 GHz.

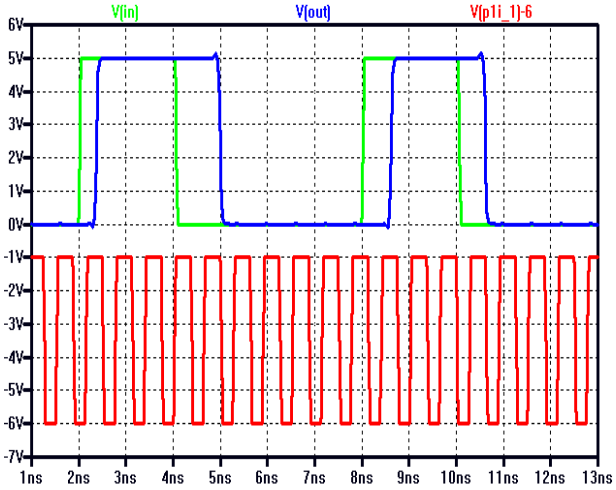


Figure 2 The operation of the DFF operates at 1.6 GHz.

From the timing perspective the DFF used to capture modulators is the most critical component. If the DFF cannot operate fast enough, we will not be able to capture the correct modulator output. Thus even we have a good modulator design we won't be able to take the advantage of it if the DFF's setup and hold times are not satisfied. If an error, as the example in the problem statement, is made in the DFF, digital filtering will significantly remove it. However, if the we design the modulator for a very wide bandwidth (the input is changing in a much faster rate), the DFF may not be able to clock in most of the modulator output correctly, which will result in a large degradation of the ADC performance.