PROBLEM # 11.1 **Meshack Pavan.A**

Estimate the noise margins for the inverters used to generate Fig. 11.4.

***Solution*: -**

From the graphs in Fig. 11.4 and the text in p11.3, we have

V_{OH} = 5V
V_{OL} = 0V
V_{IL} = 1.8V
V_{IH} = 2.1V

Long channel Process

Therefore, noise margins,
$NM_H = V_{OH} - V_{IH} = 5 – 2.1 = 2.9V$
$NM_L = V_{IL} - V_{OL} = 1.8 – 0 = 1.8V$

For the short channel process, similarly from the graph and text in the book,

V_{OH} = 1V
V_{OL} = 0V
V_{IL} = 400mV
V_{IH} = 500mV

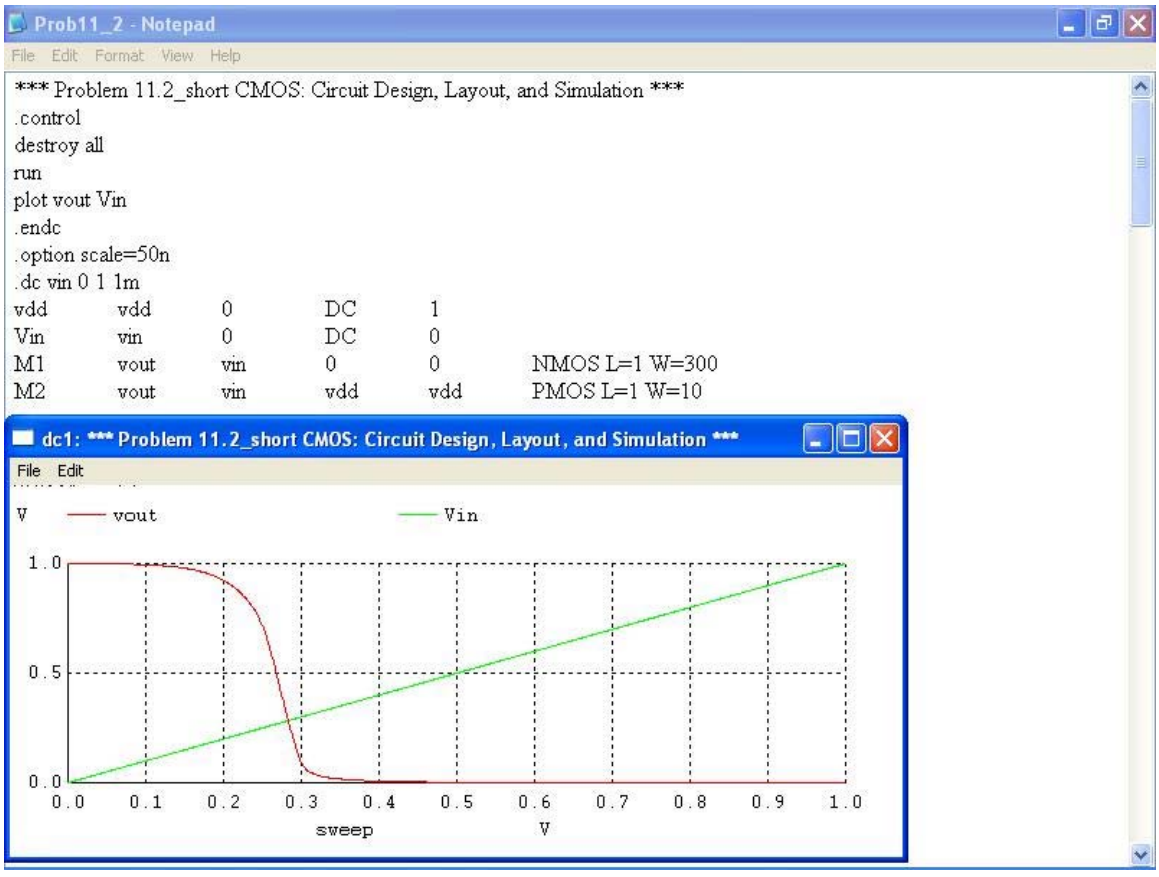
So, noise margins,
$NM_H = V_{OH} - V_{IH} = 1 – 0.5 = 0.5V = 500mV$
$NM_L = V_{IL} - V_{OL} = 0.4 – 0 = 0.4V = 400mV$

Vinay Dindi EE510

11.2) Design and simulate the DC characteristics of an inverter with Vsp approximately equal to VTHn. Estimate the resulting noise margins for the design.

For Vsp~=Vthn, (ßn/ ßp) should be as large as possible.
Let (ßn/ ßp)=90
So Wn=30*Wp assuming KPn=KPp and Ln=Lp
If Wp=10, then Wn=300.
Substituting these values in equation 11.4,
we get Vsp=0.32. (Vtn=Vtp=0.28V from Table 6.3)

From simulations we obtain Vsp~=0.27V.



Problem 11.3 **Satish Dulam**

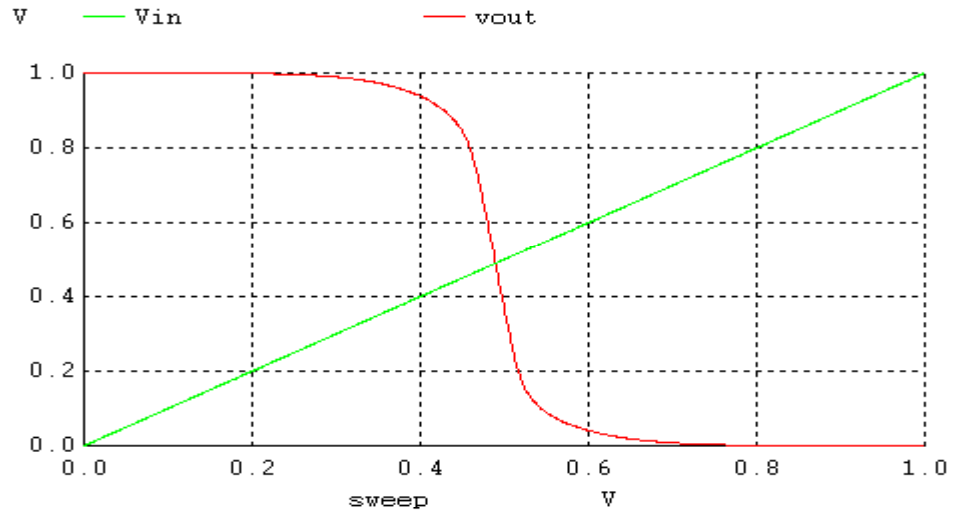
Question:

Show that the switching point of three inverters in series is dominated by the Vsp id the first inverter.

Solution:

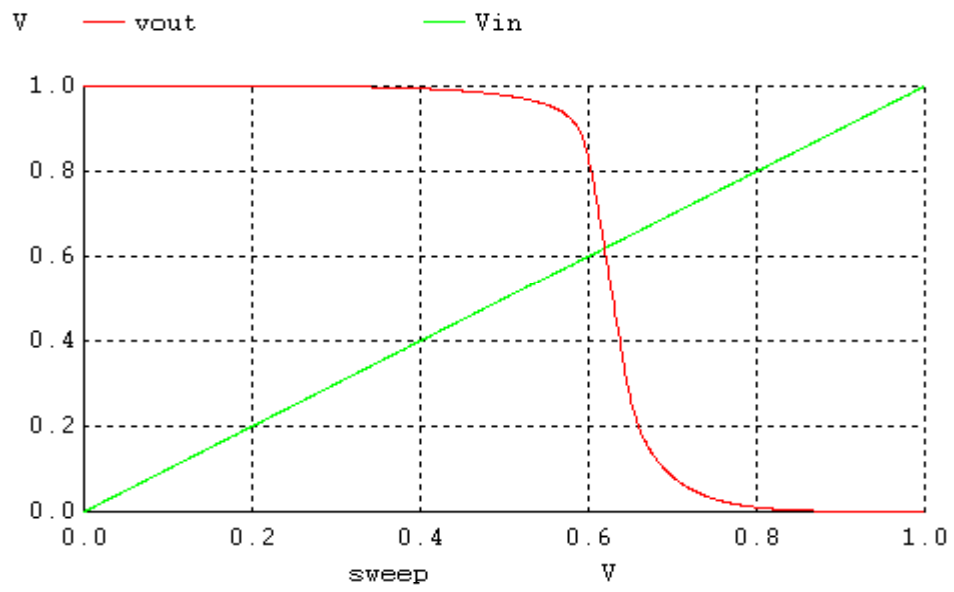
Three inverters with different switching points are simulated as below:

```
*Stage1 Inverter
.control
destroy all
run
let Icross=-i(vdd)
*plot Icross
plot vout Vin
.endc
.option scale=50n
.dc vin 0 1 1m
vdd     vdd     0       DC      1
Vin     vin     0       DC      0
M1      vout    vin     0       0       NMOS L=1 W=10
M2      vout    vin     vdd     vdd     PMOS L=1 W=20
* 50nm BSIM4 models
```

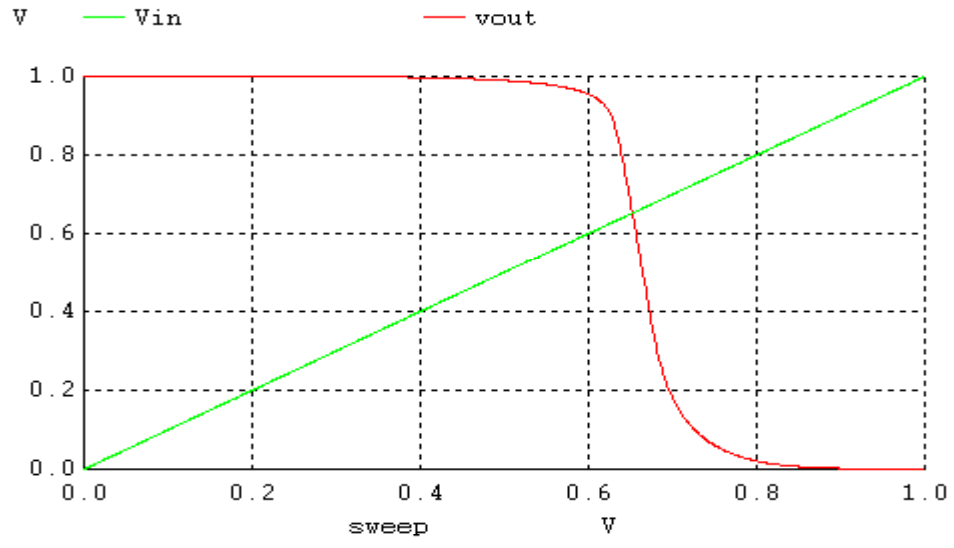


Stage2 and 3 Inverters with different Switching points:

```
*Stage2 Inverter
.control
destroy all
run
let Icross=-i(vdd)
*plot Icross
plot vout Vin
.endc
.option scale=50n
.dc vin 0 1 1m
vdd     vdd     0       DC      1
Vin     vin     0       DC      0
M1      vout    vin     0       0       NMOS L=1 W=10
M2      vout    vin     vdd     vdd     PMOS L=1 W=200
* 50nm BSIM4 models
```



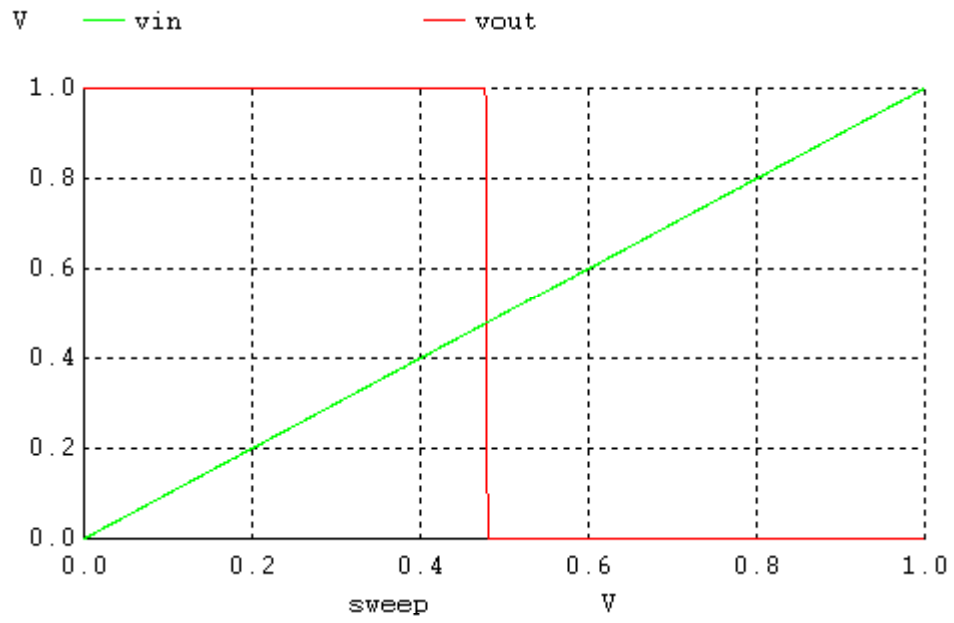

```
*Stage3 Inverter
.control
destroy all
run
let Icross=-i(vdd)
*plot Icross
plot vout Vin
.endc
.option scale=50n
.dc vin 0 1 1m
vdd     vdd     0       DC      1
Vin     vin     0       DC      0
M1      vout    vin     0       0       NMOS L=1 W=10
M2      vout    vin     vdd     vdd     PMOS L=1 W=400
* 50nm BSIM4 models
```



```
*Three inverters in series
.control
destroy all
run
plot vout vin
.endc
.option scale=50n
.dc vin 0 1 1m

vdd     vdd     0       DC      1
Vin     vin     0       DC      0
M1      vout1   vin     0       0       NMOS L=1 W=10
M2      vout1   vin     vdd     vdd     PMOS L=1 W=20
M3      vout2   vout1   0       0       NMOS L=1 W=10
M4      vout2   vout1   vdd     vdd     PMOS L=1 W=200
M5      vout    vout2   0       0       NMOS L=1 W=10
M6      vout    vout2   vdd     vdd     PMOS L=1 W=400

* 50nm BSIM4 models
* Don't forget the .options scale=50nm if using an Lmin of 1
* 1<Ldrawn<200   10<Wdrawn<10000 Vdd=1V
* Change to level=54 when using HSPICE
```



Notice the switching point of the 3stage inverters is around 500mv though the second and third stage switching points are at 640mv.

Problem 11.4 **Rahul Mhatre**

Repeat Ex. 11.6 using a PMOS device with a width of 10.

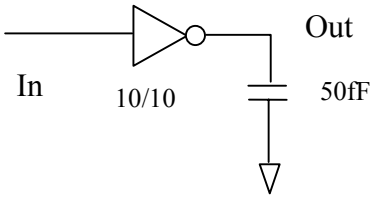


Figure 11.11 Circuit Schematic for Problem 11.4.

Solution: Replacing the inverter with its digital model, we get the following schematic

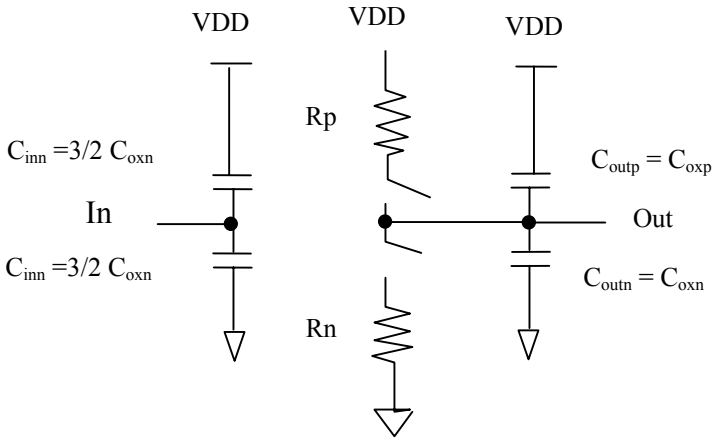


Figure 11.4.1 Digital Model for the inverter

The total capacitance at the output node is given as
$C_{tot} = C_{oxp} + C_{oxn} + C_{load}$
C_{tot} = (62.5aF) [WnLn + WpLp] + 50fF
= (62.5aF) [10 + 10] + 50fF
C_{tot} = 51.25 fF

From Table 10.1,
Rp = 68k/Wp
Rp = 68k/10 = 6.8K

Rn = 34K/Wn
Rn = 34K/10 = 3.4K

T_{pHL} = 0.7 Rn C_{tot}
T_{pHL} = 0.7 * 3.4K * 51.25fF
T_{pHL} = 122 pS

$T_{pLH} = 0.7\ Rp\ C_{tot}$
$T_{pLH} = 0.7 * 6.8K * 51.25fF$
T_{pLH} = 244pS

The SPICE Simulation netlist is as shown in Figure 11.4.2

```
*** Problem 11.4 CMOS: Circuit Design, Layout, and Simulation ***
.control
destroy all
run
plot vin vout
.endc

.option scale=50n
.tran 10p 2n UIC

vdd     vdd     0       DC      1
Vin     vin     0       DC      0       pulse 0 1 500p 0 0 1n 2n

M1      vout    vin     0       0       NMOS L=1 W=10
M2      vout    vin     vdd     vdd     PMOS L=1 W=10
Cl      vout    0       50f

***Models for NMOS and PMOS****
.end
```

Figure 11.4.2 SPICE netlist for Figure 11.11

The SPICE simulations are as shown in Figure 11.4.3. The **T_{pHL}** was found to be **100 ps** and **T_{pLH}** was found out to be around **200ps.**

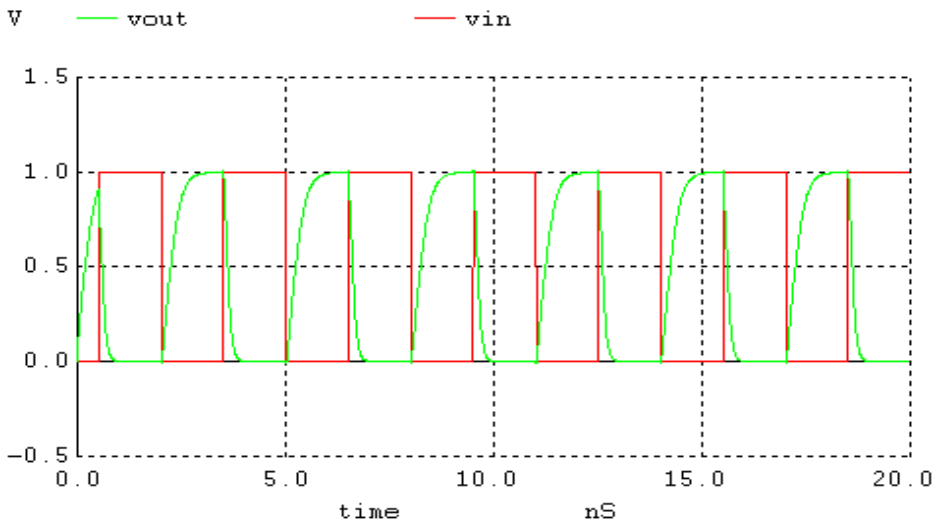


Figure 11.4.3 SPICE Simulation for the netlist of Figure 11.1

John Spratt

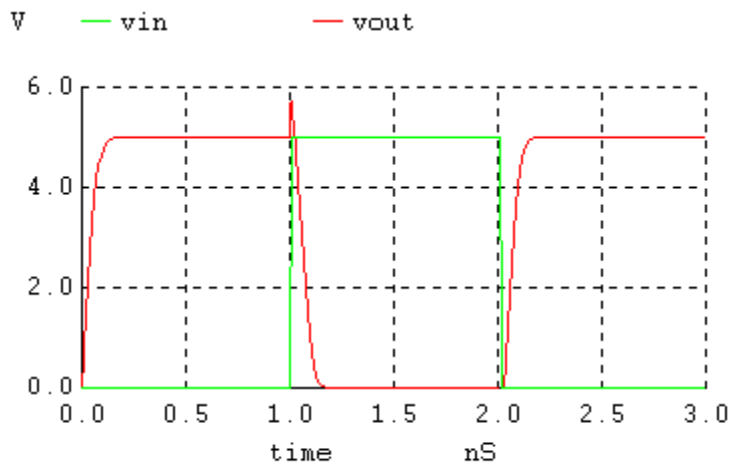
Problem 11.5: Repeat Ex. 11.6 using the long channel process with a 30/10 inverter.

Solution:

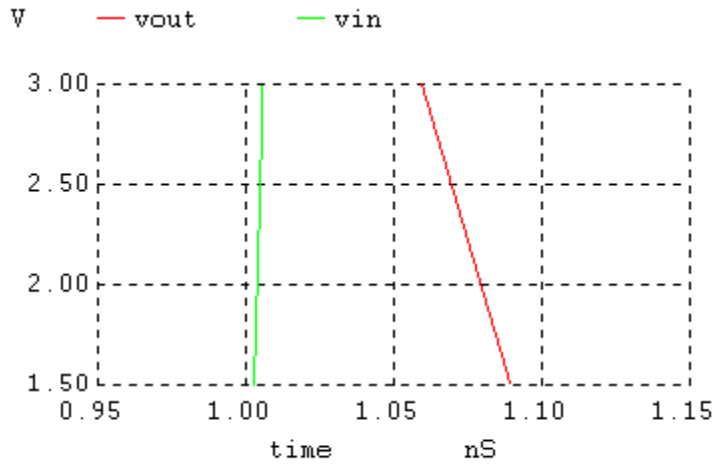
```
*** Top Level Netlist ***
vdd         vdd         0           DC          5
Vin         vin         0           DC          0           pulse 0 5 1n 0p 0p 1n 2n
C1      Vout 0 50fF

M1      Vout Vin 0 0   NMOS  L=1u W=10u
M2      Vout Vin Vdd Vdd PMOS  L=1u W=30u
```

Simulation:

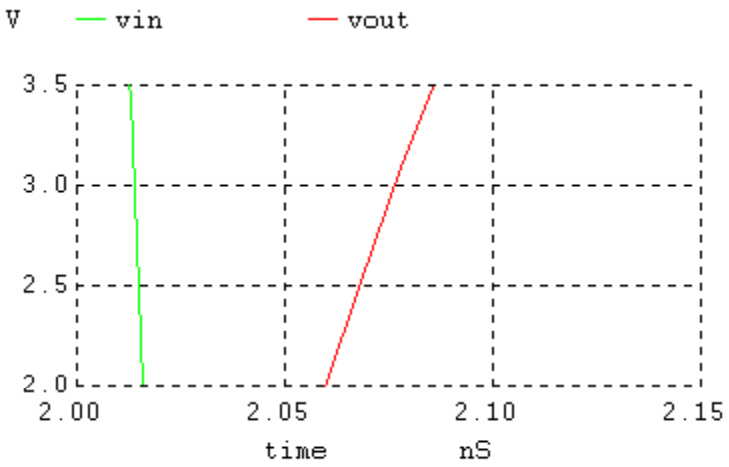


tPHL=69ps



tPLH=67ps

John Spratt



Taking into account the output capacitance of the MOS's:

tPHL=.7*Rp*Ctot=.7*45k/30*(1.75f*(30+10)+50f)=126ps
tPLH=.7*Rn*Ctot=.7*15k/10*(1.75f*(30+10)+50f)=126ps

W/O taking into account the output capacitance of the MOS's:

tPHL=.7*Rp*Ctot=.7*45k/30*(50f)=52.5ps
tPLH=.7*Rn*Ctot=.7*15k/10*(50f)=52.5ps

W/O appears to be closer to the sim.

Problem 11.6 Steve Bard

Estimate the oscillation frequency of an 11-stage ring oscillator using 30/10 inverters in the long-channel CMOS process. Compare your hand calculations to the simulation results.

Solution: The frequency is about 250 MHz when calculated by hand. When simulated on SPICE, the frequency is higher, reaching 495 MHz. The hand calculations are shown below, and the SPICE simulation is shown on the next page.

$$f_{rosc} = \frac{1}{n\left(t_{PHL} + t_{PLH}\right)}$$

$$t_{PHL} + t_{PLH} = 0.7\left(R_n + R_p\right)C_{TOT}$$

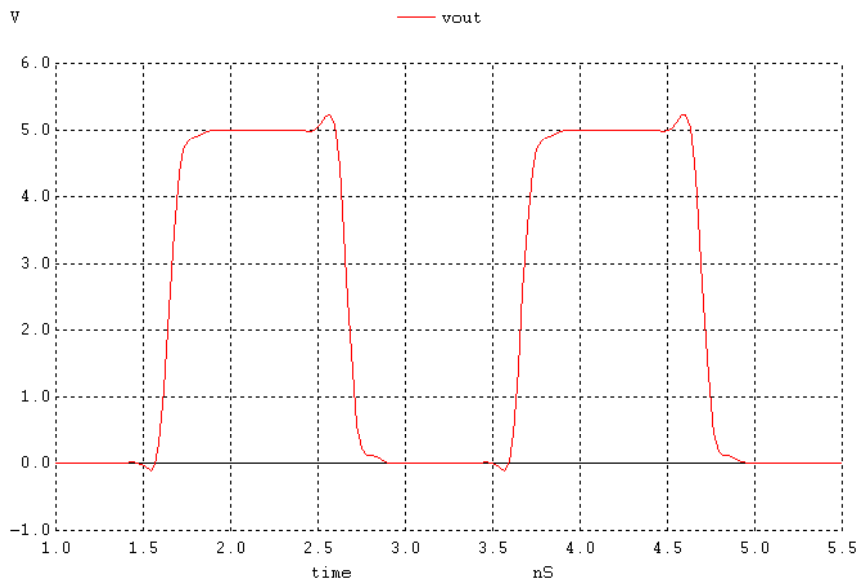
$$C_{TOT} = \frac{5}{2}\left(C_{oxP} + C_{oxN}\right)$$

$$R_n = 15\ k\ \frac{L}{W} = \frac{15\ k}{10} = 1.5k$$
$$R_p = 45\ k\ \frac{L}{W} = \frac{45\ k}{30} = 1.5k$$

$$C_{oxP} = 1.75fF \cdot W \cdot L = 52.5fF$$
$$C_{oxN} = 1.75fF \cdot W \cdot L = 17.5fF$$

$$C_{TOT} = \frac{5}{2}\left(52.5fF + 17.5fF\right) = 175fF$$

$$t_{PHL} + t_{PLH} = 0.7\left(1.5k + 1.5k\right)(175fF) = 368ps$$
$$f_{rosc} = \frac{1}{11(368ps)} \approx 250MHz$$



From the SPICE simulation, the frequency = 1/T = 1 / 2.02 ns = 495 MHz.

*** Problem 11.6 ***

```
.control
destroy all
run
plot vout
.endc
.option scale=1u
.tran .1n 6.5n uic

vdd         vdd         0           DC          5
R1          vout        0           1MEG

**********D********G*******S*******B****
M1          vout1       vout        0           0           NMOS L=1 W=10
M2          vout1       vout        vdd         vdd         PMOS L=1 W=30
M3          vout2       vout1       0           0           NMOS L=1 W=10
M4          vout2       vout1       vdd         vdd         PMOS L=1 W=30
M5          vout3       vout2       0           0           NMOS L=1 W=10
M6          vout3       vout2       vdd         vdd         PMOS L=1 W=30
M7          vout4       vout3       0           0           NMOS L=1 W=10
M8          vout4       vout3       vdd         vdd         PMOS L=1 W=30
M9          vout5       vout4       0           0           NMOS L=1 W=10
M10         vout5       vout4       vdd         vdd         PMOS L=1 W=30
M11         vout6       vout5       0           0           NMOS L=1 W=10
M12         vout6       vout5       vdd         vdd         PMOS L=1 W=30
M13         vout7       vout6       0           0           NMOS L=1 W=10
M14         vout7       vout6       vdd         vdd         PMOS L=1 W=30
M15         vout8       vout7       0           0           NMOS L=1 W=10
M16         vout8       vout7       vdd         vdd         PMOS L=1 W=30
M17         vout9       vout8       0           0           NMOS L=1 W=10
M18         vout9       vout8       vdd         vdd         PMOS L=1 W=30
M19         vout10      vout9       0           0           NMOS L=1 W=10
M20         vout10      vout9       vdd         vdd         PMOS L=1 W=30
M21         vout        vout10      0           0           NMOS L=1 W=10
M22         vout        vout10      vdd         vdd         PMOS L=1 W=30

.MODEL NMOS NMOS LEVEL  = 3
.MODEL PMOS PMOS LEVEL  = 3
.end
```

Problem 11.7 **Lincoln Bollschweiler**

Using the long channel process design a buffer with minimum delay (A=e) to insert in between a 30/10 inverter and a 50pF load capacitance. Simulate the operation of the design.

Solution:
For a 30/10 long channel process using table 10.2;
using (11.6), $C_{IN,\ 30/10\ INV}$ = 105fF;
using (11.7), $C_{OUT,\ 30/10\ INV}$ = 70fF.

Using (11.20), $e = \left[\frac{50p}{105f}\right]^{\frac{1}{N}} \Rightarrow N = \ln\left[\frac{50p}{105f}\right] = 6.17.$

Although we are creating a buffer to go *in between* the 30/10 inverter and a load capacitance, we are including the 30/10 inverter in the calculations above. Therefore, in order to keep the required inversion we must choose N equal to the closest *odd* number of gates. As N=6.17, we choose to round to N=7.

Using (11.20), $A = \left[\frac{50p}{105f}\right]^{\frac{1}{7}} \Rightarrow A = 2.41.$

The first gate in the buffer will be sized up by A=2.41 compared to the 30/10 inverter. The second gate will have $A=2.41^2$, the third $A=2.41^3$ and so on until the last, gate 6 of the buffer, will have $A=2.41^6$.

Using $t_{PHL} + t_{PLH} = 0.7 \cdot N\left(R_N + R_P\right)\left(C_{OUT1} + A \cdot C_{IN1}\right)$, we have

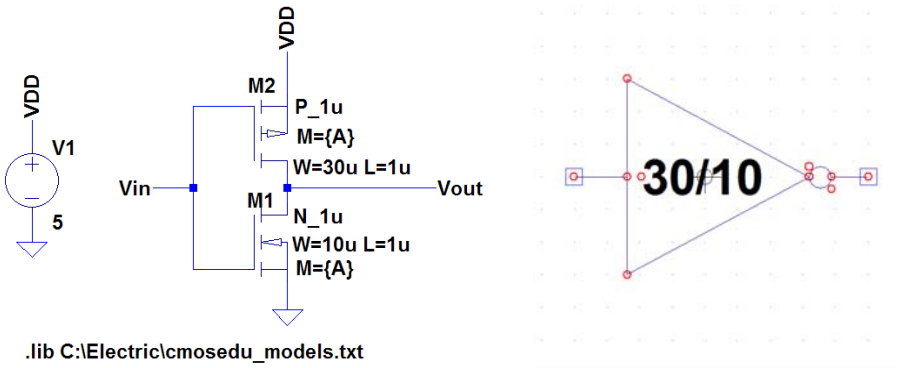
$t_{PHL} + t_{PLH} = 0.7 \cdot 7\left(1500 + 1500\right)\left(70E-15 + 2.41 \cdot 105E-15\right) = 4.75ns$ with a 6 gate buffer (7 gates total including the 30/10 inverter).

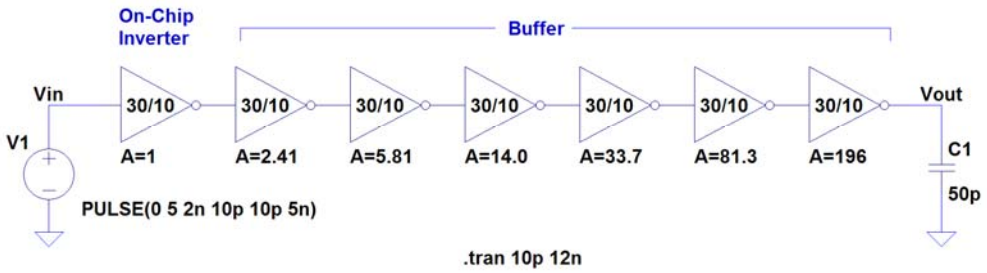
To find the delay for the 30/10 inverter with no buffer we can use
$t_{PHL} + t_{PLH} \approx 0.7\left(R_N + R_P\right)\left(C_L\right)$, and so we find

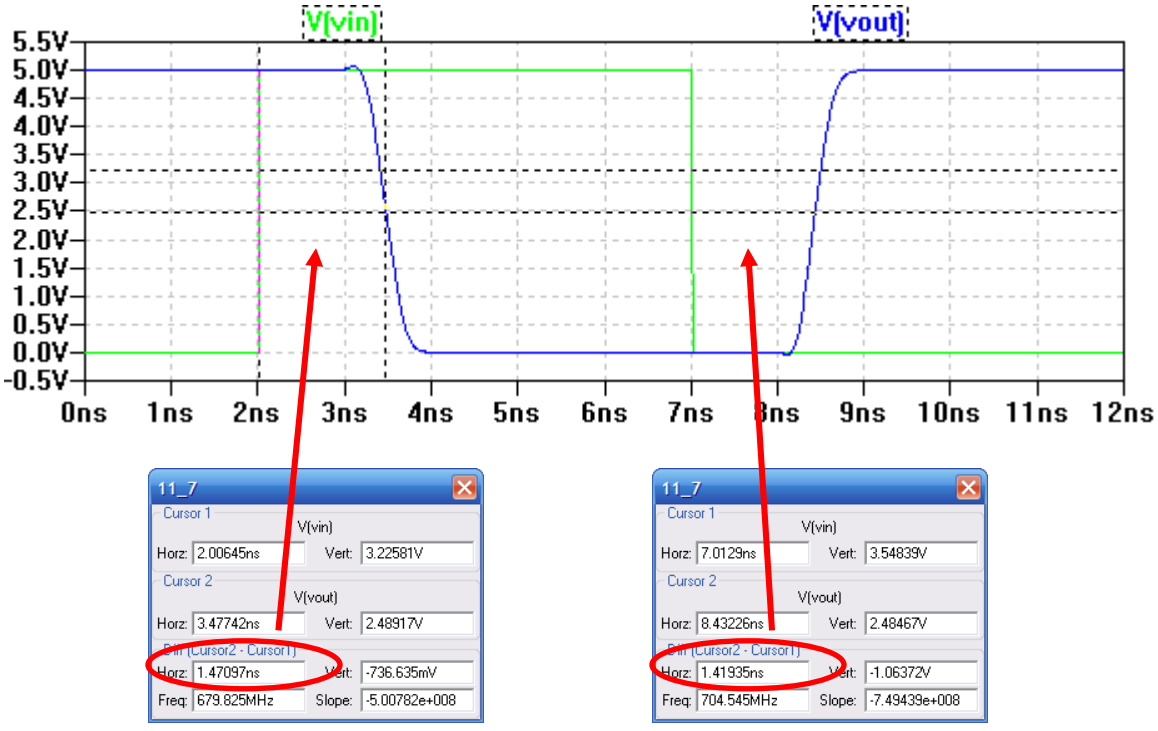
$t_{PHL} + t_{PLH} \approx 0.7\left(1500 + 1500\right)\left(50p\right) = 105ns$ for no buffer.

The simulations show our approximations are, just that, approximations. The simulated results are about 60% of the calculated values. The biggest cause for the discrepancy is most likely lower actual channel resistances (R_N and R_P) than the values used in calculations.

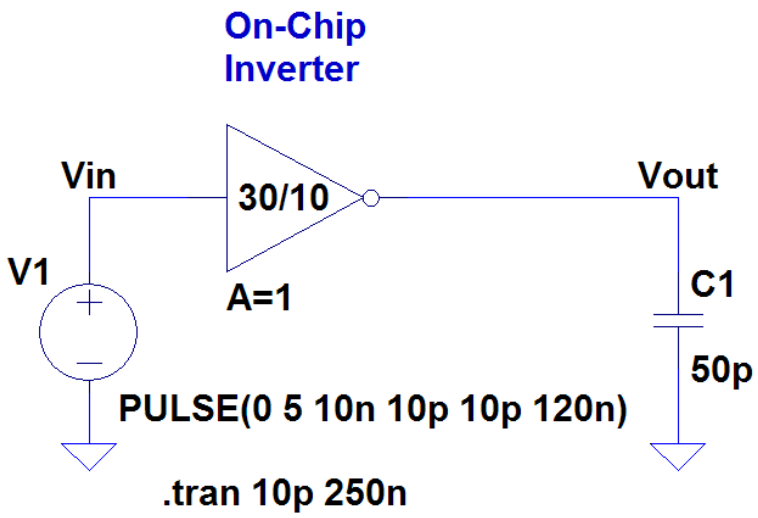
The following are the simulation results:

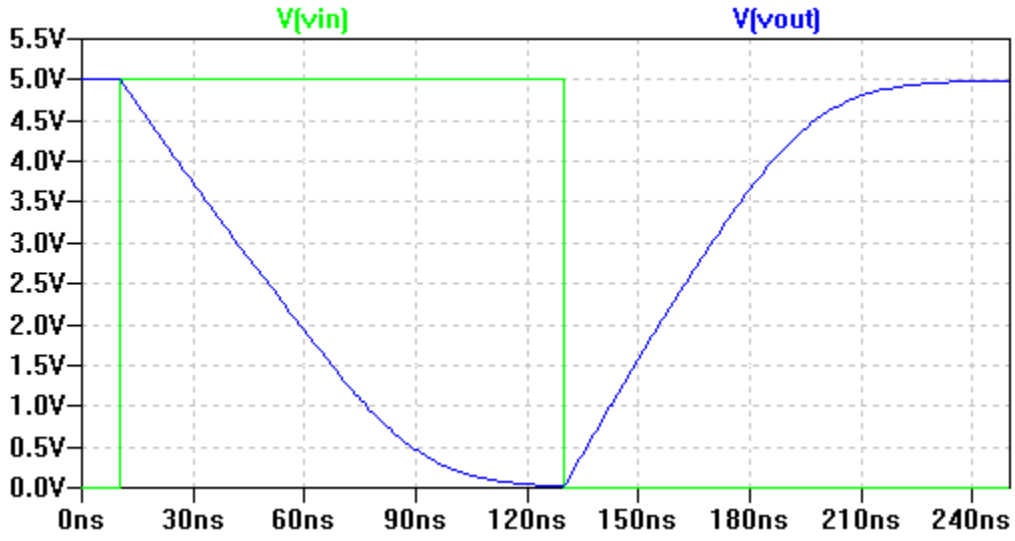






Simulation results: $t_{PLH} + t_{PHL} = 1.47n + 1.42n = 2.89ns$.





Simulation results: $t_{PLH} + t_{PHL} = 40n + 32n = 72n$. ■

Problem 11.8 **Harish Reddy Singidi**

Repeat problem 11.7 using an area factor, A of 8.

Solution: -

A = 8

Cin1 = 1.5 (Coxn + Coxp)

Cin1 = 1.5 ((1.75)(30) + (1.75)(10))

Cin1 = 105fF

Cout1 = Coxn1 + Coxp1 = (1.75)(10)(1.75)(30) = 70fF

Rn1 = 15K/10 = 1.5K

Rp1 = 15K/10 = 1.5K

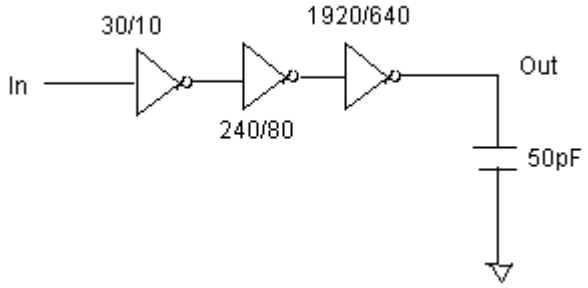
N = ln((Cload/Cin1))/ln(A)

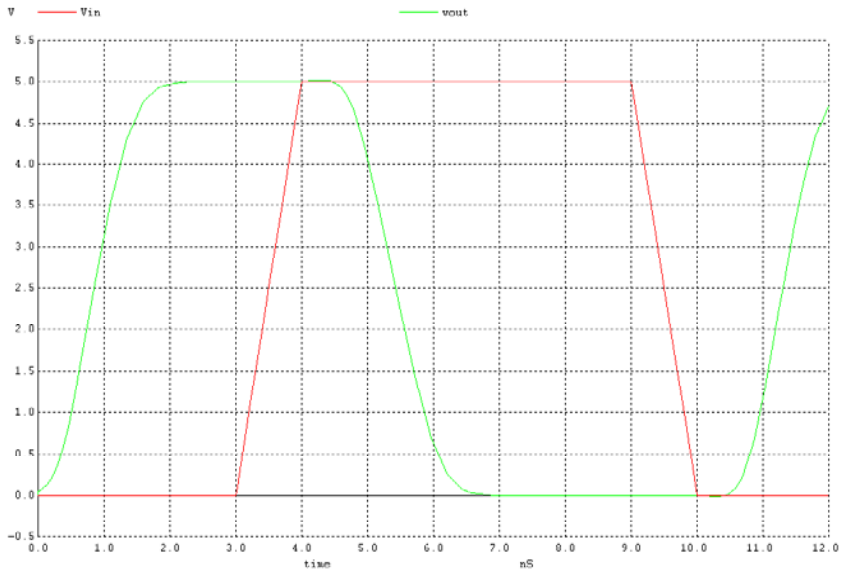
N= 2.9 Stages = 3 Stages

(TPHL + TPLH) = 0.7* N(Rn1+Rp1)(Cout1+A*Cin1)

(TPHL + TPLH) = 0.7* 3*(1.5K+1.5K)(70fF+8*105fF)

(TPHL + TPLH) = 5.73ns





11.9) Derive an equation for the switching point voltage, similar to the derivation of Eq(11.4), for the NMOS inverter seen in Fig11.24a.

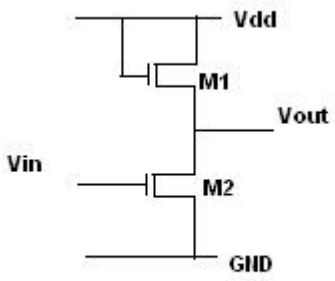
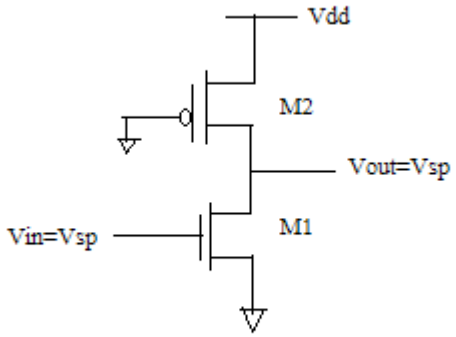


Fig 11.24a

To find the switching point voltage, let Vin=Vout=Vsp
At the conditions mentioned above, both M1 and M2 are in saturation.
So I_{ds1} (sat)=I_{ds2} (sat)
$(ß_{n2}/2)(V_{sp}-V_{thn2})2= (ß_{n1}/2)(V_{dd}-V_{sp}-V_{thn1})$
Solving for Vsp gives
$V_{sp}= [V_{thn1}\sqrt{(ß_{n1}/ ß_{n2})} + (V_{dd}-V_{thn2})] / [1 + \sqrt{(ß_{n1}/ ß_{n2})}]$
If $ß_{n1}=ß_{n2}$ and $V_{thn2} =V_{thn1}$, then
$V_s= V_{dd}/2$.

Problem 11.10 **Rupa Balan**

Repeat problem 11.9 for the inverter in fig 11.24c. Note that the PMOS transistor is operating in the triode region when the input/output are at V_{sp}.



Given M2 is in the triode region.

For M1 to be in saturation, $V_{ds} > V_{gs} - V_{thn}$

$V_d > V_g - V_{thn}$

$V_{thn} > 0$ ($V_d = V_g = V_{sp}$)

Hence M1 is in saturation.

Current through M1, $I_{DN} = (\beta_n/2)(V_{sp} - V_{thn})^2$

Current through M2, $I_{DP} = \beta_p [((V_{dd} - V_{thp})(V_{dd} - V_{sp})) - ((V_{dd} - V_{sp})^2/2)]$

Equating the currents, $(\beta_n/2)(V_{sp} - V_{thn})^2 = \beta_p [((V_{dd} - V_{thp})(V_{dd} - V_{sp})) - ((V_{dd} - V_{sp})^2/2)]$

Simplifying we get,

$\beta_p/\beta_n = (V_{sp} - V_{thn})^2 / [(V_{dd} - V_{thp})^2 - (V_{sp} - V_{thp})^2$

Cross-multiplying we get an equation of the form

$aV_{sp}^2 + bV_{sp} + c = 0$

where

$a = \beta_n + \beta_p$

$b = -2(\beta_n V_{thn} + \beta_p V_{thp})$

$c = \beta_n V_{thn}^2 - \beta_p V_{dd}^2 + 2\beta_p V_{dd} V_{thp}$

This is a quadratic equation which can be solved to get V_{sp}.