Submitted by L. Bollschweiler
Lincolnbollschweiler@gmail.com

3.1 Redraw the layout and cross-scctional views of a pad, similar to Fig. 3.2, if the final pad size is 50µm x 75µm with a scale factor 100nm.

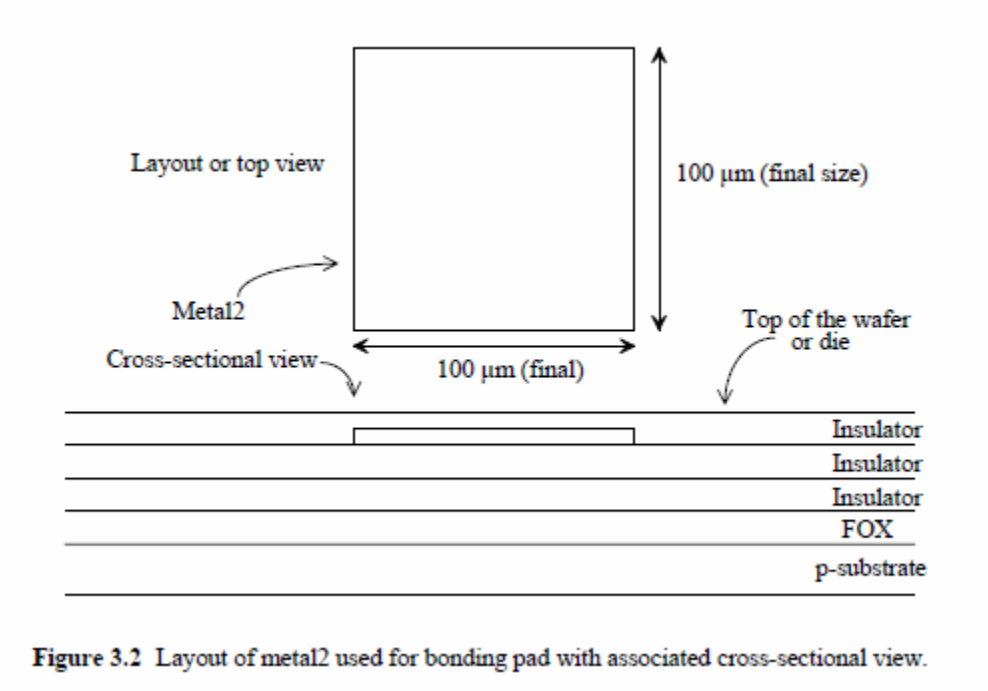
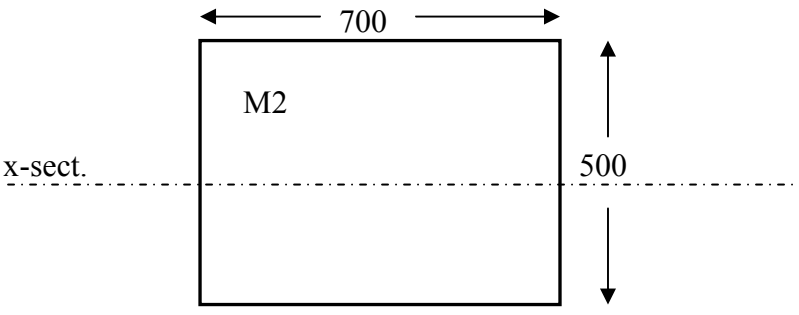
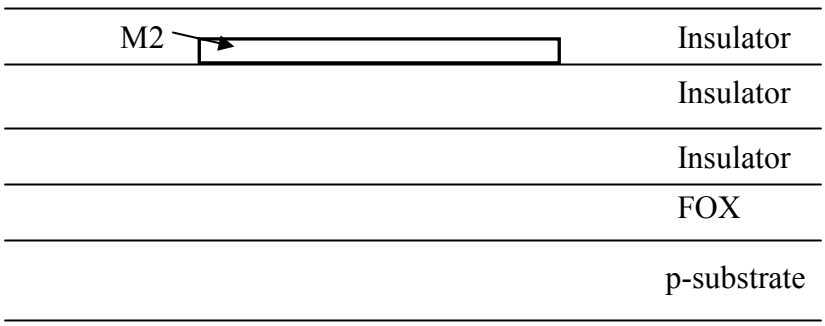


Figure 3.2 Layout of metal2 used for bonding pad with associated cross-sectional view.

Units = Size / scale. W = 70µm/100nm = 700units. L = 50µm/100nm = 500 units.





3.2 Estimate the capacitance to ground of the pad in Fig.3.20 made with both metal1 and metal2.

Soln:

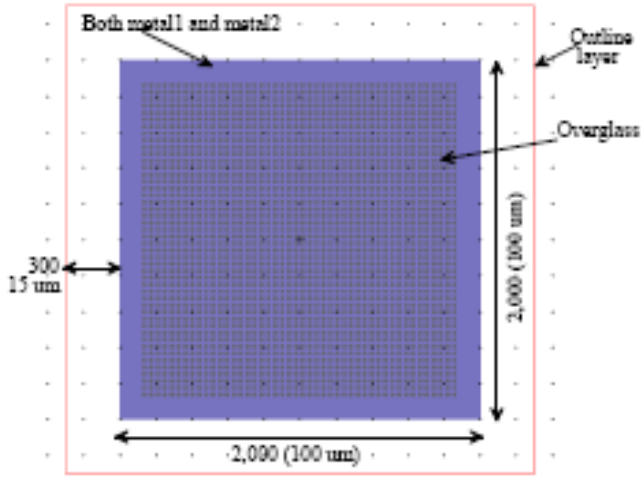
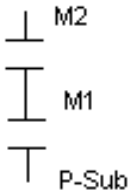


Figure 3.20 Layout of the bonding pad.

M1 and M2 are connected through vias, thus capacitance from M2 to M1 or M2 to substrate is not applicable, leaving only the capacitance from M1 to P-Sub.



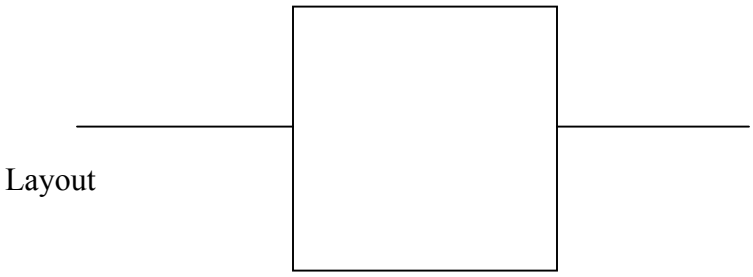
$$C_{1sub} = area \times C_{plate} \times Scale^2 + permeter \times C_{fringe} \times Scale$$

Getting the values of C_{plate} *and* C_{fringe} *from table 3.1 on page 61*

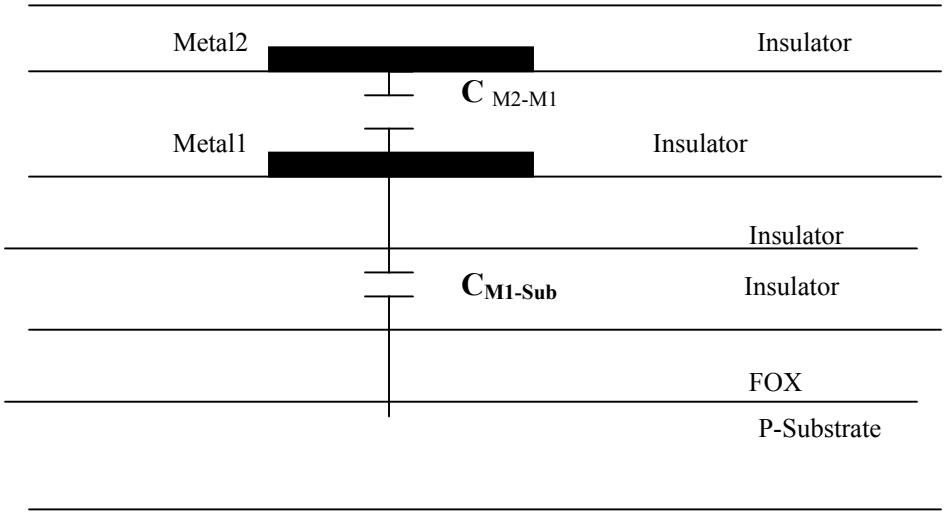
$C_{1sub} = 2000^* \ 2000^* \ 23aF/um2 \ ^*(50nm)^2 + 2000^* \ 4^*79aF/um^*50nm$
$C_{1sub} = .26\ pF$

Harish Reddy Singidi

3.3) Suppose a parallel plate capacitor was made by placing a 100μm square piece of metal1 directly over metal1 below metal2 in Fig: 3.2. Estimate the capacitance between the two plates of the capacitor. Estimate the capacitance from metal1 to substrate.



Cross section view



$\mathbf{C}_{M1\text{-}M2}$ = Area . Plate capacitance + perimeter . Fringe capacitance

$\mathbf{C}_{M1\text{-}M2} = (100\mu m)^2 . 35\ aF/\mu m^2 + 400\ \mu m . 100aF/\mu m$

$\mathbf{C}_{M1\text{-}M2} = 390fF$

$C_{M1\text{-}Sub} = (100\mu m)^2 . 23\ aF/\mu m^2 + 400\ \mu m . 79aF/\mu m$

$C_{M1\text{-}Sub} = 261.6fF$

3.4 Sketch the cross section for the layout seen in Fig 3.26

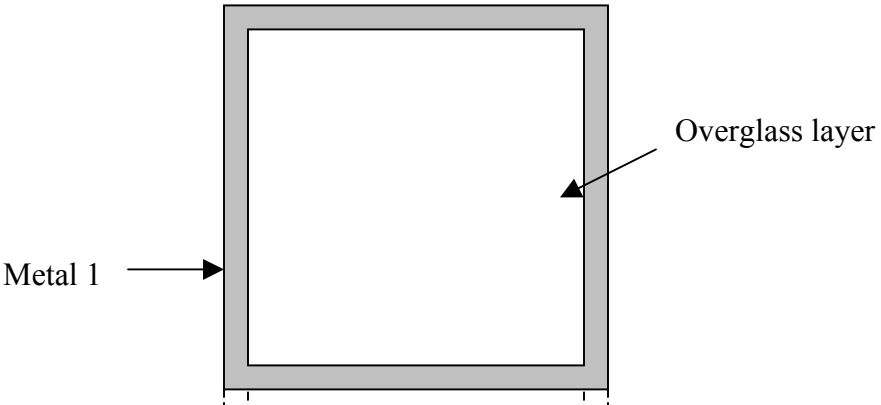
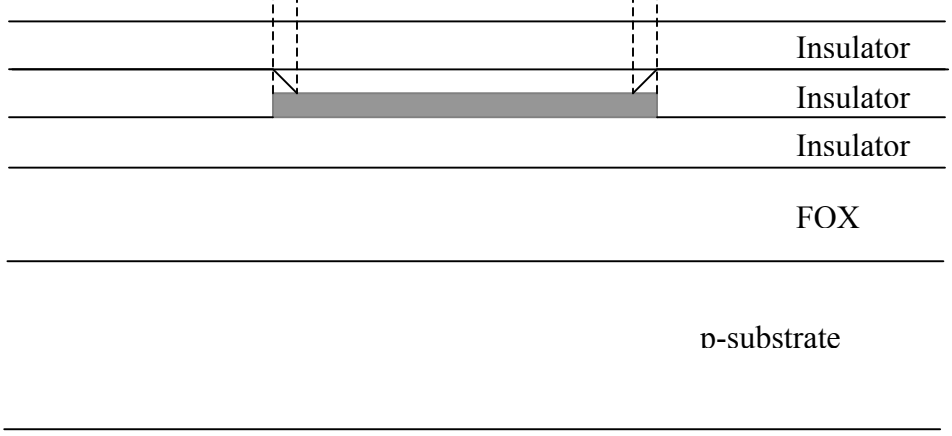


Fig. 3.26 Layout used in Problem 3.4

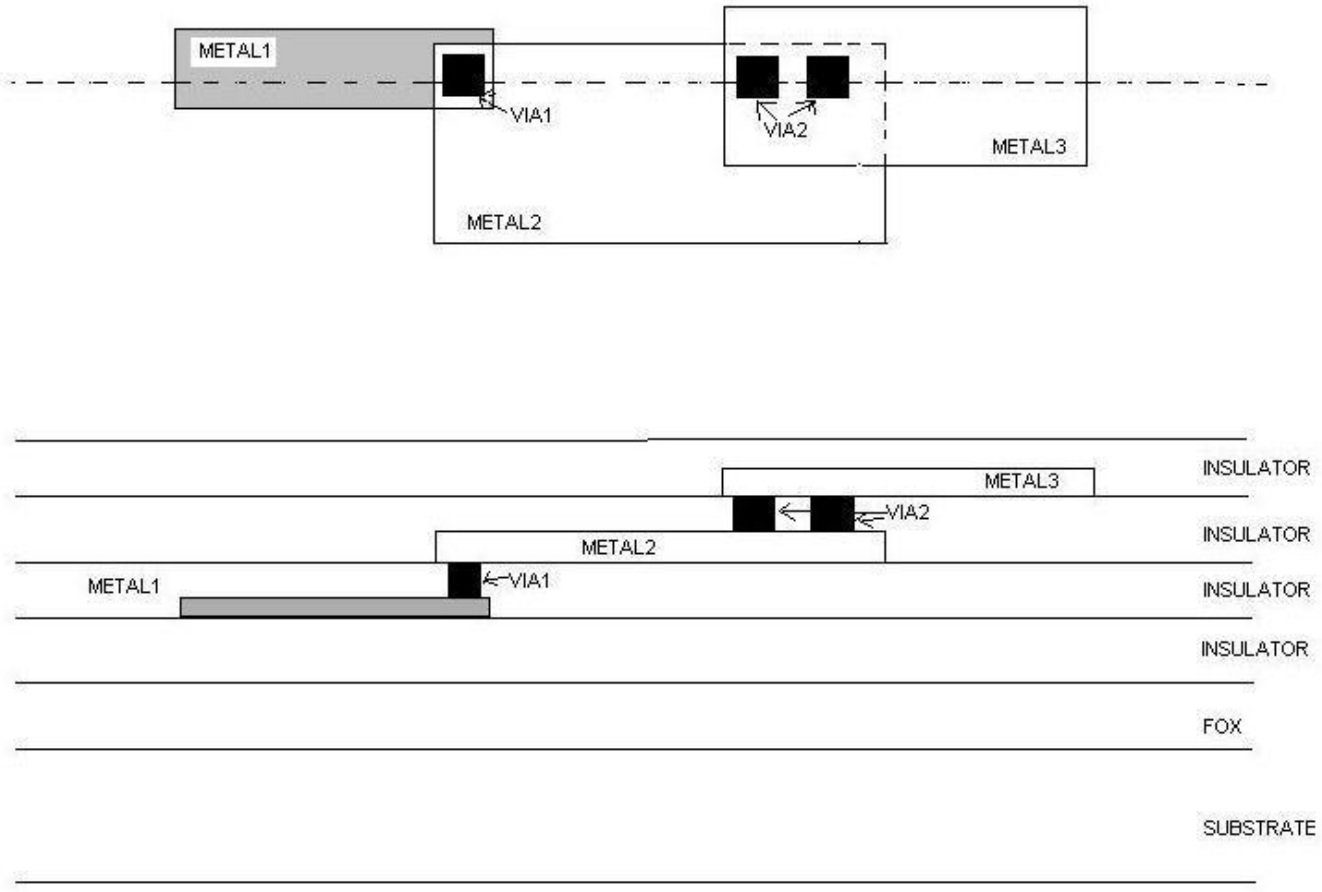
Sol:



KRISHNAMRAJU KURRA

Q #3.5: Sketch the cross-sectional view, at the dashed line, for the layout seen in Fig.3.27. What is the contact resistance between metal3 and metal2.

Figure: 3.27



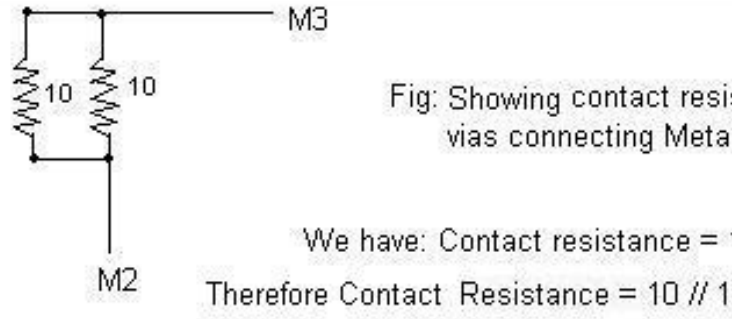


Fig: Showing contact resistance of the two vias connecting Metal3 and Metal2.

We have: Contact resistance = 10 ohms/ contact.

Therefore Contact Resistance = 10 // 10 = 10/2 = 5 ohms.

Problem 3.6 Edward Kunz

Estimate the intrinsic propagation delay through a metal line encapsulated in an ILD with a relative dielectric constant of 1.5. What value metal sheet resistance, using the values from ex 3.3 would be required if the RC delay through metal the metal line is equal to the intrinsic delay?

$t_{d\ intrinsic} = \frac{\sqrt{\varepsilon}}{c} = \frac{\sqrt{1.5}}{3*10E8} =$ 4ns/meter = 4ps/mm

$t_{d\ metal} = .35 * R * C$

4ps = .35*R*162fF

$R = \frac{4\,ps}{.35*162\,fF} = 70\Omega$

$R\ sheet = \frac{70\Omega}{5000} = .014\Omega$

3.7

Using *CV=Q* rederive the results in Ex. 3.5.

We have 10 by 10 square piece of metal1 and an equal-size piece of metal2 placed exactly above the metal1 piece.
Scale factor = 50nm.
C. V = Q

For metal 2 to metal 1 $C_{12} . V_{12} = Q_{12}$
For metal 1 to substrate $C_{1sub} V_{1sub} = Q_{1sub}$

From the circuit $Q_{12} = Q_{1sub}$

Implies $C_{12.} V_{12} = C_{1sub} V_{1sub}$

Implies $C_{12} (\Delta Vm2 - \Delta V_{m1}) = C_{1sub.} (\Delta V_{m1} - 0)$ ---- (1)

From ex 3.5:

$C_{12} = 10. 10. (0.05)^2. 35$ aF + 40 (0.05). 100 aF

Implies $C_{12} = 209$ aF

$C_{1sub} = 10. 10. (0.05)^2. 23$ aF + 4. 10. (0.05) 79 aF

Implies $C_{1sub} = 164$ aF

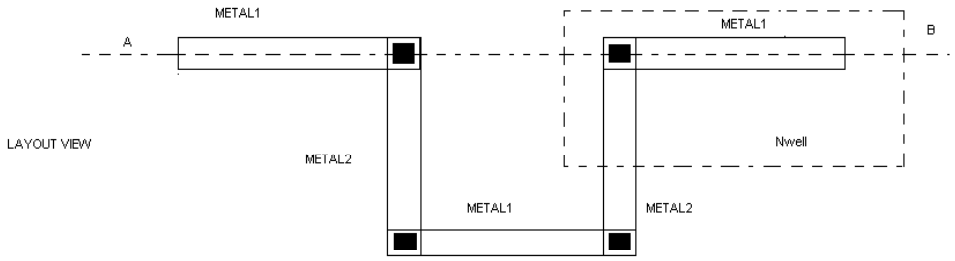
Equation ---(1) implies 209 aF $(1- \Delta V_{m1}) = 164$ aF (ΔV_{m1})

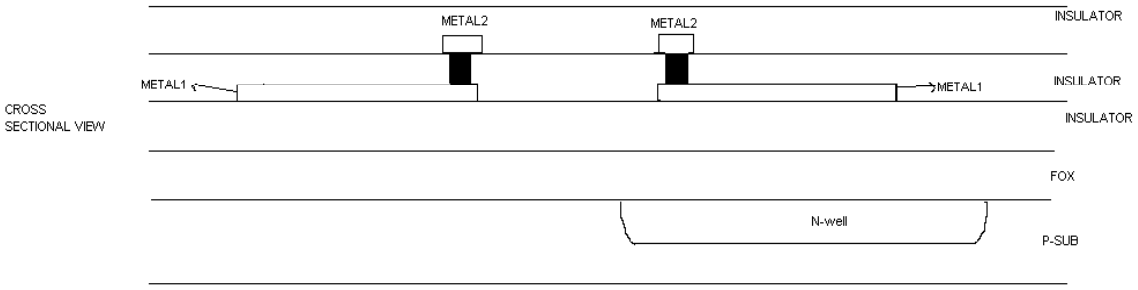
Implies $\Delta V_{m1} = 209/ (209+ 164) = 560$ mV

Therefore $\Delta V_{m1} = 560$ mV

PROBLEM 3.8) For the layout seen in figure below sketch the cross-sectional view(along the dotted line) and estimate the resistance between points A and B. Remember a via is sized 1.5 by 1.5.

Solution:-





Given metal sheet resistance =0.1 ohm/square
Metal contact resistance = 10 ohms
I assumed that there are 7 squares in each metal (between A and B)
The total resistance between A and B = (6+5+5+5+6) x (0.1ohm/square) + 4 x (10 ohms)
= 2.7 + 40
= 42.7 ohms(approximately)

--Steve Bard

Problem 3.9

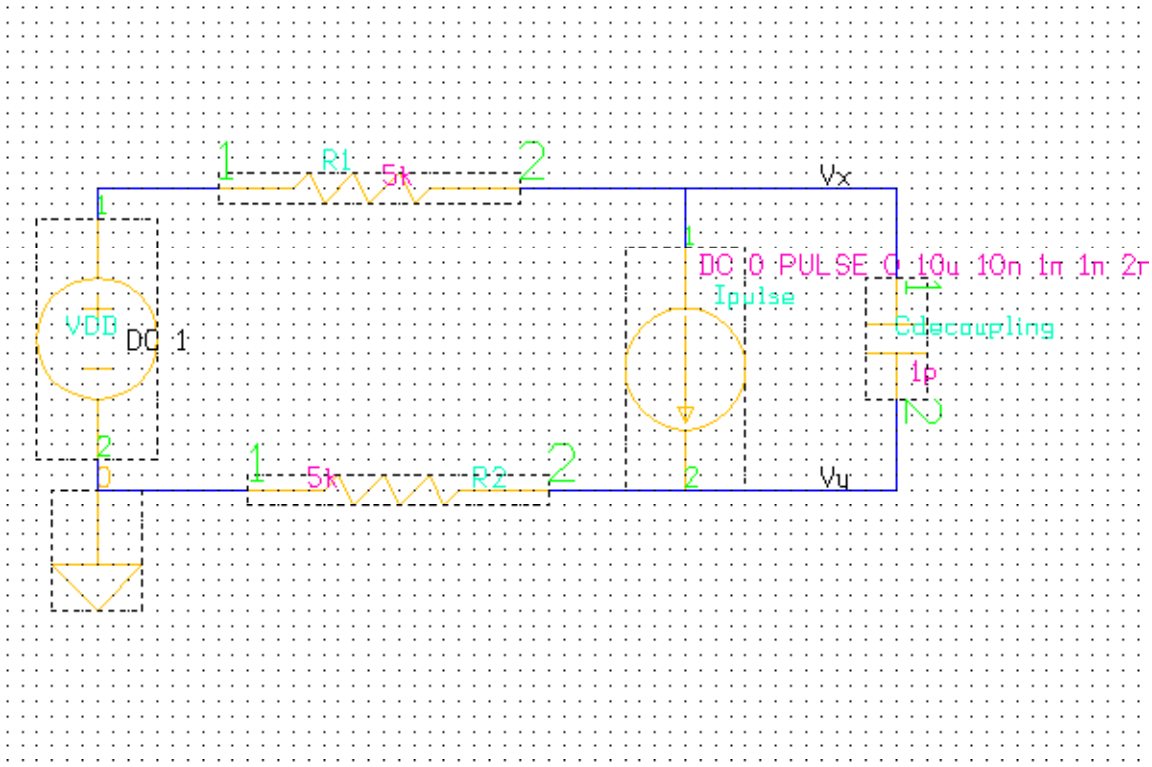
Question: Laying out two metal wires directly next to each other, and with minimum spacing, for a long distance increases the capacitance between the two conductors, C_m. If the two conductors are V_{DD} and ground, is this a good idea? Why or why not?

Answer: Yes, this is a good idea. The mutual capacitance between the wires, C_m, serves as a decoupling capacitor that supplies charge during transient periods. That capacitance helps keep the wires at their respective voltages, V_{DD} and ground, when the circuit in the chip begins drawing power.

EE 510 SPRING 2004 HOMEWORK 4

MAEZLIN J AVILA TAYLOR

P3.10 Consider the following schematic:

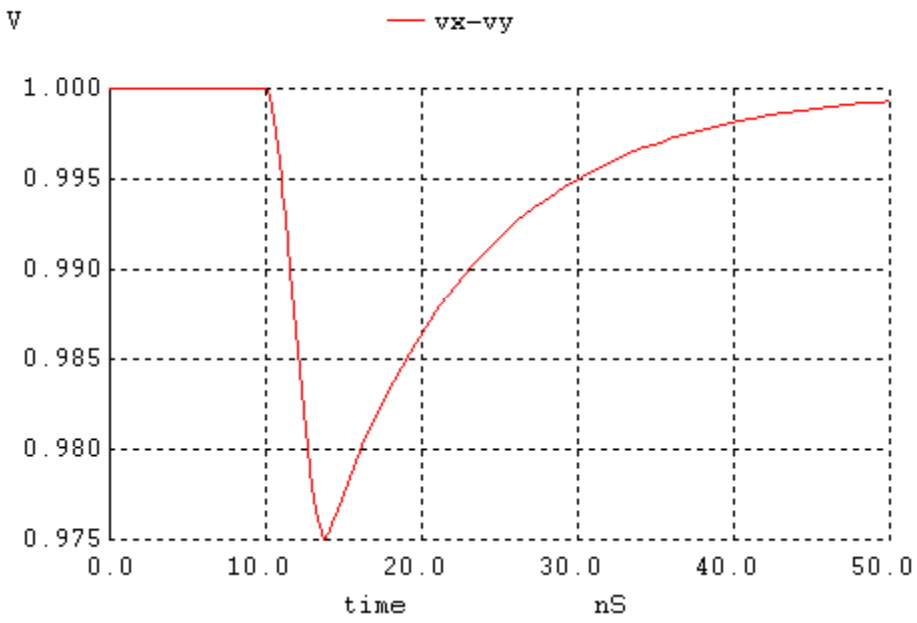


This circuit can be used to model ground bounce and VDD droop. Show, using SPICE, that a decoupling capacitor can be used to reduce these effects for various amplitude and duration current pulses.

The schematic drawn in LASI creates the following .CIR file:

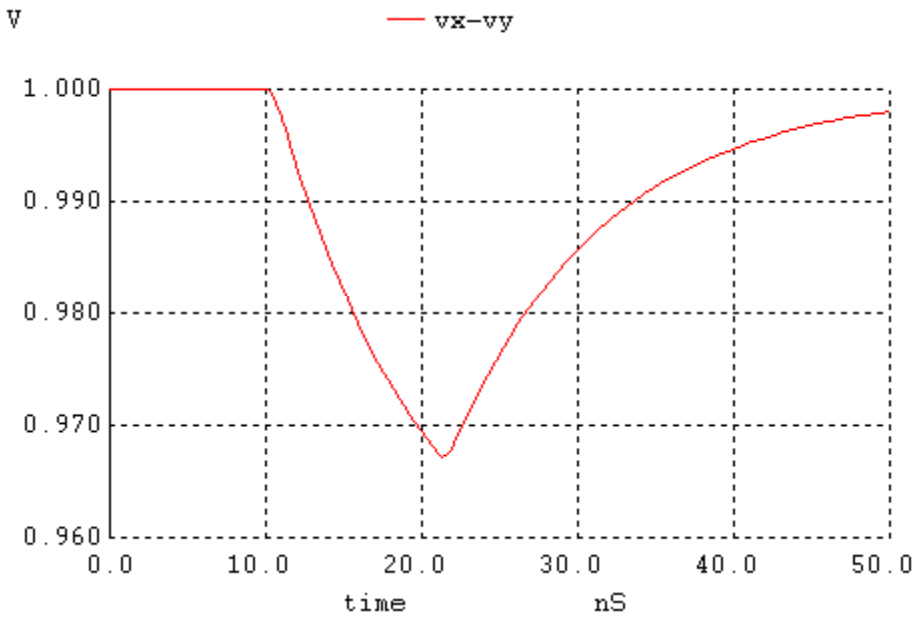
```
*** SPICE Circuit File of 3_10_SCH

.control
destroy all
run
plot vx-vy
.endc

.tran 1n 50n

* End of E:\Lasi7\Mosis\3_10_sch.hdr

* MAIN 3_10_SCH
Cdecoupling Vx Vy 1p
Ipulse Vx Vy DC 0 PULSE 0 10u 10n 1n 1n 2n 50n
R1 vn1 Vx 5k
R2 0 Vy 5k
VDD vn1 0 DC 1
.END
```

This file plots the difference between the model VDD and model ground nodes:

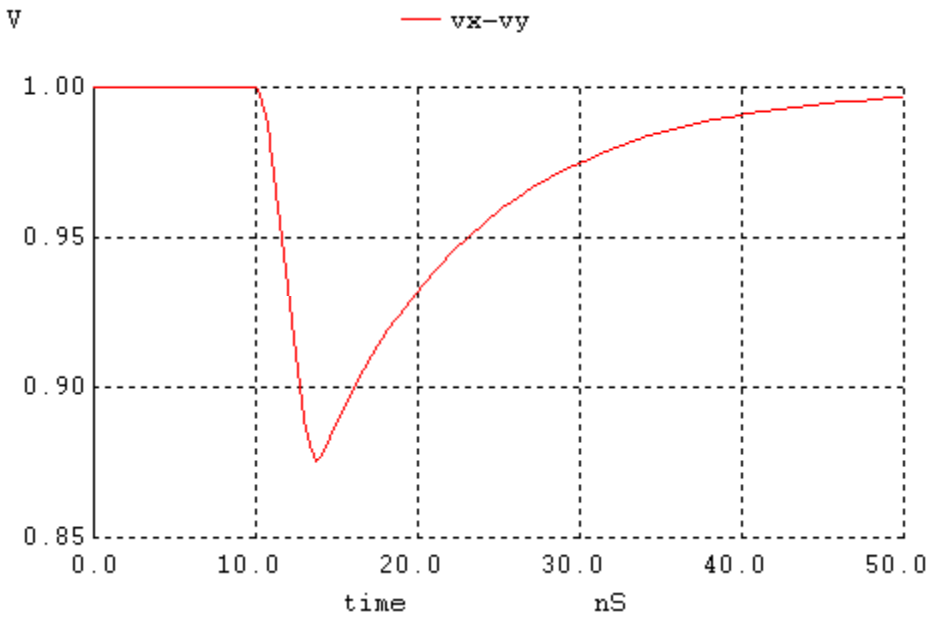


The 1pF capacitor controls the droop/bounce caused by a 10uA current spike resulting in a minimal 2.5% change.

A longer pulse, 10ns, of the same amplitude results in a slightly more significant change of 4.75%:



A bigger pulse, such as 50uA results in a significant 15% change:



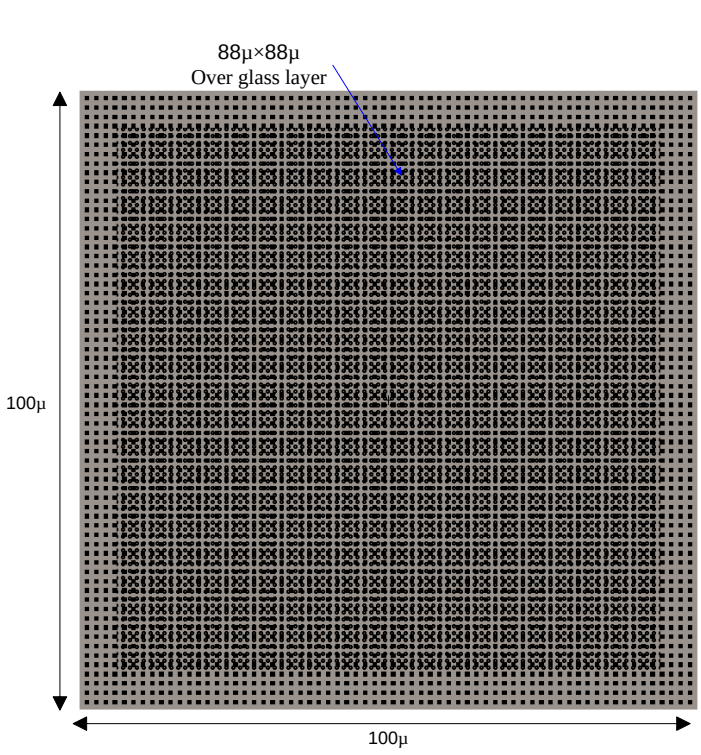
3.11) Lay out the pad frame specified by the information in Table 3.2. Assume a 3 metal CMOS process is used. Comment on how the scale factor affects the (drawn) layout size.

Sol: - As stated in the book Table 3.2 is given as below:-

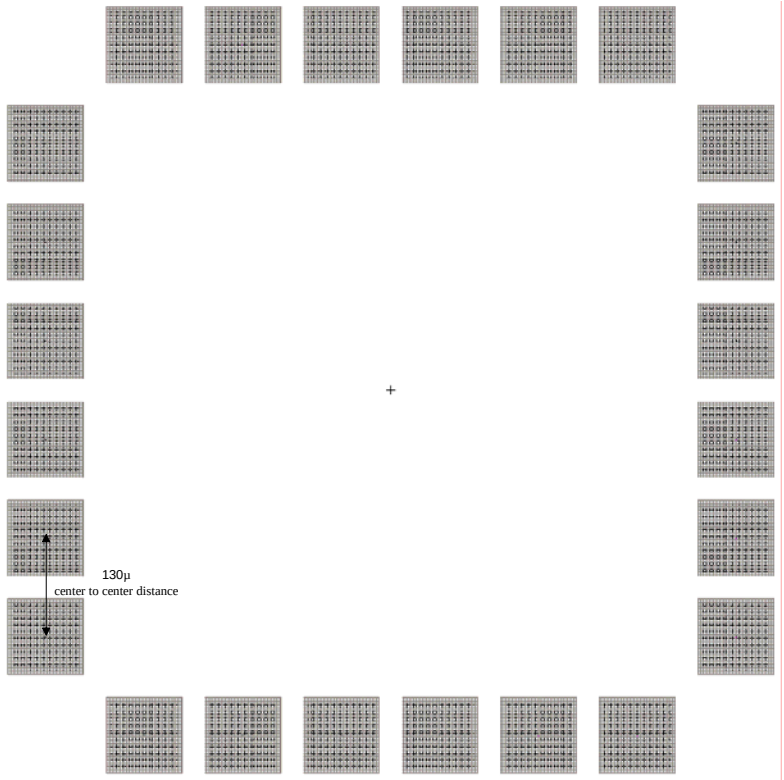
Sizes for an example 1 mm square chip with a scale factor of 50 nm.

	Final size	Scaled size
Pad size	100 μm by 100 μm	2,000 by 2,000
Pad spacing (center to center)	130 μm	2,600
Number of pads on a side (corners empty)	6	6
Total number of pads	24	24
Overglass opening	88 μm by 88 μm	1,760 by 1,760

Layout of single pad & pad frame is as shown below:-



Metal-3 to Metal-2 to Metal-1 Pad



24 pin pad frame

Scale factor determines the actual size of the feature being fabricated on the wafer. Actual size = scale factor × drawn size; smaller the scale factor smaller is the actual size and thus more number of die per wafer can be processed which makes the product cheaper because, processing cost per wafer is fixed.

-Shantanu Gupta

3.12 Propose, and lay out, a test structure to measure the sheet resistance of metal3. Comment on the trade-offs between accuracy and layout size. Using your test structure provide a numerical example of calculating sheet resistance for metal3.

Solution:

Let's get started by writing down the equation for calculating the resistance

$$R = R_{\square} \cdot N + \sum_{i=1}^{N} \Delta R_i \tag{1}$$

where $R_{\square}$ is the sheet resistance, ΔR_i is the variation of the i-th sheet resistance, and N is the total number of $R_{\square}$. If the layout is relatively large and symmetrical, the error term is averaged to zero

$$\sum_{i=1}^{N} \Delta R_i \to 0 \tag{2}$$

Also notice that the resistance of the conductor (metal3) is probably very small. Intuitively we know that a number of $R_{\square}$ is necessary in order to minimize the error and to avoid electromigration. Since we also don't want the layout size to be too large, the test structure may be laid out in a serpentine pattern, Fig. 1.

Figure 1: A test structure in serpentine pattern.

The overall resistance between A and B is

$$R_{AB} = \frac{V_{AB}}{I_{AB}} = R_{\square} \cdot (N_R \cdot N_L + N_V + 0.6 \cdot N_C + 2) \tag{3}$$

where N_R is the number of rows, N_L is the number of $R_{\square}$ within a row excluding the corners, N_V is the total number of $R_{\square}$ between corners in the vertical lines, and N_C is the number of corners (note that the corner sheet resistance is estimated to be $0.6\,R_{\square}$). If we lay out the test structure so that in Fig. 1 $W_{Gap} = W_L$, we have

$$\begin{aligned} N_V &= N_R - 1 \\ N_C &= 2N_R - 2 \end{aligned} \tag{4}$$

Thus rewriting Eq. (3) we get

$$R_{\square}=\frac{V_{AB}}{I_{AB}}\cdot\frac{1}{[(N_L+2.2)N_R-0.2]} \tag{5}$$

Knowing N_L and N_R we can use Eq. (5) to estimate the sheet resistance.

Suppose we are tasked to measure the metal3 sheet resistance of the ON Semiconductor C5 process (the scaling factor $\lambda=300\,nm$) [1]. Before we starting layout, let's take a look at the sheet resistance for different processes [2]:

Process	Metal3 Sheet Resistance (Ω)
IBM 130 nm	0.05
IBM 90 nm	0.08
TSMC 180 nm	0.04
TSMC 350 nm	0.07

We can make a guess that metal3 sheet resistance of the C5 process may be around $0.05\,\Omega$. Lets lay out a test structure consists of approximately 5000 $R_{\square}$ in order to reduce the error term in Eq. (1). Lets also try to avoid elecromigration as well as large layout size by setting the width of the metal3 to be twice of the minimum in DRC rules, or a drawn width of 10. If there are 100 $R_{\square}$ in a single row of the structure, we then need about 50 rows. This layout is shown in Fig. 2.

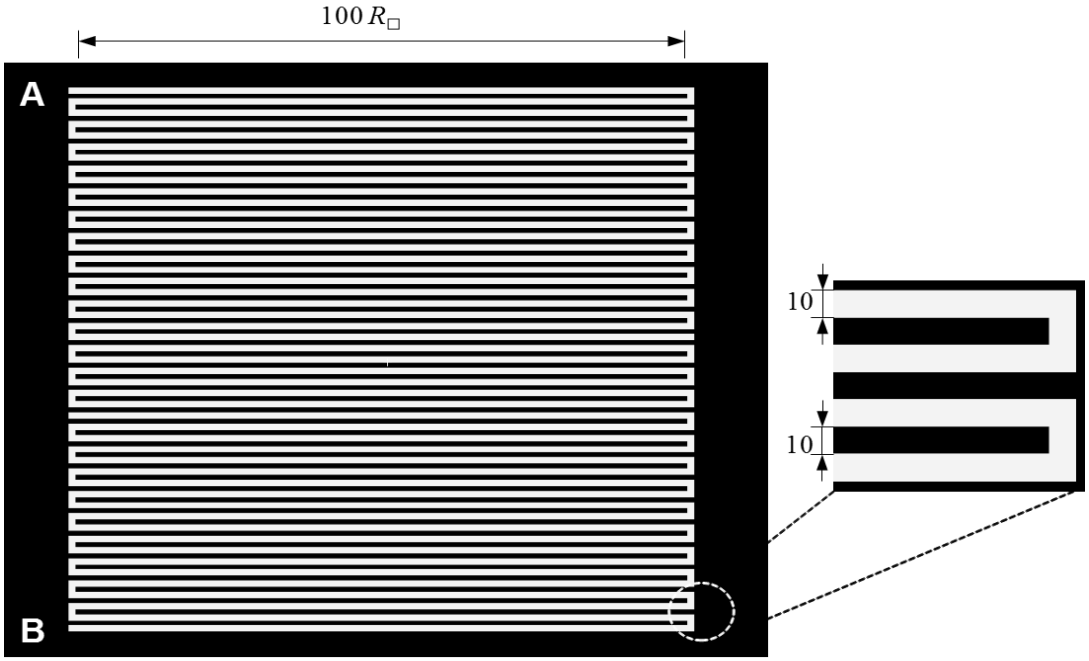


Figure 2: A test structure layout in a serpentine pattern.

Since there are corners in the serpentine pattern, the layout in Fig. 2 only has 49 rows. Therefore $N_R = 49$ and $N_L = 100$. Using Eq. (5), the relation between $R_\square$ and test voltage V_{AB} and measured current I_{AB} is

$$R_\square = \frac{V_{AB}}{I_{AB}} \cdot 199.7 \times 10^{-6} \tag{6}$$

A chip fabricated through MOSIS may be $1.5\,mm \times 1.5\,mm$. The width of this structure is roughly $100 \cdot 10 \cdot \lambda = 0.3\,mm$, or 1/5 of the total chip width. If more accurate result is needed, we can increase the total number of $R_\square$ (a larger layout size).

A final comment is about the electromigration. The metal width in this layout is $10 \cdot \lambda$, or $3\,um$. A typical current threshold for avoiding electromigration effect is $1\,mA/um$. Thus the maximum allowed current flowing through this structure is $3\,mA$. Assume $R_\square = 0.05\,\Omega$, using Eq. (6), the voltage applied to the test structure should not exceed 0.75V.

Reference:

[1] ON Semiconductor C5 Process, http://www.mosis.com/on_semi/c5/

[2] MOSIS fabrication processes, http://www.mosis.com/products/fab/vendors/