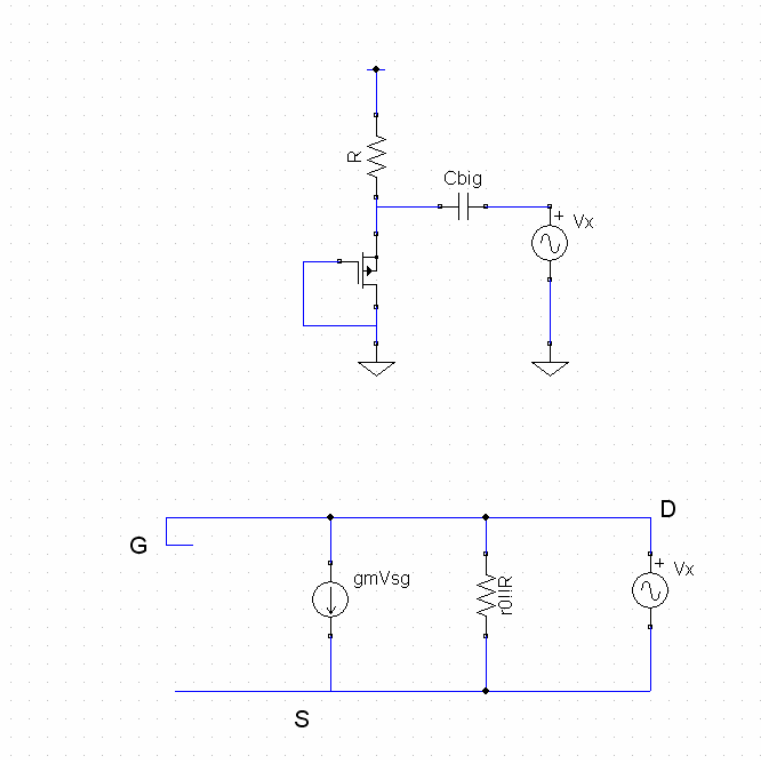
21.1)

To show that the small signal resistance of a gate drain connected PMOS device behaves like a resistor with a value of $1/g_m$.



The small signal equivalent circuit to determine the small signal resistance is shown above.

From the above circuit we can see that

$$V_{gs} = V_x$$

Therefore we can write

$$I_x = \frac{V_x}{r_o} + g_m V_x$$

$$= V_x\left(\frac{1}{r_o} + g_m\right)$$

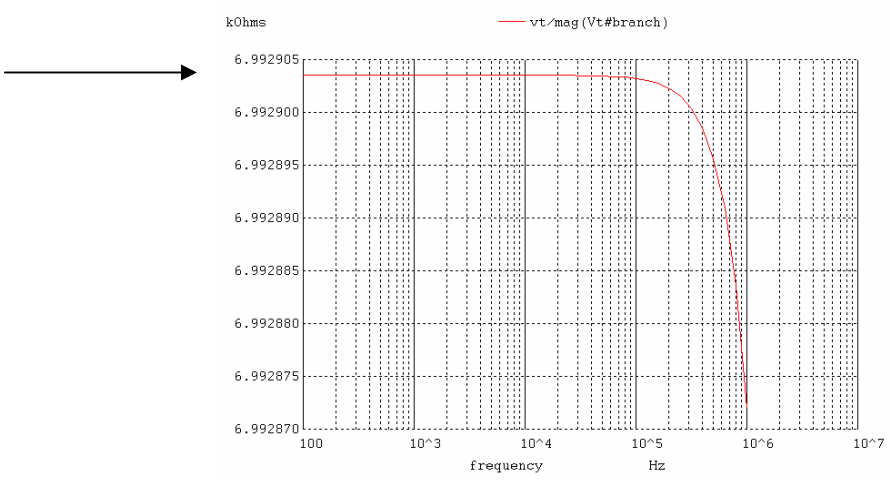
Therefore from the above relation we can write the small signal resistance of the gate drain connected MOSFET is given as

$$\frac{V_x}{I_x} = \frac{1}{\frac{1}{r_o} + g_m}$$

= $1/g_m \,||\, r_o$ which is approximately equal to $1/g_m$

From table 9.2 the small signal resistance is found out to be g_m^{-1} which is equal to 6.66 KΩ.

From simulations it is found out to be: 6.992 KΩ.

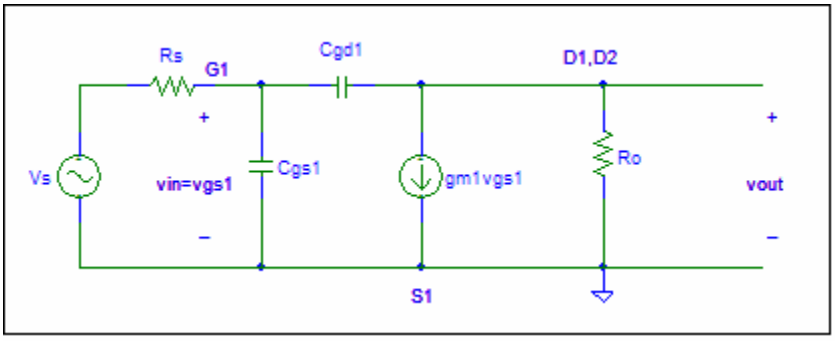


Netlist:

```
.option scale=1u
.control
destroy all
run
plot vt/I(Vt)
.endc
.ac DEC 10 100 1MEG
Vdd vdd 0 DC=5
Vt vt 0 DC=0 AC=1m
C1 vs vt 1
R1 vdd vs 200k
M1 0 0 vs vs pmos L=2 W=30
```

21.2

The circuit used to calculate the transfer function for this circuit would be as below



The transfer function would be Eq. 21.53 without the C_o terms. The zero is located at

$$f_z = \frac{g_{m1}}{2\pi C_{gd1}}$$

The low frequency pole is located at [from Eq. 21.55 removing the C_o terms]

$$f_1 = \frac{1}{2\pi[(C_{gs1} + C_{gd1})R_s + C_{gd1}g_{m1}R_oR_s]}$$

The second frequency pole is located at [from Eq. 21.61 removing the C_o terms].

$$f_2 = \frac{g_{m1}C_{gd1} + (C_{gs1} + C_{gd1})\frac{1}{R_o}}{2\pi C_{gs1}C_{gd1}}$$

We have,

C_{gs1}=23.3fF, C_{gd1}=2fF, R_s= 100k,

R_o=$r_{o1}\|\ r_{o2}$= 5MΩ $\|$ 100k = 98K.

Substituting, we get

f_z = 12 GHz,

f_1= 28.8 MHz,

f_2= 1.91 GHz.

From SPICE simulation

f_z = 12 GHz,

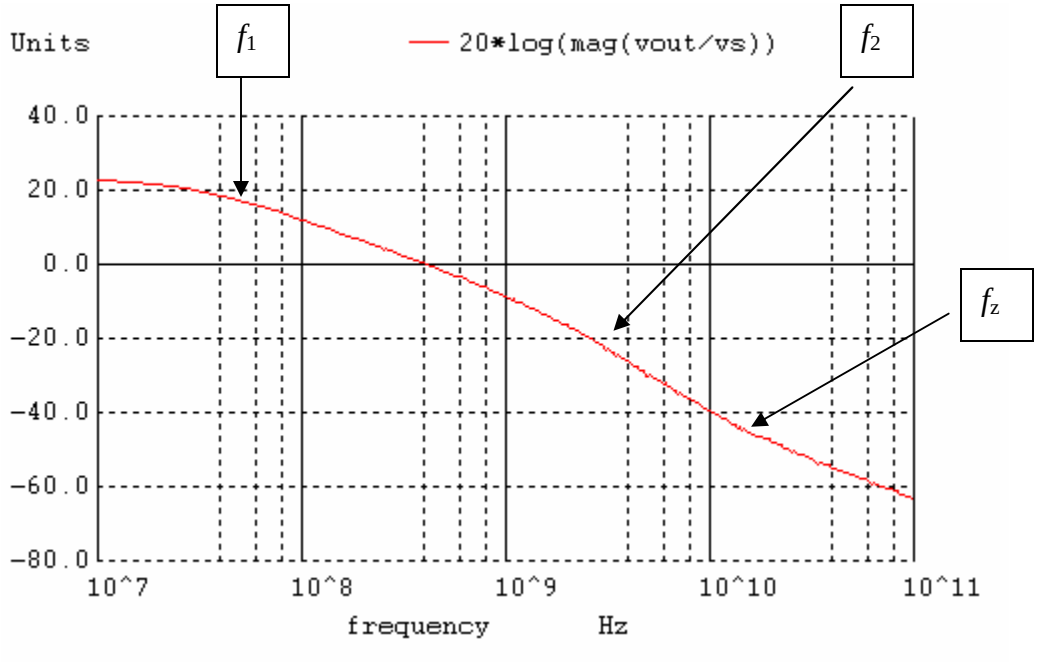
f_1= 30 MHz,

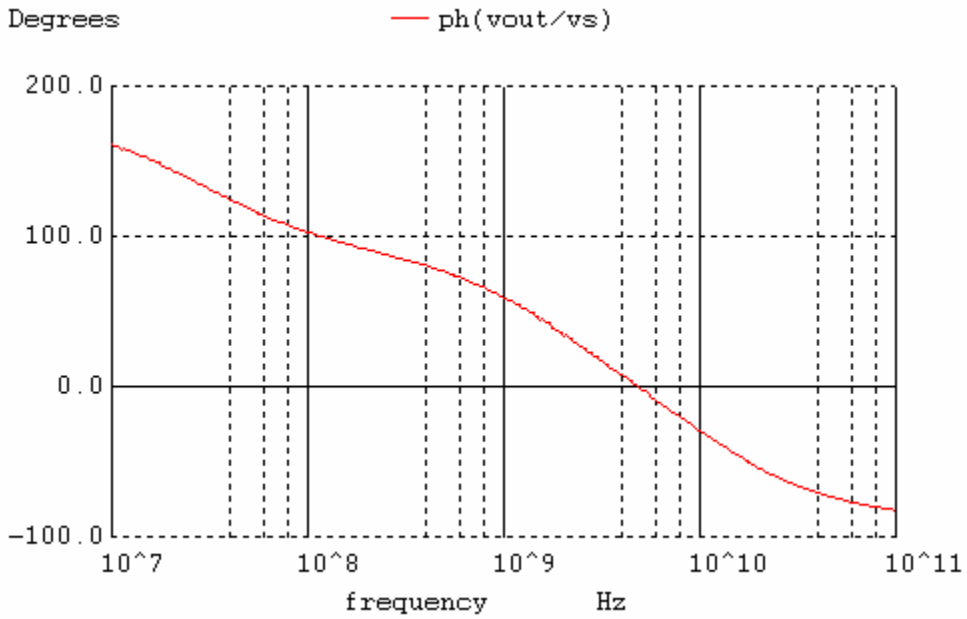
f_2= 2 GHz.

NETLIST

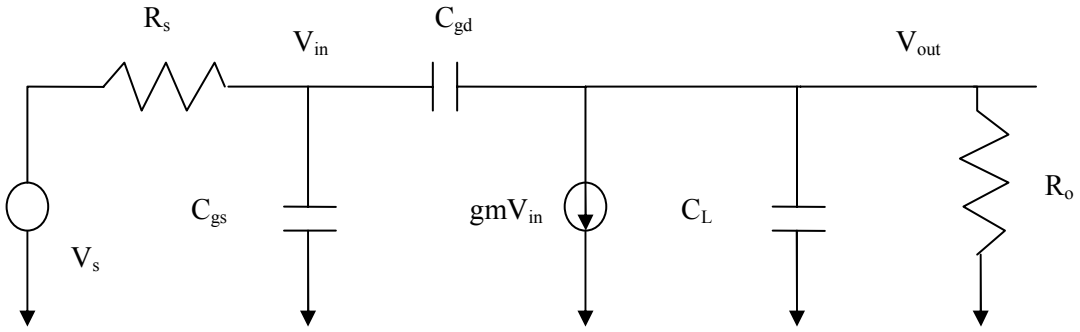
```
.control
destroy all
run
plot 20*log(mag(vout/vs))
set units=degrees
plot ph(vout/vs)
.endc

.option scale=1u
.AC DEC 100 10MEG 100G

VDD     VDD     0       DC      5
Vs      Vs      0       DC      0       AC      1
Rs      Vs      Vss     100k
M1      Vout    Vin     0       0       NMOS L=2 W=10
Rp      vdd     vout    100k
Rbig    Vbias4  Vin     10G
Cbig    Vss     Vin     10

Xbias   VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas biasckt
*from fig. 20.43*
.subckt biasckt VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas
--------
.ends
*BSIM models
--------
.end
```

SIMULATION RESULTS





Problem 21.3



where, $R_o = R \,//\, r_{01}$

$$\frac{V_{in} - V_{out}}{1/\ jwC_{gd}} = gmV_{in} + \frac{V_{out}}{R_o} + \frac{V_{out}}{1/\ jwC_L}$$

$$V_{in}\left[jwC_{gd} - gm\right] = V_{out}\left[\frac{1}{R_o} + jw\left(C_{gd} + C_L\right)\right]$$

$$\therefore V_{in} = \frac{V_{out}\left[\frac{1}{R_o} + jw\left(C_{gd} + C_L\right)\right]}{\left[jwC_{gd} - gm\right]} \qquad \rightarrow (1)$$

and

$$\frac{V_s - V_{in}}{R_s} = \frac{V_{in}}{1/\ jwC_{gs}} + \frac{V_{in} - V_{out}}{1/\ jwC_{gd}}$$

$$V_s - V_{in} = R_s\left[V_{in}\left(jw\left(C_{gs} + C_{gd}\right)\right) - V_{out}\left(jwC_{gd}\right)\right]$$

$$V_s = V_{in}\left[jwR_s\left(C_{gs} + C_{gd}\right)\right] - V_{out}\left(jwR_sC_{gd}\right) \qquad \rightarrow (2)$$

Substituting equation (1) in equation (2) and s = jw, we get

$$V_s = V_{out}\left[\left(1+sR_s\left(C_{gd}+C_{gs}\right)\right)*\frac{\left(\frac{1}{R_o}+s(C_L+C_{gd})\right)}{\left(sC_{gd}-gm\right)}-sR_sC_{gd}\right]$$

$$V_s = V_{out}\left[\frac{1+s\left[R_s\left(C_{gd}+C_{gs}\right)+R_o\left(C_L+C_{gd}\right)+R_oR_sC_{gd}gm\right]+s^2\left[R_oR_s\left(C_LC_{gs}+C_LC_{gd}+C_{gs}C_{gd}\right)\right]}{R_o\left(sC_{gd}-gm\right)}\right]$$

$$\frac{V_{out}}{V_s} = \frac{-gmR_o\left(1-\frac{sC_{gd}}{gm}\right)}{1+s\left[R_s\left(C_{gd}+C_{gs}\right)+R_o\left(C_L+C_{gd}\right)+R_oR_sC_{gd}gm\right]+s^2\left[R_oR_s\left(C_LC_{gs}+C_LC_{gd}+C_{gs}C_{gd}\right)\right]}$$

From the above equation, we have

$$f_z = \frac{gm}{2\pi * C_{gd}} \qquad \rightarrow (3)$$

$$f_1 = \frac{1}{2\pi\left[R_s\left(C_{gd}+C_{gs}\right)+R_o\left(C_L+C_{gd}\right)+R_oR_sC_{gd}gm\right]} \qquad \rightarrow (4)$$

$$f_2 = \frac{R_s\left(C_{gd}+C_{gs}\right)+R_o\left(C_L+C_{gd}\right)+R_oR_sC_{gd}gm}{2\pi\left[R_oR_s\left(C_LC_{gs}+C_LC_{gd}+C_{gs}C_{gd}\right)\right]} \qquad \rightarrow (5)$$

Using the values from Table 9.1, i.e.,
C_{gd} = 2 fF
C_{gs} = 23.3 fF
gm = 150 μA/V
r_{01} = 5 MΩ

And from the given circuit
R = 100 KΩ
C_L = 100 fF
R_s = 100 KΩ

$R_o = r_{01} // R$
$R_o \approx R$ since $r_{01} >> R$

Substituting these values in (3), (4) and (5) we get

$f_z = 11.9\text{GHz}$

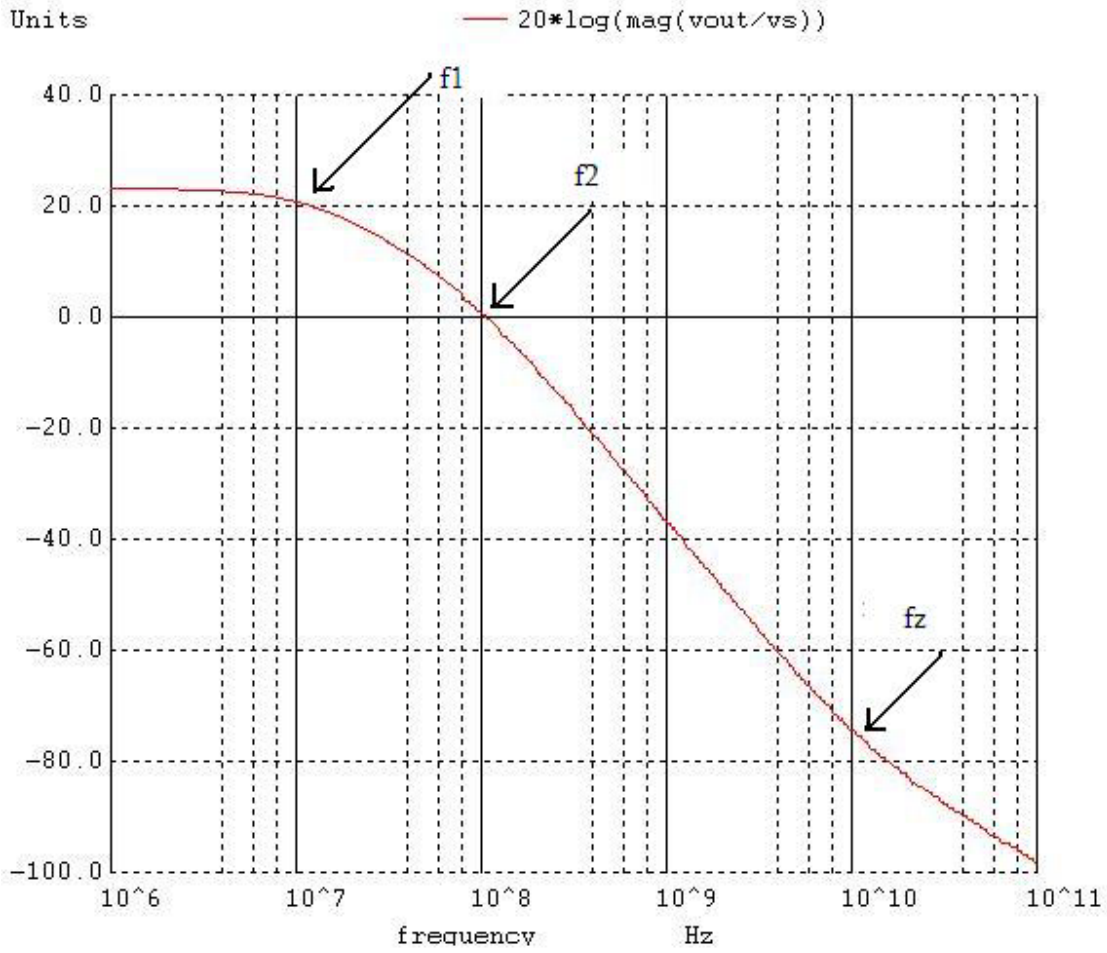
$f_1 = 10.1\text{MHz}$

$f_2 = 97\text{MHz}$

The phase of the gain of the circuit is given by,

$$\angle A_v = 180^\circ - \tan^{-1}\left(\frac{f}{11.9G}\right) - \tan^{-1}\left(\frac{f}{10.1M}\right) - \tan^{-1}\left(\frac{f}{97M}\right)$$

The following figures from SPICE simulations show the frequency response of the circuit.

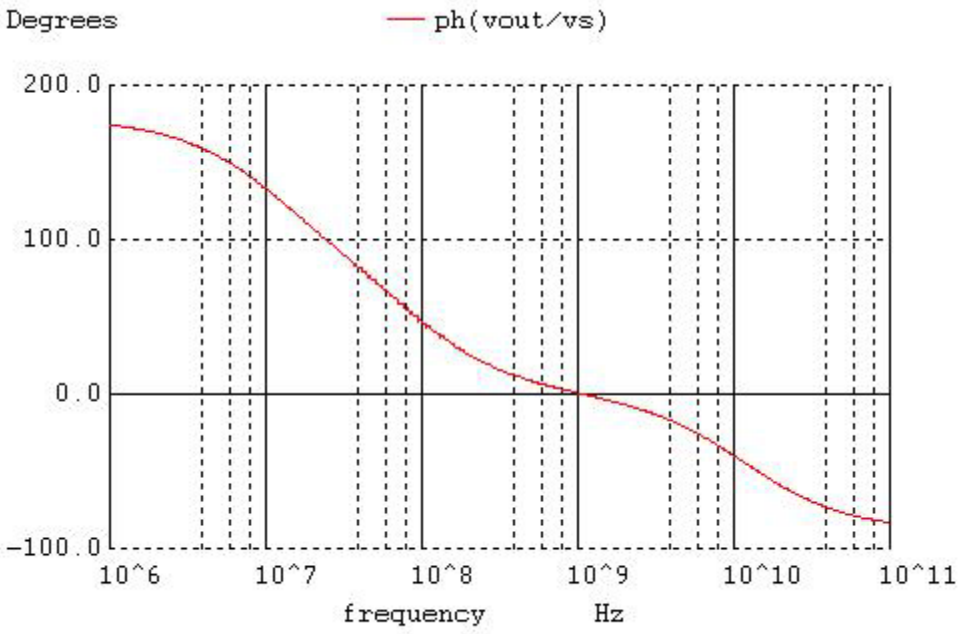


From the figure we find

$f_z = 10\text{GHz}$

$f_1 = 10\text{MHz}$

$f_2 = 100\text{MHz}$


Degrees
ph(vout/vs)
200.0
100.0
0.0
-100.0
10^6
10^7
10^8
10^9
10^10
10^11
frequency
Hz

Problem 21.4
For the circuit in Fig 21.12:

$$i_d = g_m v_{gs}$$

$$v_{in} = v_{gs} + i_d R$$

$$i_d\left(\frac{1}{g_m} + R\right) = v_{in}$$

$$\frac{i_d}{v_{in}} = \frac{1}{\frac{1}{g_m} + R}$$

$$G_{m,eff} = \frac{1}{\frac{1}{g_m} + R}$$

$$G_{m,eff} = \frac{1}{\frac{1}{150\mu} + 50k} = 17.6\mu A/V$$

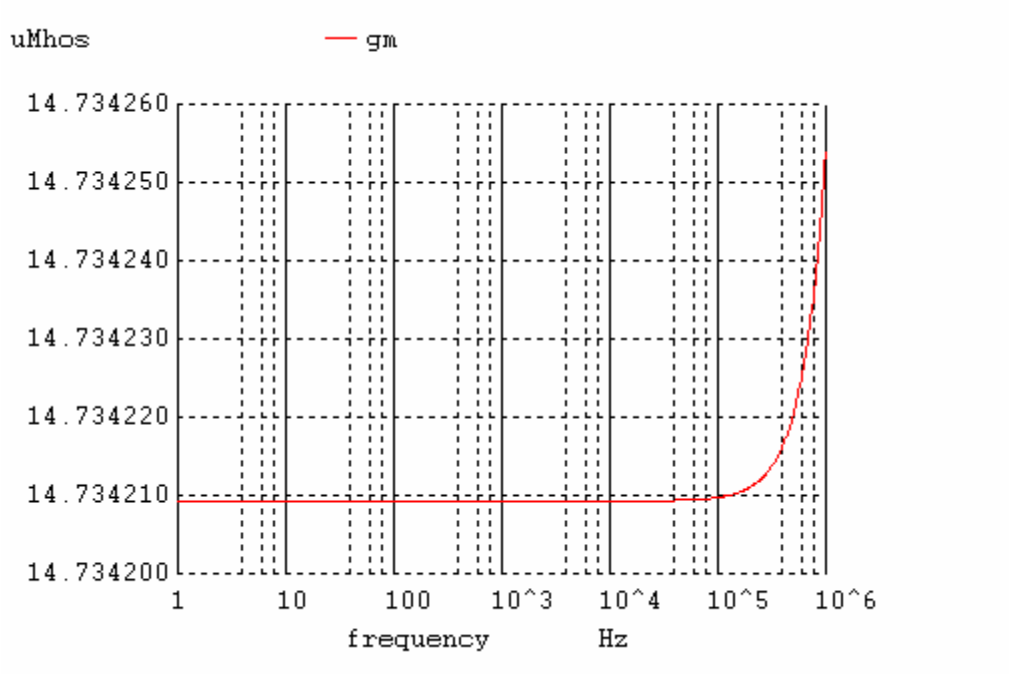
For sizes in Table 9.1 with bias currents of 20uA the effective transconductance from hand calculations is 17.6uA/V.
From SIMS (Refer to Figure 21.13 used for the SIMS where $V_{gs} = 2.05V, V_{ds} = 5V, v_{in} = 1V, R = 50K$) the effective transconductance with body effect is 14.73uA/V and without body effect is 17.47uA/V.

Netlist

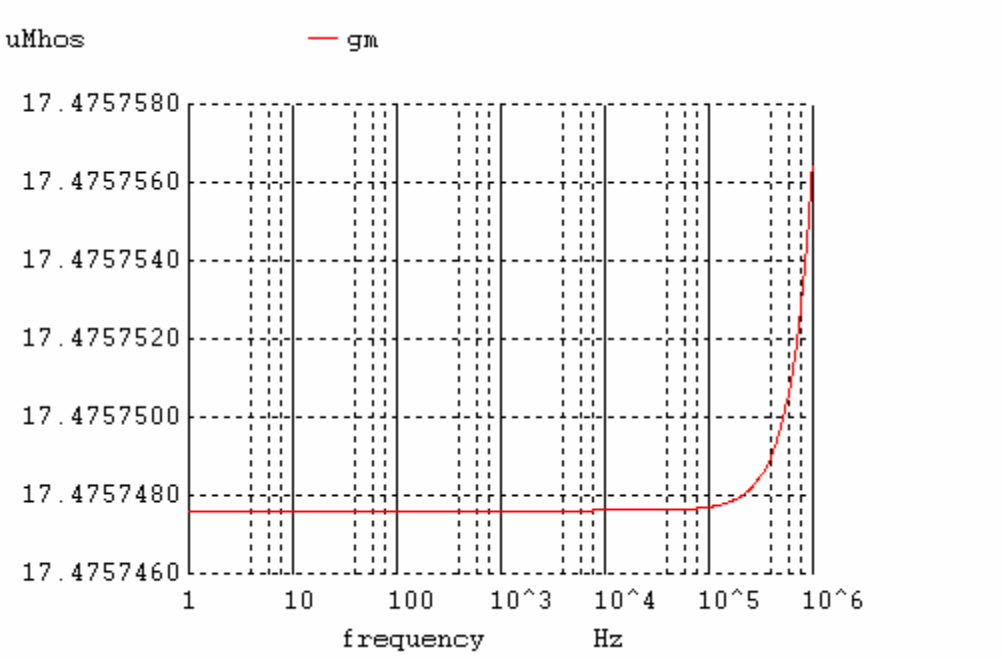
*** Figure 21.29 CMOS: Circuit Design, Layout, and Simulation ***

```
.control
destroy all
run
let id=mag(vdd#branch)
let gm=id/mag(vin)
plot gm
.endc

.ac dec 100 1 1MEG
.option scale=1u

VDD   VDD   0     DC    5
Vin   Vin   0     DC    2.05   AC    1

M1    VDD   Vin   VR    VR     NMOS  L=2 W=10
R1    VR    0     50K
```

```
.MODEL NMOS NMOS LEVEL  = 3
+ TOX    = 200E-10        NSUB   = 1E17          GAMMA  = 0.5
+ PHI    = 0.7            VTO    = 0.8           DELTA  = 3.0
+ UO     = 650            ETA    = 3.0E-6        THETA  = 0.1
+ KP     = 120E-6         VMAX   = 1E5           KAPPA  = 0.3
+ RSH    = 0              NFS    = 1E12          TPG    = 1
+ XJ     = 500E-9         LD     = 100E-9
+ CGDO   = 200E-12        CGSO   = 200E-12        CGBO   = 1E-10
+ CJ     = 400E-6         PB     = 1             MJ     = 0.5
+ CJSW   = 300E-12        MJSW   = 0.5
*
.end
```



With Body Effect



Without Body Effect

Problem Solution for 21.5:

Rin = 1/gm1 and Rout = (1/gm2)||(rout1) ≈ (1/gm2)

Av = Rout/Rin=gm1/gm2

From table 9.1 gm1=gm2=gm=150 uA/V

So Av=1

Figure 1 and Figure 2 show WinSpice simulation results for Common gate amplifier with parameters from table 9.1 and biasing circuit in figure 20.43. For low frequencies gain is approximately 1.

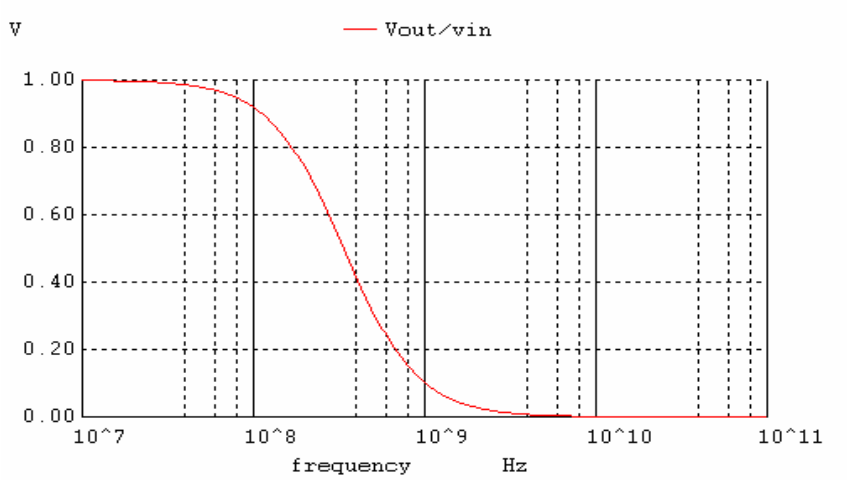


Figure 1. Simulation results of Gain versus Frequency

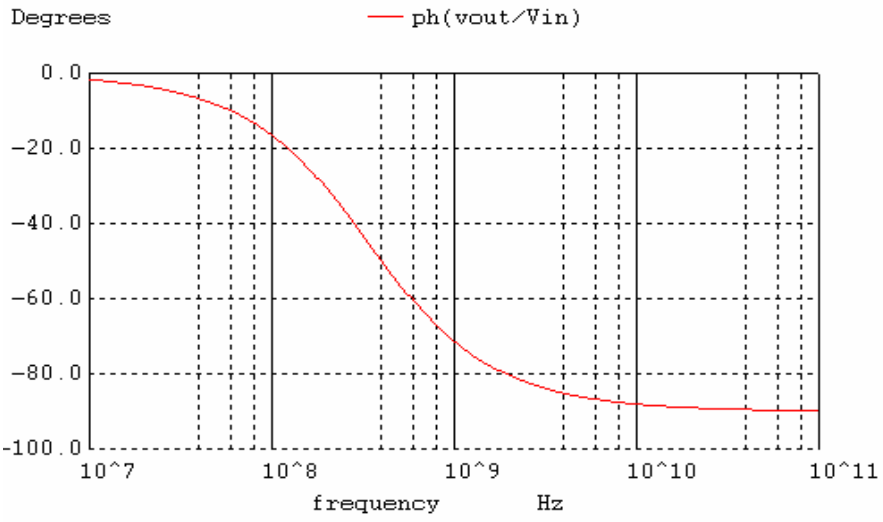


Figure 2. Simulation results for Phase versus Frequency

Now, f3db = gm2/(2π Cgs2) = (150 x 10^{-6})/(2π 70 x 10^{-15}) ≈ 341 MHz
We can see that this is pretty close to the simulation results in figure 3.

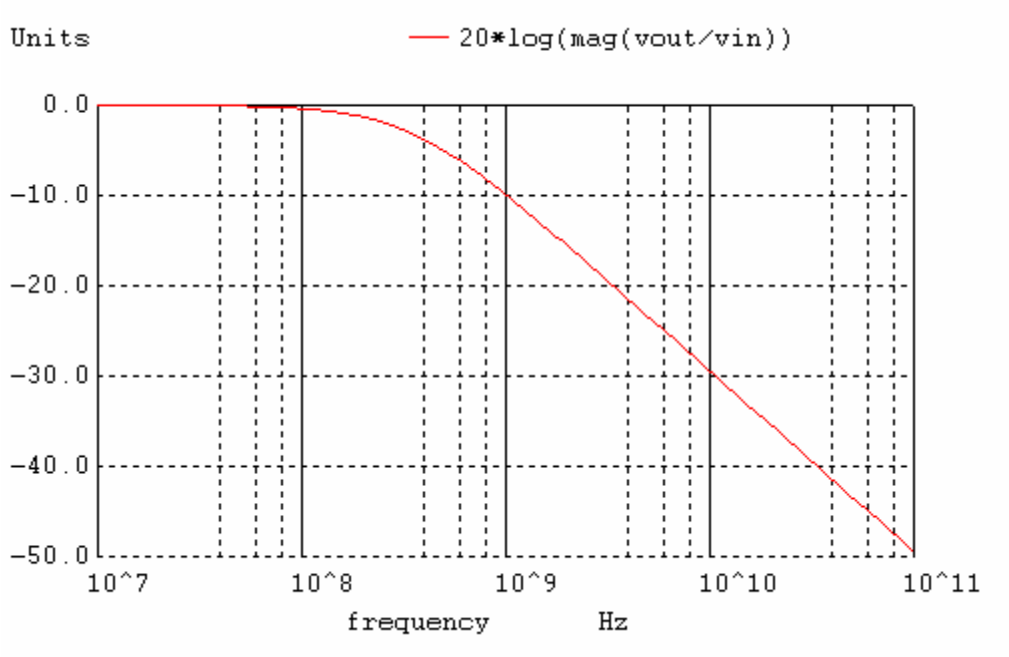


Figure 3. Bode plot for Common Gate Amplifier

*** Problem 21.5 WinSpice code***

```
.control
destroy all
run
plot 20*log(mag(vout/vin))
plot Vout/vin
set units=degrees
plot ph(vout/Vin)
.endc

.option scale=1u
*.dc Von 0 5 1m
.AC DEC 100 10MEG 100g
**.op

VDD   VDD   0     DC    5
Vin   Vin   0     DC    0     AC    1

M1    Vout  Vg1   Vin   Vin   NMOS L=2 W=10
M2    Vout  Vout  VDD   VDD   PMOS L=2 W=30
```

```
Rbig    Vbias4 Vg1     1G
Cbig    Vg1    0       1

Xbias   VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MN1    Vbias2 Vbiasn 0      0      NMOS L=2 W=10
MN2    Vbias1 Vbiasn 0      0      NMOS L=2 W=10
MN3    Vncas  Vncas  vn1    0      NMOS L=2 W=10
MN4    vn1    Vbias3 vn2    0      NMOS L=2 W=10
MN5    vn2    vn1    0      0      NMOS L=2 W=10
MN6    Vbias3 Vbias3 0      0      NMOS L=10 W=10
MN7    Vbias4 Vbias3 Vlow   0      NMOS L=2 W=10
MN8    Vlow   Vbias4 0      0      NMOS L=2 W=10
MN9    Vpcas  Vbias3 vn3    0      NMOS L=2 W=10
MN10   vn3    Vbias4 0      0      NMOS L=2 W=10

MP1    Vbias2 Vbias2 VDD    VDD    PMOS L=10 W=30
MP2    Vhigh  Vbias1 VDD    VDD    PMOS L=2 W=30
MP3    Vbias1 Vbias2 Vhigh  VDD    PMOS L=2 W=30
MP4    vp1    Vbias1 VDD    VDD    PMOS L=2 W=30
MP5    Vncas  Vbias2 vp1    VDD    PMOS L=2 W=30
MP6    vp2    Vbias1 VDD    VDD    PMOS L=2 W=30
MP7    Vbias3 Vbias2 vp2    VDD    PMOS L=2 W=30
MP8    vp3    Vbias1 VDD    VDD    PMOS L=2 W=30
MP9    Vbias4 Vbias2 vp3    VDD    PMOS L=2 W=30
MP10   vp4    vp5    VDD    VDD    PMOS L=2 W=30
MP11   vp5    Vbias2 vp4    VDD    PMOS L=2 W=30
MP12   Vpcas  Vpcas  vp5    VDD    PMOS L=2 W=30

MBM1 Vbiasn Vbiasn 0      0      NMOS L=2 W=10
MBM2 Vbiasp Vbiasn Vr     0      NMOS L=2 W=40
MBM3 Vbiasn         Vbiasp VDD   VDD   PMOS L=2 W=30
MBM4 Vbiasp Vbiasp VDD    VDD    PMOS L=2 W=30

Rbias   Vr     0      6.5k

MSU1  Vsur   Vbiasn 0      0      NMOS L=2   W=10
MSU2  Vsur   Vsur   VDD    VDD    PMOS L=100 W=10
MSU3  Vbiasp Vsur   Vbiasn 0      NMOS L=1   W=10

.ends
```

Problem 21.6:
Using eq.21.64 that is

$$f1 = 1/[2\pi[(Cc + C2).R_2 + (C_1 + C_c(1 + g_m R_2)).R_1]]$$

where $C_C=C_{gd1}$=2fF; $C_2=C_{gd2}+C_{load}$=6fF+100fF=106fF; $C_1=C_{gs1}$=23.3fF; g_{m2}=150uA/V;$R_2=r_{o1}$ll r_{o2}=2.22Mohm; $R_1=R_s$=100Kohms;$g_{m1}=1/R_s=10^{-5}$A/V

Substituting the values we have f1=0.447MHz.

Using eq.21.61 that is

$$f2 = \frac{g_{m2}Cc + (C_{gd1} + C_2)/Rs}{2\pi(CcC_1 + C_1C_2 + C_cC_2)}$$

substituting values in the above equation we get f2=80.9 MHz .
but when use equation 21.66 that is

$$f2 = \frac{g_{m2}Cc}{2\pi(CcC_1 + C_1C_2 + C_cC_2)}$$ we get f2=17.5MHz. In this equation we assumed that R_S is big and neglected the term $(C_{gd1} + C_2)/Rs$. But here in this problem R_S is not that big to neglect the term.

using eq.21.63 that is

$$fz = \frac{g_{m2}}{2\pi.C_c}$$

substituting the values in the equation we have fz=11.9GHz.

$A_{DC}= g_{m1}R_1g_{m2}R_2$ where $g_{m1}=1/R_s$=10uA/V.

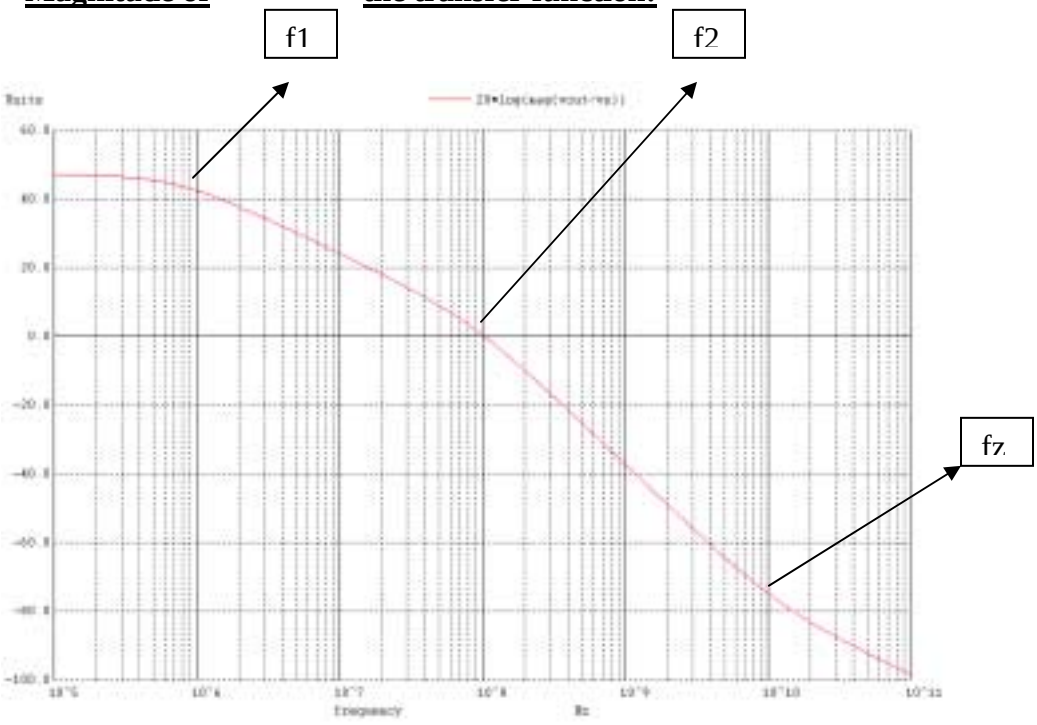
Therefore A_{DC}=333v/v-→50dB.

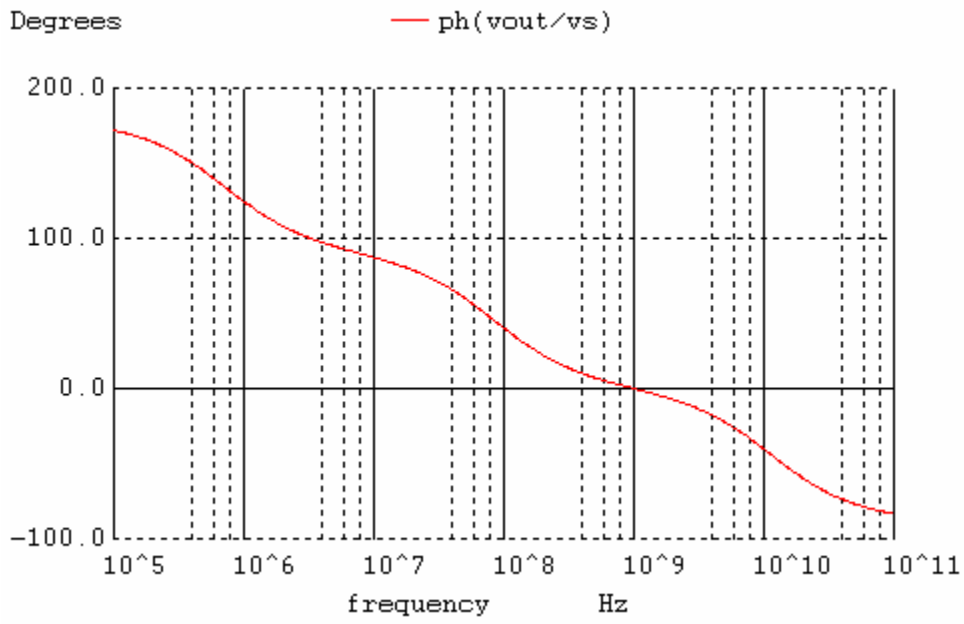
The transfer is then written as

From eq 21.67 $$\frac{V_{out}(f)}{V_{in}(f)} = g_{m1}R_1g_{m2}R_2\frac{(1 - j.\frac{f}{f_z})}{(1 - j.\frac{f}{f_1})(1 - j.\frac{f}{f_2})}$$

Therefore $$\frac{V_{out}(f)}{V_{in}(f)} = 333.\frac{(1 - j.\frac{f}{11.9GHz})}{(1 - j.\frac{f}{0.44MHz_1})(1 - j.\frac{f}{80.9MHz})}$$

Magnitude of the transfer function:





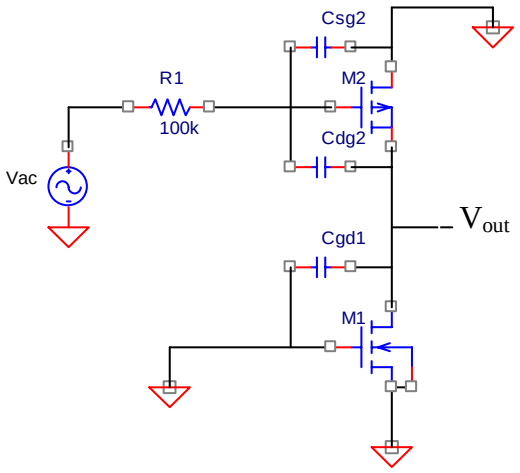
Simulated values:	Hand calculated values
f1=0.36 MHz	0.44MHz
f2=100 MHz(approx.)	80.9MHz
fz=15GHz	11.9GHz

Netlist:

```
.control
destroy all
run
plot 20*log(mag(vout/vs))
set units=degrees
plot ph(vout/vs)
.endc

.option scale=1u
.AC dec 100 100k 100G

VDD   VDD   0       DC     5
Vs    Vs    0       DC     0       AC     1

M1    Vout  Vin     0      0       NMOS L=2 W=10
M2    Vout  Vbias1  VDD    VDD     PMOS L=2 W=30
Rbig  Vout  Vin     10G
Cbig  V1    Vin     1
Rs    Vs    V1      100k
Cl    Vout  0       100f

Xbias  VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MN1   Vbias2 Vbiasn 0      0       NMOS L=2 W=10
MN2   Vbias1 Vbiasn 0      0       NMOS L=2 W=10
MN3   Vncas  Vncas  vn1    0       NMOS L=2 W=10
MN4   vn1    Vbias3 vn2    0       NMOS L=2 W=10
MN5   vn2    vn1    0      0       NMOS L=2 W=10
MN6   Vbias3 Vbias3 0      0       NMOS L=10 W=10
MN7   Vbias4 Vbias3 Vlow   0       NMOS L=2 W=10
MN8   Vlow   Vbias4 0      0       NMOS L=2 W=10
MN9   Vpcas  Vbias3 vn3    0       NMOS L=2 W=10
MN10  vn3    Vbias4 0      0       NMOS L=2 W=10

MP1   Vbias2 Vbias2 VDD    VDD     PMOS L=10 W=30
MP2   Vhigh  Vbias1 VDD    VDD     PMOS L=2 W=30
MP3   Vbias1 Vbias2 Vhigh  VDD     PMOS L=2 W=30
MP4   vp1    Vbias1 VDD    VDD     PMOS L=2 W=30
MP5   Vncas  Vbias2 vp1    VDD     PMOS L=2 W=30
MP6   vp2    Vbias1 VDD    VDD     PMOS L=2 W=30
MP7   Vbias3 Vbias2 vp2    VDD     PMOS L=2 W=30
MP8   vp3    Vbias1 VDD    VDD     PMOS L=2 W=30
MP9   Vbias4 Vbias2 vp3    VDD     PMOS L=2 W=30
```

```
MP10  vp4     vp5     VDD   VDD   PMOS L=2 W=30
MP11  vp5     Vbias2 vp4     VDD   PMOS L=2 W=30
MP12  Vpcas  Vpcas  vp5     VDD   PMOS L=2 W=30

MBM1 Vbiasn Vbiasn 0        0       NMOS L=2 W=10
MBM2 Vbiasp Vbiasn Vr       0       NMOS L=2 W=40
MBM3 Vbiasn          Vbiasp VDD   VDD   PMOS L=2 W=30
MBM4 Vbiasp Vbiasp VDD   VDD   PMOS L=2 W=30

Rbias   Vr       0        6.5k

MSU1  Vsur    Vbiasn 0        0       NMOS L=2   W=10
MSU2  Vsur    Vsur    VDD   VDD   PMOS L=100 W=10
MSU3  Vbiasp Vsur    Vbiasn 0        NMOS L=1   W=10

.ends

.MODEL NMOS NMOS LEVEL  = 3
+ TOX    = 200E-10       NSUB   = 1E17          GAMMA  = 0.5
+ PHI    = 0.7           VTO    = 0.8           DELTA  = 3.0
+ UO     = 650           ETA    = 3.0E-6        THETA  = 0.1
+ KP     = 120E-6        VMAX   = 1E5           KAPPA  = 0.3
+ RSH    = 0             NFS    = 1E12          TPG    = 1
+ XJ     = 500E-9        LD     = 100E-9
+ CGDO   = 200E-12       CGSO   = 200E-12       CGBO   = 1E-10
+ CJ     = 400E-6        PB     = 1             MJ     = 0.5
+ CJSW   = 300E-12       MJSW   = 0.5
*
.MODEL PMOS PMOS LEVEL  = 3
+ TOX    = 200E-10       NSUB   = 1E17          GAMMA  = 0.6
+ PHI    = 0.7           VTO    = -0.9          DELTA  = 0.1
+ UO     = 250           ETA    = 0             THETA  = 0.1
+ KP     = 40E-6         VMAX   = 5E4           KAPPA  = 1
+ RSH    = 0             NFS    = 1E12          TPG    = -1
+ XJ     = 500E-9        LD     = 100E-9
+ CGDO   = 200E-12       CGSO   = 200E-12       CGBO   = 1E-10
+ CJ     = 400E-6        PB     = 1             MJ     = 0.5
+ CJSW   = 300E-12       MJSW   = 0.5

.end
```

Problem 21.7



ac equivalent circuit

The model parameters for the above circuit (with the help of table 9.1) are

$R_1 = R_S = 100k$
$C_1 = C_{sg2} = 70$ fF
$C_C = C_{dg2} = 6$ fF
$C_2 = C_{gd1} = 2$ fF
$R_2 = r_{01}$ (parallel with) $r_{02} = 2.22$ MΩ
$g_{m2} = 150\mu A/V$
$g_{m1} = 1/R_S = 10\mu A/V$

Form Eq : 21.70 (page no : 24)

$A_V = g_{m1}R_1g_{m2}R_2$; Substituting the above values we get

A_V = 333 V/V => 50dB

Form Eq : 21.63 (page no : 23)

$f_Z = \frac{g_{M2}}{2\pi C_C}$; Substituting the above values we get

f_Z = 3.97 GHz

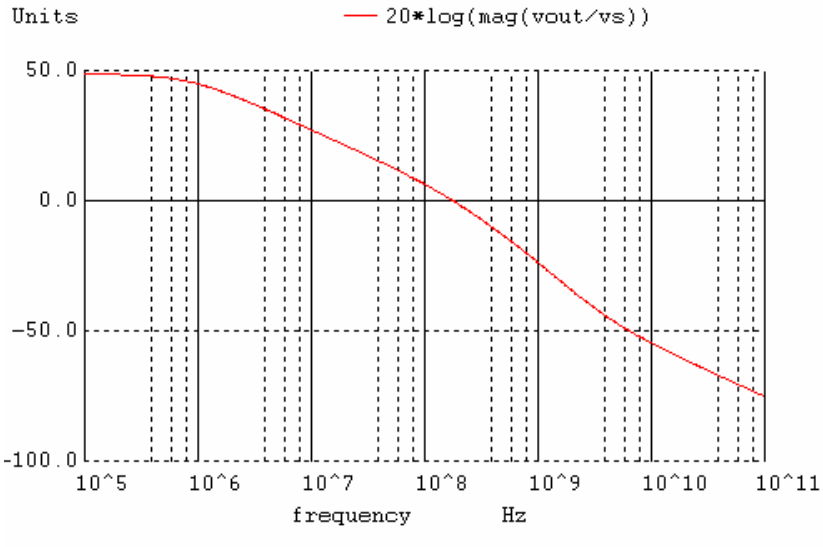
Form Eq : 21.65 (page no : 23)

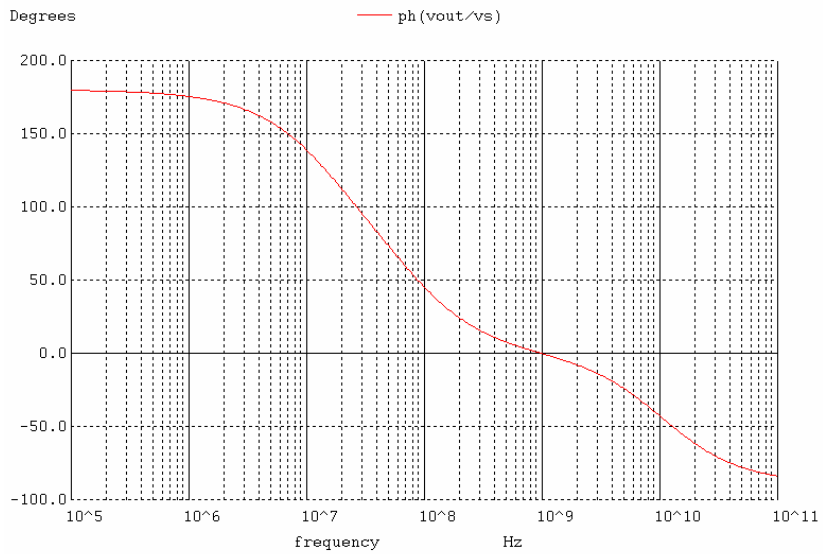
$$f_1 = \frac{1}{2\pi g_{m2} R_2 R_1 C_C} = \mathbf{0.79\ MHz}$$

Form Eq : 21.66

$$f_2 = \frac{1}{2\pi[C_C C_1 + C_1 C_2 + C_C C_2]} = \mathbf{0.25\ GHz}$$

SIMULATION RESULTS





From the above simulations we have

Simulation results	Hand Calculations
f_Z = 3.97 GHz	f_Z = 4 GHz
f_1 = 1 MHz	f_1 = 0.79 MHz
f_2 = 0.2 GHz	f_2 = 0.25 GHz

NETLIST

```
.control
destroy all
run
plot 20*log(mag(vout/vs))
set units=degrees
plot ph(vout/vs)
.endc

.option scale=1u
.AC dec 100 100k 100G

VDD   VDD   0       DC    5
Vs    Vs    0       DC    0      AC    1

M1    Vout  Vbias4  0     0      NMOS L=2 W=10
M2    Vout  Vin     VDD   VDD    PMOS L=2 W=30
Rbig  Vout  Vin     10G
Cbig  Vss   Vin     1
Rs    Vs    Vss     100k

Xbias  VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MN1   Vbias2 Vbiasn 0     0      NMOS L=2 W=10
MN2   Vbias1 Vbiasn 0     0      NMOS L=2 W=10
MN3   Vncas  Vncas  vn1   0      NMOS L=2 W=10
MN4   vn1    Vbias3 vn2   0      NMOS L=2 W=10
MN5   vn2    vn1    0     0      NMOS L=2 W=10
MN6   Vbias3 Vbias3 0     0      NMOS L=10 W=10
MN7   Vbias4 Vbias3 Vlow  0      NMOS L=2 W=10
MN8   Vlow   Vbias4 0     0      NMOS L=2 W=10
MN9   Vpcas  Vbias3 vn3   0      NMOS L=2 W=10
MN10  vn3    Vbias4 0     0      NMOS L=2 W=10
```

```
MP1    Vbias2 Vbias2 VDD   VDD   PMOS L=10 W=30
MP2    Vhigh  Vbias1 VDD   VDD   PMOS L=2 W=30
MP3    Vbias1 Vbias2 Vhigh  VDD   PMOS L=2 W=30
MP4    vp1    Vbias1 VDD   VDD   PMOS L=2 W=30
MP5    Vncas  Vbias2 vp1    VDD   PMOS L=2 W=30
MP6    vp2    Vbias1 VDD   VDD   PMOS L=2 W=30
MP7    Vbias3 Vbias2 vp2    VDD   PMOS L=2 W=30
MP8    vp3    Vbias1 VDD   VDD   PMOS L=2 W=30
MP9    Vbias4 Vbias2 vp3    VDD   PMOS L=2 W=30
MP10   vp4    vp5    VDD   VDD   PMOS L=2 W=30
MP11   vp5    Vbias2 vp4    VDD   PMOS L=2 W=30
MP12   Vpcas  Vpcas  vp5    VDD   PMOS L=2 W=30

MBM1 Vbiasn Vbiasn 0      0      NMOS L=2 W=10
MBM2 Vbiasp Vbiasn Vr     0      NMOS L=2 W=40
MBM3 Vbiasn         Vbiasp VDD   VDD   PMOS L=2 W=30
MBM4 Vbiasp Vbiasp VDD   VDD   PMOS L=2 W=30

Rbias  Vr     0      6.5k

MSU1 Vsur   Vbiasn 0      0      NMOS L=2   W=10
MSU2 Vsur   Vsur   VDD   VDD   PMOS L=100 W=10
MSU3 Vbiasp Vsur   Vbiasn 0      NMOS L=1   W=10

.ends
```

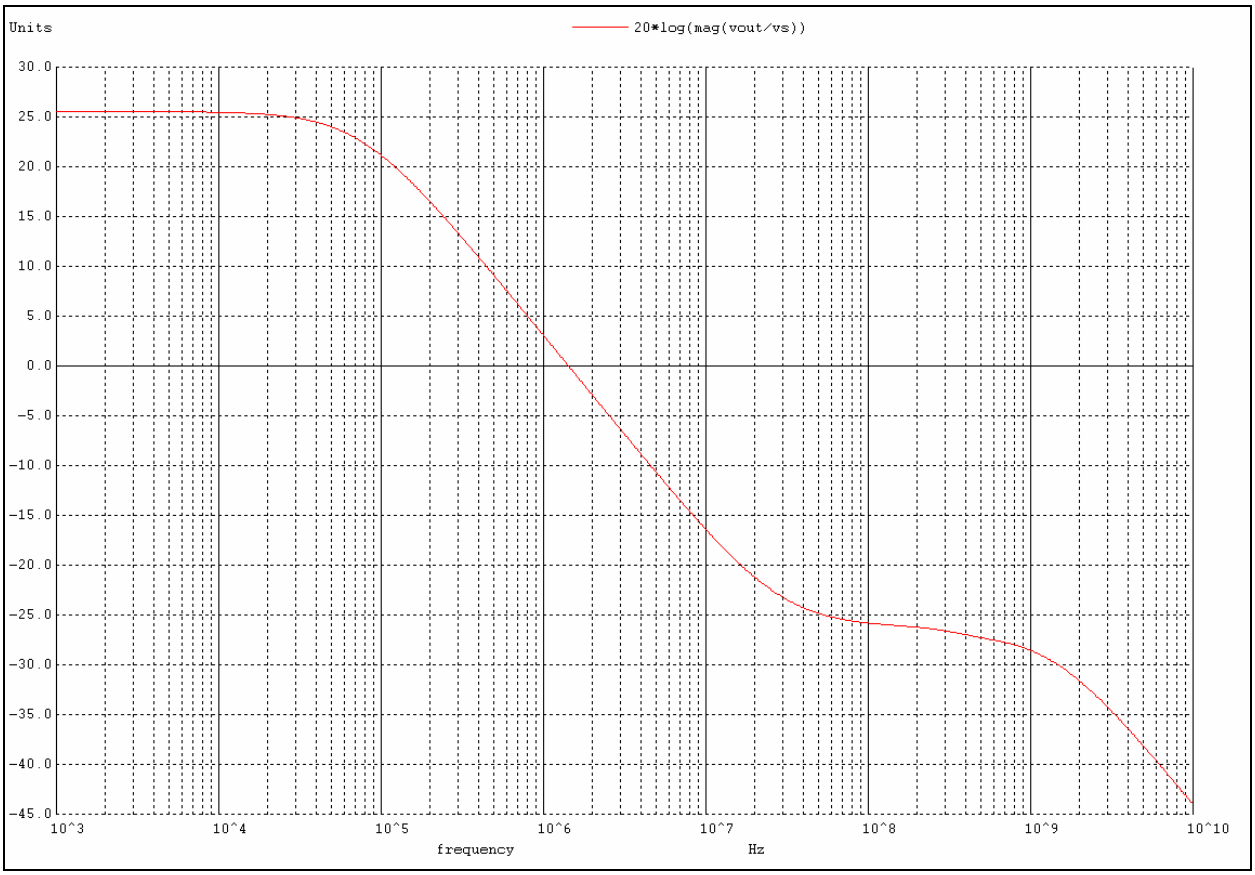
Problem 21.8)

Repeat Example 21.9 (page 21-26) using bias circuit from fig 20.47 & sizes in Table 9.2.

Use the pole splitting equations (page 21-23) to solve this problem.

$$R_1 = R_s = 100k\Omega$$
$$\mathrm{R}_2 = r_{on} \,//\, r_{op} = 111k\Omega$$
$$C_1 = \mathrm{C}_{gs1} = 4.17\mathrm{fF}$$
$$C_2 = \mathrm{C}_{dg2} = 3.7\mathrm{fF}$$
$$\mathrm{C}_c = 1pF + C_{gd1} \cong 1pF$$
$$gm_1 = \frac{1}{R_s} = \frac{1}{100k\Omega}$$
$$\mathrm{gm}_2 = \mathrm{gm}_n = 150\,\frac{\mu A}{V}$$

$$f_1 \cong \frac{1}{2\pi\left[\left(\mathrm{C}_c + \mathrm{C}_2\right)R_2 + \left(C_1 + C_c\left(1 + gm_2 R_2\right)\right)R_1\right]} = 84.8kHz$$
$$f_2 \cong \frac{\mathrm{gm}_2 \cdot \mathrm{C}_c}{2\pi\left(\mathrm{C}_c \cdot \mathrm{C}_1 + \mathrm{C}_1 \cdot \mathrm{C}_2 + \mathrm{C}_c \cdot \mathrm{C}_2\right)} = 3.0GHz$$
$$f_z \cong \frac{\mathrm{gm}_2}{2\pi \cdot \mathrm{C}_c} = 23.9MHz$$
$$f_{un} \cong \frac{1}{2\pi \cdot R_s \cdot C_c} = 1.59MHz$$
$$\frac{vout(f)}{vin(f)} \cong gm_1 \cdot gm_2 \cdot R_1 \cdot R_2 = 16.65\,\frac{V}{V} = 24.4dB$$



Plot of Magnitude response in Problem 21.8

Spice shows the following:

$f_1 \cong 80\text{kHz}$

$f_2 \cong 1.5\text{GHz}$

$f_z \cong 30\text{MHz}$

$f_{un} \cong 1.4\text{MHz}$

$\text{gain} \cong 25.5\text{dB}$

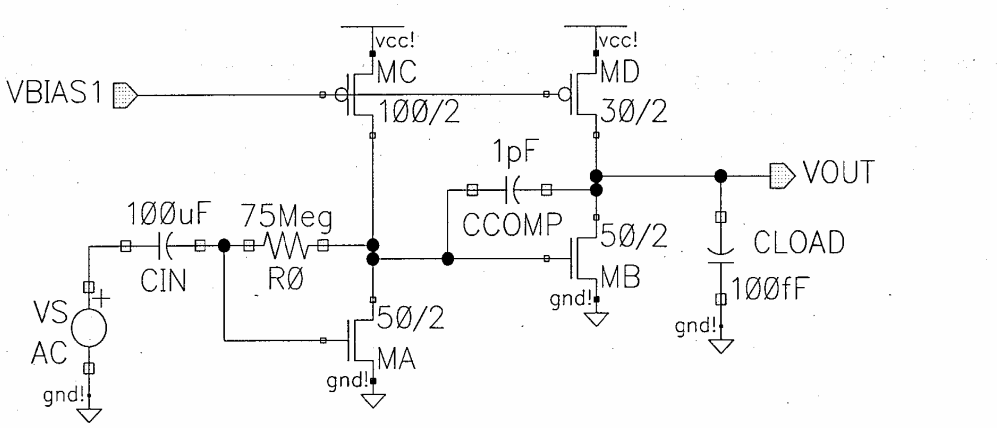
The simulation results are seen above. The value of the gain is 25.5dB (we calculated 24.4dB). The values of the poles, zero, and unity gain in the simulations are relatively close to the calculated values. The small discrepancies are most likely the result of differences in the actual circuit parameters compares to the values we used in the formulas.

```
*** Problem 21.8 CMOS: Circuit Design, Layout, and Simulation ***

.control
destroy all
run
plot 20*log(mag(vout/vs))
set units=degrees
plot ph(vout/vs)
.endc

.option scale=50n
.AC dec 100 1k 10G

VDD     VDD     0       DC      1
Vs      Vs      0       DC      0       AC      1

M1      Vout    Vin     0       0       NMOS L=2 W=50
M2      Vout    Vbias1  VDD     VDD     PMOS L=2 W=100
Rbig    Vout    Vin     10G
Cbig    Vss     Vin     1
Rs      Vs      Vss     100k
Cc      Vout    Vin     1p
Xbias   VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1     Vbias3  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP2     Vbias4  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP3     vp1     vp2     VDD     VDD     PMOS L=2 W=100
MP4     vp2     Vbias2  vp1     VDD     PMOS L=2 W=100
MP5     Vpcas   Vpcas   vp2     VDD     PMOS L=2 W=100
MP6     Vbias2  Vbias2  VDD     VDD     PMOS L=10 W=20
MP7     Vhigh   Vbias1  VDD     VDD     PMOS L=2 W=100
MP8     Vbias1  Vbias2  Vhigh   VDD     PMOS L=2 W=100
MP9     vp3     Vbias1  VDD     VDD     PMOS L=2 W=100
MP10    Vncas   Vbias2  vp3     VDD     PMOS L=2 W=100

MN1     Vbias3  Vbias3  0       0       NMOS L=10 W=10
MN2     Vbias4  Vbias3  Vlow    0       NMOS L=2 W=50
MN3     Vlow    Vbias4  0       0       NMOS L=2 W=50
MN4     Vpcas   Vbias3  vn1     0       NMOS L=2 W=50
MN5     vn1     Vbias4  0       0       NMOS L=2 W=50
MN6     Vbias2  Vbias3  vn2     0       NMOS L=2 W=50
MN7     vn2     Vbias4  0       0       NMOS L=2 W=50
MN8     Vbias1  Vbias3  vn3     0       NMOS L=2 W=50
MN9     vn3     Vbias4  0       0       NMOS L=2 W=50
MN10    Vncas   Vncas   vn4     0       NMOS L=2 W=50
MN11    vn4     Vbias3  vn5     0       NMOS L=2 W=50
MN12    vn5     vn4     0       0       NMOS L=2 W=50

MBM1    Vbiasn  Vbiasn  0       0       NMOS L=2 W=50
MBM2    Vreg    Vreg    Vr      0       NMOS L=2 W=200
MBM3    Vbiasn  Vbiasp  VDD     VDD     PMOS L=2 W=100
MBM4    Vreg    Vbiasp  VDD     VDD     PMOS L=2 W=100

Rbias   Vr      0       5.5k

*amplifier
MA1     Vamp    Vreg    0       0       NMOS L=2 W=50
MA2     Vbiasp  Vbiasn  0       0       NMOS L=2 W=50
MA3     Vamp    Vamp    VDD     VDD     PMOS L=2 W=100
MA4     Vbiasp  Vamp    VDD     VDD     PMOS L=2 W=100

MCP     VDD     Vbiasp  VDD     VDD     PMOS L=100 W=100

*start-up stuff
MSU1    Vsur    Vbiasn  0       0       NMOS L=2   W=50
MSU2    Vsur    Vsur    VDD     VDD     PMOS L=20  W=10
MSU3    Vbiasp  Vsur    Vbiasn  0       NMOS L=1   W=10

.ends
```

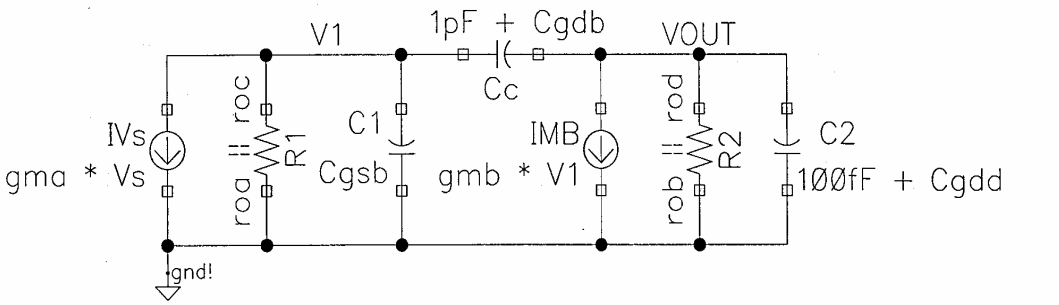
Netlist Problem 21.8 (excluding the NMOS and PMOS models)

HOMEWORK PROBLEM – 21.9.

Find the frequency response of the circuit in 21.10 using Table 9.2 and the bias circuit from Figure 20.47. The schematic was converted into the Figure 21.25 format for the AC equivalent model and is shown below. This model should be used whenever pole splitting is present. Equation 21.63 on page 21-23 was used to calculate the zero and equations 21.64 and 21.66 were used to calculate the two poles. The calculations are shown below:



Problem 21.9 Amplifier



AC Equivalent Model in Figure 21.25 Format

From Table 9.2:
Cgsa = Cgsb = 4.17f, Cgda = Cgdb = 1.56f, Cgdc = Cgdd = 3.7f, Cc = 1pF
gma = gmb = gmc = gmd = 150uA/V, r0a || rob = r0c || r0d = 111.2K

Av = gma * roa || rob * gmb * roc || rod = (150u * 111.2K) ** 2 = 278.3 = 48.8 dB

fz = gmb / 2 * pi * Cc = 2 * pi * 1pF = 23.9MHz

f1 = 1 / [2 * pi * [(Cc + C2) * R2 + (C1 + Cc * (1 + gm2 * R2)) * R1]
f1 = 1 / [2 * pi * [(3.7f + 100f) * 111.2K + (4.17f + 1P * (1 + 150u * 111.2K)
f1 = 5.2 KHz

f2 = gm1 / [2 * pi * (Cc * C1 + C1 * C2 + Cc * C2)]
f2 = 150u / [2 * pi * (1p * 4.17f + 4.17f * 103.7f + 1p * 4.17f)]

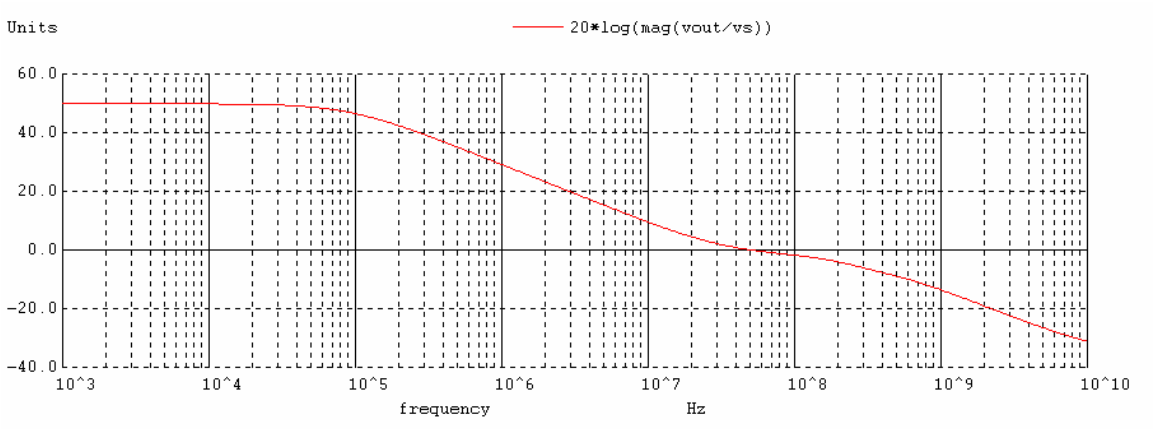
f2 = 220 MHz

The following netlist was used to simulate the frequency response of the amplifier in Problem 21.9. This netlist was also used to simulate the transient response of the circuitry by optioning in the “Transient Sections” and optioning out the “AC Sections”.

```
*** Homework 21.9     CMOS: Circuit Design, Layout, and Simulation ***
.control
destroy all
run

*** AC Section ***
plot 20*log(mag(vout/vs))
set units=degrees
plot ph(vout/vs)

*** Transient Section *****
*plot Vout
*plot Vss

.endc

.option scale=50n
.option gmin=1e-15

*** AC Section ***
.AC dec 100 1k 10G

*** Transient Section *****
*.tran .02n 300n 100n .02n

VDD   VDD   0      DC    1
*Vs   Vs    0      DC    0      AC    10m   sin 0 10m 400MEG
Vs    Vs    0      DC    0      AC    10m   sin 0 10m 10MEG

Xbias  VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

MA    V1    Vss    0      0      NMOS L=2 W=50
MB    Vout  V1     0      0      NMOS L=2 W=50

MC    V1    Vbias1 VDD    VDD    PMOS L=2 W=100
MD    Vout  Vbias1 VDD    VDD    PMOS L=2 W=100

CL    Vout  0      100f
Cc    Vout  V1     1p
Cbig1 Vs    Vss    1u
Rbig1 V1    Vss    75Meg

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1   Vbias3 Vbiasp VDD    VDD    PMOS L=2 W=100
```

```
MP2   Vbias4 Vbiasp       VDD   VDD   PMOS L=2 W=100
MP3   vp1    vp2    VDD   VDD   PMOS L=2 W=100
MP4   vp2    Vbias2 vp1   VDD   PMOS L=2 W=100
MP5   Vpcas  Vpcas  vp2   VDD   PMOS L=2 W=100
MP6   Vbias2 Vbias2 VDD   VDD   PMOS L=10 W=20
MP7   Vhigh  Vbias1 VDD   VDD   PMOS L=2 W=100
MP8   Vbias1 Vbias2 Vhigh VDD   PMOS L=2 W=100
MP9   vp3    Vbias1 VDD   VDD   PMOS L=2 W=100
MP10  Vncas  Vbias2 vp3   VDD   PMOS L=2 W=100

MN1   Vbias3 Vbias3 0     0     NMOS L=10 W=10
MN2   Vbias4 Vbias3 Vlow  0     NMOS L=2 W=50
MN3   Vlow   Vbias4 0     0     NMOS L=2 W=50
MN4   Vpcas  Vbias3 vn1   0     NMOS L=2 W=50
MN5   vn1    Vbias4 0     0     NMOS L=2 W=50
MN6   Vbias2 Vbias3 vn2   0     NMOS L=2 W=50
MN7   vn2    Vbias4 0     0     NMOS L=2 W=50
MN8   Vbias1 Vbias3 vn3   0     NMOS L=2 W=50
MN9   vn3    Vbias4 0     0     NMOS L=2 W=50
MN10  Vncas  Vncas  vn4   0     NMOS L=2 W=50
MN11  vn4    Vbias3 vn5   0     NMOS L=2 W=50
MN12  vn5    vn4    0     0     NMOS L=2 W=50

MBM1 Vbiasn Vbiasn 0     0     NMOS L=2 W=50
MBM2 Vreg   Vreg   Vr    0     NMOS L=2 W=200
MBM3 Vbiasn Vbiasp VDD   VDD   PMOS L=2 W=100
MBM4 Vreg   Vbiasp VDD   VDD   PMOS L=2 W=100

Rbias  Vr     0      5.5k

*amplifier
MA1   Vamp  Vreg  0     0     NMOS L=2 W=50
MA2   Vbiasp Vbiasn 0     0     NMOS L=2 W=50
MA3   Vamp  Vamp  VDD   VDD   PMOS L=2 W=100
MA4   Vbiasp Vamp  VDD   VDD   PMOS L=2 W=100
MCP   VDD   Vbiasp VDD   VDD   PMOS L=100 W=100

*start-up stuff
MSU1  Vsur  Vbiasn 0     0     NMOS L=2   W=50
MSU2  Vsur  Vsur   VDD   VDD   PMOS L=20  W=10
MSU3  Vbiasp Vsur  Vbiasn 0     NMOS L=1   W=10

.ends

****  include the BSIM4 models here ****
```

The simulated frequency response is shown below. The first pole occurred at 90 KHz instead of the 5 KHz calculated value. The unity gain point, fun, simulated at twice the calculated frequency, but from the graph it appears that this was caused by the zero pushing out the crossing point. The hand calculated zero frequency was the same as the unity gain frequency. Notice that the phase starts off at 0 degrees indicating that the amplifier is non-inverting. The Gain and Phase response of the amplifier is shown below:

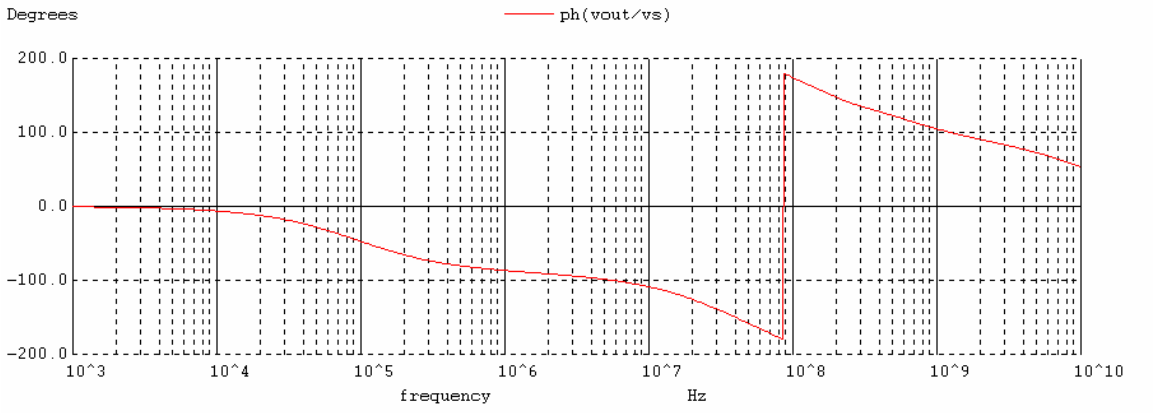


Calculated Values

Av = 48.8 dB, f1 = 5.2 KHz, f2 = 220 MHz, fz = 23.9 MHz, fun = 23.9 MHz

Measured Values

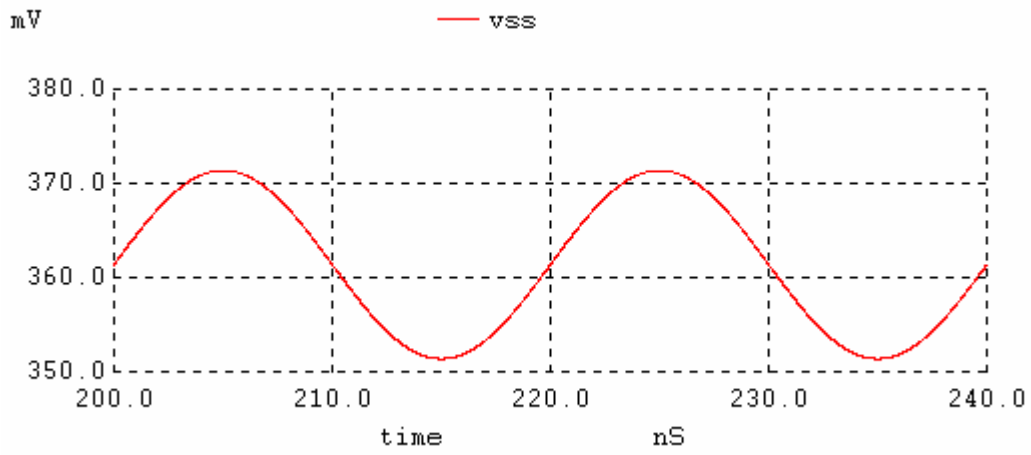
Av = 49.8 dB, f1 = 90 KHz, f2 = 200 MHz, fz = 50 MHz, fun = 50 MHz & -160 deg

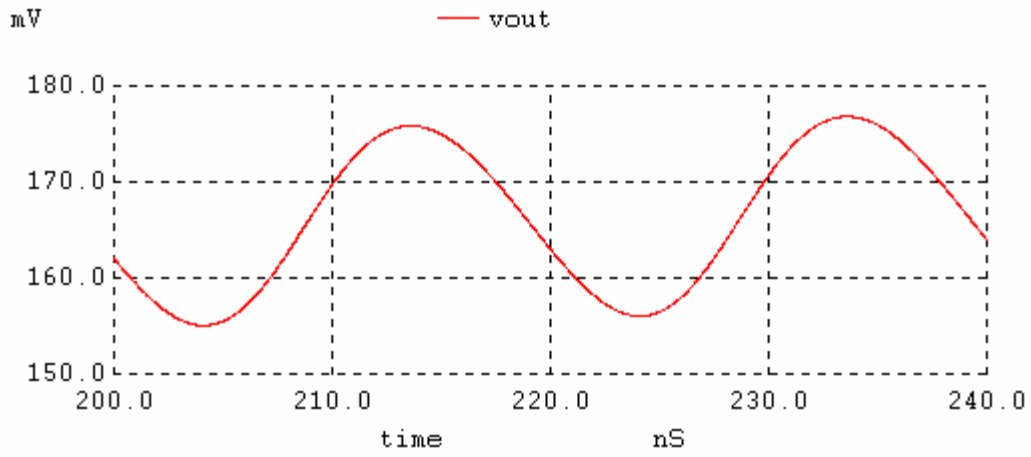


The transient simulation results for 50 MHz are shown below. From the frequency response plot above, at 50 MHz, the gain of the amplifier is one and the phase is -160 degrees. Since the phase = 360 * tD / T where tD is the time difference and T is the period, tD = phase * T / 360.

At 50 MHz, tD = -160 * (1 / 50 MHz) / 360 = -8.9 ns or Vss (amplifier input) is 8.9 ns ahead of Vout.

Simulations verified that the gain of the amplifier at 50 MHz was one since the input and output had the same voltage swing (20 mV). The time point for the maximum voltage of Vout occurs 9 ns after the maximum voltage of Vss which matches our calculated tD value.





21.10)

Repeat Ex.21.12 using the biasing circuit from fig. 20.43 and the sizes in Table 9.1.

From Table 9.1

Cgsn=23.3fF, Cdgn=2fF, gmn=150uA/V=gmp, ron=5Mohms, rop=4Mohms, Csgp=70fF, and Cdgp=6fF.

From equation 21.78 we know that Av1=-1.

$$\tau_{in} = R_s(C_{gs1} + (1+|Av|C_{gd1})) = 100k \cdot (23.3fF + 2 + 2fF) = 273ps$$

$$f_{in} = \frac{1}{2\pi\tau_{in}} = 58.3MHz$$

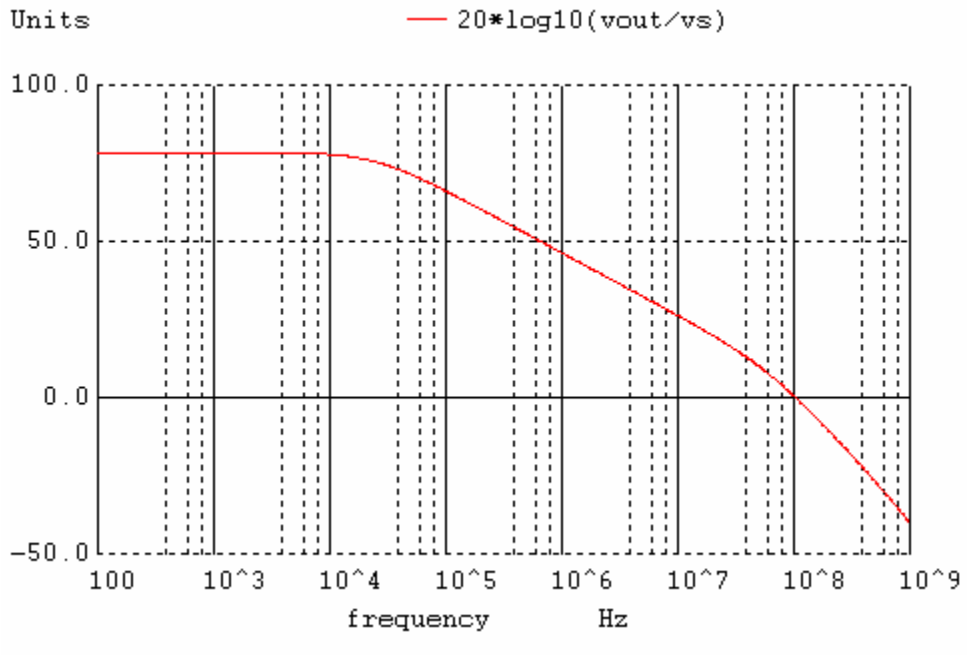
Since the load is large, $C_{load} >> C_{gd2}+C_{gd3}$, we can write

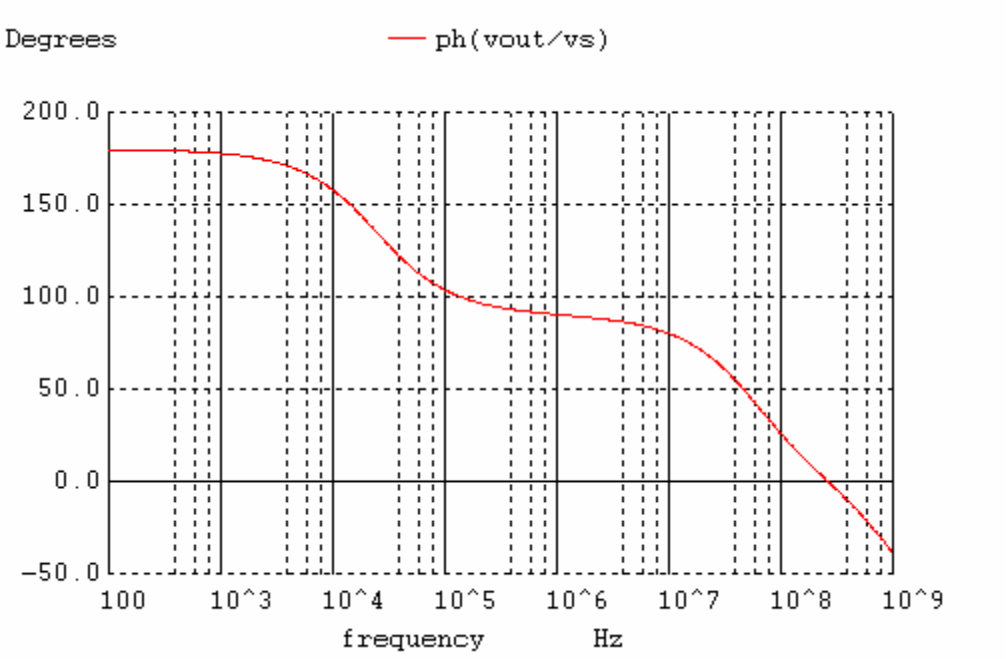
$$\tau_{out} = R_{ocas}(C_{load} + C_{gd2} + C_{gd3}) \approx g_{mn}r_{on}^{\ 2} \parallel g_{mp}r_{onp}^{\ 2} = 146\mu s$$

$$f_{out} = \frac{1}{2\pi\tau_{out}} = 1.00kHs$$

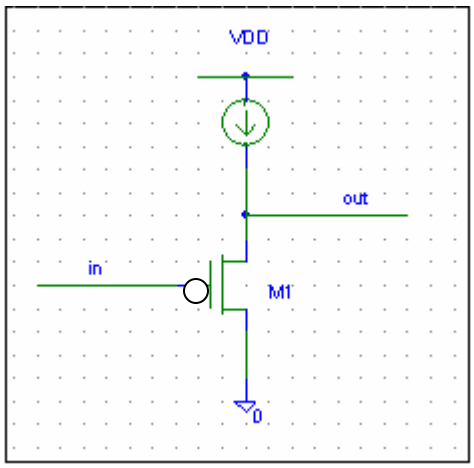
```
.control
destroy all
run
set units=degrees
plot ph(vout/vs)
plot 20*log10(vout/vs)
.endc

.option scale=1u
.AC DEC 100 100 1G
**.op

VDD     VDD     0       DC      5
Vs      Vs      0       DC      0       AC      1

Xbias   VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

M1      Vd1     Vin     0       0       NMOS L=2 W=10
M2      Vout    Vbias3  Vd1     0       NMOS L=2 W=10
M3      Vout    Vbias2  Vd4     VDD     PMOS L=2 W=30
M4      Vd4     Vbias1  VDD     VDD     PMOS L=2 W=30
Cload   Vout    0       100f
Cbig    Vin     Vss     10u
Rbig    Vout    Vin     1G
Rs      Vs      Vss     100k

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MN1     Vbias2  Vbiasn  0       0       NMOS L=2 W=10
MN2     Vbias1  Vbiasn  0       0       NMOS L=2 W=10
MN3     Vncas   Vncas   vn1     0       NMOS L=2 W=10
MN4     vn1     Vbias3  vn2     0       NMOS L=2 W=10
MN5     vn2     vn1     0       0       NMOS L=2 W=10
MN6     Vbias3  Vbias3  0       0       NMOS L=10 W=10
MN7     Vbias4  Vbias3  Vlow    0       NMOS L=2 W=10
MN8     Vlow    Vbias4  0       0       NMOS L=2 W=10
MN9     Vpcas   Vbias3  vn3     0       NMOS L=2 W=10
MN10    vn3     Vbias4  0       0       NMOS L=2 W=10

MP1     Vbias2  Vbias2  VDD     VDD     PMOS L=10 W=30
MP2     Vhigh   Vbias1  VDD     VDD     PMOS L=2 W=30
```

```
MP3     Vbias1   Vbias2   Vhigh   VDD   PMOS L=2 W=30
MP4     vp1      Vbias1   VDD     VDD   PMOS L=2 W=30
MP5     Vncas    Vbias2   vp1     VDD   PMOS L=2 W=30
MP6     vp2      Vbias1   VDD     VDD   PMOS L=2 W=30
MP7     Vbias3   Vbias2   vp2     VDD   PMOS L=2 W=30
MP8     vp3      Vbias1   VDD     VDD   PMOS L=2 W=30
MP9     Vbias4   Vbias2   vp3     VDD   PMOS L=2 W=30
MP10    vp4      vp5      VDD     VDD   PMOS L=2 W=30
MP11    vp5      Vbias2   vp4     VDD   PMOS L=2 W=30
MP12    Vpcas    Vpcas    vp5     VDD   PMOS L=2 W=30

MBM1    Vbiasn   Vbiasn   0       0     NMOS L=2 W=10
MBM2    Vbiasp   Vbiasn   Vr      0     NMOS L=2 W=40
MBM3    Vbiasn   Vbiasp   VDD     VDD   PMOS L=2 W=30
MBM4    Vbiasp   Vbiasp   VDD     VDD   PMOS L=2 W=30

Rbias   Vr       0        6.5k

MSU1    Vsur     Vbiasn   0       0     NMOS L=2   W=10
MSU2    Vsur     Vsur     VDD     VDD   PMOS L=100 W=10
MSU3    Vbiasp   Vsur     Vbiasn  0     NMOS L=1   W=10

.ends
```




Degrees
ph(vout/vs)
200.0
150.0
100.0
50.0
0.0
-50.0
100
10^3
10^4
10^5
10^6
10^7
10^8
10^9
frequency
Hz

Problem21.11
Given: An ideal current source of 10uA driving a PMOS load.
To investigate: Gain of the amplifier with and without body effect.
The schematic of the circuit is as shown in the figure below:



Theory:
Without body effect:
The gain of the amplifier without body effect can be calculated from the circuit shown below. Disregard the dependent current source Gm.Vsb.
Therefore the gain of the amplifier can be calculated as

$$V_{sg}=-(V_{in}-V_{out})=V_{out}-V_{in}.$$

$$V_{out}= Gm.Vsg.R_o = g_m R_o (V_{out} - V_{in})$$

$$\Rightarrow \frac{Vout}{Vin} = \frac{g_m R_o}{1+ g_m R_o} \cong 1$$

The gain of the amplifier is positive because of the direction of the current flowing in the device.

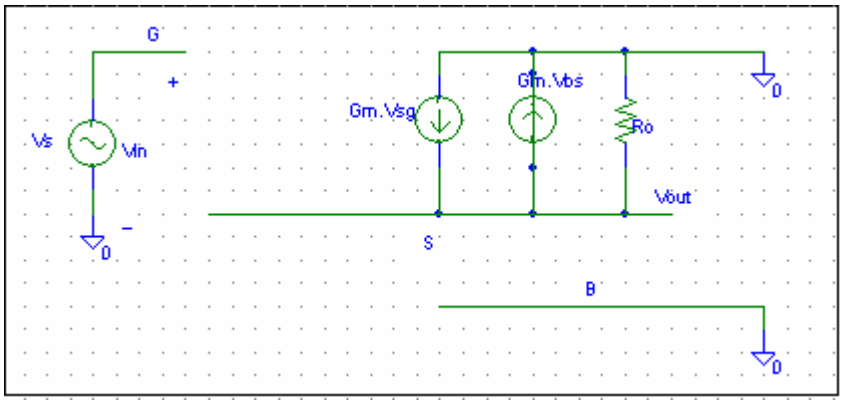


Figure showing the small signal equivalent circuit

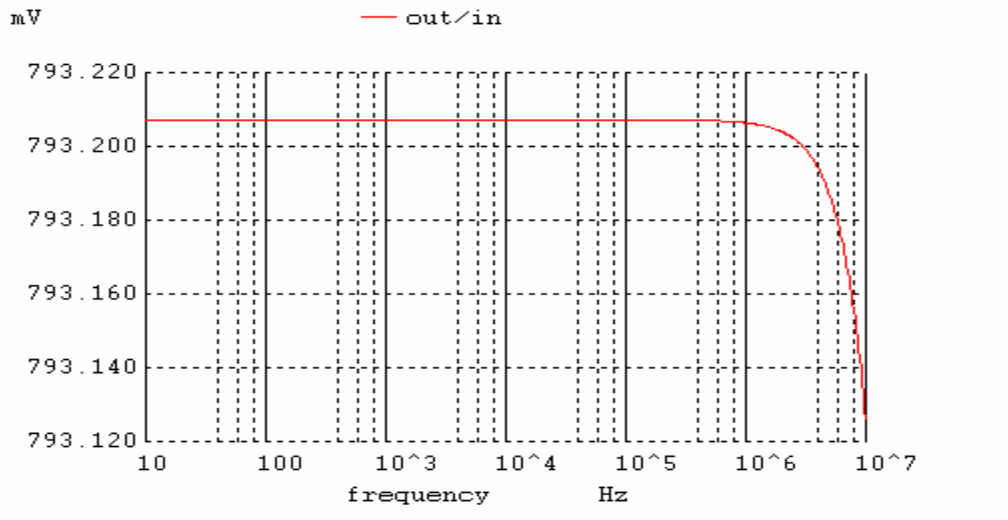
With Body Effect:
The gain of the amplifier with body effect can be found from the same equivalent circuit by considering the second current source.

$$Vout = g_m V_{sg} R_o - g_{mb} V_{bs} R_o = g_m R_o (V_{out} - V_{in}) - g_{mb} R_o (-V_{out})$$
$$= V_{out} R_o (g_m + g_{mb}) - V_{in}\, g_m R_o$$

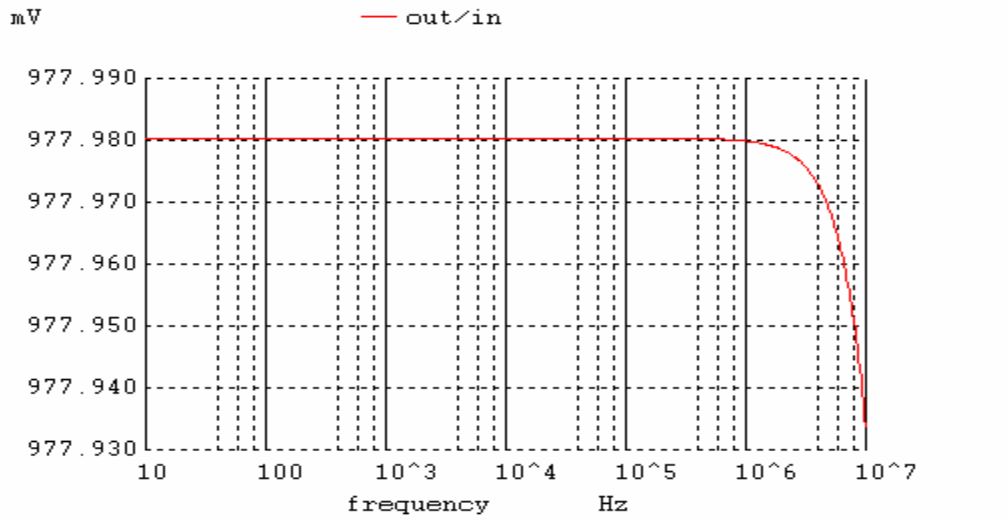
$$\frac{Vout}{Vin} \cong \frac{g_m}{g_{m+}\, g_{mb}} = \frac{1}{1+\eta} \langle 1 \qquad \text{where} \qquad \eta = \frac{g_m}{g_{mb}} \cong 0.4$$

Simulations:

With Body Effect:



Without body effect:



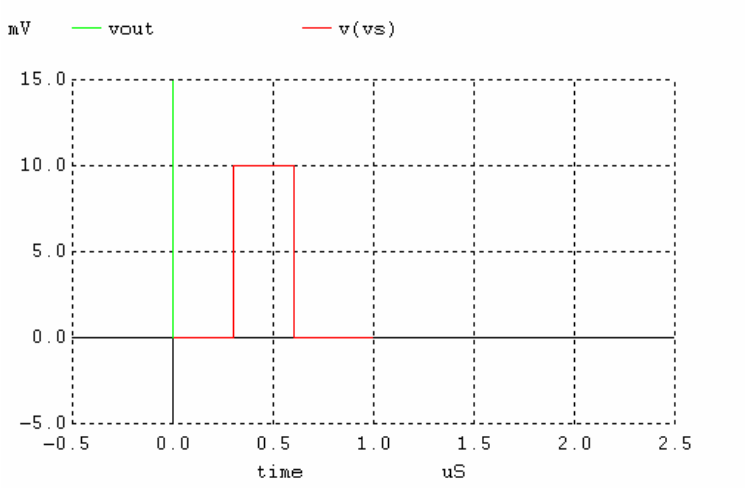
Netlist for the above simulations:

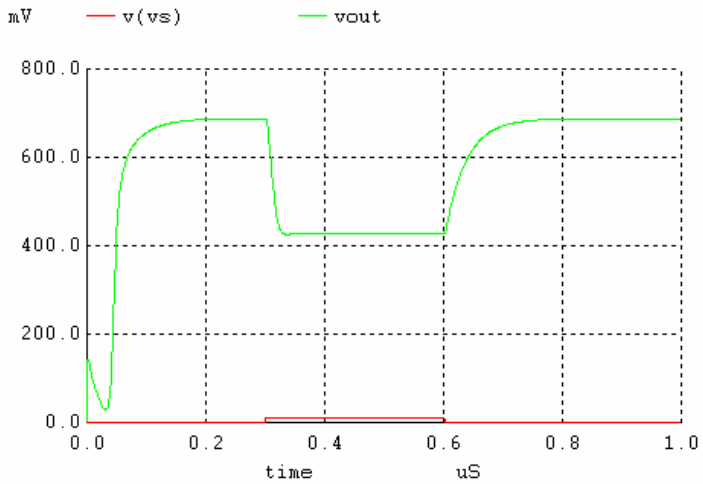
```
.control
destroy all
run
plot out/in
.endc

.options scale=50n rshunt=1e+7

.AC     DEC   100     10      10Meg

Ibias   vdd     out     DC      10u
Mp      0       in      out     out     PMOS L=2 W=100
*Mp     0       in      out     vdd     PMOS L=2 W=100

Vdd     Vdd     0       DC      1
Rbig    bias    in      10G
vbias   bias    0       DC      0
Cbig    vs       in     10
Vin     vs      0       DC      0       AC      1m
```

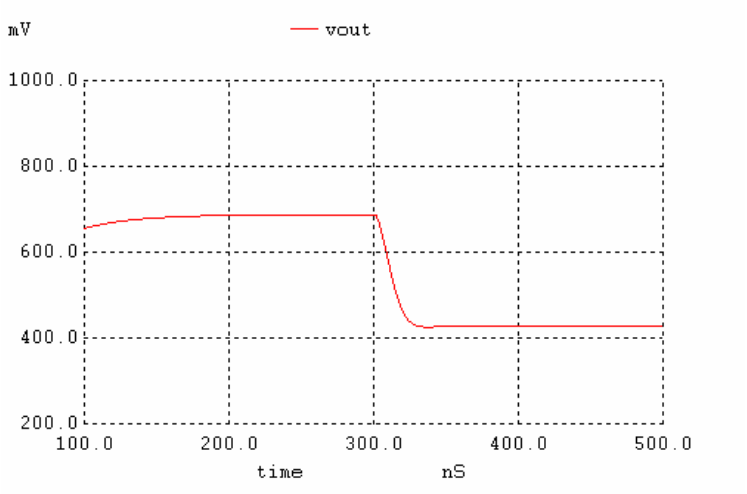
Hw 21.12

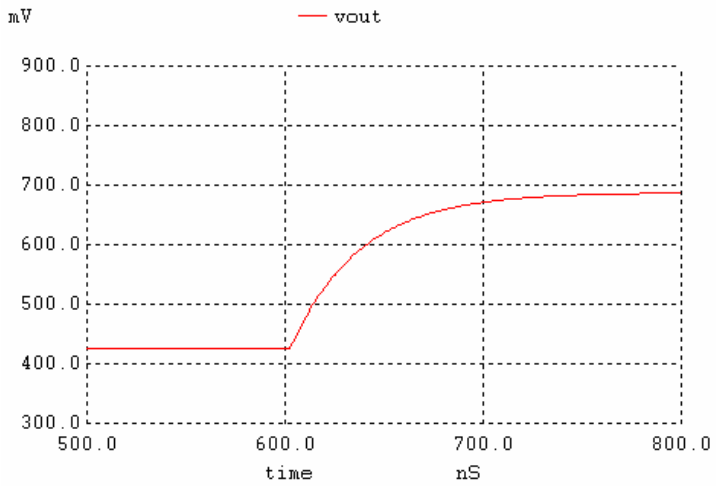
The combination of cascode and source follower circuit should not exhibit slew rate limitation in the discharge path. This is because the cascode has a very high gain, so any small increase input voltage should pull the input of M7 significantly low and turning on the transistor M7 more (meaning operating deep in saturation). While the charging path for the output capacitor is a fixed current source which has the slew rate limitation. Also we should take into consideration the 10K output resistor which helps in the discharge. Still we have a small slew rate during the discharge which is significantly low when compared with the slew rate during the charging.

The below attached sims shows this.





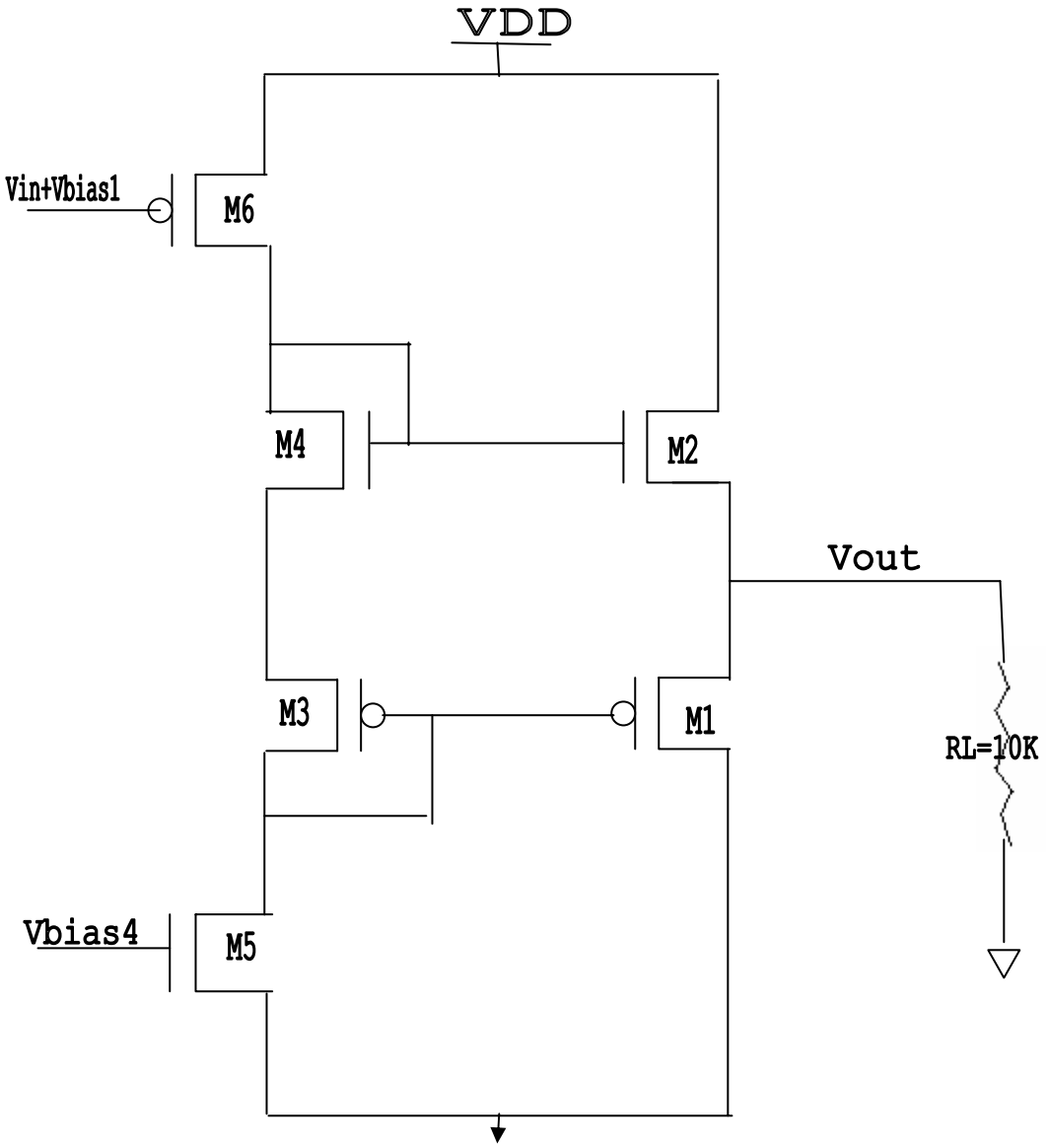





```
*** HW 21.12 CMOS: Circuit Design, Layout, and Simulation ***

.control
destroy all
run
plot v(vs)
plot vout
.endc

.option scale=50n ITL1=300
.tran 1n 1u UIC
**.op

VDD   VDD   0     DC    1
Vs    Vs    0     DC    .5    pulse 0 10m 300n 0 0 300n

Xbias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

M1    Vd1   Vin   0     0     NMOS L=2 W=50
M2    Voutcas     Vbias3      Vd1   0     NMOS L=2 W=50
M3    Voutcas     Vbias2      Vd4   VDD   PMOS L=2 W=100
M4    Vd4   Vbias1      VDD   VDD   PMOS L=2 W=100
```

```
M5    Vd5   Vbias1      VDD   VDD   PMOS L=2 W=1250
M6    Vout  Vbias2      Vd5   VDD   PMOS L=2 W=1250
M7    0     Voutcas     Vout  Vout  PMOS L=2 W=1250

Cload Vout  0     1p
Rload Vout  0     10k
Cbig  Vin   Vss   10u IC=362m
Rbig  Voutcas     Vin   10MEG
Rs    Vs    Vss   100k

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1   Vbias3      Vbiasp      VDD   VDD   PMOS L=2 W=100
MP2   Vbias4      Vbiasp      VDD   VDD   PMOS L=2 W=100
MP3   vp1   vp2   VDD   VDD   PMOS L=2 W=100
MP4   vp2   Vbias2      vp1   VDD   PMOS L=2 W=100
MP5   Vpcas Vpcas vp2   VDD   PMOS L=2 W=100
MP6   Vbias2      Vbias2      VDD   VDD   PMOS L=10 W=20
MP7   Vhigh Vbias1      VDD   VDD   PMOS L=2 W=100
MP8   Vbias1      Vbias2      Vhigh VDD   PMOS L=2 W=100
MP9   vp3   Vbias1      VDD   VDD   PMOS L=2 W=100
MP10  Vncas Vbias2      vp3   VDD   PMOS L=2 W=100

MN1   Vbias3      Vbias3      0     0     NMOS L=10 W=10
MN2   Vbias4      Vbias3      Vlow  0     NMOS L=2 W=50
MN3   Vlow  Vbias4      0     0     NMOS L=2 W=50
MN4   Vpcas Vbias3      vn1   0     NMOS L=2 W=50
MN5   vn1   Vbias4      0     0     NMOS L=2 W=50
MN6   Vbias2      Vbias3      vn2   0     NMOS L=2 W=50
MN7   vn2   Vbias4      0     0     NMOS L=2 W=50
MN8   Vbias1      Vbias3      vn3   0     NMOS L=2 W=50
MN9   vn3   Vbias4      0     0     NMOS L=2 W=50
MN10  Vncas Vncas vn4   0     NMOS L=2 W=50
MN11  vn4   Vbias3      vn5   0     NMOS L=2 W=50
MN12  vn5   vn4   0     0     NMOS L=2 W=50

MBM1  Vbiasn      Vbiasn      0     0     NMOS L=2 W=50
MBM2  Vreg  Vreg  Vr    0     NMOS L=2 W=200
MBM3  Vbiasn      Vbiasp      VDD   VDD   PMOS L=2 W=100
MBM4  Vreg  Vbiasp      VDD   VDD   PMOS L=2 W=100

Rbias Vr    0     5.5k

*amplifier
MA1   Vamp  Vreg  0     0     NMOS L=2 W=50
MA2   Vbiasp      Vbiasn      0     0     NMOS L=2 W=50
MA3   Vamp  Vamp  VDD   VDD   PMOS L=2 W=100
MA4   Vbiasp      Vamp  VDD   VDD   PMOS L=2 W=100

MCP   VDD   Vbiasp      VDD   VDD   PMOS L=100 W=100
*start-up stuff
MSU1  Vsur  Vbiasn      0     0     NMOS L=2   W=50
MSU2  Vsur  Vsur  VDD   VDD   PMOS L=20  W=10
MSU3  Vbiasp      Vsur  Vbiasn      0     NMOS L=1   W=10

.ends
```

Problem 21.13

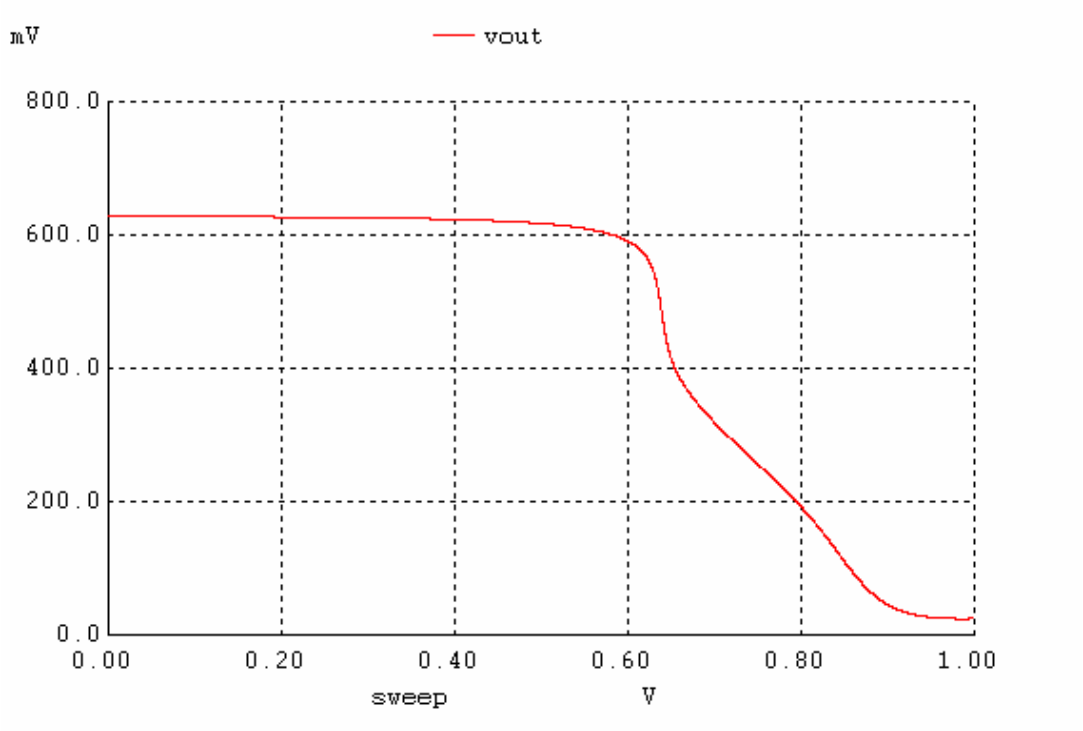


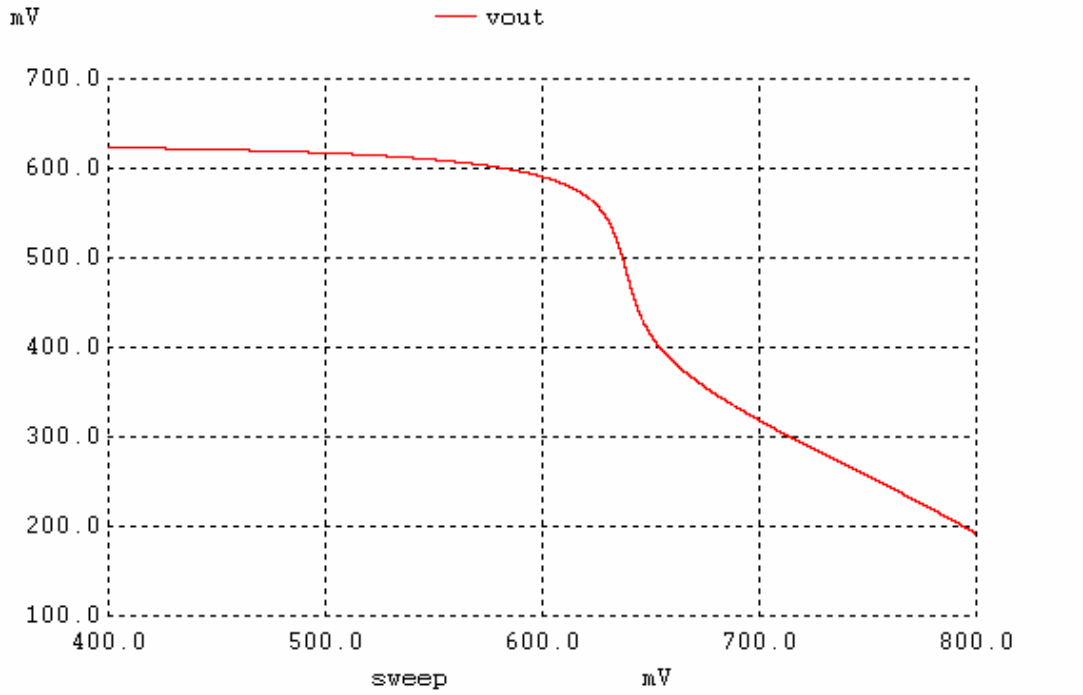
*** Problem 21.13 CMOS: Circuit Design, Layout, and Simulation ***

```
.control
destroy all
run
plot vout
.endc

.option scale=50n rshunt=1e7
.option itl5=0 itl1=1000
.dc vin   .4 .8 10u
VDD     VDD     0       DC      1
Vin     vin     0       DC      0
```

```
M6a     d4      vin     vdd     vdd     PMOS L=2 W=100
M4a     d4      d4      s3      s3      NMOS L=2 W=50
M3a     d5      d5      s3      s3      PMOS L=2 W=100
M5a     d5      vbias4  0       0       NMOS L=2 W=50
M2a     Vdd     d4      vout    vout    NMOS L=2 W=50
M1a     0       d5      vout    vout    PMOS L=2 W=100
Rl      s1      0       10k

Xbias   VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1     Vbias3  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP2     Vbias4  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP3     vp1     vp2     VDD     VDD     PMOS L=2 W=100
MP4     vp2     Vbias2  vp1     VDD     PMOS L=2 W=100
MP5     Vpcas   Vpcas   vp2     VDD     PMOS L=2 W=100
MP6     Vbias2  Vbias2  VDD     VDD     PMOS L=10 W=20
MP7     Vhigh   Vbias1  VDD     VDD     PMOS L=2 W=100
MP8     Vbias1  Vbias2  Vhigh   VDD     PMOS L=2 W=100
MP9     vp3     Vbias1  VDD     VDD     PMOS L=2 W=100
MP10    Vncas   Vbias2  vp3     VDD     PMOS L=2 W=100

MN1     Vbias3  Vbias3  0       0       NMOS L=10 W=10
MN2     Vbias4  Vbias3  Vlow    0       NMOS L=2 W=50
MN3     Vlow    Vbias4  0       0       NMOS L=2 W=50
MN4     Vpcas   Vbias3  vn1     0       NMOS L=2 W=50
MN5     vn1     Vbias4  0       0       NMOS L=2 W=50
MN6     Vbias2  Vbias3  vn2     0       NMOS L=2 W=50
MN7     vn2     Vbias4  0       0       NMOS L=2 W=50
MN8     Vbias1  Vbias3  vn3     0       NMOS L=2 W=50
MN9     vn3     Vbias4  0       0       NMOS L=2 W=50
MN10    Vncas   Vncas   vn4     0       NMOS L=2 W=50
MN11    vn4     Vbias3  vn5     0       NMOS L=2 W=50
MN12    vn5     vn4     0       0       NMOS L=2 W=50

MBM1    Vbiasn  Vbiasn  0       0       NMOS L=2 W=50
MBM2    Vreg    Vreg    Vr      0       NMOS L=2 W=200
MBM3    Vbiasn  Vbiasp  VDD     VDD     PMOS L=2 W=100
MBM4    Vreg    Vbiasp  VDD     VDD     PMOS L=2 W=100

Rbias   Vr      0       5.5k

*amplifier
MA1     Vamp    Vreg    0       0       NMOS L=2 W=50
MA2     Vbiasp  Vbiasn  0       0       NMOS L=2 W=50
MA3     Vamp    Vamp    VDD     VDD     PMOS L=2 W=100
MA4     Vbiasp  Vamp    VDD     VDD     PMOS L=2 W=100

MCP     VDD     Vbiasp  VDD     VDD     PMOS L=100 W=100

*start-up stuff
MSU1    Vsur    Vbiasn  0       0       NMOS L=2   W=50
MSU2    Vsur    Vsur    VDD     VDD     PMOS L=20  W=10
MSU3    Vbiasp  Vsur    Vbiasn  0       NMOS L=1   W=10
.ends
```

From simulations results we see that output voltage swing between 620mV and down to 20mv where as in hand calculations it should swing from 750mv to 250mv.





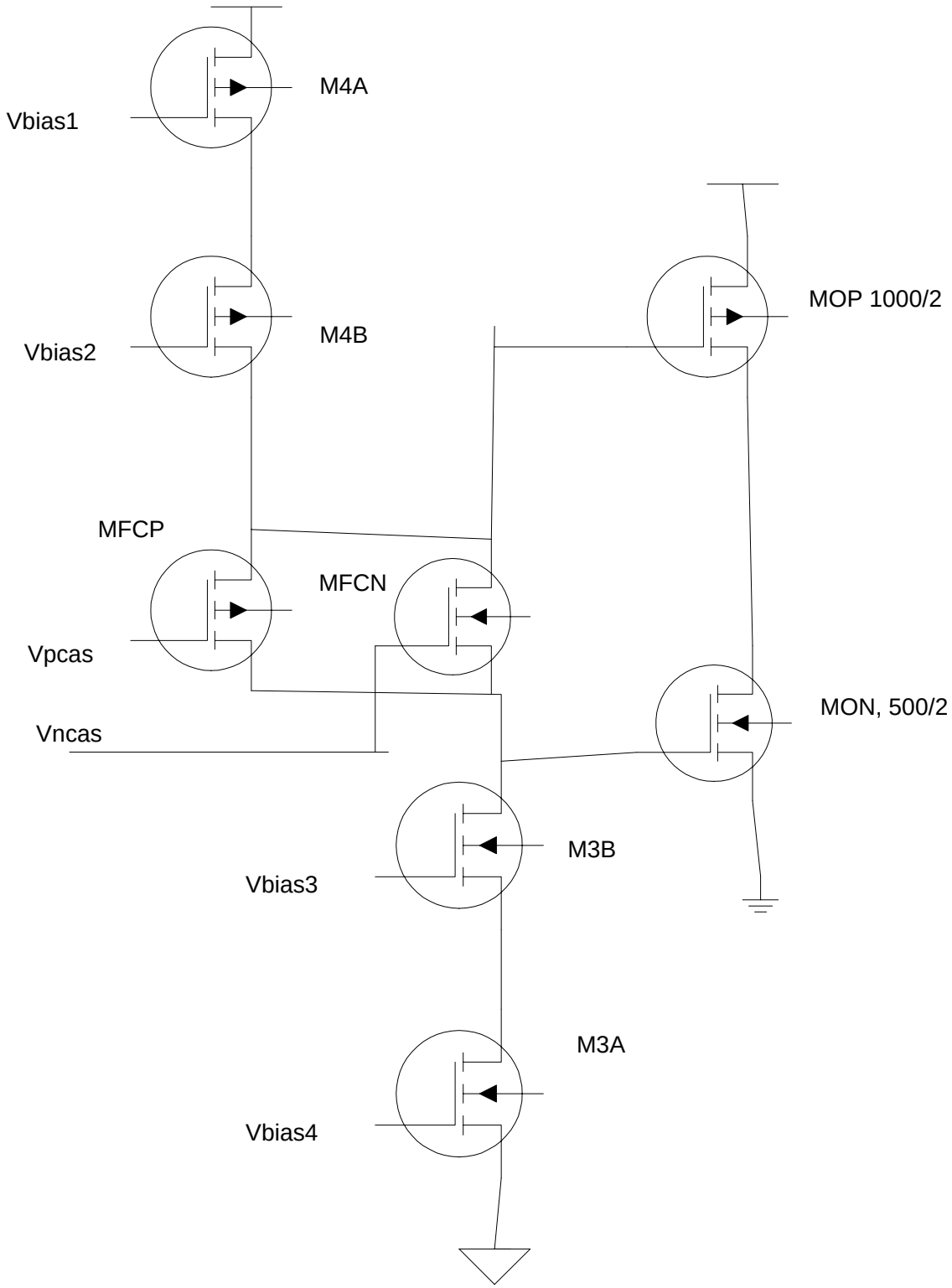


Figure 21.50 (Please refer text book)

Problem 21.14.
In the class AB output buffer in fig 21.50 or 21.51 a load resistor connected to ground causes the PMOS device to conduct more current. Why?

Ans) When a load resistor is connected, the PMOS device has to supply current to load to maintain output high and also current dissipated by NMOS device. So a PMOS device has to supply much larger current than an NMOS device.

Simulate if above device drives a 1K resistor and MON is reduced in size to 50/2. Is it a better design? Why or Why Not.

Ans) Simulations results are given below for MON W=500 and W=100 (Convergence problem with W=50) and I didn't see much difference in simulations. So its not a bad design to have a smaller W for MON

Theoretically, if the gain of first stage (floating gate op-amp) is less then vin may not toggle fully and in turn may create problems by turning on both the devices (MOP and MON) simultaneously for long time. But with reasonable first stage gain there shouldn't be any problems with a smaller width MON device.

Also the above configuration is push pull configuration. So if MOP turns on MON turns off and vice versa. This allows us to design the circuit with smaller MON widths. The same is not true for MOP transistors because it has to supply atleast Iload current to maintain output high (Iload=VDD/outputload resistance).

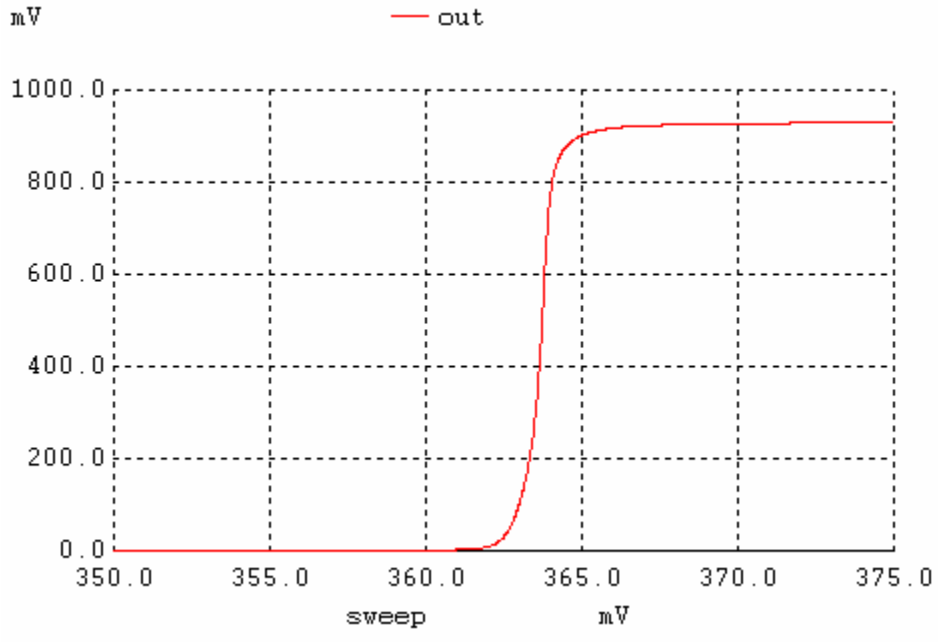


Fig.A MON W=500 and load resistor 1Kohm

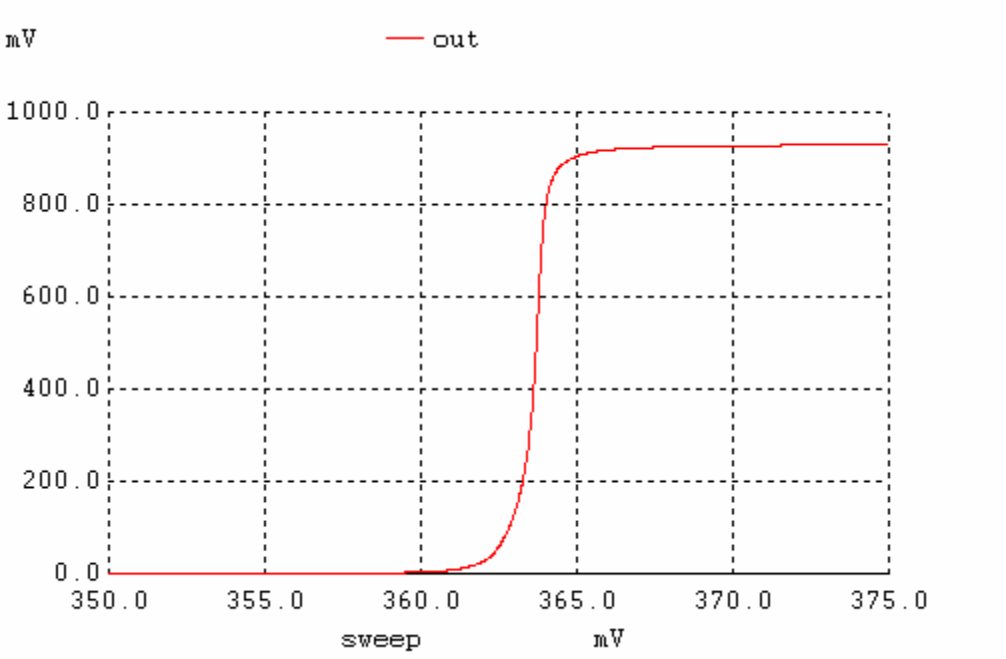
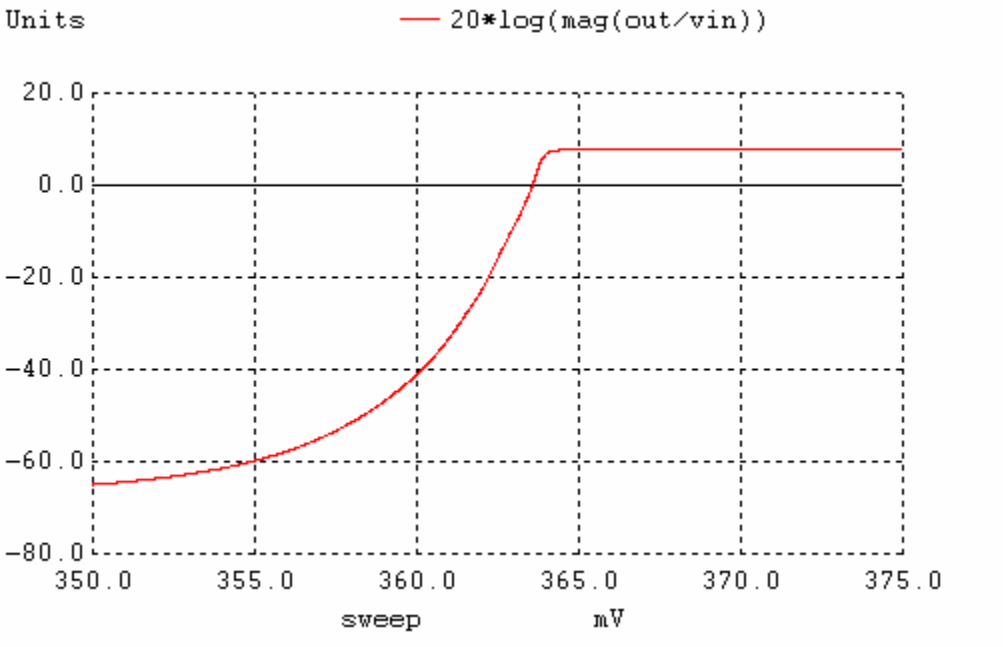


Fig.B MON W=100 and load resistor 1Kohm



Gain of the Op-Amp (Looks very similar for W=100 and W=500)

*** Figure 21.14 CMOS: Circuit Design, Layout, and Simulation ***

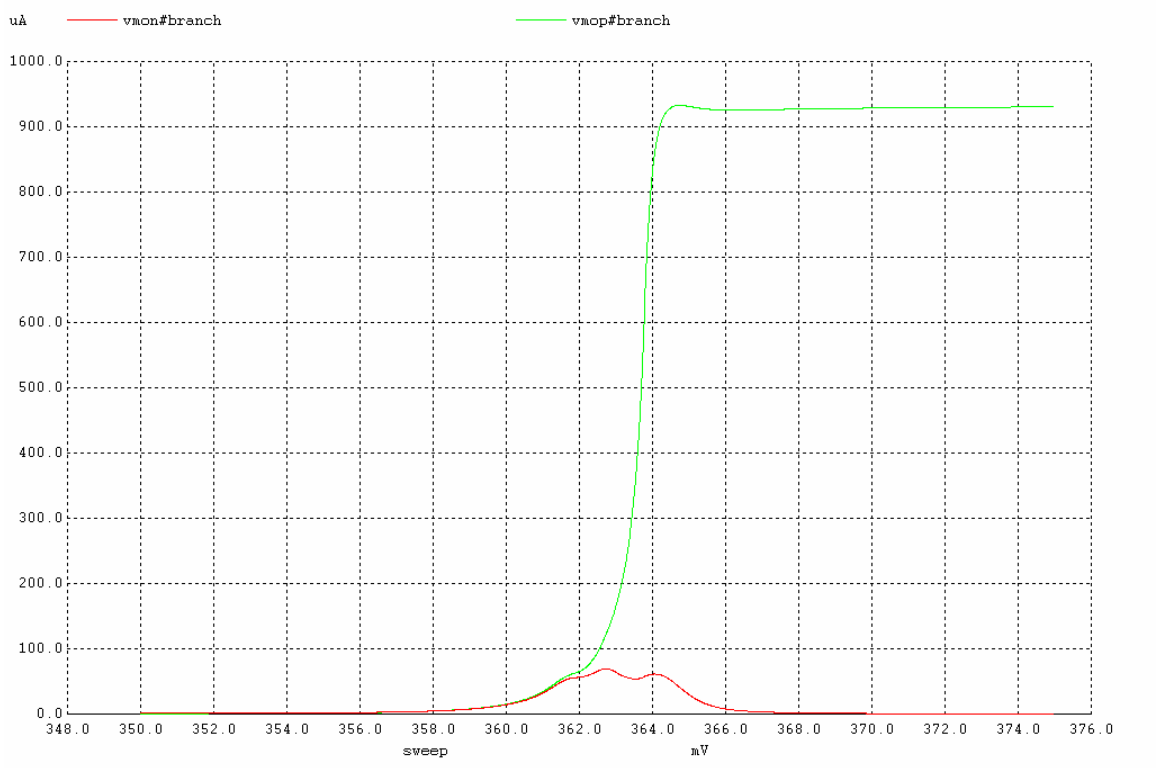
```
.control
destroy all
run
plot out
let Av=deriv(out)
plot 20*log(mag(out/vin))
plot Av
.endc

.option scale=50n  rshunt=1e7
.dc vin      0.35 0.375 10u

VDD      VDD      0        DC       1
Vin      Vin      0        DC       0

RL       out      0        1k

Xbias    VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

M4A      vp1      Vbias1   VDD      VDD      PMOS L=2 W=100
M4B      vp2      Vbias2   vp1      VDD      PMOS L=2 W=100
MFCP     vn2      Vpcas    vp2      VDD      PMOS L=2 W=50
MFCN     vp2      Vncas    vn2      0        NMOS L=2 W=25
M3B      vn2      Vbias3   vn1      0        NMOS L=2 W=50
M3A      vn1      Vin      0        0        NMOS L=2 W=50

MON      out      vn2      0        0        NMOS L=2 W=500
MOP      out      vp2      VDD      VDD      PMOS L=2 W=1000

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1      Vbias3   Vbiasp   VDD      VDD      PMOS L=2 W=100
MP2      Vbias4   Vbiasp   VDD      VDD      PMOS L=2 W=100
MP3      vp1      vp2      VDD      VDD      PMOS L=2 W=100
MP4      vp2      Vbias2   vp1      VDD      PMOS L=2 W=100
MP5      Vpcas    Vpcas    vp2      VDD      PMOS L=2 W=100
MP6      Vbias2   Vbias2   VDD      VDD      PMOS L=10 W=20
MP7      Vhigh    Vbias1   VDD      VDD      PMOS L=2 W=100
MP8      Vbias1   Vbias2   Vhigh    VDD      PMOS L=2 W=100
MP9      vp3      Vbias1   VDD      VDD      PMOS L=2 W=100
MP10     Vncas    Vbias2   vp3      VDD      PMOS L=2 W=100

MN1      Vbias3   Vbias3   0        0        NMOS L=10 W=10
MN2      Vbias4   Vbias3   Vlow     0        NMOS L=2 W=50
MN3      Vlow     Vbias4   0        0        NMOS L=2 W=50
MN4      Vpcas    Vbias3   vn1      0        NMOS L=2 W=50
MN5      vn1      Vbias4   0        0        NMOS L=2 W=50
MN6      Vbias2   Vbias3   vn2      0        NMOS L=2 W=50
MN7      vn2      Vbias4   0        0        NMOS L=2 W=50
MN8      Vbias1   Vbias3   vn3      0        NMOS L=2 W=50
MN9      vn3      Vbias4   0        0        NMOS L=2 W=50
MN10     Vncas    Vncas    vn4      0        NMOS L=2 W=50
MN11     vn4      Vbias3   vn5      0        NMOS L=2 W=50
MN12     vn5      vn4      0        0        NMOS L=2 W=50

MBM1     Vbiasn   Vbiasn   0        0        NMOS L=2 W=50
MBM2     Vreg     Vreg     Vr       0        NMOS L=2 W=200
MBM3     Vbiasn   Vbiasp   VDD      VDD      PMOS L=2 W=100
MBM4     Vreg     Vbiasp   VDD      VDD      PMOS L=2 W=100

Rbias    Vr       0        5.5k

*amplifier
MA1      Vamp     Vreg     0        0        NMOS L=2 W=50
MA2      Vbiasp   Vbiasn   0        0        NMOS L=2 W=50
```

```
MA3     Vamp    Vamp    VDD     VDD     PMOS L=2 W=100
MA4     Vbiasp  Vamp    VDD     VDD     PMOS L=2 W=100

MCP     VDD     Vbiasp  VDD     VDD     PMOS L=100 W=100

*start-up stuff
MSU1    Vsur    Vbiasn  0       0       NMOS L=2   W=50
MSU2    Vsur    Vsur    VDD     VDD     PMOS L=20  W=10
MSU3    Vbiasp  Vsur    Vbiasn  0       NMOS L=1   W=10

.ends
```

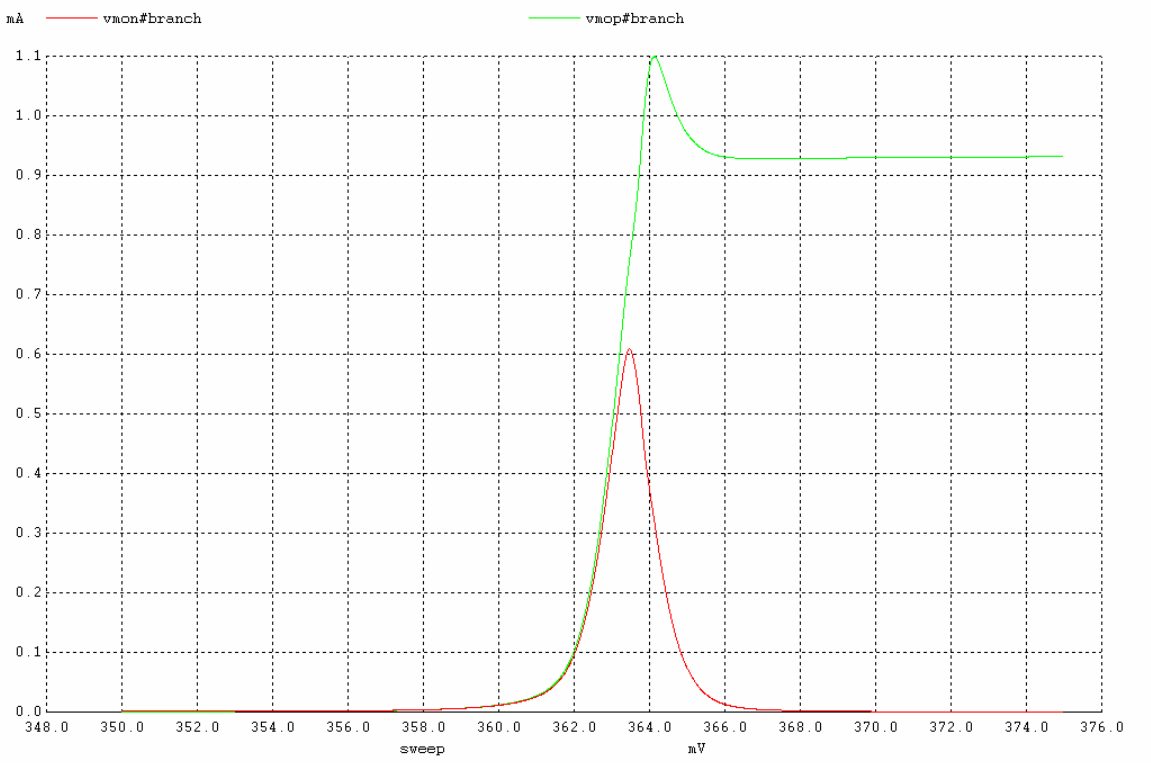
Problem 21.15

Using simulations show the problem of using an inverter output buffer without a floating current source as seen in Fig. 21.53 (the quiescent current that flows in the MOSFETs is huge and not accurately controlled as it is in Fig. 21.50)

First lets simulate the circuit of Figure 21.51 with a load resistor of 1k and a floating current source. The current that flows through the MOSFETs, MON and MOP, can be seen in the plot below:



Now we will simulate the same circuit but this time we will remove the floating current source from the output buffer. The currents now flowing through MON and MOP are shown in the plot below:



Examining the two plots we can see that the current flowing through the MOSFETs has essentially gone up by about a factor of 10. They are both conducting currents near a milli-Amp. This is a huge amount of current flowing and is a problem that can be solved by using the floating current source on the output buffer.

The Net list can be seen below:
Problem 21.15

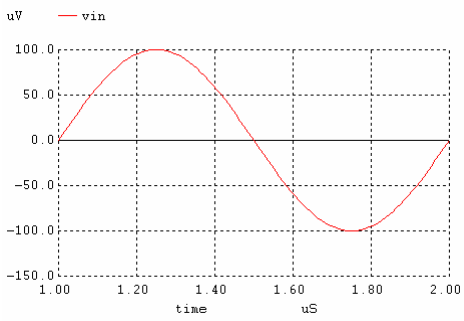
```
.control
destroy all
run
plot out
let Av=deriv(out)
plot Av
.endc

.option scale=50n rshunt=1e7 ITL1=300
.dc vin 0.35 0.375 10u

VDD   VDD   0       DC     1
Vin   Vin   0       DC     0
```

```
Vmop  vdd     mop    DC=0
Vmon  mon     0      DC=0

RL    out     0      1k

Xbias  VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias

*----- output buffer with floating current source -----
*M4A  vp1     Vbias1 VDD   VDD   PMOS L=2 W=100
*M4B  vp2     Vbias2 vp1   VDD   PMOS L=2 W=100
*MFCP         vn2    Vpcas vp2   VDD   PMOS L=2 W=50
*MFCN         vp2    Vncas vn2   0     NMOS L=2 W=25
*M3B  vn2     Vbias3 vn1   0     NMOS L=2 W=50
*M3A  vn1     Vin    0     0     NMOS L=2 W=50

*MON  out     vn2    mon   0     NMOS L=2 W=500
*MOP  out     vp2    mop   VDD   PMOS L=2 W=1000
*-------------------------------------------------------

*----- output buffer without floating current source -----
M4A   vp1     Vbias1 VDD   VDD   PMOS L=2 W=100
M4B   v2      Vbias2 vp1   VDD   PMOS L=2 W=100
M3B   v2      Vbias3 vn1   0     NMOS L=2 W=50
M3A   vn1     Vin    0     0     NMOS L=2 W=50

MON   out     v2     mon   0     NMOS L=2 W=500
MOP   out     v2     mop   VDD   PMOS L=2 W=1000
*-------------------------------------------------------

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas

MP1   Vbias3 Vbiasp VDD   VDD   PMOS L=2 W=100
MP2   Vbias4 Vbiasp        VDD   VDD   PMOS L=2 W=100
MP3   vp1    vp2    VDD   VDD   PMOS L=2 W=100
MP4   vp2    Vbias2 vp1   VDD   PMOS L=2 W=100
MP5   Vpcas  Vpcas  vp2   VDD   PMOS L=2 W=100
MP6   Vbias2 Vbias2 VDD   VDD   PMOS L=10 W=20
MP7   Vhigh  Vbias1 VDD   VDD   PMOS L=2 W=100
MP8   Vbias1 Vbias2 Vhigh VDD   PMOS L=2 W=100
MP9   vp3    Vbias1 VDD   VDD   PMOS L=2 W=100
MP10  Vncas  Vbias2 vp3   VDD   PMOS L=2 W=100

MN1   Vbias3 Vbias3 0     0     NMOS L=10 W=10
MN2   Vbias4 Vbias3 Vlow  0     NMOS L=2 W=50
MN3   Vlow   Vbias4 0     0     NMOS L=2 W=50
MN4   Vpcas  Vbias3 vn1   0     NMOS L=2 W=50
```

```
MN5   vn1      Vbias4 0      0      NMOS L=2 W=50
MN6   Vbias2   Vbias3 vn2    0      NMOS L=2 W=50
MN7   vn2      Vbias4 0      0      NMOS L=2 W=50
MN8   Vbias1   Vbias3 vn3    0      NMOS L=2 W=50
MN9   vn3      Vbias4 0      0      NMOS L=2 W=50
MN10  Vncas    Vncas  vn4    0      NMOS L=2 W=50
MN11  vn4      Vbias3 vn5    0      NMOS L=2 W=50
MN12  vn5      vn4    0      0      NMOS L=2 W=50

MBM1  Vbiasn   Vbiasn 0      0      NMOS L=2 W=50
MBM2  Vreg     Vreg   Vr     0      NMOS L=2 W=200
MBM3  Vbiasn   Vbiasp VDD    VDD    PMOS L=2 W=100
MBM4  Vreg     Vbiasp VDD    VDD    PMOS L=2 W=100

Rbias  Vr      0      5.5k

*amplifier
MA1   Vamp   Vreg   0      0      NMOS L=2 W=50
MA2   Vbiasp Vbiasn 0      0      NMOS L=2 W=50
MA3   Vamp   Vamp   VDD    VDD    PMOS L=2 W=100
MA4   Vbiasp Vamp   VDD    VDD    PMOS L=2 W=100

MCP   VDD    Vbiasp VDD    VDD    PMOS L=100 W=100

*start-up stuff
MSU1  Vsur   Vbiasn 0      0      NMOS L=2   W=50
MSU2  Vsur   Vsur   VDD    VDD    PMOS L=20  W=10
MSU3  Vbiasp Vsur   Vbiasn 0      NMOS L=1   W=10

.ends
.include C:.\50nm_models.txt
.end
```

P21.16

Pictured in figure 1 are the time domain Vin and Vout for figure 21.56. These figures and the table will be used to prove that the distortion the output of figure 21.56 introduces into the signal is **NOT** a function of load resistance.



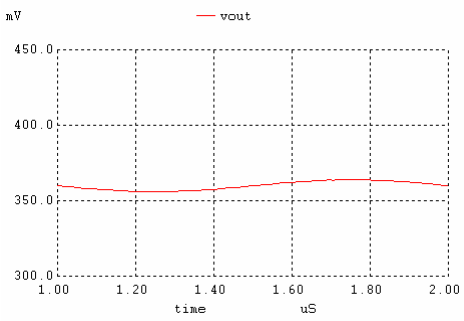


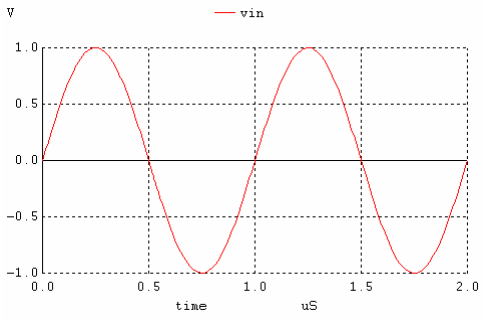
Figure 1. $Vin = 1mV * \sin(2 * \pi * 1Meg * t)$
R=1kΩ

Fourier analysis for vout:
No. Harmonics: 10, THD: 0.0458857 %, Gridsize: 200, Interpolation Degree: 1

Harmonic	Frequency	Magnitude	Phase	Norm. Mag	Norm. Phase
0	0.000000e+00	3.599225e-01	0.000000e+00	0.000000e+00	0.000000e+00
1	1.000000e+06	3.927684e-03	1.792860e+02	1.000000e+00	0.000000e+00
2	2.000000e+06	1.589805e-06	-8.67448e+01	4.047692e-04	-2.66031e+02
3	3.000000e+06	1.165721e-07	1.025288e+02	2.967960e-05	-7.67572e+01
4	4.000000e+06	3.252076e-07	-1.27064e+02	8.279883e-05	-3.06350e+02
5	5.000000e+06	2.983814e-07	-9.08216e+01	7.596879e-05	-2.70108e+02
6	6.000000e+06	1.650966e-07	-4.96128e+01	4.203410e-05	-2.28899e+02
7	7.000000e+06	4.616759e-07	8.708092e+00	1.175441e-04	-1.70578e+02
8	8.000000e+06	3.456645e-07	-1.40388e+02	8.800723e-05	-3.19674e+02
9	9.000000e+06	3.903018e-07	1.587072e+02	9.937201e-05	-2.05788e+01

Table 1.

When the input amplitude is changed to 1 volt and the load resistance is left the same, (figure 2, and table 2,) the THD increases to 42.6%, and the output voltage is distorted to the point of becoming a square wave.



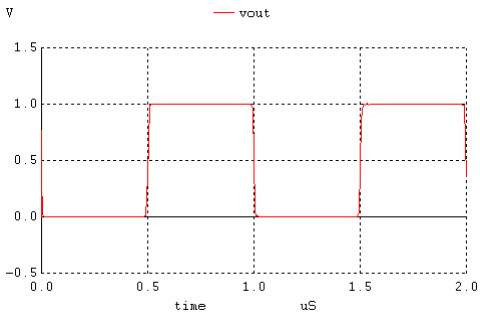


Figure 2. $Vin = 1V * \sin(2 * \pi * 1Meg * t)$
R=1kΩ

Fourier analysis for vout:
No. Harmonics: 10, THD: 42.6124 %, Gridsize: 200, Interpolation Degree: 1

Harmonic	Frequency	Magnitude	Phase	Norm. Mag	Norm. Phase
0	0.000000e+00	4.978901e-01	0.000000e+00	0.000000e+00	0.000000e+00
1	1.000000e+06	6.353245e-01	-1.79839e+02	1.000000e+00	0.000000e+00
2	2.000000e+06	4.718600e-03	-8.96841e+01	7.427071e-03	9.015497e+01
3	3.000000e+06	2.119830e-01	-1.79508e+02	3.336610e-01	3.315798e-01
4	4.000000e+06	4.347708e-03	-8.92331e+01	6.843288e-03	9.060596e+01
5	5.000000e+06	1.254022e-01	-1.79165e+02	1.973829e-01	6.744908e-01
6	6.000000e+06	4.471291e-03	-8.87649e+01	7.037808e-03	9.107421e+01
7	7.000000e+06	8.899816e-02	-1.78825e+02	1.400830e-01	1.014236e+00
8	8.000000e+06	4.298701e-03	-8.81854e+01	6.766150e-03	9.165369e+01
9	9.000000e+06	6.804643e-02	-1.78471e+02	1.071050e-01	1.368293e+00

Table 2.

Below, in figure 3 and table 3, the resistance is decreased to 500Ω, but the THD and the output waveform stay the same.

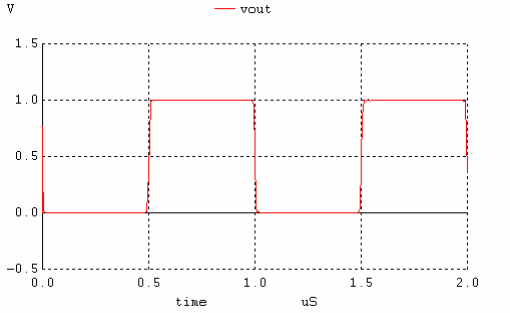


Figure 3. $Vin = 1V * \sin(2 * \pi * 1Meg * t)$
R=500Ω

Fourier analysis for vout:
No. Harmonics: 10, THD: 42.6124 %, Gridsize: 200, Interpolation Degree: 1

Harmonic	Frequency	Magnitude	Phase	Norm. Mag	Norm. Phase
0	0.000000e+00	4.978901e-01	0.000000e+00	0.000000e+00	0.000000e+00
1	1.000000e+06	6.353245e-01	-1.79839e+02	1.000000e+00	0.000000e+00
2	2.000000e+06	4.718600e-03	-8.96841e+01	7.427071e-03	9.015497e+01
3	3.000000e+06	2.119830e-01	-1.79508e+02	3.336610e-01	3.315798e-01
4	4.000000e+06	4.347708e-03	-8.92331e+01	6.843288e-03	9.060596e+01
5	5.000000e+06	1.254022e-01	-1.79165e+02	1.973829e-01	6.744908e-01
6	6.000000e+06	4.471291e-03	-8.87649e+01	7.037808e-03	9.107421e+01
7	7.000000e+06	8.899816e-02	-1.78825e+02	1.400830e-01	1.014236e+00
8	8.000000e+06	4.298701e-03	-8.81854e+01	6.766150e-03	9.165369e+01
9	9.000000e+06	6.804643e-02	-1.78471e+02	1.071050e-01	1.368293e+00

Table 3.

In figure 4 and table 4, the resistance is increased to 10kΩ. Comparing figure 4 and table 4 with figure 3 and table 3 above, there is no change in either one. Therefore it can be concluded that the distortion at the output of figure 21.56 is not a function of the load resistance, but is a function of the amplitude of the input signal, (as discussed in the text.)

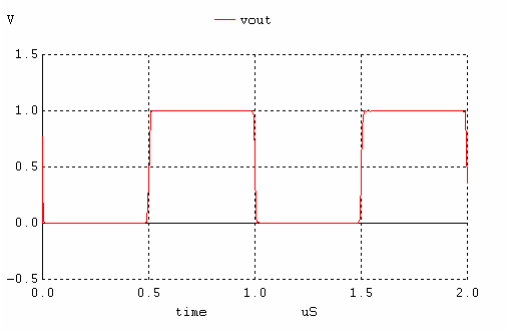


Figure 4. $Vin = 1V * \sin(2 * \pi * 1Meg * t)$
R=100kΩ

Fourier analysis for vout:
No. Harmonics: 10, THD: 42.6124 %, Gridsize: 200, Interpolation Degree: 1

Harmonic	Frequency	Magnitude	Phase	Norm. Mag	Norm. Phase
0	0.000000e+00	4.978901e-01	0.000000e+00	0.000000e+00	0.000000e+00
1	1.000000e+06	6.353245e-01	-1.79839e+02	1.000000e+00	0.000000e+00
2	2.000000e+06	4.718600e-03	-8.96841e+01	7.427071e-03	9.015497e+01
3	3.000000e+06	2.119830e-01	-1.79508e+02	3.336610e-01	3.315798e-01
4	4.000000e+06	4.347708e-03	-8.92331e+01	6.843288e-03	9.060596e+01
5	5.000000e+06	1.254022e-01	-1.79165e+02	1.973829e-01	6.744908e-01
6	6.000000e+06	4.471291e-03	-8.87649e+01	7.037808e-03	9.107421e+01
7	7.000000e+06	8.899816e-02	-1.78825e+02	1.400830e-01	1.014236e+00
8	8.000000e+06	4.298701e-03	-8.81854e+01	6.766150e-03	9.165369e+01
9	9.000000e+06	6.804643e-02	-1.78471e+02	1.071050e-01	1.368293e+00

Table 4.

```
*** Figure 21.56 CMOS: Circuit Design, Layout, and Simulation ***
.option scale=50n
.tran 10n 2u UIC
.four 1MEG Vout

VDD     VDD     0       DC      1
Vin     Vin     0       DC      0       sin 0 1 1MEG

RL      out     0       100k
Rbigp   Vbias1  vgp     1G
Cbigp   vgp     vin     1 IC=0.643
Rbign   Vout    vgn     1G
Cbign   Vgn     vin     1 IC=0.362

Xbias   VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias
MON     Vout    vgn     0       0       NMOS L=2 W=500
MOP     Vout    vgp     VDD     VDD     PMOS L=2 W=1000

.subckt bias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas
MP1     Vbias3  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP2     Vbias4  Vbiasp  VDD     VDD     PMOS L=2 W=100
MP3     vp1     vp2     VDD     VDD     PMOS L=2 W=100
MP4     vp2     Vbias2  vp1     VDD     PMOS L=2 W=100
MP5     Vpcas   Vpcas   vp2     VDD     PMOS L=2 W=100
MP6     Vbias2  Vbias2  VDD     VDD     PMOS L=10 W=20
MP7     Vhigh   Vbias1  VDD     VDD     PMOS L=2 W=100
MP8     Vbias1  Vbias2  Vhigh   VDD     PMOS L=2 W=100
MP9     vp3     Vbias1  VDD     VDD     PMOS L=2 W=100
MP10    Vncas   Vbias2  vp3     VDD     PMOS L=2 W=100
```

```
MN1     Vbias3  Vbias3  0       0       NMOS L=10 W=10
MN2     Vbias4  Vbias3  Vlow    0       NMOS L=2 W=50
MN3     Vlow    Vbias4  0       0       NMOS L=2 W=50
MN4     Vpcas   Vbias3  vn1     0       NMOS L=2 W=50
MN5     vn1     Vbias4  0       0       NMOS L=2 W=50
MN6     Vbias2  Vbias3  vn2     0       NMOS L=2 W=50
MN7     vn2     Vbias4  0       0       NMOS L=2 W=50
MN8     Vbias1  Vbias3  vn3     0       NMOS L=2 W=50
MN9     vn3     Vbias4  0       0       NMOS L=2 W=50
MN10    Vncas   Vncas   vn4     0       NMOS L=2 W=50
MN11    vn4     Vbias3  vn5     0       NMOS L=2 W=50
MN12    vn5     vn4     0       0       NMOS L=2 W=50

MBM1    Vbiasn  Vbiasn  0       0       NMOS L=2 W=50
MBM2    Vreg    Vreg    Vr      0       NMOS L=2 W=200
MBM3    Vbiasn  Vbiasp  VDD     VDD     PMOS L=2 W=100
MBM4    Vreg    Vbiasp  VDD     VDD     PMOS L=2 W=100

Rbias   Vr      0       5.5k

*amplifier
MA1     Vamp    Vreg    0       0       NMOS L=2 W=50
MA2     Vbiasp  Vbiasn  0       0       NMOS L=2 W=50
MA3     Vamp    Vamp    VDD     VDD     PMOS L=2 W=100
MA4     Vbiasp  Vamp    VDD     VDD     PMOS L=2 W=100

MCP     VDD     Vbiasp  VDD     VDD     PMOS L=100 W=100
*start-up stuff
MSU1    Vsur    Vbiasn  0       0       NMOS L=2   W=50
MSU2    Vsur    Vsur    VDD     VDD     PMOS L=20  W=10
MSU3    Vbiasp  Vsur    Vbiasn  0       NMOS L=1   W=10

.ends

* BSIM4 models
```