Lincoln Bollschweiler

28.1 Determine the number of quantization levels needed if one wanted to make a digital thermometer that was capable of measuring temperatures to within 0.1 ºC accuracy over a range from -50ºC to 150ºC. What resolution of ADC would be required?

If we need 0.lºC accuracy then if we use a resolution in measurements of every 0.2ºC we meet the requirement. For example, if the real temperature was 50.4º and we recorded a discrete point at either 50.5º or 50.3º then we would have 0.lº accuracy, worst case. Our discrete levels start at -49.9º and stop at 149.9º. We can use

$$n-1=\frac{\max-\min}{step}\Rightarrow n=\frac{149.9--49.9}{0.2}+1=1000 \text{ levels}$$

To find the resolution (number of bits needed) we can use (28.3).

$$\text{Number of input combinations} = 2^N$$

$$\text{N}=\log_2 1000 = 9.97$$

Since we cannot use a non-integer number of bits we find the needed resolution = 10 bits.

(28.2)Using the same thermometer as above, what sampling rate, in samples per second, would be required if the temperature displayed a frequency of 15°Sin(0.01.2πyt)?

The frequency of the displayed temperature is 0.01 Hz (F_{Signal_Max}). According to Nyquist criterion, the sampling frequency rate is at least two times the maximum frequency of the signal. For the given problem, the temperature is displayed at 0.01Hz. So the minimum sampling frequency is given by equation 28.2-1.

$$F_{Sampling} = 2.F_{Signal\_Max} \tag{28.2-1}$$

So, the minimum sampling rate required is 0.02 Hz or 0.02 samples per second.

Chris Gagliano

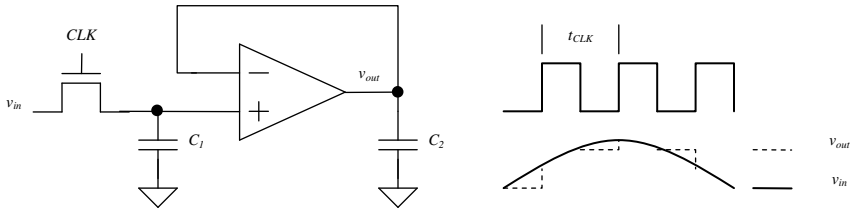
28.3 Determine the maximum droop allowed in a S/H used in a 16-bit ADC assuming that all other aspects of both the S/H and ADC are ideal. Assume $V_{ref} = 5\ V$.

A 16-bit ADC has 2^{16} quantization levels. Therefore, 1 LSB = $\frac{5V}{2^{16}} \approx 76.3\ \mu V$.

The droop should be no more than $\frac{1}{2}$ LSB, so the maximum droop allowed is $\approx 38\ \mu V$.

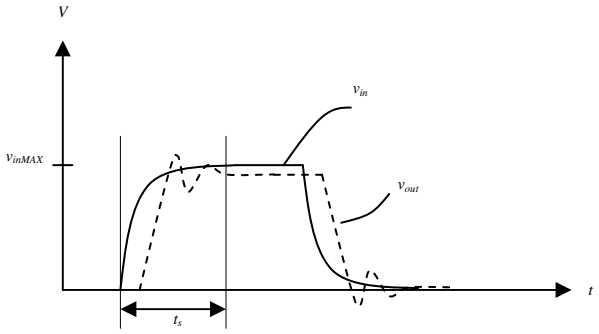
28.4 *An S/H circuit settles to within 1 percent of its final value at 5 μs. What is the maximum resolution and speed with which an ADC can use this data assuming that the ADC is ideal?*

F-1 shows a typical S/H circuit with corresponding input and output waveforms. The circuit contains one NMOS switch, two hold capacitors, and an amplifier placed in a gain of one configuration.



F-1 A S/H circuit and input output waveforms

In order to understand the operation of this circuit let's assume that all initial voltages are set to zero and that the switch and amplifier are both ideal. When the CLK signal transitions high the input is connected to C_1 capacitor and the output is equal to v_{in}. When the CLK signal transitions low the input signal is said to be sampled and held on the capacitors. The time it takes the output to reach its final value is referred to as the settling time. F-2 gives a zoomed in view of the settling time.



F-2 Visual depiction of the sample and holds output settling time and resolution.

After the output has reached its final value another sample can occur. The settling time and CLK frequency can be related as:

$$f_{CLK} = \frac{1}{t_s} = \frac{1}{5\mu s} = 200MHz$$

If the output only reaches 1% of its final value it is said to have an accuracy of 1% and is related to the resolution (number of quantization levels) as:

$$1\% = \frac{1}{2^N}$$

Where N is the number of bits of the ADC. Solving for N above gives the resolution as:

$$N = \frac{\log(100)}{\log(2)} \approx 6.6$$

In this case we state that the S/H ADC has approximately 6.6 bits of resolution.

Adam Johnson

28.5 A digitally programmable signal generator uses a 14-bit DAC with a 10-volt reference to generate a DC output voltage. What is the smallest incremental change at the output that can occur? What is the DAC's full-scale value? What is its accuracy?

The smallest incremental change is simply 1 LSB of the DAC. From Eq. (28.9),

$$1\ LSB = \frac{V_{REF}}{2^N} = \frac{10V}{2^{14}} = 0.61mV$$

The full scale value of the DAC is when the digital input is 11 1111 1111 1111b. From Eq. (28.8), we get

$$V_{FS} = \frac{2^{N-1} \cdot V_{REF}}{2^N} = \frac{16383 \cdot 10V}{16384} = 9.99939V$$

As a double-check, it should also be V_{REF} – 1 LSB, which checks out to be 9.99939V.

For an ideal DAC used over the full V_{REF} range, the accuracy is simply the resolution divided by V_{REF}. From Eq. (28.10)

$$\frac{0.61mV}{10V} = 0.006\%$$

Justin Wood

28.6 Determine the maximum DNL (in LSBs) for a 3-bit DAC, which has the following characteristics. Does the DAC have 3-bit accuracy? If not, what is the resolution of the DAC having this characteristic?

Digital Input	Voltage Output
000	0 V
001	0.625 V
010	1.5625 V
011	2.0 V
100	2.5 V
101	3.125 V
110	3.4375 V
111	4.375 V

Differential Nonlinearity (DNL) is defined as

DNL_n = Actual increment height of transition *n* - Ideal increment height

The ideal increment height is 1 LSB, assuming V_{REF} = 5V:

$$1LSB = \frac{V_{REF}}{2^N} = \frac{5}{8} = 0.625V$$

$DNL_{1\text{-}7}$ expressed in LSBs would then be

$$DNL_1 = \left((0.625V - 0V) * \frac{1LSB}{0.625V} \right) - 1LSB = 0LSB$$

$$DNL_2 = \left((1.5625V - 0.625V) * \frac{1LSB}{0.625V} \right) - 1LSB = 0.5LSB$$

$$DNL_3 = \left((2.0V - 1.5625V) * \frac{1LSB}{0.625V} \right) - 1LSB = -0.3LSB$$

$$DNL_4 = \left((2.5V - 2.0V) * \frac{1LSB}{0.625V} \right) - 1LSB = -0.2LSB$$

$$DNL_5 = \left((3.125V - 2.5V) * \frac{1LSB}{0.625V} \right) - 1LSB = 0LSB$$

$$DNL_6 = \left((3.4375V - 3.125V) * \frac{1LSB}{0.625V} \right) - 1LSB = -0.5LSB$$

$$DNL_7 = \left((4.375V - 3.4375V) * \frac{1LSB}{0.625V} \right) - 1LSB = 0.5LSB$$

The maximum DNL is 0.5 LSB or 0.3125V.

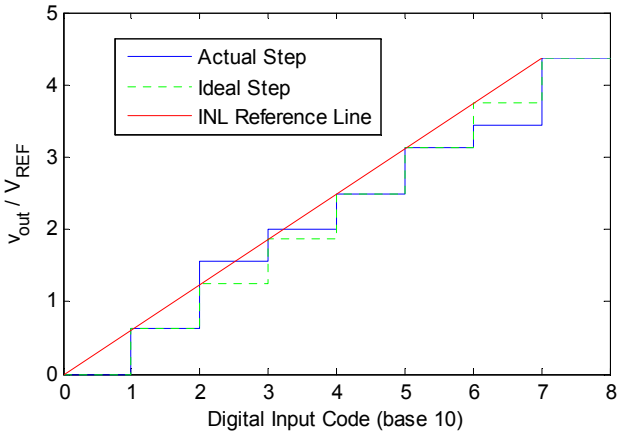
In general, for a DAC to have N-bit accuracy, the DAC must have less than +/- 0.5 LSB of DNL. Because we are within +/- 0.5 LSBs, the DAC is 3-bit accurate.

28.7 Repeat problem 28.6 calculating the INL (in LSB's). 28.6 states: Determine the maximum DNL (in LSBs) for a 3-bit DAC, which has the following characteristics. Does the DAC have 3-bit accuracy? If not, what is the resolution of the DAC having this characteristic?

Digital Input	Voltage Output (V)
000	0
001	0.625
010	1.5625
011	2
100	2.5
101	3.125
110	3.4375
111	4.375

Matlab

```
% Analog HW 6.  Problem 28.7.
x = [0 1 2 3 4 5 6 7 8];
y = [0 0.625 1.5625 2 2.5 3.125 3.4375 4.375 4.375];
stairs(x,y);
hold on;
y_ideal = 5.*[0 1/8 2/8 3/8 4/8 5/8 6/8 7/8 7/8];
stairs(x,y_ideal,'g:');
xline = [0 7];
yline = [0 4.375];
plot(xline,yline, 'r');
xlabel('Digital Input Code (base 10)'), ylabel('v_{out} / V_{REF}');
legend('Actual Step', 'Ideal Step', 'INL Reference Line');
```



We can see from the plot that the INL Reference Line follows the ideal stair steps. The maximum magnitude INL is at 010 (2 on plot) and at 110 (6 on plot) where the actual analog output is 0.3125 above the line and 0.3125 below the line, respectively. These INLs convert to $\pm\frac{1}{2}LSB$ after dividing by $V_{REF}/8$ (1LSB).

For N=3 bits the accuracy is $1/2^N = 0.125$, or 12.5%. The worst case INL is off by 0.3125. This is 0.3125/5 = 6.25%. *Yes, this DAC has 3-bit accuracy*. By similar method, the worst INL is ½ LSB and 3-bit accuracy is 1LSB, so yes, it has 3-bit accuracy.

Sakkarapani Balagopal

(28.8)A DAC has a reference voltage of 1,000V, and its maximum INL measures 2.5mV. What is the maximum resolution of the converter assuming that all the other characteristics of the converter are ideal?

It is common practice to assume that a converter with N-bit resolution will have less than ±0.5LSB of INL and DNL. The value of 0.5LSB in volts is simply given by equation 28.8-1.

$$0.5LSB = \frac{V_{ref}}{2^{N+1}} \tag{28.8-1}$$

From the problem statement, 0.5 LSB can be written as follow.

$$0.5LSB = 2.5mV = \frac{1000V}{2^{N+1}}$$

$$N = \frac{\log\left(\frac{1000V}{2.5mV}\right)}{\log(2)} - 1$$

$$N = 17.6bit$$

Since we cannot use a non-integer number of resolution, the resolution is equal to18bit.

28.9 Determine the INL and DNL for a DAC that has a transfer curve shown in Fig. 28.33.

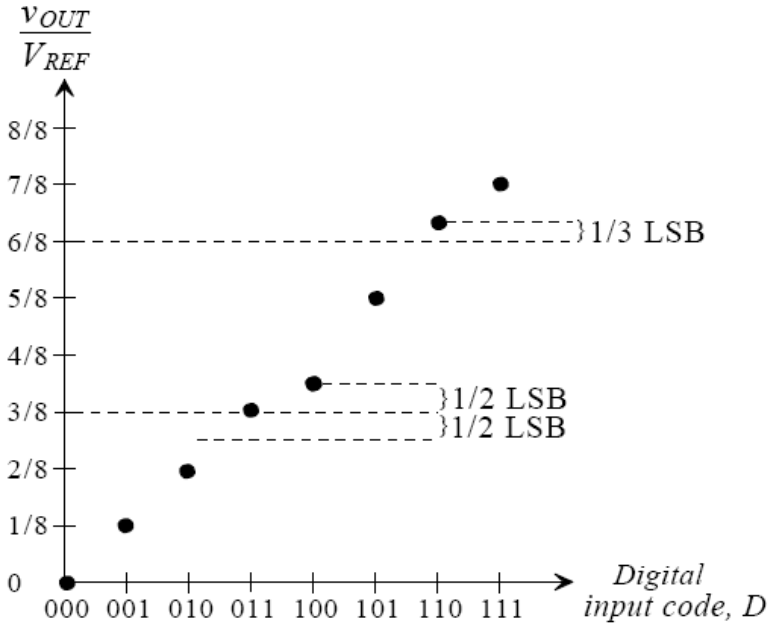
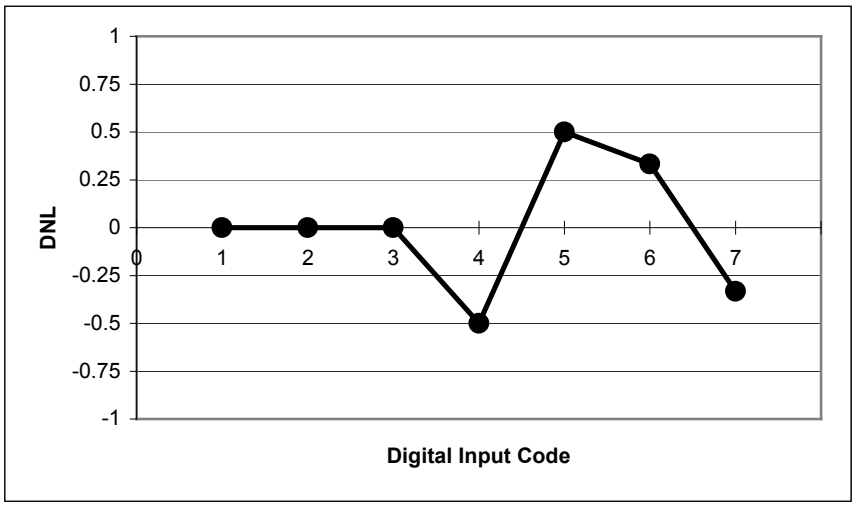


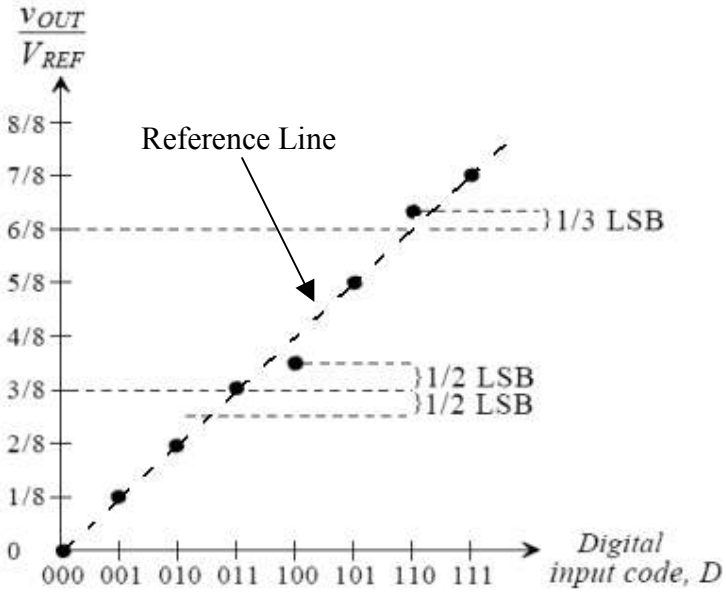
Figure 28.33 Transfer curves for Problem 28.9.

***DNL$_n$* = Actual increment height of transition *n* – Ideal increment height**
The ideal increment height is 1 LSB.

$DNL_1 = 1\text{ LSB} - 1\text{ LSB} = 0$
$DNL_2 = 1\text{ LSB} - 1\text{ LSB} = 0$
$DNL_3 = 1\text{ LSB} - 1\text{ LSB} = 0$
$DNL_4 = \frac{1}{2}\text{ LSB} - 1\text{ LSB} = -\frac{1}{2}\text{ LSB}$
$DNL_5 = 1\frac{1}{2}\text{ LSB} - 1\text{ LSB} = \frac{1}{2}\text{ LSB}$
$DNL_6 = 1\frac{1}{3}\text{ LSB} - 1\text{ LSB} = \frac{1}{3}\text{ LSB}$
$DNL_7 = \frac{2}{3}\text{ LSB} - 1\text{ LSB} = -\frac{1}{3}\text{ LSB}$

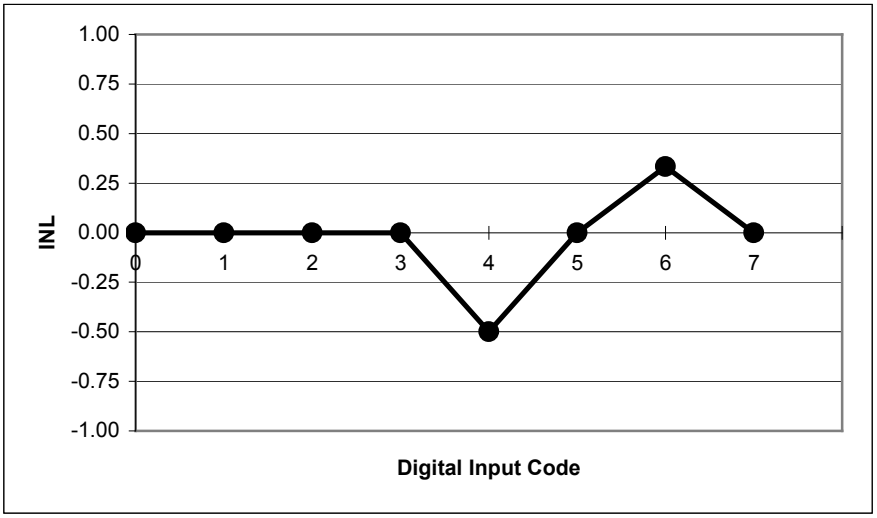


***INLn* = Output value for input code *n* – Output value of the reference line at that point**



It is clear from the figure above that the only deviations from the reference line are for input code 4 and input code 6.

$INL_0 = 0$
$INL_1 = 0$
$INL_2 = 0$
$INL_3 = 0$
$INL_4 = -\frac{1}{2}$ LSB
$INL_5 = 0$
$INL_6 = \frac{1}{3}$ LSB
$INL_7 = 0$



28.10 *A DAC has a full-scale voltage of 4.97 V using a 5 V reference, and its minimum output voltage is limited by the value of one LSB. Determine the resolution and dynamic range of the converter.*

In order to understand the full-scale voltage of a digital to analog converter we have to review the transfer curve seen in Figure 28.10.

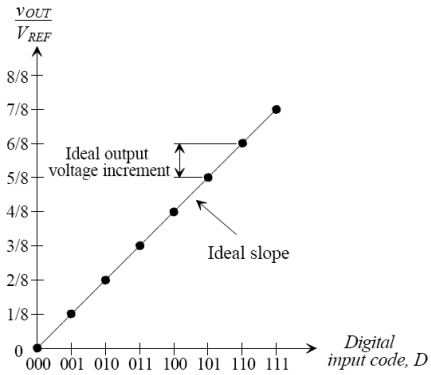


Figure 28.10 Ideal transfer curve for a 3-bit DAC.

Notice that the digital code of all zeros (000) is associated with the zero state. This means that the maximum code will only reach 1 LSB below the maximum value (counting starts at 0, not 1). The maximum output voltage is one LSB below the reference voltage:

$$1LSB = \frac{V_{REF}}{2^N} = V_{REF} - V_{FS}$$

$$2^N = \frac{V_{REF}}{V_{REF} - V_{FS}}$$

$$N = \frac{\log\left(\frac{V_{REF}}{V_{REF} - V_{FS}}\right)}{\log(2)} = 7.4$$

The DAC has a resolution of 7.4 bits.

The dynamic range (DR) of a data converter is defined as value of the maximum output signal divided by the smallest output signal. This relates directly to the number of bits (quantization levels) in the data converter by:

$$DR = 20\log\left(\frac{4.97V}{30mV}\right) = 20\log\left(\frac{2^N - 1}{1}\right) = 44.4dB$$

28.11 Prove that the RMS value of the quantization noise shown in Fig. 28.20b is as stated in Eq. (28.25).

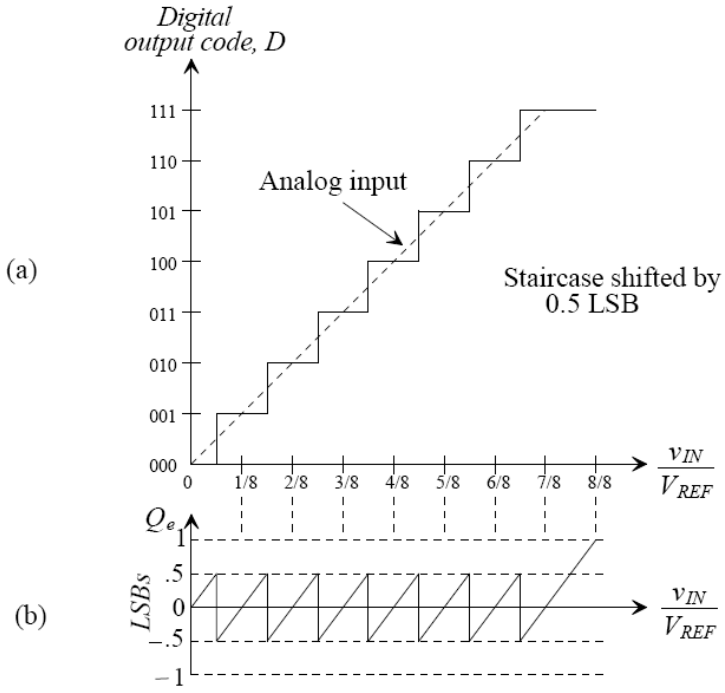
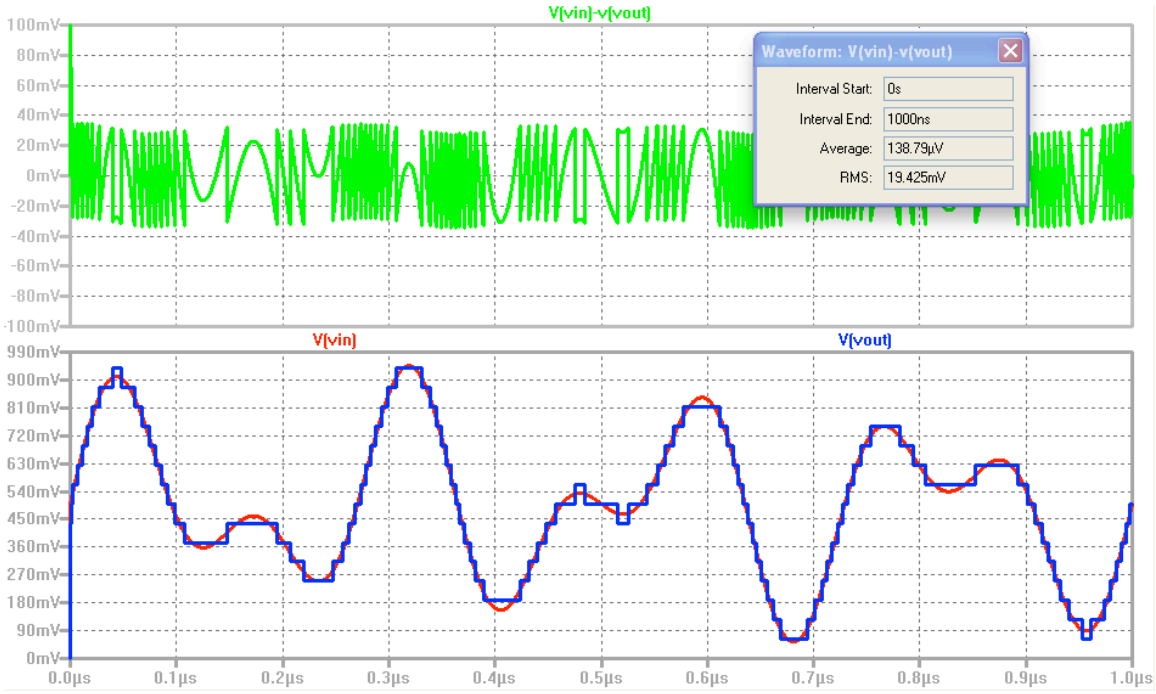


Figure 28.20 (a) Transfer curve for an ideal 3-bit ADC with (b) quantization error centered about zero.

Eq. (28.25) states the RMS noise to be

$$Q_{e,RMS} = \sqrt{\frac{1}{V_{LSB}} \int_{-0.5V_{LSB}}^{0.5V_{LSB}} (V_{LSB})^2 dV_{LSB}} = \frac{V_{LSB}}{\sqrt{12}}$$

So, the RMS value for the noise for a 4-bit ADC with a 1V VREF would be 18.0 mV. An LTSpice simulation of a complex sine wave input with an ideal 4-bit ADC/DAC yields a comparable 19.4mV.


V(vin)-v(vout)
100mV
80mV
60mV
40mV
20mV
0mV
-20mV
-40mV
-60mV
-80mV
-100mV
Waveform: V(vin)-v(vout)
Interval Start: 0s
Interval End: 1000ns
Average: 138.79µV
RMS: 19.425mV
V(vin)
V(vout)
990mV
900mV
810mV
720mV
630mV
540mV
450mV
360mV
270mV
180mV
90mV
0mV
0.0µs
0.1µs
0.2µs
0.3µs
0.4µs
0.5µs
0.6µs
0.7µs
0.8µs
0.9µs
1.0µs

Justin Wood

28.12 An ADC has a stated SNR of 94dB. Determine the effective number of bits of resolution of the converter.

From equation 28.27,

$$SNR = 6.02N + 1.76$$

$$N = \frac{94 - 1.76}{6.02} = 15.3$$

The effective number of bits of resolution is 15.

Lincoln Bollschweiler

28.13 Discuss the methods used to prevent aliasing and the advantages and disadvantages of each.

One way to prevent aliasing is to sample the signal at a higher frequency. *Advantages:* able to keep desired higher frequency signal information that otherwise might need to be filtered out, better resolution, and likely better accuracy. *Disadvantages:* more power to run the faster clock, larger layout to handle the added bits in the tighter resolution, more accuracy needed (better analog components), wide-band (high f) noise is included.

Another way to prevent aliasing is to set the pre-sampling low-pass filter to a lower cutoff frequency. *Advantages:* eliminate any unknown higher order frequency components or noise that could be aliased into the desired signal range, the lower the input frequency range bound compared to the sampling frequency makes the reconstruction filter (post DAC) easier (cheaper) to implement. *Disadvantages:* may sacrifice wanted higher frequency signal information, adds delay to the overall conversion.

Chapter 28

Problem 28.1

The quantization levels needed is

$$M = \frac{150°C - (-50°C)}{0.1°C} = \underline{2000}$$

Assume the resolution of ADC is N.

$$2^N = 2000 \Longrightarrow N = 10.9$$

$\therefore$ A <u>11-bit</u> ADC is required.

Problem 28.2

The frequency of $15°\sin(0.01 \times 2\pi t)$ is 0.01 Hz. According to Nyquist criterion, the mininum sampling frequency is $F_{sampling} = 2F_{max} = 0.02$ Hz, that is, the sampling rate required is <u>0.02 sample/sec.</u>

Problem 28.3

For a 16-bit ADC, $1\,LSB = \frac{Vref}{2^N} = \frac{5V}{2^{16}} \approx 76.3\,\mu V.$

$\therefore$ The maximum droop allowed is $\frac{1}{2}LSB \approx \underline{38.1\,\mu V.}$

Problem 28.4

Assume ADC is ideal, the maximum speed is

$$\frac{1}{5\mu s} = 0.2 \times 10^6 = \underline{200\,kHz}$$

Problem 28.4 (cont.)

Since the resolution of the S/H circuit is 1%, the maximum resolution of the ADC, N, is given by

$$\frac{1}{2^N} = 1\% \Rightarrow N = 6.64 \approx \underline{\underline{7}}$$

Problem 28.5

The smallest incremental change at output is

$$1LSB = \frac{V_{REF}}{2^N} = \frac{10v}{2^{14}} \approx \underline{\underline{0.61mV}}$$

The DAC's full-scale value is

$$V_{FS} = \frac{2^N - 1}{2^N} V_{REF} = \frac{2^{14} - 1}{2^{14}} \times 10V \approx \underline{\underline{9.9994\ V}}$$

The accuracy is

$$\frac{1}{2^N} = \frac{1}{2^{14}} = \underline{\underline{6.1 \times 10^{-5}}}$$

28.6

Digital Input	Voltage Output(V)	Actual Step height(V)	Ideal Step height(V)	DN
000	0			
001	0.625	0.625	0.625	0
010	1.5625	0.9375	"	0.31
011	2.0	0.4375	"	-0.18
100	2.5	0.5	"	-0.1
101	3.125	0.625	"	0
110	3.4375	0.3125	"	-0.3
111	4.375	0.9375	"	0.3

$|DNL|_{max} = 0.3125(V) = \boxed{0.5\ LSB}$ ← $1\ LSB = \frac{5}{2^3} = 0.625$

28.7

Digital Input	Actual Voltage Output (V)	Ideal Voltage Output(V)	INL(V)
000	0	0	0
001	0.625	0.625	0
010	1.5625	1.25	0.3125
011	2.0	1.875	0.125
100	2.5	2.5	0
101	3.125	3.125	0
110	3.4375	3.75	-0.3125
111	4.375	4.375	0

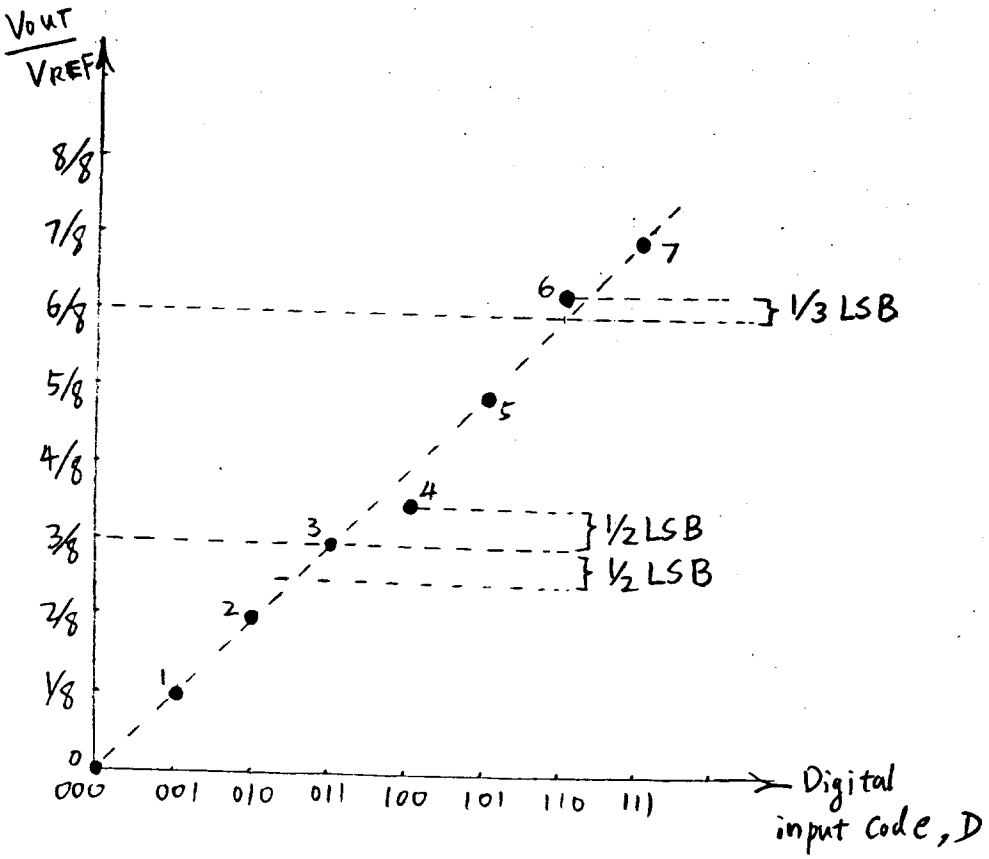
$|INL|_{max} = 0.3125(V) = \boxed{0.5 LSB}$

28.8

$$0.5\ LSB = \frac{V_{REF}}{2^{N+1}} = \frac{1000V}{2^{N+1}} = 2.5 \times 10^{-3}\ V$$

$$2^{N+1} = \frac{1000V}{2.5 \times 10^{-3}} = 400{,}000 \Rightarrow N = 18.$$

Problem 28.9



INL:

$INL0 = INL1 = INL2 = INL3 = INL5 = INL7 = 0$

$INL4 = -0.5\,LSB, \quad INL6 = +\frac{1}{3}\,LSB$

DNL:

$DNL1 = DNL2 = DNL3 = 0$

$DNL4 = \frac{1}{2}\,LSB - 1\,LSB = -\frac{1}{2}\,LSB$

$DNL5 = 1\frac{1}{2}\,LSB - 1\,LSB = +\frac{1}{2}\,LSB$

$DNL6 = 1\frac{1}{3}\,LSB - 1\,LSB = +\frac{1}{3}\,LSB$

$DNL7 = \frac{2}{3}\,LSB - 1\,LSB = -\frac{1}{3}\,LSB$

Problem 28.10

$$V_{FS} = \frac{2^N - 1}{2^N} V_{REF} \quad (\text{where } V_{REF} = 5V,\ V_{FS} = 4.97V)$$

$$\Longrightarrow N \approx 7.38$$

∴ The resolution of the DAC is 7. The dynamic range of the converter is:

$$DR = 20 \log \left(\frac{2^N - 1}{1} \right) dB = 20 \log \left(\frac{2^7 - 1}{1} \right) dB$$

$$\simeq \underline{\underline{42 dB.}}$$

28.11

$$V_{FS} = \frac{2^N - 1}{2^N} V_{REF} = \left(1 - \frac{1}{2^N}\right) V_{REF}$$

$$N = - \frac{\ln\left(1 - \frac{V_{FS}}{V_{REF}}\right)}{\ln 2} = - \frac{\ln(1 - 4.97/5)}{\ln 2}$$

$$= 7.3808$$

The converter resolution is $\boxed{N = 7}$

The converter dynamic range is

$$DR = 20 \text{Log} \left(\frac{2^N - 1}{1} \right) dB$$

$$\doteq \boxed{42.08 dB}$$

Problem 28.12

The SNR of an ADC is given by

$$SNR = 6.02N + 1.76 = 94 \text{ (dB)}$$

$$\Rightarrow N = 15.3$$

∴ The effective number of bits of resolution of the converter is 15.

Problem 28.13

There are two ways to eliminate aliasing: sampling at higher frequencies or filtering the analog signal before sampling. From theory, sampling at the frequency at least two times the highest frequency contained in signal will essencially eliminate the aliasing. The problem is that in practice some noise signals are wide-band, which makes this method practical impossible and costly. It is good practice to filter the analog signal to eliminate any unknown higher order harmonics or noise before sampling. However, simply filtering the input signal and the sampled signal will add delays to the overall conversion and increase the expense of the circuit. The best way is to use a combination of the two methods,