

Self-Biased PLL/DLL

ECG 721 – Memory Circuit Design (Spring 2017)

Dane Gentry

4/17/17

Outline

- Jitter
- Self-Biased PLL/DLL
- Differential Buffer Delay
- Fig. 19.57
- Bias Generator
- Self-Biased DLL
 - Input/Output Delay Relationship
 - **DLL Closed Loop Response**
 - **Bandwidth Tracking**
 - **Deriving ω_N/ω_{REF}**
 - Zero-Offset Charge Pump
- Self-Biased PLL
 - Input/Output Phase Relationship
 - **PLL Closed Loop Response**
 - **Bandwidth Tracking**
 - **Deriving ω_N/ω_{REF}**
 - **Feed-Forward Zero**
 - **Complete Self-Biased PLL**
- References

Jitter

- Jitter: the deviation from true periodicity of a presumably periodic signal, often in relation to a reference clock signal
- From CMOS: Circuit Design, Layout, and Simulation (pg. 591)
 - “Jitter, in the most general sense, for clock-recovery and synchronization circuits, can be defined as the amount of time the regenerated clock varies once the loop is locked.”

Jitter

- From CMOS: Circuit Design, Layout, and Simulation (pg. 591)

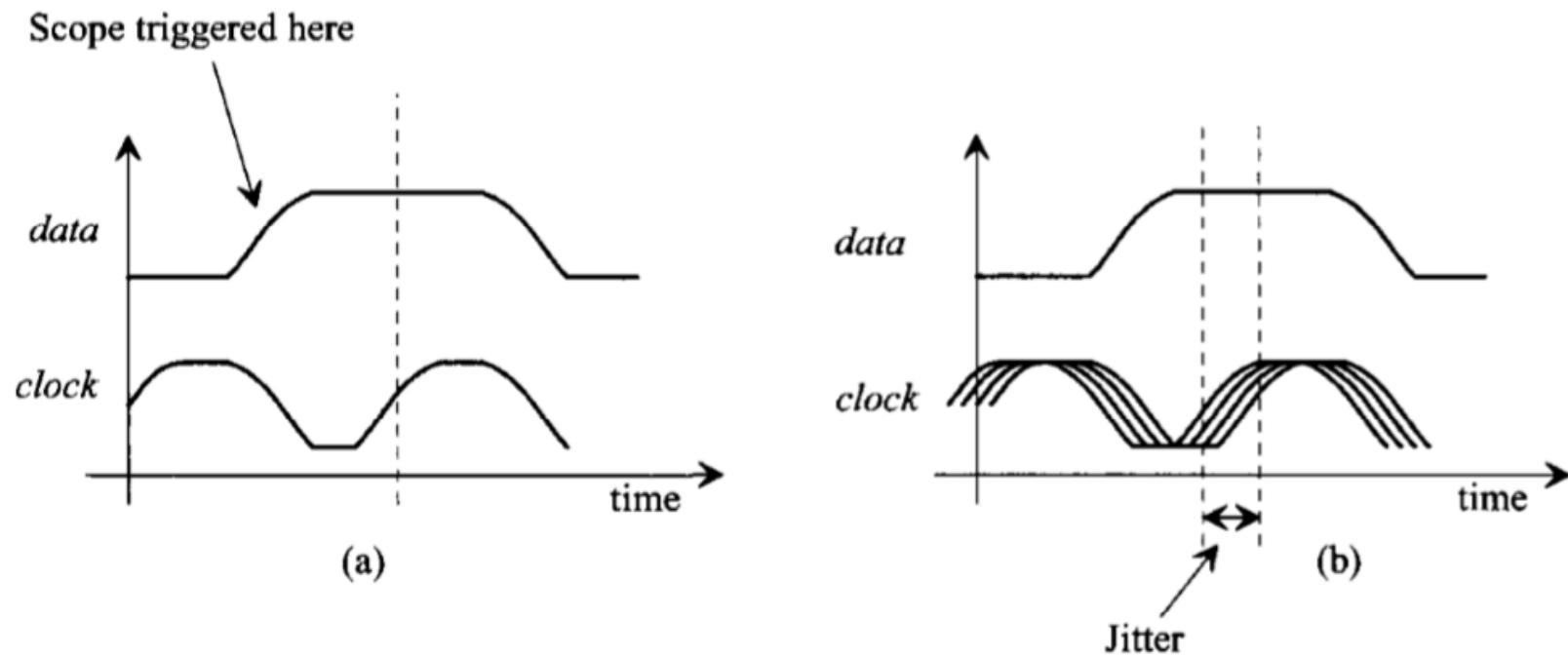


Figure 19.51 (a) Idealized view of clock and data without jitter and (b) with jitter.

Jitter

- From CMOS: Circuit Design, Layout, and Simulation (pg. 589)

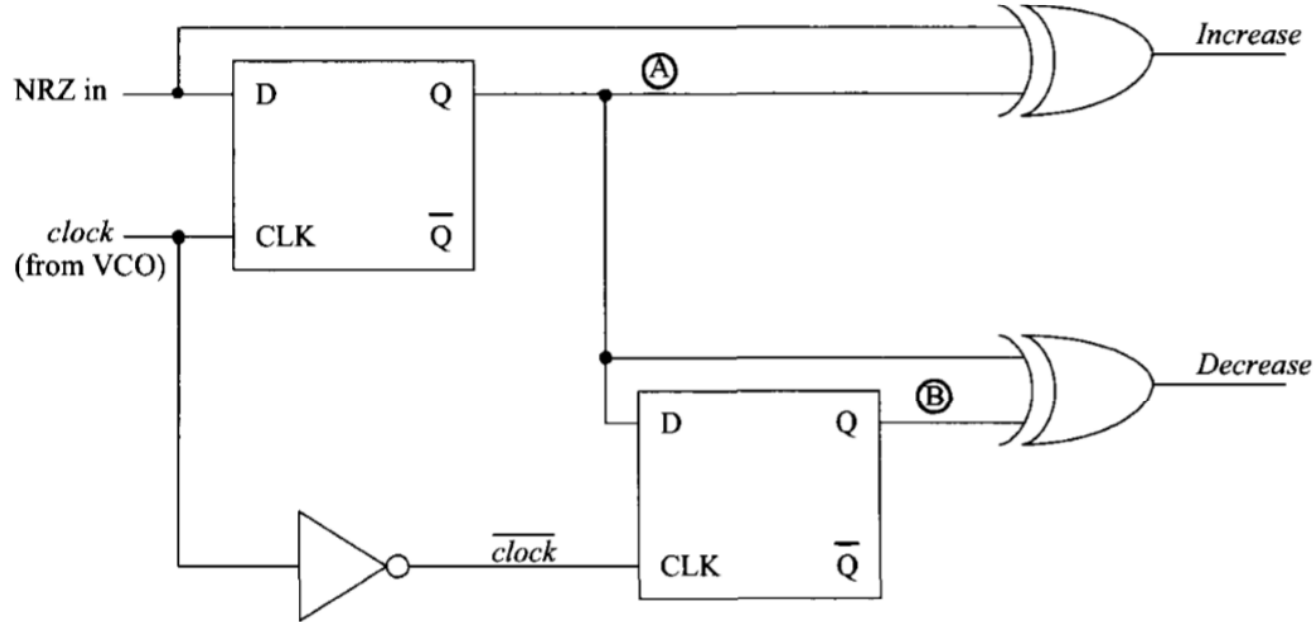


Figure 19.49 The PD (Hogge) portion of a self-correcting, clock-recovery circuit in lock.

Jitter

- From CMOS: Circuit Design, Layout, and Simulation (pg. 589)

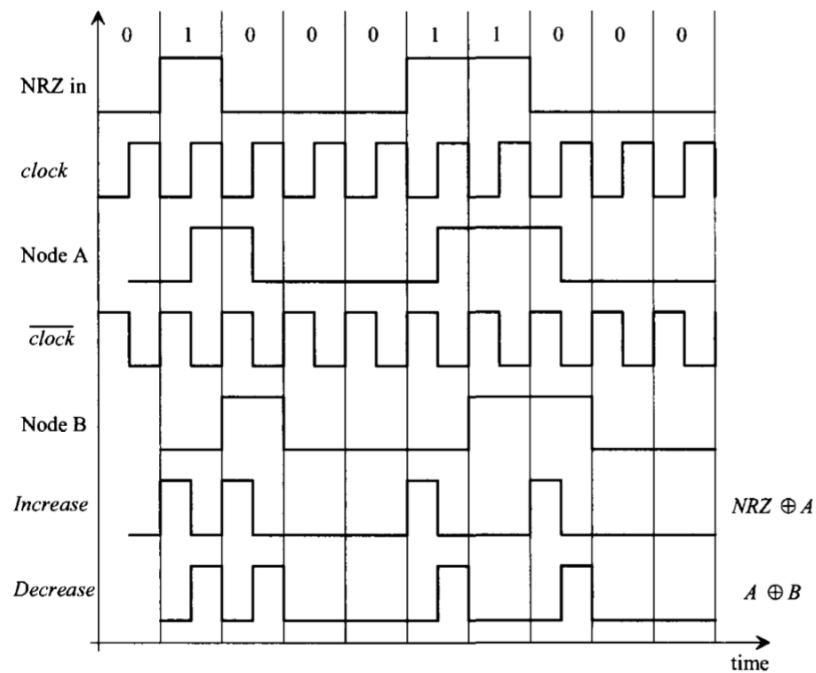


Figure 19.49 The PD (Hogge) portion of a self-correcting, clock-recovery circuit in lock.

Jitter

- From CMOS: Circuit Design, Layout, and Simulation (pg. 589)

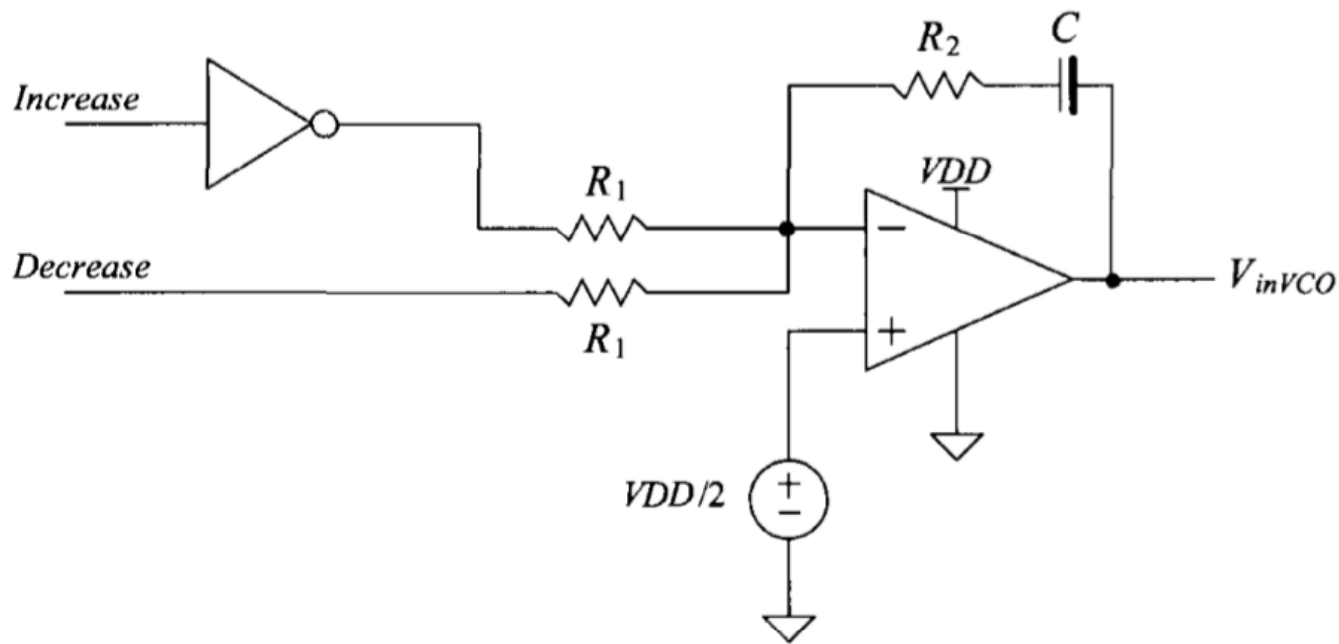


Figure 19.50 (a) Possible loop filter used in a self-correcting (Hogge) DPLL

Jitter

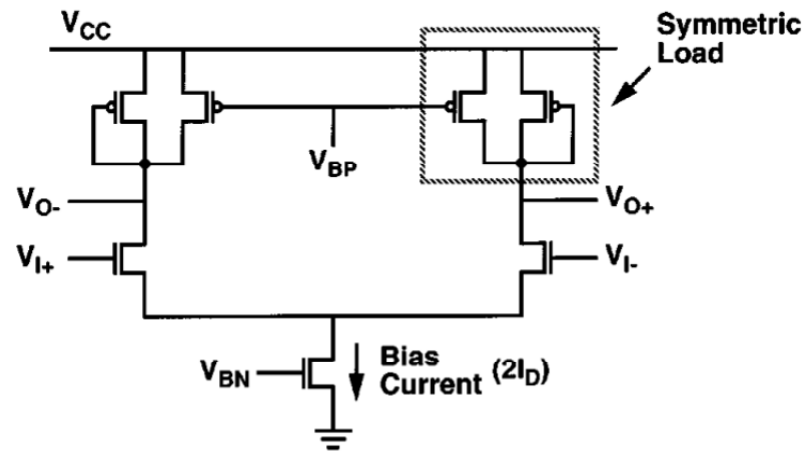
- Desire high speed data transmission (need fast clock)
- High clock frequency (f) in Hertz, Hz \rightarrow small clock period (T) in seconds, s
- Small jitter has more negative effect for small clock period
- Supply and substrate noise induced jitter

Self-Biased PLL/DLL

Self-biased DLL/PLL designs achieve:

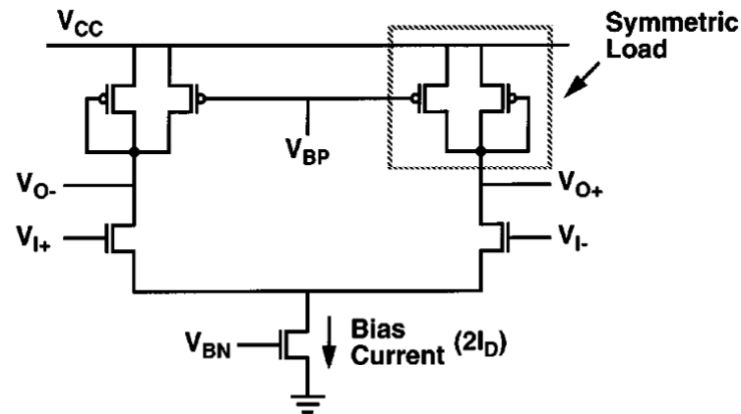
- Process technology and environmental variability independence
- Fixed damping factor (ζ)
- Fixed bandwidth to operating frequency ratio (ω_N/ω_{REF})
 - bandwidth = loop bandwidth = natural frequency (radians/second, rad/s) – ω_N
 - operating frequency (radians/second, rad/s) – ω_{REF}
- ω_N that tracks ω_{REF}
- Broad ω_{REF} range
- Low input tracking jitter / minimized supply and substrate noise induced jitter
- ζ and ω_N/ω_{REF} determined solely by ratio of capacitances (cap's)
- No external biasing (i.e. bandgap bias ckt)

Differential Buffer Delay



- Used in both PLL/DLL
- Contains source coupled pair w/ resistive load elements called symmetric loads
- Sym. loads consist of diode-connected PMOS in shunt w/ equally sized biased PMOS
- V_{CTRL} (loop filter output) generates NMOS/PMOS bias voltages (V_{BP}) and (V_{BN}), respectively
 - Defines lower voltage swing limit of buffer O/P's (V_{O+} swings VDD to V_{CTRL})

Differential Buffer Delay



- V_{BP} approximately equal to control I/P to the bias generator (V_{CTRL})
- NMOS current source dynamically biased w/ V_{BN} to compensate for drain and substrate volt. Variations
 - Provides high static supply and substrate noise rejection
- Buffer delay changes w/ V_{CTRL} since effective resistance of the load elements changes w/ V_{CTRL}

Differential Delay Element and Voltage-Controlled Resistor

- From CMOS: Circuit Design, Layout, and Simulation (pg. 596)

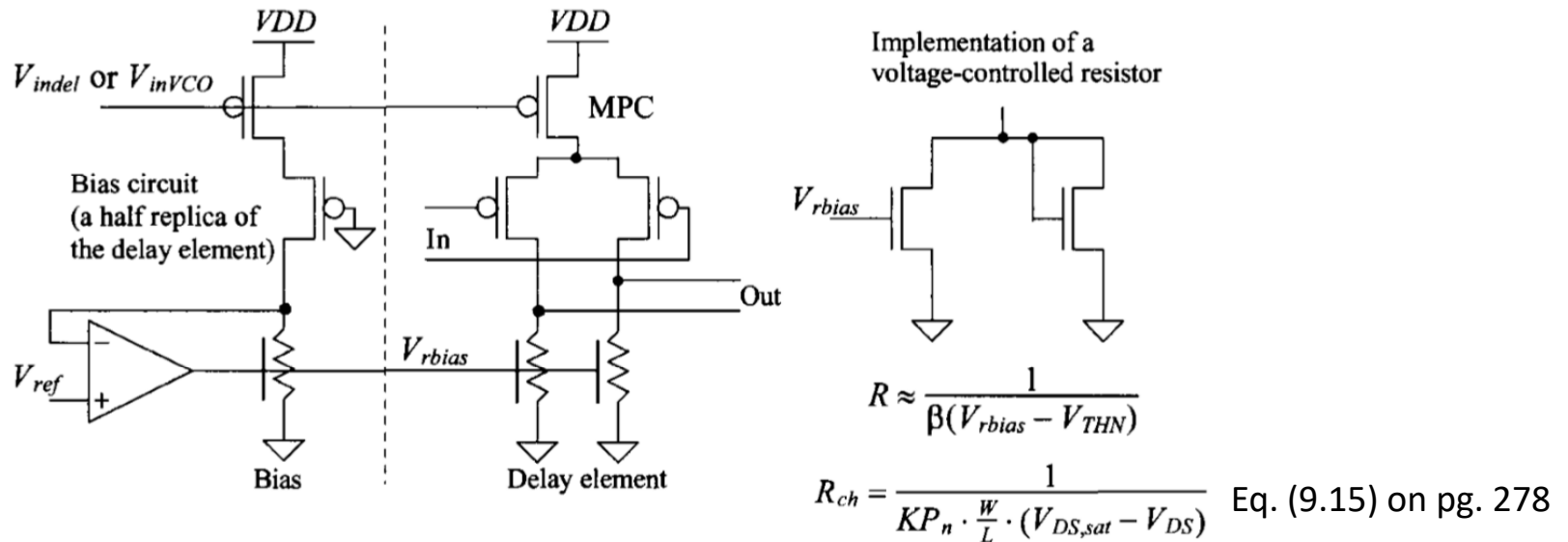
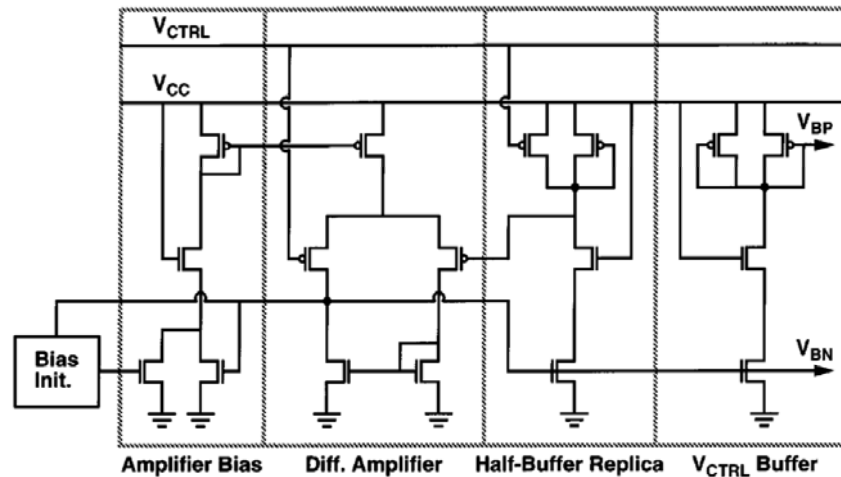


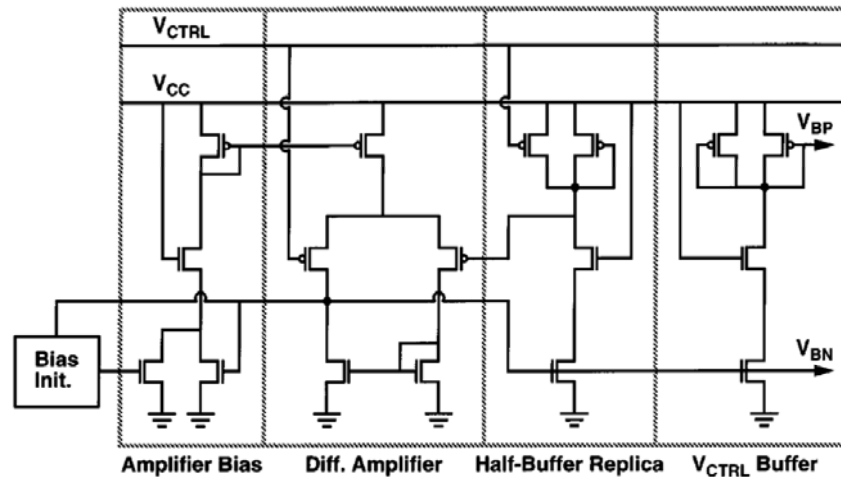
Figure 19.57 A differential delay element based on a voltage-controlled resistor. The bias circuit adjusts the value of the resistors used in the delay elements to sink the current sourced by the p-channel MOSFETs.

Bias Generator



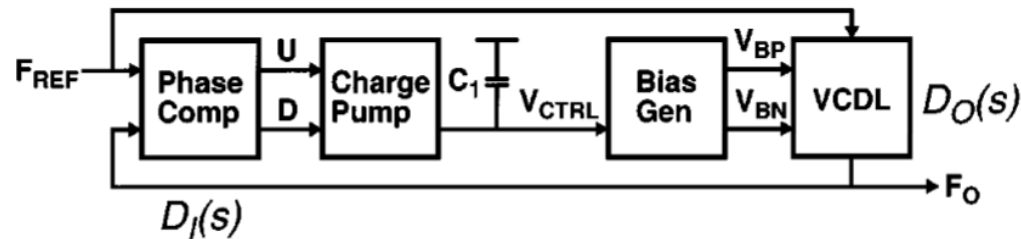
- V_{CTRL} (control I/P to bias generator) produces bias voltages V_{BN} and V_{BP}
- Bias generator continuously adjusts buffer bias current ($2I_D$) to provide correct lower swing limit (V_{CTRL}) for buffer stages
- Establishes constant current that is independent of supply volt. by using differential amplifier and half-buffer replica
- Amplifier adjusts V_{BN} so that O/P volt. of half-buffer replica is V_{CTRL} , the lower swing limit
- If supply volt. changes, amplifier will adjust to keep the swing and thus the bias current constant

Bias Generator



- Bias generator also provides buffered version of V_{CTRL} at V_{BP} O/P using additional half-buffer replica, isolating V_{CTRL} from potential capacitive coupling in buffer stages
- Compact layout since sym. load uses same size PMOS's
- Bias Initial circuit is self-bias reference aka start up circuit

Self-Biased DLL



- Neg. f/b in loop adjusts delay through VCDL by integrating phase error that results b/w the periodic reference I/P and the delay line O/P
- Once in lock, VCDL will delay reference I/P by fixed amount to form the O/P such that there is no detected phase error b/w the reference and the O/P
- VCDL delay must be a multiple of the reference I/P clock period

Input/Output Delay Relationship

$$D_O(s) = (D_I(s) - D_O(s)) \cdot F_{\text{REF}} \cdot \frac{I_{\text{CH}}}{sC_1} \cdot K_{\text{DL}}$$

- O/P delay - $D_o(s)$: delay b/w reference I/P and DLL O/P (established by VCDL)
- I/P delay - $D_i(s)$: delay to which the phase comparator compares the O/P delay
 - Phase difference for which phase comparator and charge pump generate no error signal
- Reference frequency (Hertz, Hz) - F_{REF}
- Charge pump current (Amps, A) - I_{CH}
- Loop filter capacitor (Farads, F) - C_1
- VCDL gain (seconds/Volt, s/V) - K_{DL}

DLL Closed Loop Response

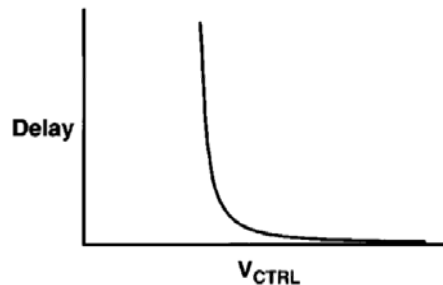
- DLL has a first-order closed loop response since loop filter integrates the phase error

$$\frac{D_O(s)}{D_I(s)} = \frac{1}{1 + s/\omega_N} \quad \omega_N = I_{CH} \cdot K_{DL} \cdot F_{REF} \cdot \frac{1}{C_1}$$

- ω_N will track ω_{REF} if I_{CH} and K_{DL} are constant
- However, I_{CH} , K_{DL} , and C_1 are process technology dependent and will cause ω_N to vary around the design target

Bandwidth Tracking

- Delay is nonlinear w/ respect to V_{CTRL} and changes proportionally to $1/(V_{CTRL} - V_T)$ w/ slope K_{DL} proportional to $1/(V_{CTRL} - V_T)^2$ or $1/I_D$



Typical symmetric load buffer stage delay as a function of control voltage

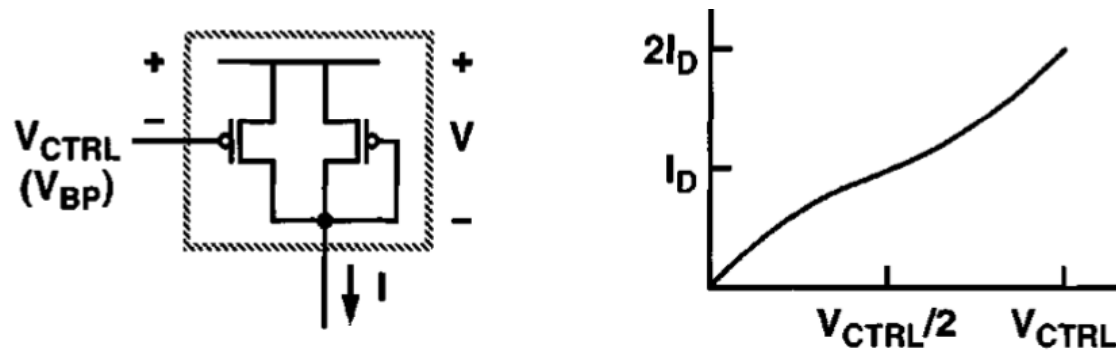
- Setting $I_{CH} = 2I_D$ eliminates K_{DL} dependence on $1/I_D$ which allows ω_N to track ω_{REF} without constraining ω_{REF} range

Deriving ω_N/ω_{REF}

$$t = R_{EFF} \cdot C_{EFF} = \frac{1}{g_m} \cdot C_{EFF}$$

- Buffer delay (seconds, s) – t
- Effective Resistance of sym. load (Ohms, Ω) – R_{EFF}
- Transconductance (Siemens, S OR mho, \mathcal{U}) – g_m
- Effective buffer O/P capacitance (Farads, F) – C_{EFF}

Deriving ω_N/ω_{REF}



- Using a half-buffer replica, the bias generator sets the buffer bias current equal to the current through a sym. load w/ its O/P volt. at V_{CTRL}
- In this case, the two equally sized PMOSs are both biased at V_{CTRL} and each source half of the buffer bias current

Deriving ω_N/ω_{REF}

- Drain current for one of the two equally sized PMOSs biased at V_{CTRL} :

$$I_D = \frac{k}{2} \cdot (V_{CTRL} - V_T)^2$$

where k is the device transconductance of one of the PMOS's

- Taking derivative w/ respect to V_{CTRL} :

$$g_m = k \cdot (V_{CTRL} - V_T) = \sqrt{2 \cdot k \cdot I_D}$$

Deriving ω_N/ω_{REF}

$$t = R_{EFF} \cdot C_{EFF} = \frac{1}{g_m} \cdot C_{EFF}$$

$$g_m = k \cdot (V_{CTRL} - V_T) = \sqrt{2 \cdot k \cdot I_D}$$

$$\rightarrow t = \frac{C_{EFF}}{k \cdot (V_{CTRL} - V_T)}$$

- Delay (D) for n stage VCDL:

$$D = n \cdot t = \frac{C_B}{2 \cdot k \cdot (V_{CTRL} - V_T)}$$

Total buffer output capacitance for all stages (Farads, F) – $C_B = 2 \cdot n \cdot C_{EFF}$

Deriving ω_N/ω_{REF}

- Delay (D) for n stage VCDDL:

$$D = n \cdot t = \frac{C_B}{2 \cdot k \cdot (V_{CTRL} - V_T)}$$

- Taking derivative with respect to V_{CTRL} :

$$\begin{aligned} K_{DL} &= \left| \frac{dD}{dV_{CTRL}} \right| = \frac{C_B}{2 \cdot k \cdot (V_{CTRL} - V_T)^2} \\ &= \frac{C_B}{4 \cdot I_D} \end{aligned}$$

- Gain inversely proportional to buffer bias current

Deriving ω_N/ω_{REF}

$$K_{DL} = \frac{C_B}{4 \cdot I_D}$$

- Let I_{CH} be set to some multiple x of the buffer bias current:

$$I_{CH} = x \cdot (2 \cdot I_D)$$

$$\begin{aligned} \rightarrow \frac{\omega_N}{\omega_{REF}} &= \frac{1}{\omega_{REF}} \cdot I_{CH} \cdot K_{DL} \cdot F_{REF} \cdot \frac{1}{C_1} \\ &= \frac{1}{2\pi} \cdot I_{CH} \cdot K_{DL} \cdot \frac{1}{C_1} \\ &= \frac{1}{2\pi} \cdot x \cdot (2 \cdot I_D) \cdot \frac{C_B}{4 \cdot I_D} \cdot \frac{1}{C_1} \\ &= \frac{x}{4\pi} \cdot \frac{C_B}{C_1} \end{aligned}$$

Deriving ω_N/ω_{REF}

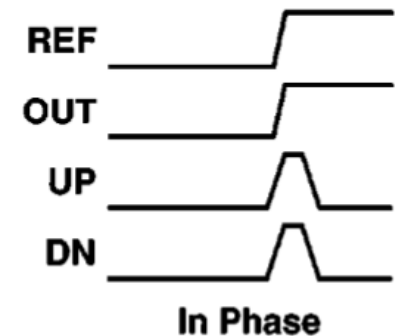
$$\frac{\omega_N}{\omega_{REF}} = \frac{x}{4\pi} \cdot \frac{C_B}{C_1}$$

- ω_N/ω_{REF} is constant and completely determined by a ratio of capacitances (C_B/C_1) that can be matched reasonably well in layout
- Dramatically reduces process technology sensitivity

Zero-Offset Charge Pump

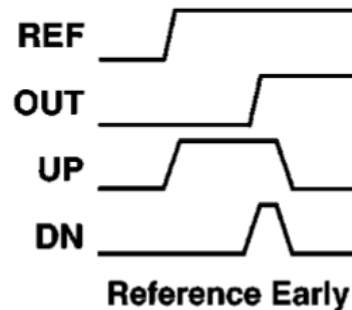
- Zero static phase offset, charge pump must transfer no net charge to the loop filter for equal duration UP and DN pulses
 - Requires UP and DN currents be identical and independent of the charge pump output voltage

- In-phase inputs:
 - Charge pump will see both UP and DN asserted for an equal and short period of time



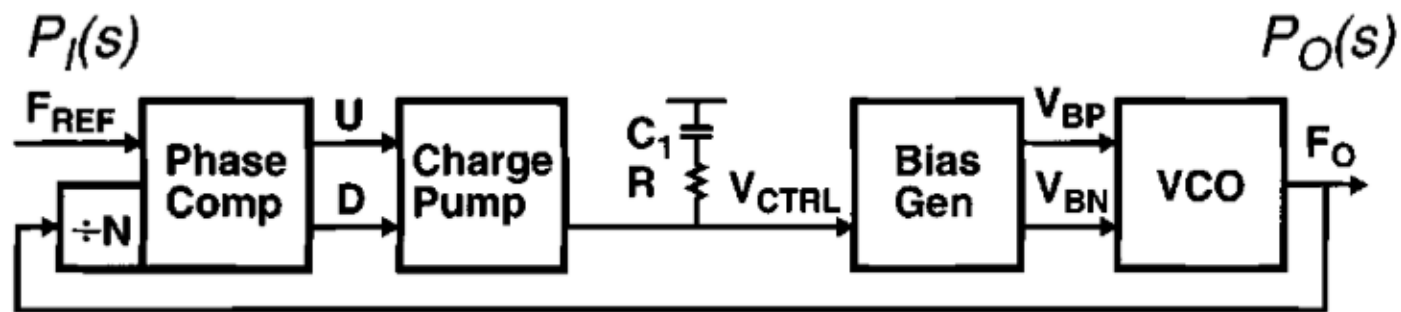
- If in-phase PFC inputs produce no UP or DN pulses, it will take some finite phase difference before a large enough pulse is produced to turn on the charge pump, i.e. dead zone

Zero-Offset Charge Pump



- If reference is early, difference b/w UP and DN pulses will be equal to I/P phase difference
- Self-biasing allows charge pump to have zero static phase offset when UP and DN are asserted for equal durations on every cycle w/ in-phase inputs
- By constructing charge pump from sym. load buffer stage, UP and DN currents for equal duration pulses completely cancel out and transfer no net charge to loop filter

Self-Biased PLL



- Res. used for stability

Input/Output Phase Relationship

- PLL has a second-order closed response b/c loop filter integrates the charge representing the phase error and the VCO integrates the O/P freq. to form the O/P phase

$$P_O(s) = \left(P_I(s) - \frac{P_O(s)}{N} \right) \cdot I_{CH} \cdot \left(R + \frac{1}{sC_1} \right) \cdot K_V \cdot \frac{1}{s}$$

- Output phase - $P_o(s)$
- Input phase – $P_i(s)$
- Charge pump current (Amps, A) - I_{CH}
- Loop filter resistor (Ohms, Ω) – R
- Loop filter capacitor (Farads, F) - C_1
- VCO gain (Hertz/Volt, Hz/V) – K_v

PLL Closed Loop Response

$$\frac{P_O(s)}{P_I(s)} = \left(\frac{1}{N} + \frac{s}{I_{CH} \cdot (R + 1/(sC_1)) \cdot K_V} \right)^{-1}$$

$$= \frac{N \cdot (1 + s \cdot C_1 \cdot R)}{1 + s \cdot C_1 \cdot R + s^2 / (I_{CH} / C_1 \cdot K_V / N)}$$

OR

$$\frac{P_O(s)}{P_I(s)} = N \cdot \frac{1 + 2 \cdot \zeta \cdot (s/\omega_N)}{1 + 2 \cdot \zeta \cdot (s/\omega_N) + (s/\omega_N)^2}$$

$$\zeta = \frac{1}{2} \cdot \sqrt{\frac{1}{N} \cdot I_{CH} \cdot K_V \cdot R^2 \cdot C_1}$$

where

$$\omega_N = \frac{2 \cdot \zeta}{R \cdot C_1}$$

- $\zeta = 1$: Critically damped
- $\zeta > 1$: Overdamped

Bandwidth Tracking

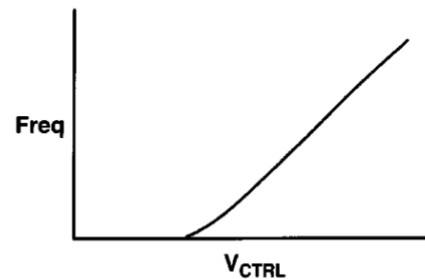
- I_{CH} , R , and K_V are constant for typical PLL \rightarrow const. ζ and ω_N
- Const. ω_N can constrain wide ω_{REF} range and low I/P tracking jitter
- Want ω_N as close to ω_{REF} as possible to minimize total phase error
 - However, ω_N must be a decade below the lowest ω_{REF} for stability
- Ideally, ζ and ω_N/ω_{REF} const. for improved jitter performance and no limit on ω_{REF} range

Bandwidth Tracking

- To keep ζ constant w/ ω_{REF} , I_{CH} can be set equal to buffer bias current ($2I_D$) and R can be set to vary inversely proportionally to the square root of the buffer bias current ($R \sim 1/\sqrt{2I_D}$)
 - $\rightarrow \zeta$ const., but ω_N will be proportional to square root of buffer bias current ($\omega_N \sim \sqrt{2I_D}$)
- For tracking bandwidth, VCO operating freq. should have same dependency on buffer bias current as ω_N

Bandwidth Tracking

- Sym. load buffer stages used to implement VCO to obtain a broad frequency range



Typical VCO frequency as a function of control voltage when implemented with symmetric load buffer stages

- Freq. proportional to $V_{CTRL} - V_T$ or, equivalently, the square root of I_D ($\sqrt{I_D}$) and slope const. slope
 - $\rightarrow K_V$ const. and ω_{REF} proportional to square root of buffer bias current ($\sqrt{2I_D}$)
- Both ω_N and ω_{REF} proportional to $\sqrt{2I_D}$
 - $\rightarrow \omega_N$ will track ω_{REF}

Deriving ω_N/ω_{REF}

- Oscillation freq. (F) of n-stage VCO:

- $F \sim \sqrt{2I_D}$

$$F = \frac{1}{2 \cdot n \cdot t} = \frac{k \cdot (V_{CTRL} - V_T)}{C_B} = \frac{\sqrt{2 \cdot k \cdot I_D}}{C_B}$$

- Taking derivative w/ respect to V_{CTRL} :

- Independent of buffer bias current

$$K_V = \left| \frac{dF}{dV_{CTRL}} \right| = \frac{k}{C_B}$$

- Let I_{CH} be set to some multiple x of the buffer bias current: $I_{CH} = x \cdot (2 \cdot I_D)$
- Let diode-connected sym. load in bias generator that establishes loop filter resistance be y times larger than sym. loads used in buffer stages

$$R = \frac{y}{2 \cdot g_m} = \frac{y}{\sqrt{8 \cdot k \cdot I_D}}$$

Deriving ω_N/ω_{REF}

$$K_V = \left| \frac{dF}{dV_{CTRL}} \right| = \frac{k}{C_B}$$

$$I_{CH} = x \cdot (2 \cdot I_D)$$

$$R = \frac{y}{2 \cdot g_m} = \frac{y}{\sqrt{8 \cdot k \cdot I_D}}$$

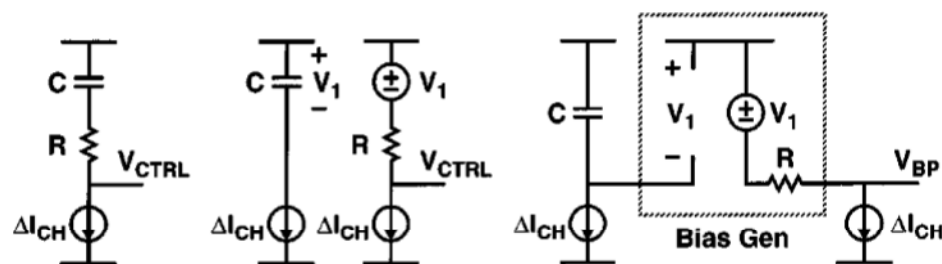
$$\begin{aligned} \zeta &= \frac{1}{2} \cdot \sqrt{\frac{1}{N} \cdot I_{CH} \cdot K_V \cdot R^2 \cdot C_1} \\ &= \frac{1}{2} \cdot \sqrt{\frac{1}{N} \cdot x \cdot (2 \cdot I_D) \cdot \frac{k}{C_B} \cdot \frac{y^2}{8 \cdot k \cdot I_D} \cdot C_1} \\ &= \frac{y}{4} \cdot \sqrt{\frac{x}{N}} \cdot \sqrt{\frac{C_1}{C_B}} \end{aligned}$$

$$\begin{aligned} \frac{\omega_N}{\omega_{REF}} &= \frac{1}{2\pi \cdot F_{REF}} \cdot \frac{2 \cdot \zeta}{R \cdot C_1} \\ &= \frac{1}{2\pi} \cdot \frac{N \cdot C_B}{\sqrt{2 \cdot k \cdot I_D}} \cdot \frac{y}{4} \cdot \sqrt{\frac{x}{N}} \cdot \sqrt{\frac{C_1}{C_B}} \\ &\quad \cdot \frac{\sqrt{8 \cdot k \cdot I_D}}{y} \cdot \frac{2}{C_1} \\ &= \frac{x \cdot N}{2\pi} \cdot \sqrt{\frac{C_B}{C_1}} \end{aligned}$$

- ζ and ω_N/ω_{REF} are both equal to a const. times square root of the ratio of two capacitances = $x \cdot \sqrt{C_1/C_B}$
- ω_N will track ω_{REF} and, therefore, sets no constraint on the operating frequency range

Feed-Forward Zero

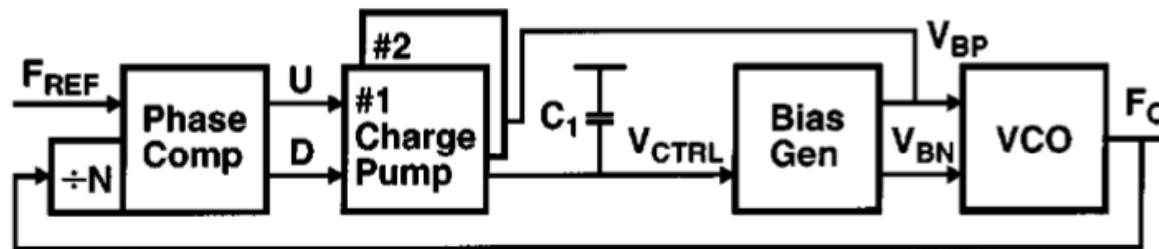
- Form res. (R) to vary proportionally to $1/\sqrt{2I_D}$ from small-signal resistance $1/g_m$ for diode-connected device
 - $\rightarrow (g_m \sim \sqrt{2I_D})$



Loop filter transformation for integration of loop filter res.

- V_{CTRL} typically sum of volt. drops across cap. and res.
- Volt. drops across cap. and res. generated separately
 - As long as same charge pump current is applied to each of them
- 2 volt. drops summed to form V_{CTRL} by replicating volt. across cap. w/ volt. source placed in series w/ res.
- Bias generator can implement this volt. source and res. since it buffers V_{CTRL} to form V_{BP} with a finite O/P resistance

Complete Self-Biased PLL



Complete self-biased PLL block diagram

- Res. formed by diode-connected sym. load or, equivalently, a diode-connected PMOS device as seen in Bias Generator
 - Resistance is equal to $1/g_m$ or inversely proportional to $\sqrt{2I_D}$
- Self-biased PLL completed by adding additional charge pump current to bias generator's O/P

References

- [1] Maneatis, John G., “Low-Jitter Process-Independent DLL and PLL Based On Self-Biased Techniques,” in IEEE Journal of Solid-State Circuits, Vol.33, No.11, Nov 1996.
- [2] Maneatis, John G., “Precise Delay Generation Using Coupled Oscillators,” in ProQuest Dissertations and Theses, 1994.
- [3] Baker, R. Jacob, “CMOS Circuit Design, Layout, and Simulation,” 3rd ed., Wiley-IEEE Press, 2010.

Questions???