Lecture 23 – eMMC Architecture and Operation

ECG 721 – Memory Circuit Design, Spring 2017

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Overview

- Flash memory programming and reading
- MultiMedia Card (MMC)
- Embedded MMC (eMMC)
- Packet Formats & Operation
- Future Technologies

Flash Memory Overview

Floating Gate Memory

ch16_16_3_p2_video

Delta Sigma Sensing Flash Memory

ch17_17_1_video

Programming Process

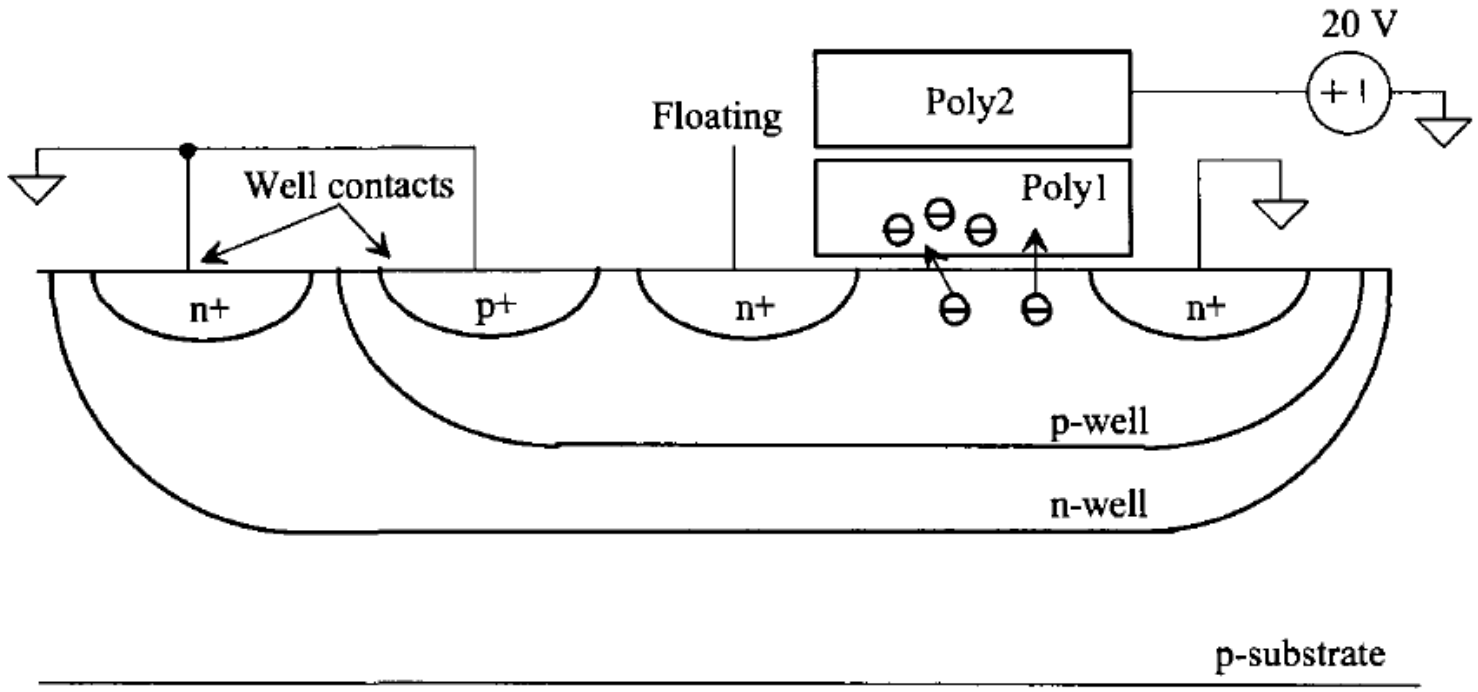


Figure 16.58 FNT of electrons from the p-well to a floating gate to increase threshold voltage (showing programming).

Source: CMOS Circuit Design Layout and Simulation Page 470

Cell Programming in NAND Architecture

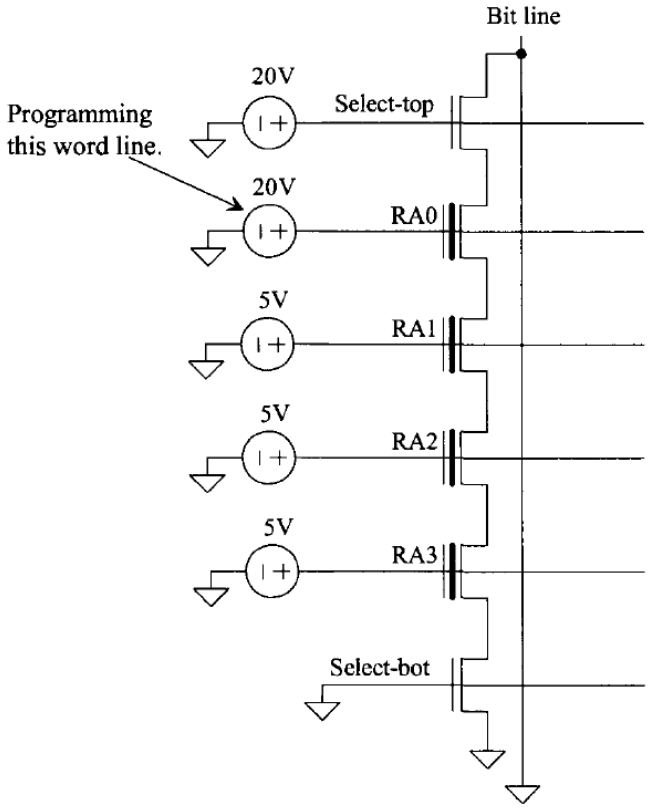


Figure 16.62 Programming in a Flash NAND cell.

Source: CMOS Circuit Design Layout and Simulation Page 472

Erasing Process

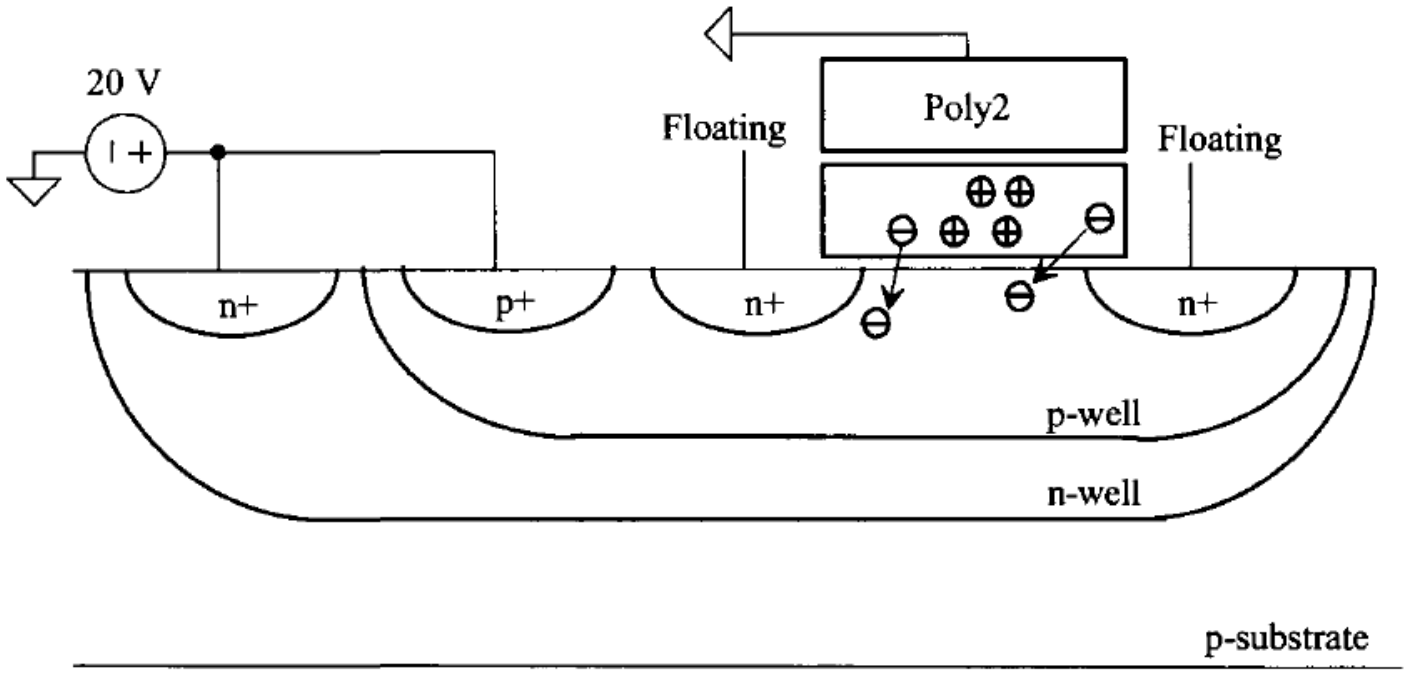


Figure 16.59 FNT of electrons from the floating gate to p-well to decrease threshold voltage (showing erasing).

Source: CMOS Circuit Design Layout and Simulation Page 470

Reading Process – Cell Properties

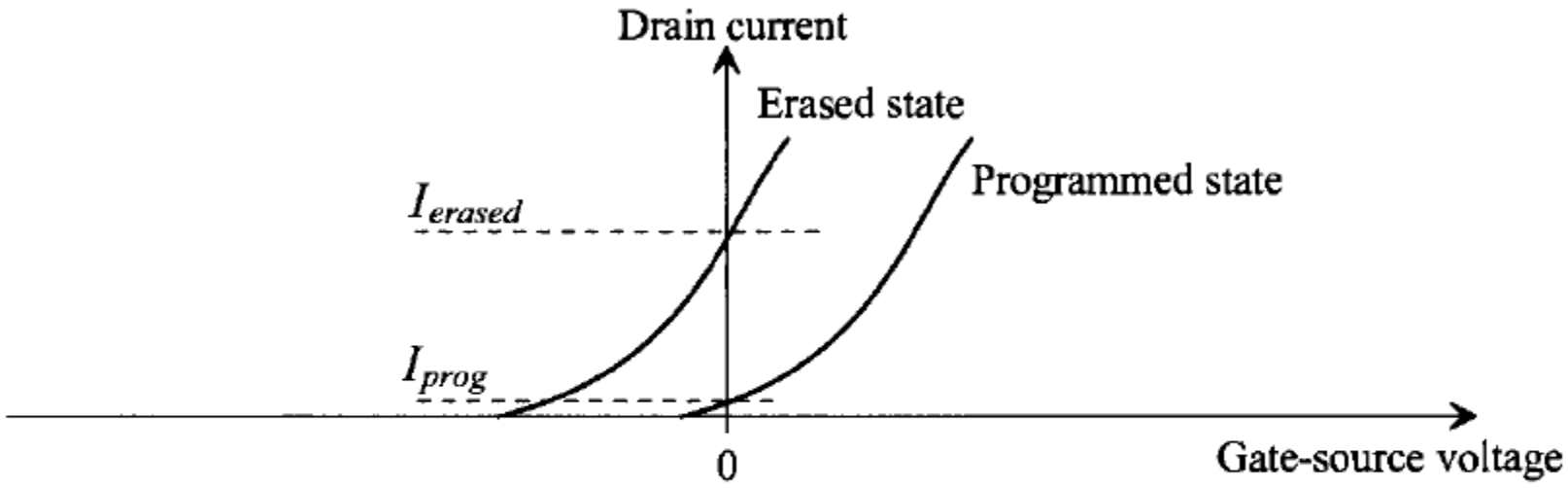


Figure 16.64 Expanded view showing erased and programmed IV curves.

Source: CMOS Circuit Design Layout and Simulation Page 471

Reading Process – Sensing

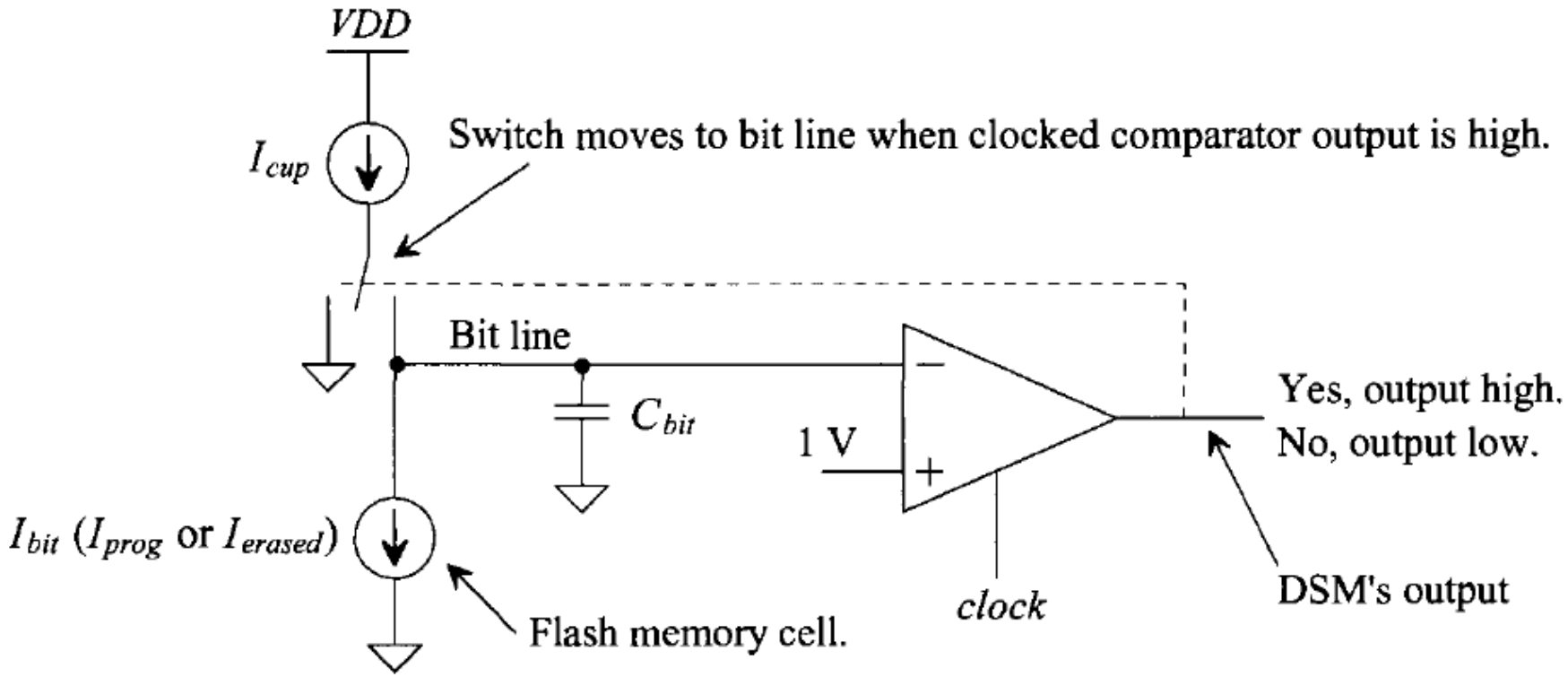


Figure 17.6 Sensing a Flash memory cell using DSM.

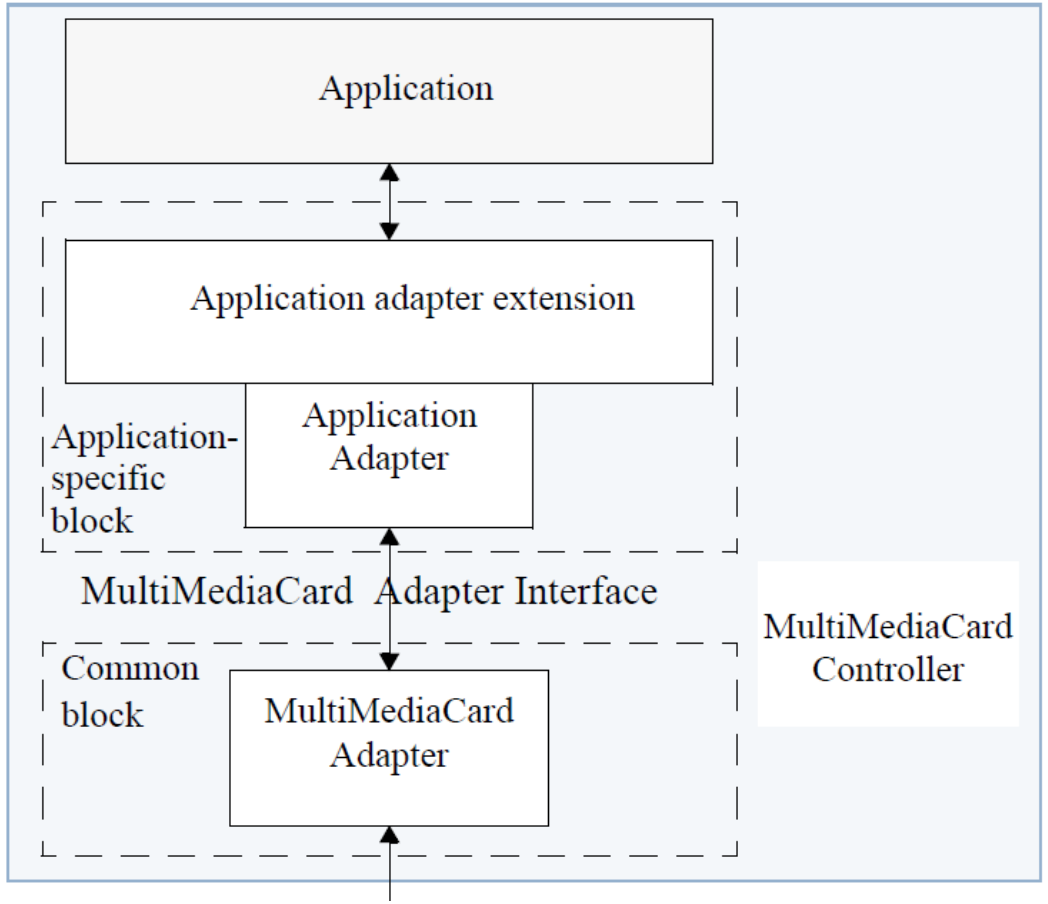
Source: CMOS Circuit Design Layout and Simulation Page 488

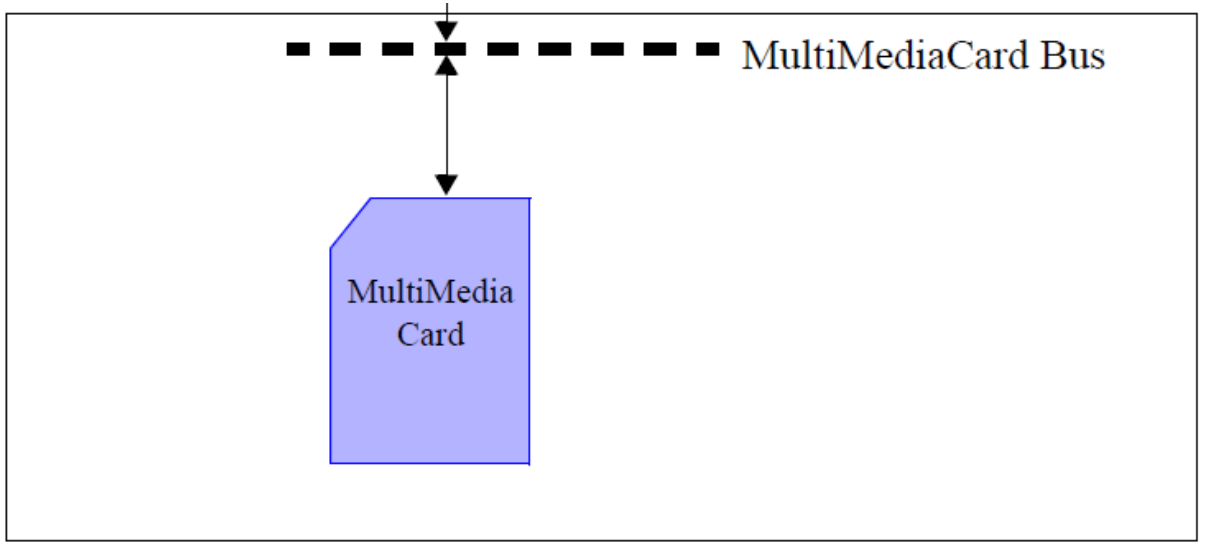
MultiMedia Card (MMC)

MMC Overview

- Developed by Joint Electron Device Engineering Council (JEDEC)
- **Standard** for flash memory
  - Low pin count
  - Cheap compared to large, high performance drives (also use NAND flash)
  - Portable, easily removed
  - Non-volatile
- SD is a **format** for flash memory

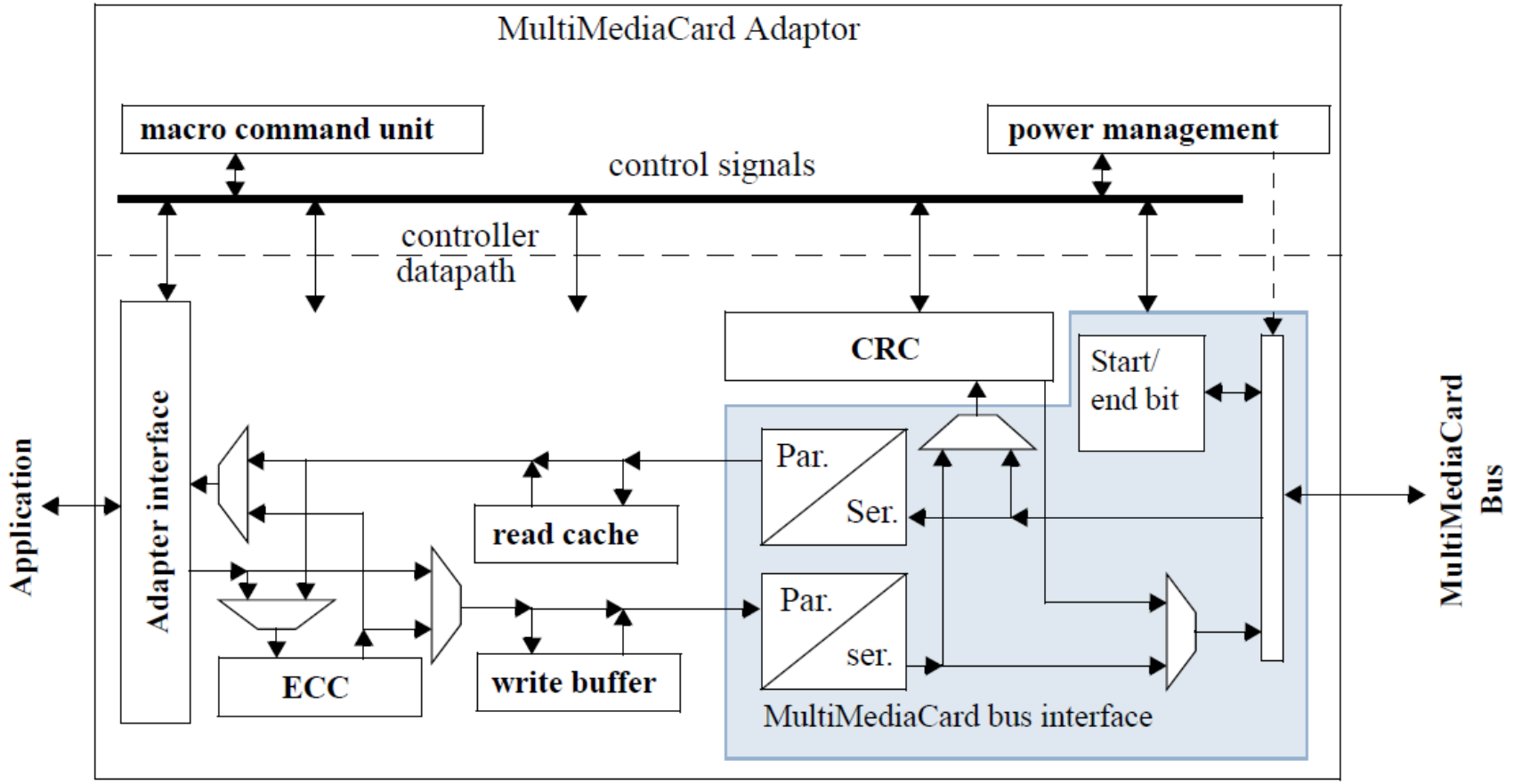
Typical MMC Application System Overview





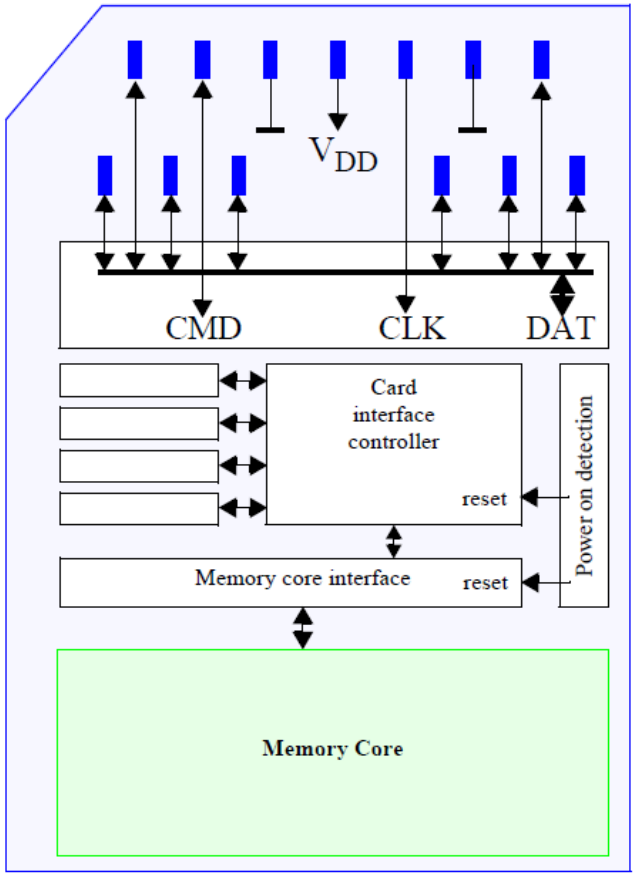
Source: JEDEC Standard No. 84-A441 Figure 3

MMC Adaptor Architecture



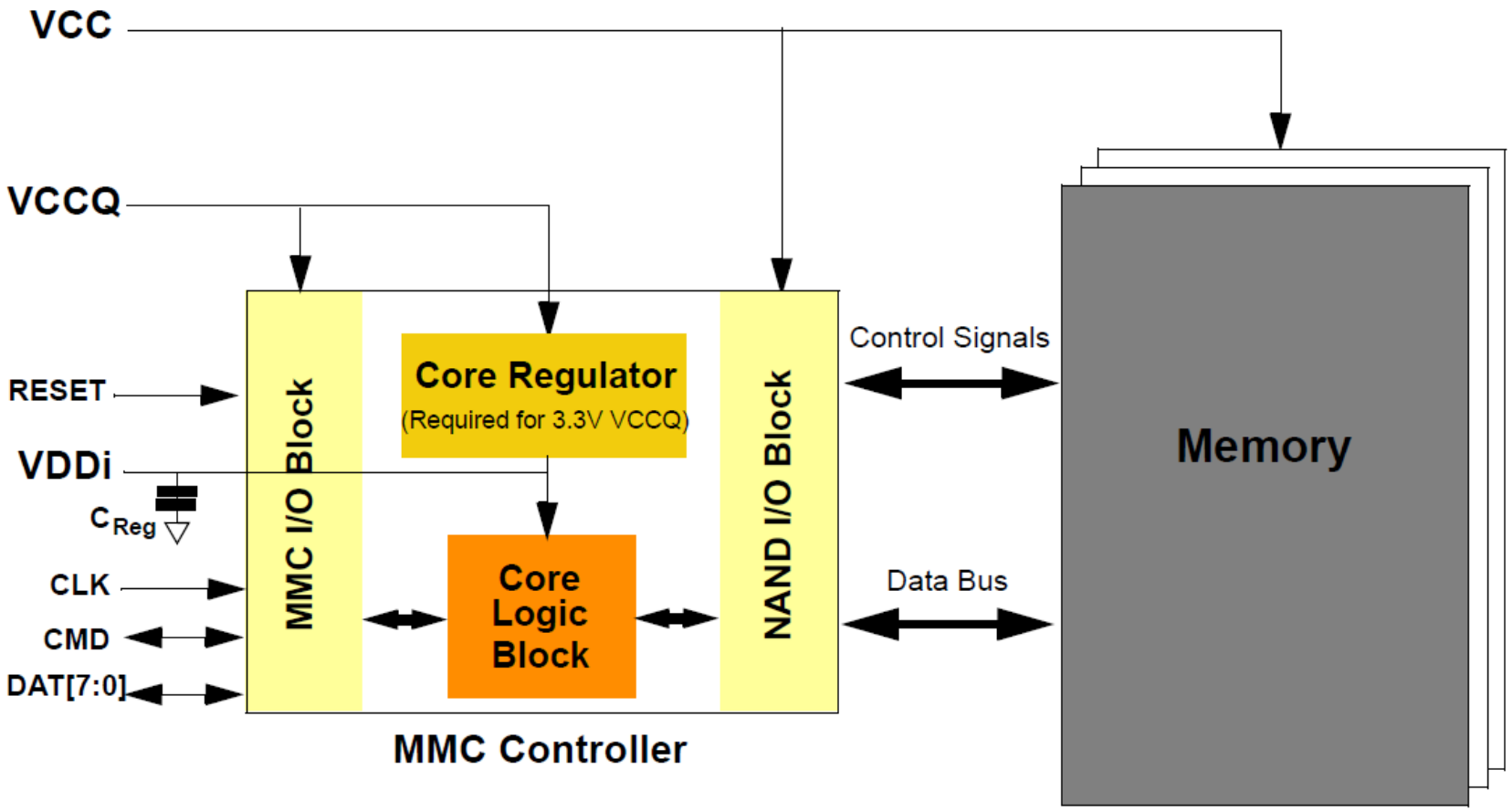
Source: JEDEC Standard No. 84-A441 Figure 16

MMC Architecture



Source: JEDEC Standard No. 84-A441 Figure 4

MMC Controller



Source: JEDEC Standard No. 84-A441 Figure 62

MMC Controller Power Supply Voltages

Parameter	Symbol	Min	Max	Unit
Supply voltage (NAND)	V_{CC}	2.7	3.6	V
		1.7	1.95	V
Supply voltage (I/O)	$V_{CC}Q$	2.7	3.6	V
		1.65	1.95	V
		1.1	1.3	V
Supply power-up for 3.3V	tPRUH		35	ms
Supply power-up for 1.8V	tPRUL		25	ms
Supply power-up for 1.2V	tPRUV		20	ms

Source: JEDEC Standard No. 84-A441 Table 106

Flash Translation Layer (FTL)

- Functions
  - Logical to physical address mapping
  - Power off recovery
  - Wear leveling (erase/write counts)
- RAM tables and Flash map storage
  - Dangerous for recovery
- FTL algorithms determine physical address
  - Block/Sector/Hybrid Mapping
  - Log Block Scheme

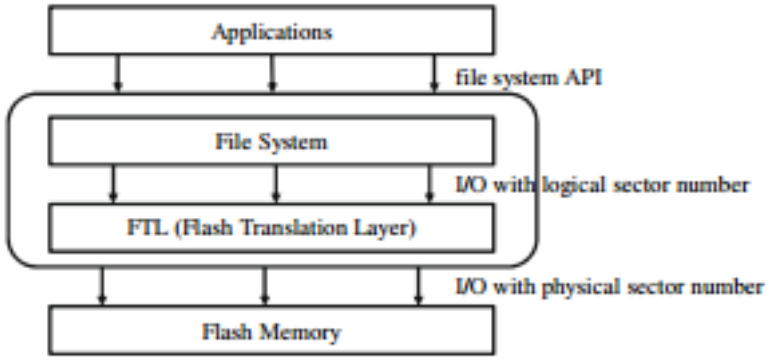
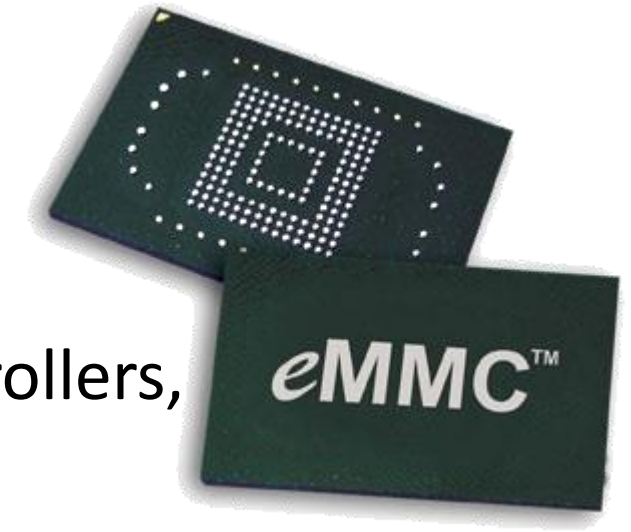


Fig. 1. Overall architecture of flash memory system.

Source: Chung et al. Figure 1

Embedded MultiMedia Card (eMMC)

eMMC Overview

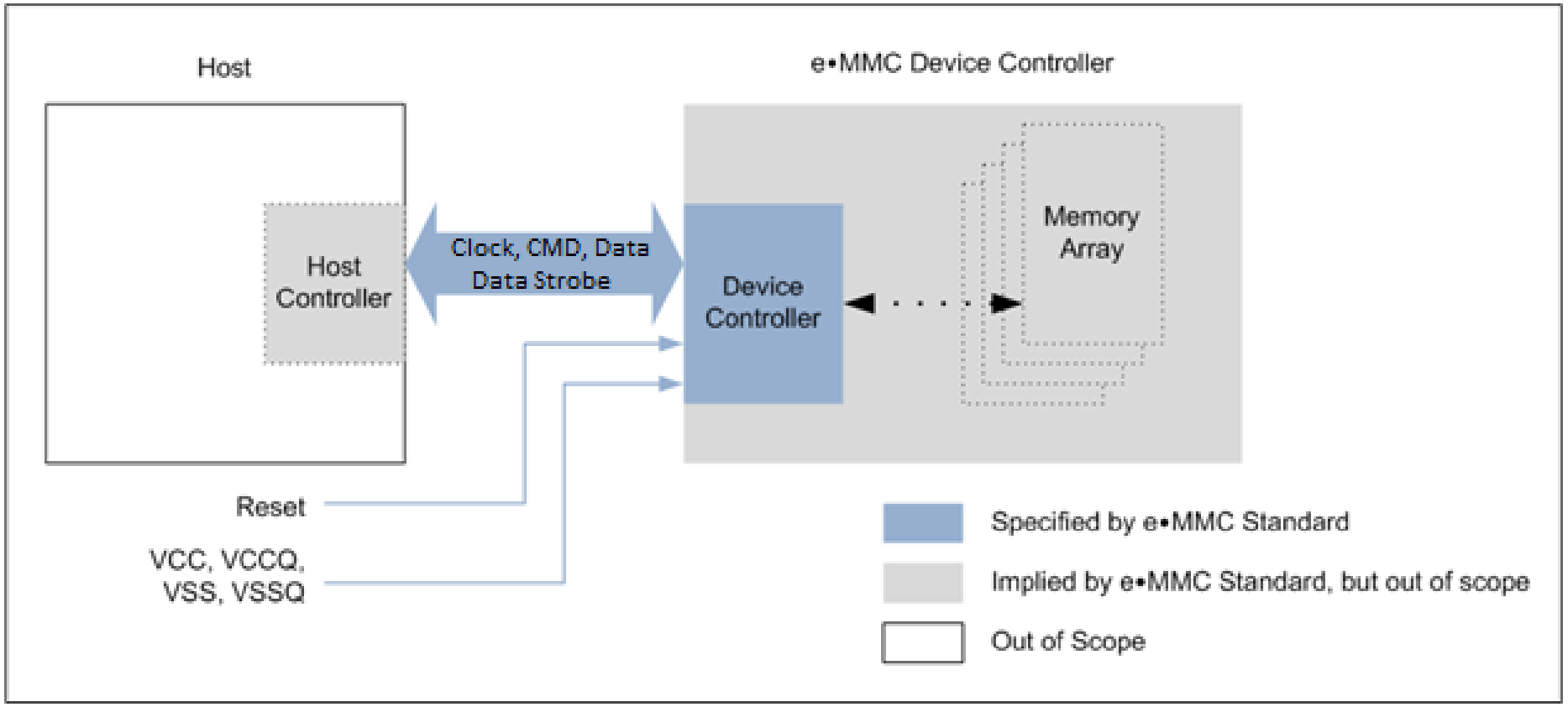


- Optimized for low power and small area
- Used in many mobile platforms: phones, microcontrollers,

- Combines the flash controller, interface adapter, and memory arrays together on the same Silicon dye
- NOT removable (perfect for OS/firmware)
- Very affordable, low tier performance

- Reset signal is unique to eMMC vs other MMC applications

eMMC System Overview



Source: JEDEC Standard No. 84-B51 Figure 1

Quick Definitions for Next Slides

- **open-drain**: A logical interface operation mode. An external resistor or current source is used to pull the interface level to HIGH, the internal transistor pushes it to LOW

- **push-pull:** A logical interface operation mode, a complementary pair of transistors is used to push the interface level to HIGH or LOW

Communication

Card state	Operation mode	Bus mode
Inactive State	Inactive mode	Open-drain
Pre-Idle State	Boot mode	
Pre-Boot State		
Idle State	Card identification mode	
Ready State		
Identification State		
Stand-by State	Data transfer mode	Push-pull
Sleep State		
Transfer State		
Bus-Test State		
Sending-data State		
Receive-data State		
Programming State		
Disconnect State		
Boot State	Boot mode	
Wait-IRQ State	Interrupt mode	Open-drain

Source: JEDEC Standard No. 84-A441 Table 5

11 Signal Bus

- CLK: 0-200MHz
- Data Strobe: output in DDR mode
  - Data output on rise and falling edges
  - CMD and CRC status is still on rising edge
- CMD
  - Bidirectional command channel
  - Open drain for initialization and push-pull for fast command transfer
- DAT[0-7]
  - Defaults to DAT[0] after boot
  - Larger bus widths are negotiated after bootup
    - Pull-ups disconnected when lines are in use

Load Capacitance

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

the sum of the host and bus capacitances not to exceed 20 pF

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100(1)	kΩ	to prevent bus floating
Pull-up resistance for DAT0–7	R_{DAT}	10		100(1)	kΩ	to prevent bus floating
Internal pull up resistance DAT1–DAT7	R_{int}	10		150	kΩ	to prevent unconnected lines floating
Bus signal line capacitance	C_L			30	pF	Single Device
Single Device capacitance	C_{DEVICE}			6	pF	
Maximum signal line inductance				16	nH	$f_{pp} \leq 52$ MHz
V_{DDi} capacitor value	C_{REG}(2)	0.1			uF	To stabilize regulator output when target device bus speed mode is either backward-compatible, high speed SDR, high speed DDR, or HS200.
		1			uF	To stabilize regulator output when target device bus speed mode is HS400.
V_{DDi2} capacitor value (e^2•MMC)	C_{REG2}	1			uF	To stabilize internal regulated voltage
V_{DDi3} capacitor value (e^2•MMC)	C_{REG3}	1			uF	To stabilize internal regulated voltage
V_{CCQ} decoupling capacitor	C_{H1}	1			uF	(3), (4), (5)

NOTE 1 Recommended maximum pull-up is 30 kΩ for 1.2 V and 50 kΩ for 1.8 V interface supply voltages. A 3 V part, may use the whole range up to 100 kΩ.
NOTE 2 Recommended value for C_{REG}, C_{REG2} and C_{REG3} might be different between *e*•MMC device vendors.
NOTE Confirm the maximum value and the accuracy of the capacitance with *e*•MMC vendor because the electrical characteristics of the regulator inside *e*•MMC is affected by the fluctuation of the capacitance.
NOTE 3 C_{H1} is V_{CCQ}-V_{SSQ} decoupling capacitor required for HS200&HS400 *e*•MMC device.
NOTE 4 C_{H1} should be placed adjacent to V_{CCQ}-V_{SSQ} balls (around DAT[7..0] balls), It should be located as close as possible to the balls defined in order to minimize connection parasitics.
NOTE 5 *e*•MMC device vendor may have more specific requirements for CH1 placement. Please confirm such requirements with specific *e*•MMC device vendor.

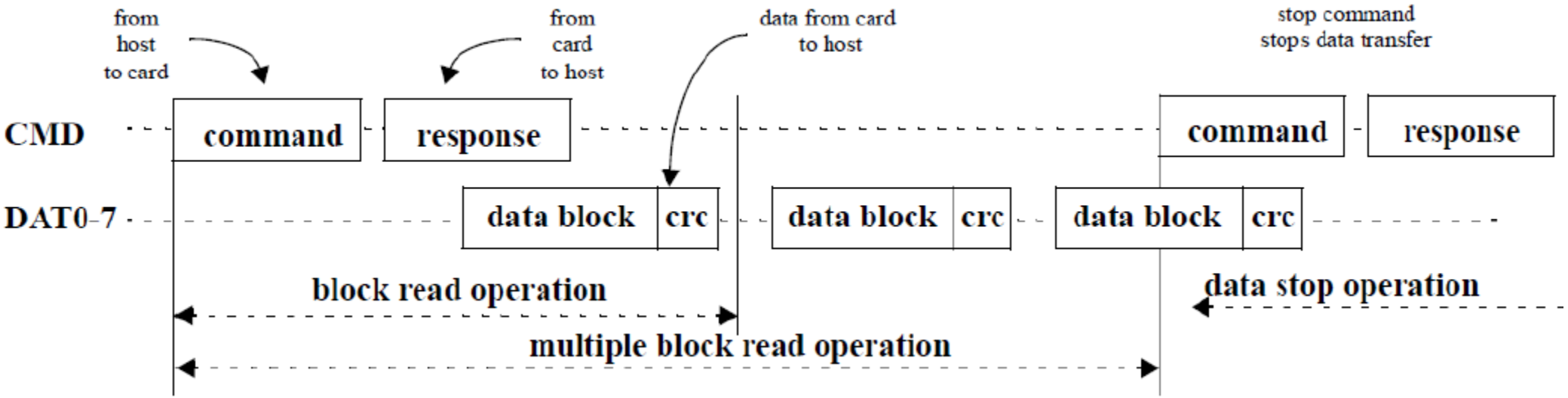
Source: JEDEC Standard No. 84-B51 Table 200 / Page 247

Address Spaces

- Mapped Host Address Space
  - Usable space by the host software
- Private Vendor Specific Address Space
  - Cannot be accessed by read command by host
  - Contains firmware and mapping tables for the controller
  - No host data
- Unmapped Host Address Space
  - Cannot be read by host
  - May contain old host data or copies
    - Reason why government does not like flash/SSD memory
- 32 bit addresses imply 2GB max unless multiple sectors are used (512B in size each)

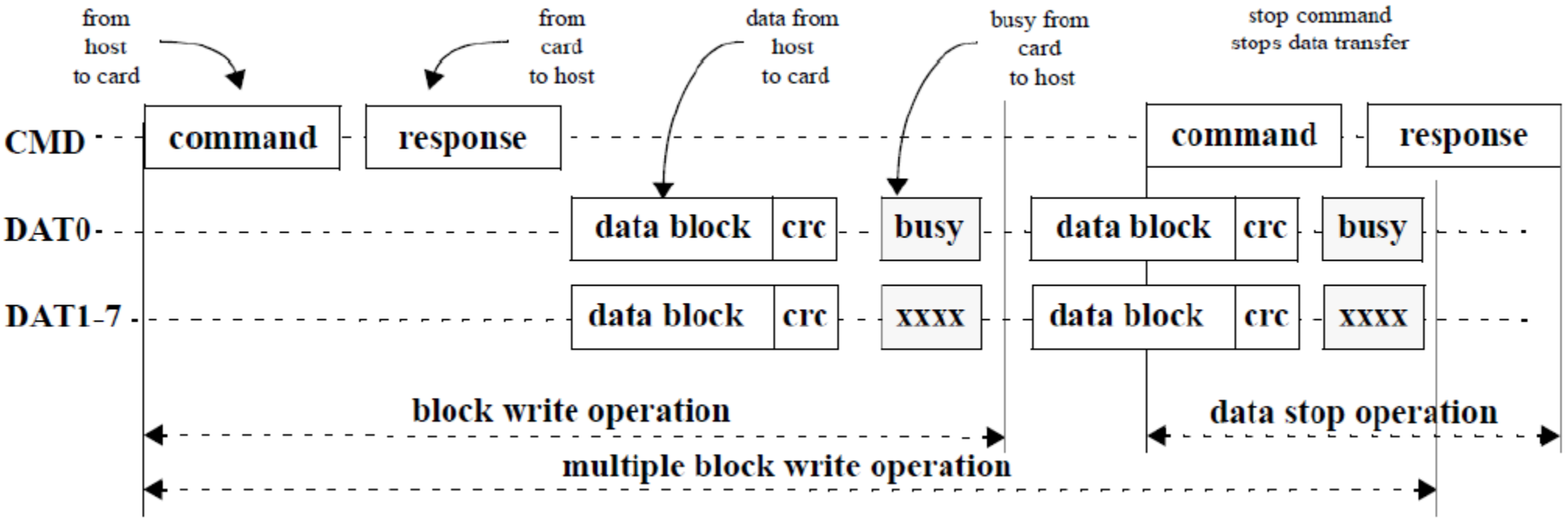
Packet Formats & Operation

Multiple Read Operation



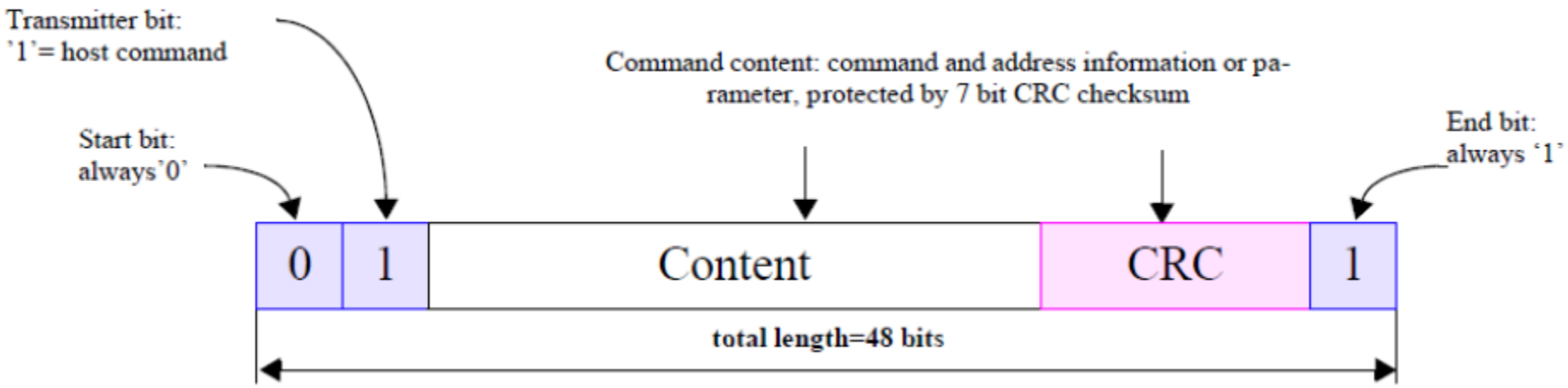
Source: JEDEC Standard No. 84-B51 Figure 2

Multiple Write Operation



Source: JEDEC Standard No. 84-B51 Figure 3

Command Token Format

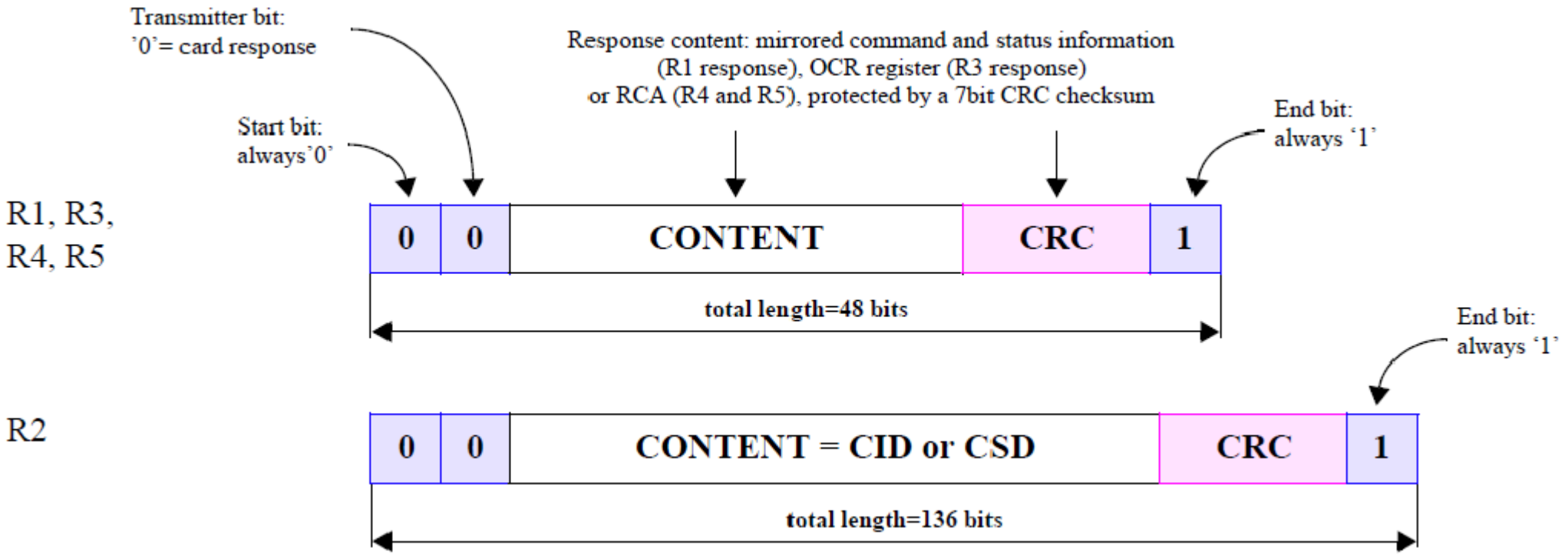


Source: JEDEC Standard No. 84-B51 Figure 5

Quick Definitions for Next Slide

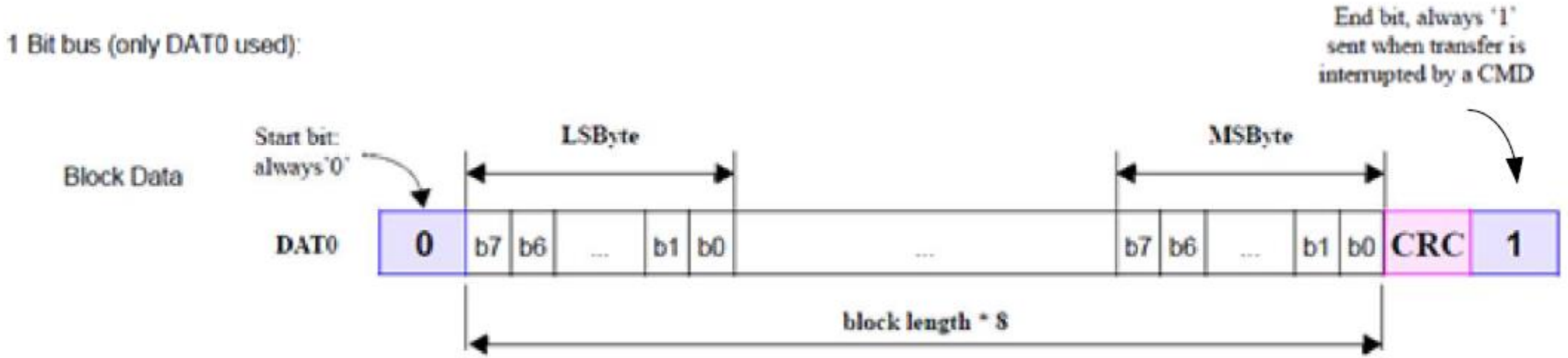
- **CID:** Card Identification number register
- **CSD:** Card Specific Data register

Response Token Format



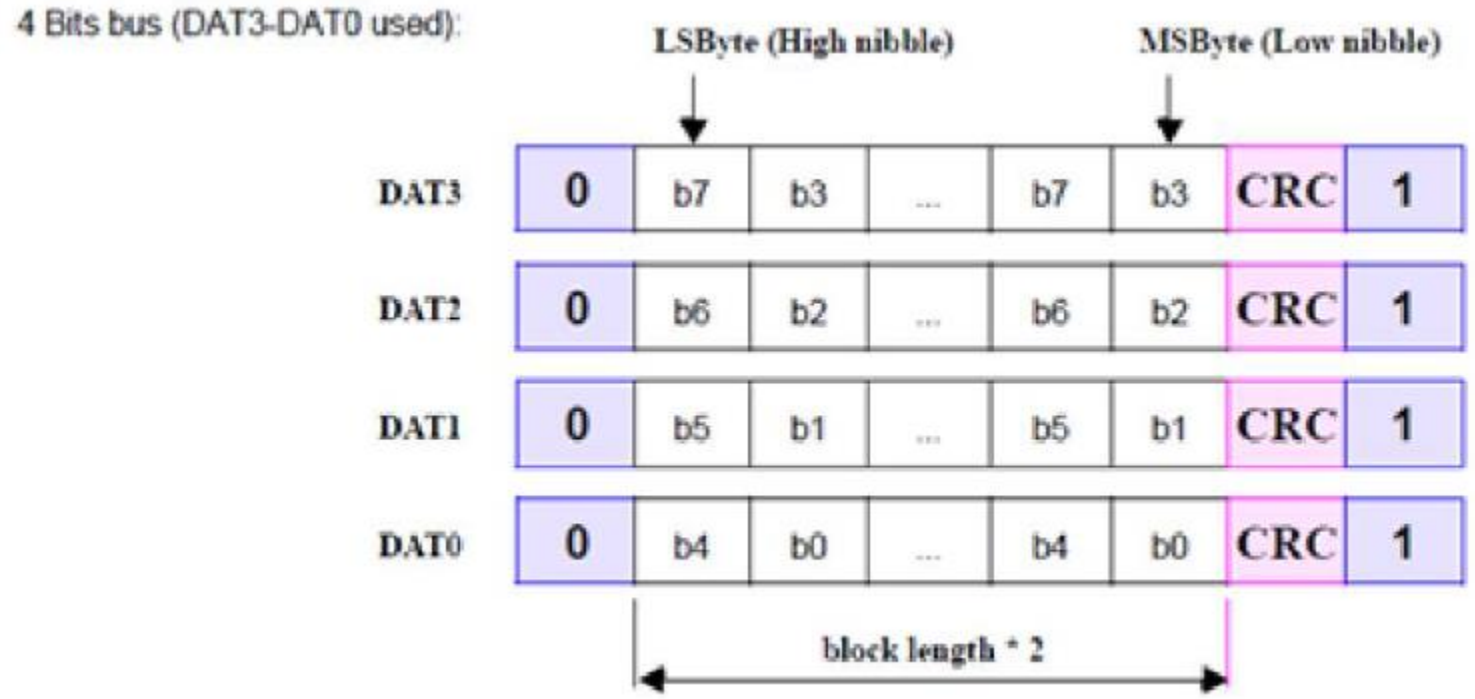
Source: JEDEC Standard No. 84-B51 Figure 6

Single Bit Bus Data Packet Format for SDR



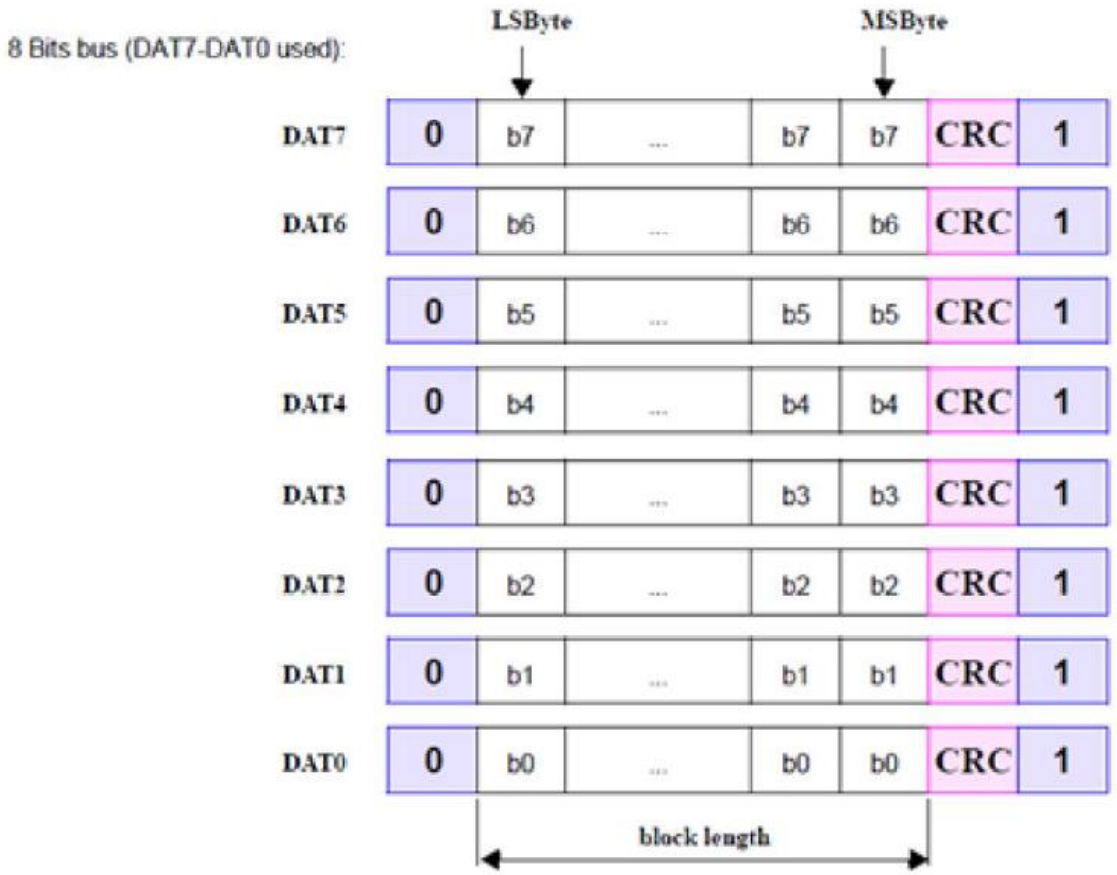
Source: JEDEC Standard No. 84-B51 Figure 7

4 Bit Bus Data Packet Format for SDR



Source: JEDEC Standard No. 84-B51 Figure 7

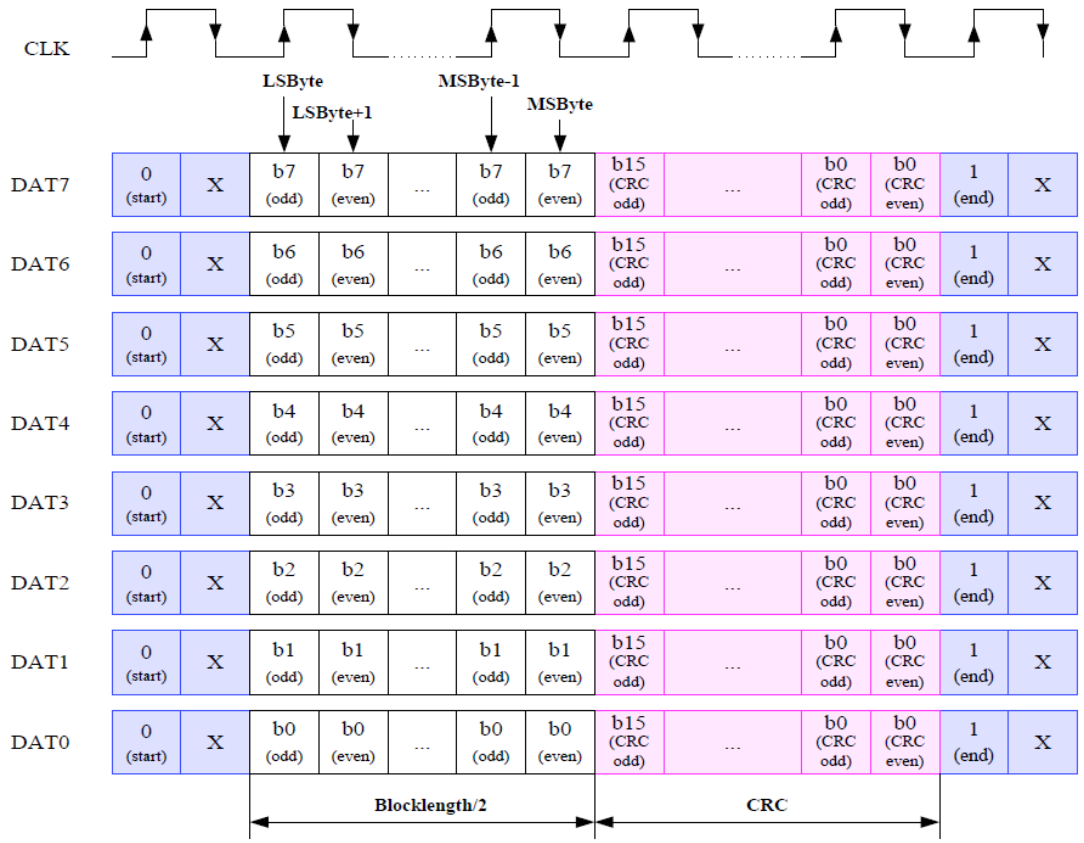
8 Bit Bus Data Packet Format for SDR



Source: JEDEC Standard No. 84-B51 Figure 7

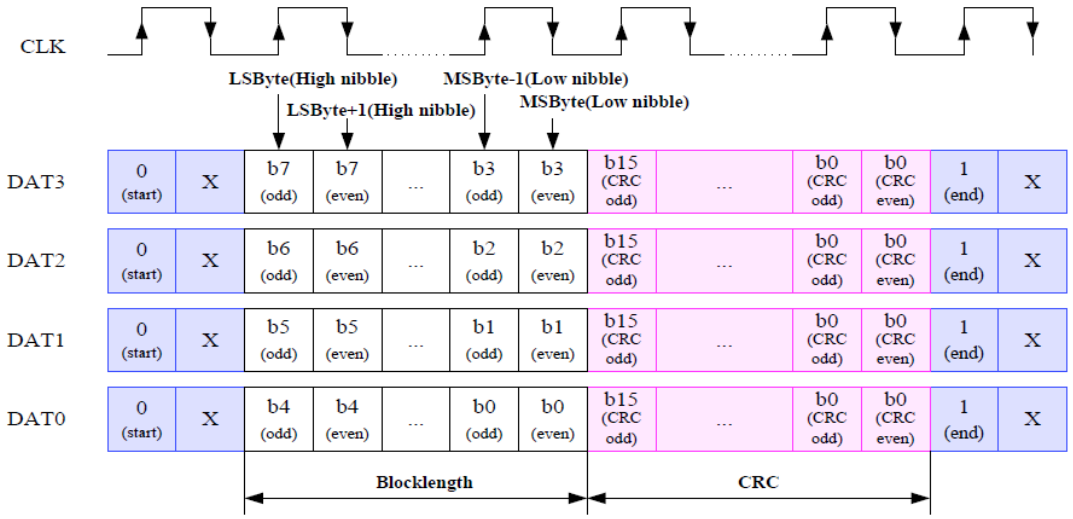
Data Packet Format for DDR

8 Bits bus DDR (DAT7-DAT0 used):



Notice that bytes data are not interleaved but CRC are interleaved
Start and end bits are only valid on the rising edge. ("x": undefined)

4 Bits bus DDR (DAT3-DAT0 used):



Source: JEDEC Standard No. 84-B51 Figure 8

Bus Speed Modes

Mode Name	Data Rate	I/O Voltage	Bus Width	Frequency	Max Data Transfer (implies x8 bus width)
Backwards Compatibility with legacy MMC card	Single	3 V/1.8 V/ 1.2 V	1, 4, 8	0-26 MHz	26 MB/s
High Speed SDR	Single	3 V/1.8 V/ 1.2 V	1,4, 8	0-52 MHz	52 MB/s
High Speed DDR	Dual	3 V/1.8 V/ 1.2 V	4, 8	0-52 MHz	104 MB/s
HS200	Single	1.8 V/1.2 V	4, 8	0-200 MHz	200 MB/s
HS400	Dual	1.8 V/1.2 V	8	0-200 MHz	400 MB/s

Source: JEDEC Standard No. 84-B51 Table 4

Interfacing with eMMC

- Interfacing with the eMMC controller is akin to microcontroller programming
  - Many different control registers
- Bus Width Selection Example:
  - SWITCH command issued on CMD
  - Write to the BUS_WIDTH byte in Modes Segment of EXT_CSD reg

7.4 Extended CSD register (cont'd)

7.4.67 BUS_WIDTH [183]

It is set to '0' (1 bit data bus) after power up and can be changed by a SWITCH command.
Bus Width, Normal or DDR mode and Strobe mode (for HS400) are defined through BUS_WIDTH register.

Source: JEDEC Standard No. 84-B51 Page 203

Table 144 — BUS_WIDTH

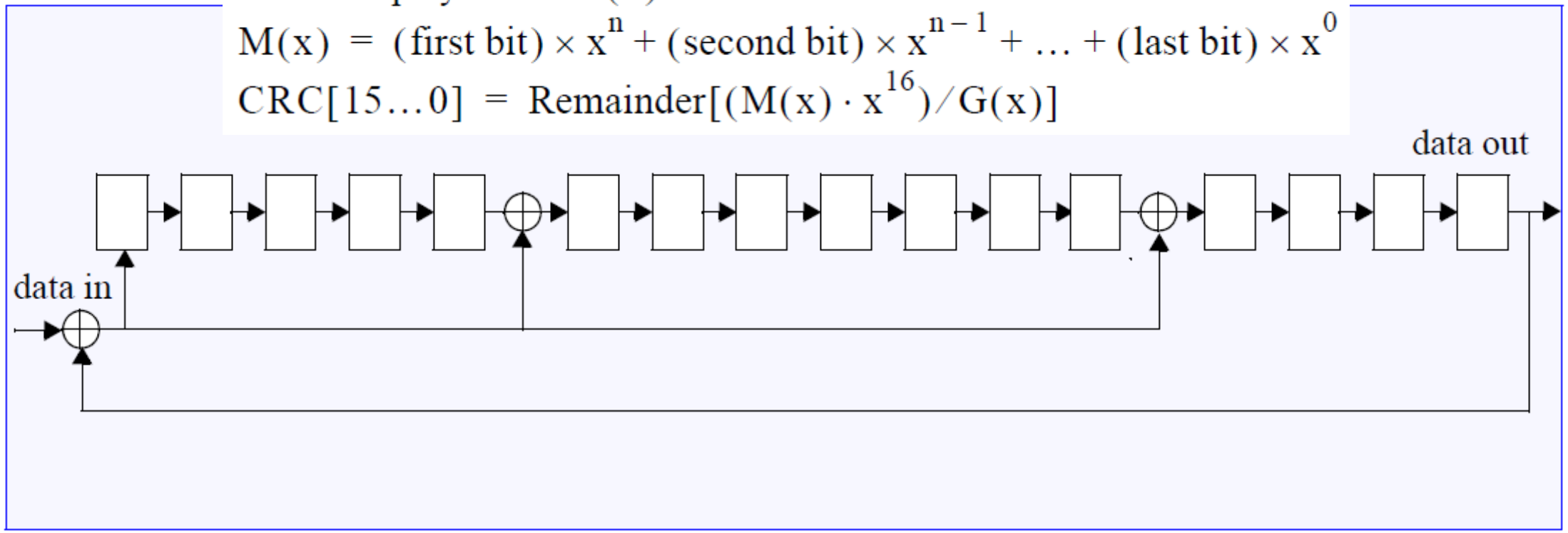
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Enhanced Strobe	Reserved	Reserved	Reserved	Bus Mode Selection			

CRC 16 Generation (Payload)

$$\text{Generator polynomial } G(x) = x^{16} + x^{12} + x^{5} + 1$$

$$M(x) = (\text{first bit}) \times x^{n} + (\text{second bit}) \times x^{n-1} + \ldots + (\text{last bit}) \times x^{0}$$

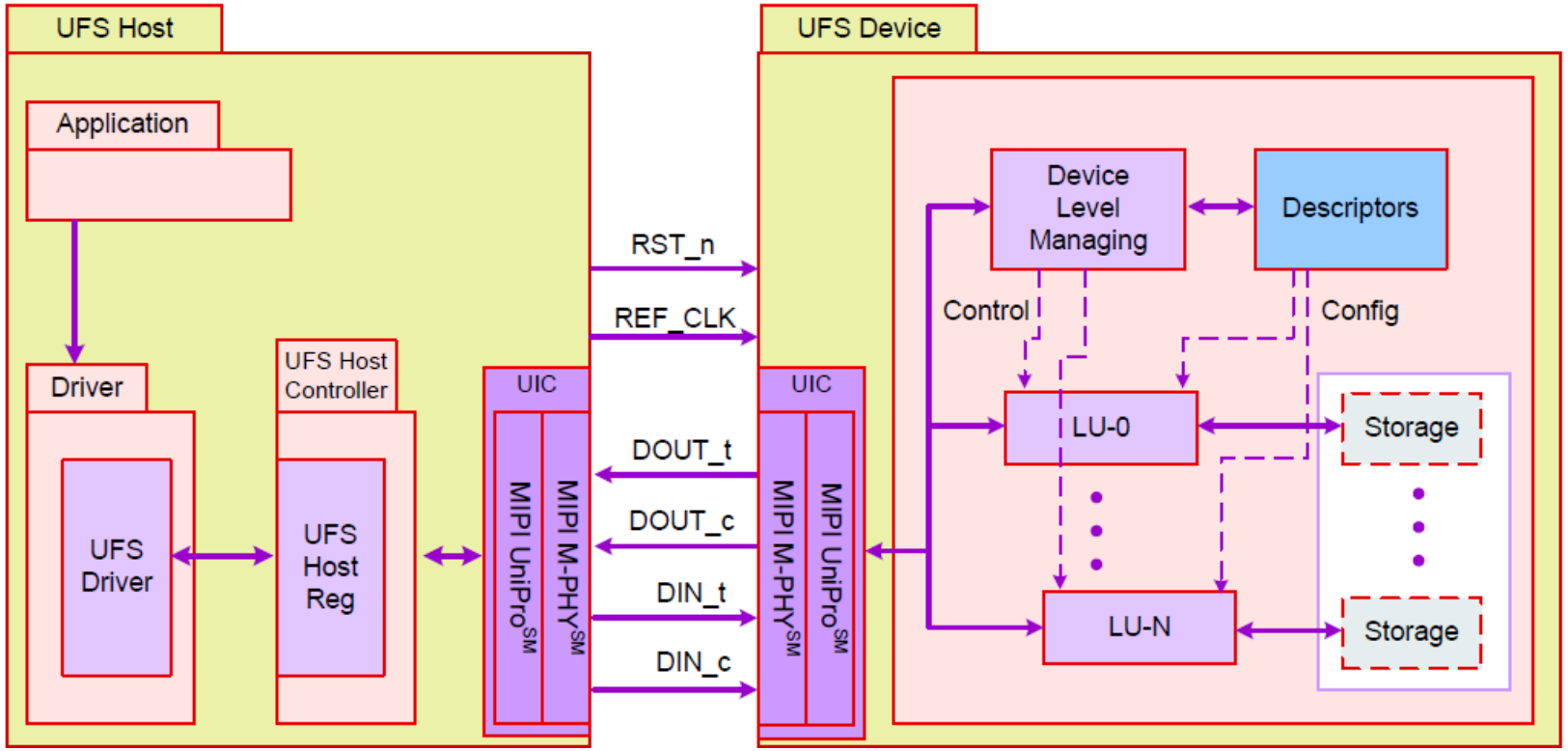
$$CRC[15\ldots0] = \text{Remainder}[(M(x) \cdot x^{16})/G(x)]$$

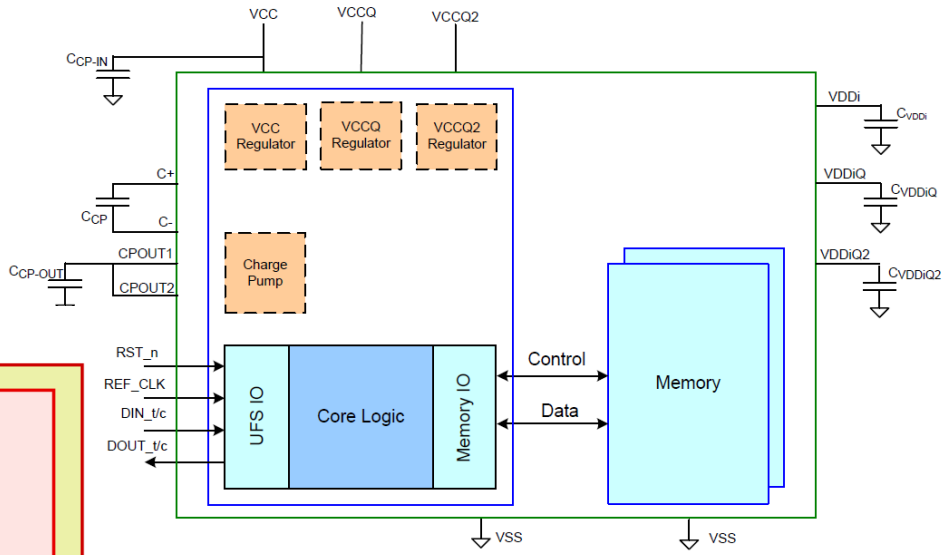


Source: JEDEC Standard No. 84-A441 Figure 56 / Page 158

Higher Performing Technologies

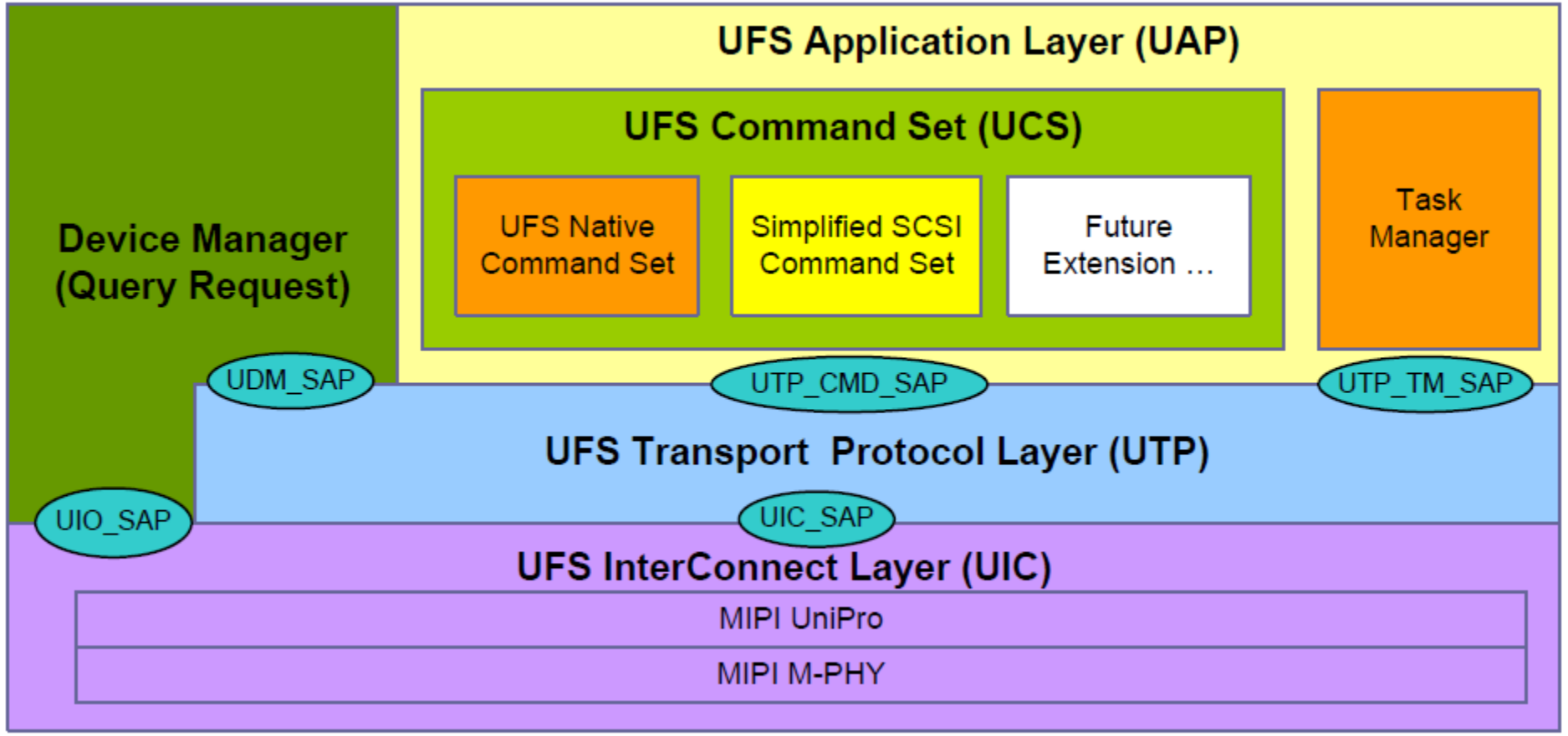
Universal Flash Storage (UFS) Architecture Overview





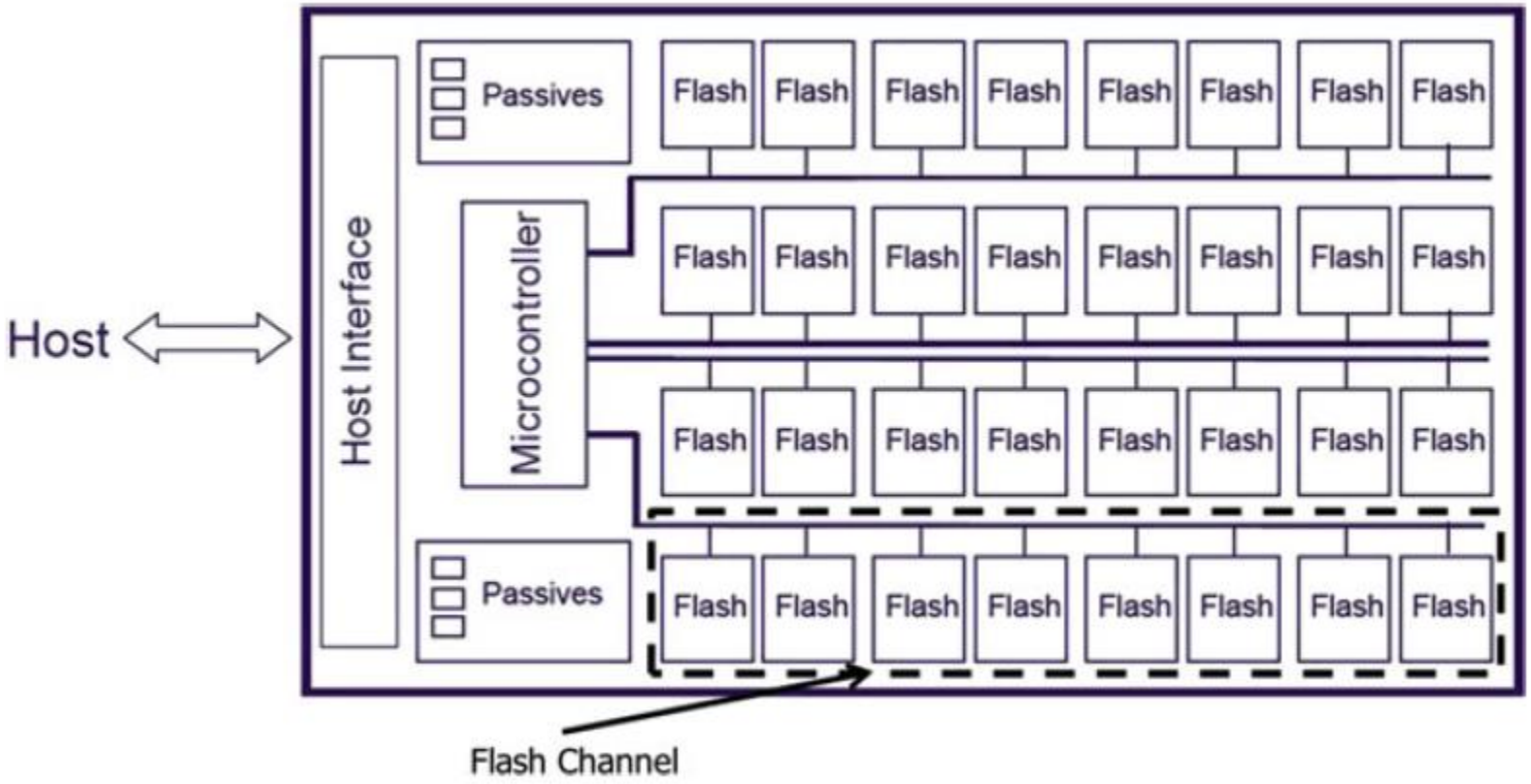
Source: JEDEC Standard No. 220C Figure 5-4 / 6-1

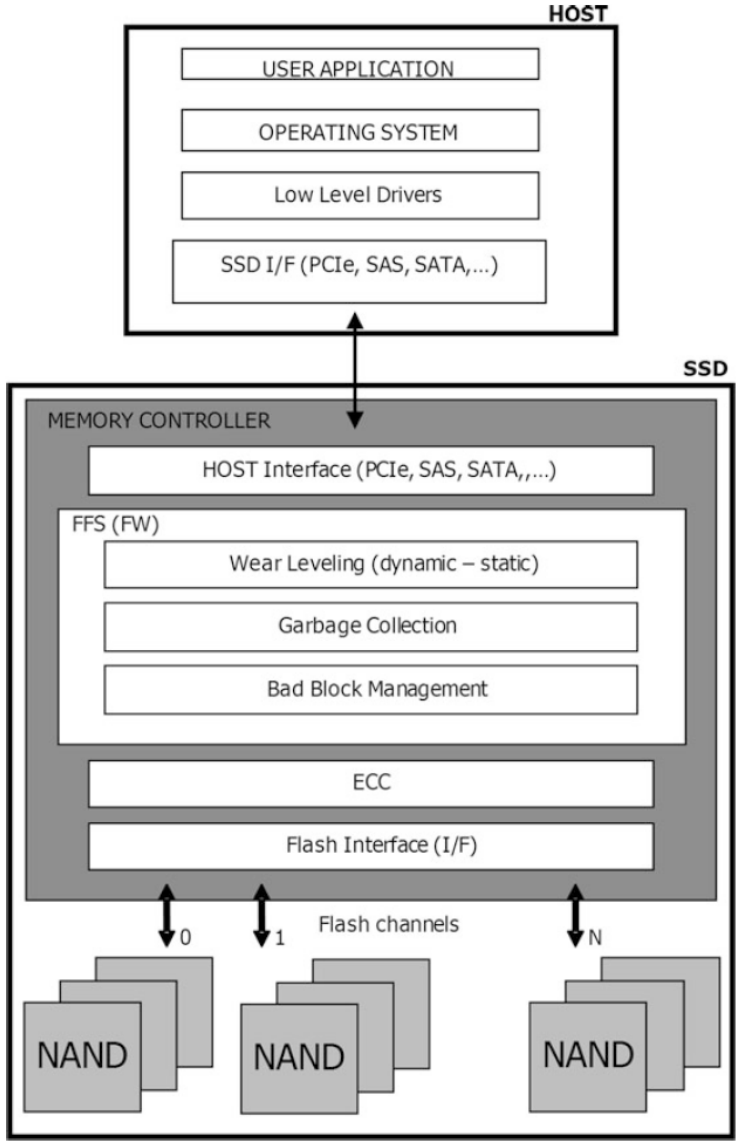
UFS Communication Overview



Source: JEDEC Standard No. 220C Figure 5-1

Solid State Drive (SSD)





Source: SSD Architecture and PCI Express Interface Figure 2.1 / 2.9

References

- CMOS Circuit Design, Layout, and Simulation, Third Edition – R. Jacob Baker
  http://cmosedu.com/cmos1/book.htm
- A Survey of Flash Translation Layer – Tae-Sun Chung, et al.
  http://idke.ruc.edu.cn/people/dazhou/Papers/AsurveyFlash-JSA.pdf
- JEDEC Standard No. 84-A441
  https://www.jedec.org/standards-documents/docs/jesd84-a441
- JEDEC Standard No. 84-B51
  https://www.jedec.org/standards-documents/docs/jesd84-b51
- JEDEC Standard No. 220C
  https://www.jedec.org/standards-documents/docs/jesd220c
- SSD Architecture and PCI Express Interface – K. Eshghi & R. Micheloni
  https://link.springer.com/chapter/10.1007%2F978-94-007-5146-0_2