The Use and Design of Synchronous Mirror Delays

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ECG 721 – Spring 2017

Presentation Overview

- Synchronization circuit
- Topologies covered in class
  - PLL and DLL – pros and cons
- Synchronous mirror delay introduction
  - Base topology
  - Theory of operation
  - Pros/cons
- Alternative topologies
  - DFF topology
  - Analog topology

Synchronization Circuits

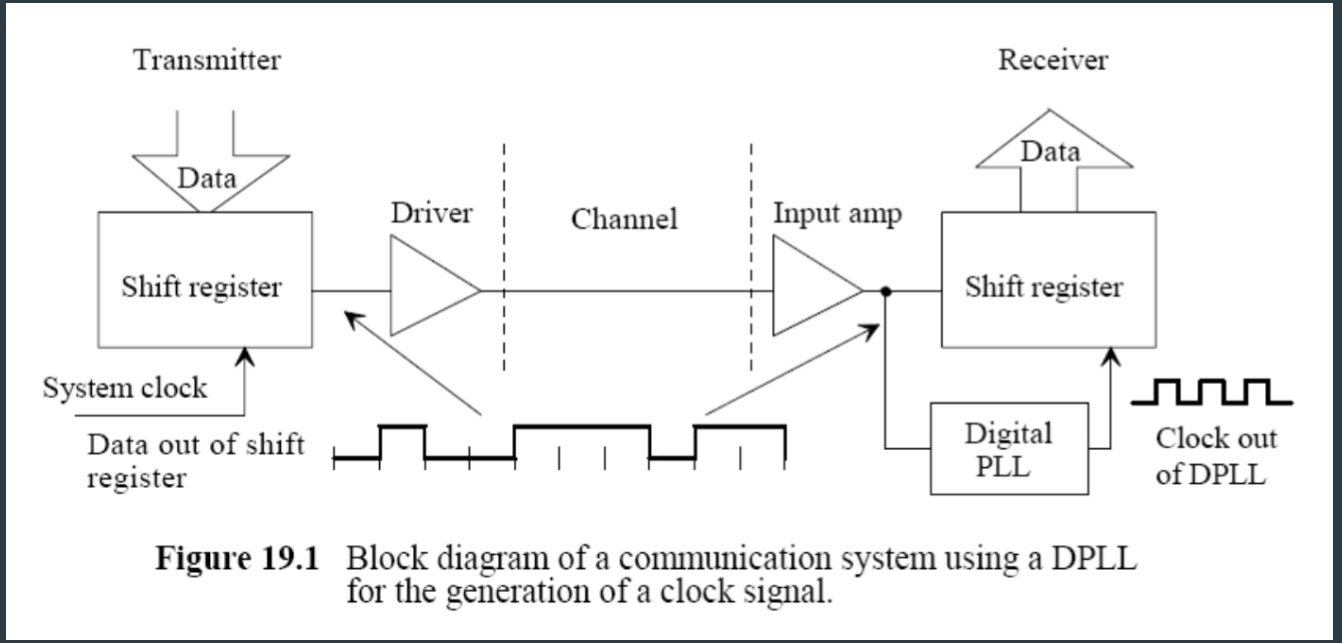


Figure 19.1 Block diagram of a communication system using a DPLL for the generation of a clock signal.

- Goal: Regenerate the transmitted clock so that received data can be read correctly
- Clock skew becomes more of a problem as frequency and channel distance increases

Class Taught Topologies

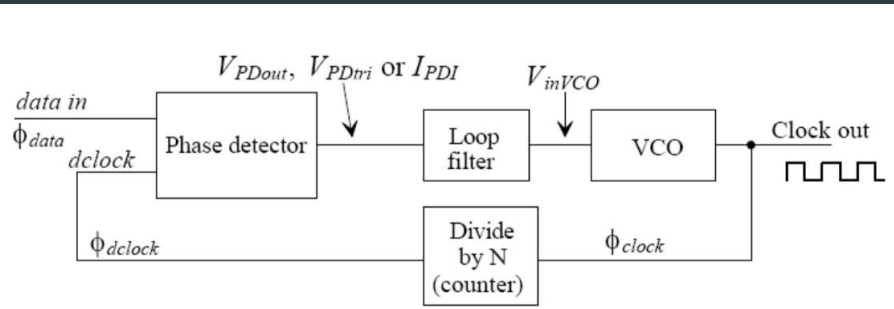


Figure 19.3 Block diagram of a digital phase-locked loop.

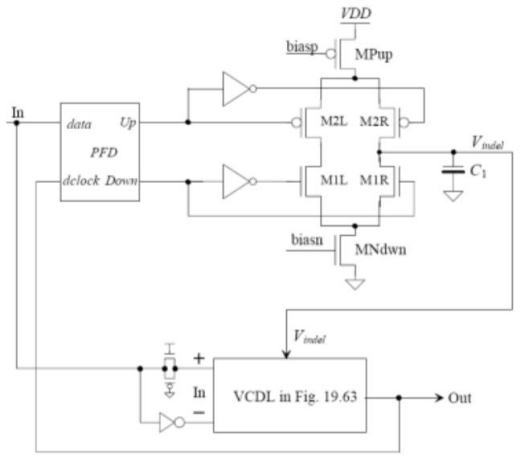
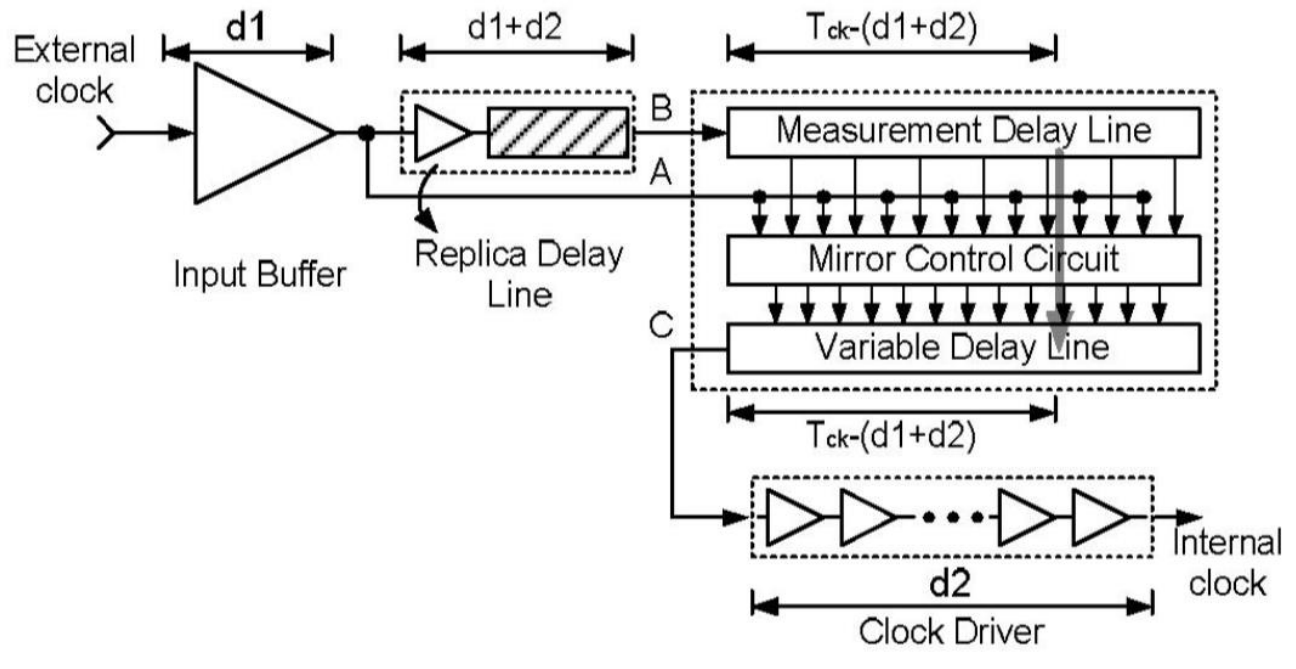


Figure 19.65 Block diagram of a DLL.

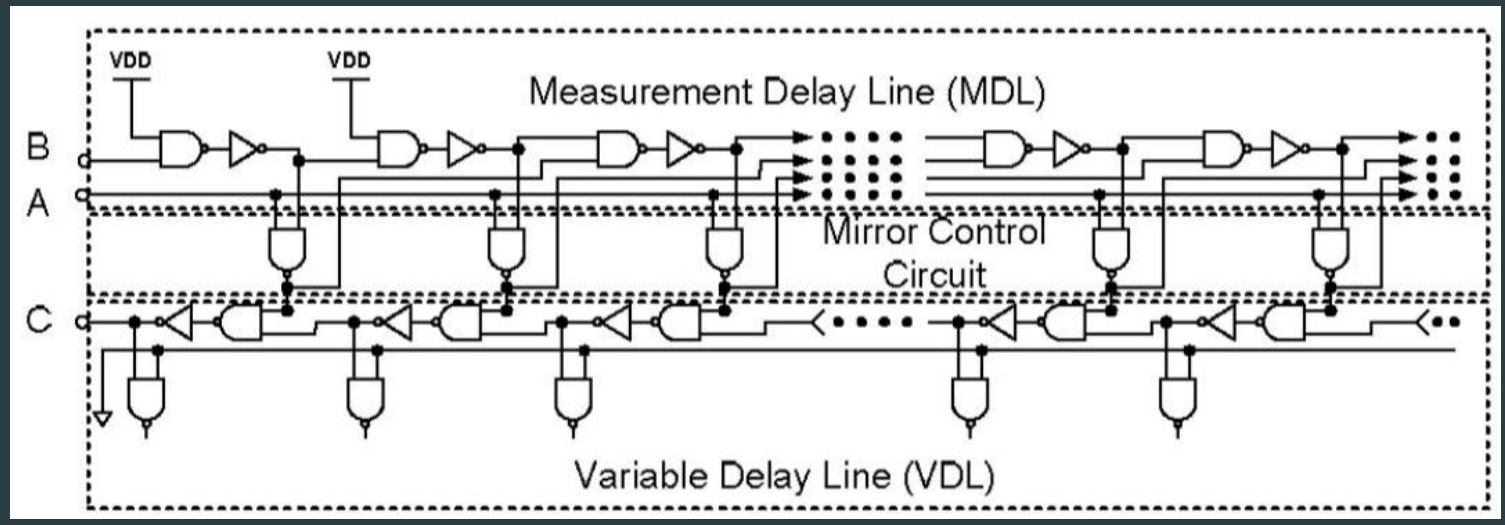
- The phase-locked loop (PLL) and delay locked-loop (DLL) do a good job of correcting clock skew and regenerating a proper clock
- Both are closed loop systems
  - Higher order system = complicated control operations
  - Long lock time = burns power

Synchronous Mirror Delay - Topology



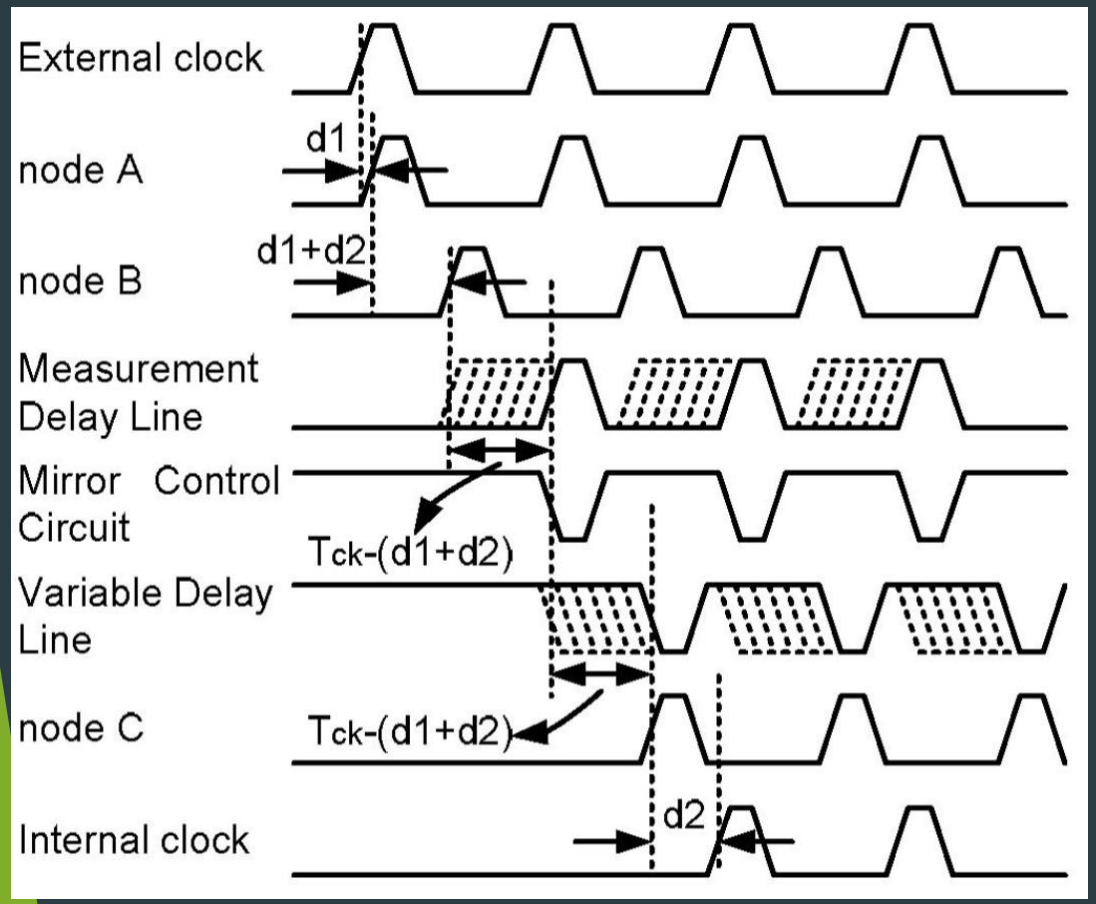
- 6 main parts
  - Measurement delay line (MDL)
  - Mirror control circuit (MCC)
  - Variable delay line (VDL)
  - Input buffer
  - Clock driver
  - Replica delay line

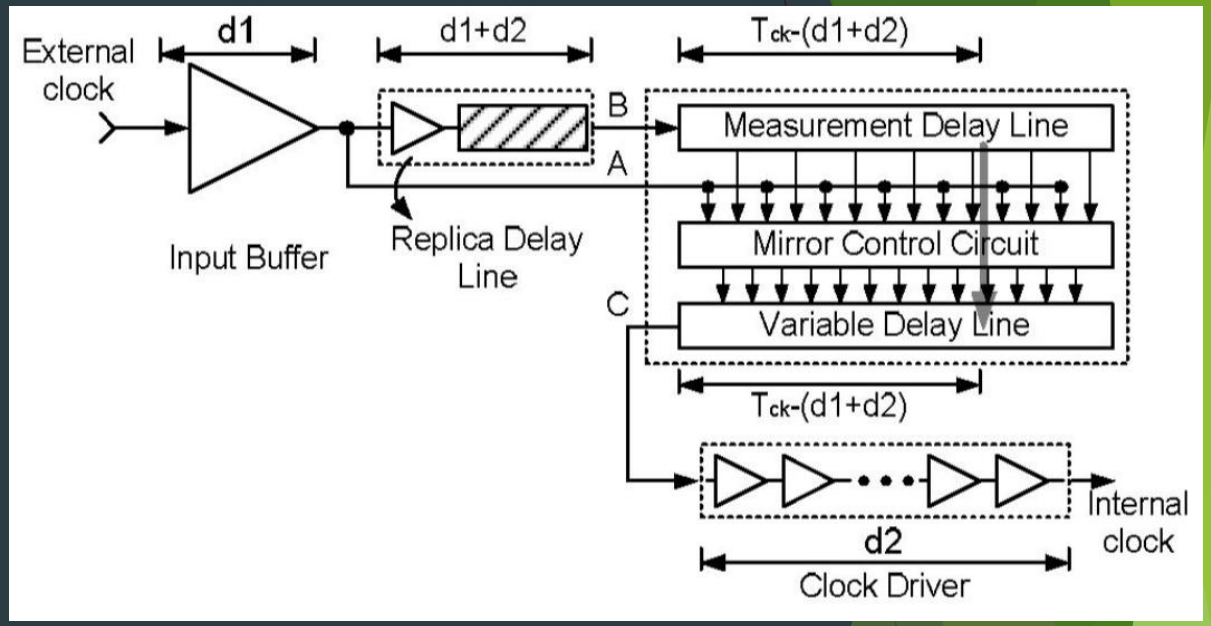
Synchronous Mirror Delay - Operation

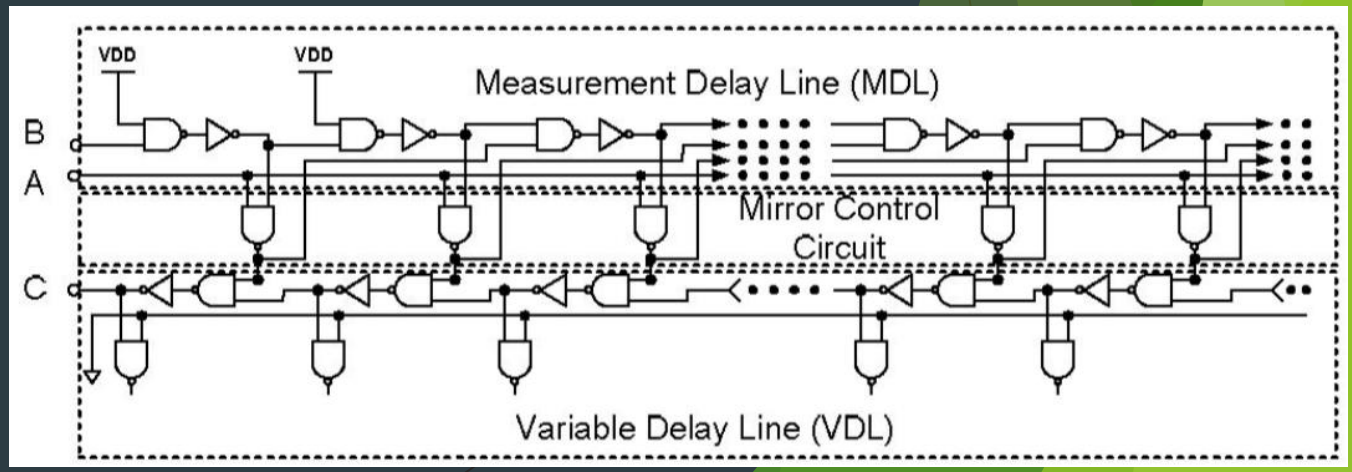


- Consider n, n+1, and n+2 clock pulses
- MDL delay of nth pulse is T_{clk} - $(d_1 + d_2)$; first clock delay
- nth pulse is mirrored into VDL through the MCC by the (n+1) pulse
- VDL delay of nth pulse is also T_{clk} - $(d_1 + d_2)$; second clock delay
- VDL outputs the nth pulse to a clock driver with delay d_2
- nth pulse arrives at output as n+2 input pulse is at the input

Synchronous Mirror Delay - Operation







Synchronous Mirror Delay - Design

$$\underbrace{d_1}_{\text{Input buffer}} + \underbrace{(d_1 + d_2)}_{\text{Replica delay line}} + \underbrace{(T_{clk} - d_1 - d_2)}_{\text{Measurement delay line}} + \underbrace{(T_{clk} - d_1 - d_2)}_{\text{Variable delay line}} + \underbrace{d_2}_{\text{Clock driver}} = 2T_{clk}$$

$$T_{clk,max} = d_1 + d_2 + NT_{cd}$$

T_{cd}; *cell delay*

$$T_{clk,min} = d_1 + d_2$$

$$N = \frac{T_{clk,max} - (d_1 + d_2)}{T_{cd}}$$

quantization error will be introduced if N is not a whole number

Synchronous Mirror Delay - Calculation

- A typical circuit can have the following properties
  - d_1 = 55ps
  - d_2 = 220ps
  - T_{cd} = 48ps
- For a design of 1.5GHz
  - $T_{clk,max} = 667\text{ps}$
  - N = 8.17, round to N = 9
- Notice that for a slower design, N increases
  - 1GHz $\rightarrow$ N = 16
  - 100MHz $\rightarrow$ N = 203
  - This can be less dramatic by increasing T_{cd}, but you add quantization error

Synchronous Mirror Delay – Pros/Cons

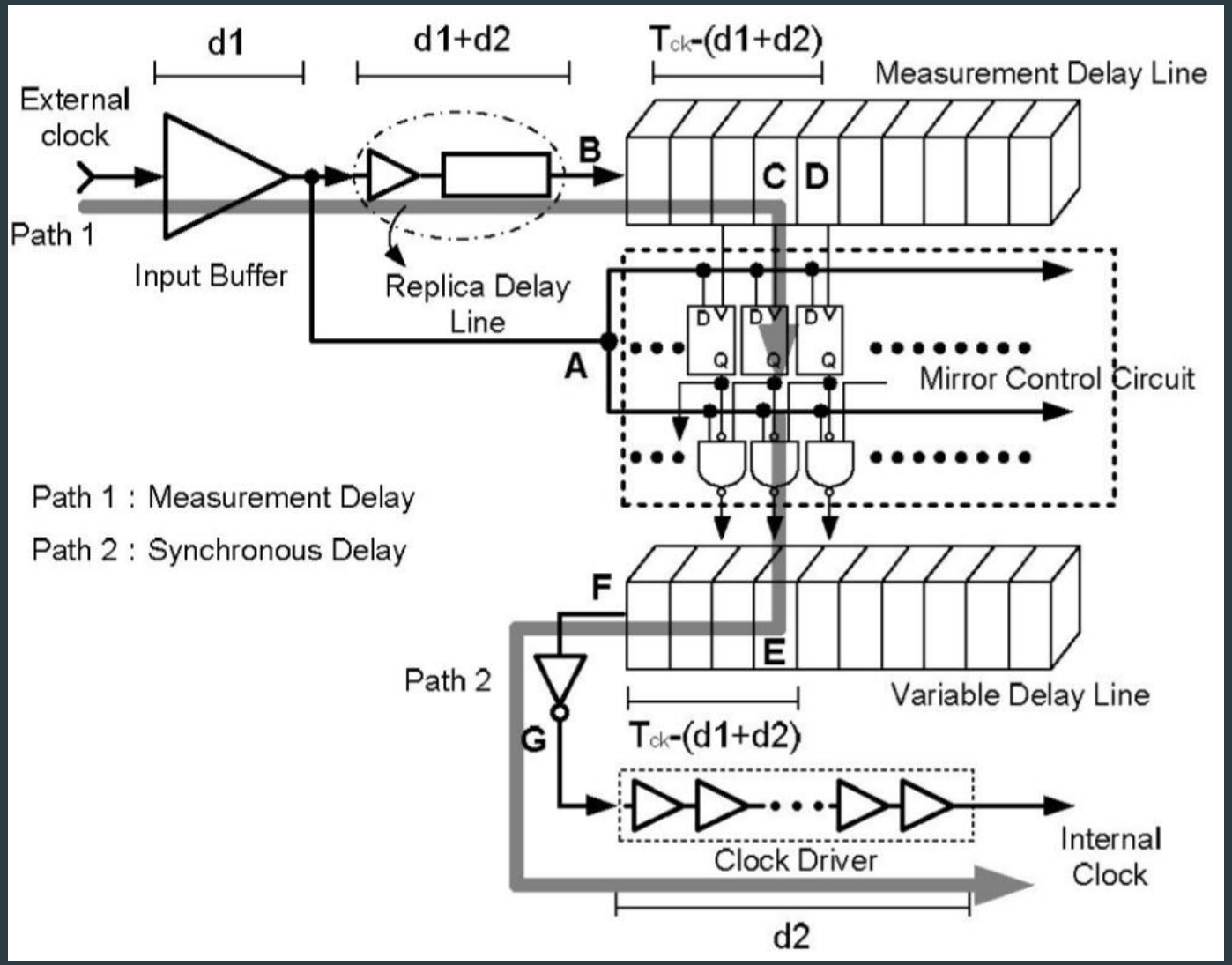
Pros

- Less complicated design
- Fast 2 cycle lock time
- Low power consumption
- No feedback jitter

Cons

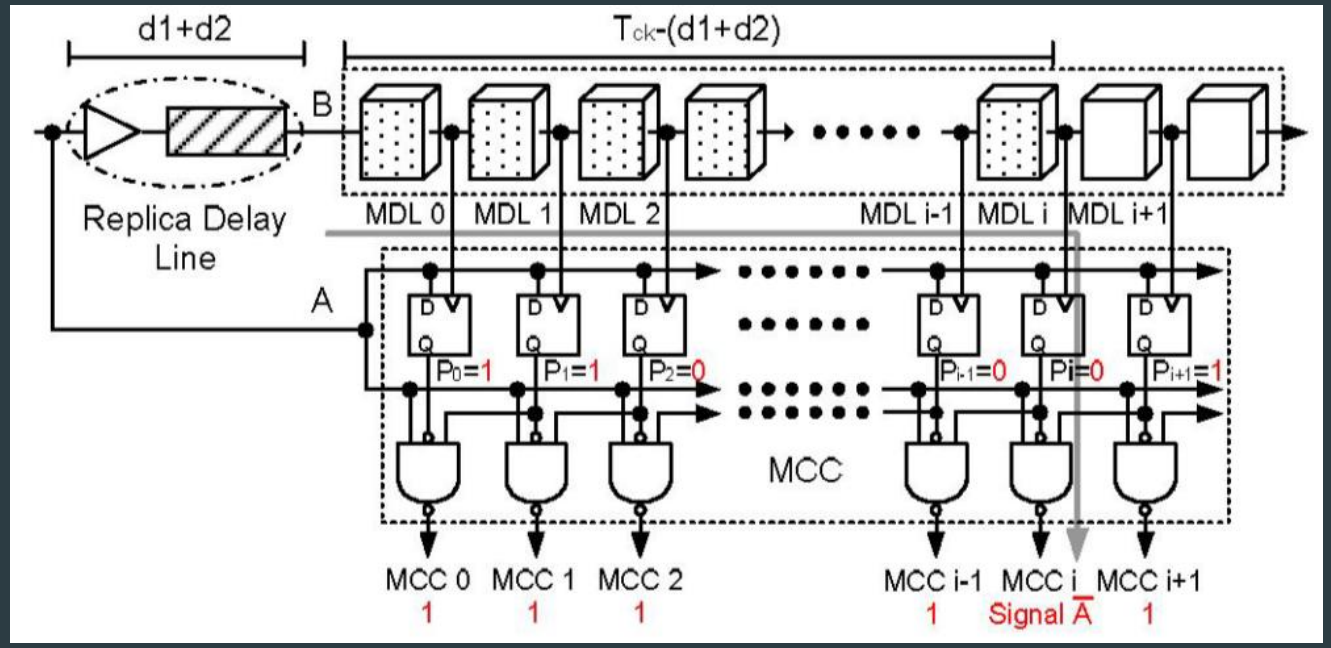
- Layout blows out for lower frequencies
- Must be designed for specific frequency – not very versatile
- Will only accept an input with 50% or less duty cycle
- Has a quantization error

Alternative Topology – D Flip-Flop



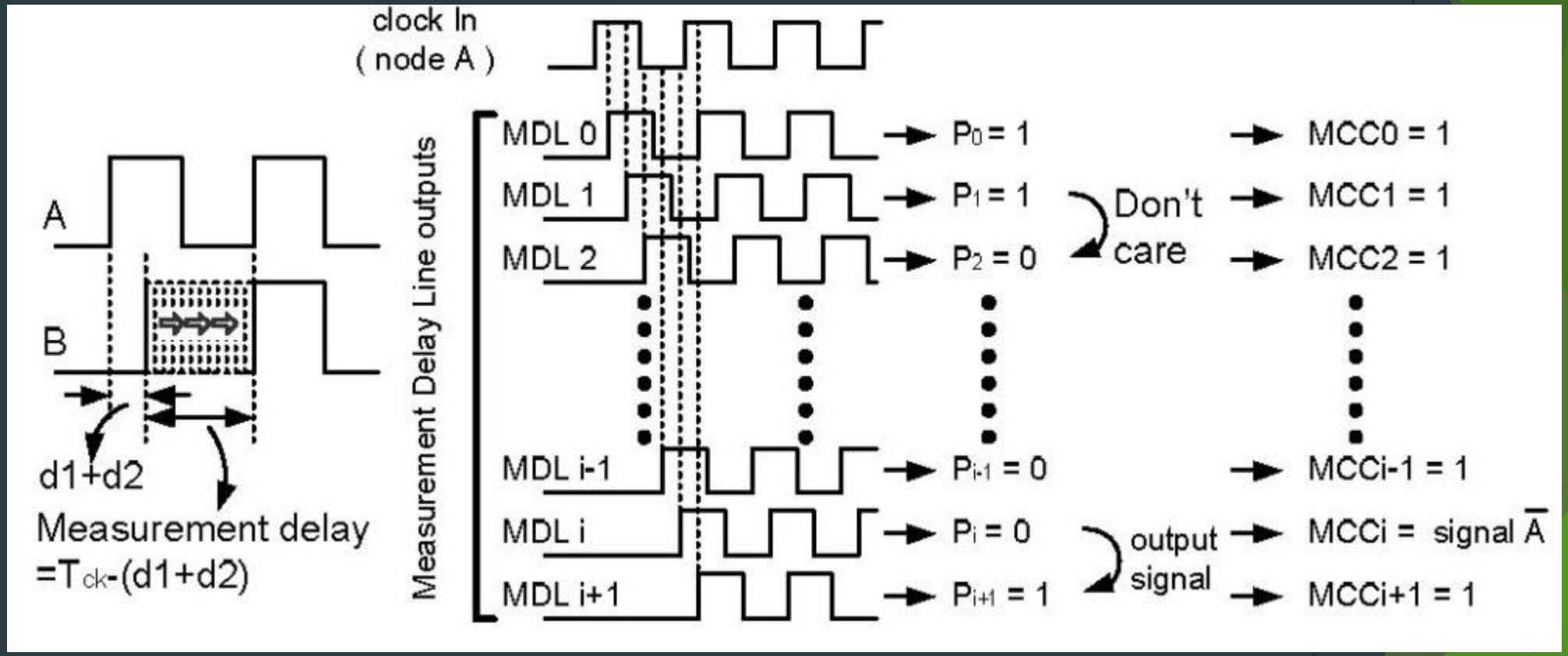
- D type flip-flop and 3-input NAND gates replace original NAND gates in MCC
- Detects clock edge instead of pulse width

Alternative Topology – D Flip-Flop



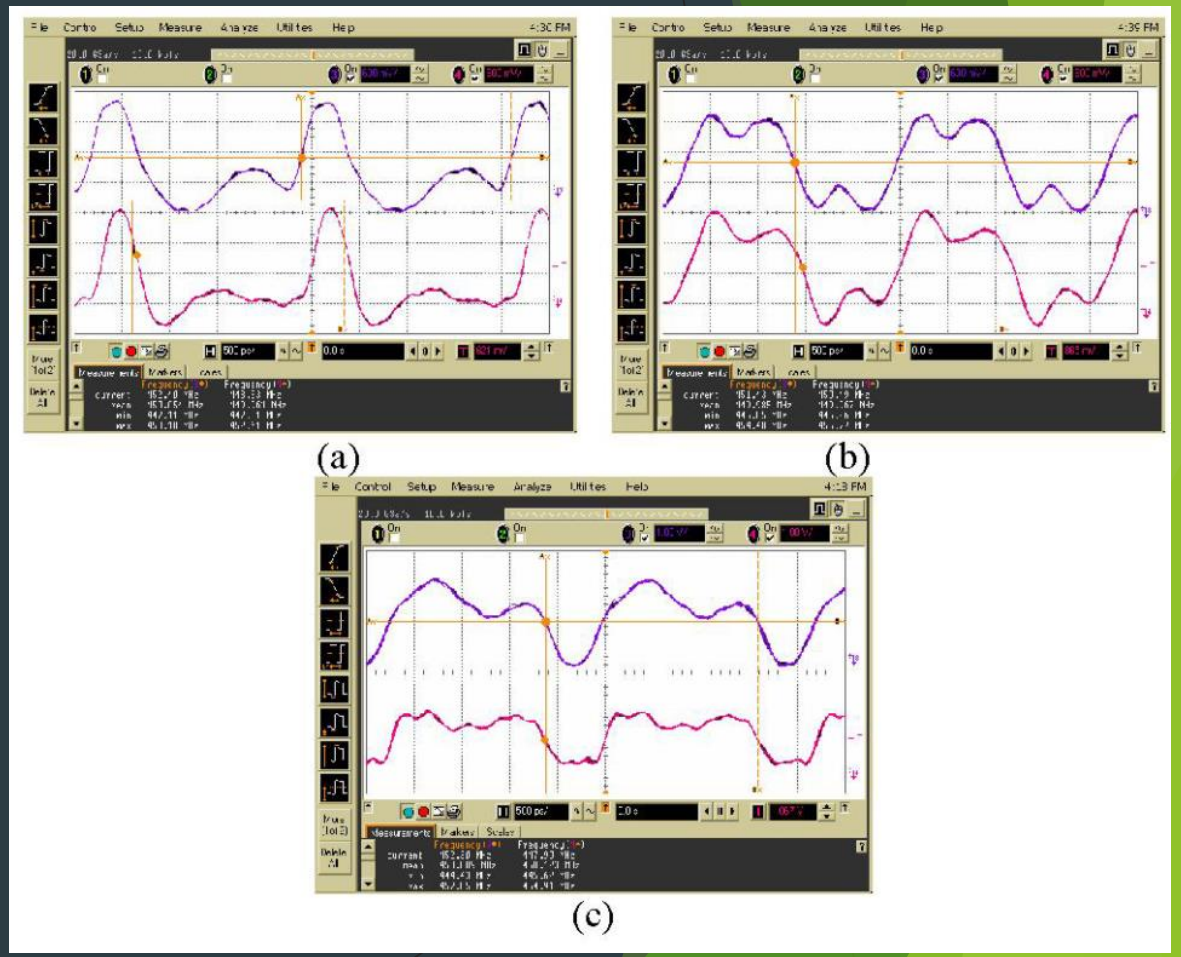
- Outputs of MDL are used as the DFF control signals to sample the clock signal
- Each 3-input NAND also contain the output of the next stage
- Only 1 MCC output can change which occurs when the DFF outputs of stage i and i+1 are different (clock edge)

Alternative Topology – D Flip-Flop



Alternative Topology – D Flip-Flop

Performance Summary	
Process	TSMC 0.18 μm 1P6M CMOS
Supply Voltage	1.8 V
Operating Frequency Range	450 ~ 750 MHz
Duty Cycle Range	20% ~80 %
Number of delay cells	20
Lock Time	2 cycle time
Static Phase Error	<58.7ps
Jitter @ 450MHz	2.558ps rms / 22ps pk-pk
Jitter @ 750MHz	2.94ps rms / 24ps pk-pk
Power Consumption	5.4mW@450MHz 9mW@750MHz
Active Area	58 x 180 μm^2 (without I/O buffer)
Chip Area	600 x 440 μm^2 (with I/O pad)



Alternative Topology – DFF SMD Pros/Cons

Pros

- Less complicated design
- Fast 2 cycle lock time
- Low power consumption
- No feedback jitter
- Will accept an input with >50% duty cycle

Cons

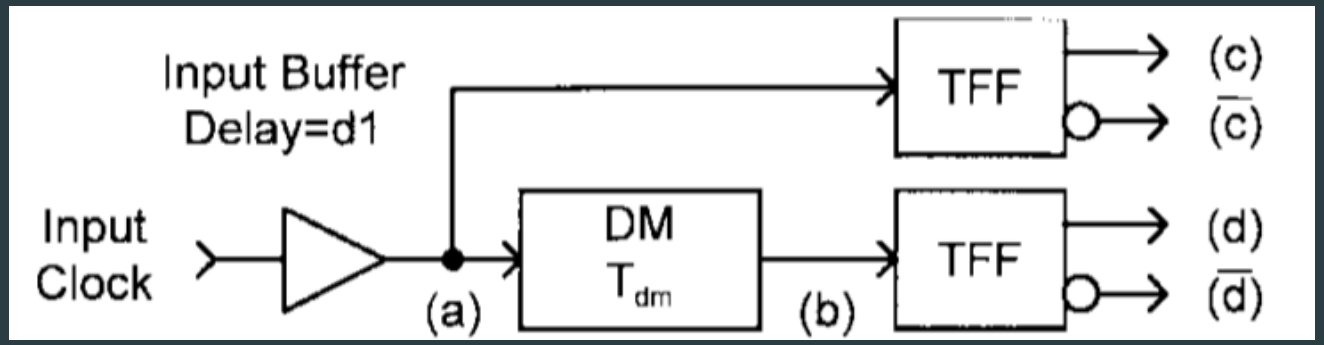
- Layout blows out for lower frequencies
- Must be designed for specific frequency – not very versatile
- Has a quantization error

Alternative Topology – Analog SMD (ASMD)

- Goal: use an analog topology (charge pumps) to regenerate the input clock in order to eliminate the effects of quantization

- Main components:
  - Input buffer
  - Delay monitor
  - Clock divider
  - Charge pump and comparator
  - Clock driver

Alternative Topology – Analog SMD (ASMD)

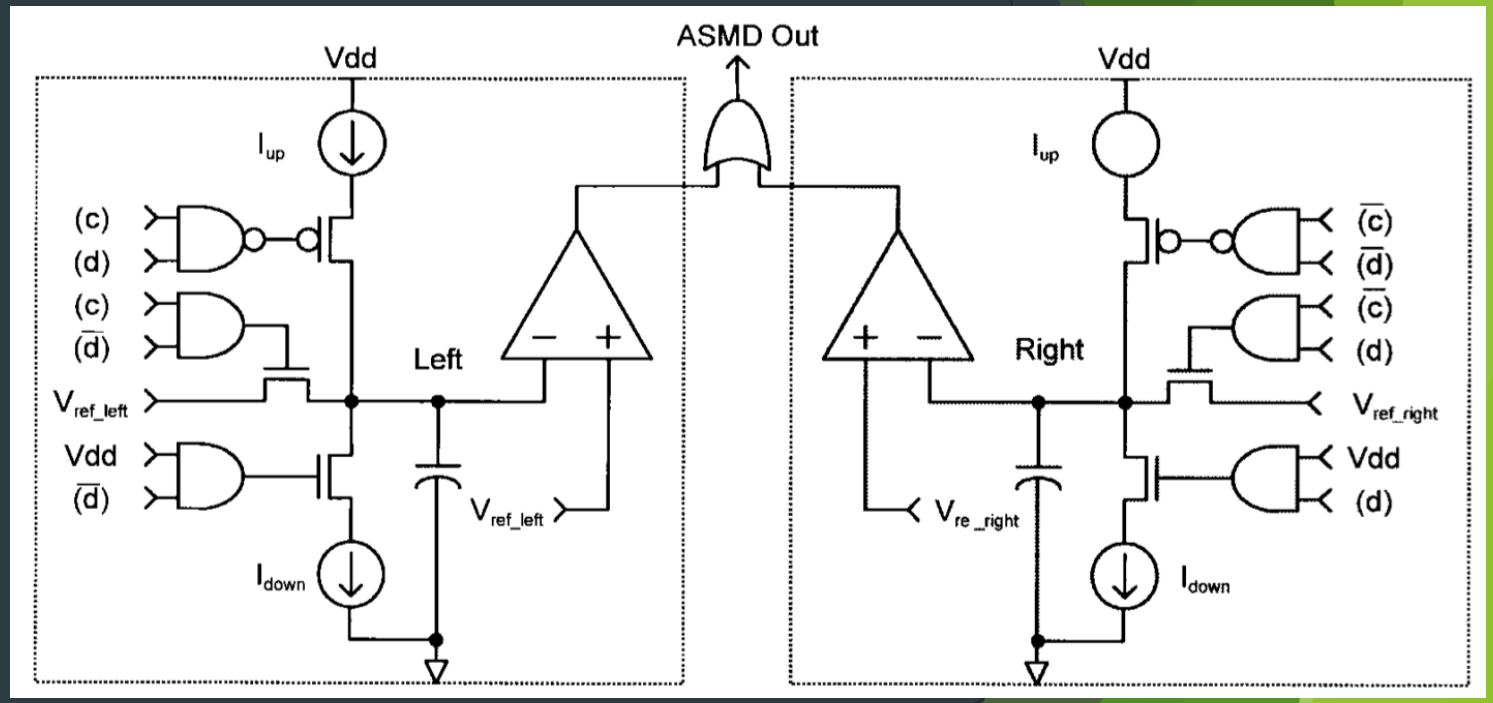


T	Q	Q^+	Operation
0	0	0	Hold
0	1	1	Hold
1	0	1	Toggle
1	1	0	Toggle

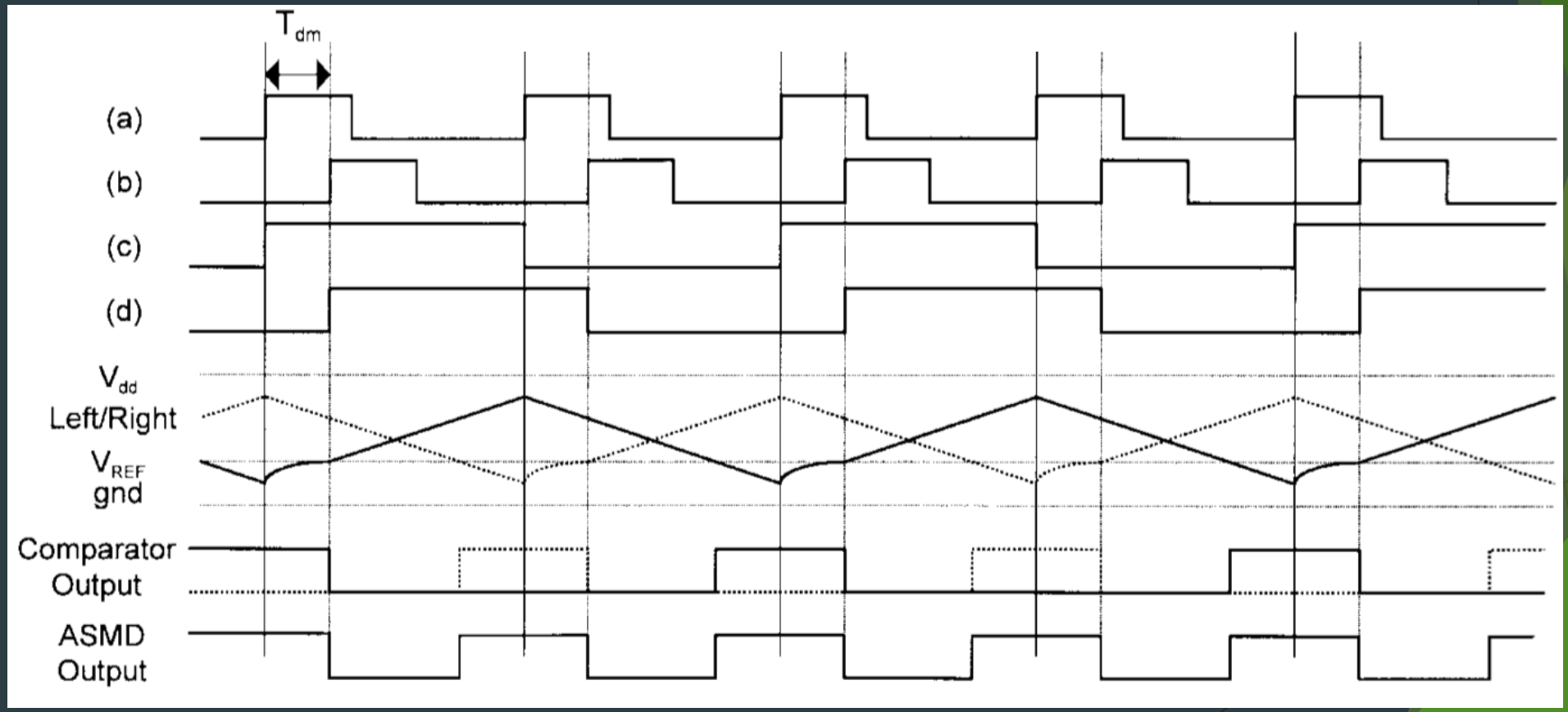
- TFF is used for similar reasons as the DFF was used on the previous topology; it operates based on edge detection in order to accept a more arbitrary duty cycle
- TFF doubles the period

Alternative Topology – Analog SMD (ASMD)

- {c,d} = {H,L} : eq-period
  - Initialize the voltage of the left node to V^{ref}
- {c,d} = {H,H}: up-period
  - Pump up the voltage of the left node form V^{ref} toward V^{dd} using a current source whose interval is (T^{clk} – T^{dm})
- c = L: down-period
  - Pump down the voltage of the left node from the final up-period value toward ground and measure the time when the “left” crosses V^{ref} and generates an output pulse
- Same logic for “right” which is 180° out of phase
  - x2 multiple accounts for the ½ of TFF



Alternative Topology – Analog SMD (ASMD)



Alternative Topology – ASMD Pros/Cons

Pros

- Less complicated design
- Fast 2 cycle lock time
- Low power consumption
- No feedback jitter
- Will accept an input with >50% duty cycle
- Ideally, no quantization error
- Will accept a broad range of frequencies
- Layout does not blow out for lower frequencies

Cons

- Dependent on having very linear and matched pumping current
- Consumes more power
  - Comparator and bias circuit constantly consume power

Thank You!

QUESTIONS??

References

- [1] Baker, R. Jacob, “CMOS Circuit Design, Layout, and Simulation,” 3rd edition, John Wiley & Sons, 2010
- [2] Hung, C. et al, “Arbitrary Duty Cycle Synchronous Mirror Delay Circuits Design,” IEEE Solid State Circuits Conference, 13-15 Nov. 2006
- [3] Shim, D. et al, “An Analog Synchronous Mirror Delay for High-Speed DRAM Application,” IEEE Journal of Solid-State Circuits, Vol. 34, pp. 484-493, Apr. 1999
- [4] Cheng, K. et al, “Wide-Range Synchronous Mirror Delay with Arbitrary Input Duty Cycle,” Electronics Letters, Vol. 44, Issue: 11, pp. 665-667, 17 June 2008
- [5] “Introduction to Flip Flops: D and T,” University of Maryland, 2003, Web, 07 Apr. 2017, https://www.cs.umd.edu/class/sum2003/cmsc311/Notes/Seq/flip.html