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Overview of packaging DRAMs and use of RDL

ECG 721 – Memory Circuit Design

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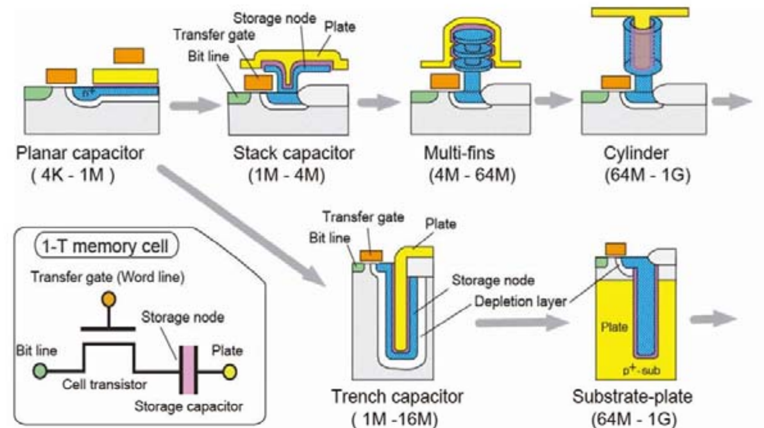
A die photograph of the Micron Technology MT4C1024 DRAM integrated circuit. It has a capacity of 1 megabit, equivalent of 2^20 bits or 128 kB [1]

What is Dynamic Random-Access Memory (DRAM)

- Random-Access… because data can be accessed in the same amount of time irrespective of their physical location
- Dynamic… because data have to be refreshed periodically

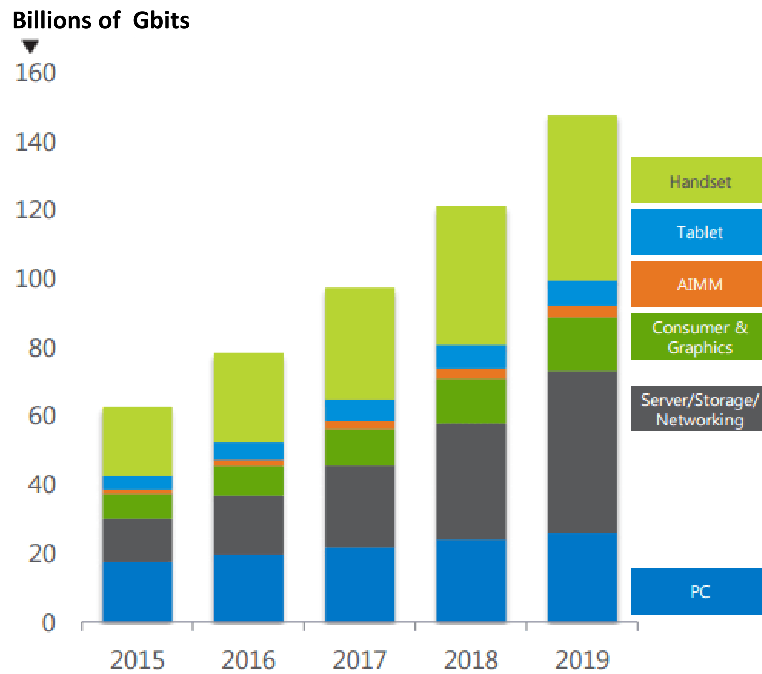
DRAM stores each bit of data in a storage cell consisting of a capacitor and a transistor (1T1C DRAM memory cell)



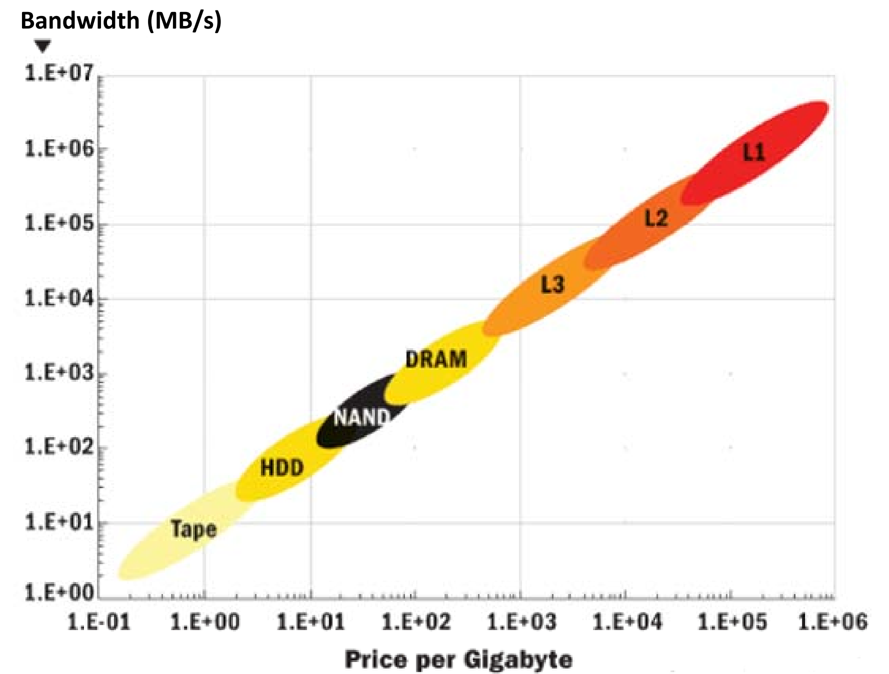
The DRAM cell (bottom left) has remained relatively the same, but the manufacturing technology has kept it competitive for decades [2]

Where is it used?

- ❑ Volatile memory
- ❑ Fast but not too expensive memory



Growing and Diversifying DRAM Demand [3]

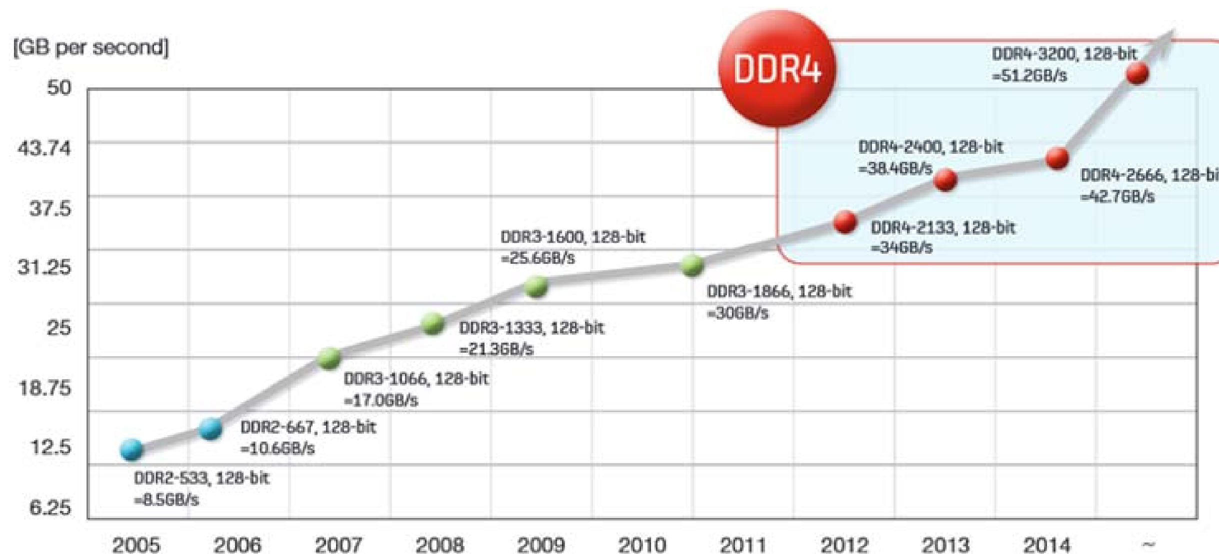


Cost vs speed in memory hierarchy [4]

DRAM types

- Asynchronous DRAM
- Synchronous DRAM (SDRAM)
  - Single Data Rate (SDR)
  - Double Data Rate (DDR)

  Samsung has begun mass production of **10-nm** class, **8-Gbit DDR4** DRAM chips, which support speeds up to **3.2GT/s** (equal to 51.2GB/s) [5]



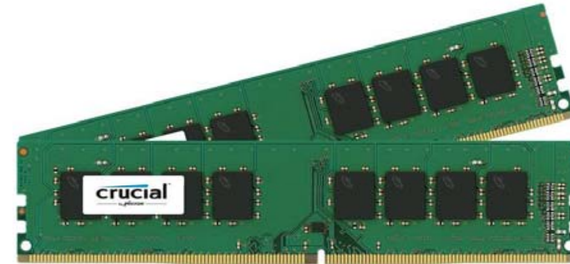
DDR4 high speed performance compared with DDR3 and DDR2 [5]

DRAM modules

- Single Inline Memory Module (SIMM)
  - early 80s to late 90s
  - 32-bit data path (72 pins)

From top to bottom: SIMM (30-pin), SIMM (72-pin) [5]

- Dual Inline Memory Module (DIMM)
  - contacts on both sides
  - 64-bit data path
  - 288-pins used for DDR4 SDRAM



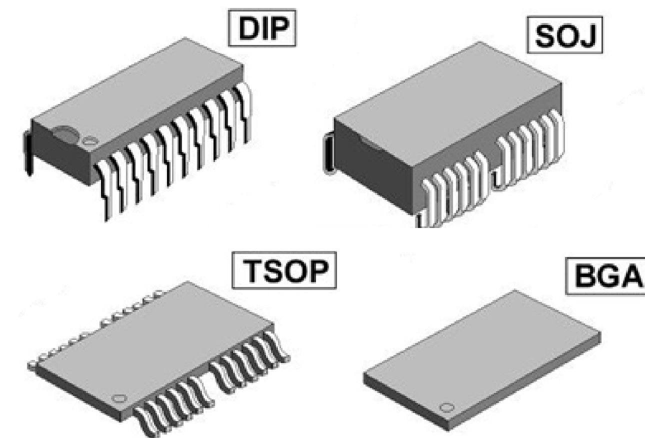
Crucial 16GB Kit (8GBx2) DDR4 2133 MT/s
UDIMM 288-Pin Memory (Amazon.com - $102.99)

- Small outline DIMM (SoDIMM)
  - 260-pins used for DDR4 SDRAM

Crucial 16GB Kit (8GBx2) DDR3/DDR3L 1866 MT/s
SODIMM 204-Pin Memory (Amazon.com - $89.99)

Why packaging?

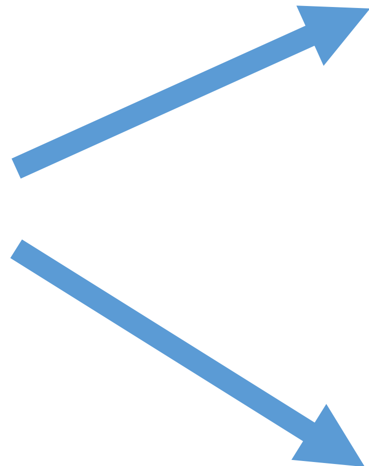
- Protection
  - Physical damage
  - Environmental damage
- Electrical connections
  - Redistributes I/O
- Heat dissipation
  - Transfer via convection
  - Increased surface area

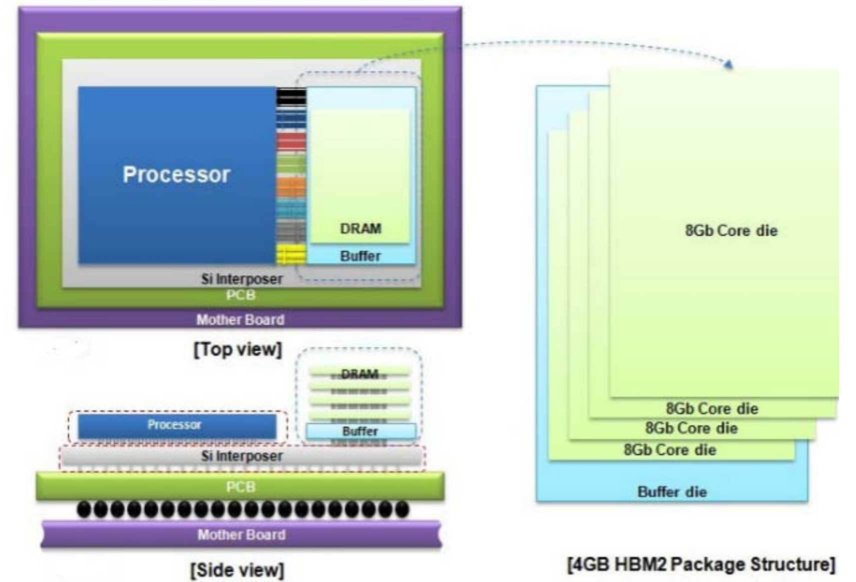


DRAM package evolution [6]

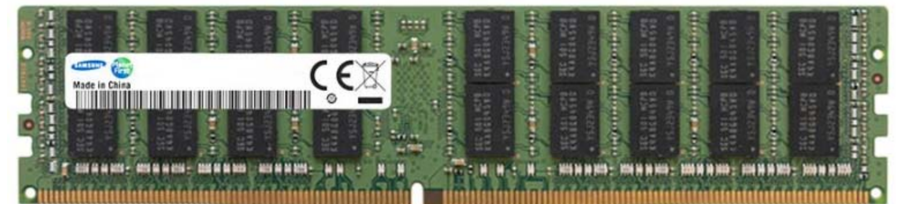
DRAM packaging in time

Intel 1101: The first MOS memory chip (July 1969). A 1024-bit DRAM, that made Intel a world leader in memories for a decade [7]



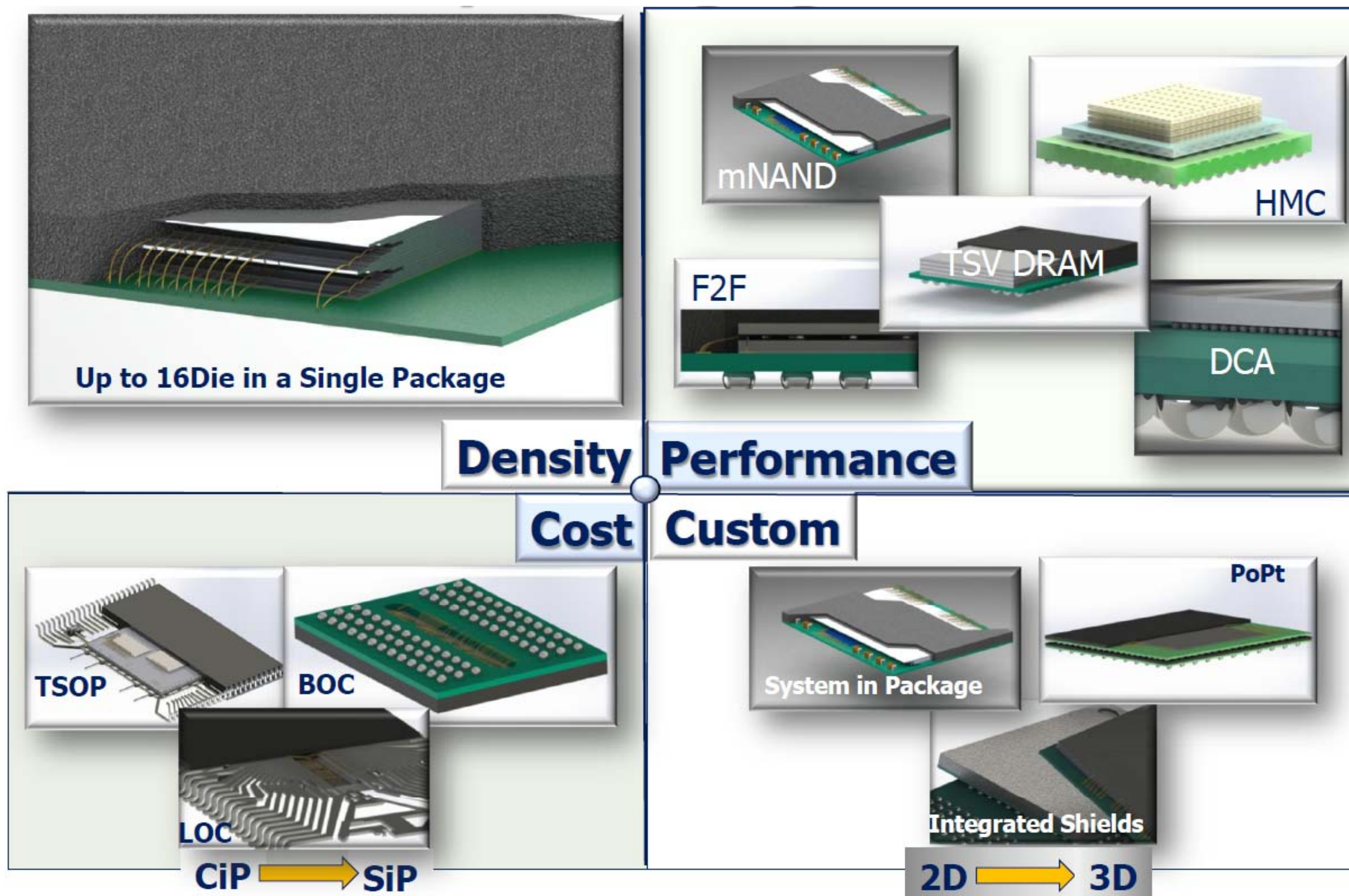


Samsung: World's fastest (Jan. 2016), mass produced DRAM, for HPC and graphics cards. 4GB HBM2 package structure – 4H x 8Gb dies – 256GB/s **speed** [8]



Samsung: World's largest capacity and highest energy efficiency (Nov. 2015), mass produced DRAM. 128GB TSV DDR4 RDIMM – 36 x (4H x 8) Gb dies – 2.4GB/s speed [9]

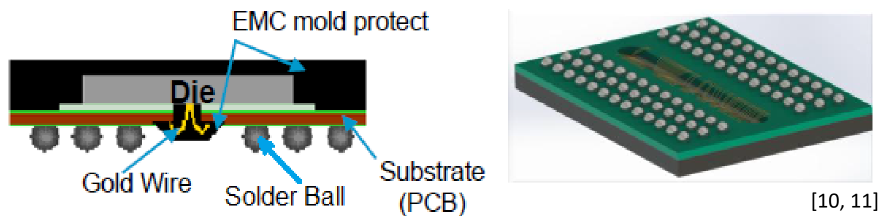
Memory Packaging Tradeoffs



Memory packaging tradeoffs [10]

DRAM Packaging Terminology and Stacking Technologies

- ❑ Number of identical die in package.
  - ❖ SDP, DDP, 3DP, QDP
- ❑ **Re-Distribution Layer (RDL)**, routes edge to center, where DDR dies have the wire-bond sites
- ❑ Fine Pitch Ball Grid Array (FBGA)
  - ❖ Board On Chip (BOC)



[10, 11]

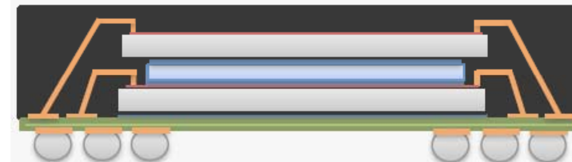
  - ❖ Chip on Board (COB) or Face-Up without RDL

Challenges: gold wire cost, cost of Film-over-Wire material/process, thermals [12]

  - ❖ Opposing-Face without RDL

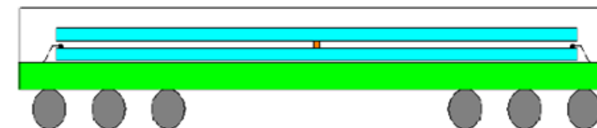
Challenges: gold wire cost, unbalanced signal length, thermals [12]

  - ❖ Face-Up with RDL



Challenges: RDL cost, thermals [12]

  - ❖ Face-to-Face (F2F) with RDL

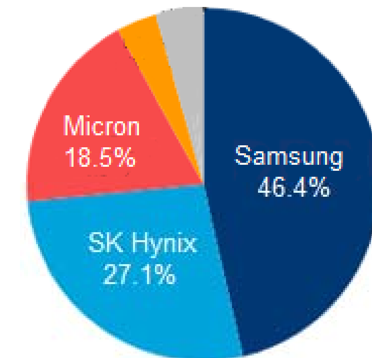


Challenges: RDL cost, thermals [10]

- ❑ Direct Chip Attach (DCA)
- ❑ Through Silicon Via (TSV)

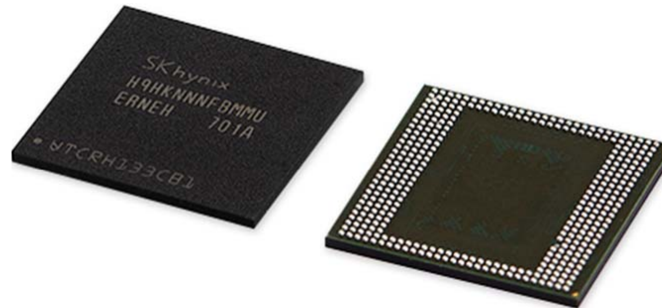
DRAM packages in market today

- DDR4 (Server, PC, Consumer*)
  - 78, 96 FBGA, 96 TFBGA,
  - 2 and 4-die stacks using TSV (Samsung – Server DRAM)
  - 1 and 2-die stacks not using TSV (Samsung – Server DRAM)
  - Up to 8-die stacking capability (Micron)
- LPDDR4 (Smartphones, Tablets)
  - 196, 200, 272, 344, 366, 376 FBGA
  - 1 and 2-die stack (Micron)
  - Up to 8 GB of mobile DRAM in a single package (Samsung)
  - SK Hynix announced (Jan. 17) industry's first 8 GB LPDDR4X package, using 4-die stack, for mobile devices
- GDDR5 (Graphic)
  - 170, 190 FBGA



1Q16 Branded DRAM Market Share by Manufacturer [13]

Samsung DDR4 promo shot – 78 FBGA [5]

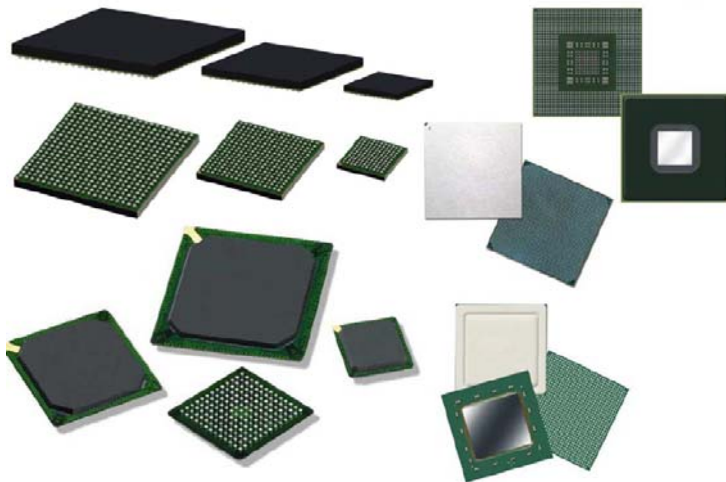


SK Hynix 8 GB LPDDR4 – 376 FBGA [14]

*Consumer applications include: smart TV, digital cameras, set top box, gaming console

FBGA packages

Thin Small-Outline Package (TSOP) for DDR SDRAM [15]



Fine-pitch Ball Grid Array (FBGA) Packages [16]

Code	Name	Dimension
E	Enlarged	≥1.50mm
Blank	Standard	≥1.00mm and <1.50mm
F	Fine	<1.00mm
	F1 Fine	= 0.80mm
	F2 Fine	= 0.75mm
	F3 Fine	= 0.65mm
	F4 Fine	= 0.50mm
	F5 Fine	= 0.40mm
	F6 Fine	= 0.30mm

Ball Pitch Dimensions and Code (JESD30E) [17]

Code	Subcode	Profile Description	Profile Height
–	B2	Extra thick	>3.50mm
–	B1	Very thick	>2.45mm and ≤3.50mm
B	–	Thick	>2.45mm
Blank	–	Standard	>1.70mm and ≤2.45mm
L	–	Low	>1.20mm and ≤1.70mm
T	–	Thin	>1.00mm and ≤1.20mm
V	–	Very thin	>0.80mm and ≤1.00mm
W	–	Very, very thin	>0.65mm and ≤0.80mm
U	–	Ultra thin	>0.50mm and ≤0.65mm
X	–	Extremely thin	≤0.50mm
–	X1	Extra-thin	>0.40mm and ≤0.50mm
–	X2	Super-thin	>0.30mm and ≤0.40mm
–	X3	Paper-thin	>0.25mm and ≤0.30mm
–	X4	Die-thin	≤0.25mm

BGA Maximum Package Height Profile (JESD30E) [17]

FBGA packages: Features and Benefits

- ❑ High density

  Samsung FBGA packages [18]:

  Up to 600 balls (I/Os)

  package size: 5x5mm to 19x19mm

  thickness: 0.8 – 1.4mm

- ❑ Chip Scale Package (CSP)

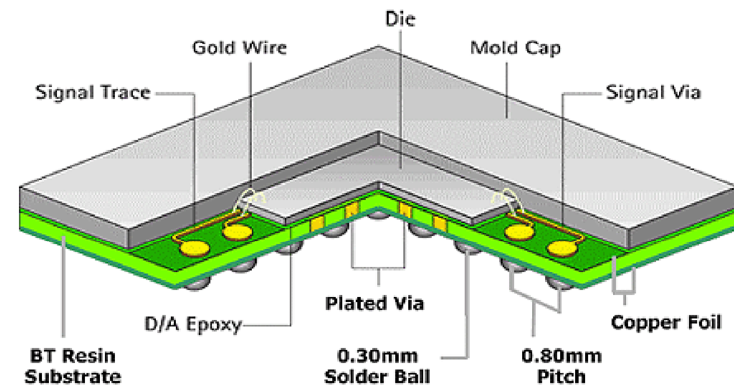
  package size ≈ die size

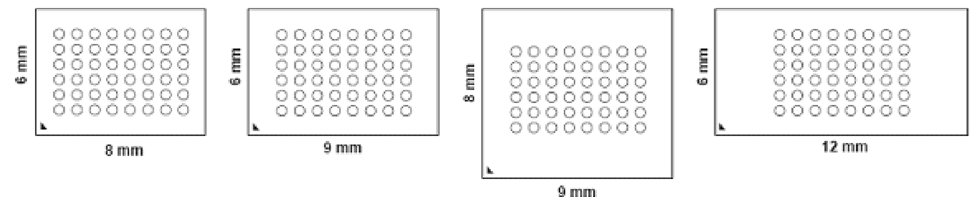
- ❑ Better heat dissipation

  thermal vias, thermal balls

- ❑ Low-inductance leads

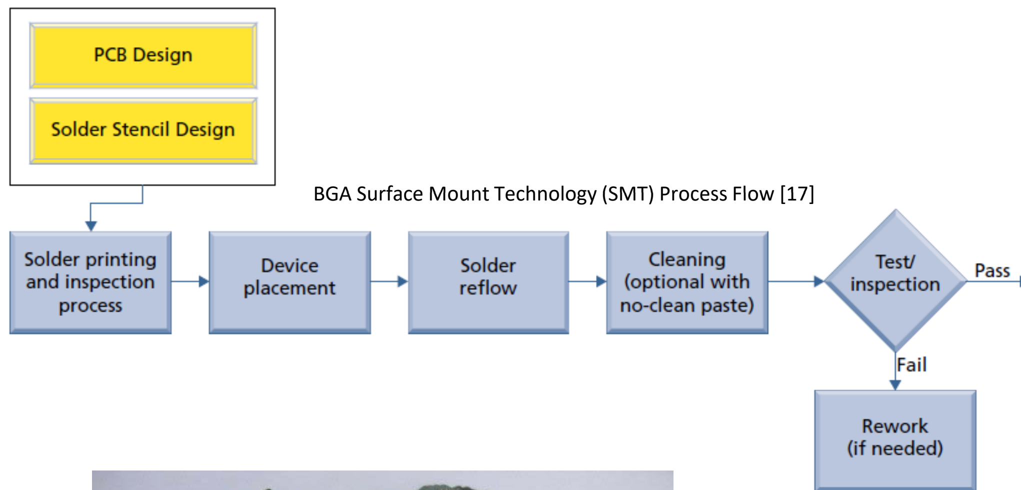
- ❑ Soldering requires precision





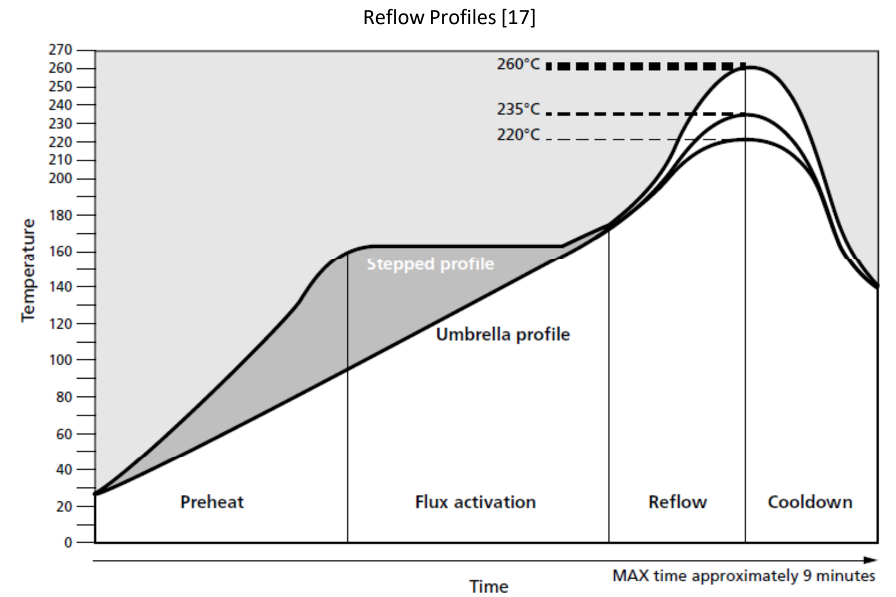
FBGA sample with different form factors [19]

BGA Surface Mount Technology (SMT)

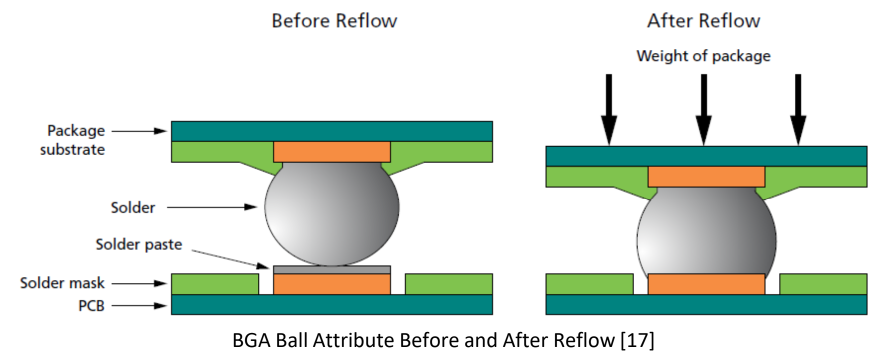


BGA Surface Mount Technology (SMT) Process Flow [17]

Reflow Profiles [17]



BGA stencils in different shapes and sizes [20]



BGA Ball Attribute Before and After Reflow [17]

Why stacking?

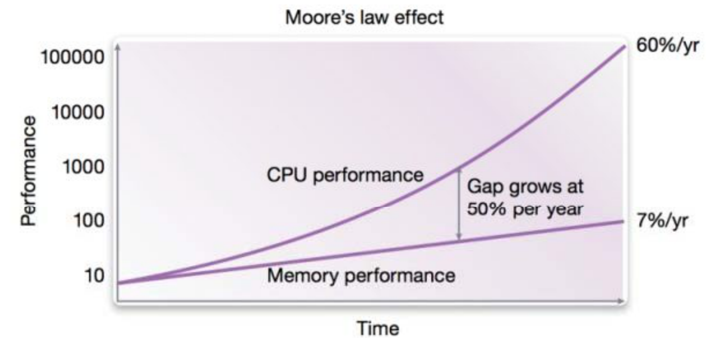
- "Memory wall", "Memory Bottleneck"
  - "Hitting the Memory Wall: Implications of the obvious" (1995) [21]
- Increased package density (capacity)
- Shorter paths => speed

But…

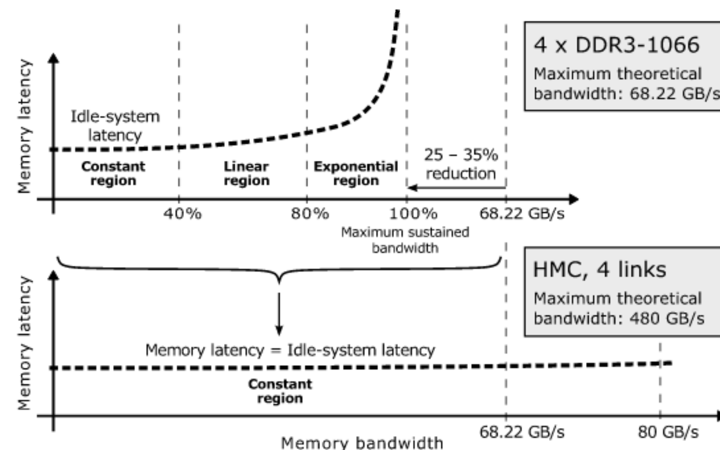
- "Another Trip to the Wall" (2015)
  - Skepticism about both latency and bandwidth [22]

$$effective\ bandwidth \propto \frac{outstanding\ memory\ requests}{memory\ latency}$$

- In-memory processing, sophisticated memory controller functionality



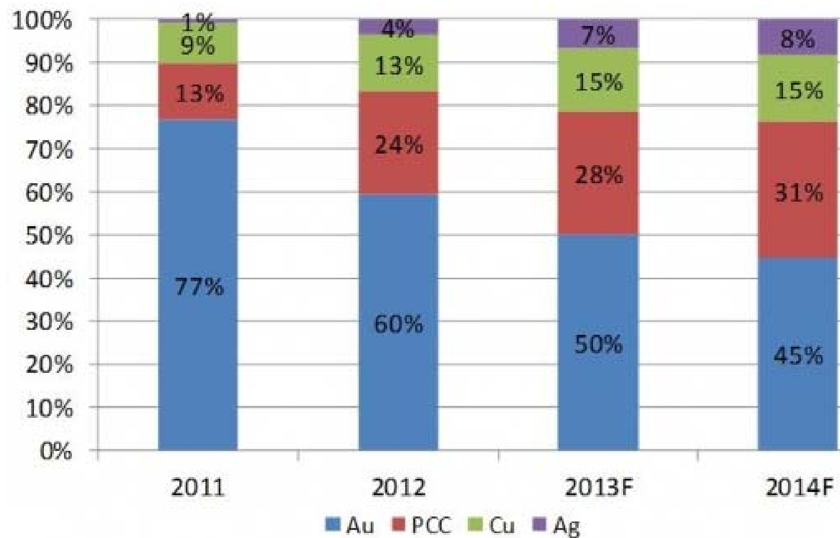
The gap between memory and CPU performance [23]



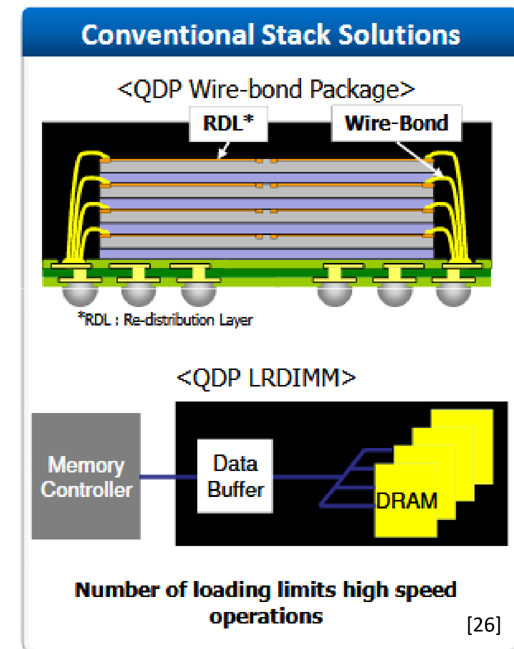
Bandwidth-latency curves of DDR3 and HMC systems [23]

Wire bonding

- Materials (Micron, 2010) [24]:
  - Pads: Nickel-Palladium (NiPd) and Aluminum (Al)
  - Wires: Gold (Au)
- ~80% of IC packages

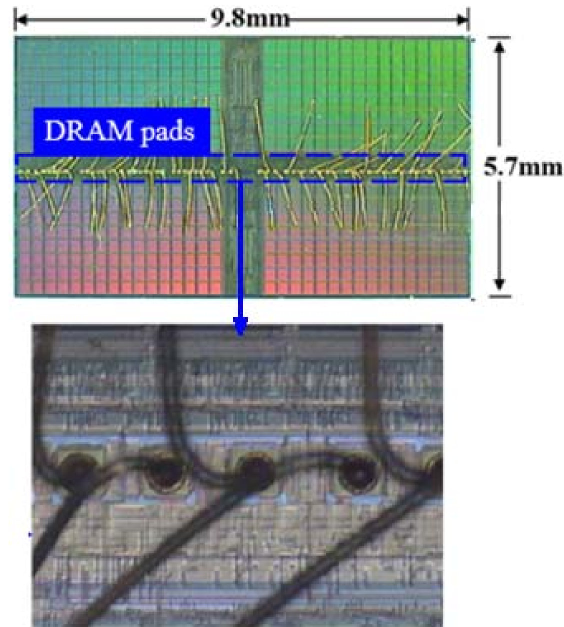


Percentage Share of Wire Shipped by Material Type [25]



Redistribution Layer (RDL)

- Metal and dielectric layers on the surface of the die to route the pads to the edges

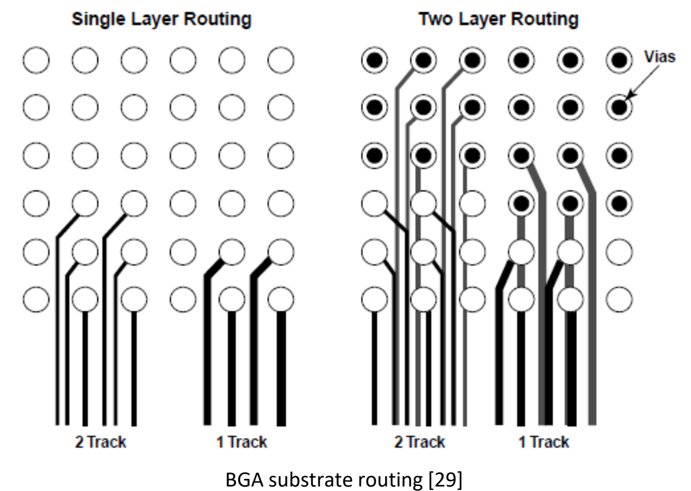


Commercial DRAM chip after decapsulation (top). Enlarged view of DRAM pads (bottom) [27]

1. Dielectric Deposition
2. Mask , Etch Dielectric
3. Metal Deposition
4. Mask , Etch Metal
5. Dielectric Deposition
6. Mask , Etch Dielectric
7. NiAu plating

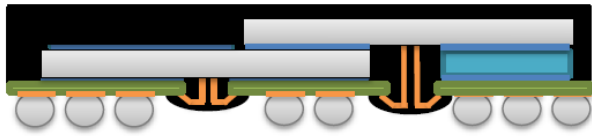
Wafer-Level RDL process [28]

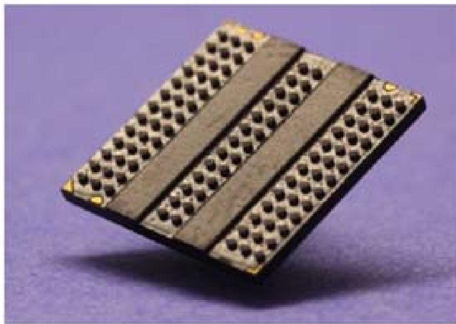
- Substrate routing to connect signals from die(s) to solder balls

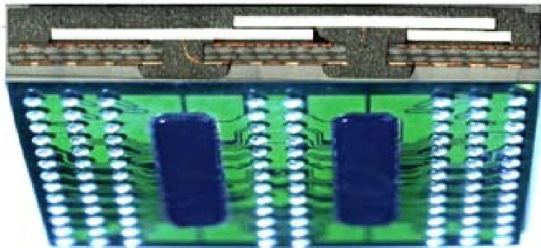


BGA substrate routing [29]

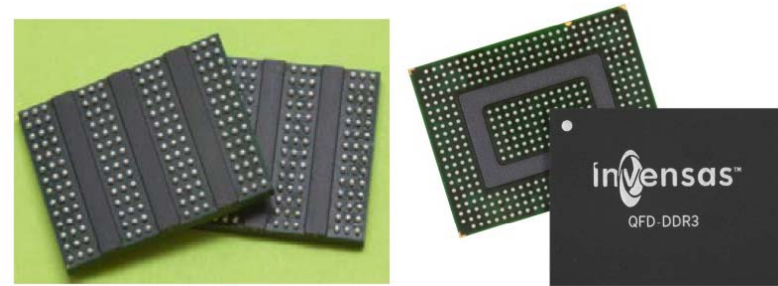
Invensas' no RDL approach



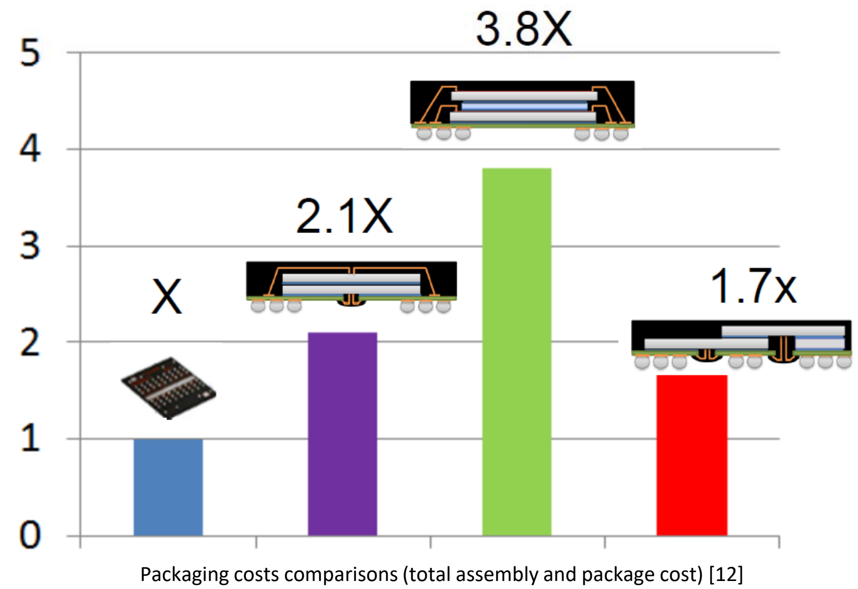




Invensas' Dual Face Down package (DFD) [12]



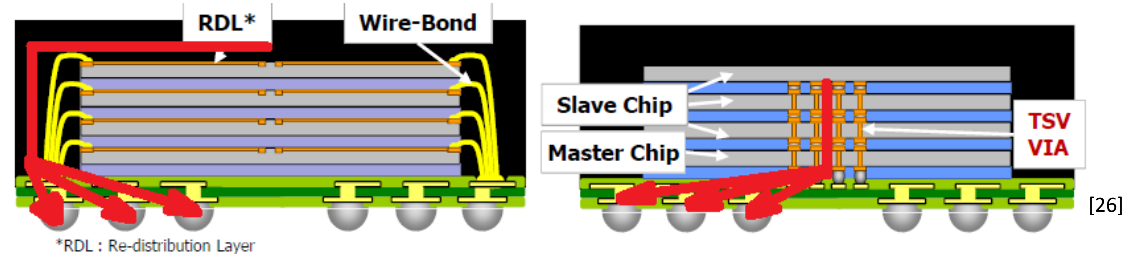
Invensas' Tri-Face Down (TFD) and Quad-Face Down (QFD) packages [30]



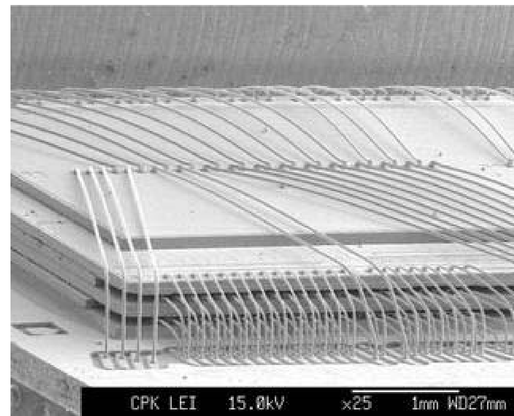
Packaging costs comparisons (total assembly and package cost) [12]

Wire Bonding vs TSV

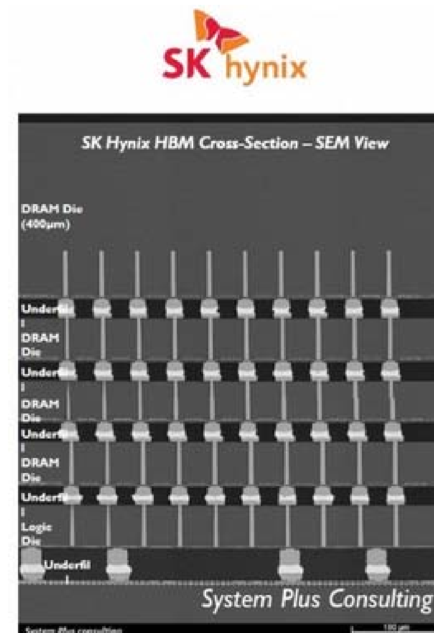
- Shorter distance
  - Reduced RC Delays
  - Lower power consumption
- More space for interconnections
  - Wider buses
  - Increased bandwidth
- Lower profile
  - No spacers
- Heat dissipation
  - Less power
  - Through vias

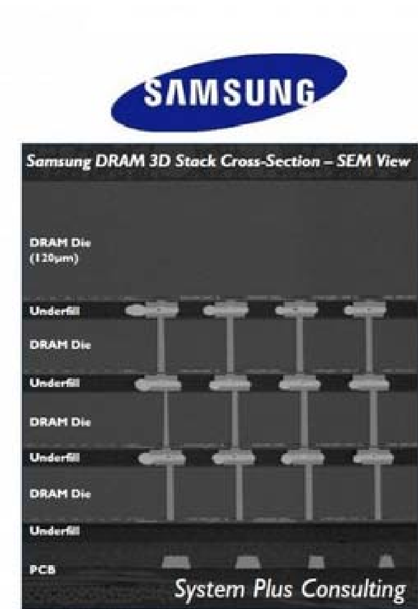


[26]



Stacked die package with 4 dies and 2 spacers [31]

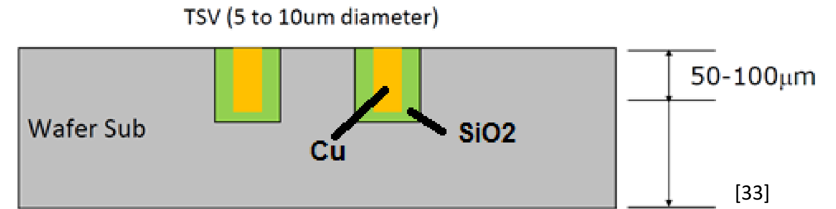


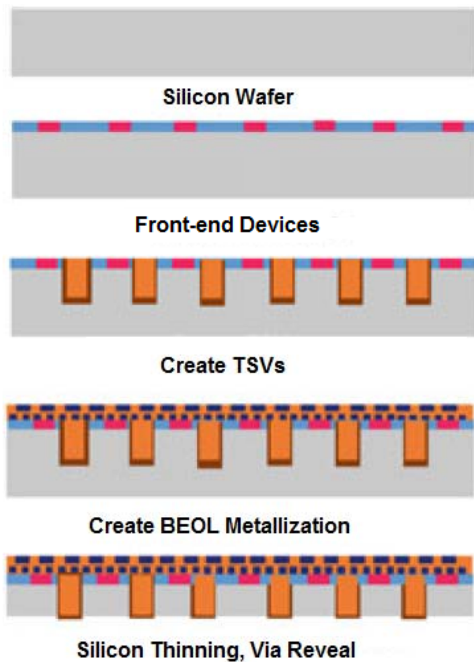


[32]

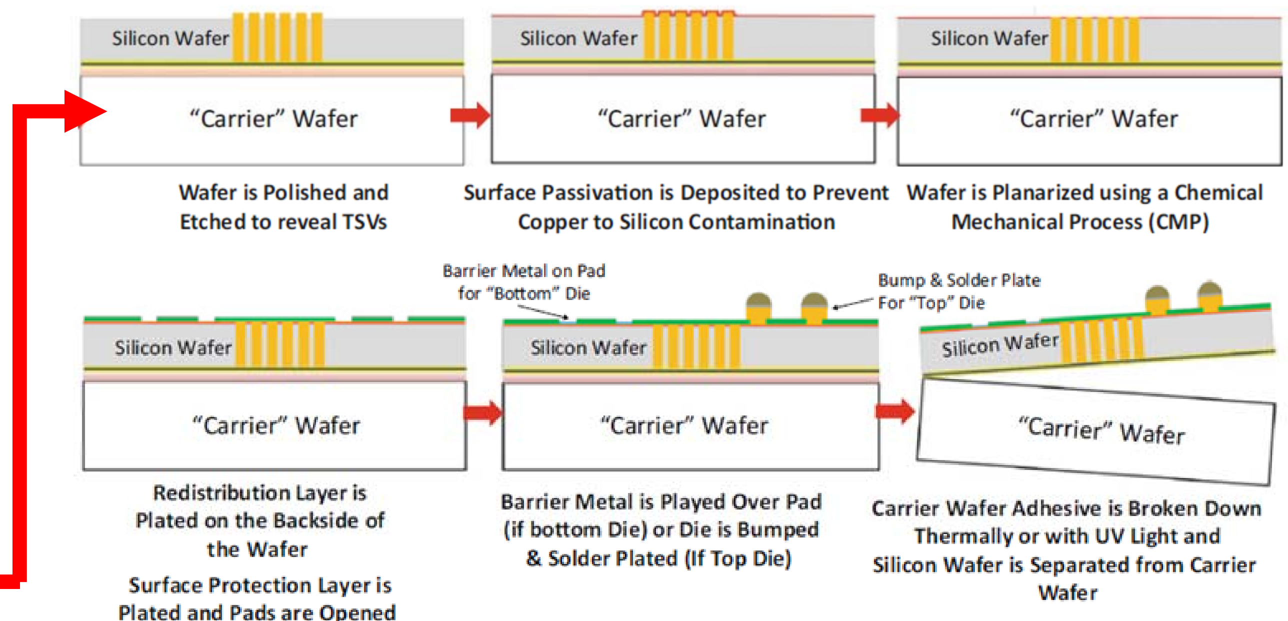
TSV process flow

- Wafer thinning and thin wafer handling make die stacking manufacturing feasible [33]





Via Middle TSV process [34]



Bumping process flow post TSV formation [34]

What's next?

- More dies stacked together
  - HBM3 promises stack heights > 8
  - Increased bandwidth and density
- DRAM on the same package as CPU
  - Intel will add 16 GB of Multi-Channel DRAM (MCDRAM) on CPU package

Intel's Knights Landing CPU architecture integrates high-performance, on-package memory directly onto the CPU package [35]

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Questions?