Use of an over-damped PLL in place of DLL in SDRAM

Presented by
Sachin P Namboodiri
SDRAM clock synchronization

- Clock skew: timing difference between input and output interfaces
  - Caused by internal buffers and long interconnect

- Crucial in high speed I/O operation

- Clock synchronization circuit is essential to solve the above issues

- Both DLL and PLL are good to synchronization
Clock Synchronization

A PLL/DLL is necessary to reduce the skew and improve the timings for the on-chip and inter-chip operations.
Why Delay Locked loop (DLL)?

• Simple
  – Passing the signal through a delay element

• More stable
  – First order system
  – Process and temperature variation effects are minimal

• Jitter Performance
  – No Jitter circulation
  – However, input jitter will get passed as there is no filtering
Delay locked loop (DLL)

Fig 1. Delay Locked loop Block diagram [2]
PLL vs DLL

- Second order system
- Stability issues
- Frequency lock
- Phase alignment by VCO
- Jitter accumulation

- First order system
- Stable
- No frequency multiplication
- Phase alignment by VCDL
- No jitter accumulation

Courtesy: [2]
Phase error (DLL vs PLL)

![Graph showing phase error vs time for DLL and PLL with different bandwidths.]
PLL Components in a nutshell

• PFD: Generates a digital signal depending to the phase error
• CP: Digital error signals converted to analog error current
• LPF: Integrates the error current to generate VCO input voltage
• VCO: Oscillator with the frequency depending on the input voltage.
PLL Transfer Function

• Closed loop transfer function

\[ H(s) = \frac{K_{PD} K_F K_{VCO}}{s + \beta K_{PD} K_F K_{VCO}} \]

  – Low pass filter wrt input reference signal

• Error transfer function

\[ H_e(s) = \frac{s}{s + K_{PD} K_F K_{VCO}} \]

  – High pass filter wrt to noise signal
Second order PLL

• Reduced second order transfer function

\[ H(s) = \frac{2\zeta w_n s + w_n^2}{s^2 + 2\zeta w_n s + w_n^2} \]

• Where
  – \( w_n \) is the natural frequency
  – Zeta is the damping factor

• Underdamped: Damping factor < 1
• Critically damped: Damping factor = 1
• Overdamped: Damping factor > 1
Damping factor and natural frequency

\[ w_n = \sqrt{\frac{K_{PDI}K_{VCO}}{NC_1}} \quad \zeta = \frac{w_n}{2} RC_1 \]

- \( w_n \) is the frequency at which the system oscillates at zero damping
- Set by the resistors and capacitors of the loop filter
- PLL can be stable or unstable depending on the damping factor
- Stability effects phase error (Jitter) and settling time
Stability of a PLL

- Second order system
- Stability depends on the damping factor
- Adding zero
- PFD must sample faster
  - Discrete time stability limit (Gardner’s limit)[5,6]

\[ w_n^2 < \frac{w_{ref}^2}{\pi (R_{max} C_1 w_{ref} + \pi)} \]

- Increasing damping factor has limit
Transfer function vs Damping factor

- Gain overshoot at low damping factor
  - Errors will re-circulated and amplified
- Flattens out as damping factor increases

- Gain overshoot at the higher damping factor due to stability limit (Gardner limit)
- Good Compromise – damping factor = 1
Transfer function vs Damping factor

PLL Transfer Function (Phase Out/In) vs. Damping

![Graph showing PLL transfer function vs damping factor with various damping factors D=0.1 to D=5.0]

Courtesy: [3]

ECG 721 MEMORY CIRCUIT DESIGN
0.5 < Damping < 2

PLL Phase Transfer Function (FB/Ref) vs. Damping

DB

0.00

-5.00

-10.00

-15.00

-20.00

-25.00

w_{mod}/w_n

0.01

0.10

1.00

10.00

100.00

D=0.5
D=0.7
D=1.0
D=1.5
D=2.0

Courtesy: [3]
Phase response Vs damping

• Transient simulation for phase step

• Overshoot and ringing for under-damped systems

• Minimal overshoot and ringing for critically damped

• Overshoot and fast ringing for over-damped systems
  – Due to Gardner’s limit
Phase response

Phase Response (\(T_{ref}/T_{step}\)) to 8 nS Ref Phase Step

Normalized Time (\(wn^t\))

Terr/Tstep

D=0.5
D=0.7
D=1.0

Courtesy: [3]
Phase response

Phase Response (\(T_{ref}/T_{step}\)) to 8 nS Ref Phase Step

Normalized Time (\(wn^*t\))

\(D=1.0\)
\(D=1.5\)
\(D=2.0\)
\(D=3.0\)

Courtesy: [3]
Other key parameters of PLL

- **Hold range**: Frequency range that the PLL can track without losing lock
- **Lock range**: Frequency range at which the loop recapture the lock within one cycle
- **Lock time**: Time taken for PLL to lock during the lock in process
- **Pull in range**: Frequency range in which the loop can acquire a lock
- **Pull in time**: Time taken for PLL to lock during the pull in process
Noise in PLL

• Types of noise
  – Flicker noise: Caused by silicon interface traps
  – Thermal noise: Caused by random Brownian motion of carriers in a resistive medium

• Noise in PLL components
  – Charge Pump: Flicker and thermal
  – Loop Filter: Mostly thermal
  – VCO: Mostly thermal
  – VCO Bias: Flicker and thermal
Some Noise parameters

• Signal to noise ratio:

\[ SNR = \frac{P_s}{P_n} \]

• Noise Bandwidth \((B_L)\):

\[ B_L = \frac{w_n}{2} \left( \zeta + \frac{1}{4\zeta} \right) \]
Noise Bandwidth vs Damping factor

Courtesy: [7]
Phase noise (Jitter)

- Jitter: A short term timing variation from its ideal position

\[ V_{out}(t) \propto \sin\left(2\pi f_{out} t + \phi_n(t)\right) \]

Courtesy: [3]
Jitter measurement

- **Phase Jitter**
  - Deviation of VCO output edges from ideal placement in time
- **Period Jitter**
  - Deviation of VCO period from the ideal period
  - Derivative of phase Jitter wrt time
- **Cycle to cycle Jitter**
  - Change in VCO period from cycle N to cycle N+1
- **TIE(Time interval error)**
  - Time difference between total of N consecutive actual VCO cycle and N ideal cycles
Phase error vs Bandwidth and Damping factor

\[ \phi_{\text{error}} \propto \sqrt{\frac{1}{\zeta \cdot BW}} \]

**Fig. 4.** Long-term jitter (due to VCO noise) sensitivity to: (a) loop bandwidth and (b) loop damping factor.

Courtesy: [4]
Jitter reduction

- Increase frequency
- Increase the gate area of the transistors
- Increasing the power dissipation
- Choosing number of stages at VCO
  - More stages can reduce noise
- Differential delay buffer as a stage in VCO
- Self biased techniques to track process and temperature variation
Conclusion

• Major advantages of PLL
  – Input noise filtered
  – Can generate frequencies

• Can we use overdamped PLL instead of DLL in SDRAM?
  – Yes. But not recommended

• Disadvantages
  – Stability
  – Jitter accumulation
  – Higher pull in time
  – Must tract frequency input
Reference


Thank you!