Tutorial: Digital Delay-Locked Loop Design In SDRAM

ERIC MONAHAN
University of Nevada, Las Vegas
ECG721 Memory Circuit Design
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What is a Delay-Locked Loop (DLL)?

- A dynamic, variable delay circuit used to synchronize the signals between a memory controller and a synchronous memory device.

- Why use a DLL in Synchronous DRAM (SDRAM)?

  DLL generates a delayed clock signal that synchronizes the output data with the system clock.

What is SDRAM?

- Asynchronous DRAM = uses timing
- Synchronous DRAM = uses a synchronous clock to execute commands
- All commands/data executed on edges synchronous with system clock
- Initial SDRAM was Single Data Rate (SDR), then Double Data Rate (DDR) and DDR2, DDR3, DDR4 and developing DDR5

DDR SDRAM Architecture

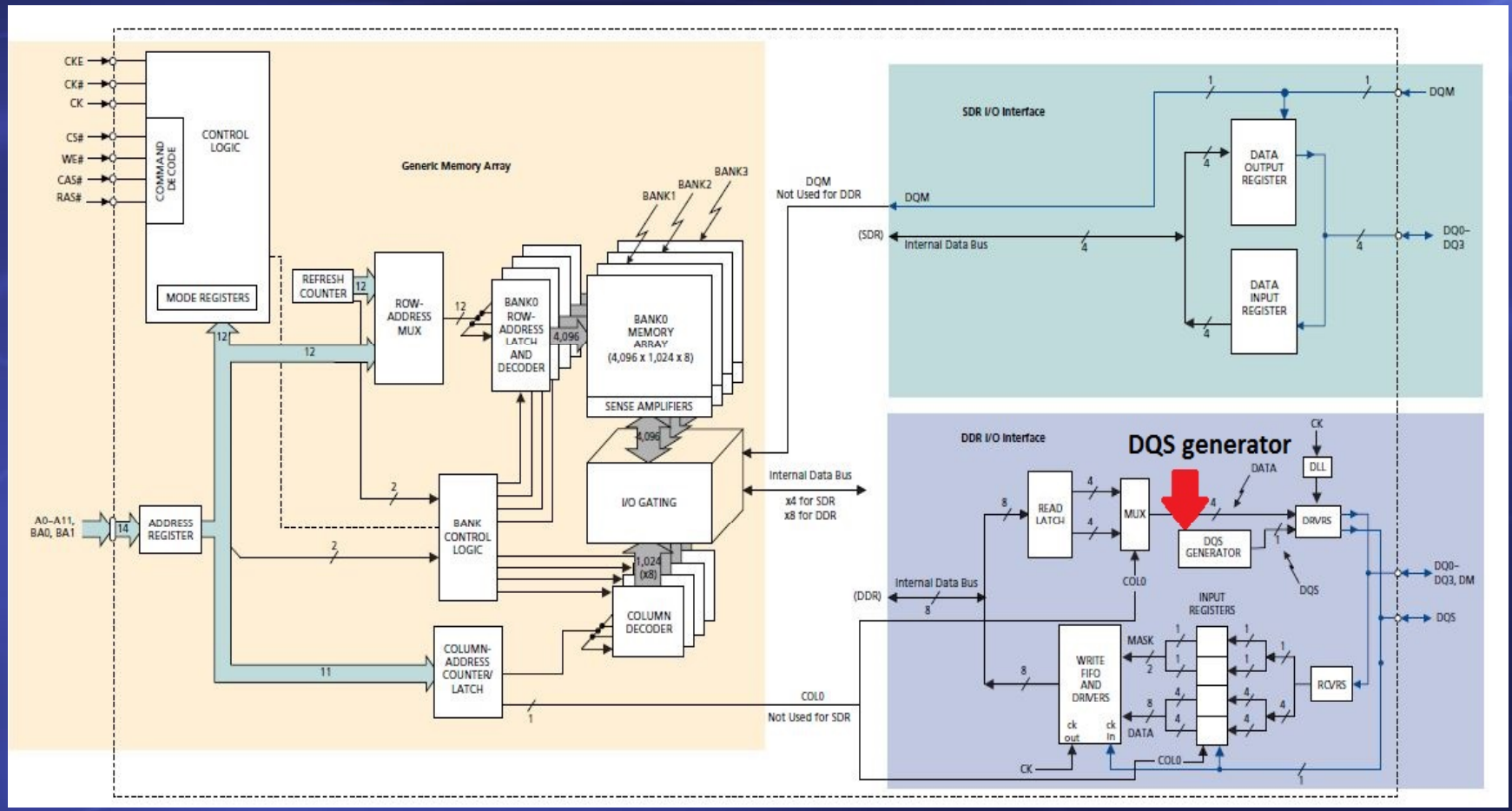


Figure 1 2MEG x 4 Memory Array with SDR and DDR Interface [1]

DDR Read Example

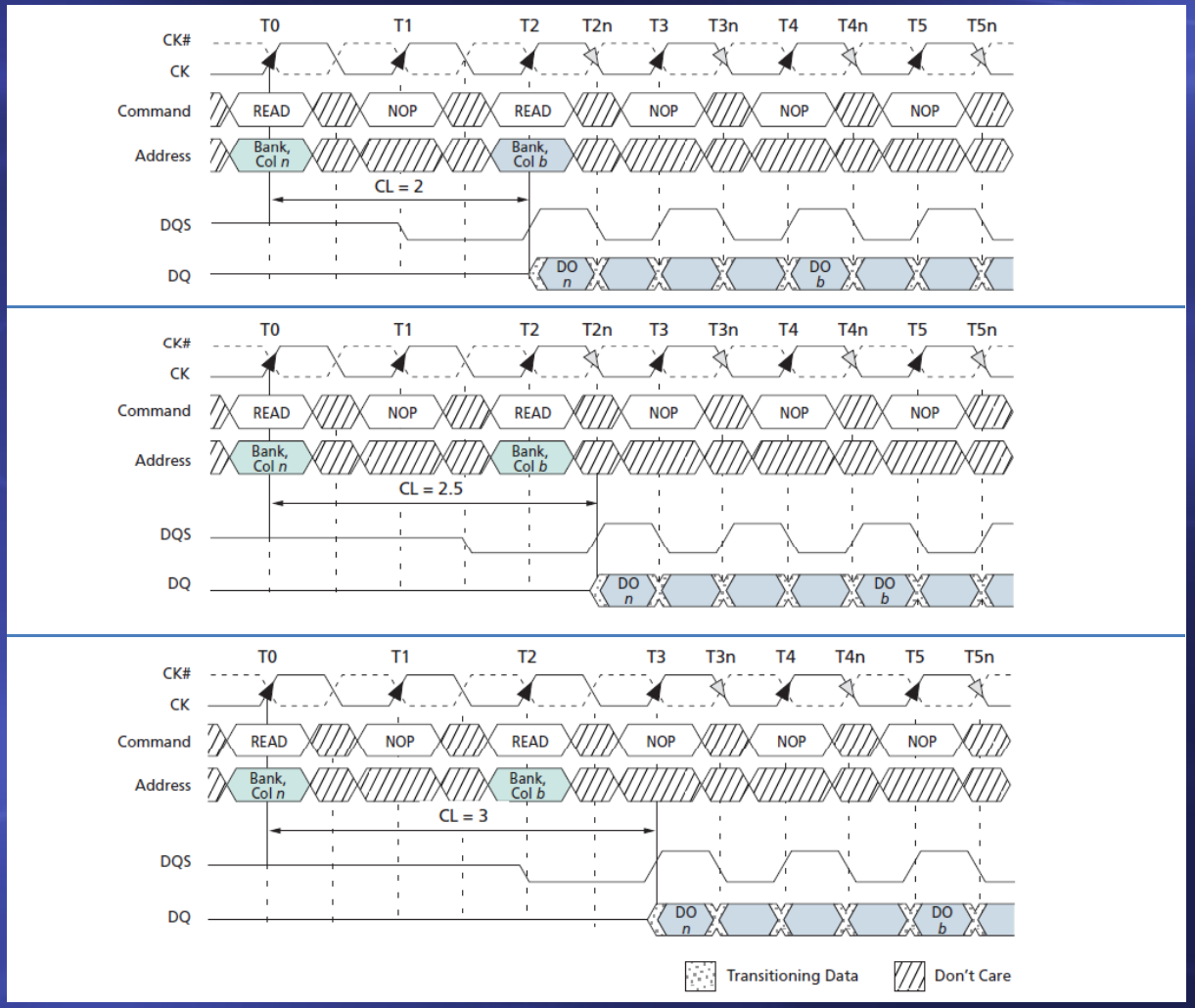


Figure 2 SDRAM CAS latency [2]

SDRAM DQS Signal

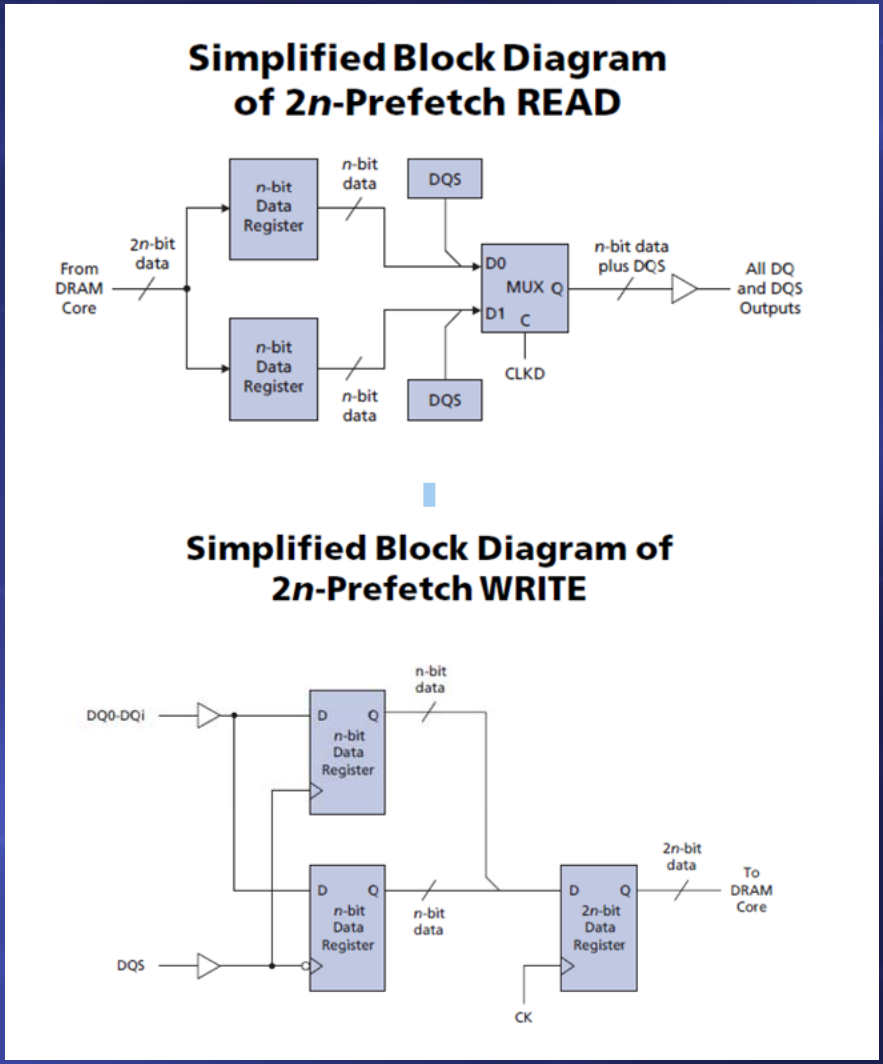


Figure 3 Prefetch READ and WRITE Block Diagrams [1]

Relating CLK to DQS

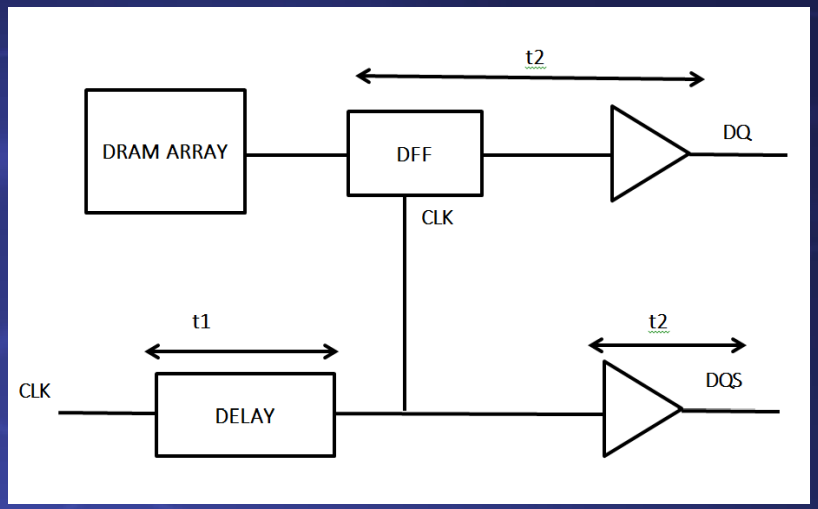


Figure 4

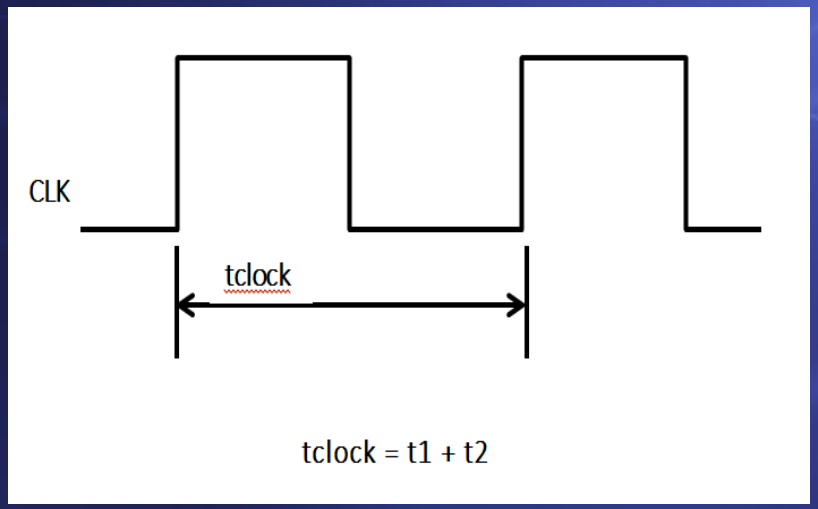


Figure 5

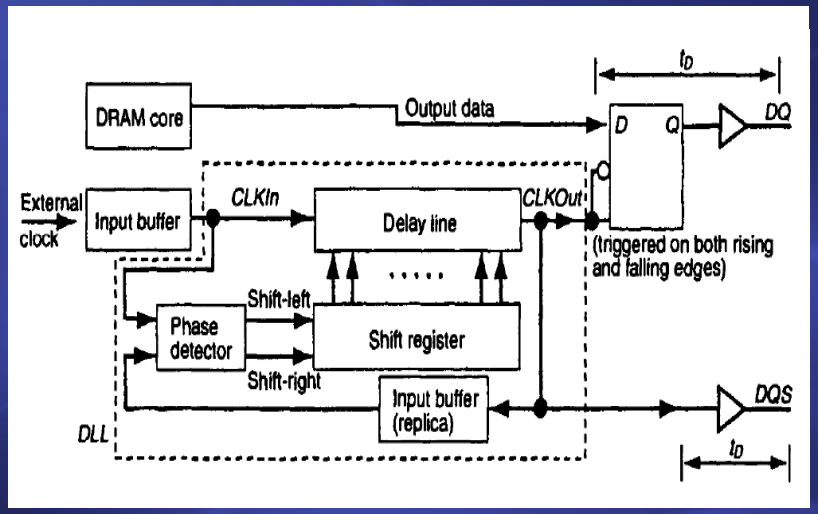


Figure 6 Block Diagram for DDR SDRAM DLL [3]

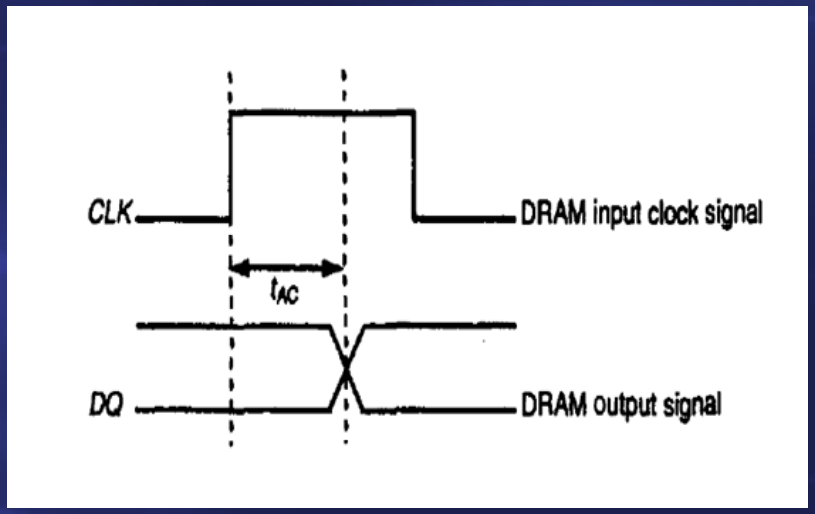


Figure 7 SDRAM CLK input and DQ output [3]

Advantages of Digital DLL

- Minimum delay is a known, quantized step
- Short locking time
- Zeroth order transfer function makes DLL easier to stabilize than alternatives, such as a PLL.
- Low clock skew
- Maintains lock even if clock stops

DLL Basics

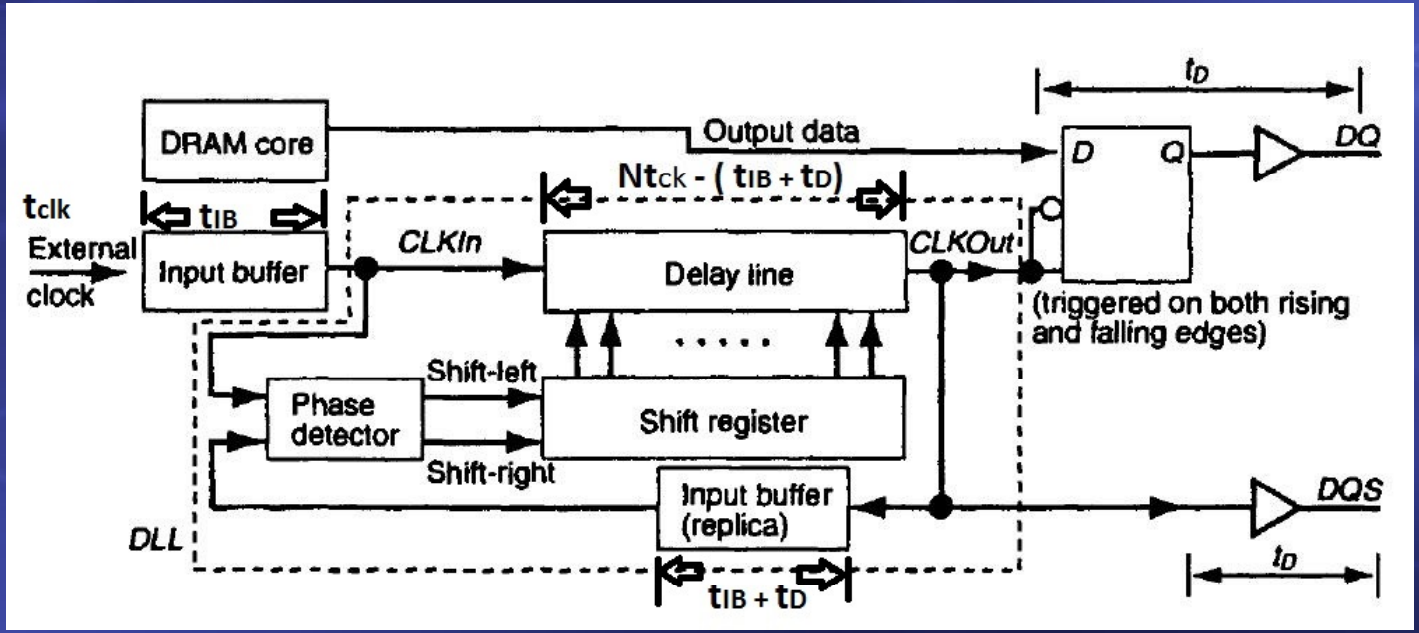


Figure 8 Block Diagram for DDR SDRAM DLL [3]

- Input Buffer
- Delay Line
- Feedback with Delay Model
- Phase Detector
- Shift Register

- PD loop dely = $N*t_{clk}$
- $t_{clk} = t_{IB} + t_D$
- tIB and tD subject to PVT variations
- Delay line = $N*t_{clk} – (t_{IB} + t_D)$
- Ideal forward delay =
  $t_{IB} + N*t_{clk} – (t_{IB} + t_D) + t_D = N*t_{clk}$

Design Considerations

- PVT variations
- False lock
- Duty Cycle at 50%
- Jitter

I/O Buffers and Feedback Delay Model

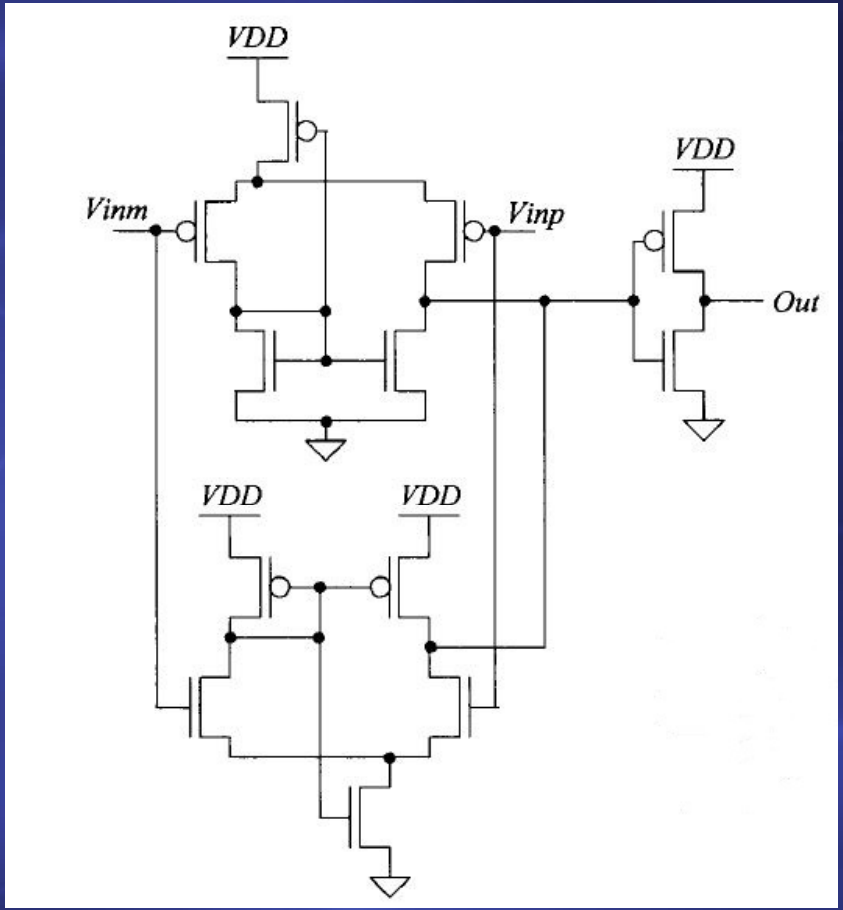


Figure 9 Rail-to-rail input buffer [4]

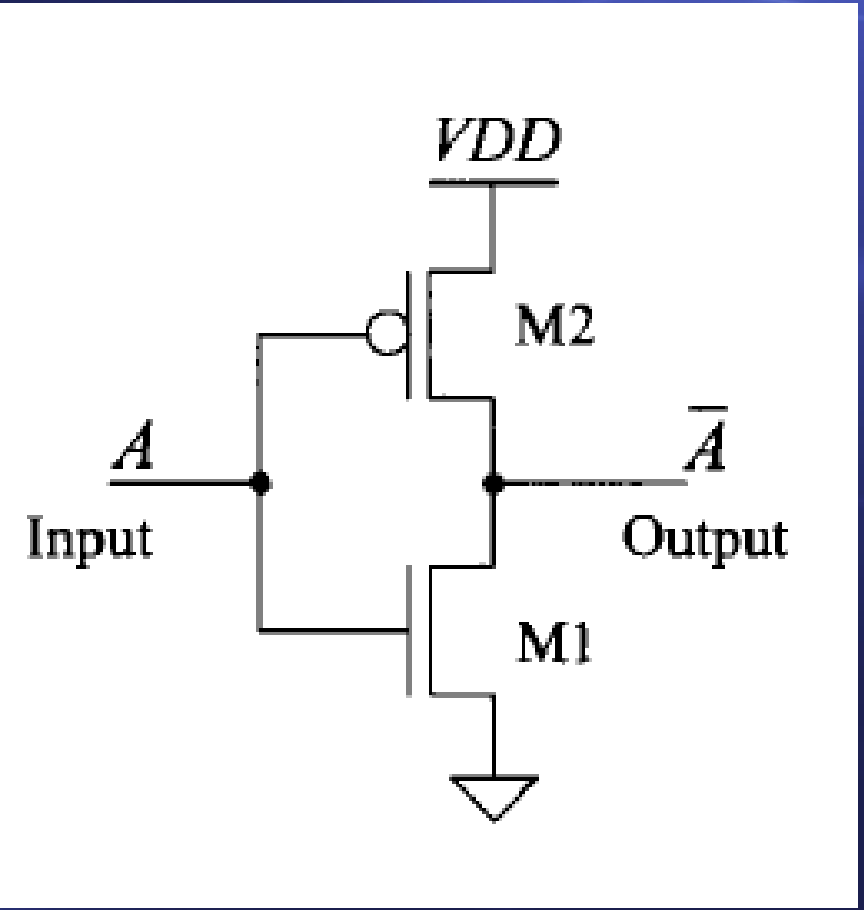
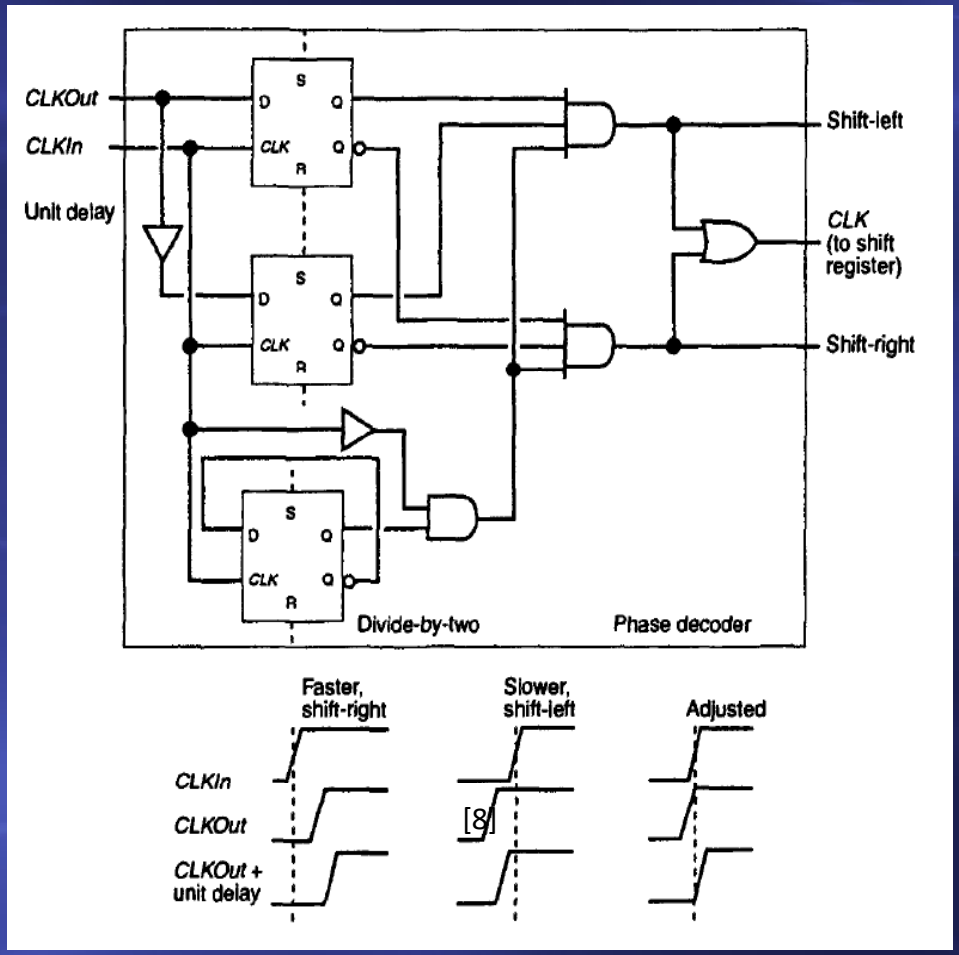


Figure 10 CMOS Inverter [4]

Phase Detector



[8]

[12]

Figure 11 Phase Detector Circuits [5]

Voltage Controlled Delay Line (VCDL)

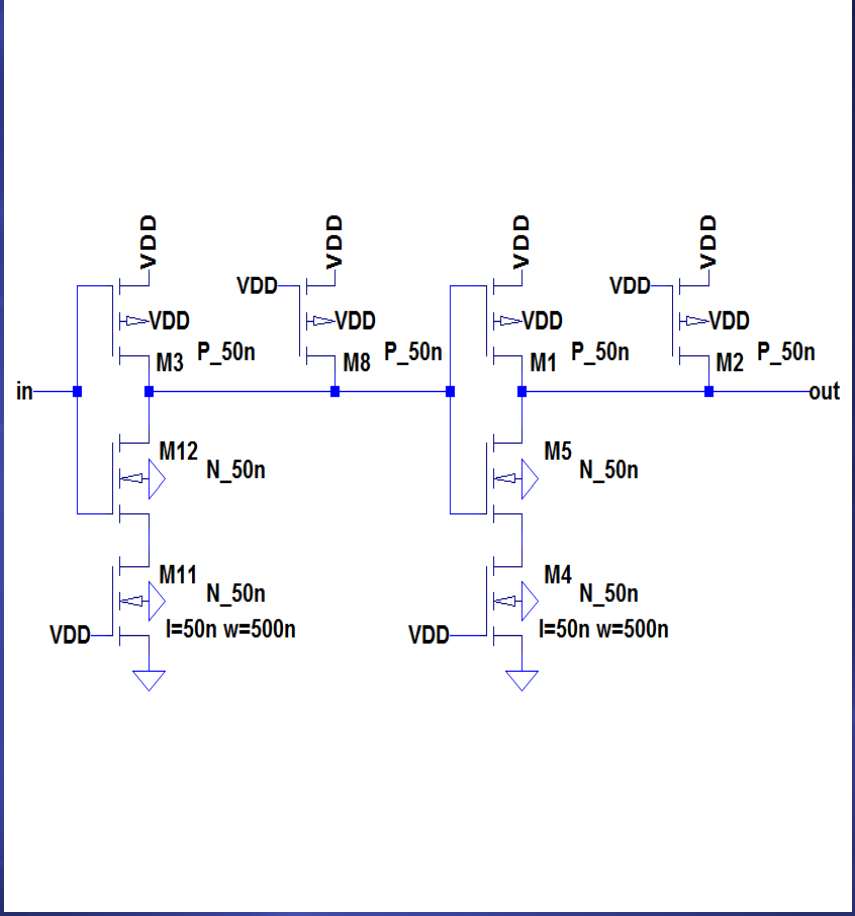


Figure 12 Coarse Delay with NAND Pair [4]

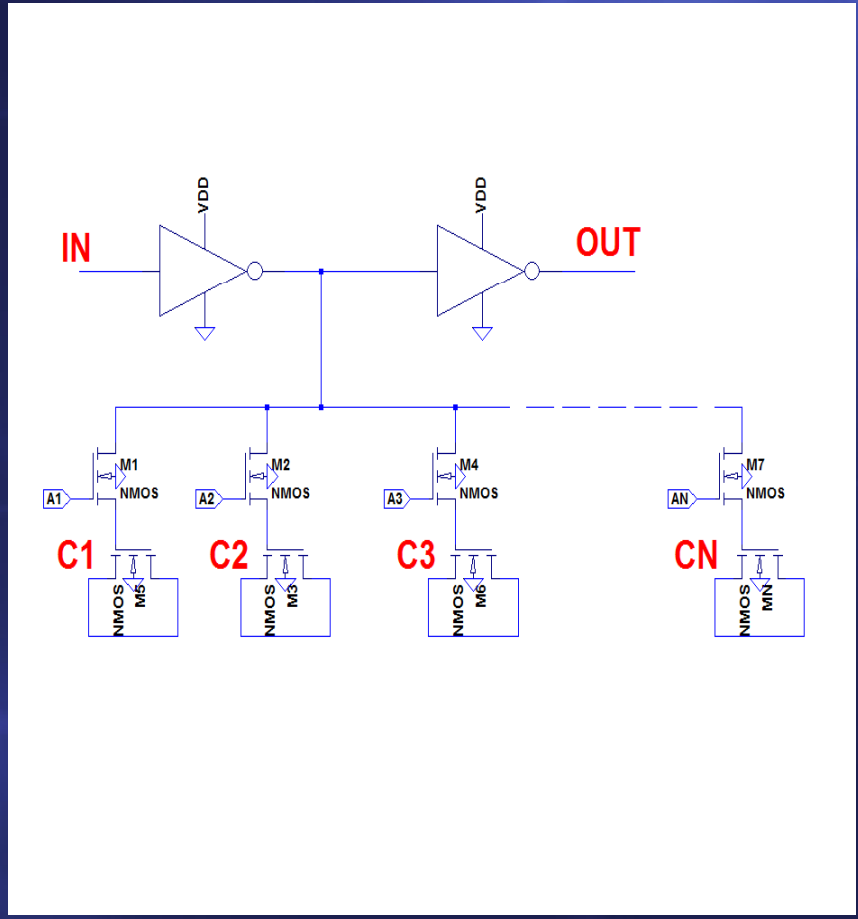


Figure 13 SCI based Fine Delay [6]

Clock Insertion via Shift Register

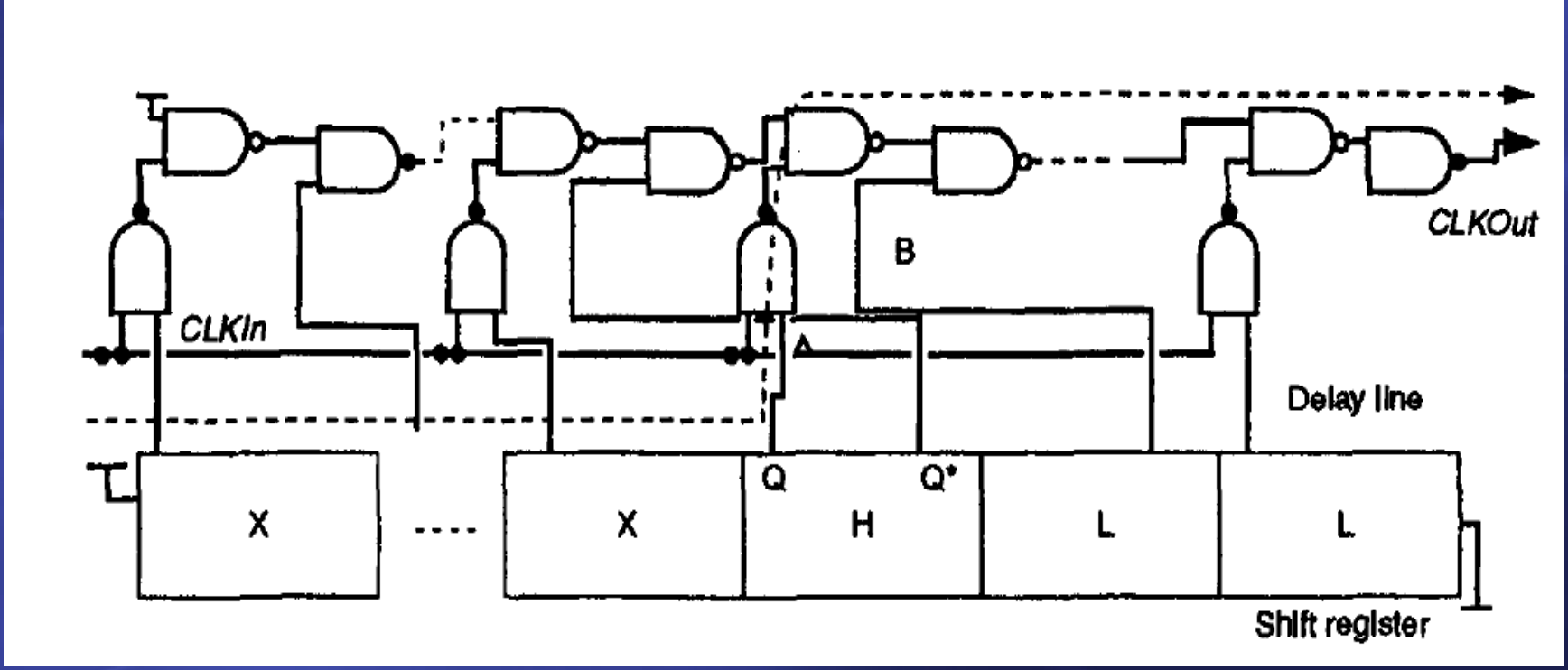
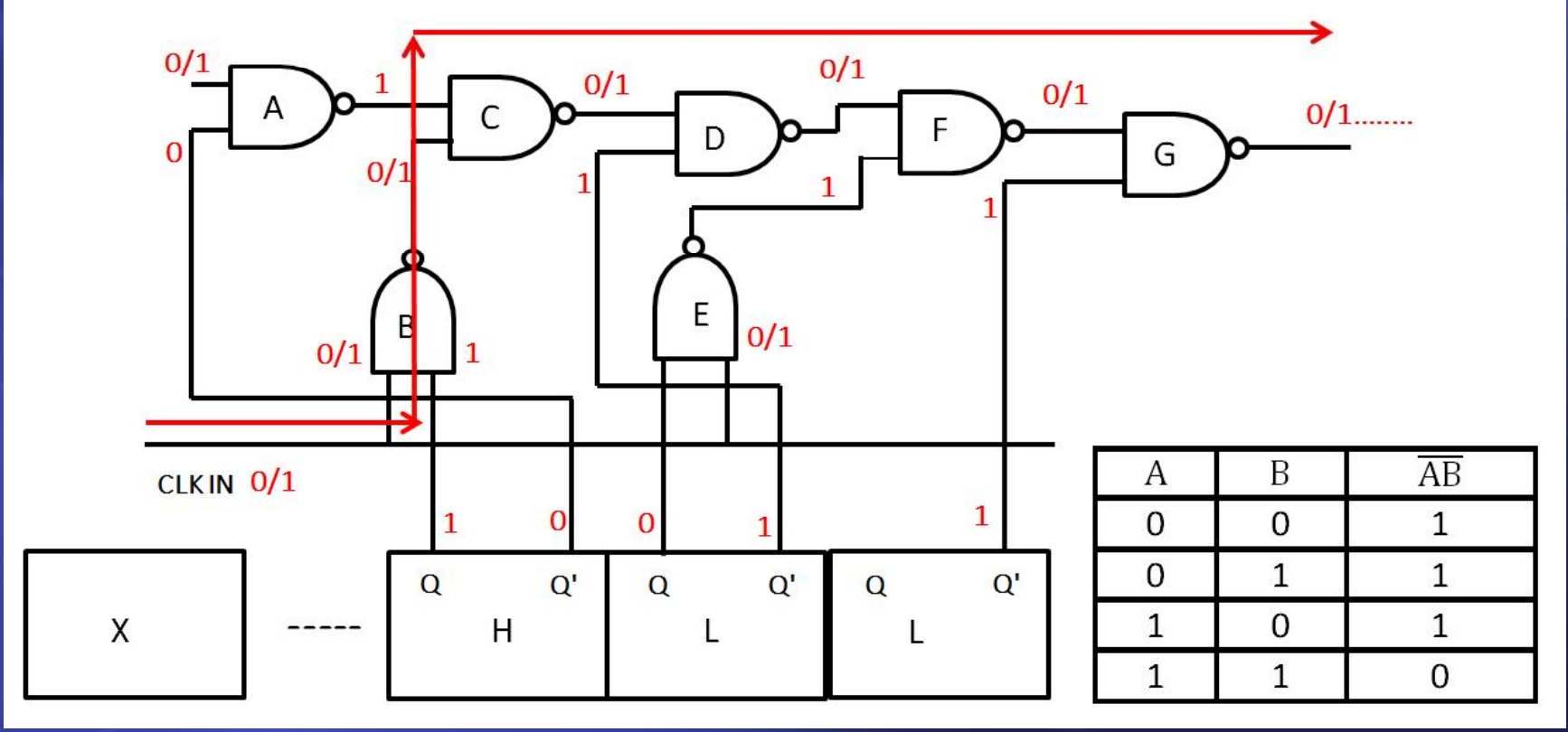


Figure 14 Delay Line and Shift Register [5]

Clock Insertion Example



A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

Figure 15 Delay line and shift register clock insertion example [5]

Delay Line Control Variations

Counter

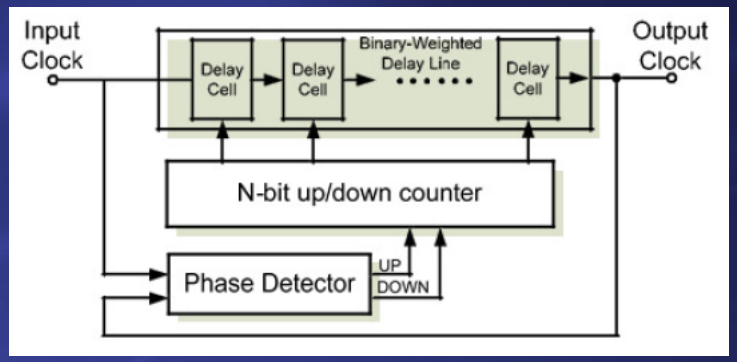


Figure 16 Counter Controlled DLL [7]

Time-to-Digital Converter (TDC)

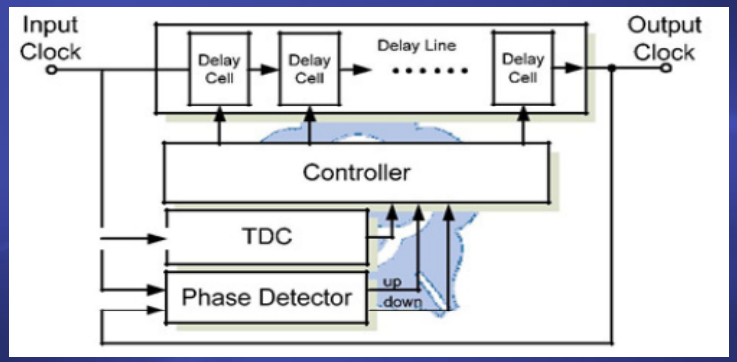


Figure 17 TDC Based DLL [7]

Successive Approximation Register (SAR)

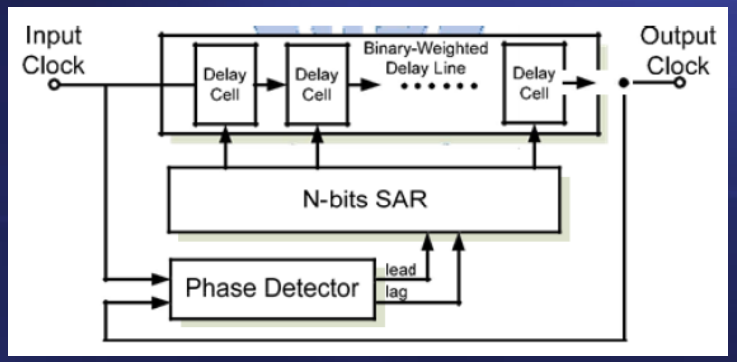


Figure 18 SAR Based DLL [7]

SAR Basics

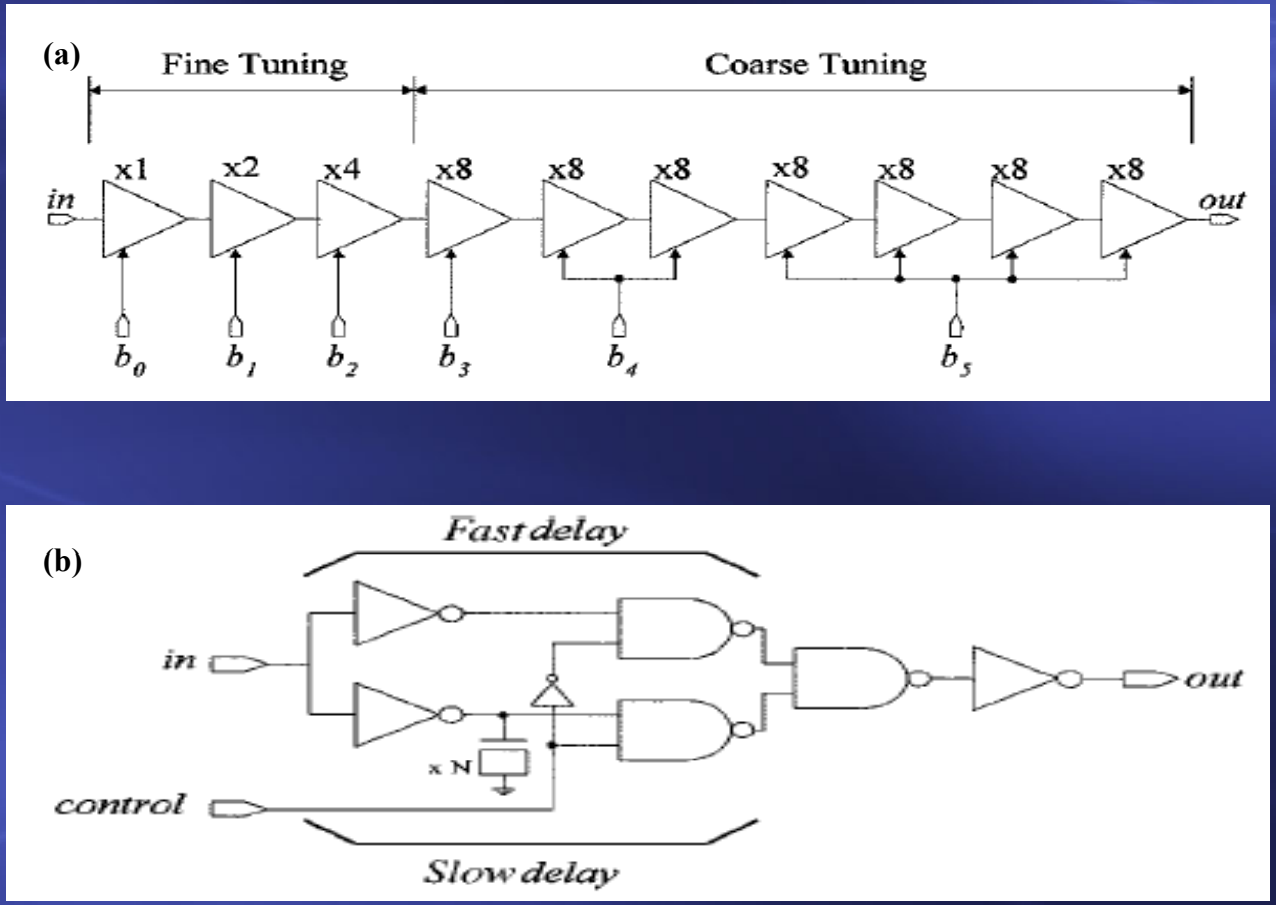


Figure 19 (a) Binary-weighted digital delay line (b) Delay cell [8]

SAR Operation

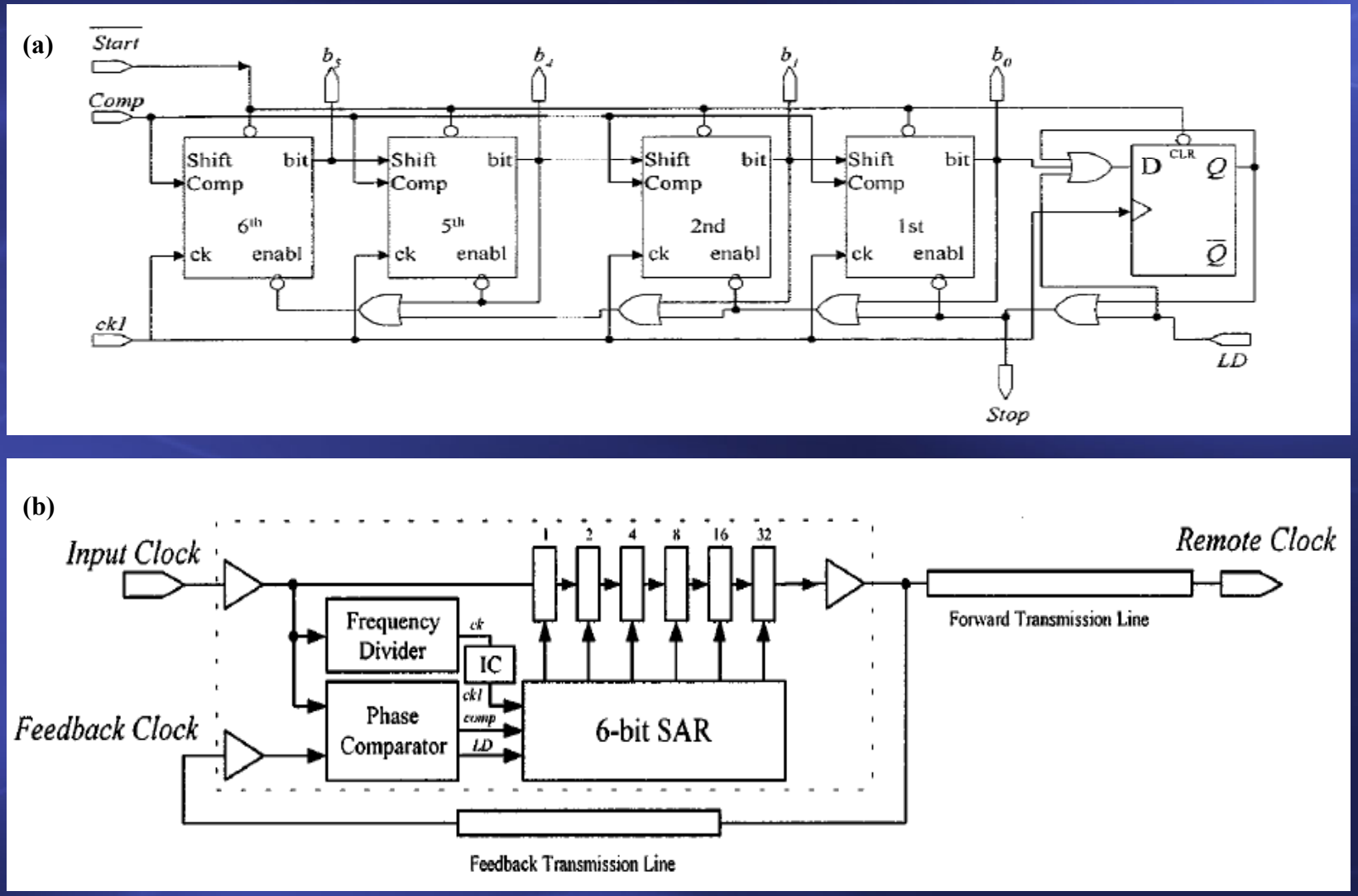


Figure 20 (a) 6-bit SAR (b) Example SAR Circuit [8]

Alternate SAR based DLL

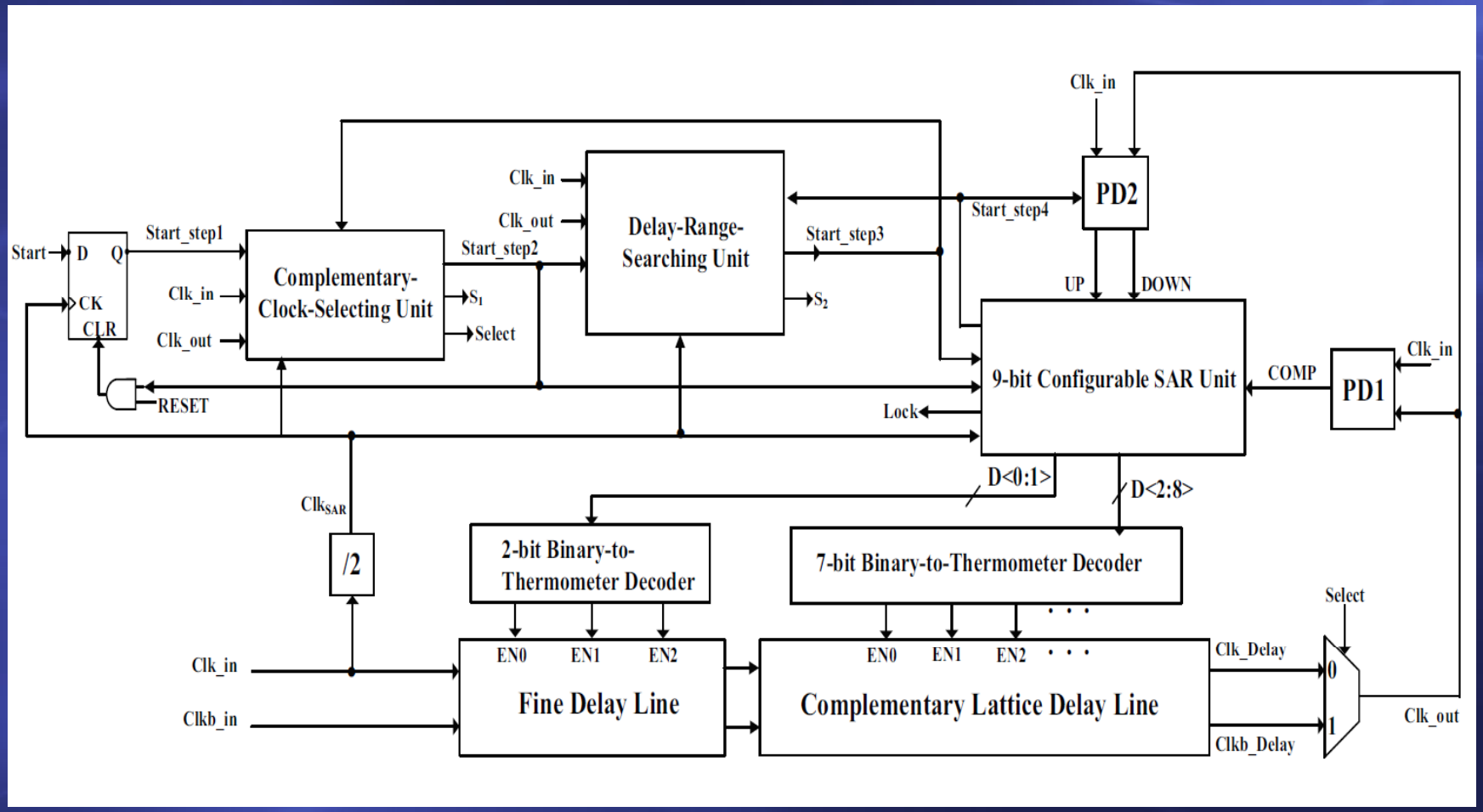
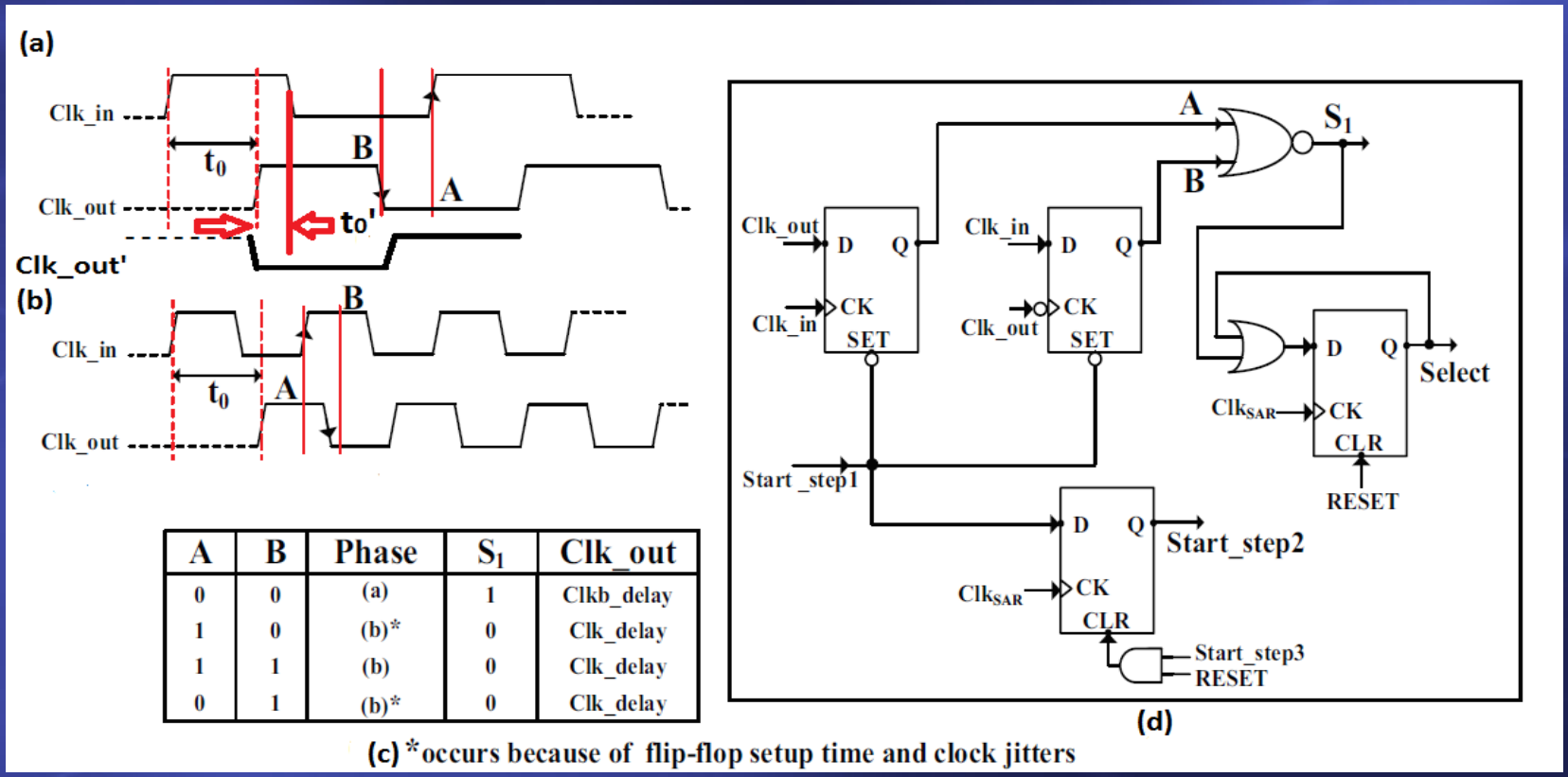


Figure 21 All-digital SAR based DLL [9]

Complementary Clock Select Unit



A	B	Phase	S_1	Clk_out
0	0	(a)	1	Clkb_delay
1	0	(b)*	0	Clk_delay
1	1	(b)	0	Clk_delay
0	1	(b)*	0	Clk_delay

(c) *occurs because of flip-flop setup time and clock jitters

Figure 22 (a) and (b) Phase relations between Clk_out and Clk_in
(c) CCSU decision table (d) CCSU circuit [9]

Delay Range Search

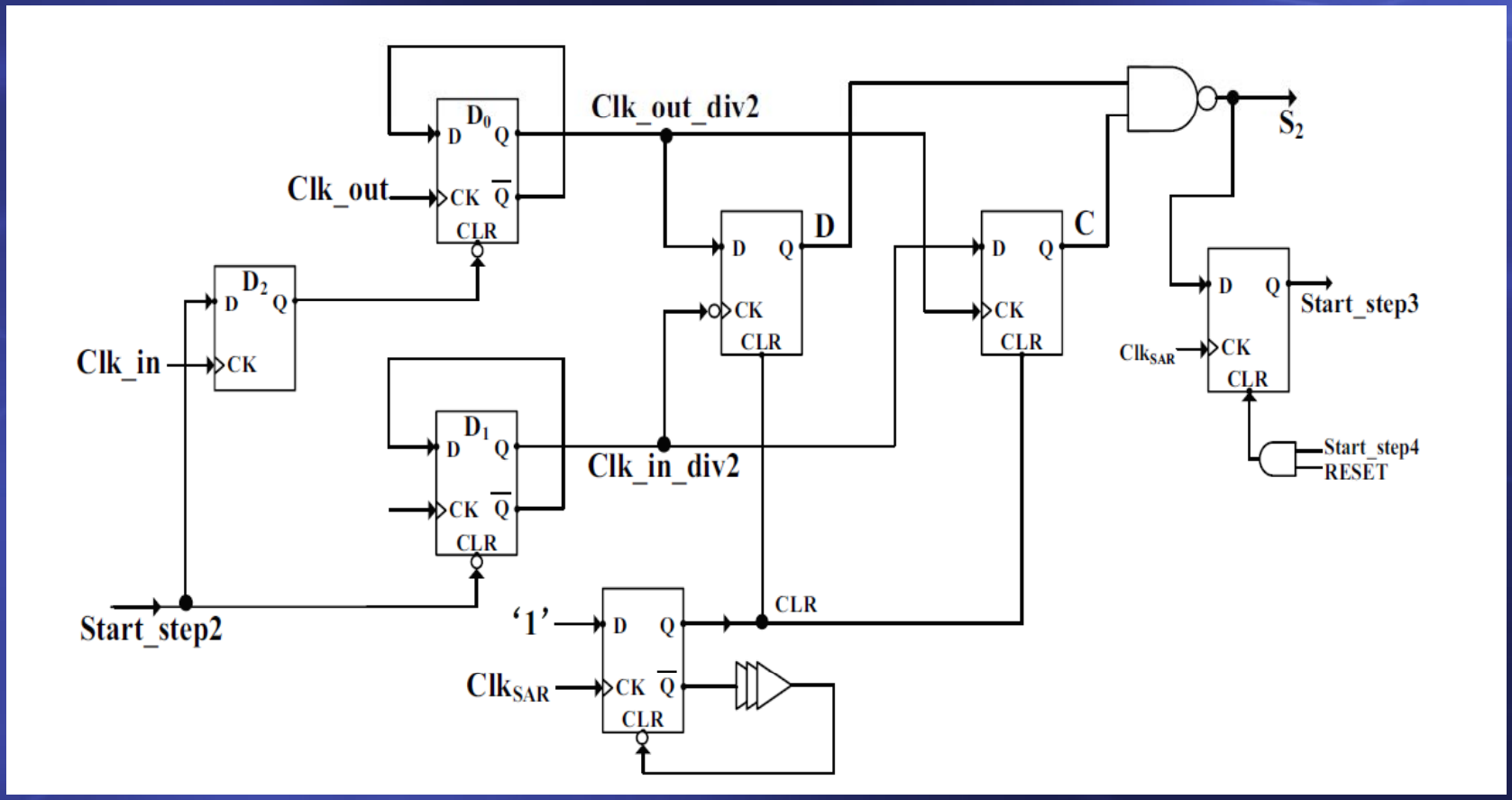


Figure 23 Delay range search circuit [9]

Delay Range Search Operation

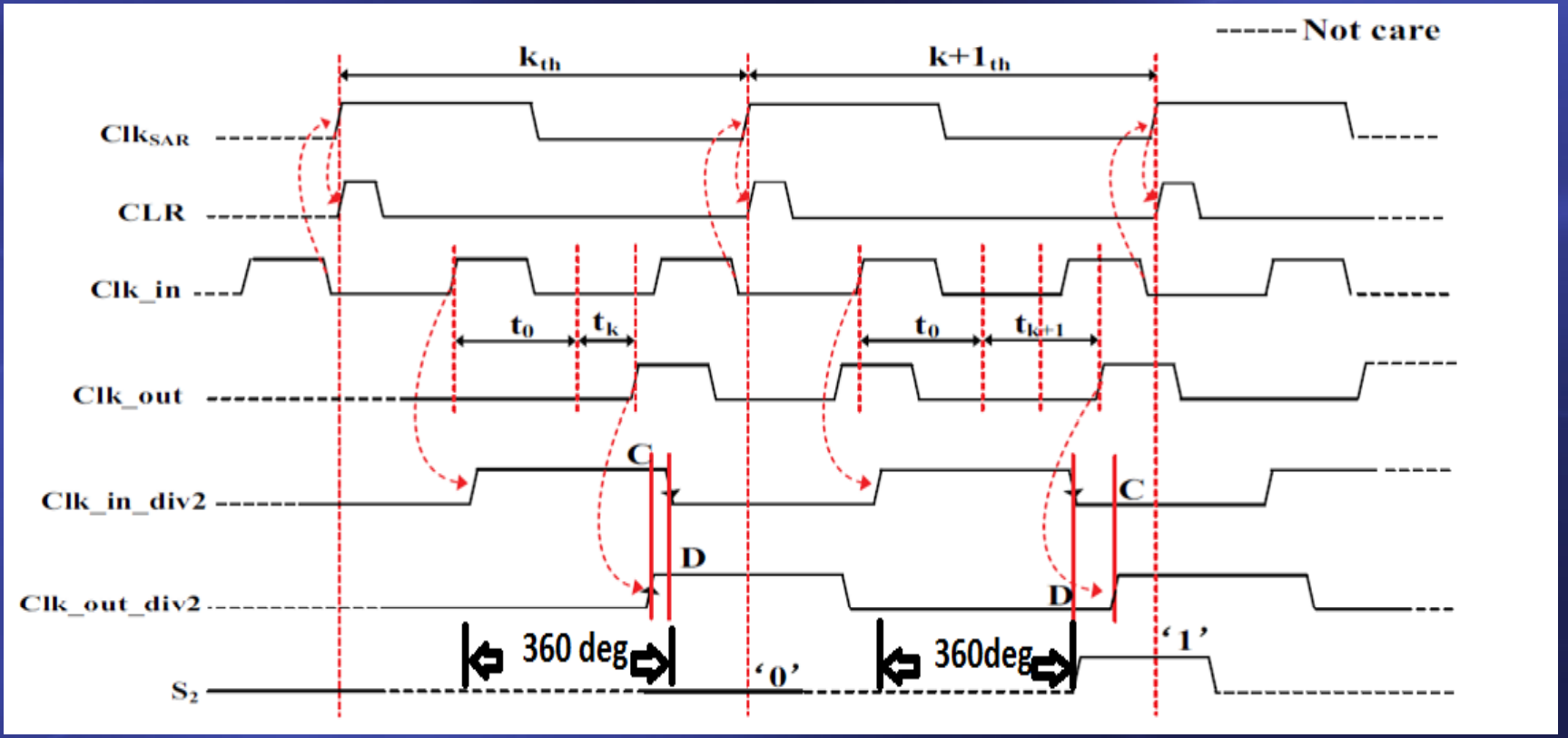


Figure 24 Delay range search timing diagram [9]

Delay Lines

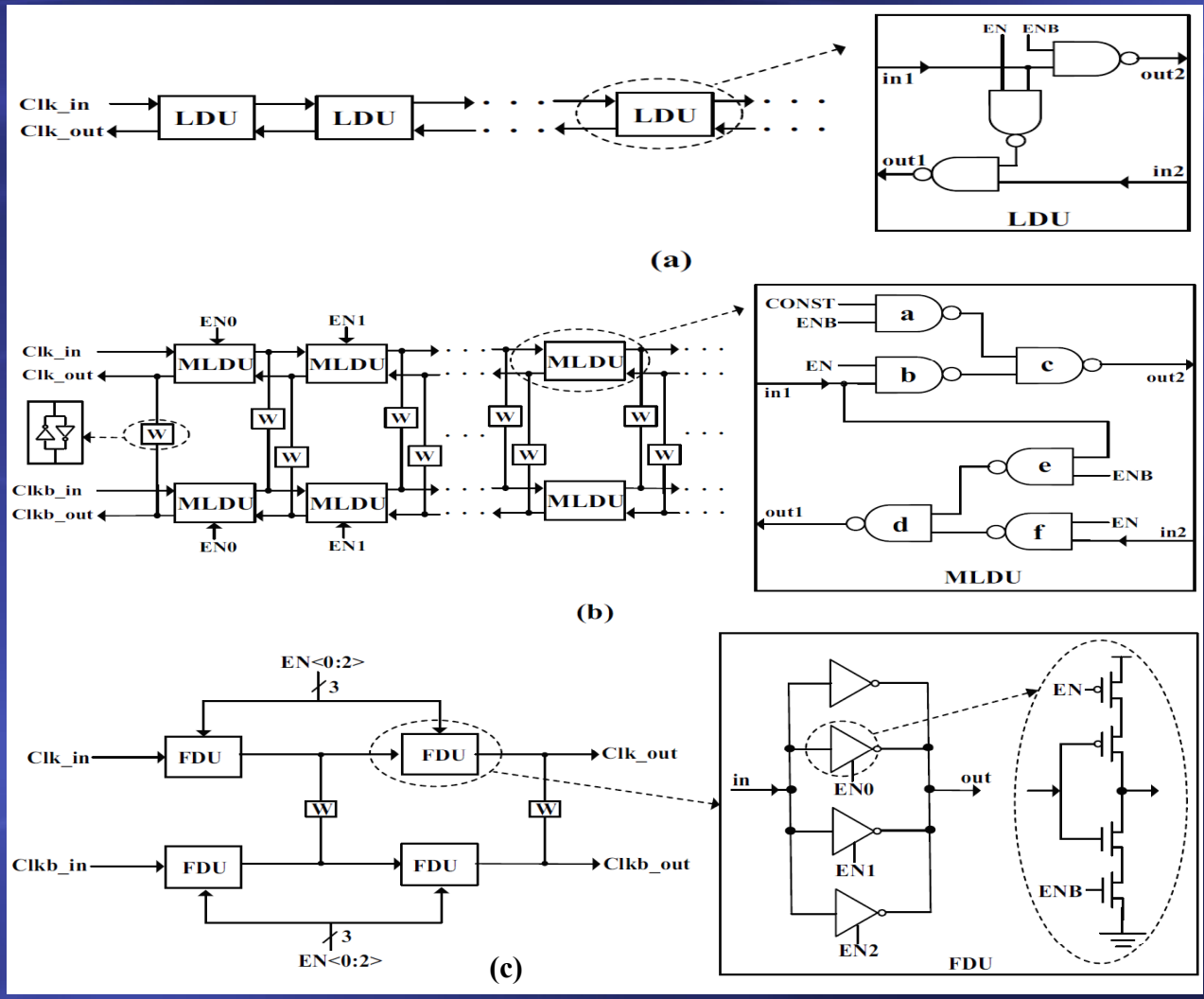


Figure 25 (a) Lattice delay line (b) Modified lattice delay line (c) Fine delay [9]

9 bit-SAR

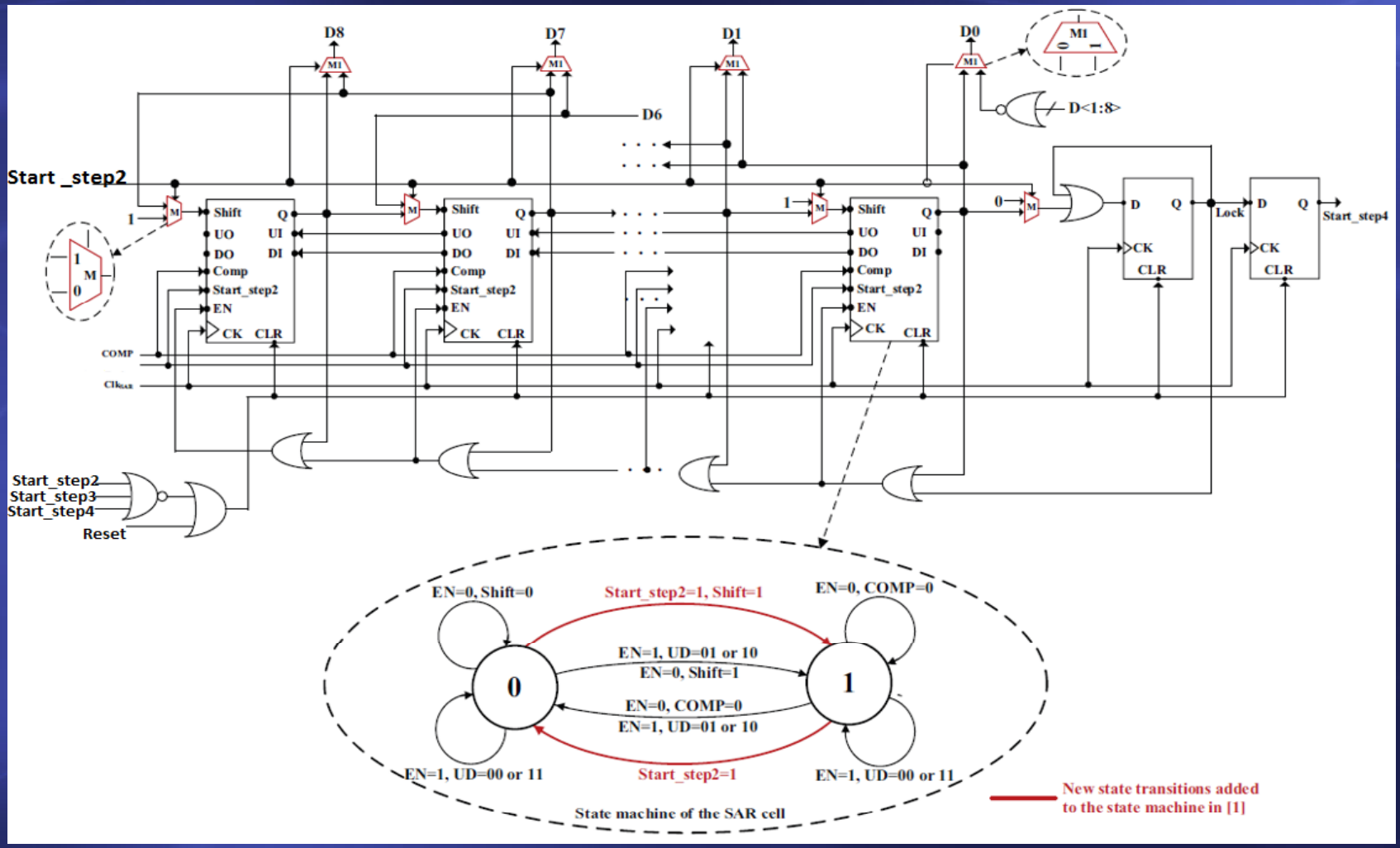
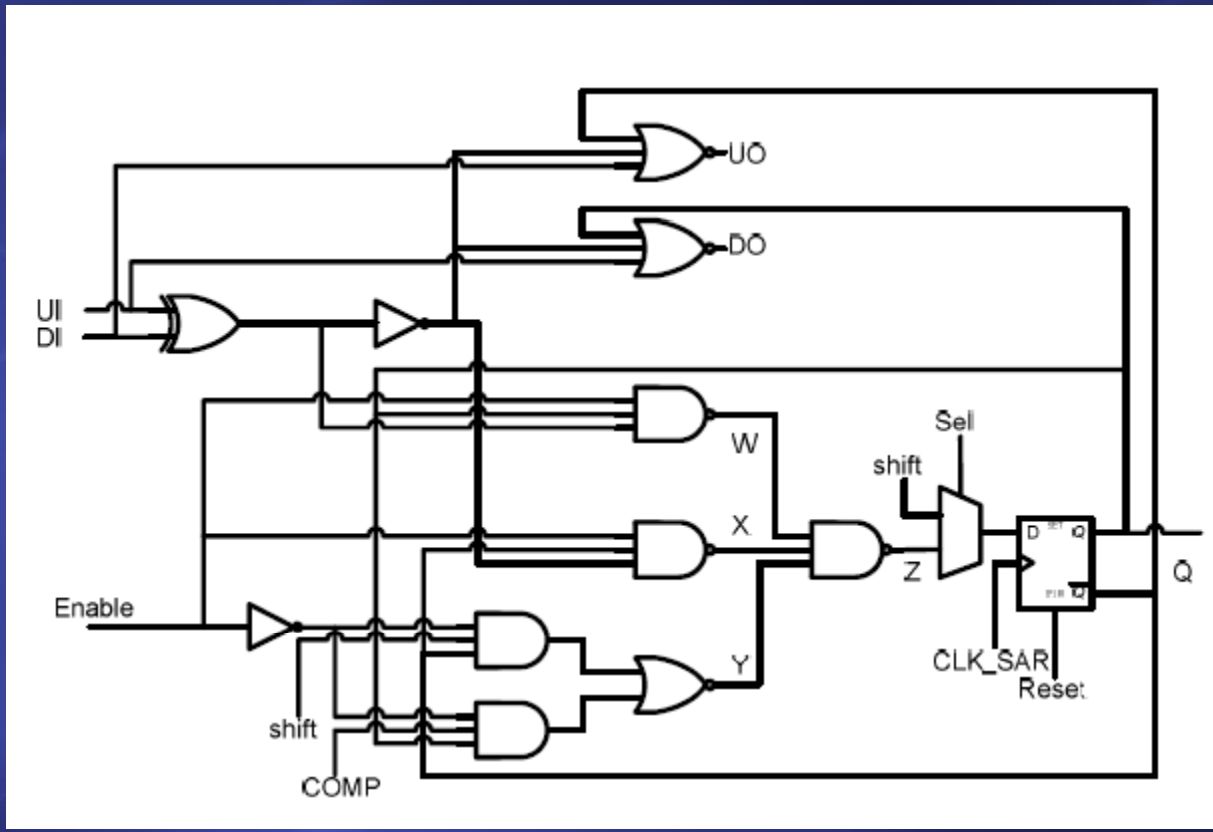


Figure 26 9-bit configurable SAR unit [9]

Shift-Counting SAR cell (SCSAR)



2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

2 Input EXOR gate		
A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Figure 27 Shift-counting SAR cell [10]

QUESTIONS ?

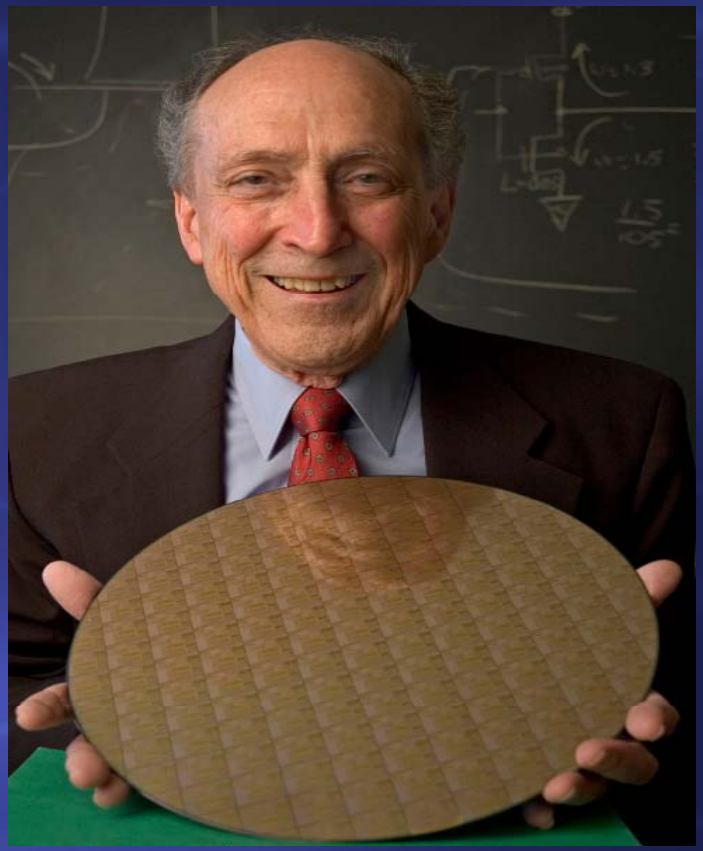


Figure 28 Robert H. Dennard [11]

References

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- [2] “Double Data Rate (DDR) SDRAM”, 512Mb: x4, x8, x16 DDR SDRAM Features, Micron Technology, Inc, 2000
- [3] Feng Lin, J. Miller, A. Schoenfeld, M. Ma and R. Jacob Baker, “A register-controlled symmetrical DLL for double-data-rate DRAM,” in *IEEE Journal of Solid-State Circuits*, vol. 34, no. 4, pp. 565-568, Apr 1999
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