OPERATION OF DIMM'S USING DDR4

ECG721 (Memory Circuit Design)

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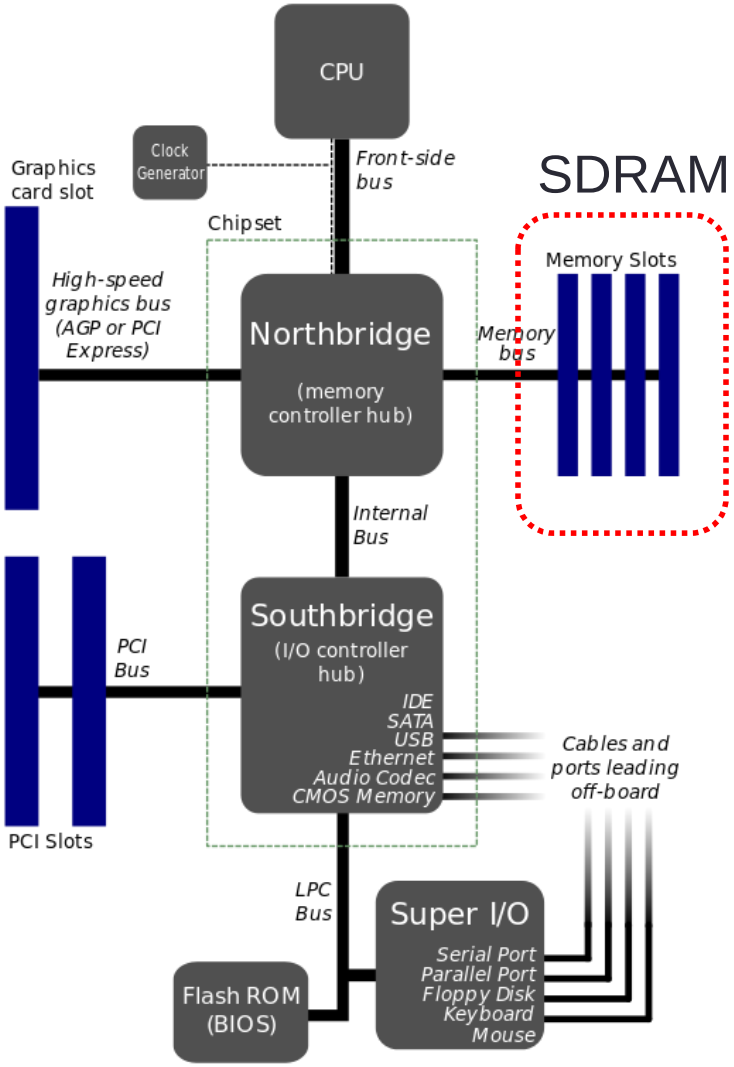
Outline

- Computer memory organization
- DDR interface
- DDR4 advantages
- DDR4 techniques
- Types of DIMM
- The future

Memory terminologies

- DDR – Double Data Rate
  - Data changes on both rising and falling edge
- SDRAM – Synchronous DRAM
  - An input clock dictates input and output of data compared to Asynchronous DRAM which is dependent on the internal latencies
- Memory bank
  - Collection of small DRAM arrays which has its own peripheral circuitry
- Memory configuration - x4, x8
  - Memory is arranged such that 4 bits (for x4) are read from columns at a time from separate memory arrays in the same chip

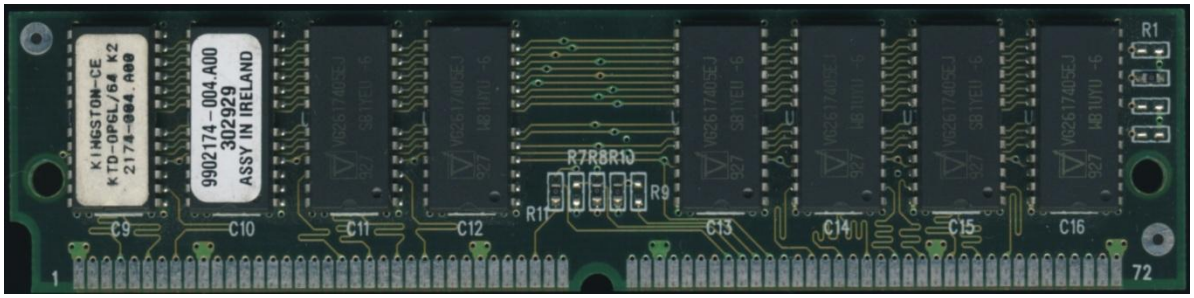
Computer memory organization

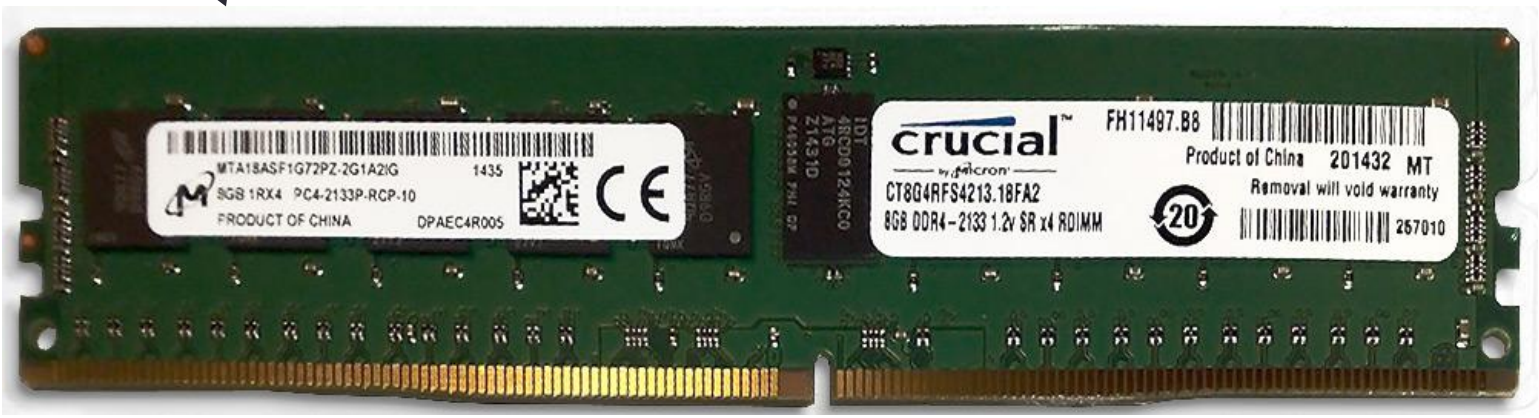


SDRAM DIMMs

Computer memory packaging evolution

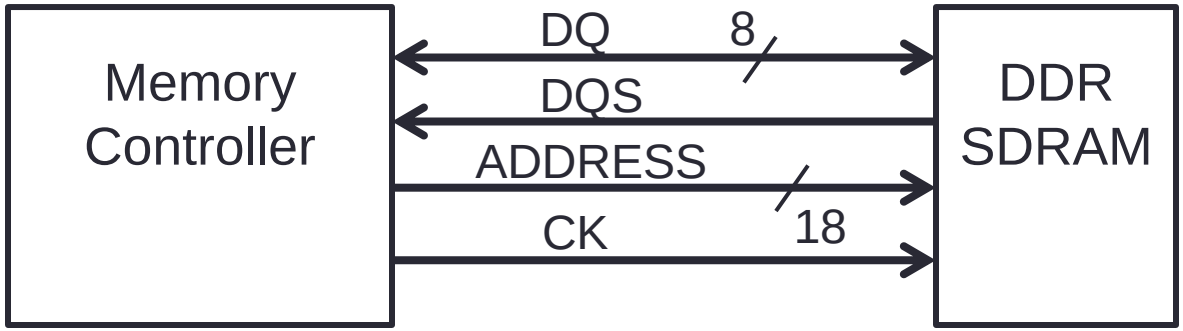
- Discrete DRAM memory chips
- SIMM (Single Inline Memory Module)
- DIMM (Dual Inline Memory Module)



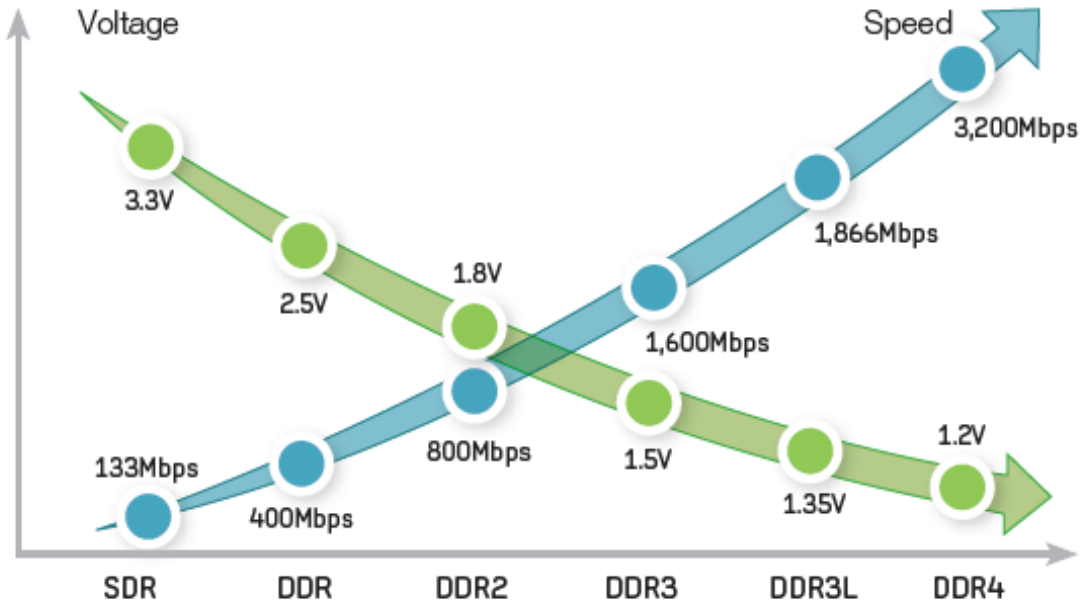


DDR interface block diagram

- Basic DDR SDRAM interface:



Why DDR4?



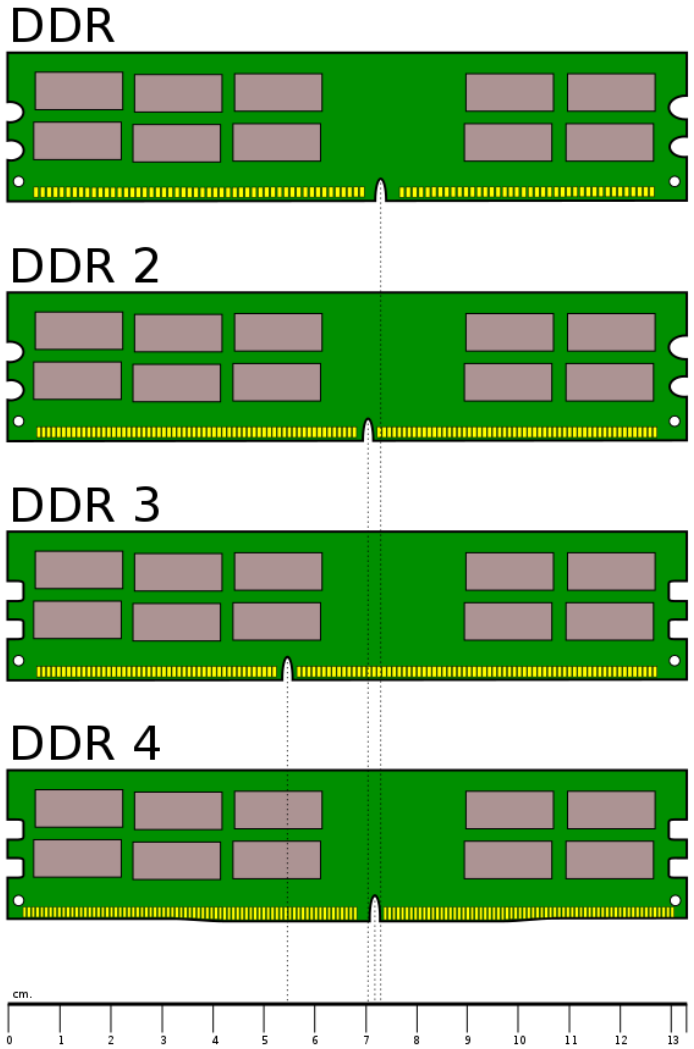
- Low voltage leading to low power
- Higher data transfer speeds
- Higher module density
- Maximum theoretical capacity per DIMM of 512GiB

DDR comparison

	DDR1	DDR2	DDR3	DDR4
VDD [V]	2.5	1.8	1.5	1.2
Data Rate [bps/pin]	200M~400M	400M~800M	800M~2.1G	1.6G~3.2G
Pre-Fetch	2 bit	4 bit	8 bit	8 bit
STROBE	Single DQS	Differential DQS, DQSB		
Interface	SSTL_2	SSTL_18	SSTL_15	POD_12
New Feature		▪OCD calibration ▪ODT	▪Dynamic ODT ▪ZQ calibration ▪Write leveling	▪CA parity ▪DBI*, CRC* ▪Gear down ▪CAL* ▪ PDA* ▪FGREF * ▪ TCAR* ▪Bank grouping

* DBI: Data bus inversion
* CRC: Cyclic redundancy check
* CAL: Command address latency
* PDA: Per DRAM addressability
* FGREF: Fine granularity refresh
* TCAR: Temperature controlled array refresh

DDR module physical comparison



- DDR4 modules feature a curved edge to help with insertion and alleviate stress on the PCB during memory insertion

DDR4 speed grades

Standard name	Memory clock (MHz)	I/O bus clock (MHz)	Data rate (MT/s)	Module name	Peak transfer rate (MB/s)	Timings, CL-tRCD-tRP	CAS latency (ns)
DDR4-1600J* DDR4-1600K DDR4-1600L	200	800	1600	PC4-12800	12800	10-10-10 11-11-11 12-12-12	12.5 13.75 15
DDR4-1866L* DDR4-1866M DDR4-1866N	233.33	933.33	1866.67	PC4-14900	14933.33	12-12-12 13-13-13 14-14-14	12.857 13.929 15
DDR4-2133N* DDR4-2133P DDR4-2133R	266.67	1066.67	2133.33	PC4-17000	17066.67	14-14-14 15-15-15 16-16-16	13.125 14.063 15
DDR4-2400P* DDR4-2400R DDR4-2400U	300	1200	2400	PC4-19200	19200	15-15-15 16-16-16 18-18-18	12.5 13.33 15
DDR4-3200	400	1600	3200	PC4-25600	25600		

DDR4 command set

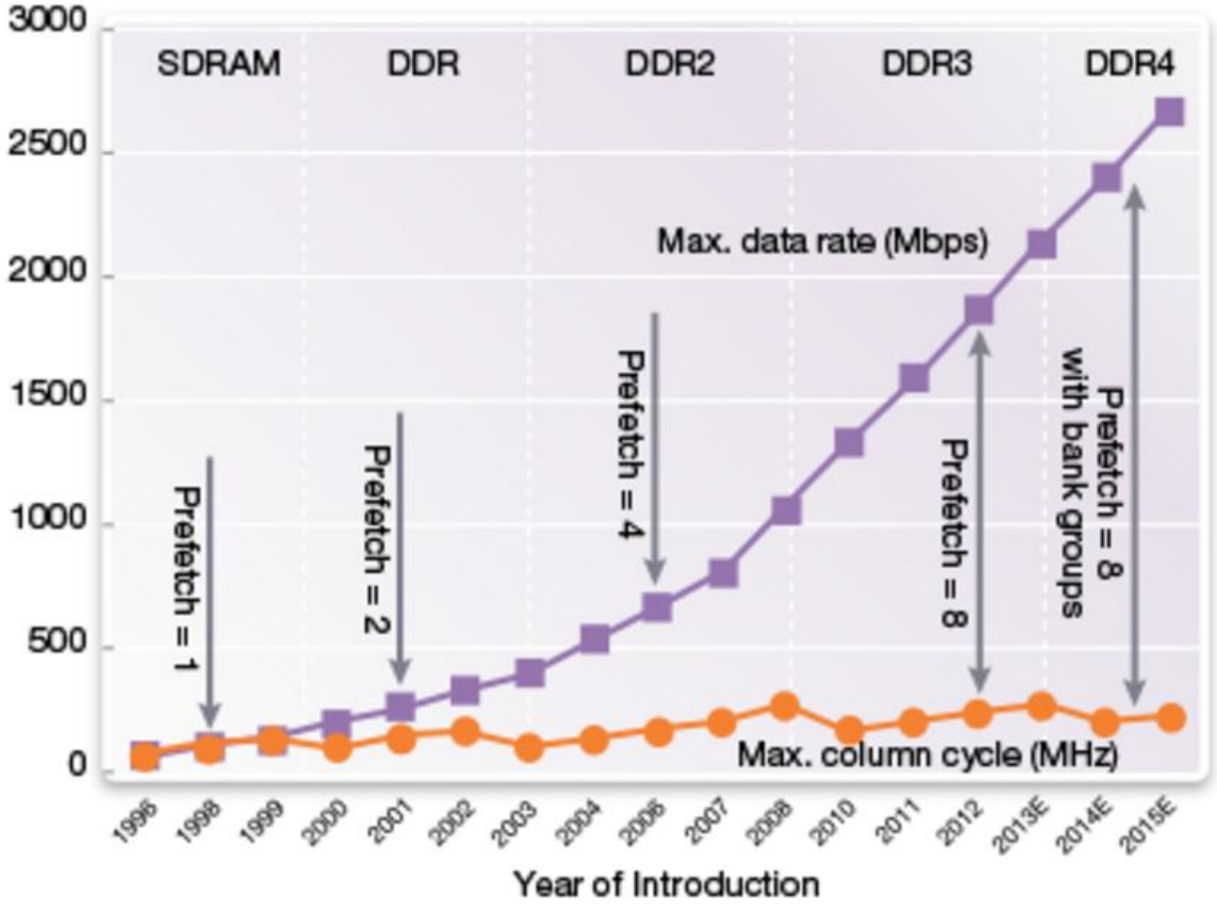
Command	$\overline{CS}$	BG1	BG0, BA1–0	$\overline{ACT}$	A17	A16 / $\overline{RAS}$	A15 / $\overline{CAS}$	A14 / $\overline{WE}$	A13	A12	A11	A10	A9–0
Deselect (no operation)	H	X											
Active (activate): open a row	L	Bank		L	Row address								
No operation	L	V		H	V	H	H	H	V				
ZQ calibration	L	V		H	V	H	H	L	V			Long	V
Read (BC, burst chop)	L	Bank		H	V	H	L	H	V	BC	V	AP	Column
Write (AP, auto-precharge)	L	Bank		H	V	H	L	L	V	BC	V	AP	Column
Unassigned, reserved	L	L		H	V	L	H	H	L				
Precharge all banks	L	V		H	V	L	H	L	V			H	V
Precharge one bank	L	Bank		H	V	L	H	L	V			L	V
Refresh	L	V		H	V	L	L	H	V				
Mode register set (MR0–MR6)	L	L	Register	H	L	L	L	L	L	Data			

Signal level (H, high · L, low · V, either low or high, a valid signal · X, irrelevant) · Logic level (Active · Inactive · Not interpreted)

DDR4 techniques for high-speed

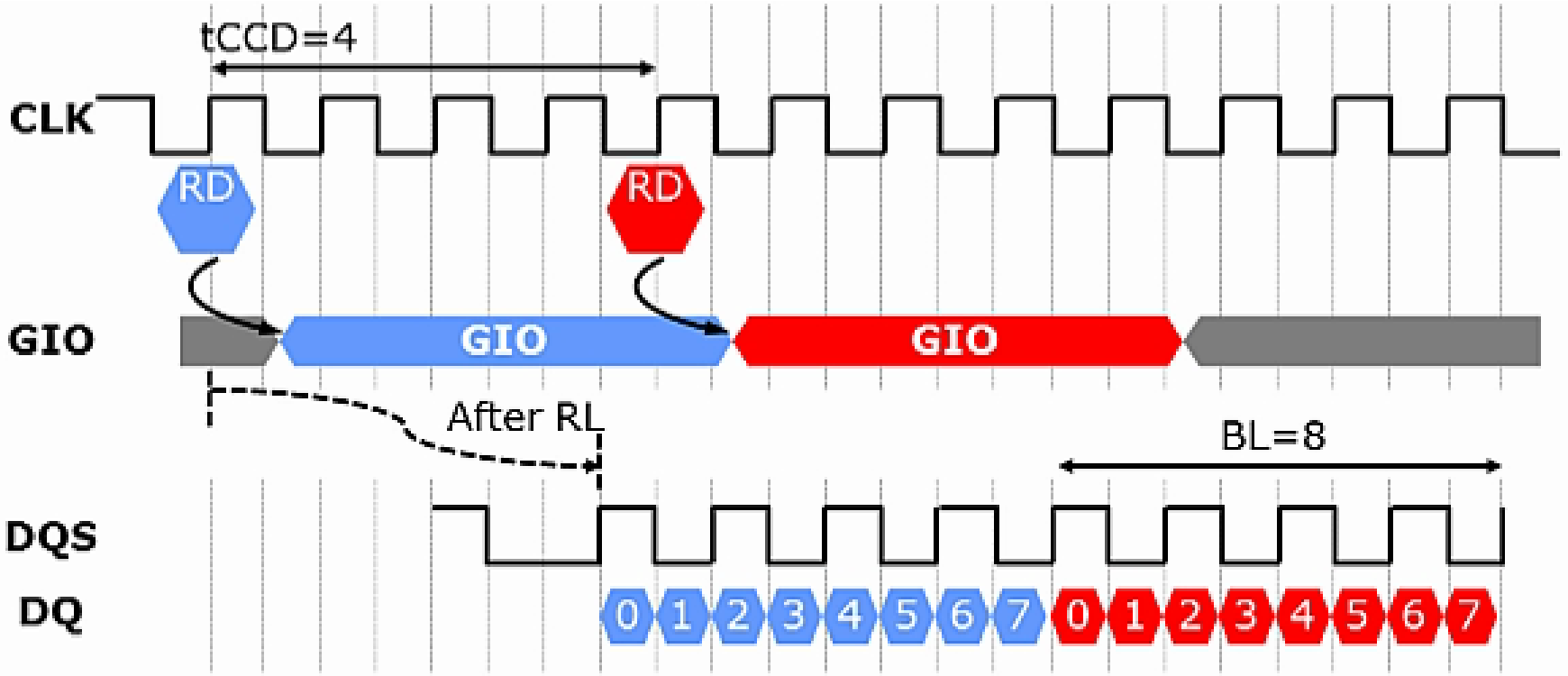
- Prefetch/burst-length
- Bank groups
- Smaller row sizes eases bank switching

Prefetch



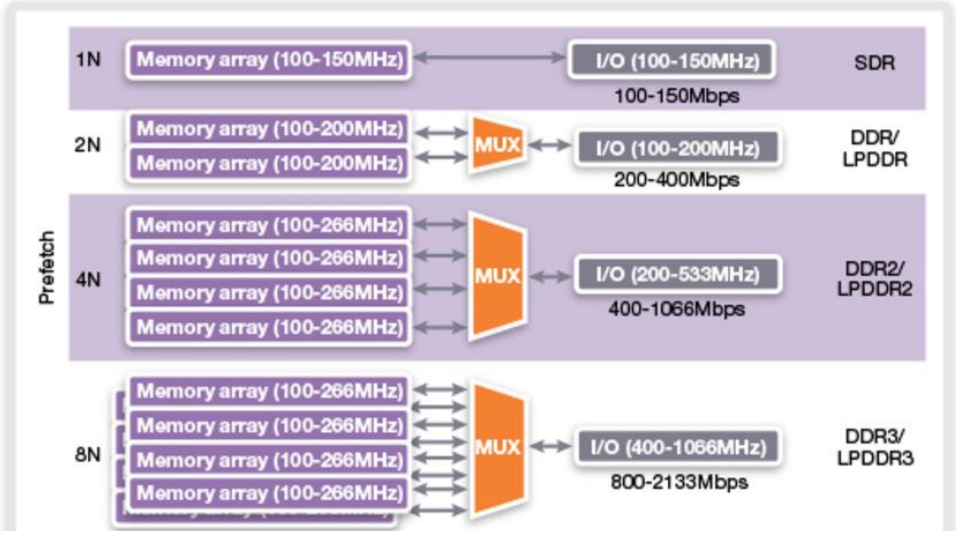
- Number of data words fetched for a single column command
- Prefetch is used to increase the data input/output rate even when the core memory speed remains same

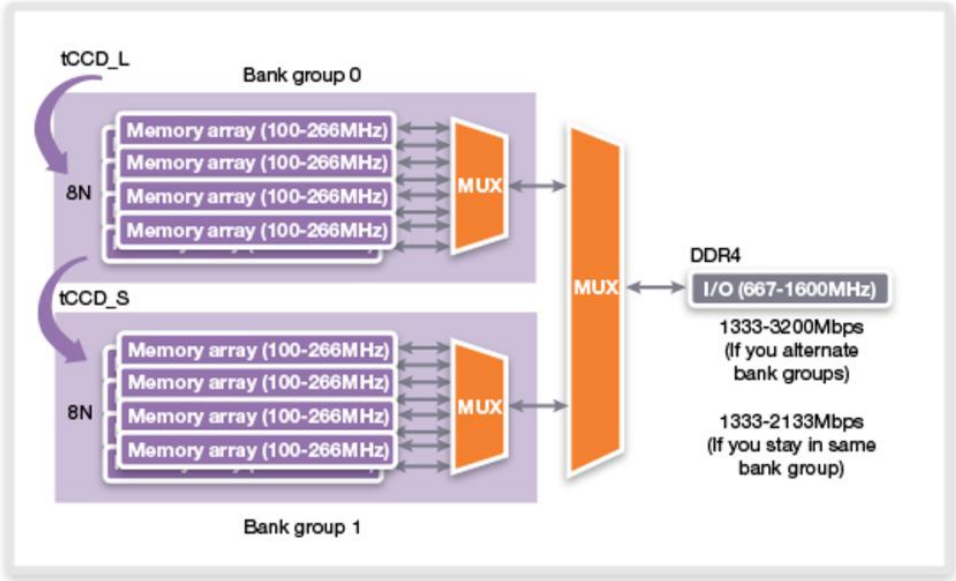
Prefetch (DDR3)



- tCCD = Time between CAS to CAS commands

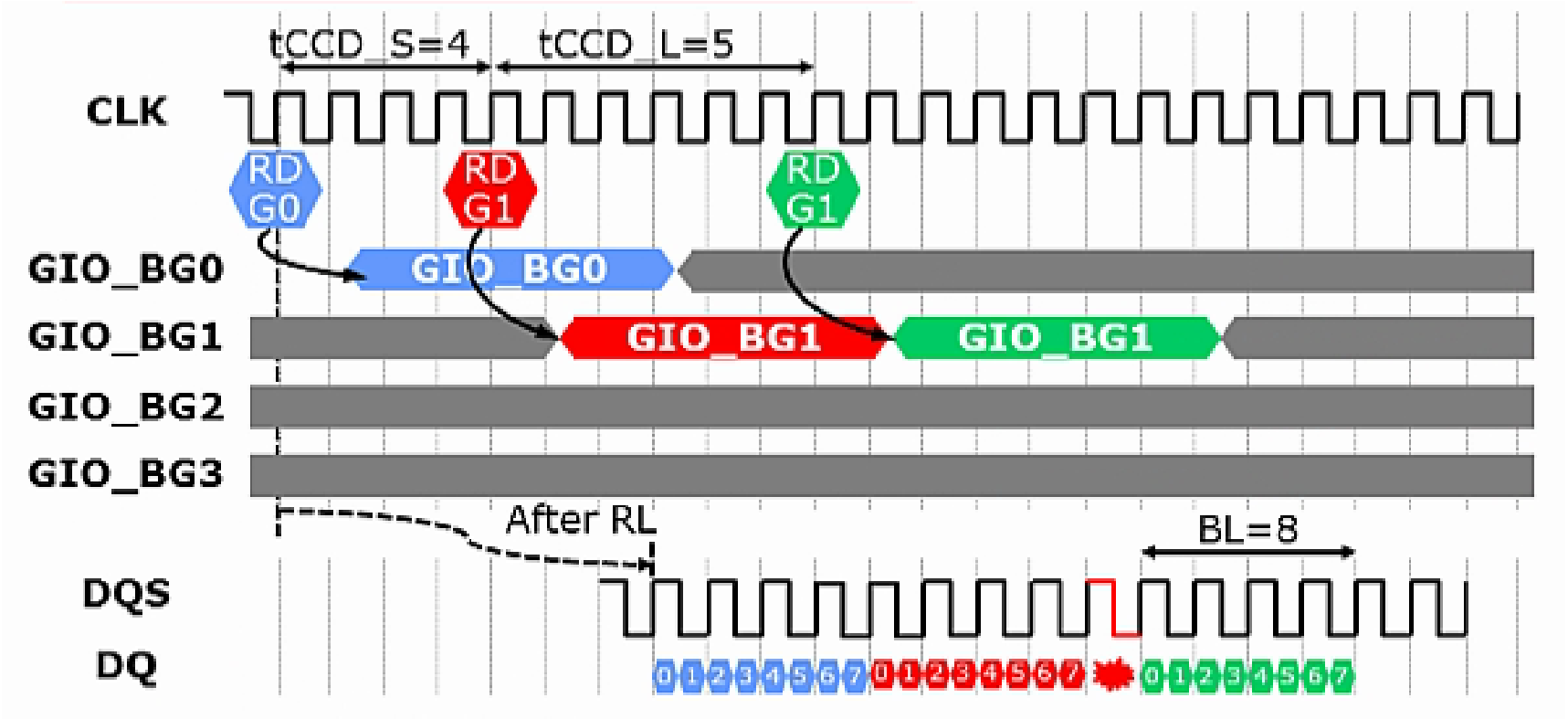
Prefetch and Bank groups





- DDR4 has 8n prefetch but uses bank groups to increase throughput
- Data should be read/written to different bank groups alternately to take advantage of lower tCCD_S

Prefetch (DDR4)

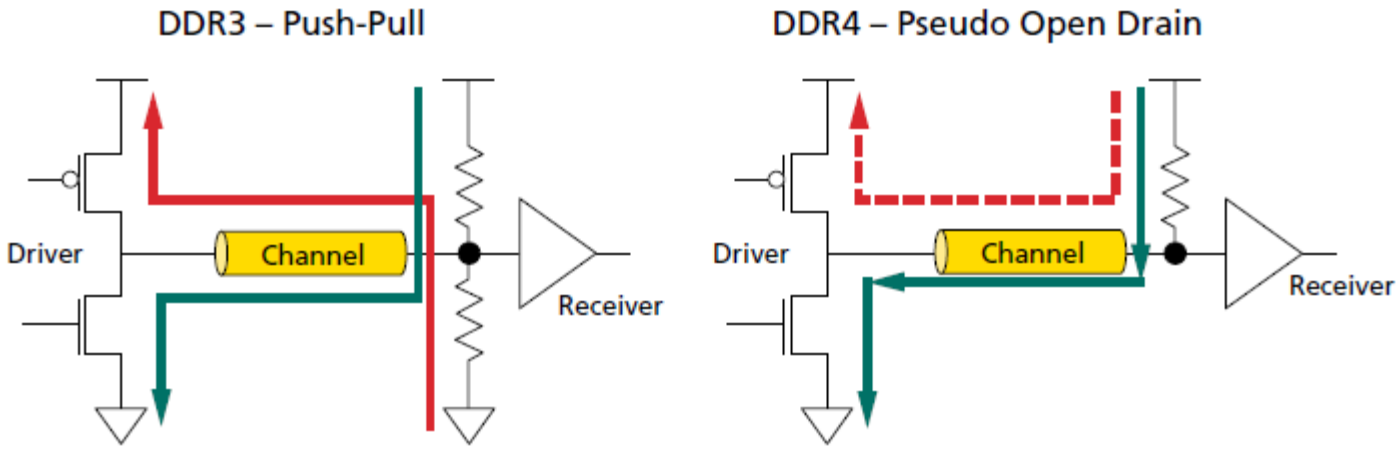


- tCCD_S = tCCD if data is prefetched from different bank groups
- tCCD_L = tCCD if data is in same bank group

Techniques for low power

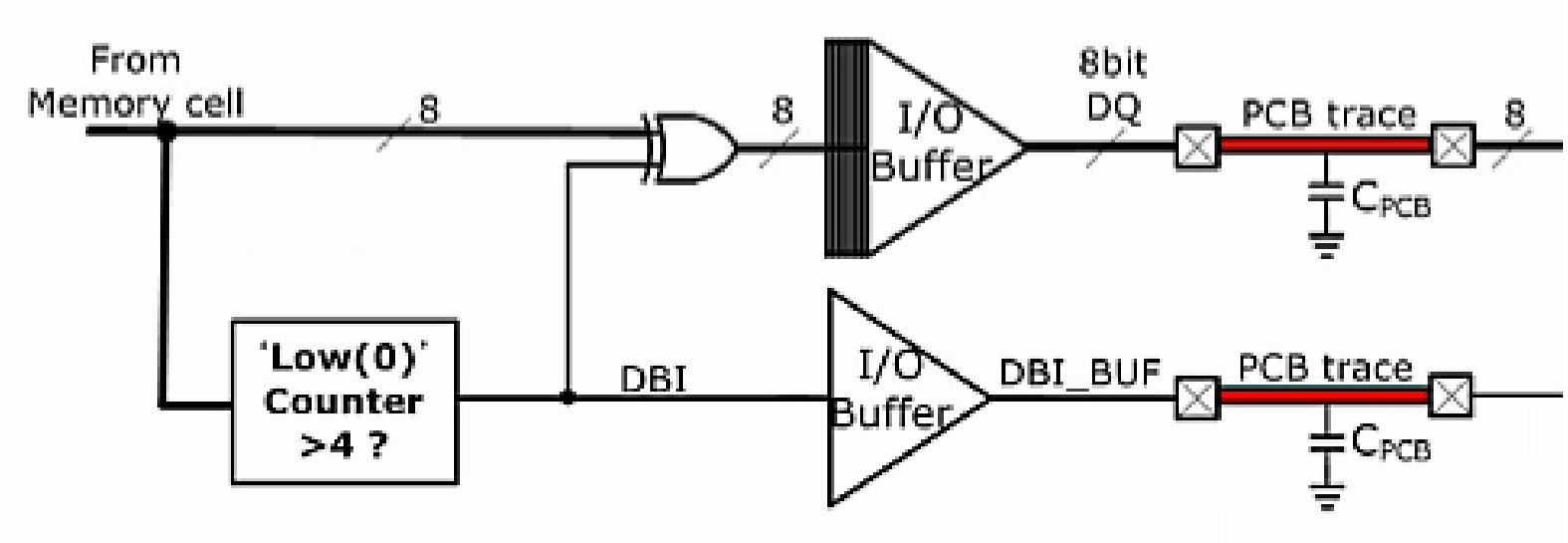
- Reduced VDDQ (power supply voltage)
- POD12 (Pseudo Open Drain at 1.2V)
- DBI (Data Bus Inversion)
- Smaller row sizes reduces activation currents

POD12 (Pseudo Open Drain 1.2V)



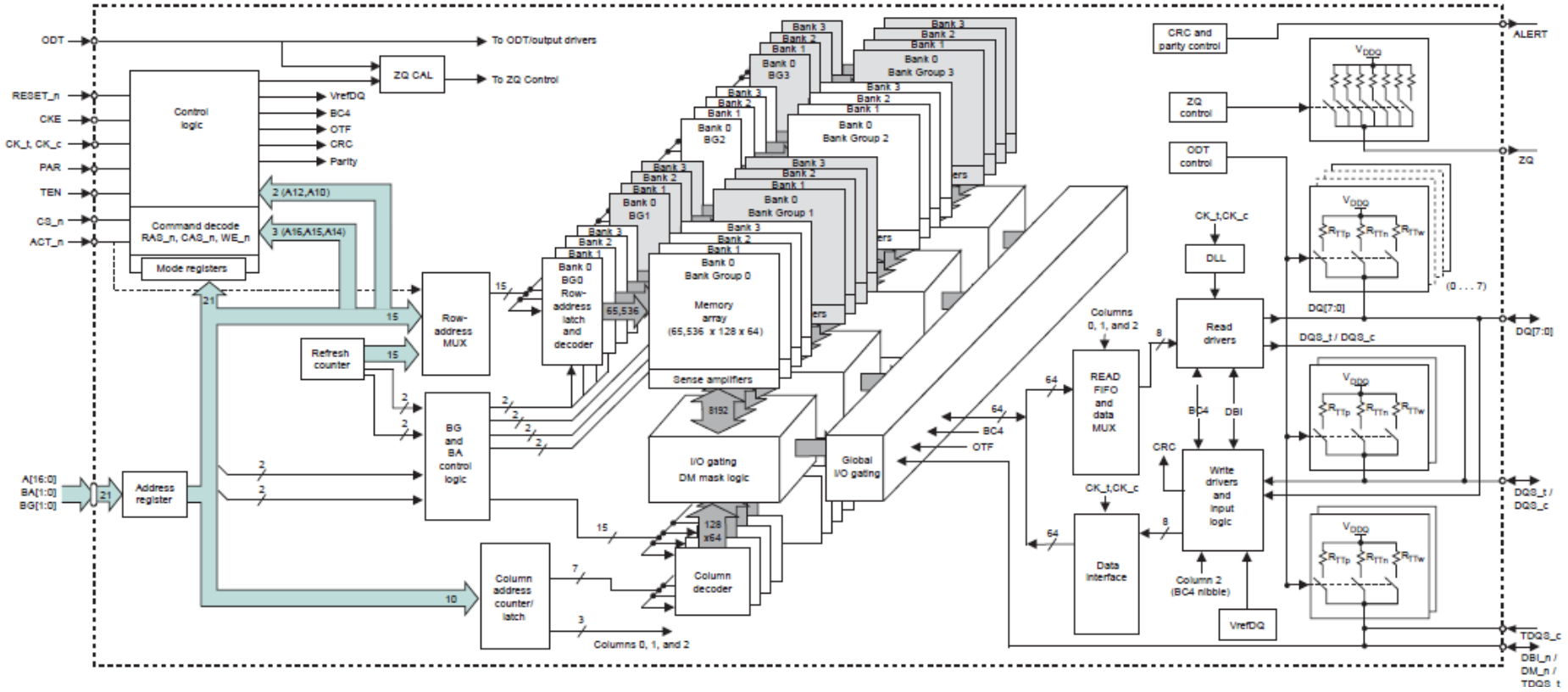
- POD enables reduced switching current when driving data since only 0's consume power
- Additional switching current savings can be realized with DBI enabled
- JEDEC JESD8-24 standard

DBI (Data Bus Inversion)



- Adopted for power savings
- DQ inverted if the data byte contains more than 4 0's

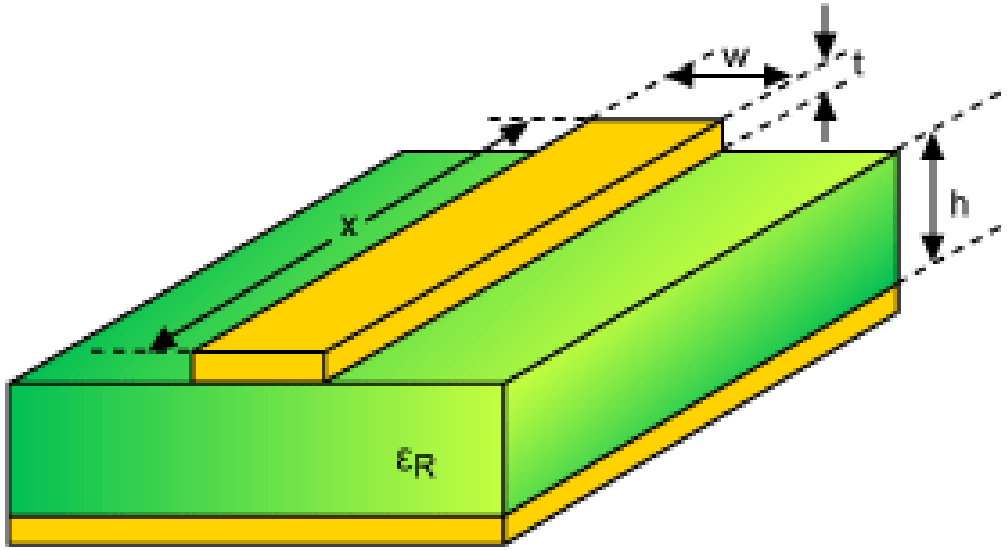
DDR4 SDRAM chip block diagram



Symbol	Parameter	Rating			Unit	Notes
		Min	Typ	Max		
V_{DD}	Supply voltage	1.14	1.2	1.26	V	1, 2, 3, 4, 5
V_{DDQ}	Supply voltage for output	1.14	1.2	1.26	V	1, 2, 6
V_{PP}	Wordline supply voltage	2.375	2.5	2.750	V	7

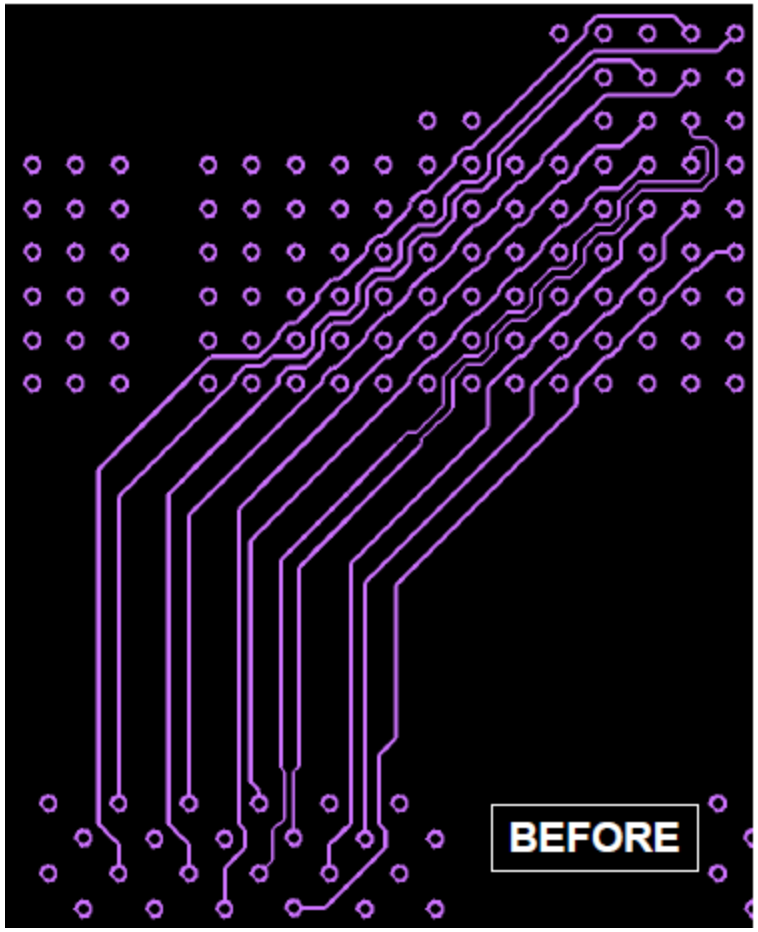
PCB microstrip transmission line

- DQ[x:0] and DQS should reach at the same time
- Any wire carrying an AC signal whose period is less than the propagation delay of the wire needs to be considered as a transmission line
- PCB microstrip signal speed = 2 inch/ns
- Target impedance for DDR4 microstrip transmission line is 100 to 120 ohms

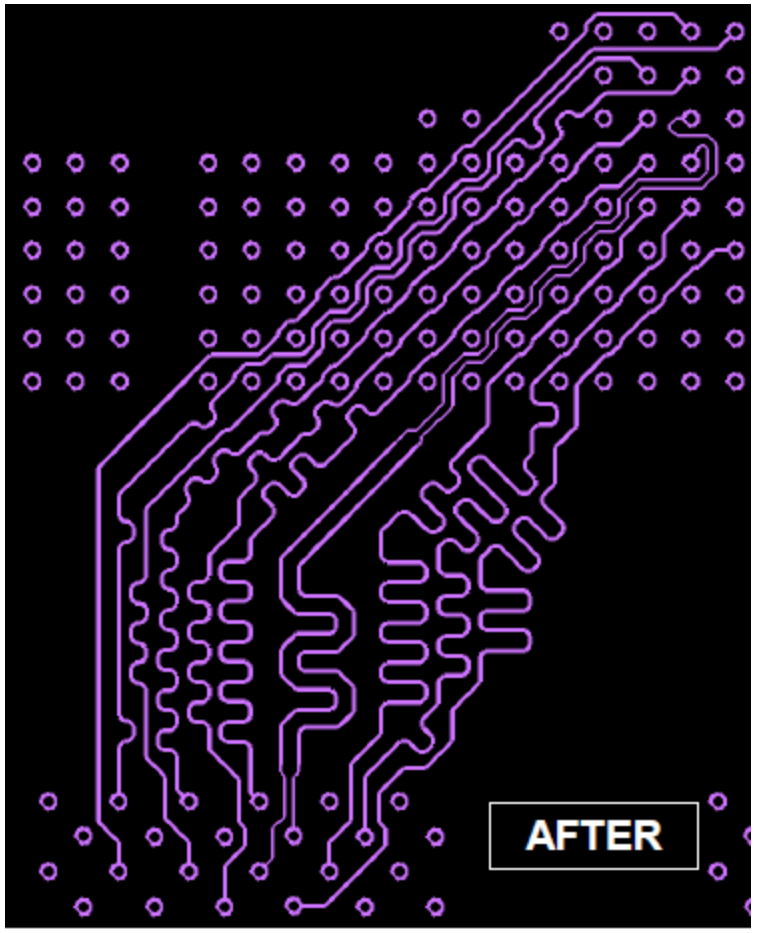


PCB trace length matching

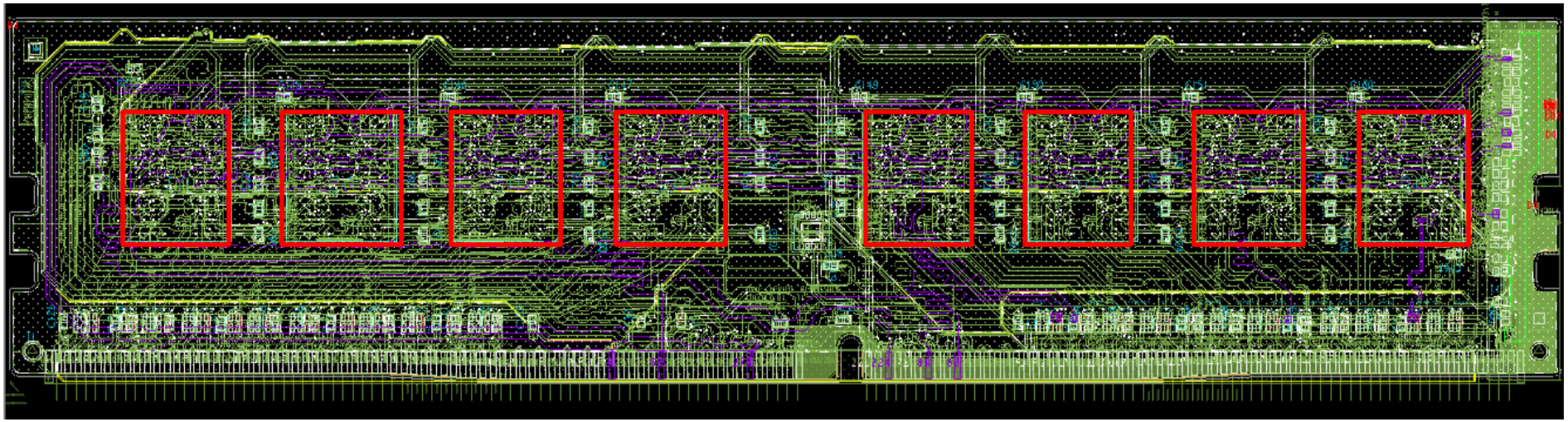
Unmatched



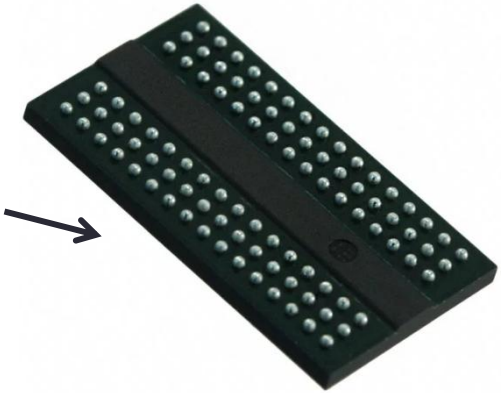
Matched



DDR4 DIMM PCB



- 8 layer PCB
- 8 SDRAM chips
- FBGA footprint (Fine Pitch Ball Grid Array)



Types of DDR4 DIMM modules

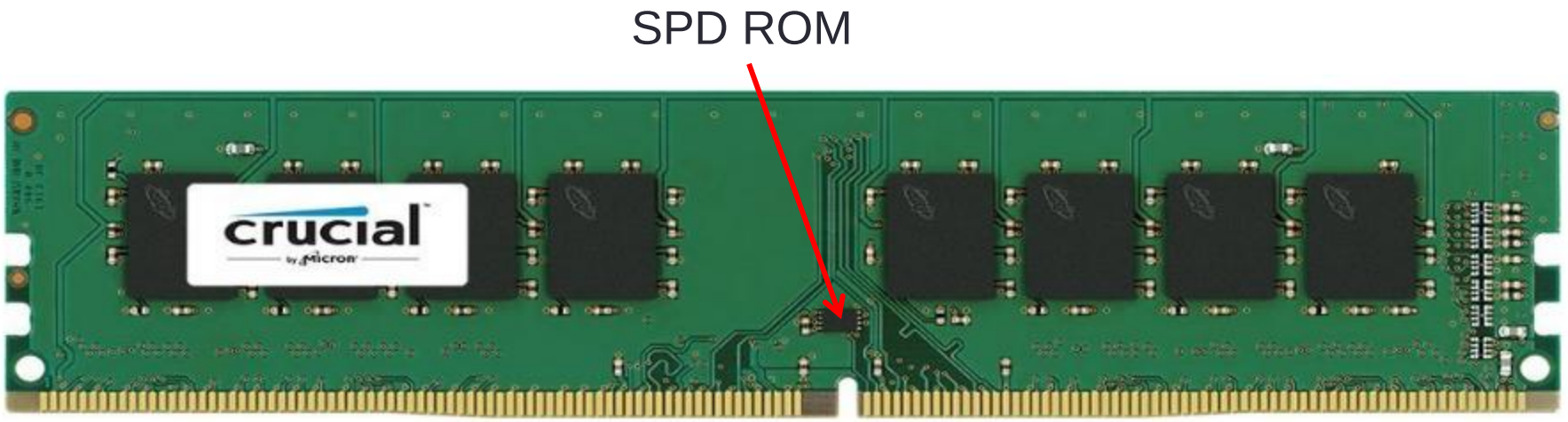
- Mainstream
  - UDIMM (Unbuffered DIMM)
  - LRDIMM (Load-reduced DIMM)
  - RDIMM (Registered DIMM)
  - FBDIMM (Fully-buffered DIMM)

  } Buffered memory

  - NVDIMM (Non-volatile DIMM)
- Physical sizes
  - DIMM
  - SODIMM (Small-outline DIMM)
  - VLP-DIMM (Very low profile DIMM)
  - Mini-DIMM

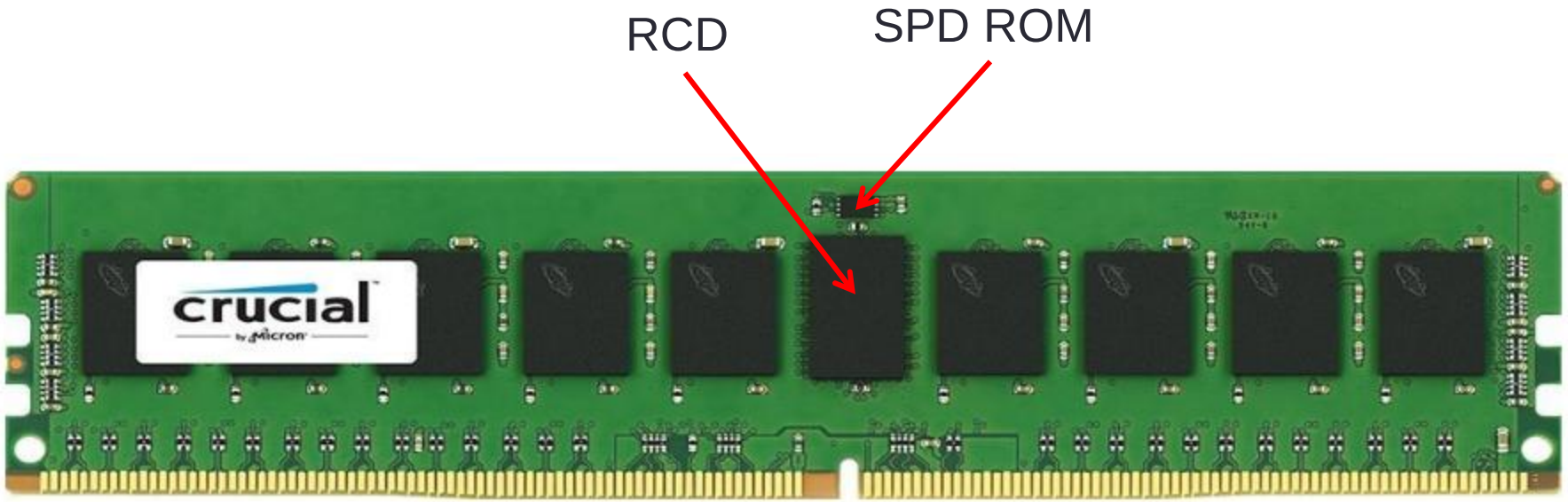
UDIMM (Unregistered DIMM)

- Regular DIMMs used in desktop computers
- Memory controller interfaces directly to SDRAM chips
- SPD (Serial Presence Detect) ROM provides information about the DIMM during power on self test



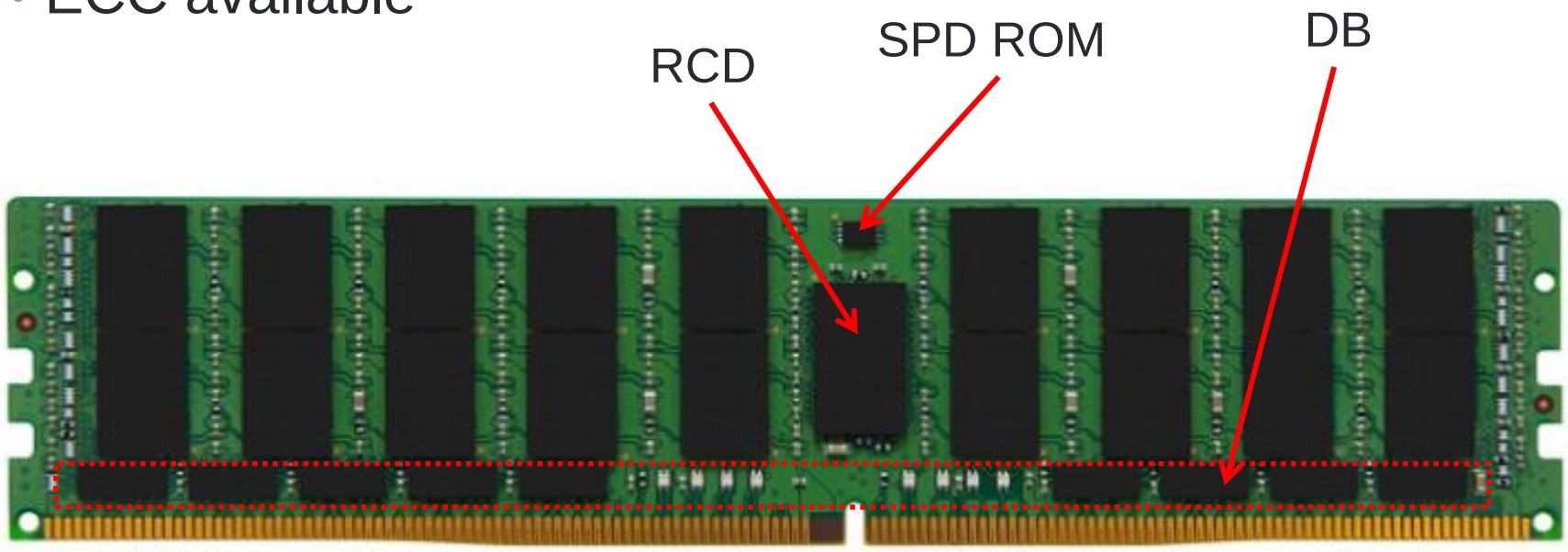
RDIMM (Registered DIMM)

- Buffers command and address signals. Data signals connect unbuffered
- Contains RCD (Registering Clock Driver)
- More robust than UDIMMs
- ECC option available



LRDIMM (Load-Reduced DIMM)

- Trades-off latency for capacity
- Buffers both data and command/address lines
- Contains RCD (Registering Clock Driver) and DB (Data Buffer) for distributed buffering of data
- ECC available



FB-DIMM (Fully-Buffered DIMM)

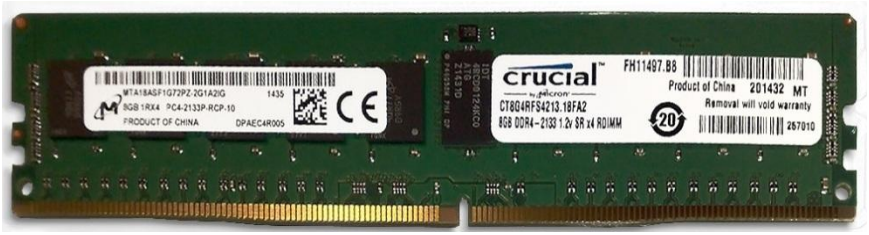
- Scalable to very large memory sizes. Trades-off latency and speed
- Uses serial data link to transfer data
- Additional logic on DIMM converts serial to parallel
- JEDEC JESD206
- Used in servers

NVDIMM (Non-volatile DIMM)

- DDR4 DIMMs can contain memory other than DRAM
- Called “Hybrid Memory Modules”
- JEDEC JESD248 standard for NAND backed DRAM
- Another example is Intel and Micron’s 3D Xpoint DDR4 DIMM
- Mainly used in servers

DDR4 DIMM sizes

UDIMM/RDIMM/LRDIMM



SODIMM/
SORDIMM

VLP-UDIMM/VLP-RDIMM

VLP-Mini UDIMM

Implementing a DDR4 DIMM system

- JEDEC standards dictate almost all aspects of DDR4 system which ensures interoperability
- List of standards
  - JESD79-4 : DDR4 SDRAM specs
  - JESD8-24 : POD12
  - JESD82-32 : DB specs
  - JESD82-31 : RCD specs
  - JESD248 : NVDIMM specs
  - SPD4.1.2 : SPD specs
  - Etc…
- Ad-hoc standards such as DFI (DDR PHY Interface)

Other types of DDR memory

- GDDR – Graphics DDR
  - Optimized for large bandwidth and soldered on board. Has large IO like x16/x32
  - Used in conjunction with GPUs
- LPDDR – Low Power DDR (also called Mobile DDR)
  - Optimized for low power consumption and used as PoP or SiP
  - Used in mobile devices

The future

- DDR4 is the most cutting edge memory protocol standard to date (as of April 2017)
- DDR5 development in progress. JEDEC is working on the specification and plans to release in 2018 (estimated). DIMMs available for end user purchase in 2020
- Hybrid Memory Cube seeks to extend the life of DRAM by using stacked dies connected by TSVs
- Memory technologies like 3D Xpoint, PCM, RRAM etc. to be the successors (supposedly)


"That's all Folks!"

References

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- https://en.wikipedia.org/wiki/Northbridge_(computing)
- https://en.wikipedia.org/wiki/NVDIMM

QUESTIONS?